Published by IOP Publishing for Sissa Medialab

Received: *November 5, 2025*
Accepted: *January 27, 2026*
Published: *March 12, 2026*

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

Characterization of the bPOL48V GaN DC-DC buck converter for R&D on future particle collider power systems

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Abstract: The bPOL48V is a DC-DC Point-Of-Load (POL) buck converter developed at CERN and characterized at RWTH Aachen University under the DRD7 program. The bPOL48V is designed to address power distribution challenges of next-generation high-energy physics experiments by enabling power delivery at higher voltages and lower currents in supply cables, thereby minimizing power losses. It supports a higher input voltage (48V) compared to existing solutions by using a CERN-designed GaN controller with a commercial GaN power stage. The bPOL48V has been characterized in various setups. Its performance results are presented, including efficiency, line and load regulation, performance as a function of temperature as well as emitted and conducted noise. As a case study, a CMS Phase-2 silicon strip module is powered by the bPOL48V, which allows operation at a higher input voltage and therefore at a higher conversion ratio.

Keywords: Particle detectors; Particle tracking detectors; Radiation-hard electronics

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https://doi.org/10.1088/1748-0221/21/03/C03021

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1 Introduction

Future high-energy particle colliders will require significant electrical power. Delivering this power over long cables at high current leads to Ohmic losses ($P_{\text{loss}} = R_{\text{cable}} \cdot I^2$). However, the reduction of cable resistance by increasing the copper cross-section is constrained, as the detector design imposes strict limits on the amount of material. To reduce these losses, it is of advantage to transport power at high voltage and low current, and to locally convert it to the voltage required by detector electronics using DC-DC buck converters. These converters step down the high input voltage to the low ASIC supply voltage on the detector.

Next-generation colliders, with lower ASIC voltages, stricter material budgets, and operation in extreme radiation and magnetic field environments, make power distribution increasingly challenging. The bPOL48V [1], developed by CERN's EP-ESE group, addresses these challenges. This DC-DC Point-of-Load (POL) buck converter enables localized voltage regulation by stepping down 48 V to an adjustable 5–24 V. Its performance is being characterized under the DRD7 Collaboration, a Detector R&D initiative focused on future particle physics electronics.

Currently, DC-DC converters are implemented for example on CMS Phase-2 silicon strip modules, which step down 12 V to 1.25 V. The bPOL48V supports higher conversion ratios, reducing losses. Key to the bPOL48V's performance is its use of Gallium Nitride (GaN) technology, with a radiation-hardened GaN controller ASIC (in silicon) developed at CERN and a commercial EPC2152 GaN power stage [2]. This design allows high-voltage operation, improved thermal performance, low conduction and switching losses, radiation tolerance up to 50 MRad and $4 \cdot 10^{14}$ n/cm^2 and $2.23 \cdot 10^{14}$ p/cm^2 (30 MeV proton beam), magnetic field compatibility above 4 T, and efficient operation with small PCB air-core inductors (200–500 nH) at switching frequencies of 0.5–3 MHz [3]. The bPOL48V including PCB has been provided to RWTH Aachen University for extensive characterization (section 2) and is used as a case study for integration tests with a CMS Phase-2 strip module [4] (section 3).

2 Characterization measurements

The bPOL48V characterized in this section has an output voltage of 12 V, a switching frequency of 2 MHz, six 47 µF output filter capacitors in parallel, and a PCB toroidal air-core inductor of 241 nH, as the strong magnetic field in the detector would saturate ferromagnetic cores.

2.1 Efficiency

The efficiency of the converter is one of its main characteristics. It is defined as the ratio of the output power to the input power. An automated measurement sets input voltages in a range of 25–48 V in steps of 1 V, and for each input voltage the output current is swept from 0.1 A to 5 A in steps of 0.1 A. For each combination, the corresponding input current and output voltage are measured, and the efficiency is calculated. The results are visualized as a 2D-histogram in figure 1. The bPOL48V reaches an efficiency around 90 % in a large working range.

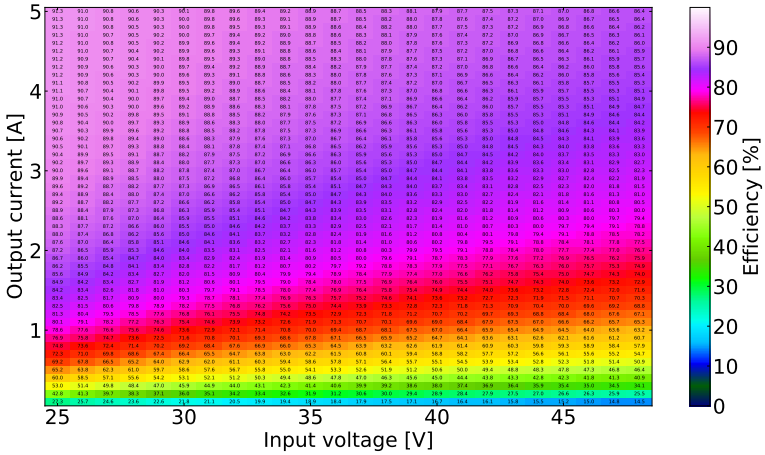

Figure 1. The efficiency of bPOL48V for different combination of input voltage and output current.

2.2 Stability and temperature dependence

An important characteristic of a DC-DC converter is its ability to maintain a constant output voltage despite changes in the input voltage at constant load. This is called line regulation, and is shown in figure 2 (left) for different loads at room temperature. It is quantified by taking the slope of each curve, giving the change in output voltage per 1 V change in input voltage. For the bPOL48V, this is approximately 0.004 V. The line regulation is measured at different air temperatures using a climate chamber. The air temperatures are set from +20 °C to − 20 °C in steps of 5 °C, for a constant output current of 2 A. The resulting curves at different temperatures are shown in figure 3 (left). The slope of each of these curves is determined and plotted against temperature in figure 3 (right). The slope increases with temperature, indicating better line regulation at lower temperatures.

The same process is applied to the load regulation, which is the ability of the DC-DC converter to maintain a constant output voltage despite changes in the output current, at constant input voltage. Figure 2 (right) shows the load regulation for different input voltages at room temperature. The slopes correspond to an output voltage change of approximately −0.011 V per 1 A change in output current. Load regulation is also measured in the climate chamber and shows a temperature dependence as well, but in contrast to line regulation, it improves at higher temperatures.

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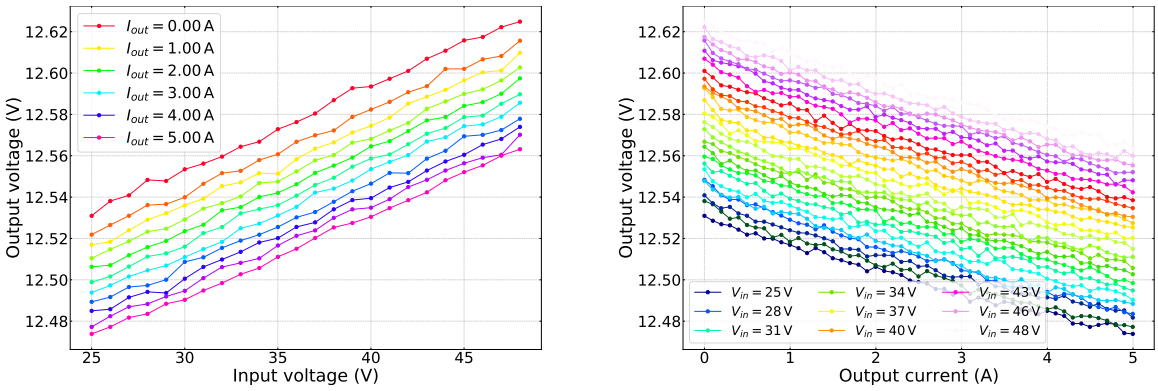

Figure 2. Line regulation curves at room temperature (left). Load regulation curves at room temperature (right).

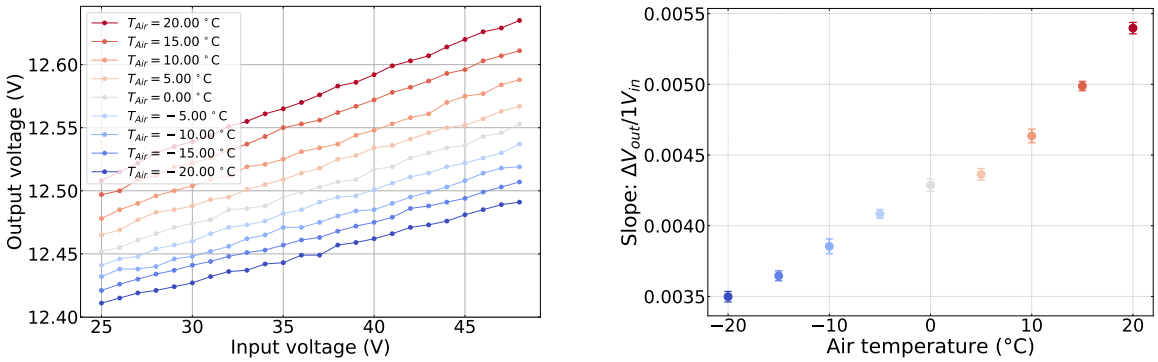

Figure 3. Line regulation curves for an output current of 2 A for different air temperatures (left) and the slope of the corresponding curves (right).

2.3 Radiated noise

DC-DC buck converters switch large currents at MHz frequencies, causing a triangular AC current in the inductor:

$$\Delta I_L = \frac{V_{\text{in}} - V_{\text{out}}}{Lf} D, \tag{2.1}$$

where V_{in} is the input voltage, V_{out} is the output voltage, f is the switching frequency, L is the inductance and D the duty cycle ($V_{\text{out}}/V_{\text{in}}$). This AC current generates a switching magnetic field. The field is measured using a pickup coil connected to a spectrum analyzer. The coil is positioned parallel to, and roughly 0.5 cm above, the DC-DC converter board, measuring the radiated magnetic field in the z-direction, perpendicular to the PCB. The coil is moved across the converter by an xyz-stage. The resulting scan in figure 4 (left) shows a clear maximum above the inductor. To reduce radiation, a test shield was made from two commercial shields soldered together, made of a 300 µm thick non-magnetic nickel, copper and zinc alloy. This test shield already shows an improvement of a factor 35, as can be seen in figure 4 (right).

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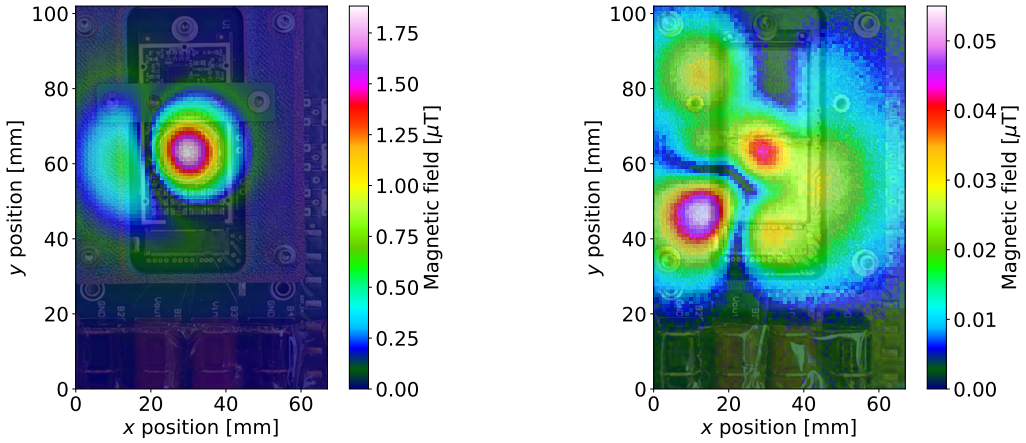

Figure 4. The magnetic field strength in the $x - y$ plane above the bPOL48V powered at 48 V, left without shielding and right with shielding. The scale is adapted to the maximum measured field strength.

2.4 Conducted noise

Conducted noise is transmitted through power supply lines and trace patterns on the PCB. It originates from the rapid switching, which causes high frequency modulations in the direct current of both the input and output of the DC-DC converter.

To measure it, the converter is powered with 48 V from a power supply via a Line Impedance Stabilisation Network (LISN), and its output is connected to an Impedance Stabilised Load (ISL). Differential-mode (DM) or common-mode (CM) conducted noise is measured using a current clamp and spectrum analyser, by routing the positive and negative lines either parallel (CM) or anti-parallel (DM) through the clamp. The complete setup is mounted on a copper reference plane.

The bPOL48V is optimised to have a low DM noise at the output; this spectrum is shown in figure 5 (left). The spectrum shows the noise at switching frequency and its higher harmonics. To further reduce the DM output noise, the original board was modified by adding an extra pi filter. A 12 nH inductor was added in a pi filter configuration at the output, with five 47 µF capacitors placed before the inductor and one 47 µF capacitor after it. This reduced the noise by a factor five, as shown in figure 5 (right).

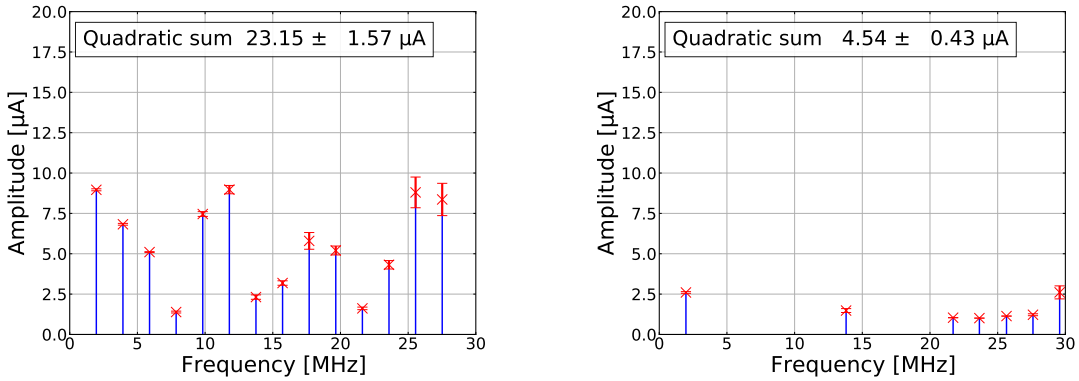

Figure 5. The DM noise at the DC-DC converter's output (left), and the same measurement with a pi filter (right).

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2.5 Output voltage ripple

The alternating current through the inductor (eq. (2.1)), shaped by the output capacitors, generates a voltage ripple at the converter output. This ripple was measured in a configuration without the pi filter, using an active differential probe and an oscilloscope.

One part that contributes to the voltage ripple originates from the parasitic parallel capacitance of the inductor. This allows the fast edges of the switching waveform to couple to the output, causing high-frequency spikes.

The second part is the low frequency ripple which is caused by the AC inductor current flowing through the output capacitors and their equivalent series resistance (ESR) and equivalent series inductance (ESL). This contribution is calculated by adding up each contribution to a total output voltage ripple $V_{\text{out}} = V_{\text{ripple}_C} + V_{\text{ripple}_{\text{ESR}}} + V_{\text{ripple}_{\text{ESL}}}$. These components are given in equation (2.2).

$$V_{\text{ripple}_C} = \frac{1}{C_{\text{out}}} \int I_L dt, \qquad V_{\text{ripple}_{\text{ESR}}} = I_L \cdot \text{ESR}, \qquad V_{\text{ripple}_{\text{ESL}}} = -\text{ESL} \cdot \frac{dI_L}{dt} \tag{2.2}$$

The calculated output voltage ripple is compared with low bandwidth oscilloscope measurements, and shown in figure 6. The calculation is in good agreement with the measurements.

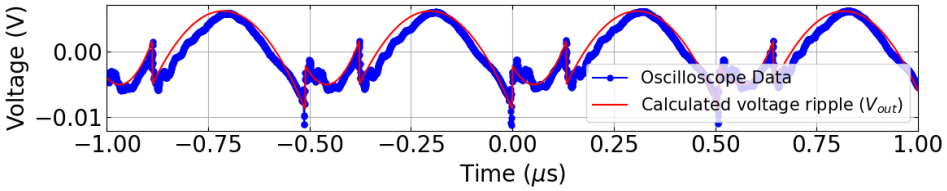

Figure 6. The measured and calculated low bandwidth total output voltage ripple.

3 Integration test with a CMS Phase-2 strip module

As a case study, a CMS Phase-2 silicon strip module, so-called a 2S module [4], is powered using the bPOL48V. Instead of powering the 2S module with a 10.5 V input via the bPOL12V [5] and bPOL2V5 [6], the module is powered with a 30 V input via the bPOL48V and bPOL2V5, maintaining an output voltage of 1.25 V. This setup is not intended for actual CMS Phase-2 operation. Noise measurements of the 2S module are performed inside a dark box. In this study, it is evaluated whether the noise in this measurement increases when the 2S module is powered by the bPOL48V with the converter placed as close as possible to the 2S module. With the shielding and the pi filter described in sections 2.3 and 2.4, the noise level is comparable to that obtained in the reference measurement performed with the standard powering scheme. Only a modest noise increase of approximately 20 % is observed. Further methods are being investigated to potentially reduce the noise even more.

4 Summary

The bPOL48V DC-DC converter was characterized in various setups. It achieves an efficiency of approximately 90 % across a wide operating range. Line and load regulation were determined and found to be temperature dependent. Radiated and conducted noise were measured and reduced. A test shield reduced radiated emissions by a factor of 35, and a pi filter lowered the differential-mode

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conducted noise at the output by a factor of five. The output voltage ripple was measured and compared to calculations of the low bandwidth ripple component, and good agreement was found. As a proof of principle, a CMS silicon strip module was powered and read out in a two-step powering scheme using the bPOL48V to convert 30 V to 1.25 V. This corresponds to an overall conversion ratio of 25.

Acknowledgments

This work was partly funded by the German Federal Ministry of Research, Technology and Space (BMFTR). We further thank the CERN EP-ESE group for the development of the bPOL48V and for making the device available to us. The research was conducted within the framework of the DRD7 collaboration, whose support is gratefully acknowledged.

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