

# Increasing Radon Daughter Plate-out onto Superconducting Qubits

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## Abstract

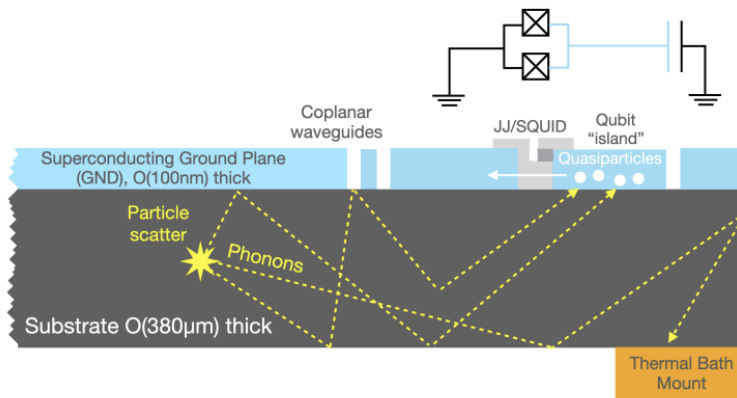
Radon daughter plate-out may pose a fundamental limitation to realizing large-scale superconducting quantum computers. Radon daughters plated-out on a superconducting qubit can decay, releasing energy into the substrate, producing phonons. Phonon-induced quasiparticles then generate bit-flip errors and reduce coherence times. We seek to increase plate-out on chips to enable future study of the impact of radon on coherence times. In this project, we utilize COMSOL Multiphysics simulations to visualize electric field configuration and model ion transport to finalize design of a device to increase radon plate-out on qubit chips.

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## 1 Motivation

### 1.1 Superconducting qubit errors

Cosmic rays have previously been shown to cause catastrophic correlated bit-flip errors in superconducting quantum computers [1]. The rays strike the qubit, generating collective vibrations of the material (phonons) on the substrate. The phonons carry bursts of correlated bit-flip errors and overall reductions in coherence time through the qubit [1]. Yet to be demonstrated,  $^{222}\text{Rn}$  plate-out may cause the same bit-flip errors and reductions in coherence time through a similar phonon-mediated process. Radon daughters plated-out on superconducting qubit chips can decay, releasing energy into the substrate, producing phonons. The subsequent phonon-induced quasiparticles could then generate bit-flip errors and reduce coherence times [2]. As a result, radon and its progeny, present in the air, fundamentally bottleneck the realization of a large-scale quantum computer unless solutions are found for controlling plate-out.

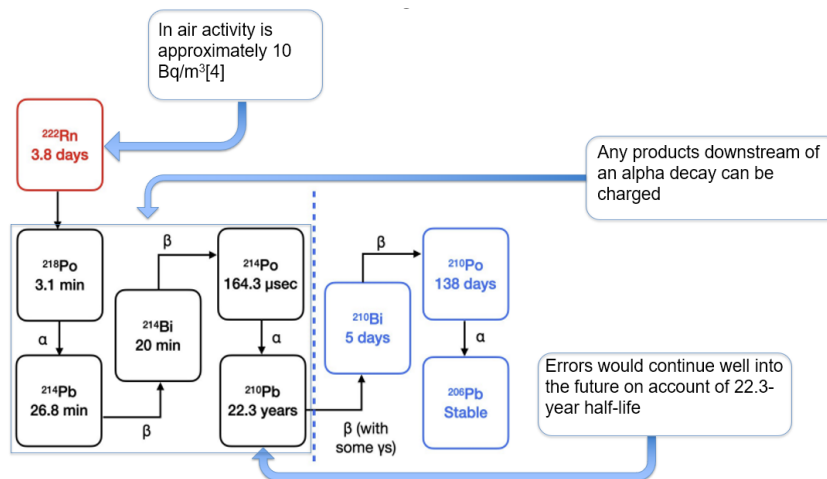


**Figure 1.** Illustration of phonon induced bit-flip errors resulting from a particle scattering event [2]

1.2 Radon daughter plate-out

Each decay event shoots a daughter in a random direction with the possibility of embedding in the material. In air activity of  $^{222}\text{Rn}$  is on the order of  $10 \text{ Bq/m}^3$ , but varies depending on location [3]. This means that in every cubed meter volume roughly ten potential plate-out events occurs per second in steady state. Beyond  $^{222}\text{Rn}$ , the decay chain is rapid, on the order of minutes, until  $^{210}\text{Pb}$ , with a half-life of 22.3 years. This means that  $^{222}\text{Rn}$  plated-out during the fabrication process will generate random occurrences of correlated bit-flip errors and a reduced coherence time for over 20 years even if plate-out is controlled during operation of the computer.

Each product downstream of an alpha decay can be positively charged. As such, radon’s daughters can be guided by electric field lines. In order to study the effect of radon daughter plate-out onto superconducting qubits, we seek to increase plate-out on chips. This project aims to design and simulate devices for facilitation of plate-out via DC electric field tailoring.

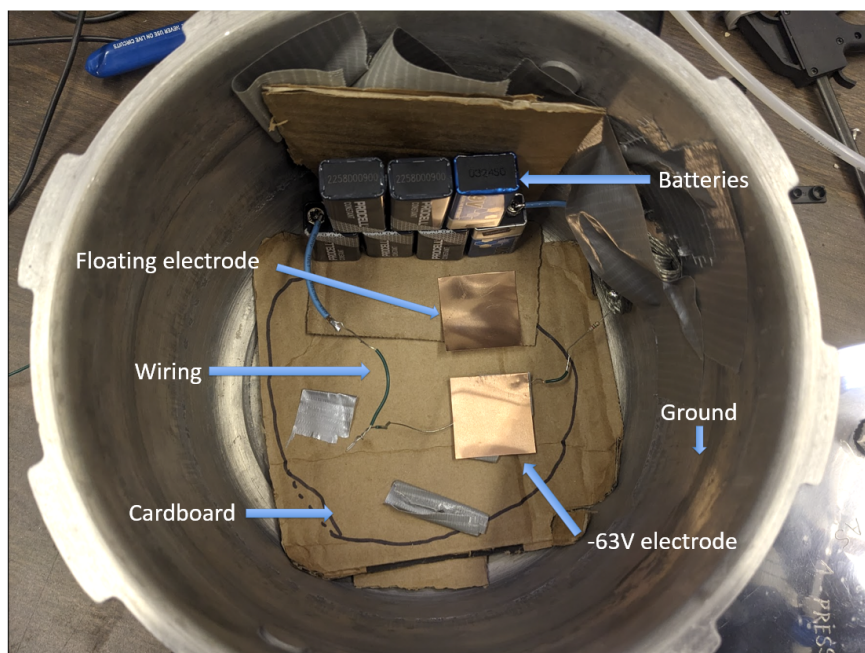


**Figure 2.** Diagram of radon decay chain with arrows added to highlight features pertinent to concerns of plate-out [4]

2 Methods

2.1 Accelerating plate-out

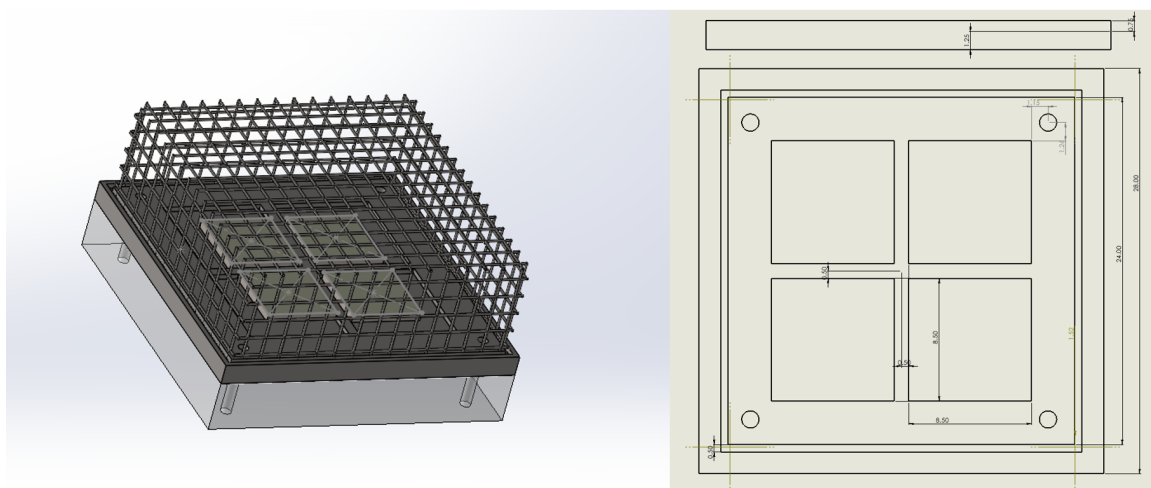
Currently, our collaborators at South Dakota School of Mines & Technology are collecting data on the effects of electric field on plate-out efficiency. Their setup is a pair of copper plates on top of cardboard in a pressure cooker. seven nine-volt batteries set one of the plates at -63 volts with respect to the walls of the cooker, while the other remains floating.



**Figure 3.** Current experimental setup for increasing plate-out at SDSM. 7 9-volt batteries supply a negative voltage to a copper sheet relative to the cooker walls, while the other sheet remains floating. Voltages are insulated by cardboard.

We expect based on first principles that electric fields modify transport of the charged daughter species, resulting in increased plate-out rate on negatively charged surfaces. Previous literature has documented augmented transport such as a marked decrease in ground-level activity due to strong electric fields associated with atmospheric activity as far back as the 1960's [5]. What we do not know is exactly how much we can increase this plate-out rate. Moreover, we need to determine if the current apparatus or future iterations could destroy the junctions of the superconducting qubit targeted for plate-out. It has been demonstrated that charge build-up during the etching process via the antenna effect can damage the terminals of a Josephson Junction [6]. Similar damage to the junctions could occur in the presence of fields generated by a nearby high voltage electrode.

We plan to build an electrode configuration to test its effect on the structural integrity of the junctions and radon plate-out. We first generated a CAD file and technical drawing of the likely design for ease of machining.



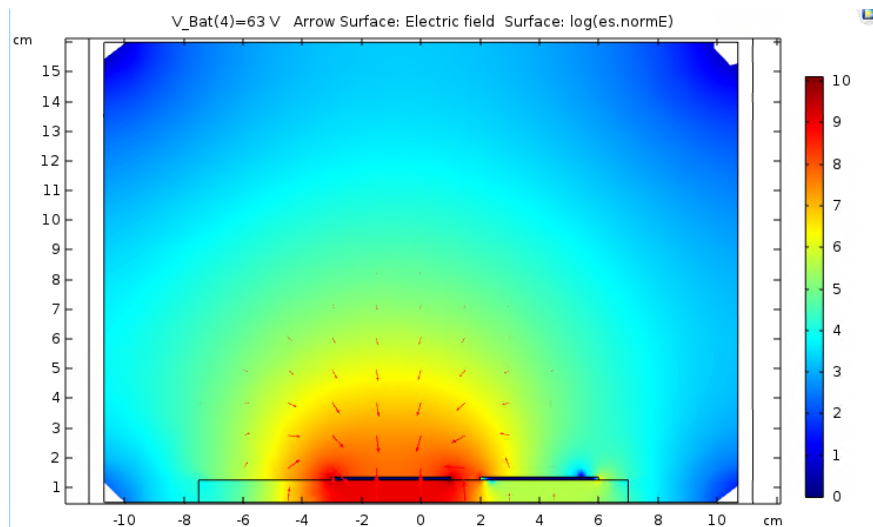
**Figure 4.** Left: CAD file for a four qubit holder electrode connected to dielectric base. Right: technical drawing of the four qubit holder electrode for machining

The design consists of a copper or steel electrode to be held at a voltage, machined with slots for four qubits and a groove for attachment of a copper or steel mesh Faraday cage. The reason for

the four qubit slots is to allow plateout of a higher number of qubits at once. This increases the speed at which experimentation on the qubits can move, while also allowing for greater reproducibility between runs. Each of the four qubits is expected to share the exact same plate-out parameters. Moreover, this makes it a more manageable size to form at 2.8x2.8cm area as opposed to the 1.8x1.8cm area it would be otherwise. Additionally, the mesh was chosen to reduce stray fields impinging on the qubit (effectively reduce field to zero) while maintaining 60+% visibility to allow ion transport to the qubit. It is worth noting that ion transport will still occur in the absence of a field due to diffusion. As the daughters will diffuse towards regions of lower concentration, our goal is to accumulate a high enough concentration around the cage at a low enough voltage to enter a regime where diffusion carries a significant amount of daughters to the qubit.

## 2.2 Multi-physics simulations

To verify our collaborators' data and finalize our device design, we conducted simulations with COMSOL Multiphysics. Our first aim was to visualize the electric field configuration of our collaborators' experimental setup.

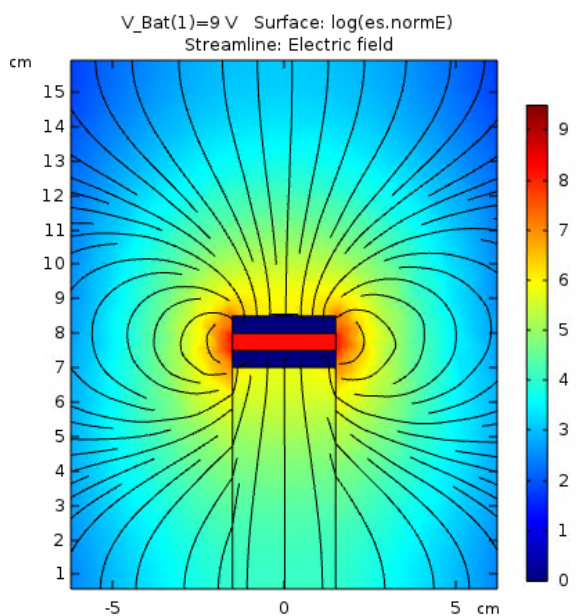


**Figure 5.** Natural log scale arrow and magnitude  $\ln(V/m)$  plot of electric field for current experimental setup in COMSOL Multiphysics.

We placed 4x4x1mm copper sheets (one floating and one held at -63V) on top of a dielectric with a relative permittivity of 2.3 (to model cardboard) inside a steel pressure cooker with a height of 155 mm and radius of 107.5 mm. The floating plate was defined with the floating potential boundary condition, while the -63V plate was held at this voltage relative to the walls of the cooker which was tied to ground. There was no free charge defined on any surface. We modeled both the average and vector field values in natural log scale. There was a significant field hot spot around the -63V plate with most of the field leading to the plate.

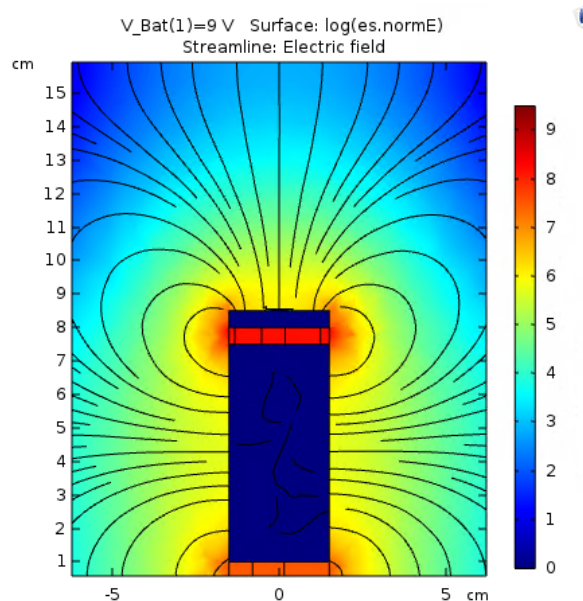
Next we sought to finalize our own experimental geometry by simulating various arrangements of the electrodes. For now, we are not considering a field cage. Our initial design was based on the idea of a negative point charge within a sphere of positive voltage that would yield a uniform radial electric field. As a result, our earlier designs featured a large dielectric base to hold the electrode near the center of the pressure cooker. We could then place the qubit on top of the electrode.

At this point, we had an issue with a large volume of field lines drawing ions towards the bottom of the electrode rather than the top, where the qubit is situated. This led us to a design where we placed a parallel plate capacitor on top of the dielectric stand to recirculate field from the bottom of the electrode back to the top [6](#).



**Figure 6.** Natural log scale plot of field magnitude  $\ln(V/m)$  and field lines for double plate configuration with a bottom plate at +9V and a top plate at -9V.

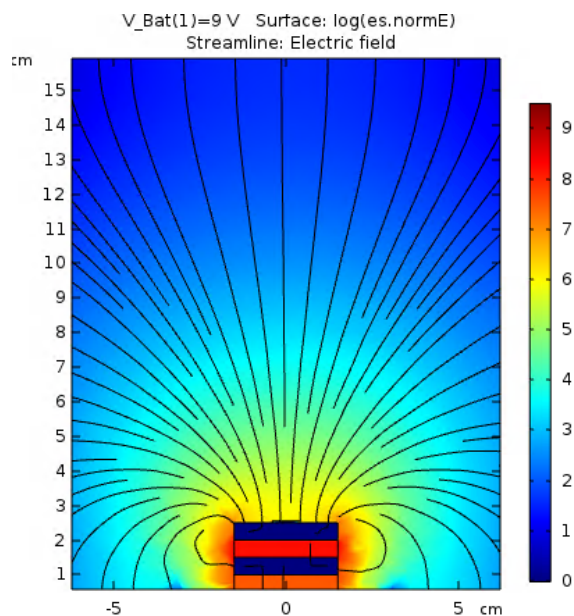
This recirculated the field well enough, but we were worried about charge build-up in a tall dielectric block engulfing a large region of field. As such, we increased the size of the bottom electrode and decreased the size of the bottom dielectric 7.



**Figure 7.** Natural log scale plot of field magnitude  $\ln(V/m)$  and field lines for double electrode configuration with a large bottom plate at +9V and a top plate at -9V.

Although this configuration worked well for high voltages (72V+), it wasn't effective for lower voltages which may be necessary if we want to allow significant diffusion through a field cage or circumvent one altogether.

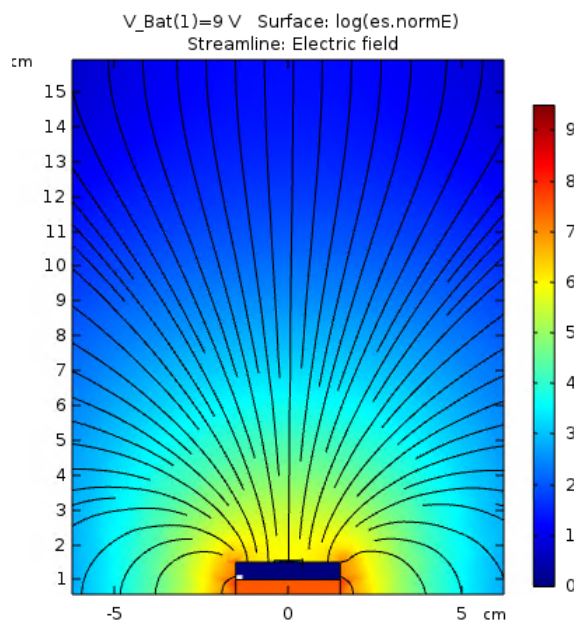
We then significantly decreased the size of the bottom electrode to drop the configuration closer to the bottom of the cooker 8.



**Figure 8.** Natural log scale plot of field magnitude  $\ln(V/m)$  and field lines for low stack double plate configuration with a bottom plate at +9V and a top plate at -9V.

This proved to be our best design yet, most effectively funneling field lines towards the qubit. The key insight that enabled this drastic change is that the most important parameter in directing field lines to the top of the negative electrode is maximizing proportion of the cooker above the stack.

As the stack was now close to the bottom of the cooker, the necessity of a positive electrode to circulate field was brought into question. This brought us back to our collaborators' initial design of a single negative electrode at the bottom of the cooker 9.



**Figure 9.** Natural log scale plot of field magnitude  $\ln(V/m)$  and field lines for single plate configuration at -9V

Qualitatively, this is marginally less effective than the parallel plate design, but with the advantage of a simpler fabrication process. Quantitative analysis is needed to verify, but this is the design we will proceed with for now.

So far, our discussion of the ionic migration of daughters has been purely qualitative. To validate our design choices and experimental findings, we seek a more quantitative measure of simulated plate-out. This requires simulating ionic transport to predict plate-out.

There is no immediate clear way of defining a steady-state condition for the plate-out of charged ions on a complex geometry of variable voltage boundaries acting as ion sinks. As such, rather than solve for a steady state condition of the radon's activity as COMSOL would, we seek a time dependent approach, stepping randomly generated individual particles until they reach a defined boundary. To accomplish this task, we use the Python programming language to build a Monte Carlo simulation capable of quantifying plate-out from electric field distributions generated in COMSOL.

We randomly generate a large number of individual particles to sample the set of potential ion migration paths through the volume of the cooker. For each particle, we step through a time  $dt$  until they reach a defined boundary of our geometry, at which they terminate and register as plated-out. The electric field imparts a drift velocity to charged ions given by the equation:

$$\mu \vec{E} * dt \quad (1)$$

Additionally, we must consider a diffusion component to our ion's motion. Diffusion is different from electromagnetic migration in that it is not caused by a force in the traditional sense. At its core, it is a purely stochastic process described completely by a Gaussian distribution. With the assumption of a large medium, we can find the standard deviation of a Gaussian distribution with the following equation:

$$\sigma = \sqrt{2Ddt} \quad (2)$$

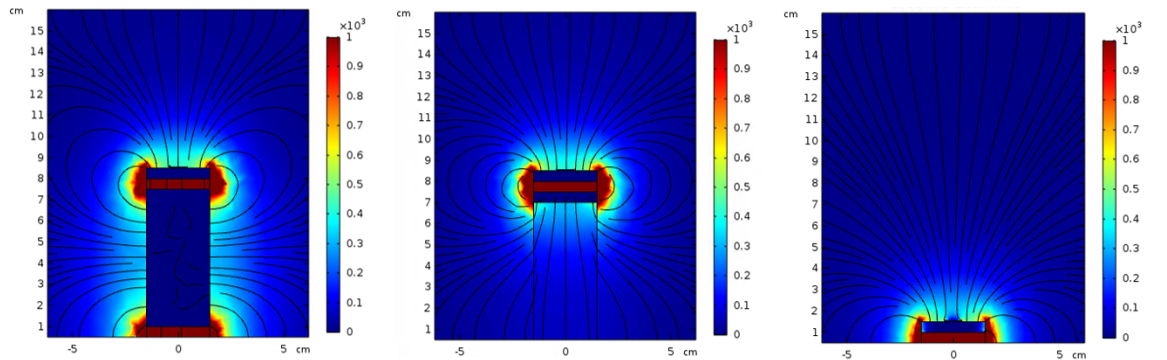
We can then solve for the distance of each step as the vector addition of the drift and diffusion terms.

$$\Delta \vec{x}_i = \mu \vec{E} dt + \langle X(\sigma), Y(\sigma), Z(\sigma) \rangle \quad (3)$$

Where the second term is a random vector determined by a Gaussian about zero with a standard deviation solved as previously described by 2.2. Our motivation for modeling electro-migration of the charged ions has been established. What may not be entirely clear is the impact of the diffusion term in our model. As alluded to earlier, with our discussion of the field cage 2.1, we need to consider diffusion because ion transport is not deterministic. The effects of diffusion could significantly impact ion transport throughout the cooker, especially in regions of low field. As such, it must be taken into account when predicting plate-out. It is not entirely clear how viable a field cage is for facilitating ion transport to the qubit or how voltage will affect plate-out of any given geometry when considering the effects of diffusion. These are questions best answered by a multiphysics simulation of the two processes. Luckily, we have all of the information necessary for constructing the simulation. The diffusivity of radon in air is  $1.2 * 10^{-5} m^2 s^{-1}$ , which fully defines our Gaussian function for diffusion [7]. Additionally, the mobility of radon daughter ions in air was found to be a distribution with a mean value of  $0.9 * 10^{-4} m^2 v^{-1} s^{-1}$ , which allows us to define our electro-migration steps [8]. All that follows is to debug our program and compile plate-out statistics.

### 3 Conclusions

#### 3.1 Optimizing electrode for plate-out



**Figure 10.** Field line and magnitude (V/m) plots of various electrode configurations in COMSOL Multiphysics. Right to left: -9V top electrode and +9V large bottom electrode; -9V top electrode and +9V bottom electrode; -9V electrode short stack

Our collaborators' initial design of a single electrode at the bottom of the cooker turned out to be close to optimal. We started with the assumption the qubit should be near the center to maximize plate-out, but this assumed spherical symmetry in an inherently asymmetric device. The most important parameter is the proportion of field lines above the qubit, and a single plate allows us to stay nearest to the bottom of the cooker, maximizing this parameter. More complex configurations like the parallel plate capacitor proved minimally more effective, if at all. The single plate is easy to fabricate and optimized for plate-out so it will be the subject of further simulations and experiments.

### 3.2 Future directions

We plan to continue our simulations, as well as experimentally prototype and characterize our design. We first plan to quantitatively analyze our collaborator's plate-out with the ion drift Monte Carlo simulation we have partially completed. We will then utilize this simulation to test further iterations of our design, both with and without the Faraday cage. Currently it is unclear if voltage will destroy the qubit with electrostatic discharge. As such, we will apply voltage to our qubit device with and without the field cage. This will determine the voltage we can apply without destroying the qubit and whether the field cage is necessary.

### Acknowledgments

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