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Development of the MOSAIX chip for the ALICE ITS3 upgrade

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Abstract: Following the ALICE ITS3 detector development path of wafer-scale monolithic stitched pixel detector prototypes (MOSS & MOST) in the TPSCo. 65 nm CMOS imaging technology, the MOSAIX chip is the prototype of the final full-size and full-functionality ITS3 sensor. MOSAIX has a die size of $26.6 \times 1.96\,\mathrm{cm}^2$ with an active area exceeding 93 %. It has 144 sensor tiles which can be powered down individually to compensate for manufacturing defects, where each tile has 69.2k pixels with a $22.8 \times 20.8\,\mu\mathrm{m}^2$ pixel size. This contribution provides an overview of the architectural decisions in MOSAIX, highlighting key lessons from the MOSS and MOST prototypes with a focus on yield enhancement techniques.

Keywords: Particle detectors; Particle tracking detectors; Radiation-hard electronics; VLSI circuits

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1 ITS3 detector and challenges

The ALICE (A Large Ion Collider Experiment) collaboration has undertaken an ambitious project to upgrade the Inner Tracking System (ITS) as part of the ITS3 upgrade. The primary goal is to reduce the material budget per layer from 0.35% X_0 to 0.07% X_0 per layer while positioning the first layer of the detector just 19 mm away from the interaction point. This will significantly enhance particle tracking efficiency, particularly for low-momentum particles. The detector will replace the three innermost layers of the current ITS during the upcoming Long Shutdown 3 (LS3) at CERN with 3 concentric layers of wafer-scale sized sensors thinned to 50 µm which, are bent around the beam pipe and held in place only with carbon foam spacers [1–4].

This introduces the challenge of integrating all services, including power distribution and data communication, directly onto the chip, which were previously available on the stave. The sensitive area and peripheral circuitry must coexist on the same die, reducing the fill factor. Additionally, the lack of active cooling, due to the use of air cooling, limits the allowable power density. Managing the impact of manufacturing defects also poses a large challenge as a single short in the global power grid can compromise an entire layer.

The core challenge of this project is developing a silicon-only, wafer-scale, monolithic stitched pixel sensor with a bent design, optimized for defect rates $< 2\%$, 40 mW/cm^2 power consumption, and 30.72 Gb/s nominal data transmission load — all under stringent mechanical constraints. Figure 1 shows a comparison between the ITS2 half inner barrel and the ITS3 half inner barrel mock-up.

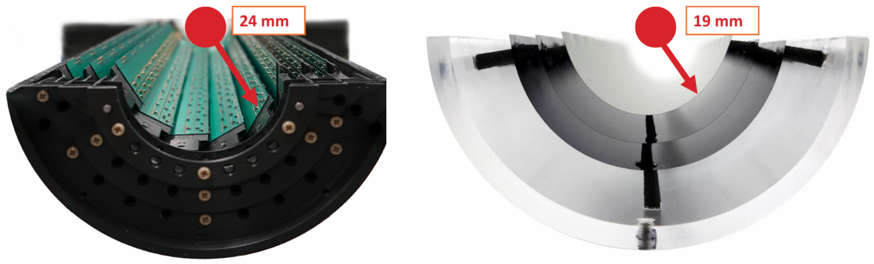

Figure 1. (a) ITS2 half inner barrel, 24 mm from the beampipe, 0.35 % X_0 per layer (b) ITS3 half inner barrel mock-up, 19 mm from the beampipe, 0.07 % X_0 per layer.

Semiconductor photomasks generally restrict the maximum circuit area that can be fabricated in a single exposure due to limitations in the lithography equipment. However, with stitching technology, these individual sections can be seamlessly combined to form a continuous large-scale chip. An example is shown in figure 2, where the sensitive area, A, is aligned and stitched together to make a larger sensitive area. This stitching approach requires carefully designed power distribution and data communication networks to ensure consistent functionality across the entire stitched area.

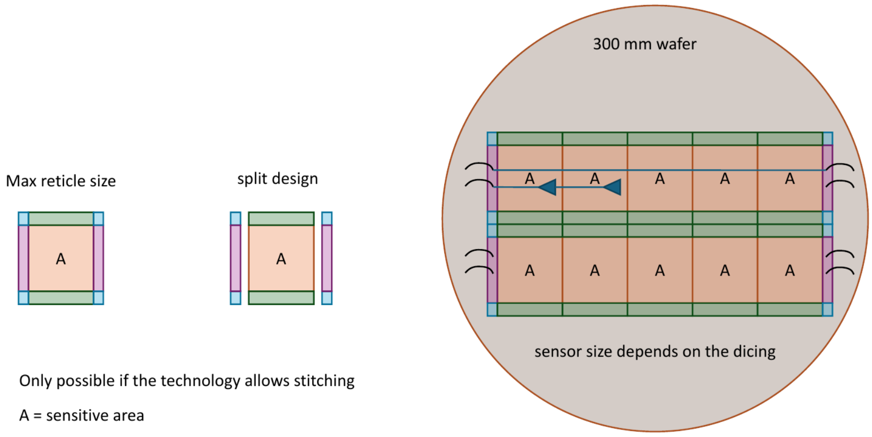

Figure 2. Stitching example of 300 mm wafers.

Figure 3 illustrates the structure of the ITS3 detector, with an exploded view of its layers shown on the left and the ITS3 sensor's wafer map on the right. The stitching approach enables the precise dicing of every sensor layer by selecting how many segments are diced together. A segment is composed of stitched units which can be diced out to make a layer. Specifically, layer 0 requires three segments, layer 1 requires four, and layer 2 requires five, achieving the necessary radii around the beam pipe depending on the number of diced off segments. This segmentation allows the entire detector to be built using the same photomasks and design in just 6 wafers.

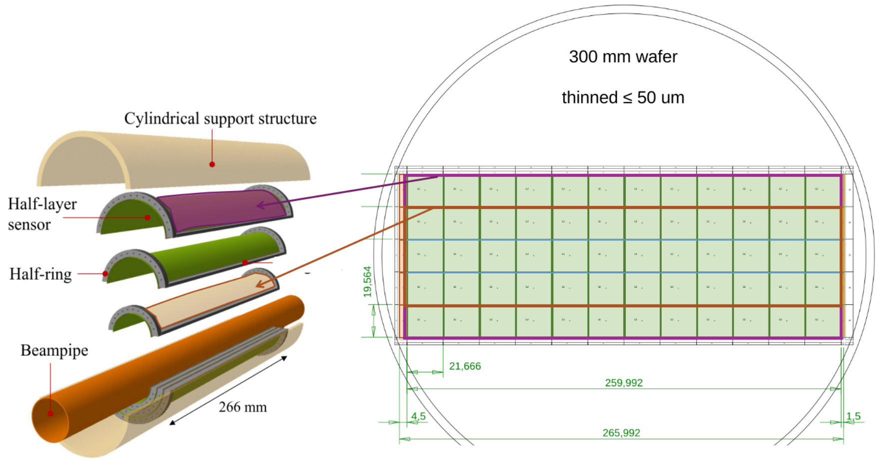

Figure 3. (a) breakdown of the ITS3 detector layers (b) wafer map of the ITS3 sensor.

2 Wafer scale stitched sensors demonstrators

The development of MOSAIX builds on valuable insights from its predecessors, MOSS (Monolithic Stitched Sensor) [5] and MOST (Monolithic Stitched Sensor with Timing), both designed using TPSCo's 65 nm imaging technology with stitching and submitted in December 2022.

Each prototype implement different methodologies to best manage manufacturing defects. MOSS focused on studying yield and uniformity across large sensing areas, employing design rules with enlarged spacing and a coarse power modularity. MOST, on the other hand, investigated techniques to detach small pixel groups from the main power grid via switches, utilizing minimum spacing rules and finer power modularity. Both designs demonstrated the criticality of power modularity in mitigating the impact of defects across extensive sensor areas. The new MOSAIX stitched sensor integrates best practices from both prototypes, combining refined power modularity with advanced yield-enhancement techniques to develop a reliable, high-yield, large-area sensor.

Further yield enhancement techniques, including custom cell libraries, increased metal width and spacing, and formal Design Rule Checks, were incorporated based on lessons from MOSS and MOST prototyping.

3 MOSAIX chip

The MOSAIX chip is a full size, fully functional, stitched sensor production prototype for the ALICE ITS3 detector. Measuring 26.6 cm by 1.96 cm, the MOSAIX chip covers an active area of 93% with a total of 144 independently powered sensor tiles. This modular approach allows for effective defect management by isolating each tile as an independent unit for both power and data acquisition. Figure 4 shows the MOSAIX block diagram, highlighting the Left Endcap block, Repeated Sensor Unit block (12 tiles each) and the Right Endcap block. Due to the mechanical constraints of the ITS3 detector, data and power can only be supplied via the short edges. The Right Endcap is only used for power connections. The hit data from every tile flows towards the Left Endcap, which acts as the chip's data hub and is outside of the detector's acceptance area. Each sensor tile transmits on-chip packaged hit data differentially at 160 Mb/s, in a point to point connection fashion to the Left Endcap. Table 1 summarizes the key chip specifications.

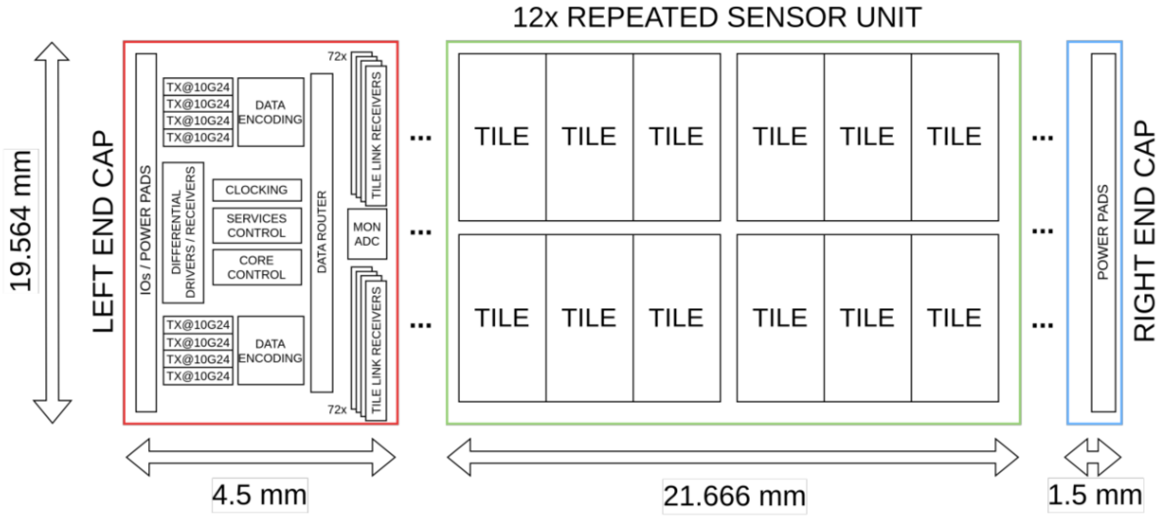

Figure 4. MOSAIX block diagram.

Table 1. MOSAIX chip key specifications.

Fill factor	93 % sensitive region
	0.7 % sensor area modularity
	144 tiles (independent units)
Pixel performance	$22.8 \times 20.8\,\mu m^2$ pixel size
	Detection Efficiency >99 %
	Fake hit rate <0.1 $pixel^{-1}\,s^{-1}$
Data taking	$4.4\,MHz/cm^2$ particle rate
	30.72 Gb/s off-chip data transmission
	minimum 2 µs integration time
Radiation performance	10^{13} NIEL (1 MeV n_{eq}/cm^{-2})
	10 kGray TID
	Triple modular redundancy
Power budget	$40\,mW/cm^2$

3.1 Repeated Sensor Unit

The Repeated Sensor Unit block is shown in figure 5(a). In order to control the power on/off of the Sensor Tile, a dedicated slow control is used, which directly actuates on the power switches of the tile. The hit data is buffered and retimed over 26 cm every 10.8 mm of silicon by the stitched backbone block.

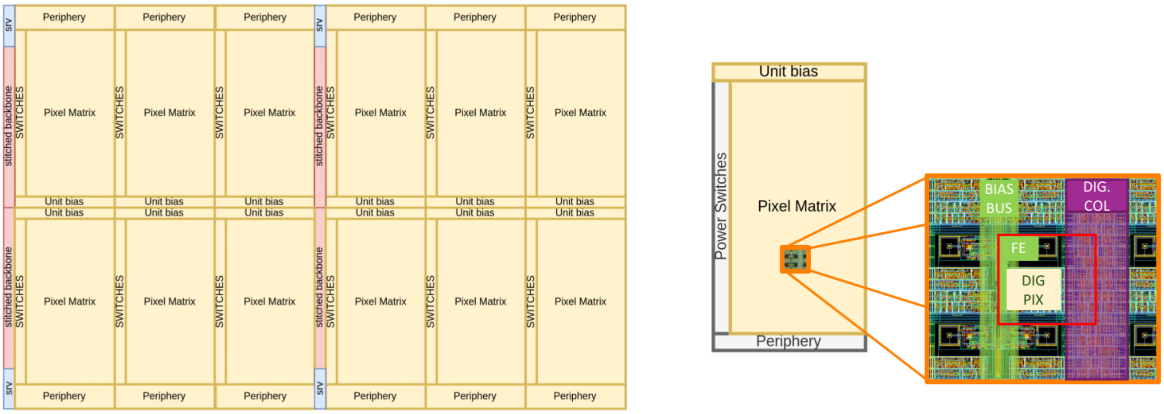

Figure 5. (a) Repeated Sensor Unit block diagram with services node, stitched backbone and 12 tiles (b) Sensor Tile focusing on the Unit Bias, Pixel Matrix block.

3.2 Sensor Tile

A Sensor Tile can be seen as an independent sensor unit in terms of power and data taking. It is comprised of four blocks: the pixel matrix which instantiates an array of 444 rows by 156 columns in a double column readout scheme; the unit bias which biases the analog front-end of the pixels; the periphery which reads out the hit from the pixel matrix, packages the data and sends it to the Left Endcap differentially at 160 Mb/s; and the power switches, which enables the user to isolate the Sensor Tile block from the main power grid in case of manufacturing shorts in the local power domain.

Figure 5(b) illustrates the floorplan arrangement of the tile, focusing on the analog and digital columns together with the analog and digital pixel sections of the pixel.

3.3 Left Endcap

The Left Endcap block diagram is shown in figure 6. The purpose of the Left Endcap is to consolidate hit data from the 144 tiles and send the data off-chip. The data path is Versatile Link+ compatible [6], using lpGBT frame encoding, which enables the reuse of existing resources in the counting room for interfacing and reading the chip.

The Left Endcap integrates eight high-speed serializers, each operating at 10.24 Gb/s. These serializers are grouped such that every four serializers connect to one VTRX+ opto-electronic module, providing a direct off-chip link. However, nominal data requirements necessitate only three active serializers at 10.24 Gb/s.

To cope with fault mitigation in the transmission medium (e.g. in cases of fiber breakage or VTRX+ module failure) the instantiation of the eight serializers offer two levels of protection. Should one VTRX+ module or serializer fail, data can be rerouted to an alternative serializer bank through slow control. Additionally, if transmission medium constraints prevent reliable operation at 10.24 Gb/s, the system can reconfigure the hit data transmission to operate at a lower rate of 5.12 Gb/s. Across all configurations, the total bandwidth remains at 30.72 Gb/s. Unused serializers can be deactivated to conserve power.

An Analog-to-Digital Converter (ADC) in the Left Endcap enables voltage monitoring across all Sensor Tiles, possibly identifying fluctuations in the power grid and in the biasing unit.

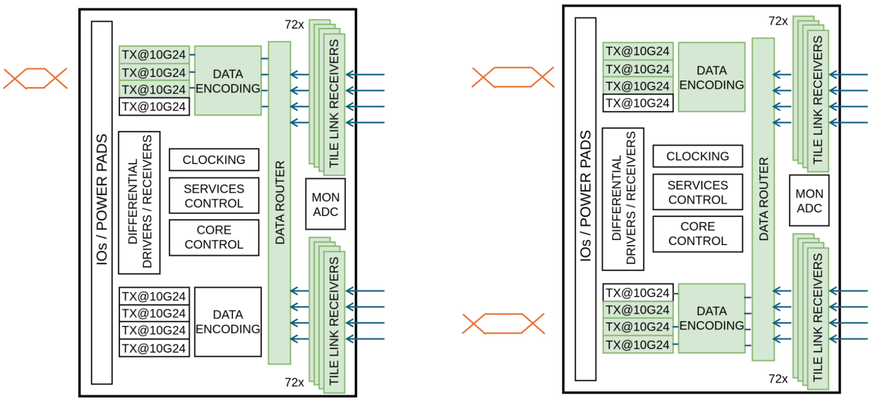

Figure 6. (a) Left Endcap nominal operation with 3x 10.24 Gb/s serializers (b) Left Endcap backup operation with 6x 5.12 Gb/s serializers.

4 Conclusions

The MOSAIX chip is a full-scale, fully functional stitched sensor prototype for the ALICE ITS3 detector, achieving wafer-scale integration with high yield and reliability.

Key specifications include a die size of $26.6 \times 1.96\,\text{cm}^2$, a 93 % active area, and a pixel size of $22.8 \times 20.8\,\mu\text{m}^2$, supporting detection efficiencies above 99 % at particle rates of $4.4\,\text{MHz/cm}^2$. To address manufacturing challenges, MOSAIX implements 144 independently powered sensor tiles via on-chip power switches, allowing defective tiles to be isolated without compromising the entire sensor. Data from each tile is transmitted at 160 Mb/s to the Left Endcap, where it is consolidated and serialized off-chip at up to 30.72 Gb/s. Extra serializers enable fault tolerance by rerouting data or adjusting bandwidth per serializer as needed.

The MOSAIX represents a pioneering advancement in detector technology, introducing wafer-scale, stitched pixel sensors to high-energy physics for the first time. The tapeout is foreseen during Q1 2025.

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