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of the Twelfth Workshop on Electronics for LHC and Future Experiments

València, Spain, 25–29 September 2006

Organized by

Instituto de Fisica Corpuscular (IFIC)
Universitat de València
Consejo Superior de Investigaciones Científicas (CSIC)

on behalf of the
CERN LHC Electronics Co-ordinating Committee

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Abstract

The purposes of the workshop were to review electronics progress for the LHC experiments; to present results and original concepts for electronics research and development relevant to possible future upgrades of the LHC; to present innovative electronics developments for other particle, astroparticle and space physics experiments; to identify and encourage common efforts for the development of electronics within and between the different experiments; to promote collaboration in the relevant engineering and physics communities.

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Organization

The twelfth in this series of workshops on Electronics for LHC and Future Experiments was organized for the CERN LHC Electronics Co-ordinating Committee by three Spanish institutions participating in experiments of the LHC programme:

Instituto de Fisica Corpuscular (IFIC)
Universitat de València
Consejo Superior de Investigaciones Cientificas (CSIC)

The workshop was held from **25-29 September 2006** in the Instituto de Fisica Corpuscular (IFIC), València.

Local Organizing Committee

Juan Antonio VALLS (Chair)	IFIC
Antonio FERRER	IFIC
Esteban FULLANA	IFIC
Emilio HIGON	IFIC
Belen SALVACHUA	IFIC

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Kevin EINSWEILER	LBL
Philippe FARTHOUAT	CERN
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Mike LETHEREN	CERN
Lucie LINSSEN	CERN
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Steve QUINTON	RAL
Veljko RADEKA	BNL
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Thijs WIJNANDS	CERN
Ray YAREMA	FNAL

Workshop Secretariat

José María AMENGUAL	IFIC
Sandra CLAUDE	CERN
Ana SANMATÍAS	IFIC

Proceedings Editors

Sandra CLAUDE	CERN
Kate ROSS	CERN

Overview

The purposes of the workshop were:

- to review electronics progress for the LHC experiments,
- to present results and original concepts for electronics research and development relevant to possible future upgrades of the LHC,
- to present innovative electronics developments for other particle, astroparticle and space physics experiments,
- to identify and encourage common efforts for the development of electronics within and between the different experiments,
- to promote collaboration in the relevant engineering and physics communities.

The main subjects of the workshop were recent research and developments in the following areas relevant to particle physics experiments:

- Tracking, Calorimetry, Muon Detection and Triggering Systems;
- Accelerator and Beam Instrumentation;
- Astrophysics and Space Applications;
- Custom Analogue and Digital Circuits;
- Circuit Developments in Deep Sub-micron Technologies;
- Applications of Programmable Digital Logic and Embedded Processing;
- Optoelectronic Data Transfer and Control;
- Radiation and Magnetic Tolerant Components and Systems;
- Electronics Assembly and Hybrid Packaging Technologies;
- Production, Testing, Quality Assurance and Reliability;
- Power Management and Conversion;
- Grounding, Shielding and Cooling;

The welcome address was given by **Geoff Hall**, chairperson of the programme committee, and the introduction was given by **Juan Antonio Fuster Verdú**, the Director of IFIC

One half-day (Plenary Session 5) was devoted to important issues for the electronics of the experiments at a possible future luminosity upgrade of the LHC machine. This took the form of a number of presentations on selected topics, each followed by an extended discussion session. The topics covered included SLHC machine issues; efficient power delivery and distribution on the detectors; timing distribution, control and data readout links; and options for optical links.

Two dedicated working group meetings were held, one on microelectronics and the other on optoelectronics.

PLENARY SESSIONS

Plenary Session 1- Opening plenary, Chaired by Geoff HALL

Particle and Astroparticle Physics in Spain	FERRER Antonio
The LHC machine status, calibration run and commissioning plans	LAMONT Mike
CMOS directions in industry	PEREA Ernesto
3D electronics	SUNTHARALINGAM Vyshnavi

Plenary Session 2 - Plenary ILC & high reliability, Chaired by Fabio FORMENTI

Detector and readout systems for the ILC	GREENSHAW Tim
High Availability Electronics standards	LARSEN Ray

Plenary Session 3 – Optoelectronics, Chaired by Francois VASEY

Optoelectronic developments for remote-handled maintenance tasks in ITER	VAN UFFELEN Marco
State of the art technologies for front-end hybrids	DE OLIVEIRA Rui

Plenary Session 4 - HEP electronic and ASIC trends, Chaired by Alessandro MARCHIORO

3D Circuit Integration for High Energy Physics	YAREMA Ray
Technology Scaling and CMOS Analog Design	MALOBERTI, Franco

Plenary Session 5 – LHC experiment electronic upgrades, Chaired by Lucie LINSSEN

Informal comments on SLHC machine issues	BUTTERWORTH Andy
Charge pump DC to DC converter Inner Tracker Applications	GARCIA-SCIVERES Mauricio; ELY Robert
The GBT Bi-directional link and data system	MOREIRA, Paulo
Future options for optical links	VASEY Francois

Plenary Session 6 - LHC Machine, Chaired by Mike LETHEREN

LHC machine RF issues and developments	BUTTERWORTH Andy
The LHC beam loss monitoring system's data acquisition card	EFFINGER Ewald
An on line radiation monitoring system for the LHC machine and experimental caverns	WIJNANDS Thijs

Plenary Session 7 – Beam, SLHC & closeout, Chaired by Mike LETHEREN

Beam Phase and Intensity Monitor for the LHCb experiment	JACOBSSON Richard
Proposal for a First Level Trigger using pixel detector for CMS at Super-LHC	PALLA Fabrizio
Stacked Tracking for CMS at Super-LHC	JONES John
Workshop closeout and concluding remarks	HALL Geoff

PARALLEL WORKING GROUPS

Parallel Sessions A and B were chaired by:

Thijs WIJNANDS
Emilio PETROLO
Jordan NASH
Wesley SMITH
Jorgen CHRISTIANSEN
Fabio FORMENTI
Ray YAREMA
Chris PARKMAN
Francois VASEY
Philippe FARTHOUAT
Stephen QUINTON
Alessandro MARCHIORO

POSTERS

The poster session was chaired by Lucie LINSSEN and Stephen QUINTON.

INDUSTRIAL EXHIBITION

The company exhibiting was :

W-IE-NE-R Plein & Baus GmbH, Burscheid-Hilgen, Germany.

SPONSORSHIP

The workshop was sponsored by:

- CERN, Geneva, Switzerland
- CSIC, Consejo Superior de Investigaciones Cientificas, Spain
- IFIC, Institut de Fisica Corpuscular, València
- Universitat de València

NEXT WORKSHOP

The next workshop will take place from 3 to 7 September 2007, in Prague (Czech Republic). The scope of the next workshop will be broadened to include electronics for major particle physics programmes. As a consequence, the workshop will carry a new name: **TWEPP-07**, Topical Workshop on Electronics for Particle Physics.

Opening Plenary Session

Particle and Astroparticle Physics in Spain

Antonio FERRER

Universidad de Valencia
IFIC Instituto de Fisica Corpuscular

Particle and Astroparticle Physics in Spain

Antonio Ferrer
Past (2000-2003) HEP Spanish Committee chairman
IFIC-Universitat de València & CSIC

12th Workshop on Electronics for LHC and Future Experiments
Valencia 25-29 september 2006

SPAIN

A total of 44,4 M hab. (8,75% foreign residents)

GNP 900.000 M€
R&D 9.000 M€ (~1%)

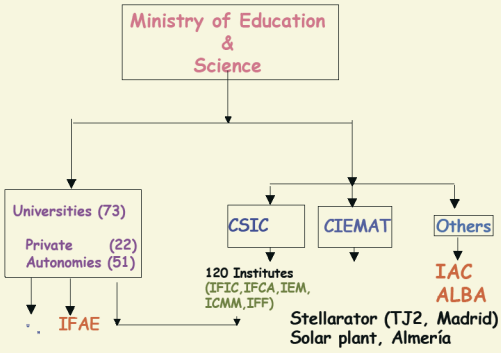
CERN Contribution ~80 MCHF (~8%)

to be compared (G 20%)
(UK 17%)
(F 15%)
(I 12%)

Research groups in Spain



Research institutions in Spain



Particle & Astroparticle physics in the Vth National Plan (2004-2007)

One of the 23 National R&D Programs

Basic research: Astronomy & Astrophysics,
Particle Physics,
Physics,
etc...

Priorities of the National Program

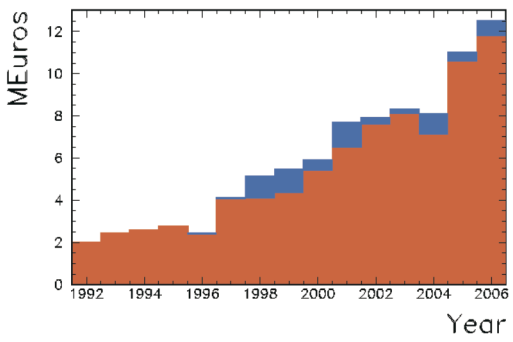
1. Particle Physics (CERN).
   - Quarks & Leptons, Neutrino, Hadrons, Theory.
2. Astroparticle physics & Cosmology.
3. Experimental Nuclear Physics (N-TOF, ISOLDE,GSI).
4. GRID Technologies .
5. Detectors and Accelerators Tecnologies.

National Program of Particle Physics (2006)

A total of ~ 60 research projects
About 400 researchers, 62 technicians, 212 fellows & st.
11,8 M€ 2006 budget

1.	Theory	11.7 %
2.	LHC (ATLAS, CMS, LHC-b)	24.4 %
3.	GRID (ATLAS, CMS, LHC-b)	21.2 %
4.	HERA (Zeus) CDF, BABAR	5.9 %
5.	Nuclear+ISOLDE (Dirac, +Legnaro, Ganil, GSI)	9.7 %
6.	Astroparticles(Auger,Canfranc,Magic,Antares,Icarus)	20.7 %
7.	Technologies & Applications	6.1 %

Particle physics funding

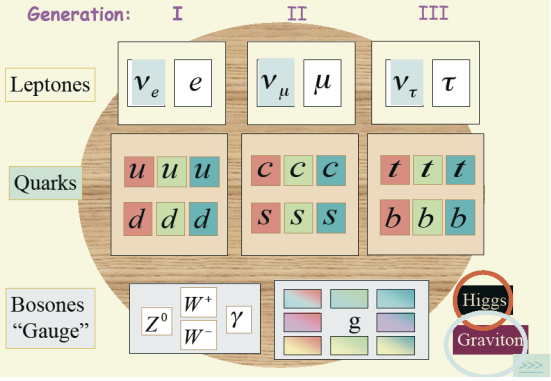


6 questions* defining Particle physics

1. Which are the ultimate matter constituents?
2. Which are the forces that bind or break them?
3. By which mechanism do constituents get their masses ? Does the Higgs boson exist?
4. What is the nature of neutrinos ?
5. Is supersymmetry a valid theory?
6. Are there any hints of a GUT theory ?

*"Science is the art of replacing unimportant questions that can be answered by important ones which cannot" Edward B. Ferguson Jr. 1976.

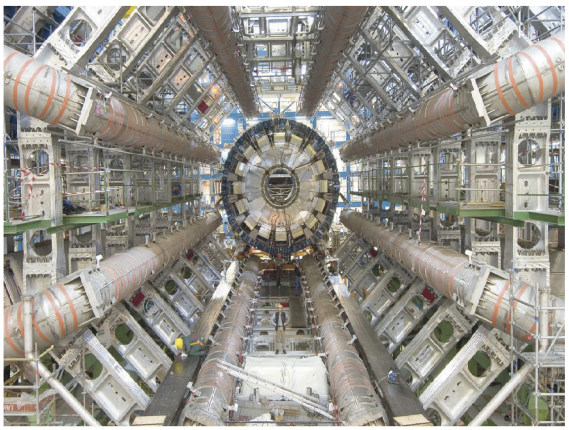
The Standard Model



Spanish contributions to the LHC

ATLAS	IFIC-Valencia	TiCal	315 submodules (50% of EB)
			1500 PMs
			ROD
	IFIC-Valencia	STC	200 silicon modules (+IMB)
	Barcelona IFAE		315 submodules
		TiCal	65 modules (1 Extended Barrel)
	Madrid UAM		Forward LAr Calorimeter
CMS	CIEMAT		Chambers MB2 (70)
			Electronics
	IFCA Santander		Alignment
	Madrid UAM		Trigger, Electronics
LHCb	USC		Si Tracker
	UB-URL		RICH (PM, Electronics)
LCG	All groups		





Experimental projects at IFIC

Particle & Astroparticle
- LHC-ATLAS:
  - TiCal
  - SCT
  - GRID computing
  - Software
- K2K
- Antares
- B-Factory/BaBar
- LEP/Delphi
- Accelerator Physics
- Detector R&D

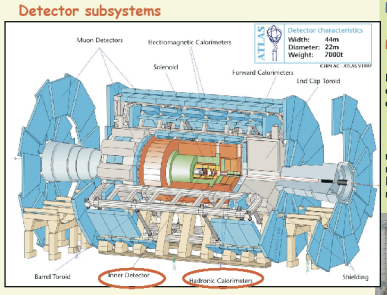
Nuclear Physics
- γ–Spectroscopy
  - nTOF
  - ISOLDE
  - FAIR, ALBA
- Nuclear Reactions
  - Hades
  - TAPS
- Integral

Medical Applications
- Nuclear Medicine
- CIMA



LHC-ATLAS

Detector subsystems



LHC Accelerator Physics:

Luminosity and Fwd Physics with ATLAS:

Optics design & Beam Dynamics simulation for an absolute Luminosity determination

LHC Injector (SPS)

Optics design, modelling of machine, study of non-linear resonance driving terms, localisation of sources of non-linearity



Software and Simulation

Inner Detector Alignment
B-tagging techniques
Higgs in MSSM and Top quark production

ATLAS-TiCal

Submodules Construction

315 iron submodules assembled (900 kg each), half extended barrel



Photomultipliers Testbench

1750 (17.5%) of the Tilecal photomultipliers tes in test bench labview

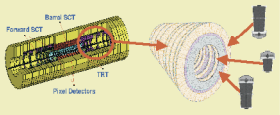
Read Out Driver (ROD)

Design, assembly, test and commissioning of the 32 ROD electronic boards to calculate energy, time and quality information of the more than 10.000 channels

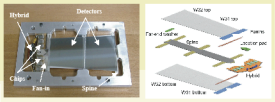


ATLAS-SCT

Characterization, assembly, metrology, bonding and test of **220 modules with 4 silicon wafers** each and its corresponding read out electronics of the Atlas Forward Tracker



Forward outer module

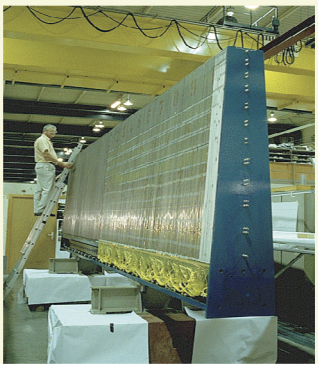


TileCal Submodule





TileCal Module

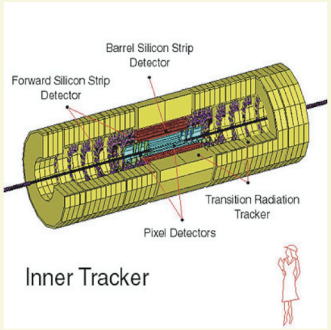


Spain built 1 EB
= 64 modules
640 Tons

50% submodules in Valencia (IFIC)
50% submodules in Barcelona (IFAE)

Extended Barrel mounted and instrumented in IFAE

SCT (Silicon inner tracker)



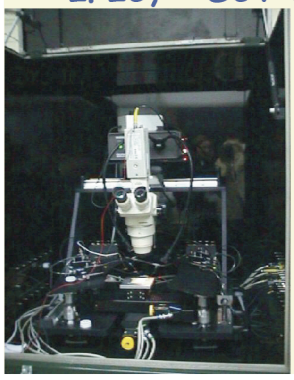
IFIC - Valencia
CNM-Barcelona

2 Wheels

200 modules

Test, Microbonding, Mount

IFIC, SCT clean room



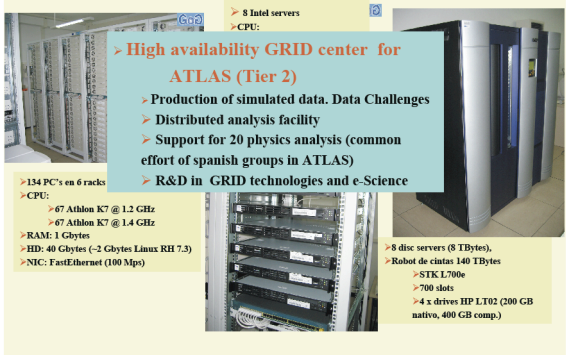


IFIC, clean room (SCT)



ATLAS-GRID

GRID Infraestructure at IFIC

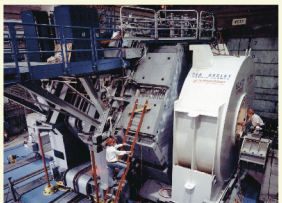


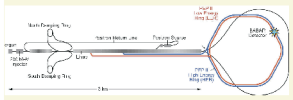
- High availability GRID center for ATLAS (Tier 2)
  - Production of simulated data. Data Challenges
  - Distributed analysis facility
  - Support for 20 physics analysis (common effort of spanish groups in ATLAS)
  - R&D in GRID technologies and e-Science

- 8 Intel servers
- CPU:
- 134 PC's en 6 racks
- CPU:
  - 67 Athlon K7 @ 1.2 GHz
  - 67 Athlon K7 @ 1.4 GHz
- RAM: 1 Gbytes
- HD: 40 Gbytes (~2 Gbytes Linux RH 7.3)
- NIC: FastEthernet (100 Mps)
- 8 disc servers (8 TBytes),
- Robot de cintas 140 TBytes
  - STK L700e
  - 700 slots
  - 4 x drives HP LT02 (200 GB nativo, 400 GB comp.)

BaBar: Asymmetric B-Factory at SLAC







Very rich B, charm and tau physics program

Search for CP Violation in B meson decays and test at this low energy scale the SM

CP violation established in 2001

Direct CP violation established in August 2004

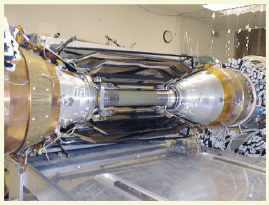
Try to open windows on new Physics

Since 1999, recorded ~260 M BB pairs. ~4-8 times more by end of decade

BaBar: Asymmetric B-Factory at SLAC

Silicon Vertex Tracker (SVT) reconstruction software

Feasibility studies to use and increase IFIC computing resource for official Monte Carlo productions (also being negociated)

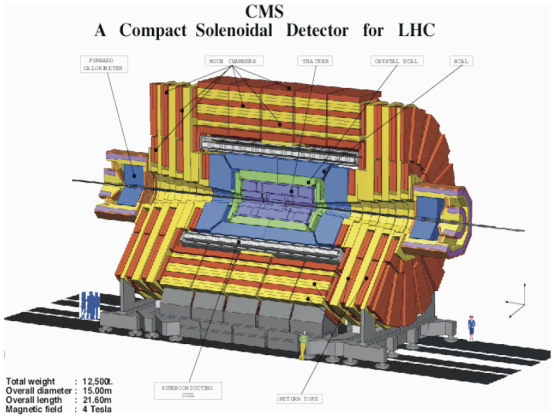




BaBar/PEP-II Long Term Planning Task Force. Evaluation of Physics impact of increased PEP-II luminosity and possible BaBar dectector upgrades (DOE report)

- CP violation measurements of the 3rd CKM weak angle γ in $B^- \rightarrow D_0^* K^-$ decays
- Precision CP Violation measurements with charmonium events and mixing studies with fully reconstructed hadronic decays
- Detailed studies of Quantum Mechanics of the BB System at the $\Upsilon(4S)$: simultaneous and precision test of all discrete symmetries, as a probe for New Physics

CMS
A Compact Solenoidal Detector for LHC

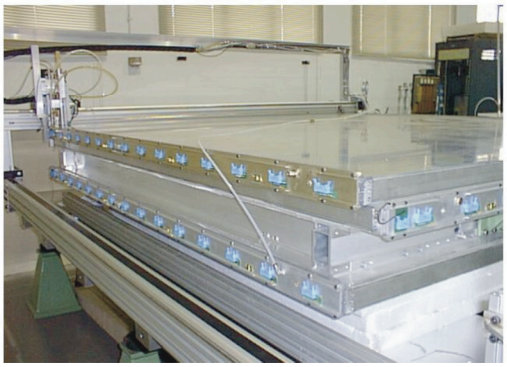


Total weight : 12,500t.
Overall diameter : 15.00m
Overall length : 21.60m
Magnetic field : 4 Tesla

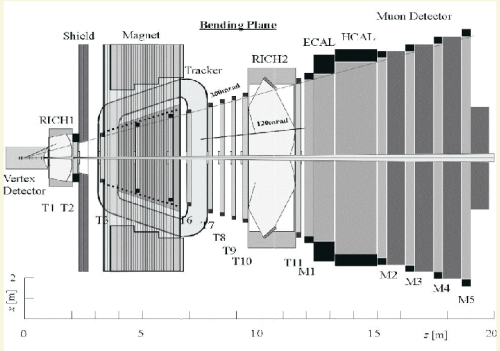
Muon chambers construction at CIEMAT



First MB2 Chamber Assembled at CIEMAT



El espectrómetro LHCb



6 questions* defining Astroparticle physics

1. What is the Universe made of ?
2. Do protons have a finite life time ?
3. What are the properties of neutrinos ? What is their role in cosmic evolution ?
4. What do neutrinos tell us about the interior of Sun and Earth, and about Supernova explosions ?
5. What is the origin of cosmic rays ? What is the view of the sky at extreme energies ?
6. What is the nature of gravity ? Can we detect gravitational waves ? What will they tell us about violent cosmic processes ?

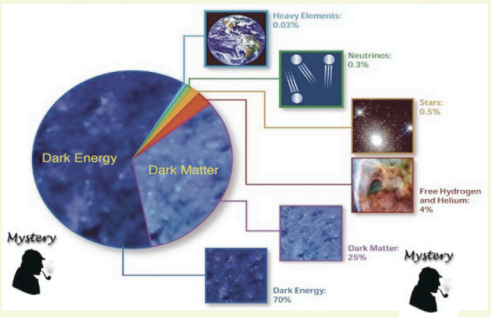
*"Science is the art of replacing unimportant questions that can be answered by important ones which cannot" Edward B. Ferguson Jr. 1976.

Astroparticles (+ neutrinos) in Spain

1. LSC CANFRANC	& CAST UZ
2. MAGIC	IFAE - UAB - UCM
3. ANTARES	IFIC
4. AMS	CIEMAT
5. AUGER	USC-UCM-UAH
6. K2K	IFAE+IFIC
7. ICARUS	UGR - CIEMAT
8. CHOOZ	CIEMAT

What is the Universe made of?

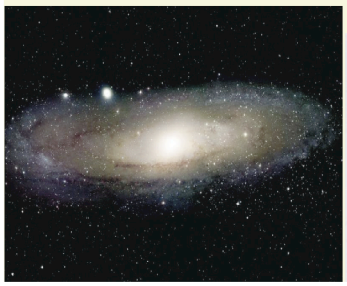
Stars and planets account only for a small fraction of the Universe!

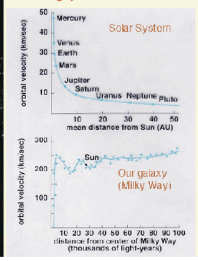


Proof of existence of « dark matter»

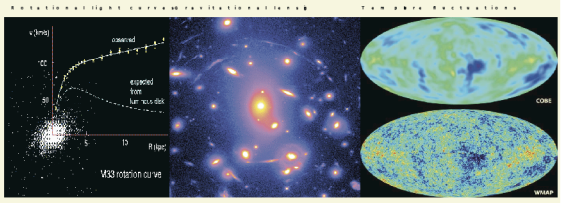
Rotational curves

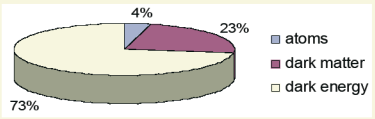
(velocity of peripheral stars, too large)





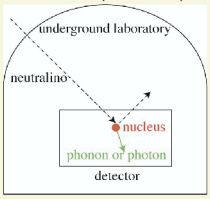
Dark Matter



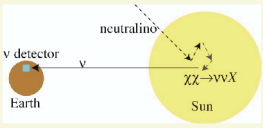


Detection of Dark Matter

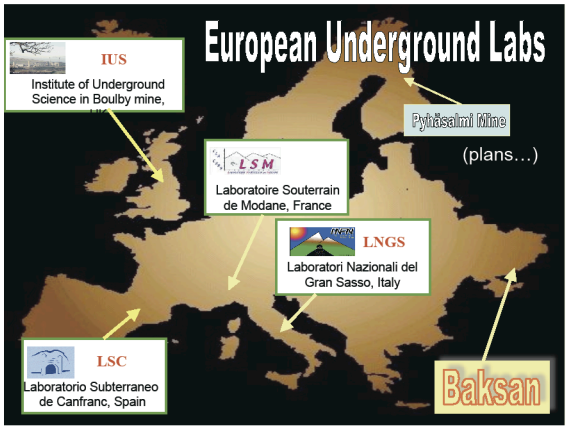
- Direct detection
- CDMS-II, Cuore, DAMA, ANAIS, etc



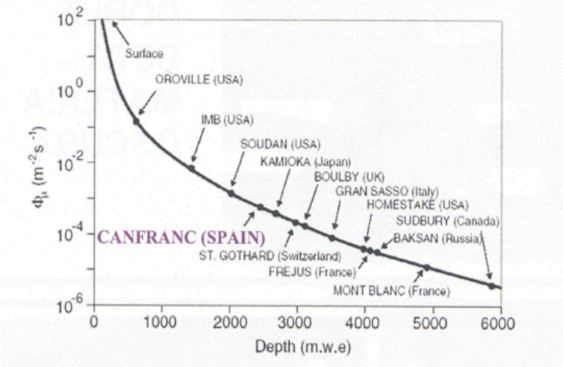
- Indirect detection
- SuperK, AMANDA, ICECUBE, Antares, etc



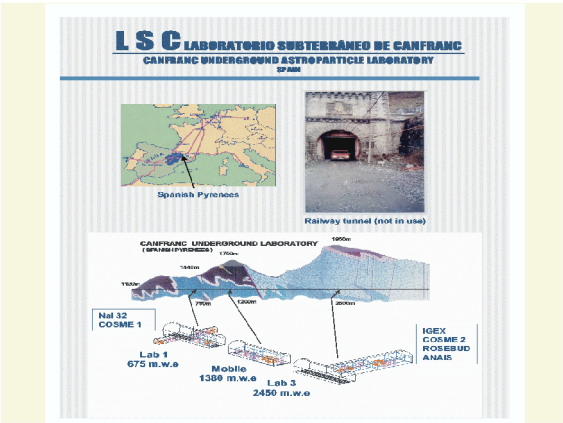
complementary techniques are getting into the interesting region of parameter space

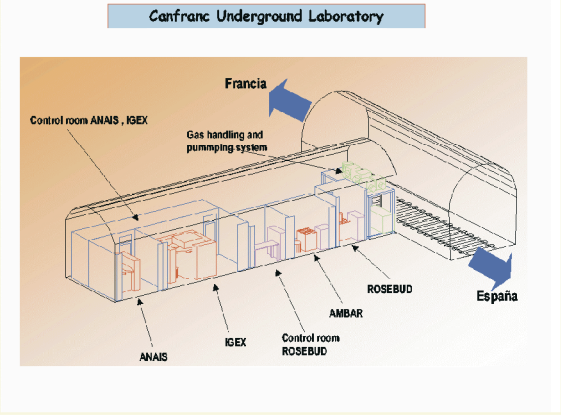


Underground Laboratories













ICARUS in LNGS Hall B

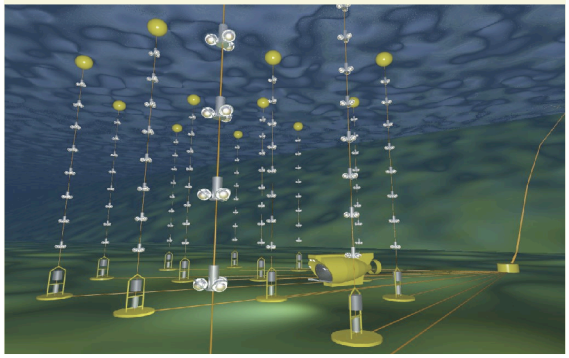


Origin & properties of Cosmic Rays

1. Neutrinos (Antares)
2. Gamma rays (Magic)
3. Charged particles (Auger)
4. Antimatter? (AMS)

*"Science is the art of replacing unimportant questions that can be answered by important ones which cannot" Edward B. Ferguson Jr. 1976.

ANTARES 0.1 km^2 detector

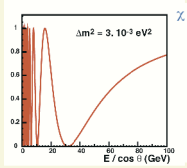


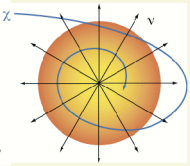
ANTARES

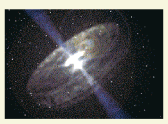


Photomultiplier to detect Cherenkov light

ANTARES

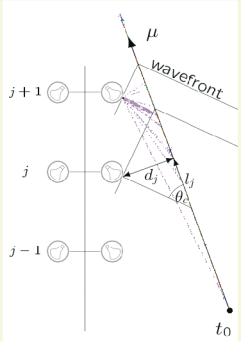


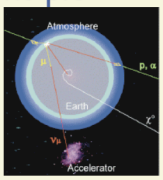




Low Energy	Medium Energy	High Energy
ν oscillations (Observation of first oscillation minimum)	Neutralino search Self-annihilation at center of Earth, Sun, Galaxy $\chi\chi \rightarrow \ell, \rightarrow \nu$	ν from (extra-) galactic sources SN remnants, AGN, GRB, …

Detection principle





$\cos\theta_c$

medium properties

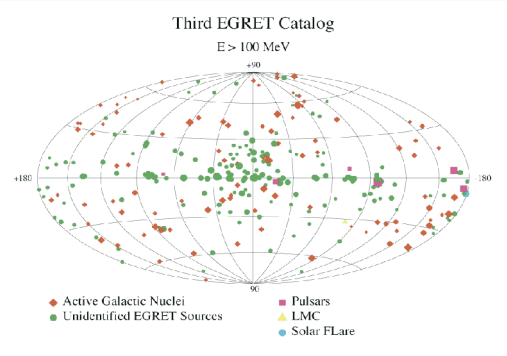
δ_x = 20 cm

$\delta\theta$ = 0.2 deg.

δ_t = 1 ns

$\nu_\mu + N \rightarrow \mu + X$

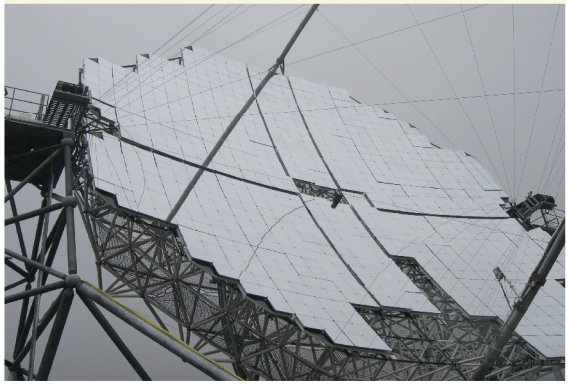
Gamma-ray galactic sources



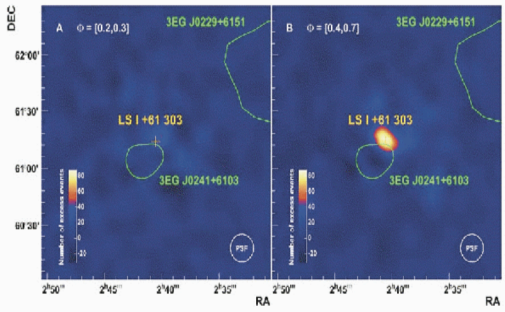
El Roque de los Muchachos (MAGIC)



Magic, the inauguration day



Microquasar (MAGIC)



AUGER

Purpose: Detect & discover the origin of cosmic rays with

$E > 10^{19}$ eV

2 deployments (each cost 50 M$)

In each hemisphere:

1600 detectors (surface) + 30 fluorescence telescopes in

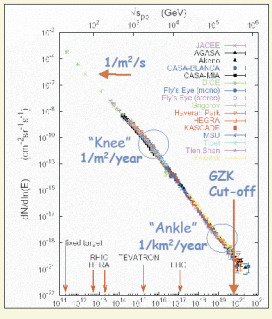
3000 km^2

South: Provincia de Mendoza, Argentina

North: ?

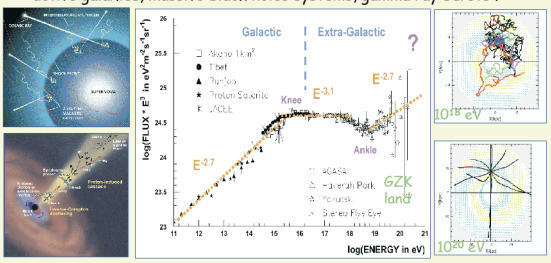
Cosmic Rays Spectrum

- High energy cosmic rays consist of protons, nuclei, gammas,...
- Measured flux extends to $s^{1/2}$ ~ 400 TeV
- Highest energy particles are extremely rare
- Supernova shock fronts can accelerate particles upto 10^{15} eV
- Above ~10^{15} eV, presumably acceleration is in AGNs (?)
- How do UHECR protons evade the GZK cut-off at ~7 x 10^{19} eV (if source is >100Mps away)?
- UHECR manifest themselves as extended air showers (EAS) --an indirect way of measuring CRs

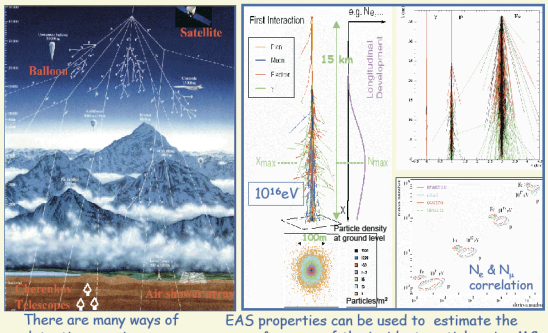


Misteries of the Spectrum

- Protons are trapped in our Galaxy (μG B-fields) up to ~10^{17} - 10^{18}eV
- Protons can travel straight above ~10^{20}eV
- Supernova shockwave acceleration up to ~10^{15} eV
- Above the knee the acceleration mechanism is essentially unknown: active galaxies, massive black holes systems, gamma ray bursts ?



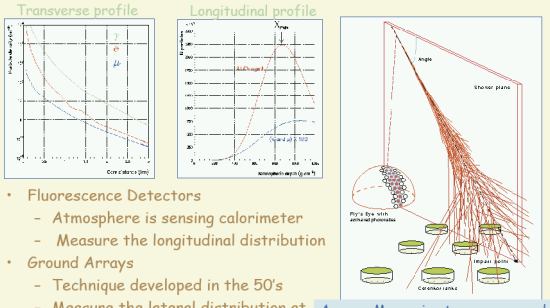
Extended Air Showers



There are many ways of detecting cosmic rays

EAS properties can be used to estimate the mass & energy of the incident particle using MC

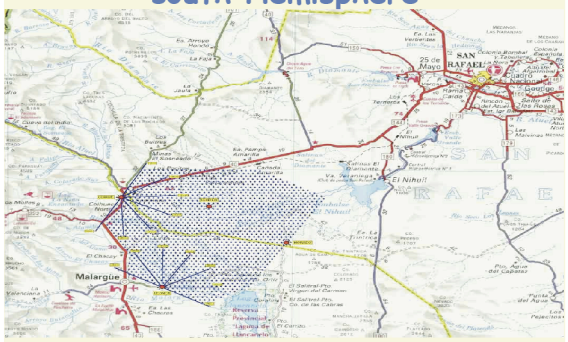
The Atmosphere as a Calorimeter



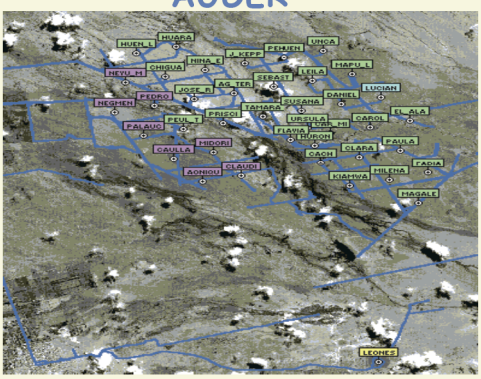
- Fluorescence Detectors
  - Atmosphere is sensing calorimeter
  - Measure the longitudinal distribution
- Ground Arrays
  - Technique developed in the 50's
  - Measure the lateral distribution at ground

Auger - Measuring transverse and Longitudinal shower profiles

Auger observatory in the south Hemisphere



AUGER



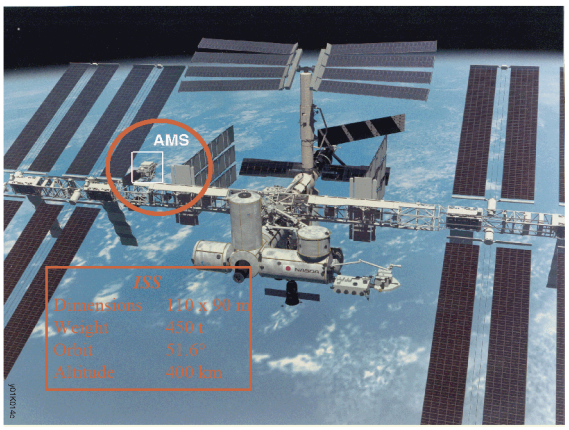
AUGER



Spanish Contribution:

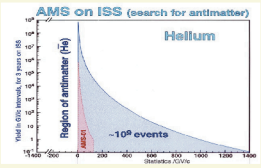
Solar panels (1000) at surface detectors (Cerenkov)

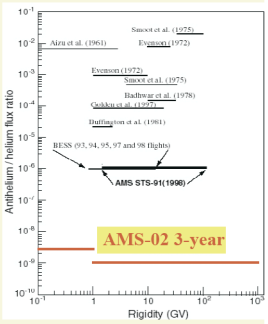
Shower simulation



AMS-02 sensitivity to Antimatter

In 3 years AMS
Will detect 10^9 He
with E $\lesssim$ 1 TeV



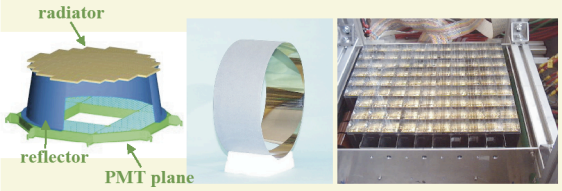


AMS-02 Ring Imaging Cerenkov Counter

3 cm silica aerogel (n=1.05) radiator

680 multianode (4x4) PMTs

$\sigma(\beta)/\beta = 0.1\%$ @ $\beta = 1$ (protons)



The Neutrino mass

Experimental detection of neutrino oscillations

⇓

Neutrinos have got mass

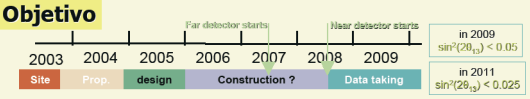
How large is $m(\nu_e)$, what is the mass hierarchy?

1. Tritium b-decay
   $m(\nu_e)^2 = -0,6 \pm 2,2 \pm 2,1\ eV^2$ Mainz
   P $m(\nu_e) \leq 2,3eV$ (95%)
2. 0νbb-decay
   $\langle m(\nu_e) \rangle \gg 0,4\ eV$ to be confirmed
3. ν-Oscillations
   $7,3\times10^{-5}eV^2 < \Delta m_{12}^2 < 9.3\times10^{-5}eV^2$ solar
   $1,6\times10^{-3}eV^2 < \Delta m_{23}^2 < 3.6\times10^{-3}eV^2$ atm.
   ⇒ There is a ν with $m_{\nu i} \geq 0,009eV$ and one with $m_{\nu j} \geq 0,05eV$
4. Cosmology
   $\sum m_{\nu i} \leq 0,7eV$

Double-CHOOZ (France)



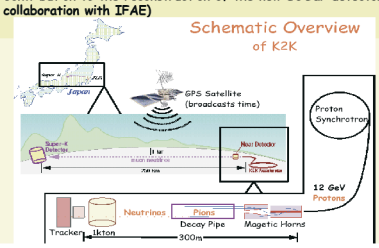
Objetivo



Neutrino Oscillations-K2K

KEK to SuperKamiokande:
- Confirm the evidence of oscillations observed by Super-Kamiokande
- Measure the disappearance of muonic neutrinos in a beam that is produced in KEK and detected in Super-Kamiokande

Two major contributions:
- Extrapolation of the neutrino flux measured in the near detector to the far detector (from Harp data)
- Contribution to the reconstruction of the new SciBar detector (in collaboration with IFAE)



Conclusions

1. Spain is very active in

   Particle & Astroparticle physics and in a continuous growth.

2. We are deeply involved in the CERN program, and more modestly with DESY, Fermilab, SLAC, KEK programs.

3. There are two important infraestructures for Astroparticle Physics: the Canfranc underground lab and El Roque de los Muchachos observatory.

4. My best wishes for a very nice workshop !

The LHC machine status, calibration run and commissioning plans

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Abstract

The status of the ongoing LHC installation is reported with some attention given to the long straight sections around the experiments. An overview of the proposed commissioning schedule for 2007 and 2008 presented. This schedule includes a calibration run at the end of 2007 which aims to deliver collisions at 450 GeV beam energy. The details of this run and planned beam conditions are summarised. The full commissioning to 7 TeV will be a challenging exercise and an overview of the plans for 2008 is given.

Finally, the beam related issues associated with the LHC upgrade are briefly introduced.

I. MACHINE STATUS

At the time of writing (September 2006) LHC installation is proceeding at a very committed pace around the whole ring. The situation is summarised in table 1 [1].

Table 1: Status of LHC installation – September 2006 (c/o Sylvain Weisz)

Sector	Phase
1-2	QRL installation has now passed 90%, with all internal welds done. Pressure tests October 28th.
Point 2	Water cooled cables installation in progress in UA23, done in UA27. Air treatment and cooling units installation close to completion in UA23/27. Installation of power converters just started in UA23, done in UA27.
2-3	Cryo-magnet installation in progress, from RZ33 to Point 2 (14 dipoles and 1 SSS in place).
LSS3	Installation of power converters in UJ33 slightly delayed. Installation of control cables and refurbishing of warm cables in progress in RZ33.
3-4	Cryo-magnet transport and alignment in progress: all 154 dipoles in place, 44 (out of 45 available) arc SSS in place. Interconnection in progress.
Point 4	RF installation in progress: 4 cavities (ACS) in place, damper (ADT) and pick-up (APWL) in place in LSS4R. RF wave guides in place, connection to cavities in progress. Klystron installation in progress (7 out of 16 in place in UX45). Interconnection D4-Q5/DFBML and Q6/DFBMG about to start in LSS4R.
4-5	All available cryo-magnets are in place. Interconnection in progress, above nominal rate
Point 5	RR53 & USC55: Short circuit tests finish next week. Low-β, DFBXF, D1 (6 MBXW) in place in LSS5R. UJ56-RR57: power converters, DYPE racks, energy extraction systems (DQR/DQS) in place.
5-6	Cryo-magnet transport in progress: 153 MB and 41 SSS in place. Dump 62 - installation of vacuum pipe in progress in TD62. All elements in place, about 50% welded
Point 6	UA63: ready to start short circuit tests UA67: power converters in place, cabling (AC, DC, Control & Water cooled) in progress, MKD generators and associated control racks installation in progress
6-7	Cryo-magnet installation: Dipoles during week-ends. 26 dipoles and 22 SSS in place (06/10/2006)
LSS7	Straight section: all services completed UJ73, UJ76 & UJ77: power converters and energy extraction systems in place TZ76 gallery: control cabling completed, modification of ventilation duct in progress
7-8	DFBAN (7R) installed 25/09, Q6.R7 installed 29/09, DFBMH installed 02/10. All cold elements in place. Interconnections in progress.
LSS8L	Cold parts: Interconnection DFBAO-HCM/LCM in progress. Interconnections done for low-β/DFBX, Q4-D2/DFBMA, Q5/DFBMC. Warm parts: All components in place (except large beam pipe between D1-D2)
LSS8R	Cold part: DFBMB, DFBMI & DFBMJ in place, interconnection in progress (Low-β, D2-Q4, Q5, Q6). Warm part: MKI & MSI installed, power cabling of MKI in place
8-1	All cryo-magnets in place, interconnections in progress. DFBAA-HCM ready and transported.
LSS1L	Interconnection of low-β/DFBX, D2-Q4/QRL in progress.

As can be seen from table 1, the installation of the cryogenic distribution line has almost finished, with the last sector (1-2) due for completion in October 2006. Magnet installation is progressing well with over 1000 out of the total 1728 superconducting magnets having been installed on 5th September 2006. Installation of the last magnets is foreseen for March 2006.

One class of critical components are the feed boxes which couple the room temperature cables into the cold mass. There are four types: DFBAs for the arcs; DFBMs for the stand alone quadrupoles; DFBXs for the inner triplets and the DFBLs for the superconducting links. Planned delivery and installation over the coming months put some of these items on the critical path; in particular the DFBAs which have to be in place before a sector cool-down can proceed.

The critical job of interconnecting the dipoles and short straight sections is ongoing. Around 1700 interconnects have to be made with four teams working in parallel around the ring. This is huge, painstaking, industrialised job which involves: vacuum plus leak checks, bellows, RF contacts, cryogenics, thermal shield, heat exchanger, as well as around

10,000 bus bar superconducting splices using induction welding and around 50,000 corrector circuit splices using ultrasonic welding.

The latest schedule for 2007 is available [2] and it clearly represents a huge challenge with the express goal of finishing the job of interconnections, the cool-down and at least partial hardware commissioning of all sectors.

II. 450 GeV Commissioning

The 2007 schedule also foresees a calibration run at the end of the year. It is envisaged that 4 sectors of the LHC will be hardware commissioned to a reduced level allowing powering of the main circuits to a 1.1 TeV equivalent level. As a prelude to the six weeks beam time, the schedule for the end of the year includes ring wide access tests and a ring wide machine checkout phase.

The beam time will be made up of 3 weeks beam commissioning with single beam, at low intensity for the most part, followed by 3 weeks collisions. Initial collisions will be with a single bunch on a single bunch followed by a staged increase to 156 bunches of 4 x 10^{10} protons per bunch or possibly higher. Luminosities should range from 1.3 10^{28} to 2.6 10^{29} $cm^{-2}s^{-1}$. The potential performance of this phase is summarised in table 2.

Table 2: Potential performance at 450 GeV

Number of bunches	43	43	156	156
Bunch current [10^{10}]	2	4	4	10
Intensity per beam	8.6 10^{11}	1.7 10^{12}	6.2 10^{12}	1.6 10^{13}
Beam energy [MJ]	0.06	0.12	0.45	1.1
Beta* [m]	11	11	11	11
Luminosity [$cm^{-2}s^{-1}$]	10^{28}	7.2 10^{28}	2.6 10^{29}	1.6 10^{30}
Event rate [kHz]	0.4	2.8	10.3	6.4

The collisions phase will be interleafed with low intensity single beam machine development; in particular we would hope to perform initial ramping tests to 1.1 TeV.

The commissioning run at 450 GeV is potentially very useful operationally. It allows critical checks of the whole machine with beam – principally aperture and polarities – with increased lead time for problem resolution following the run. Although reduced hardware commissioning is planned, it's clear that the machine has to be in safe state for 450 GeV operations. It will be necessary to cycle the main circuits to around 20% of nominal; quenches, with or without beam, are still possible and the Quench Protection System shall be operational, Power Interlock Controllers etc. must be qualified to the necessary level.

A. 450 GeV Machine configuration

1) Optics:

The plan is to use a partially squeezed optics with:

- β*= 11 m in IR 1 & 5
- β*= 10 m in IR 2 & 8

The squeeze is essentially limited by triplet aperture [3]. To keep things simple and to gain experience with a machine setup close to the nominal, no further squeezing is planned.

2) Crossing angles & Separation bumps

The crossing angle bumps will be off allowing 1, 12, 43, 156 bunches per beam. 156 represents the maximum number of bunches that can be injected without parasitic encounters in the interaction regions. The separation bumps will be brought on for two beam operation.

3) LHCb

The displaced IP at LHCb will necessitate the shifting of a certain number of bunches to provide collisions at point 8. It is foreseen to shift 4 out of 43 bunches, or 24 bunches out of 156. In these configurations the other experiments will experience parasitic collisions 75/2 ns away from their nominal collision point.

4) Solenoids & Exp. Dipoles etc.

It is envisioned that the experiments' solenoids and the dipole magnets in LHCb and Alice will be off to start with. Bringing then on will be scheduled in the single beam phase before collisions are established.

B. Phases

The main phases of 450 GeV beam commissioning are shown in table 3.

Table 3: Outline of 450 GeV commissioning phases

	Phase	**Main Objectives**
1	First turn	Commission end TI2, TI8, injection region, BPMs, BLMs, thread first turn, polarity checks.
2	Circulating beam	Closed orbit, chromaticity, energy matching, tune, RF capture.
3	Initial commissioning	RF, control & correction, transverse diagnostics, linear optics checks, beam dump, machine protection.
4a	Measurements	Beta beating, aperture, field quality checks, transfer functions, BLMs.
4b	System commissioning	RF, transverse feedback, BLMs to machine protection, tune PLL, collimators and absorbers.
5a	Two beam operations	Parallel injection, separation bumps, instrumentation and control.
5b	Establish collisions	Establish collisions, luminosity monitors, collimation, solenoids.
5c	Increase intensity	Collimators, longitudinal feedback, multi-batch injection.

For beam commissioning the basic probe beam will the pilot: a single bunch of 5 - 10 x 10^9 protons with possibly reduced emittance. For more precise measurements, the

intensity is increased to a super pilot: a single bunch of around 3 to 4 x 10^{10} protons.

Given appropriate system commissioning and control of the key beam parameters the number of bunches will be increased gradually to 4, 12 bunches etc. pushing towards 43, 156 bunches of 3 to 4 x 10^{10} protons per bunch.

156 x 4 x 10^{10} represents 2% of the nominal beam intensity. This can clearly quench and/or damage a magnet at 450 GeV and it is imperative that the machine protection system be commissioned appropriately.

The estimated beam time required for commissioning two beam operation at 450 GeV is shown in table 4.

Table 4: Estimated time required for commissioning two beam operation at 450 GeV

	Phase	Time [days]	Beam
1	First turn	4	1 x pilot
2	circulating beam	3	1 x pilot
3	Initial commissioning	3	1 x pilot++
4a	Measurements	1-2	1 x pilot++
4b	System commissioning	2-3	1 x pilot++
5a	Two beam operations	1	2 x pilot++
5b	Collisions	1-2	2 x 1 x 10^{11}
		16 days	

Given an operational efficiency of 60%, the estimated time to establish first collisions gives an elapsed time of about 26 days with the obvious caveat that machine availability might well be lower during this period. There are some opportunities for parallel development and parasitic studies and one might hope gain some time here. Full details are available at [5].

C. *Machine Issues*

1) Luminosity measurement

The low luminosity will be straining the bounds of machine luminosity monitors installed at points 1 & 5 (ionization chambers produced by LBL, these are known as the BRAN). There will be low rates of high energy neutrons in the BRAN, with potentially high background, and a low signal/noise ratio. Initial collisions with single bunch 1.0 x 10^{11} are planned to give the BRAN something to bite on. Complementary signals from the experiments would clearly be advantageous.

Other ideas being pursued machine side to get a handle on the luminosity at this stage include the use of the beam-beam coupling signal from high sensitivity BPMs, the use of Schottky monitors and the possibility of installing dedicated scintillators.

2) Background

Background in the experiments' insertions will come from beam gas interactions and beam halo. There are four main contributing factors:

- residual gas within the experiments. The experiments themselves should be baked out and this contribution should be low;
- residual gas in the long straight sections (LSS);
- elastic scattering from gas in the adjacent cold sectors (the gas pressures here could be relatively high at start-up);
- the cleaning inefficiency of the collimator systems in IR7 & IR3.

The 450 GeV run will represent stage 0 for the vacuum system. There will have been no beam conditioning, minimal pump-down time in some sectors. The conditions will be given by the static vacuum. Potentially some LSSs could be un-baked and consequently no NEG activation. The experiments' LSS are, however, the priority and should be baked. The vacuum life time shall be greater than 35 hours and 50 hours for 2007 and 2008 respectively compared with the 100 hours nominal. For a detailed analysis, see [5].

3) Halo

Beam halo generation in the LHC will arise from: RF noise; intra beam scattering (IBS); optics mismatch; beam-gas etc. In addition, poor parameter control (tune, chromaticity) will lead to poor lifetime and stream particles to aperture limit. Nominally the halo is cleaned by the collimation system with the resulting tertiary halo potentially finding its way to the experiments insertion and the tertiary collimators installed there.

However, firstly, at 450 GeV the aperture limit is very much the arcs and the dispersion suppressors, and secondly a minimal collimator scheme is foreseen at this stage of commissioning. With low beam intensity only primaries and the TCDQ (downstream dump absorbers) will be used. At higher intensity the primary and secondary collimators will be closed to protect the arcs, however, the tertiary collimators and absorbers are not planned to be used. Un-squeezed with the tertiary collimators out and the aperture limit in the arcs one will expect low halo losses in interaction regions.

III. COMMISSIONING 2008

A staged approach is clearly going to be useful to tackling the complexity of the LHC. It is envisaged to stage the commissioning of the machine with beam as follows:

- a possible sector test [6,7] which would provide an invaluable milestone;
- 450 GeV commissioning run [4];
- Stage 1 - physics 43 x 43 with moderate intensities;
- Stage 2 - move to 75 ns with the aim of moving to intensities around 3 - 4 10^{10} protons per bunch;
- Stage 3 - move to 25 ns with the aim of moving to intensities around 3 - 4 10^{10} protons per bunch. This will need to be followed by long shutdown for installation of phase 2 collimation and additional beam dump dilutors;

- nominal 25 ns running pushing towards design intensity and full squeeze.

This staged approach will allow phased commissioning of the key sub-systems with increasing intensity. Thus initial commissioning can be performed without having to face the dangers of high beam intensity and the full rigours of the final machine protection system.

The phases of full commissioning are shown in table 5. The shaded phases are those that will possibly be addressed during the calibration run. It can be seen that the run should enable considerable progress to be made on the full commissioning plan. Although there will obviously be hand-over costs in breaking the commissioning into two stages, these costs are probably equaled by the benefits that an extended period of consolidation after the calibration run would provide.

Table 5: 7 TeV Beam commissioning phases

Phase	Main goals
Transfer and Injection	Pilot on axis through to TDI
First turn	Pilot threaded – single turn
Circulating beam	Multiple turns, RF capture.
450 GeV: initial commissioning	Q, Q', coupling. Polarities and apertures checked; basic optics checks.
450 GeV: consolidation	Well adjusted beam parameters, key instrumentation operational, machine protection as required for ramp.
450 GeV: two beam operation	Two beams, well adjusted beam parameters.
Snapback: single beam	Single beam, good transmission through snapback, requisite measurements.
Ramp: single beam	Single beam to top energy, beam dump commissioned in ramp, PC tracking checked
Single beam to physics energy	Stable beam at top energy, measurements, beam parameter adjustment.
Two beams to physics energy	Separation bumps on. Commission ramp with two beams
Physics: un-squeezed	establish collisions
Partial squeeze: single beam	single beam in steps through squeeze, parameter control
Physics: partial squeeze	Two beam through squeeze - collide

Briefly, 2008 will see the completion of the hardware commissioning to the 7 TeV level. This will be followed by a one month machine checkout and test phase, leading to the beam commissioning outlined in table 5. Given the experience gained during the calibration run, this is estimated that it will take around 2 months elapsed time to establish collisions at 7 TeV. Thus an optimistic schedule would see collisions at or near full energy around mid-2008.

IV. LHC UPGRADE - BASICS

The motivation for an LHC upgrade is essentially statistics driven: if the LHC achieves design luminosity within, say, four years, the statistical halving time will exceed 5 years within a further four years, some what more if the push to ultimate intensity and luminosity can be achieved. Thus given the present schedule and these assumptions it is reasonable to plan a phase 1 upgrade before around 2014 [8].

The upgrade options are many and varied, and only a brief attempt is made here to introduce the issues by way of motivation for discussions on this subject later in the workshop.

A. Basics Issues

Some of the main issues that must be addressed when considering an upgrade are:

- head-on beam-beam tune shift;
- long-range beam-beam in the interaction regions;
- the effect of the crossing angle: firstly via the geometrical luminosity reduction factor (F), the larger the crossing angle the larger the reduction in luminosity; and secondly the larger the crossing angle, the larger the required aperture in the insertion quadrupoles;
- β^* and beam size at IP: the smaller the β^*, the larger the beam size in the triplets and larger the required aperture;
- radiation deposition in the insertion region.

B. Options

There are many ways of playing on these various factors.

- More and shorter bunches. This could be achieved by either increasing the bunch intensity or by increasing the number of bunches by reducing bunch spacing with major implications on the RF systems of the injectors depending on the spacing chosen. The positives are a large luminosity gain with minimal event pile up.
- Increase bunch intensity via injector upgrade such as a 1 TeV superconducting SPS.
- Fewer and longer bunches give a large luminosity gain with no e-cloud, lower total beam current, easier collimation & machine protection
- The idea of super bunches has been abandoned because the event pile up becomes intolerable.
- Increase F by reducing the crossing angle and fighting long range with beam-beam compensation schemes.
- Decrease the effect of the crossing angle by using crab cavities.
- Redesign the insertions and reduce beta*, this implies new stronger quadrupoles with larger apertures. Variations include: placing a dipole first near IP to allow small crossing angle; dipole first and large crossing angle and long bunches or crab cavities. Dipoles first plus quad triplets or quad doublets. Dipoles inside the detector. Quadrupoles first, pushed in closer to IP.

Space precludes detailing these options. For more details see any of the many summary talks on the subject at, for example, [8,9,10].

C. Summary

Several LHC IR upgrade options are currently being explored. The baseline scenario includes variations on: a reduction of β* to 0.25 m, an increased crossing angle and a new bunch-shortening RF system. The corresponding peak luminosity with ultimate beam intensity is 4.6 x 10^{34} $cm^{-2}s^{-1}$ at the two interaction points. Electron cloud effects and/or cryogenic heat loads may exclude the possibility to double the number of bunches.

There is considerable amount of research and development ongoing. This research includes magnets, crab cavities, long range beam-beam compensation. A major conference devoted to the LHC upgrade was held Valencia in October 2006 under the auspices of CARE – HHH [10].

V. References

1. Sylvain Weisz, LHC TCC minutes, September 2006.
2. http://sylvainw.home.cern.ch/sylvainw/planning-follow-up/Schedule.pdf
3. Minutes of the 59th LTC Meeting held on 5.7.2006 http://edms.cern.ch/lhc_proj/plsql/lhcp.page?p_number=7700
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5. A. Rossi, Residual Gas Density Estimations in the LHC Insertion Regions IR1 and IR5 and the Experimental Regions of ATLAS and CMS for Different Beam Operations, CERN-LHC-Project-Report-783, Geneva : CERN, 15 Sep 2004.
6. M. Lamont, "LHC Sector Test", LHC Performance Workshop 2004, CERN-AB-2004-014.
7. M. Lamont, http://cern.ch/lhc-injection-test
8. F. Ruggiero, LHC beam performance and luminosity upgrade scenarios, Univ. "La Sapienza", Rome, 20–24 March 2006.
9. W. Scandale, LHC Luminosity and Energy Upgrade, EPAC 06, 27 June 2006.
10. http://care-hhh.web.cern.ch/CARE-HHH/LUMI-06/

CMOS directions in industry

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ST Microelectronics

Crolles2 Alliance

CMOS Directions in Industry

12th Workshop on Electronics for LHC and futute Experiments

25-29 September 2006, Valencia, Spain

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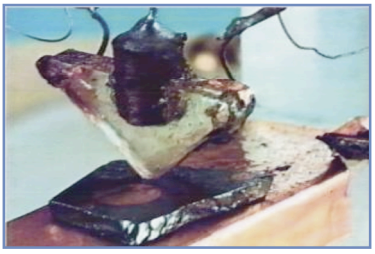
SUMMARY

- Moore's-Law scaling impact on digital and analog circuits
- Regular reconfigurable structures (Networks on Chip, Multi-core Architectures, and Sampled Analog and RF circuits.
- More than Moore and 3D System Integration
- Fundamental physical limiting effects (oxide tunneling, finite sub-threshold slope, etc)
- New CMOS structures (new dielectric materials, band-gap engineering
- Statistical nature of parameter variabilities
- Device architectures beyond 45nm (new metal-dielectrics gate stacks, stressed-strained channels, etc.
- New tightly-coupled system-architecture-circuit-device design.
- Conclusion: Where is all this going?: The Process, Circuit, Architecture and System Design, and Manufacturing unique synergies and new innovative Cooperation-Competition industrial schemes.

2

Point Contact Semiconductor Amplifier



By Bardeen and Brattain, Dec. 16, 1947

3

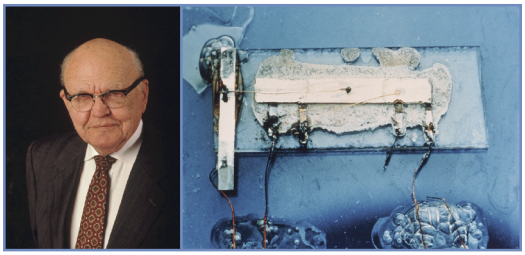
1956 Nobel Prize for Transistor Invention at AT&T Bell Labs



J. Bardeen *W. Shockley* *W. Brattain*

4

Texas Instrument, 1st IC in 1958



Jack Kilby (Nov. 8, 1923- June 7, 2005) 2000 Nobel
1Tr (Germanium), 1C, 3R, Oscillator, 0.04 inch X 0.06 inch.

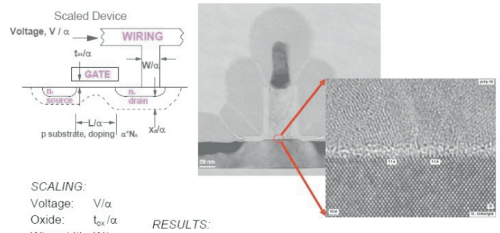
5

Scaling:

Moore's-Law scaling impact on digital and analog circuits

6

CMOS Scaling Rules

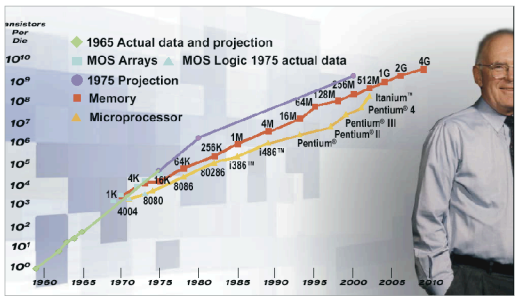


SCALING:
Voltage: V/α
Oxide: t_{ox}/α
Wire width: W/α
Gate width: L/α
Diffusion: x_d/α
Substrate: α * N_A

RESULTS:
Higher Density: ~α^2
Higher Speed: ~α
Power/ckt: ~$1/\alpha^2$
Power Density: ~Constant

Passive Power:
–Gate leakage
–Sub-threshold leakage (source-drain)

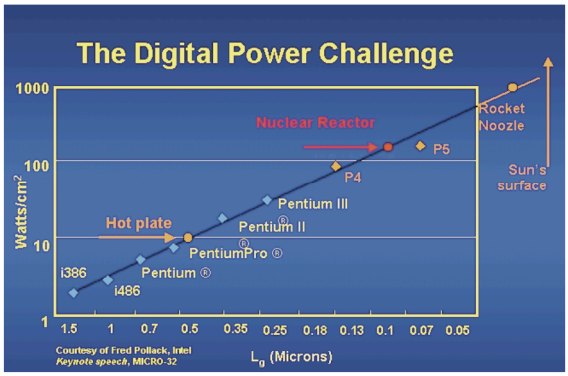
SOC Integration: Scaling and Digital



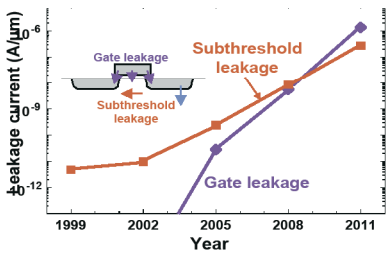
Source: Intel, Intel Developers Forum, 2/2003

Source: Intel

The Digital Power Challenge



Drain and Gate increase in leakage currents

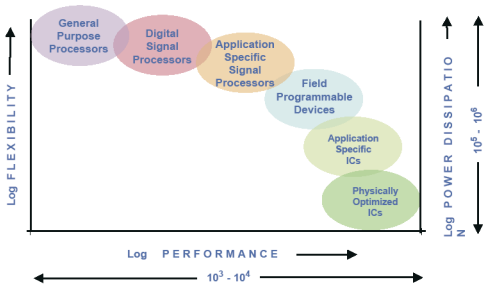


Soft error rates increases 2X for SRAMs at each new proces node and Single event transient below 45nm could escalate 3 decades.

Reasons:Vdd decrease, Q nodes decrease, higher clock speeds.

- ❑ **Signal Integrity, ElectroMagnetic Coupling and RF (SI/EMC/RF) solutions.**
- ❑ **Single and Multiple Event Upsets protections at architectural,circuit and device levels.**
- ❑ **Single event latch up.**
- ❑ **Hardened libraries (process and design levels).**
- ❑ **Fail safe architectures.**
- ❑ **…**

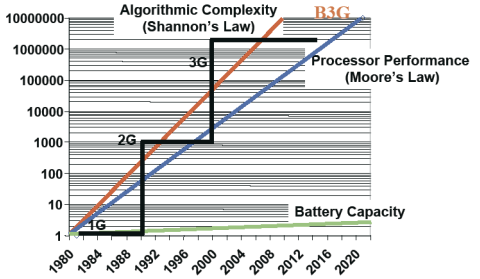
Implementation Space



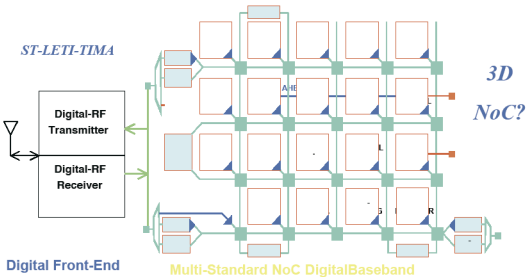
Source: T.Noll, RWTH Aachen

The Algorithmic Driving Force

Shannon asks for more than Moore can deliver...



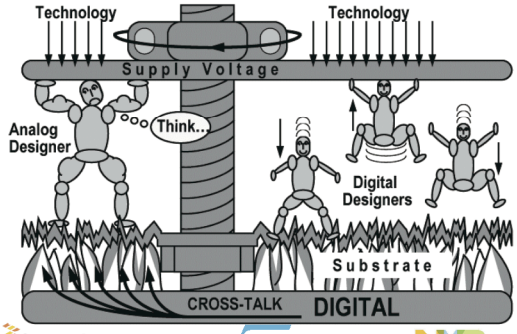
Reconfigurable Globally Asynchronous-Locally Synchronous Network-on-Chip Transceiver Architecture



Key Processing Elements (PE's) Required

- Multistandard operation will require:
  - *FIR Filters*
  - *FFTs, IFFTs*
  - *Viterbi and Turbo Decoders*
  - *Rakes*
  - *Synchronizer Blocks*
  - *….etc*
- These parametrable blocks can be arranged in a programmable NoC architecture:
  - *Array of heterogeneous processing elements*
  - *Programmable / parameterizable PEs (reconfigurable logic)*
  - *Routing interconnect*
  - *Soft loadable*

Analog and Digital Scaling Challenges



Panic…



…But it's nice to have Good Digital Neighbors...

- Digital Compensation can be included almost for free:
  - –Account for Analog Imperfections through Digital Compensation (Linearity, Offsets, etc)
  - –Digital self-calibration and dynamic element matching can be used at small feature size and low voltage.

Analog Systems Considerations/Trends

- Discrete time techniques will work better in scaled submicron CMOS
  - Switched-capacitor (SC) techniques, Bucket-Brigade, CCD's, etc.
  - Switches usually need complementary devices ($V_{DD} > V_{TN} + V_{TP}$)
  - For analog: lower V_T typically offer:
    - ✓ Faster switches
    - ✓ Better amplifier input range
- Dynamically adjust supply and threshold design parameters to center the design in the presence of process variations!
- Digital Compensation can be included almost for free:
  - Account for Analog Imperfections through Digital Compensation (Linearity, Offsets, etc)
  - Digital self-calibration and dynamic element matching can be used at small feature size and low voltage.
- Auto-ranging, Self-Calibration, Self-Test, Active Linearization, Reconfigurability allowing a different performance/cost tradeofs.
  - These functions will have an impact on the Silicon cost, largely compensated by the Total Cost Reduction induced.

Continuous Time versus Discrete Time and Scaling

- Discrete time techniques will work better in scaled submicron CMOS
  - Switched-capacitor (SC) techniques, Bucket-Brigade, CCD's, etc.
  - Switches usually need complementary devices ($V_{DD} > V_{TN} + V_{TP}$)
  - For analog: lower V_T typically offer:
    - Faster switches
    - Better amplifier input range

Reconfigurable Front-End Radios

- The concept of Integrated Reconfigurable Radios (SW Defined Radios = SDR) has been around for many years, but it regains interest for mobile terminals now because advances in silicon technologies make it possible.
- The reason for this regain of interest is also the expectation that a unique radio architecture, reconfigurable by SW to different standards will add flexibility and strongly reduce costs, by simplifying board development, calibration, and BOM, reducing the total cost seen by the phone manufacturer.

A full Mobile System-on-Chip:

- Full HW/SW integration of
  - Communication + Application + Intelligence
- Intelligence should include:
  - For digital functions:
    - Fine-grain integrated power management and control, including all available techniques at all levels (from SW to partitioning, design and process). Also Reconfigurability for standards.
    - Design for Test, Self-Test, Fault observability, detection and correction.
  - For Front-End (RF and ABB) functions:
    - Auto-ranging, Self-Calibration, Self-Test, Active Linearization, Reconfigurability allowing a different performance/cost tradeofs.
- HW/SW overhead:
  - These functions will have an impact on the Silicon cost, largely compensated by the Total Cost Reduction induced.

…But, What about the Reconfigurable Digital Baseband ?

More Than Moore's Law (ITRS2005)

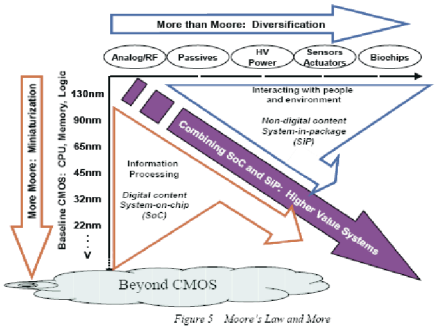
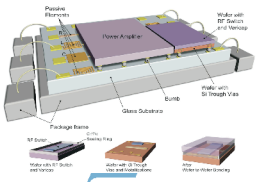


Figure 5 Moore's Law and More

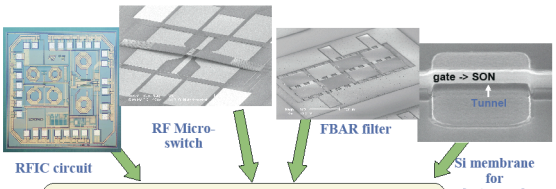
SOC + SIP Integration

- Module integration offers the possibility to integrate different technologies together
  - SOC Transceiver
  - GaAs or Si (Power Amplifier)
  - Passive components
  - RFMEMS components



RFMEMS Integration

- Allows System on Chip (SoC) approach
- Opens the door to Innovative RF Front-End Architectures



Co-integration of ICs, passives and RF-MEMS
New RF functions through strong co-development between technology & RF design

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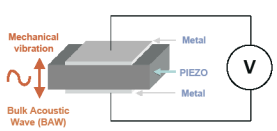
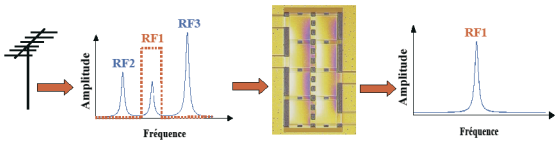
BAW Filter Operating principle

(LETI-ST)





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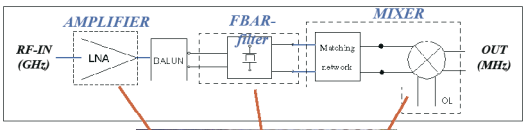
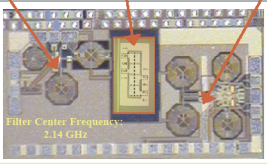
RF Front-End FBAR integration





ST-LETI-CSEM
ISSCC-2005

RF Process:
BiCMOS7RF
(SiGe-0.25 µm)

Challenge: Process Integration and new Architectures

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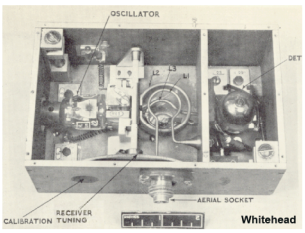
The Old Super-Regenerative Receiver

- Invented by Armstrong in 1922
- Possible radio operation above device f_T, allowing:
  - -Subthreshold biasing and/or
  - -High carrier frequency, increasing integration
- Modern devices/MEMS can solve traditional problems with architecture:



1940s - Super-regenerative
f_c= 500MHz (above f_T)
2 active devices
high quality passives – hand tuning required

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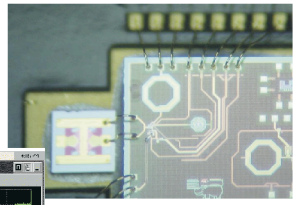
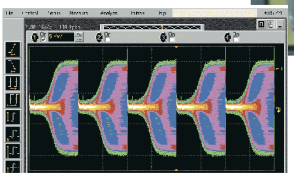
Receiver Implementation

BWRC, ISSCC-2005

0.13µm CMOS





OOK Modulation

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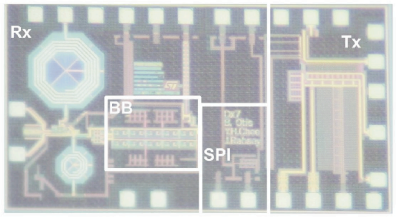
Next Generation: (1x1.9)mm² Rx/Tx



- Above IC Components (inductors, crystals, capacitors)
- Full Digital control of analog/RF blocks
  - -Rx Osc Frequency: 3.15MHz x 500kHz
  - -BB Filter BW/Gain
  - -Tx Tank Frequency

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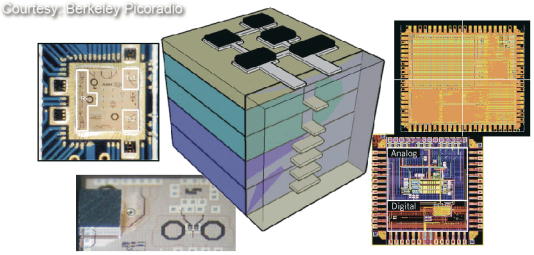
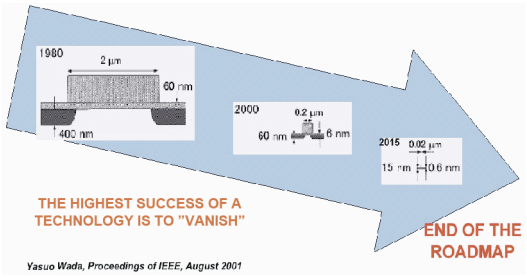
Dealing with Mixed-Everything through Packaging



SIP for Optimum Technology Mix

- Close to the antenna, advanced SiGe:C Bipolars will continue to play an important role for very low NF @ Low-Power, as well as for RF Power Amplification @ High Efficiency, for battery life.
- Medium Voltage / Power functions such as Energy Management and Audio will continue to be handled by adapted MOS/Bip Technologies for reliability and lowest cost. High density/quality capacitors will be key differenciators.
- This Technology Mix will be possible by SIP techniques also allowing Hi-Q Passives and MEMS Integration.

The Ultimate Nanometer MOS

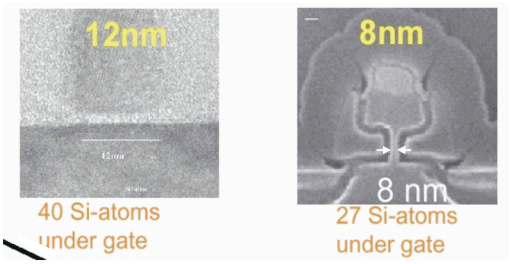


WAYS BACK TO HEALTHY SCALING

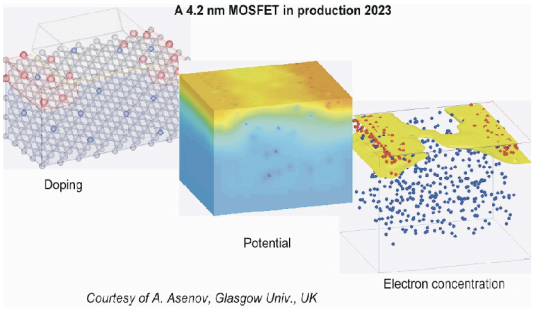
TECHNOLOGY BOOSTERS

- H- K DIELECTRICS (Improves MOS behavior)
- METAL GATES (Improves Ion/Ioff)
- STRAINED Si, SiGe and Ge (Improves Mobility)
- DEVICE STRUCTURE (Reduces Ioff)
- SOI / SON (Improves speed, Reduces Ioff)
- MULTIPLE GATES (Improves MOS, Reduces Ioff)
- BALLISTIC TRANSPORT (Improves Speed)

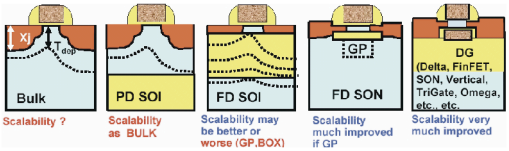
REAL NANO- MOSFETs



The Discrete Nature of Matter is Visible

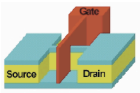


FUTURE MOS ARCHITECTURE EXAMPLES

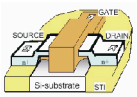


But…How do we do any useful design with these devices? Will they buy us any renewed life for Digital / Analog / RF ??

We need to start working on these questions NOW !

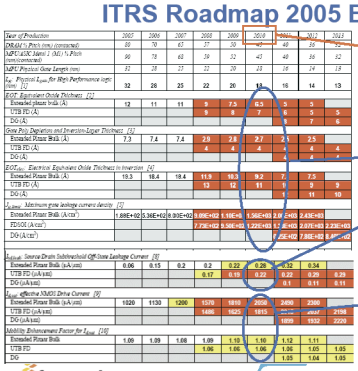


Tied Gates side-wall conduction: DELTA, FINFET, OMEGAFET,...



Tied gates planar conduction: DG SON

ITRS Roadmap 2005 Edition



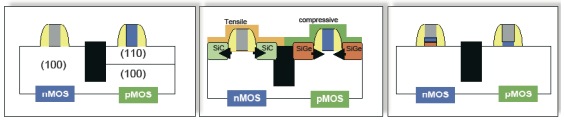
Products ready in 2010

High-k + Metal gate

Bulk or FDSOI

Mobility booster
-Process induced strain
- Crystal orientation
- sSOI
- Dual channel

CMOS Worlwide Trends



Mobility enhancement
Orientation for pMOS

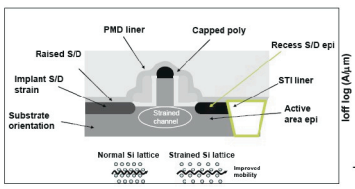
Strain
Tensile strain for nMOS
Compressive strain for pMOS

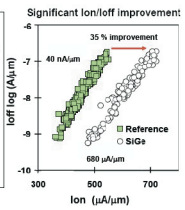
Dual MG + Higk-K
for reduced gate tunneling

IEDM-2005 Trends

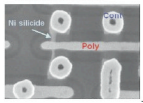
- **Standard CMOS platform**
  - **Main 65nm and 45nm general plaform stay in bulk conv.**
- **Strained Silicon**
  - **Intensively full strain sources re-use**
    - NMOS= SMT+high tensile stress
    - PMOS= eSiGe+high compressive stress
  - **Very interesting IBM paper using hybrid subtsrate types (bulk)**

Strained-Silicon Performance Enhancement



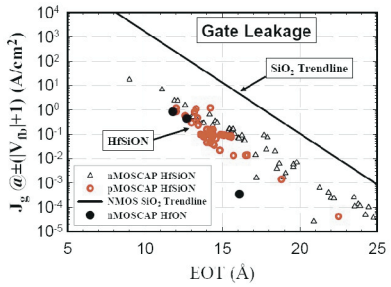


Defect in Silicon



1. Strained Si can produce an increase in I_{on} without a degradation in I_{off}.
2. Stress-induced defects can occur in the silicon if the stress is not applied properly.

Impact of High-k on Gate-Dielectric Leakage



$$EOT = \left(\frac{k_{SiO_2}}{k_{high-k}}\right) \bullet (thickness)_{high-k}$$

High-k thickness can be kept relatively thick, to control leakage, while EOT can be made quite low.

Paper 3.5

A 65nm Ultra Low Power Logic Platform Technology using Uni-axial Strained Silicon Transistors Intel Corporation

	High Perf. CPU Process	Low Power SOC Process	
Transistor	Logic	Logic	I/O
Nom. Volt	1.0/1.1 V	1.2 V	1.5-5 V
Tox	1.2 nm	1.7 nm	5 nm
Min. Gate Length	35 nm	55 nm	140 nm
Cont-Gate Pitch	220 nm	240 nm	400 nm
SRAM Cell (um²)	0.57 µm²	0.68 µm²	

Table 1. Summary of key transistor design rules of low power vs. high performance CPU version of Intel 65 nm technology.

	High Perf. CPU Process	Low Power SOC Process	Lithography
MT1	210 nm	210 nm	193 nm
MT2	210 nm	210 nm	193 nm
MT3	220 nm	220 nm	193 nm
MT4	280 nm	280 nm	248 nm
MT5	330 nm	275 nm	248 nm
MT6	400 nm	280 nm	248 nm
MT7	720 nm	420 nm	248 nm
MT8	1080 nm	1080 nm	248 nm

Table 2 Summary of key interconnect design rules of h performance process [4] and this work.

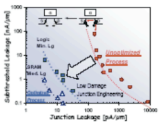


Fig. 6 Low damage junction engineering to mitigate junction leakage while maintaining good short channel effect.

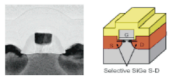
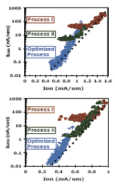


Fig. 1 XTEM of PMOS uni-axial strained silicon transistors developed for low power process.



g. 8 NMOS (upper) and PMOS (lower) total leakage, I_{DS}, s, drive currents, Ion, at 1.2V. Process I and II are un-ptimized processes with better Ioff and short channel con-ol, but worse total leakage due to gate/junction leakages.

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Paper 3.4

Design of High Performance PFETs with Strained Si Channel and Laser Anneal,

IBM System & Technology Group, 1Chartered Semiconductor Manufacturing, Ltd,
2Infineon Technologies AG, 3Samsung electronics Co., Ltd,
4Toshiba America Electronic Components, Inc.,

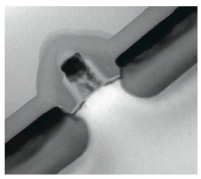

Fig. 2 Cross-section of a typical transistor with e-SiGe and CSL

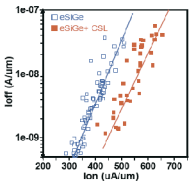

Fig. 5 Ion vs Ioff at |Vdd|=1V of PFETs with e-SiGe and PFETs with e-SiGe + CSL.

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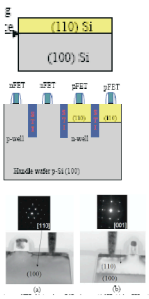
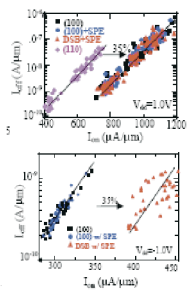
Paper 10.3

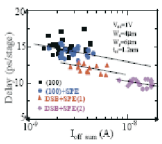
IBM

High Performance CMOS Bulk Technology Using Direct Silicon Bond (DSB) Mixed Crystal Orientation Substrates

Chun-Yung Sung[1], Haizhou Yin, Hung Y. Ng, Katherine L. Saenger[2], Victor Chan, Scott W. Crowder, Jinghong Li, John A. Ott[3], Robert Bendernagel, Jeremy J. Kempisty, Victor Ku, H.K. Lee, Zhijiong Luo, Amita Madan, Renee T. Mo, Phung Y. Nguyen, Gerd Pfeiffer, Michael Raccioppo, Nivo Rovedo, Devendra Sadana[1], Joel P. de Souza[1], Rong Zhang, Zhibin Ren and Clement H. Wann







Comments:
NMOS → (100) <100>
PMOS → (110) <110>
Very nice integration

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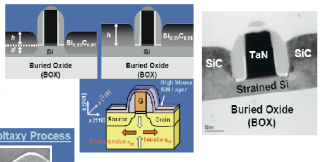
Paper 20.3

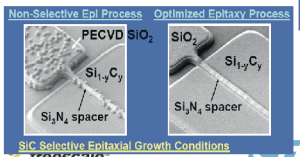
Thin Body Silicon-on-Insulator N-MOSFET with Si:C S/D Regions for Performance Enhancement

Singapore University

Main features:
- Si:C S/D stressor
- Metal gate
- I_D improved by 35% (70nm gate)
- (100) substrate
- various channel orientations
- <100> found the with tensile strain

Concept = Si:C SEG → tensile uni-axis strain





Comments:
- SiC SEG with [C] of about 1%
- Specific Epi process development

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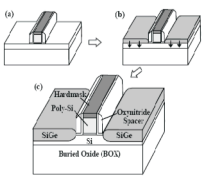
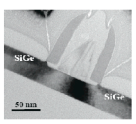
Source/Drain Germanium Condensation for P-Channel Strained Ultra-Thin Body Transistors

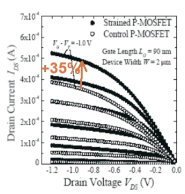
National University of Singapore

This paper reports a novel technique to fabricate uniaxial compressive strained P-channel transistors with Silicon-Germanium (SiGe) source and drain (S/D) stressors.

The process involves local Ge condensation of a selectively grown SiGe region, thus driving Ge into and enriching the Ge concentration in the source and drain regions adjacent to the transistor channel.







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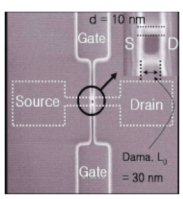
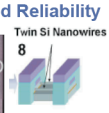
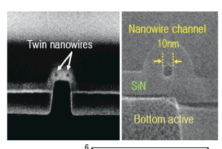
High Performance 5nm radius Twin Silicon Nanowire MOSFET(TSNWFET) : Fabrication on Bulk Si Wafer, Characteristics, and Reliability

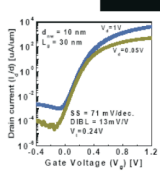
Samsung Electronics Co.

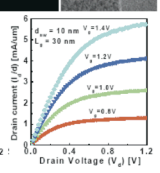






!Drain current normalized with the diameter of the nanowire!





freescale semiconductor

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Paper 36.7

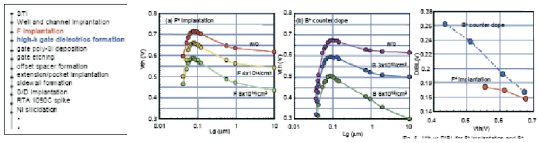
Vth-tunable CMIS Platform with High-k gate Dielectrics and Variability Effect for 45nm node

T. Hayashi, M. Mizutani, M. Inoue, J. Yugami, J. Tsuchimoto, M. Anma, S. Konori, K. Tsukamoto, Y. Tsukamoto, K. Nii, Y. Nishida, H. Sayama, T. Yamashita, H. Oda, T. Eimori, and Y. Ohji

Renesas Technology Corp., Wafer Process Engineering Development Dept.

Renesas

F implant for Vth correction (poly/ HfSiON!)



615/221 µA/µm @ 20pA/µm (V_{dd}= 1.2V)

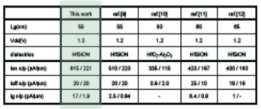
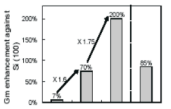


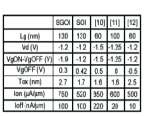
Table 1. Performance comparison with other papers.

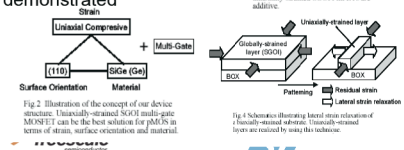
30.1 **High Performance Multi-Gate pMOSFETs using Uniaxially-Strained SGOI Channels**

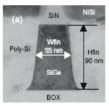
MIRAI-ASET+, MIRAI-AIST++, Toshiba Ceramics*

- "Ultimate" PMOS device combining Multi-gate, SiGe channel, uniaxial strain & (110) conduction
- Strong performance improvement demonstrated





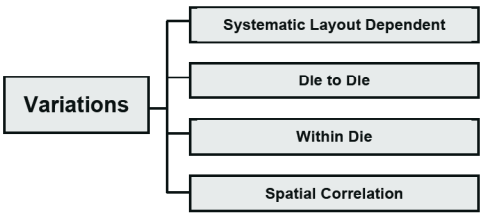




Variability matters !

- Identify main sources
- SRAM test structures
- Analog test structures (Diff. Pair matching, Switches, etc ..+ passives…)
- Digital basic cells (RO's, Adders, Latches, etc)
- Environment measurements (Vdd noise, couplings, etc)
- Wiring RC delay characterization
- Using variability information
  - Exhaustive Data Mining approach
  - Variability modeling
  - Yield models
- Impact on Circuit / Device / Process design choices

Categorizing Variations



Systematic and Random Device Variations

Parameter	Random		Systematic
Channel dopant concentration Nch	Affects Δvth		Non-uniformity in the process dopant implantation dosage diffusion
Gate Oxide thickness Tox	Gate- dielectric-channel interface roughness		Non-uniformity in the process oxide growth
Gate length L	Line edge roughness		Lithography Proximity effects Resist development etching, etc

The Importance of Variability

- Absolute amount of variability for a particular design
  - Often captured in design corners
  - Determines power penalty for guaranteeing performance
  - Limits benefits of technology scaling
  - Avoid pessimistic Over-Design
- Nature of variability
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Fab-2-Fab
  - Spatial vs. Temporal (incl. intermittent)
  - Systematic vs. random
  - Correlated vs. uncorrelated

Digital Systems Considerations/Trends

- Process and design interaction: DFM
  - Physical design impacts yield
  - Power management and Analog/RF integration require more extensive modeling
  - Distributed test and debug functions
- Fine-grain integrated power management and control necessary, including all available techniques at all levels (from SW to partitioning, design and process). not all transistors need min Lg or LVt.
- Scaling: Intrinsic chip speed grows faster than I/O bandwith: Data will be trapped on-chip.
- Layout/Routing techniques will outperform Low-K approaches.
- Multi-Core Trend: Simpler cores, smaller clock zones, shorter wires, lower latencies: Network-on-Chip, higher IP-reuse, higher parallelism/multi-threading, smaller cores/redundancy: improved yields, self-repair.
- Needed: more design for testability, better yield models, higher I/O bandwidth, better system-level power reduction.

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Conclusion

Where is all this going?:
Process, Circuit, Architecture and System Design, and Manufacturing unique synergies and new innovative Cooperation-Competition industrial schemes.

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…Evolution of Integration…

- *SSI*
- *MSI*
- *LSI*
- *VLSI*
- *SoC (System on a Chip)*
- *NoC (Network on a Chip)*
- *LoC (Laboratory on a Chip)*
- *CiH (Chip in a Human)*
- *…HiC ?... maybe not…*

freescale semiconductor NXP 57

There is plenty of room at the bottom

(Richard Feynman, 1960)



- "Can we write the Encyclopedia Brittanica on the head of a pin?"
- "Can we write all books into the volume of a pin?" (3D)
- "How do we writ it?"
- How do we read it?"
- "Can we see atoms?"
- "Can we move and manipulate individual atoms?"
- "Can we build machines at the atomic level?"
- "Can we synthesize substances with physics, not chemistry?"
- "Can we build an atomic-scale computer?"

freescale semiconductor NXP 58

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3D electronics

SUNTHARALINGAM Vyshnavi

MIT Lincoln Laboratory-USA

3-D Integrated Circuit Fabrication Technology for High Density Electronics

Vyshnavi Suntharalingam

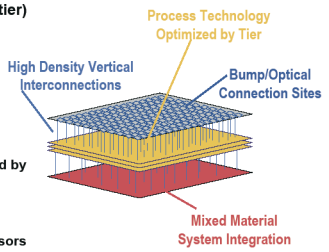
Brian Aull, Robert Berger, Jim Burns, Chenson Chen, Jeff Knecht, Chuck Stevenson, Brian Tyrrell, Keith Warner, Bruce Wheeler, Donna Yost, Craig Keast

12th Workshop on Electronics for LHC and Future Experiments
15th International Workshop on Vertex Detectors
25-29 September 2006

This work was sponsored by the Defense Advanced Research Projects Agency under Air Force contract #FA8721-05-C0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

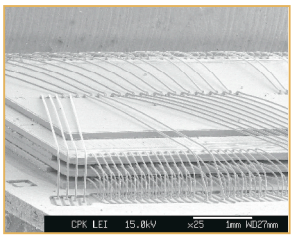
Motivation for 3-D Circuit Technology

- 3-D Circuit = Multi-layer (multi-tier) stacked circuit
- Advantages
  - Reduced interconnect length
  - Reduced chip size
  - Reduced parasitics
  - Reduced power
  - Fabrication process optimized by tier function
- Applications
  - High bandwidth microprocessors
  - Mixed material system integration
  - Advanced focal planes
    - Local computation and/or memory
    - 100% fill-factor diodes



Pad-Level "3D Integration" *Die Stacking*

Stacked-Die Wire Bonding



ChipPAC, Inc.

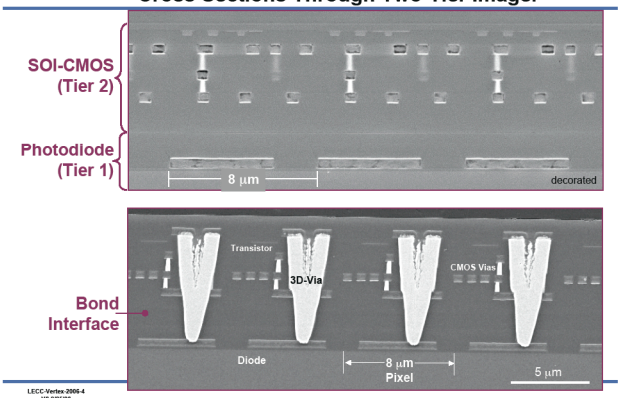
Stacked Chip-Scale Packages



Tessera, Inc.

In Production!

Pixel-Level 3-D Integration
Cross Sections Through Two-Tier Imager

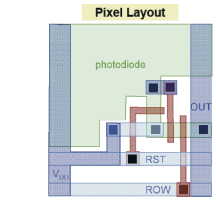


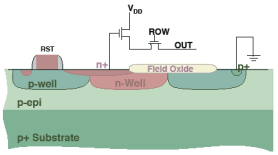
Outline

- Advantages of Vertical Integration for Focal Planes
  - MIT-LL Demonstration of Three-tier ring oscillators
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

Limitations – Standard Bulk CMOS APS
Monolithic APS – MAPS

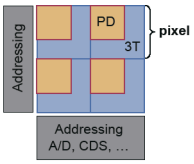
- Fill factor compromised
  - Photodetector and pixel transistors share same area
- Low photoresponsivity
  - Shallow junctions
  - High doping
  - Limited depletion depth
- High leakage
  - LOCOS/STI, salicide
  - Transistor short channel effects
- Substrate bounce and transient coupling effects





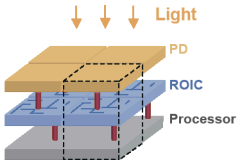
Advantages of Vertical Integration

Conventional Monolithic APS



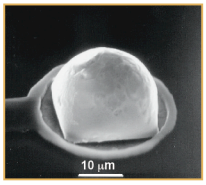
- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

3-D Pixel

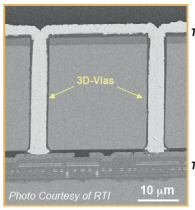


- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes

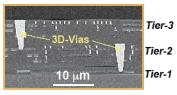
Approaches to 3D Integration
(Photos Shown to Scale)



Bump Bond used to flip-chip interconnect two circuit layers



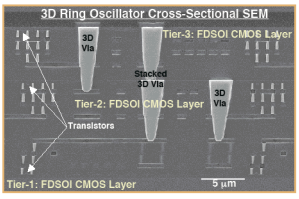
Two-layer stack with insulated vias through thinned *bulk* Si

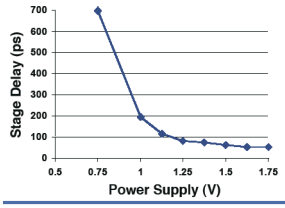


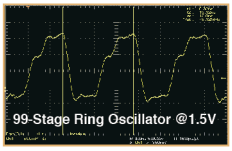
Three-layer circuit using Lincoln's SOI-based vias

3-Tier, 3D-Integrated Ring Oscillator
(DARPA 3DL1 *Multiproject Run*)

- Functional 3-tier, 3D-integrated ring oscillator
  - Uses all three active transistor layers, 10 levels of metal and experimental *stacked 3D-vias*
  - Demonstrates viability of 3D integration process







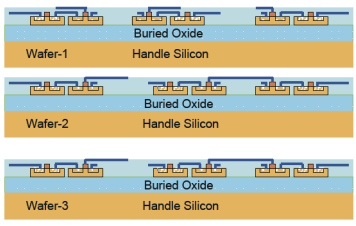
Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence and Five Key Elements
  - Low dark current photodiodes
  - Silicon on Insulator (SOI) circuits
  - Low-temperature, wafer-scale oxide-to-oxide bond
  - Precision overlay
  - High-density vertical interconnection
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

3-D Circuit Integration Flow-1

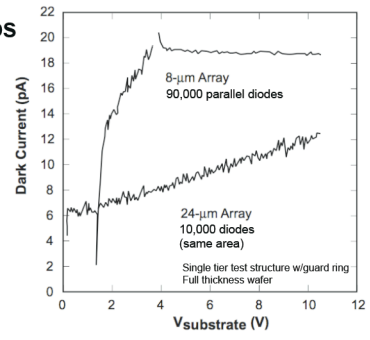
- Fabricate circuits on SOI wafers
  - SOI wafers greatly simplify 3D integration
- 3-D circuits of two or more active silicon layers can be assembled

Wafer-1 can be either Bulk, SOI, or Compound Semiconductor



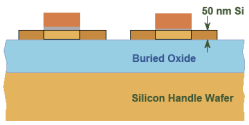
1. Low Dark Current Photodiodes

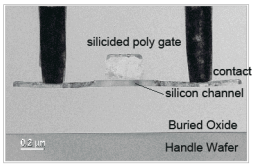
- Photodiode independent of CMOS
- High-resistivity substrates
- Back-illumination process
- Photodiode leakage <0.2nA/cm² @ 25°C
- Similar results after 3D-stacking



2. Silicon-On-Insulator Circuits

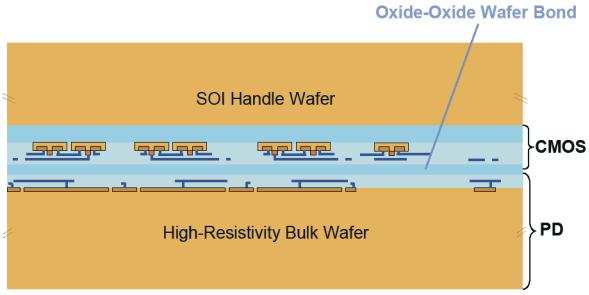
- 3.3-V, 350-nm gate length, fully depleted SOI CMOS
- Buried oxide
  - Dielectric isolation
  - Reduced parasitic capacitances
  - Enhanced radiation performance
  - Essential wafer-thinning etch stop





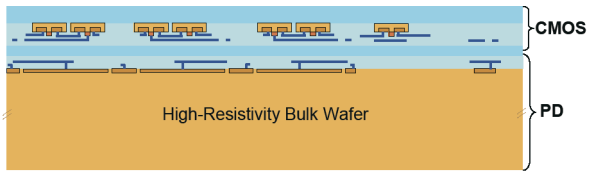
3-D Circuit Stacking

- Invert, align, and bond Tier 2 to Tier 1



3-D Circuit Stacking

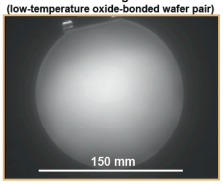
- Remove handle silicon from Tier-2



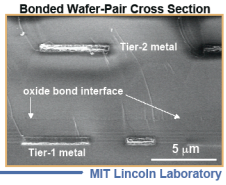
3. Low Temperature Oxide Layer-to-Layer Bonding

- Deeply scaled 3-D interconnect technology requires robust wafer-to-wafer bonding technology
- MIT-LL low temperature oxide bonding process provides
  - Thin and controllable bondline
  - Enables use of standard IC high aspect ratio contact etch and plug fill technologies
    - ~475ºC process
  - Allows for 3-D interconnect to be sintered
  - Standard, high reliability semiconductor material

IR Image
(low-temperature oxide-bonded wafer pair)



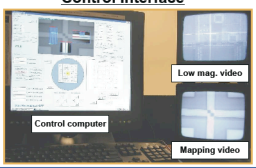
Bonded Wafer-Pair Cross Section

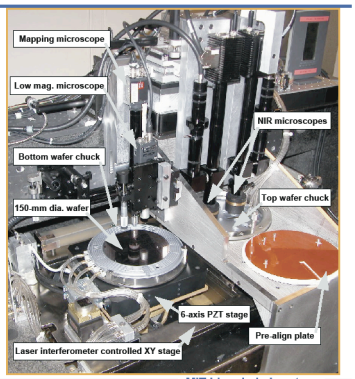


4. Precision wafer-to-wafer overlay

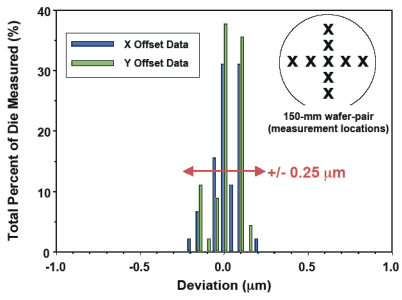
- Provide a wafer-to-wafer alignment accuracy compatible with a submicron 3D Via
- Tool based on modern IC wafer stepper technology
- 0.5 μm 3-sigma overlay demonstrated

Control Interface



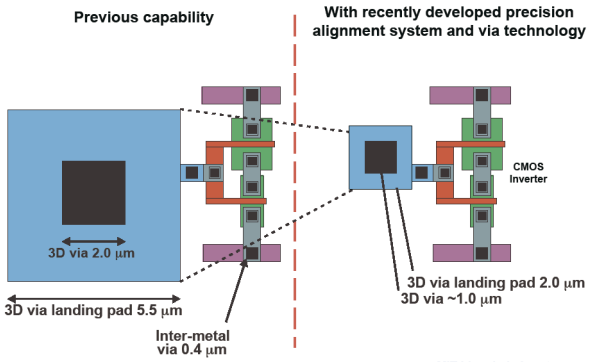


Repeatability Data
MIT-LL Precision Aligner

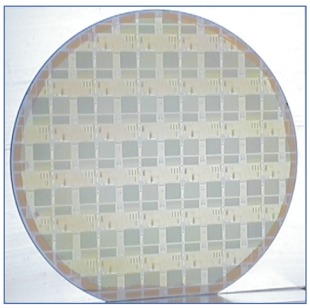


- Data from five repeated alignments of same wafer pair
- Nine die measured per alignment

3D Via Layout Comparison
(Based on MIT-LL 180nm FDSOI CMOS rules)



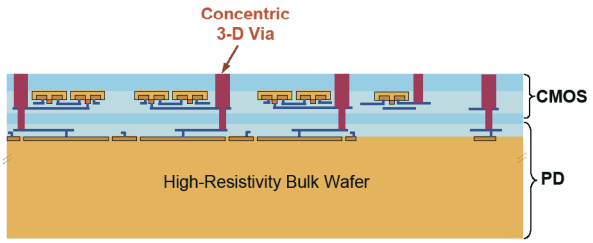
Bonded Two Wafer Imager Stack



150-mm Diameter Wafer Pair

Inter-Tier Via Connections

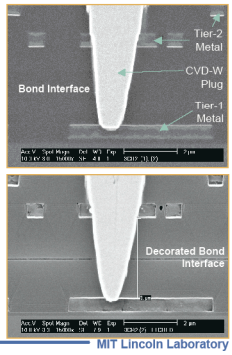
- Pattern, etch, and fill 3-D vias
- (Additional circuit tiers could be added)

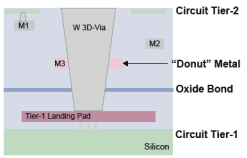


5. High Density, High Yield, Compact 3D-Via

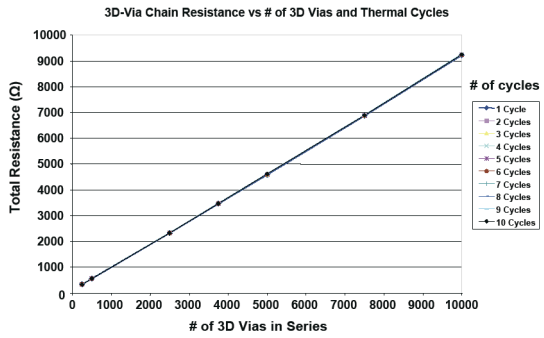
- Leverages standard high-yield IC process technology for 3D interconnection
  - High density plasma oxide etch of via hole
  - Chemical vapor deposition of tungsten plug
  - Chemical mechanical planarization (CMP) to form damascene plug

3D Via Cross-sections



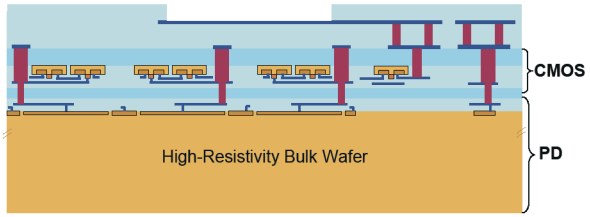


Thermal Cycle Effects on 3D-Via Chains
Thermal Cycle: 300 K/ 77 K/ 300 K



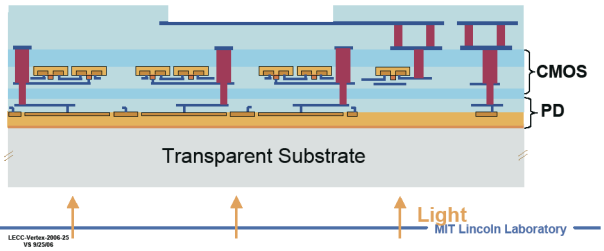
Back Metal-1 and Back Metal-2

- Deposit and pattern Back Metal-1
- Deposit and CMP ILD
- Deposit and pattern Back Metal-2
- Sinter



Completed Back-Illuminated CMOS Imager

- Thin photodiode substrate to 50μm
- Epoxy bond to quartz

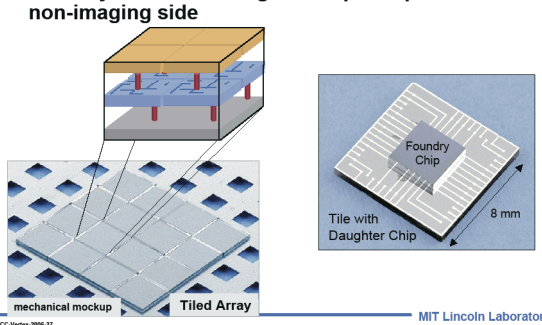


Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - **Two-tier backside-illuminated visible imager**
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

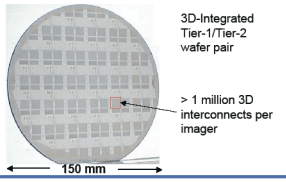
Four-Side Abuttable Goal

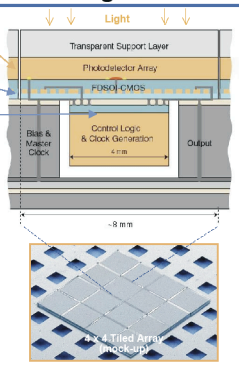
- 3-D CMOS imagers tiled for large-area focal planes
- Foundry fabricated daughter chip bump bonded to non-imaging side



Four-Side Abuttable Vertically Integrated Imager

- Silicon photodetector layer (Tier-1)
  - Four-side abuttable 1024 x 1024 array of 8μm x 8μm pixels
- Address and readout layer (Tier-2)
  - 3.3 volt FDSOI CMOS layer
- Timing, control, and analog-to-digital electronics (Tier-3)
  - MOSIS fabricated chip bump bonded to detector array
- Active-pixel architecture for radiation tolerance

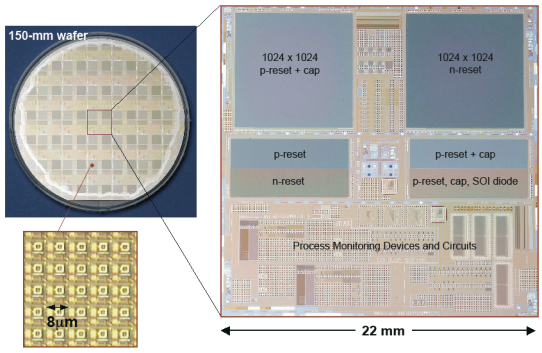




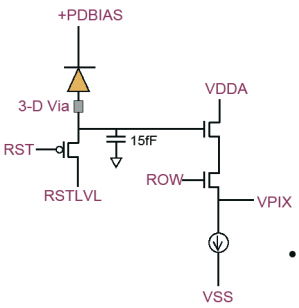
Design Goals

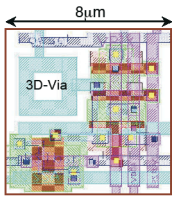
- Four-side abuttable Active Pixel Sensor
- 1024 x 1024 array of 8μm x 8μm pixels
- 3-D interconnections per pixel
- 3.3-V operating voltage
- Full digital control and readout at 10 fps

Completed 3D-Stacked Imager
Wafer and Die Layout



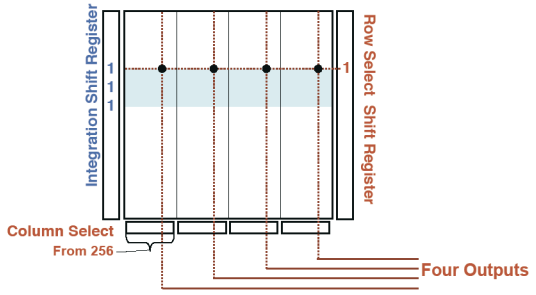
3T Pixel Schematic and Layout





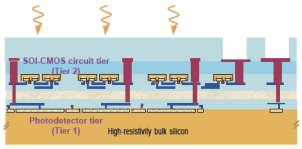
- **Design Variations**
  - pFET Reset with 15fF capacitor
  - nFET Reset with no capacitor

1024 x 1024 Imager Array Architecture



Preliminary Tier-1-2 3D Imager Test Results

- **Electrical probe station preliminary imager test result using *frontside* illumination**
  - **Final processing steps will result in unobstructed backside illuminated device**



**35-mm slide image projected through CMOS-circuit-side of 3D-integrated imager on chip test station*

1024 x 1024 Image from *FIRST* 3D-Integrated Wafer Pair*



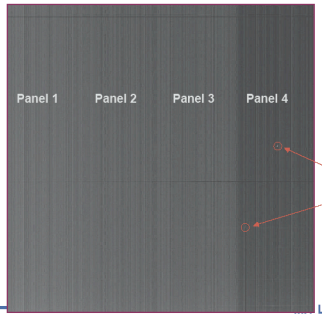
Image acquired at 10 frames/sec
(Background Subtracted, Pixel Yield > 99.9%, 3.8M transistors)

Presented at 2005 ISSCC

Sample Dark Background

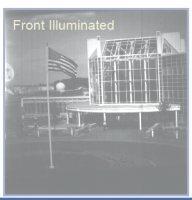
- **Raw image without fixed pattern noise suppression**
- **Dominant yield detractor is row/column drop-outs**

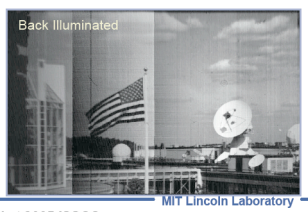
Four Analog Outputs



Four-Side Abuttable Vertically Integrated Imaging Tile

- **Wafer-Scale 3D circuit stacking technology**
  - **Silicon photodetector tier**
  - **SOI-CMOS address and readout tier**
    - **Per-pixel 3D interconnections**
  - **1024 x 1024 array of 8 μm x 8 μm pixels**
  - **100% fill factor**
  - **>1 million vertical interconnections per imager**





Presented at 2005 ISSCC

Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence

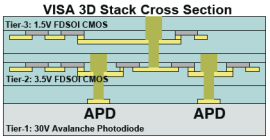
- **MIT Lincoln Laboratory Demonstrations**
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - **Three-tier laser radar focal plane**
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material

- Summary

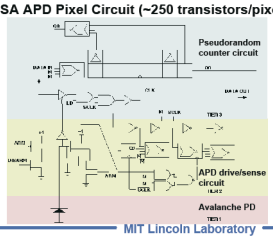
Three-Tier Laser Radar Focal Plane

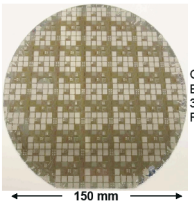
- Based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 demonstration circuit (scalable to large imager formats)
  - Pixel size reduction from 100 μm to 30 μm
  - Timing resolution reduction from 1 ns to 0.1 ns
  - 100x reduction in voxel volume

VISA 3D Stack Cross Section



VISA APD Pixel Circuit (~250 transistors/pixel)

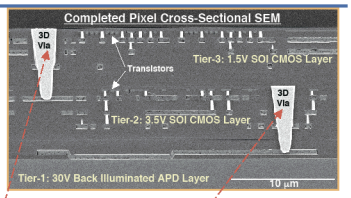




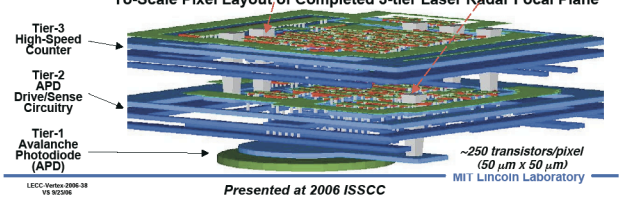
Completed Backside-illuminated 3-tier, 3D Laser Radar wafer

Functional 3D-Integrated, 3-Tier Avalanche Photodiode Focal Plane

- *VISA* laser radar focal plane based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 format
  - 50-μm pixel size



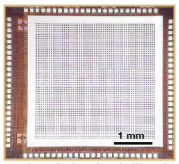
To-Scale Pixel Layout of Completed 3-tier Laser Radar Focal Plane



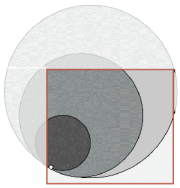
Presented at 2006 ISSCC

64x64 LADAR Focal Plane
First Demonstration of 3-Tier Focal Plane

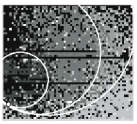
- Rudimentary ladar image of 28" long cone with 8-in timing resolution
  - Timing circuit limited to only 9-bits of its full 12-bit range



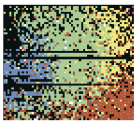
Complete 3-tier, back-illuminated 64 x 64 APD Laser Radar



Orientation of cone image on focal plane



Grayscale range image with superimposed contours



False color range image

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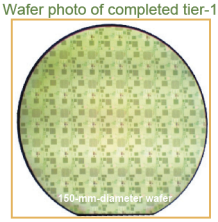
3-D IC *Multiproject Run* Completed
(Three 180-nm, 1.5 volt FDSOI CMOS Tiers)

- MIT-LL 3D circuit integration technology
- Preliminary 3D design kits developed
  - Mentor Graphics – *MIT-LL*, Cadence – *NCSU*, Thermal Models – *CFRDC*
- Design guide release 11/04, fab start 6/05, 3D-integration complete 3/06

Wafer photo of completed tier-1



Concepts being explored in run:

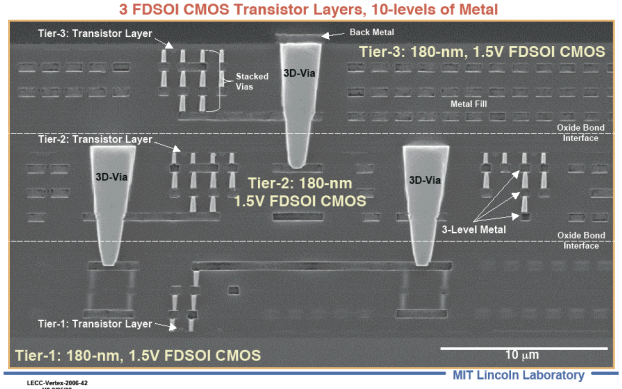
- 3D FPGAs, digital, and digital/mixed-signal/RF
- ASICs exploiting parallelism of 3D-interconnects
- 3D analog continuous-time processor
- 3D-integrated S-band digital beam former
- Stacked memory (SRAM, Flash, and CAM)
- Self-powered CMOS logic (scavenging)
- Integrated 3D Nano-radio and RF tags
- Intelligent 3D-interconnect evaluation circuits
- DC and RF-coupled interconnect devices
- Low Power Multi-gigabit 3D data links
- Noise coupling/cross-talk test structures and circuits
- Thermal 3D test structures and circuits

3DL1 Participants (Industry, Universities, Laboratories)

BAE	Lincoln Laboratory	Purdue
Cornell	Maryland	RPI
Delaware	Minnesota	Stanford
HRL	MIT	Tennessee
Idaho	North Carolina State	UCLA
Johns Hopkins	NRL	Washington
LPS	Pennsylvania	Yale

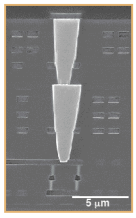
Cross-Section of 3-Tier 3D-integrated Circuit
(DARPA 3DL1 *Multiproject Run*)

3 FDSOI CMOS Transistor Layers, 10-levels of Metal



3D Technology Improvements
(DARPA 3DL1 *Multiproject Run*)

- 3D technology enhancements successfully demonstrated in 3DL1 Run
  - Stacked 3D-vias for electrical and thermal interconnect
  - 2X reduction in 3D-via size
  - Improved tier-to-tier overlay



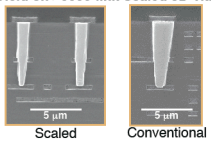
Stack 3D-vias demonstrated

>95% yield on 4800 link chains

Stacked 3D-via resistance ~1Ω

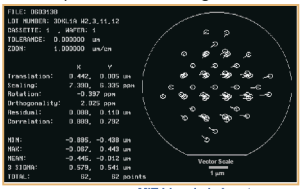
Can be used as thermal vias

High-Yield on >5000-link Scaled 3D-via Chains



Scaled Conventional

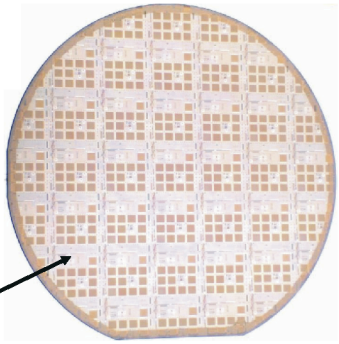
~0.5 µm 3σ Tier-to-Tier Registration



Silicon to InP Wafer Bonding

- Successful demonstration of 3D-bonding of SOI CMOS circuit layer to InP handle wafer
- Enables extension of 3D-integration technology to higher density, longer wavelength focal plane detectors
  - Tight pixel-pitch IR focal planes and APD arrays
  - InGaAsP (1.06-µm), InGaAs (1.55-µm)

Oxide-bonded circuit layer transferred from silicon wafer



150-mm-diameter InP Wafer

Summary

- MIT Lincoln Laboratory-developed 3D circuit integration technology has been applied to advanced focal planes and three-tier computational circuits
- Successful demonstrations:
  - Two-tier visible imager: 1024x1024 array of 8µm x 8µm pixels integrated to 100% fill factor photodiodes, backside illuminated
  - Three-tier ring oscillators in 180-nm gate length technology
  - Three-tier laser radar focal plane: 64x64 array of Geiger-mode avalanche photodiodes with per-pixel timing and bias circuitry
  - Three-tier 3-D IC Multiproject Run in 180-nm gate length technology
  - Two-tier bonding and interconnection to SWIR-sensitive detector materials (InP)

Plenary Session 2

Plenary ILC & high reliability

Detectors for the International Linear Collider

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green@liv.ac.uk

Abstract

Some of the challenges of experimentation at the International Linear Collider (ILC) are discussed and the different detector concepts designed to cope with those challenges presented. These different concepts lead to various alternative technologies for the major ILC detector components, some of which are briefly presented.

I. INTRODUCTION

The International Linear Collider (ILC), an electron positron collider with an initial centre-of-mass energy in the range $\sqrt{s} = 200...500\,\mathrm{GeV}$, upgradeable to 1 TeV, is the ideal complement to the Large Hadron Collider (LHC). The clean environment at the ILC will allow precision studies to be made of any new effects discovered at the LHC, as well as making possible the discovery of new physics up to mass scales well beyond the kinematic limit of the machine. A comprehensive and detailed review of the physics potential of the ILC and how this complements that of the LHC is given in [1]. This potential can only be fully realised if the detectors at the ILC's interaction point[1] (IP) have a precision concomitant with the physics requirements. These requirements, and the detector designs and technologies necessary for their realisation, are discussed briefly in this document.

II. DETECTOR REQUIREMENTS AT THE ILC

The demands placed on the ILC detectors are manifold, but can be illustrated by considering a small number of the physical processes which will be studied at the ILC. The first of these is the requirement that it be possible to precisely measure the decay branching ratios of the Higgs boson. Identifying the quarks to which the Higgs decays, primarily the b and c, requires that each of the ILC detectors be equipped with an extremely precise vertex detector (VXD) The inner radius of the VXD is constrained by the ILC backgrounds to be about 15 mm. Flavour identification of high efficiency is necessary as cross-sections at the ILC are small, and of high purity as backgrounds are not negligible. This demands that about 5 hits be recorded on the charged tracks of the b and c hadron decay products with a precision of better than 5 μm. Furthermore, the momentum distribution of the decay products extends down to below 1 GeV, so the beampipe within the VXD and the VXD itself must present the minimum possible amount of material to the particles traversing them.

A further measurement which the ILC detectors must be able to make is the identification of and the determination of the mass of particles such as the Higgs even when these decay invisibly. For example, if the Higgs is produced through the Higgs-strahlung process, $e^+e^- \to Z^0H$, and the Z^0 then decays to a muon pair, knowing the initial e^+ and e^- momenta allows the determination of the Higgs mass provided the momenta of the muons can be measured with sufficient precision. This leads to the requirement that the transverse momentum resolution of the tracking systems of the ILC detectors be $\delta p_T / p_T^2 = 5\times10^{-5}\,\mathrm{GeV}^{-1}$ or better.

If no Higgs boson is found, there will be particular interest in measuring the reactions $e^+e^- \to W^+W^-\nu\bar{\nu}$ and $e^+e^- \to Z^0Z^0\nu\bar{\nu}$, where the W and Z bosons decay primarily to jets of hadrons. Separating the two processes requires that masses of the bosons be reconstructed from these jets with sufficient precision to discriminate between m_W and m_Z, requiring a jet energy resolution of about $\sigma_{jet} = 0.3/\sqrt{E_{jet}\,(\mathrm{GeV})}$. Note that the presence of the neutrinos prohibits the use of simple kinematic constraints in determining these masses. One means of obtaining such energy resolution is to use "particle flow" techniques, i.e. to combine precise measurements of the momentum of the charged particles in a jet made in the tracking system with measurements of the energy of photons made in the electromagnetic calorimeter (Ecal) and of neutral hadrons in the hadronic calorimeter (Hcal), avoiding the loss or double counting of energy. The limiting factor in the jet energy resolution is then not the resolution of the tracking system or calorimeters but the problems associated with correctly identifying how the charged and neutral particles in a jet contribute to the showers measured in the calorimeters. It thus becomes more important to obtain good spatial resolution in the calorimeters than optimal energy resolution. Alternatively, novel calorimetric techniques can be pursued in order to obtain the necessary jet energy resolution using the calorimeter alone.

A further reaction of interest is fermion pair production, particularly given the polarisation of the ILC e^- beam. The left-right asymmetry, A_{LR}, in $b\bar{b}$ or $c\bar{c}$ production is sensitive to the effects of, for example, extra dimensions, allowing such effects to be observed up to masses well above the kinematic limit of the ILC. Interestingly, the coupling constants are such that the effects on lepton production asymmetries are very small. Measuring A_{LR} for b and c quarks requires not only the determination of the flavour of the quarks but also their charge. This places even more stringent requirements on the VXD. All charged particles must be correctly associated with the secondary and, in the case of b

[1] It is likely that the ILC will have only one IP which will be equipped with two detectors. These will share the beam time in so-called "push-pull" operation.

quarks, tertiary vertices if the quark's charge is to be correctly determined.

III. ILC Detector Concepts

Four concepts are currently under discussion for the ILC detectors, the Giant Linear Collider Detector (GLD) [2], the Large Detector Concept (LDC) [3], the Silicon Detector (SiD) [4] and the Fourth Concept (4th) [5]. A common feature of all these detectors is that their ECal and Hcal are placed inside the solenoid which provides the magnetic field for their central tracking systems, ensuring that the amount of energy lost before calorimetric measurements are made is minimised. The first three concepts rely on particle flow techniques to obtain the required jet energy resolution, necessitating the development of calorimeters with good spatial resolution and the associated particle flow algorithms, while the lattermost requires the development of calorimeters which themselves provide excellent jet energy resolution. The relative sizes of

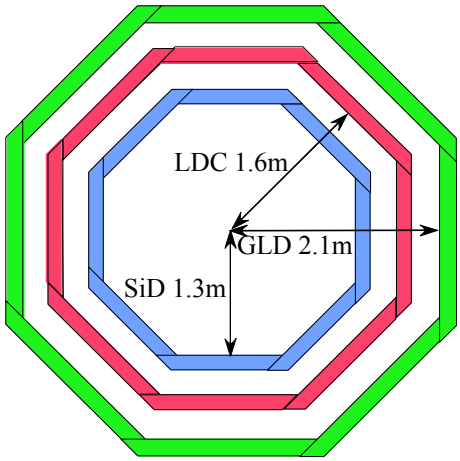

Figure 1 Illustration of relative sizes of GLD, LDC and SiD; shown is the inner radius of the Ecal in each case)

the GLD, LDC and SiD are illustrated in Figure 1, which shows the inner radius of the Ecal of these detectors. The 4th detector is of a similar size to the LDC. All the detectors are of the familiar nested design, the inner vertex detector being surrounded by a tracking system, an Ecal, an Hcal the coil providing the central magnetic field and a muon system, as illustrated in Figure 2 for the LDC detector. The flux return for the magnetic field is provided by an iron yoke in the case of the GLD, LDC and SiD concepts, this iron being instrumented to provide muon detection. In the case of the 4th concept, shown in Figure 3, a second solenoid surrounding the first is used to provide the flux return.

The GLD relies on the large distance particles travel before encountering its calorimeter to separate adjacent energy deposits sufficiently to allow their identification with modest spatial resolution and association with charged tracks where appropriate. The large inner tracking volume also makes possible the use of a relatively small solenoidal magnetic field of 3 T while retaining good momentum resolution. The main elements of the tracking detector are the VXD, a large Time Projection Chamber (TPC) and some supplementary silicon tracking. Surrounding the solenoid is an instrumented iron yoke that provides the flux return for the B field, measures any energy leaking out of the Hcal and measures the paths of penetrating particles such as muons.

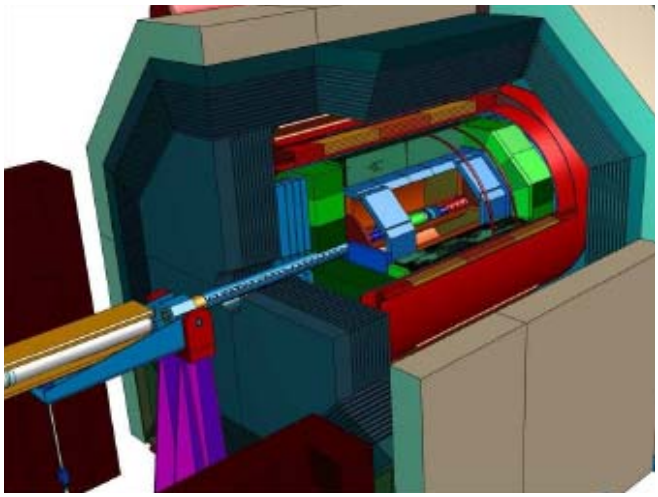

Figure 2 An illustration of the LDC detector.

The LDC is smaller than the GLD, but similar to it in that the tracking volume contains a VXD and a TPC with some supplementary silicon tracking detectors. A stronger magnetic field of 4 T allows the required momentum resolution to be achieved despite the smaller radius of the tracking volume. The smaller size also requires that the spatial resolution of the calorimeters be higher than is necessary for the GLD, but reduces their overall volume. Again, the calorimeters are surrounded by an instrumented iron yoke.

The SiD is the smallest of the detectors being considered for the ILC and utilises a 5 T magnetic field with high precision tracking, provided by a vertex detector and a silicon strip based outer tracking system, to obtain the necessary momentum resolution. Again, high granularity calorimetry is essential for particle flow measurements, and flux return and muon measurements are provided by an instrumented iron yoke.

The 4th detector, shown in Figure 3, represents a departure

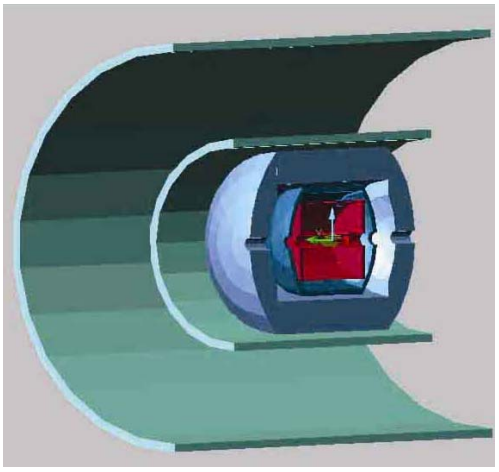

Figure 3 Illustration of the 4th concept, showing the dual solenoid system.

from the above three concepts in several respects. Perhaps most importantly, this detector aims to obtain the required jet energy resolution using high precision calorimetry alone. Further, it utilises two solenoids, the first to provide a magnetic field of about 3.5 T in the central tracking volume, in which the main tracking elements are a VXD and a TPC, possible with some supplementary silicon tracking, and the second to return the flux from the central field in the space outside the Hcal. This obviates the need for an iron yoke, with the associated multiple scattering. The magnetic field in this outer region of about 1.5 T, with direction opposite to that of the field in the inner tracking volume, makes precise muon momentum measurements possible.

IV. Calorimeters for the ILC

Much effort has been invested in research on and development of the calorimeters necessary for precise particle flow measurements. For the relatively small LDC and SiD concepts, extremely good spatial resolution is required, particularly in the Ecal. This means that materials with small Moliere radii must be used and fine granularity readout is essential. The absorber material of choice for the Ecal is thus tungsten, with the readout granularity being matched to the Moliere radius of $R_M \sim 1$ cm. Readout can be provided by silicon pad detectors. The total depth of the calorimeter, which consists of ~ 40 layers, is about 24 X_o or 0.9 λ_0. In order to ensure that the electromagnetic energy deposits remain compact, the thickness of the gaps in the tungsten in which the silicon readout pads are placed must be minimised. There is thus no space for cooling, and readout systems with extremely low power consumption are essential. These are being realised by exploiting the duty cycle of the ILC: bunch trains cross for a period of about 1 ms at the ILC IP and the gap between bunch trains is about 200 ms. A device that effectively exploits this time structure is the Kpix chip [6], which can provide the readout for 1024 calorimeter cells with a power consumption of less than 20 mW. This is achieved by turning off the digital functions of the chip during the bunch train (0.5% of the time) while the analogue signals are amplified and buffered, then turning off the analogue functions during the readout (99.5% of the time). An alternative approach is to use Monolithic Active Pixel sensors (MAPs).

A somewhat lower granularity is required in the Hcal, with current studies suggesting that scintillator tiles of size about 3×3 cm^2 are adequate. These are read out using silicon photomultipliers (SiPMs). Alternatively, "digital" readout could be performed using resistive plate chambers (RPCs) at a granularity of about 1×1 cm^2. This approach records only whether energy above threshold was deposited in the cell, no attempt is made to record the amplitude of the signal.

High spatial resolution electromagnetic and hadronic calorimeters are being studied by the CALICE Collaboration [7]. They have demonstrated that it is possible to track the energy deposited by individual particles in a sufficiently fine-grained calorimeter. Indications are that such calorimeters, and their associated particle flow algorithms, will indeed allow the required jet energy resolution to be achieved, though it is possible that this resolution will fall below $\sigma_{jet} = 0.3/\sqrt{E_{jet}\,(\mathrm{GeV})}$ at the highest jet energies, as the separation between the energy deposits in the calorimeter decreases.

The GLD concept aims to obtain an effective readout granularity of 1×1 cm^2 in its Ecal by using a combination of orthogonal $1 \times 20 \times 0.2$ cm^3 scintillator strips in successive gaps in the absorber material, backed up by scintillator pads of size $4 \times 4 \times 0.2$ cm^3. For all these layers, readout will be via wavelength shifting fibres and SiPMs.

The alternative approach to obtaining the required jet energy resolution being pursued by the 4th concept requires the development of a fine-grained sampling Hcal with multiple fibre readout. Scintillating fibres allow the measurement of all of the charged particles produced in a shower, while the Čerenkov light produced in quartz fibres is sensitive primarily to the highly relativistic electrons in the electromagnetic component of the shower. The binding energy losses in hadronic showers are roughly proportional to the number of neutrons produced and can thus be deduced by detecting these neutrons. This can be done, for example, using fibres doped with lithium or boron. Hence, the three major components that contribute to hadronic showers can be separately measured, allowing precise determination of the total jet energy despite the large fluctuations in the proportions of these components. Dual readout, using quartz and scintillating fibres, has been tested in the DREAM calorimeter [8].

The 4th concept supplements the above Hcal with a crystal Ecal, again with dual quartz and scintillating fibre readout.

V. Tracking Detectors

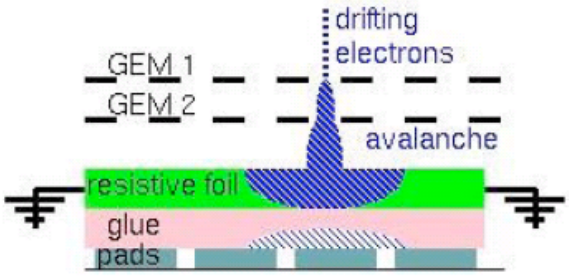

Figure 4 Use of resistive foil to disperse charge across several TPC readout pads following gas amplification using a pair of GEM foils.

As is mentioned above, three of the four detector concepts propose that a large TPC be the main element of their central tracking systems. These have the advantage that they have a large sensitive volume, measure many space points on the paths of charged particles offering excellent pattern recognition capabilities, present only about 3% X_0 to normally incident particles and allow particle identification using dE/dx. However, the momentum resolution required at the ILC exceeds that which has been achieved at e^+e^- detectors using TPCs to date and the TPC end plates represent a significant amount of material, so improvements in the technology are needed. For example, although the baseline design of the LDC concept specifies that the TPC be read out using multi-wire proportional chambers (MWPCs) with pad

sizes of about $2 \times 6\ \mathrm{mm}^2$, similar to the approach that has been successfully used at other e^+e^- detectors, much interesting research is being pursued on alternative readout systems [9]. Some of these utilise micro-patterned gas detectors such as Gas Electron Multiplier (GEM) foils or Micro-mesh Gas (Micromegas) detectors. The limitations on the resolution when such readout is used often result from the width of the pads on which the signal is induced following gas amplification. Resolution can be improved by dispersing the charge across several pads, hence allowing centroid determination, as is illustrated in Figure 4.

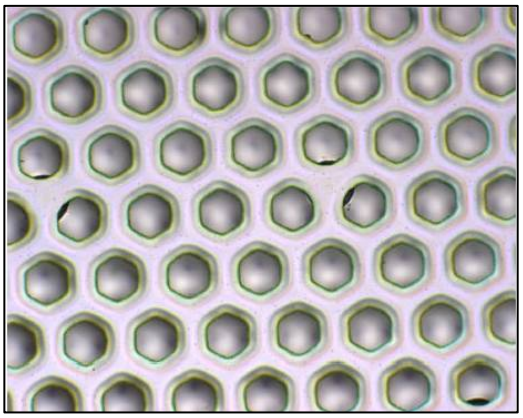

Figure 5 Patterned metal layer used to provide gas gain for TPC readout integrated onto MediPix2 sensor.

An alternative approach to improving the resolution offered by the TPC is to integrate the MPGD on to a pixel sensor by post-processing the sensor wafers. This has been successfully done for MediPix2 sensors [10], which have a pixel size of $55 \times 55\ \mu\mathrm{m}^2$. The patterned metal above the chip, shown in Figure 5, allowed gas gains of up to 10^4 to be achieved in an 80:20 Ar:CO_2 gas mixture. Problems with occasional sparking, which destroyed the readout, may well be overcome by incorporating a few mm thick highly resistive amorphous silicon layer to protect the sensors.

While the GLD, LDC and 4th concepts have chosen to rely on gaseous tracking systems, the SiD requires the increased point precision provided by silicon sensors to obtain a transverse momentum resolution of $\delta p_T / p_T^2 = 5 \times 10^{-5}\ \mathrm{GeV}^{-1}$ or better. Efforts here are largely directed at reducing the material budget of silicon strip detectors to values well below those typical for the LHC. This requires the development of low power electronics, as well as light but rigid support structures. The Kpix chips mentioned above in the context of the calorimeter readout represent one possible approach to low power readout and the SiD concept has invested considerable effort in the design and study of low mass support structures for its tracking sensors. The modules, illustrated in Figure 6, are based on carbon fibre and rohacell, with a 50% void, and present a material budget of only 0.8% X_0 per layer to the particles which traverse them. These modules are mounted on a low mass framework, again using carbon fibre technology.

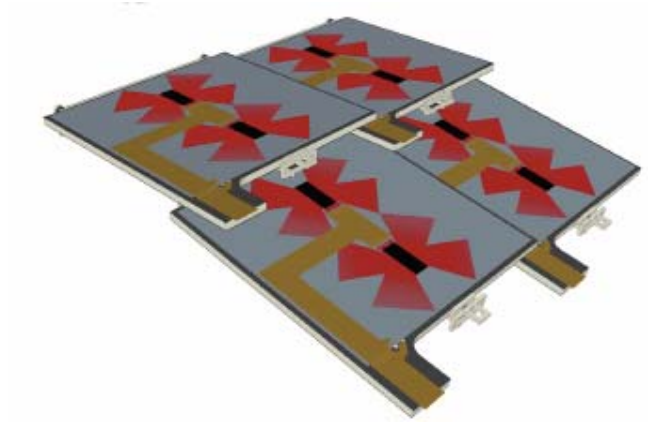

Figure 6 Four modules of the SiD central silicon track detector.

VI. Vertex Detectors

In addition to the physics requirements discussed above, significant constraints are placed on the ILC VXDs by the collider itself. Trains of about 3000 bunches pass through the beampipe within the detector at a frequency of approximately 5 Hz. Within these trains, tightly focused electron and positron bunches collide roughly every 350 nanoseconds generating not only the e^+e^- interactions of interest but also large numbers of electron-positron pairs which cause background hits in the vertex detector. For a detector with pixels of size $20 \times 20\ \mu\mathrm{m}^2$, this implies the signals in the sensors must be read out or stored about 20 times during the bunch train, that is, roughly every 50 μs, to ensure that the occupancy remains below about 1%.

A further challenge at the ILC is illustrated by the experience of the SLD vertex detector, the only vertex detector operated in a linear collider environment to date. This detector suffered from beam-induced pickup, presumably from the leakage of RF power generated by the wake fields of passing electron and positron bunches.

The complications of satisfying both theconstraints placed on the VXD by the machine and satisfying the physics requirements have led to the investigation of many sensor types. Not surprisingly, given the success of the VXD3 vertex detector of the SLD [11], Charge-Coupled Devices (CCDs) are one of these. Two CCD architectures are being studied. The first uses $20 \times 20\ \mu\mathrm{m}^2$ pixels and achieves high readout speeds by getting rid of the serial register found in conventional CCDs and placing readout circuitry at the bottom of every pixel column. Even with the large increase in readout speed this column parallel architecture offers, the image register must be clocked at a rate of 50 MHz if readout is to be achieved in the required time. Such CCDs have been produced and tested, together with column parallel readout chips which have been bump-bonded to the CCDs. These bump-bonded assemblies have been shown to function well, albeit so far only at reduced clock speeds [12]. CCDs for which the required 50 MHz clock rate should be achievable are currently under test with second generation column parallel readout chips, as are chips designed to produce the 20 A drive signals necessary to clock the charge through the CCDs.

The second CCD architecture that is being considered for the ILC avoids the need for high-speed readout by increasing the number of pixels by a factor of about 20 compared to the above design, hence maintaining a similar occupancy, provided the number of pixels under which charge is collected for each traversing track remains similar. These Fine Pixel

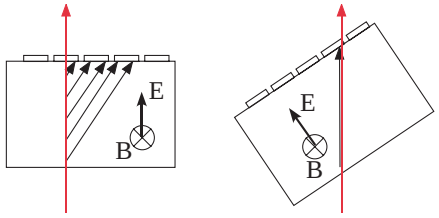

Figure 7 Fine Pixel CCD illustrating the orientation needed to prevent charge spreading due to Lorentz angle effects in detector's B field.

CCDs [13] thus have a pixel size of $5 \times 5\ \mu m^2$, are fully depleted to minimise the spread of charge and so oriented that they compensate for the Lorentz angle at which the electrons drift in the CCD due to the detector's magnetic field, as illustrated in Figure 7.

Several groups are working on the design of CMOS Monolithic Active Pixel Sensors (MAPS) for the ILC VXD. For example, the Strasbourg group has reported resolutions as good as 1.5 μm from its $20 \times 20\ \mu m^2$ pixel MIMOSA9 sensors [14]. The challenge here is to design full length ladders using this technology, while keeping the material budget as small as possible. In addition to sensors with high speed readout, CMOS devices with a set of capacitors in each pixel have been proposed. These would allow conversion of the charge collected in the pixel to a voltage and storage in pixel during the bunch train, with readout following in the

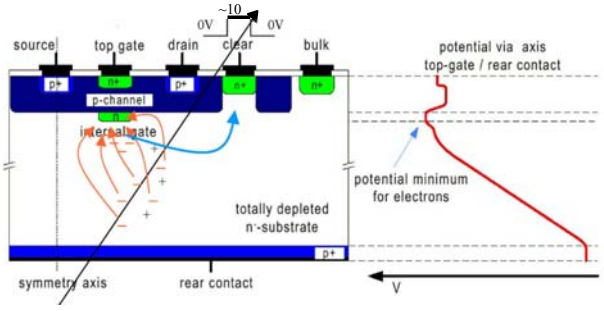

Figure 8 Operation principle of the DEPFET sensor.

inter-bunch train gap at a more relaxed pace. First tests of these devices have been carried out.

A further interesting sensor for the ILC vertex detector is the DEPFET [15], the operating principle of which is illustrated in Figure 8. Progress with designing the electronics necessary to readout and steer this sensor has been good. They promise low noise operation at room temperature and resolutions of 9.5 μm have been obtained from sensors with $20 \times 25\ \mu m^2$ pixels.

A novel sensor which also allows storage of the signals in-pixel during the bunch train and later readout is the In-situ Storage Image Sensor (ISIS). Within each imaging pixel, this device has a small storage CCD. The charge collected in the imaging pixel is stored in this CCD and read out during the inter-train gap, a column parallel readout speed of about 1 MHz being adequate. This device promises to provide very high tolerance to electromagnetic interference effects as the signal charge is trapped in the buried channel of the storage CCD during the bunch train and charge to voltage conversion and readout happen in the relatively quiet period between bunch trains. First "proof-of-principle" devices have been tested and functioned well [12]. The integration of CMOS and CCD features onto one wafer represents the major challenge for the further development of this sensor.

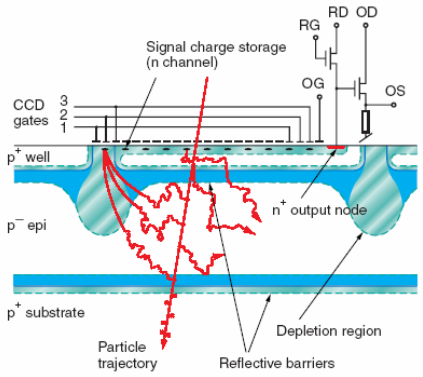

Figure 9 Illustration of the operating principle of the ISIS.

VII. SUMMARY

Physics at the International Linear Collider demands that the ILC detectors provide more precise vertex and track information, as well as better jet energy measurements, than has previously been possible. These demands have spawned interesting developments in calorimetry, tracking, vertex detection and in the interplay between these elements of the ILC detectors. Some of these developments have been briefly described in this report.

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High Availability Electronics Standards

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Abstract

Availability modeling of the proposed International Linear Collider (ILC) predicts unacceptably low uptime with current electronics systems designs. High Availability (HA) analysis is being used as a guideline for all major machine systems including sources, utilities, cryogenics, magnets, power supplies, instrumentation and controls. R&D teams are seeking to achieve total machine high availability with nominal impact on system cost. The focus of this paper is the investigation of commercial standard HA architectures and packaging for Accelerator Controls and Instrumentation. Application of HA design principles to power systems and detector instrumentation are also discussed.

I. INTRODUCTION

The International Linear Collider will be one of the largest and most complex accelerators ever built. The sheer number of single-point failures in multiple systems makes it imperative that a major design emphasis be placed on Availability, the amount of time the machine is operational during planned running time. An accelerator availability modeling program developed for the ILC, *Availism* [1], has shown that the ILC cannot operate with acceptable up-time unless all systems are designed with a very high tolerance to individual unit failures. As a result ILC designers are exploring High Availability (HA) design of the entire accelerator, including major machine systems, utilities, cryogenics, magnets, power supplies, instrumentation and controls.

The main focus of this paper is the development of HA packaging standards for Accelerator Controls and Instrumentation. Current modular standards, some invented by the physics community, achieve improved up-time by rapidly interchangeable plug-in modules. However this requires machine interruption to replace a failed module, which means lost machine productivity. In addition, current modular standards share a parallel bus backplane in which a single-point failure can disable the entire crate and interrupt the beam for hours. *Availism* shows that for ILC, reliability of all key systems must be improved significantly to meet an availability goal of >85%. This is true whether all systems are in a single tunnel and inaccessible during running, or in a parallel service tunnel with all active components accessible for immediate repair. The Baseline model for ILC is a parallel service tunnel. Even so, many sub-components need improved Mean Time Before Failure (MTBF), some by large factors that are impossible without new design strategies. While statistics show that controls and instrumentation of existing machines contribute less downtime than power systems, the sheer size of the ILC demands an effective reliability improvement in all subsystems by at least an order of magnitude.

The chief contributor to machine downtime currently is magnet power supply systems, followed by RF power systems, and then by instrumentation and controls. For instrumentation and controls, the key high availability strategy has been developed years ago in the form of the standard instrument module[3]. The main availability strategy for such systems is very short repair time (Mean Time to Repair, MTTR). In other words, when a module fails, identify the cause and replace it quickly. However this simple operation usually interrupts the machine or experiment to make the repair, leading to a recovery time which can be much longer than the actual replacement. In contrast, the guiding principle for ILC design is to make repairs without interrupting machine operations if at all possible, and to keep the probability of unavoidable interruptions to an absolute minimum.

Fortunately many new tools are now at hand to address these challenges. While the physics community in the past drove the use of modular instrumentation standards that had an impact on industry, it has been dormant for more than a decade in making any significant improvements. Industry, on the other hand, has forged ahead into new territories driven by their own need to build scaleable modular systems that can operate even while isolating faults and making repairs. This has resulted in a powerful new open standard instrumentation system, as well as many improvements in the associated power supply systems, both of vital importance to the ILC[4]. Similar design strategies are being adapted to all controls, instrumentation and power electronics systems in ILC, techniques that will be invaluable to detector systems as well.

II. SPECIAL CHALLENGES OF THE ILC

The question has been raised: Why is High Availability design such an issue for the ILC and not the LHC? There are several responses to the question:

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[2] Work supported by US Department of Energy Contract DE-AC03-76SF00515.

[3] NIM, CAMAC, FASTBUS and VME. See Ref. [2] for a brief historical review.

[4] The Advanced Telecommunications Computer Architecture, announced in June 2004, is being designed by a large industrial consortium to standardize products for the 10B$/year Telecom industry. This is a major advance in standardization for the industry. See Ref [3].

1. Availability is a crucial concern for *all accelerators and detectors*. It is a measure of the efficiency of the machine in performing its designed tasks. A chronically inefficient billion-dollar class machine speaks to poor design and poor execution. This is not acceptable when tools are available to accomplish high performance at little incremental cost.
2. The ILC, unlike a storage ring, is a *repetitive one-shot machine* where every feature has to function perfectly on every shot. An injector for example cannot fail while the experiments continue running on the already stored beams for possibly many hours before beams disappear. This is a routine failure occurrence in storage ring systems that is masked by the stored beam.
3. The ILC is of a scale of linac never before attempted. The complexity of a single linac collider like the SLC at one-tenth the length is well known. It took a very long time to commission and to finally achieve design performance. In this case both electron and positron beam shared the same linac, in principle less likely to fail than two linacs pointing at each other.
4. Not only the complex of positron and electron injectors and their respective damping rings, but critical components such as the quad magnets in the main linac need to be available all the time, or beam emittance will be lost and the beams will fail to collide.
5. A computer program designed to estimate availability has been benchmarked using real data from operating machines. The original availability goal for the NLC and TESLA machines was A=0.85 (85% uptime); however to achieve it required each of 16 machine subsystems to all be available 99% of the time. This has never been achieved before. Present estimates from the *Availism*[5] program indicate that even with factors of improvement in component MTBF's of 20-50 times present performance, it will be very hard to achieve ILC availability above 0.85.

III. BASIC HA DESIGN PRINCIPLES

The fundamental Availability equation is:
A= (MTBF-MTTR)/MTBF →1 when MTBF→∞ or MTTR→0.
The principles of HA design are simply:

1. Maximize MTBF of basic components
2. Minimize MTTR

This is achieved by:

3. Modularizing all system basic components
4. Adding *partial redundancy* into the system in the form of extra modules, N+1 or N+n where n is much smaller than N.
5. Introducing, wherever possible, module *hot-swap* capability.

Consider the example of a power supply in *Figure 1*: Some ILC magnets are critical in that loss of a single power supply will stop the machine. This is approximately true for the linac superconducting quadrupoles. In this case instead of a single power supply with a controller, the unit is modularized into several parts: A shared bulk DC supply [3]

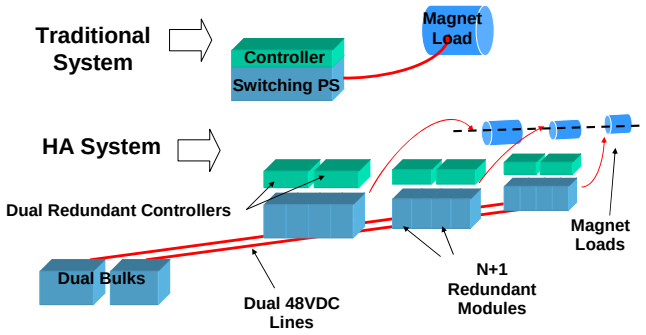

Figure 1: High Availability Power Supply System Concept

feeding several individual supplies and loads; N modular DC-DC converters operating in parallel to supply the total current needed for each load; and separate controllers to manage each supply and the total system. Both the shared bulk supply and each controller are redundant. The entire system is designed to auto-failover: If one of the shared bulk supplies fails, the second unit carries on to support the full load while the diagnostic system notifies the control room of the failure. If a DC-DC converter fails, the system continues as above. If a controller fails, its redundant neighbor takes over. All three of these features are needed to make a power supply system for the ILC that will be available 99% of the time. For repair, it seems feasible to make the N+1 or N+n converter modules as well as the controller hot swappable or perhaps even the bulk for low power supplies. However safety regulations will dictate what can be done in practice. Note that if a unit fails, it is not necessary to replace it instantly (although the quicker it is done the better in case of another failure in the same unit); one can usually wait for a programmed maintenance time to do this. In any case, if hot-swap were permissible, the most common failures could be eliminated as a source of machine interruption and *MTTR for the system can in fact be made zero.*

Note that in linac design, redundancy at a high level is always incorporated in that the machine is longer than needed for its design energy and this extra length represents an allowable number of simultaneous failures of RF stations with minimal operations impact. Although this is also planned for the ILC, it does not help the quadrupole magnet situation, where a failed single magnet could stop the machine.

In controls and instrumentation, similarly, the machine has redundancy of critical elements like steering magnets and beam position monitors. However these must be employed frequently enough all along the machine to allow failures of single units without interruption except for a tuning readjustment, which should be counted as part of MTTR even if it only temporarily knocks the beams out of collision.

The global controls system includes data communications, timing and RF phase references and which must be delivered to every critical instrument and pulsed power device with the same reliability as the AC line power supply. The concept is shown in *Figure 2*. These core

[5] *Availism*, the simulation model by T. Himel of SLAC, quantifies MTBF of all components and estimates availability for various architectural choices such as one vs. two tunnels, redundancy of sources and RF, etc. See US Linear Collider Technology Options Study, USLC Steering Group, March 4, 2004,. Chapter 4: Availability Design, http://www.slac.stanford.edu/xorg/accelops/

functions of controls are planned to be fully redundant with auto-failover hardware and software. Beyond this core which reaches into nodes at every sector of the machine, as shown in *Figure 3*, individual control and monitoring functions can be tailored with HA features in accordance with need. The overall system level of redundancy, such as RF stations, determines the level of need. For example, extra RF stations allow a unit to be taken offline and serviced *while the machine is running,* impacting availability only briefly while the control system switches stations which we assume are in operational standby mode at all times.

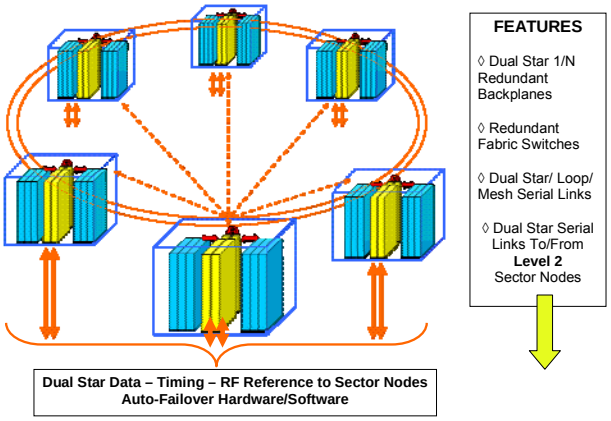

Figure 2: Main Control HA Concept

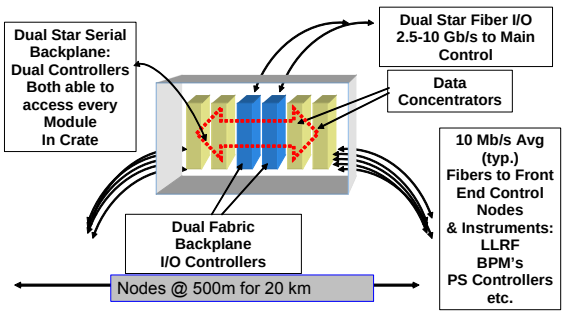

Figure 3: Linac Control Node HA Concept

Underlying all these systems is a new robust Diagnostic Layer that is essential to managing the overall HA system complex. This layer will vary in form between subsystems but its functions remain constant, namely:

1. Provide local intelligence to monitor the health of every subcomponent down to the module level
2. Help protect and isolate faulty modules by disabling local power
3. Monitor internal performance parameters and warn the control room of impending problems
4. Possibly take local action to avoid interlock trips that will interrupt the machine, such as by reducing power out of a local RF unit approaching its limits and compensating elsewhere to keep beam energy constant
5. Flag modules that need attention by hot-swap or programmed repair before multiple failures occur to cause a machine interrupt

Examples will be discussed in the following sections.

IV. HA DESIGN CONSIDERATIONS FOR DETECTORS

To a major extent the large detectors already employ high availability design architectures. The structures are inherently highly redundant in terms of layers of the various chambers, and every layer has multiple individual channels. Even a partially crippled detector that loses a segment can often keep on taking data, although at reduced efficiency. At the same time, a detector that shares a beam as in the Large Hadron Collider (LHC) must be highly reliable as a unit since a serious on-line failure could mean loss of mission for an extended period. Even if immediate repair were possible, access and repair could take weeks or months. The stakes for overall reliability/availability are high indeed. Designs tend to be unique and unproven with respect to long-term performance. It is expected that problems will be fixed with upgrades as necessary. In the execution of the front end electronics, low mass requirements together with design for radiation and magnetic field tolerance severely restrict design choices.

In view of all these risks, HA architectures should be adopted as a design strategy for future upgrades and new projects such as the ILC detectors should be designed for emergency access for critical repairs with minimum intervention and downtime. Some general HA design comments on specific issues are:

A. Front End Electronics

On multi-channel front end boards or hybrids, consider built-in redundant silicon readout structures with availability of spare sections by switches. In principle a faulty electronics channel can be isolated and replaced by program control.

B. Local Controllers

Create redundant control paths where either controller can read out the same segment independently, so in case of failure the control system executes an auto-failover.

C. Communications channels

All high end communications should be Gigabit serial with a standard protocol wherever possible. Critical controls functions will need noise immune error detection and correcting protocols. Fibers and wires including controls and front end data and controls should be redundant with auto-failover software, especially in radiation environments.

D. Front End Board Serial Gigabit Communications

In cases so demanding of real-time response or packaging constraints that a standard protocol cannot be used, provide redundant channels as well as calibration circuitry to monitor degradation of fibers.

E. Access for Repair

Critical electronics on or within a detector should be made accessible from the perimeter. This calls for a new look at segmenting into small, plug-in packages that can be replaced from outside by a human or remote handler mechanism. The challenge is to achieve this design goal with little or no sacrifice of detector hermeticity.

F. Power Systems and Management

More inadequate designs are made on detector power systems than on the much more complex custom chip functions. HA design generally calls for basic redundancy of bulk DC supplies at a high voltage such as 48V, with all loads having local on-board DC-DC hybrid size converters. A single power converter board inside a detector would feed a small group of front end boards or chips and be remotely accessible. Power loss in cables and regulation problems of very high currents at very low voltages would be minimized. A power board for a group of front end boards should be dual-fed with failover capability. Special designs on industry-standard footprints should be designed for radiation and magnetic field tolerance.

G. Module and Board Hot-swap

Major control and power boards should be designed to be hot-swappable. This means no front panel cables or connectors. Such boards would have switches and a power management control system to isolate them automatically from 48V power in case of failure.

H. Crates

All crates should use a modern standard incorporating HA features as seen in the Telecom industry ATCA system (Advanced Telecommunications Computing Architecture). Redundancy, power management and hot-swap features are standard and supported by a growing number of supplier companies. Moreover, crate manufacturers can easily design a custom backplane since many companies will specify special routing of gigabit links and user-defined transition areas.

V. ILC HA ELECTRONICS PROGRAM

Some approximate numbers of devices in the machine are as follows: 10 MW RF stations, 720; RF cavities with RF monitoring and tuning, 18,000; BPMs, 3,000; Magnets and power supplies 17,000; vacuum pumps 10,000; Instrument racks 6,000.

The Electronics R&D program aims to investigate new HA designs for the following: Controls, Beam Instrumentation, Low Level RF, Magnet Power Supplies, Modulators, Diagnostic Interlocks, Stripline Kicker Pulsers. The HA goal for each *complete system* such as controls, power supplies, RF stations etc. is an availability of at least A=0.99. The R&D programs and progress are described briefly.

A. Controls

To achieve A=0.99 Controls requires redundancy of its core communications, controls and processing systems, timing and RF reference systems down to the machine sector node level, and communications to beam instrumentation that is machine-redundant so that a single instrument, such as a BPM, can fail without beam interruption. Core system modules must be hot-swappable to avoid the unacceptably long recovery time of turning off a crate and interrupting the machine. For beamline devices where a single failure will bring down the machine, controls redundancy should be carried to the critical device.

Progress: The ATCA system (*Figure 4*) is chosen as the model for evaluation and cost estimating purposes. This features redundant power sources and shelf (crate) power management, high-density gigabit serial communications and dual communications processors, in a 14-slot crate similar in size to VXI. The management system supports full hot swap and the entire shelf of 14 modules is designed for A=0.99999 (Five 9's). For a system the size of the ILC, 0.99 system availability requires crate level availability of Four 9's. System software studies are in process at Argonne National Lab and hardware-software studies and evaluations have begun at University of Illinois Urbana Champaign (UIUC) supported by SLAC. Part of the hardware study will be how to implement fast analog connector interfaces in the rear panel user-defined space, the gigabit serial connector for analog performance, and overall crate noise performance for analog-to-digital modules. The early deliverable is an ATCA engineering test system made available to labs with development programs, with the longer term goal of a prototype segment of a full system to serve the planned Superconducting Test Facility planned for Fermilab.

B. Beam Instrumentation

The degree of required instrumentation redundancy depends on the device. BPM's do not necessarily have to be redundant if they are placed frequently enough. However since they often share a controls crate with other devices they should be hot-swappable. The goal is to evaluate whether BPM's can be effectively packaged in the ATCA system or one of its standard options.

Progress: A board area comparison with current designs in CAMAC shows this is possible, perhaps including a dual channel per board for redundancy. BPM spacing in the linac is sparse, one BPM of four channels per 36m, so the unit must be a single thin standalone rackmount or a single ATCA board sharing a slot in one of the LLRF crates. Space and connector issues will be studied further by the UIUC group.

C. Low Level RF

The LLRF is the largest subsystem in the main linac, estimated at one ATCA crate for each 10 MW station plus optical transceiver connection areas, tuner driver motors, piezo drivers and a large accompanying cable plant. The LLRF equipment will fill two water-cooled racks per 36m of linac.

Each LLRF unit takes power and phase signals from each of 36 superconducting cavities to control the drive to the klystron and maintain its output power amplitude and phase in stable relationship to the beam. In addition to RF drive the system also manages the cavity tuners which are of two types, a mechanical tuner that is slow and piezoelectric tuners which are fast to dynamically compensate for fast detuning caused by the shock of beam loading.

Progress: Technically the LLRF does not have to be a full HA design because there are redundant RF stations at the system level; however, since every interruption of crate power causes serious recovery time on its own, it is highly desirable that modules be hot swappable. The ATCA is being used as the packaging model for evaluation and cost estimating purposes. Meanwhile actual design of prototypes is proceeding at both DESY and FNAL. Collaborators at KEK, FNAL and DESY are leading the LLRF studies.



Figure 4: ATCA "A=5 Nines" Basic Components

D. *Magnet Power Supplies*

. Quad and corrector magnets in the main linac are superconducting while in the injection systems, damping rings and beam delivery all quads, correctors and bends are normal conducting. For critical loads where loss of the supply would stop operations the goal is hot-swappable redundancy at the bulk, DC-DC converter and control levels. Solutions must be cost-effective. The superconducting magnet supplies are low voltage current sources that require quench protection circuitry.

Progress: An evaluation program of N+1 topology as shown schematically in *Figure 1* is underway for a 5 kW system typical of a warm quad, including 3 of 4 and 4 of 5 modular converters, dual 48V bulks and dual controllers. DC-DC converter failover has been successfully demonstrated by disabling a supply by switching off its reference and studying transient recovery. A dual controller prototype for low voltage power systems is being designed. Demonstration of a complete prototype is planned for FY07. In addition a 40-supply demonstration system has been started for the KEK ATF2 collaboration for delivery in early FY08. Dual redundant bulks will typically be sized to drive several converters, e.g. 10-20 kW units, and hot-swap requires the addition of active isolation circuitry to make the operation safe. Worst case, for safety reasons a failed bulk may be exchanged only during scheduled maintenance. If the second unit fails and interrupts the machine, both units can be changed during a short machine interruption that minimizes MTTR.

E. *Modulators*

Klystron modulators are a major cost component of the machine. The present baseline unit for the ILC is a 10-year old design that has recently been upgraded with redundant IGBT switches. However an alternate design is underway at SLAC of an all solid state Marx generator that minimizes size and eliminates the heavy transformer, producing 120kV at 140A that can run over a short cable directly to the 10MW klystron. This design emphasizes high availability through 4 of 5 redundant IGBT switches for both charging and pulse forming in each of ten 12 kV cells in the stack. In addition it includes 2 extra cells that can be automatically switched in if a cell fails. At the system level, the linacs will have 3% extra RF stations to maintain energy in case of station failure.

Progress: The first prototype Marx 12 kV cell has been successfully tested at SLAC and the full stack is under construction and scheduled for demonstration over the next 2-3 months. See *Figure 5*. If successful, it will become the new baseline for the ILC, and several units will be built for the 10MW klystron driven test programs at SLAC and possibly at other future test facilities. Industrial designs of Marx prototypes are also proceeding.

F. *Diagnostic Interlocks*

Special attention is being paid to developing much better diagnostics than in previous generations of equipment, especially high power modulators and power supply systems. The vision is for a small board-level unit to reside in each cell of a Marx or each module of an N+1 power supply system to monitor operation, including temperature of the environment and critical components, voltage and current levels in relation to equipment safety interlock limits, and critical waveforms to

show variations in performance that indicate impending problems.

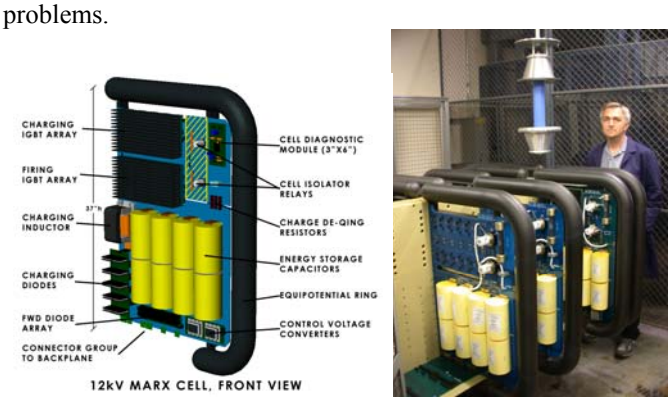

Figure 5: Marx Cell and Prototype Assembly

This information can be used to manage equipment and systems to *avoid* interlock trips, as well as to gracefully remove equipment from service for maintenance before it disrupts operations. The Diagnostic unit could also be taught to take certain actions independently rather than in present systems where every machine trip is a surprise that sends operators and maintenance personnel scurrying for answers.

Progress: A program was started in 2005 in collaboration with Pohang Light Source, Korea, to develop the first prototype of a unit for modulator and large power supply applications. This unit is complete and is undergoing evaluation. Features include fast trigger and trigger time delay management; fast and slow 8 bit and slow 16 bit converters for waveform and DC monitoring respectively; waveform memory for reconstructing trips in post-trigger operation; and serial communications to a control system IO controller via Ethernet. In addition, a special low power unit with reduced feature set has been designed for the Marx. See *Figure 6*. Its low power is necessary to operate from capacitors charged by the high voltage system, as each cell in the stack increases in voltage from ground by 12 kV up to 120kV. This unit has operated successfully on a stacked pair of Marx cells in the first prototype under assembly. See *Figure 6.*

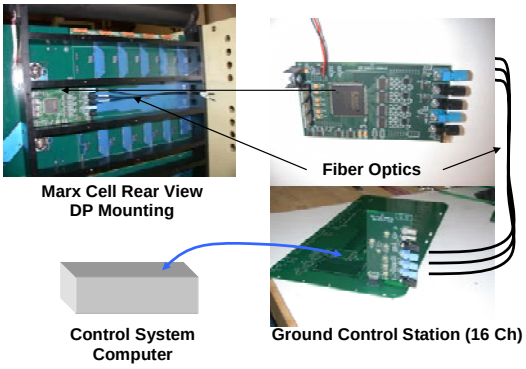

Figure 6: Marx Diagnostic Processor Prototype

G. *Stripline Kicker Pulsers*

A major challenge for damping rings is a 3 MHz kicker pulser producing +/-10kV into 50 Ohms with a baseline of 5 nsec or less and 10^{-4} or less coupling to the next pulse. If the kicker is feasible it reduces the ring from 17km to 6km. The R&D program is to produce a pulse that meets the specifications and engineer the design into a practical kicker unit. The full system will require 10-20 units in tandem to apply the total kick required. In this design as in the Marx, the system engineering aspects are most important: Inclusion of cell-level diagnostics, amplitude calibration and very precise timing control and dynamic calibration capability for the assemblage of 10-20 kickers.

Progress: In 2005 a prototype designed by LLNL in collaboration with SLAC, consisting of 15 MOSFET array driven cells in an induction stack configuration, was tested in the ATF at KEK. See *Figure 7*. The pulse was considerably

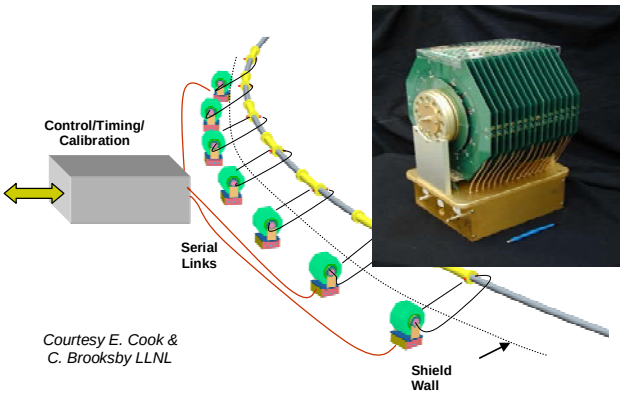

Figure 7: Prototype Damping Ring Kicker & Array

Wider than desired, the voltage was +/-5kV and the unit could only run in short burst mode not CW. Since then the unit was expanded to produce +/-8-9kV, close to the design goal, and in parallel work on new drivers carried out. At the time of writing a new push-pull pulse driver has produced a pulse with a 5.1 nsec base operating in burst mode at 3 MHz. A second prototype breadboard from a SLAC SBIR collaboration has reported a very fast rise and fall time pulse from a DSRD (Delayed Step-Recovery Diode) technique that is being investigated further as a candidate pulser. Other ILC kicker work is occurring at other laboratories as well but not reported here. The SLAC-LLNL goal is a full power and pulse rate prototype in FY07 and demonstration of tandem operation at the ATF in FY08.

VI. SUMMARY AND FUTURE PLANS

High Availability electronics design techniques are becoming standard practice in industries such as Telecom and Computing. HA design techniques can be applied to any system, not just electronics. Both Accelerator and Detector systems can both benefit if HA design is undertaken at inception or for later upgrades. This cost of N+1 redundancy is generally small and overall cost effective due to enhanced availability of the production machines and lower maintenance costs. HA design has been installed as an important performance metric for the ILC.

The ILC R&D Collaboration is investigating a range of approaches to achieving high total machine availability with nominal impact on system cost. Short term goals are to evaluate multi-gigabit serial interconnect systems for intelligent modules, demonstrate basic high availability

software failover management, and port representative core controls, serial networks and beam instrumentation designs onto new platforms. Evaluations are currently focused on the Advanced Telecommunications Computing Architecture (ATCA) system, a new industrial open standard designed for a data throughput of 2 Tb/s and A= 0.99999. Applications of HA to detector architectures is also a future goal.

VII. ACKNOWLEDGMENTS

The SLAC R&D electronics program is collaboration with the international ILC Global Design Effort (GDE) and specifically its Area and Technical groups which can be viewed at *linearcollider.org*. The current program relies on ongoing discussions and joint planning with the Global Controls, LLRF and Availability Technical Groups; as well as on working collaborations with LLNL, ANL, FNAL, KEK, DESY, UIUC, Pohang PLS and R.W. Downing Inc. The special contributions of E. Cook and C. Brooksby of LLNL, J. Carwardine of ANL, B. Chase and M. Votava, of FNAL, R. W. Downing, M. Haney of UIUC, S. Michizono and T. Naito of KEK, S. Simrock and K. Rehlich of DESY, S. Nam of PLS, and the many dedicated colleagues at SLAC and all the named institutions are gratefully acknowledged.

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Plenary Session 3
Optoelectronics

Optoelectronic Developments For Remote-Handled Maintenance Tasks in ITER

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Abstract

Remotely handled maintenance tools operated in the future International Thermonuclear Experimental Reactor (ITER) will face a harsh radiation environment, with total dose level requirements of several MGy. Optical fiber data communication has been considered as an alternative to conventional electronic transmission between the control room and remote handled maintenance equipment, mainly owing to its insentivity to electro-magnetic interference and to its wavelength encoded multiplexing capabilities. In this paper we summarise main results obtained at SCK•CEN over the past years towards the development of radiation tolerant fibre-optic communication links and report on the radiation tolerance of various individual optical components such as optical fibres, laser diodes and photodetectors, as well as their associated electronic driver circuits.

I. ITER Background

The main goal of ITER, i.e. 'the way' in Latin, is to demonstrate the feasibility of a fusion power plant to generate electrical power. It is a tokamak, in which strong magnetic fields confine a torus-shaped plasma of about 500 MW fusion power (cf. Figure 1).

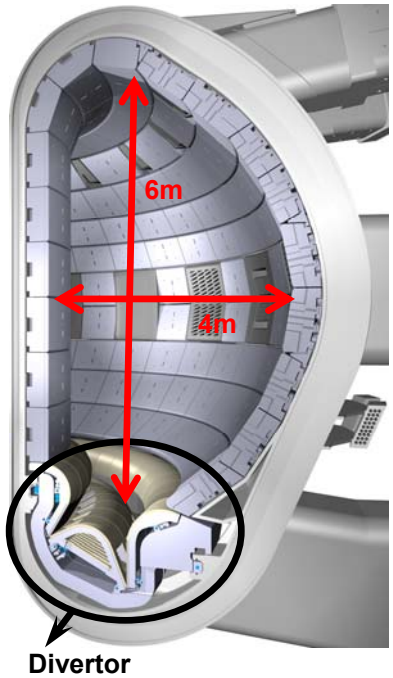


Figure 1 : Cross-section of a D-shaped torus in which a plasma will be generated and heated, hence creating conditions for fusion reactions to occur. The modular divertor elements sit at the bottom.

In-vessel first wall components in the future ITER reactor will be subject to plasma-wall interactions causing activation and erosion. This calls for regular refurbishment, depending on the erosion rate. Furthermore components may need to be replaced due to unexpected failure. Therefore common and dedicated remote handling (RH) equipment for repair and maintenance tasks are needed, which will have to withstand harsh radiation environments [1]. . Besides the very high total dose levels, ITER brings along large masses to be manipulated in a complex geometry of movement with stringent positioning accuracies. Such systems are not readily available from other fields such as underwater, space, or nuclear fission applications.

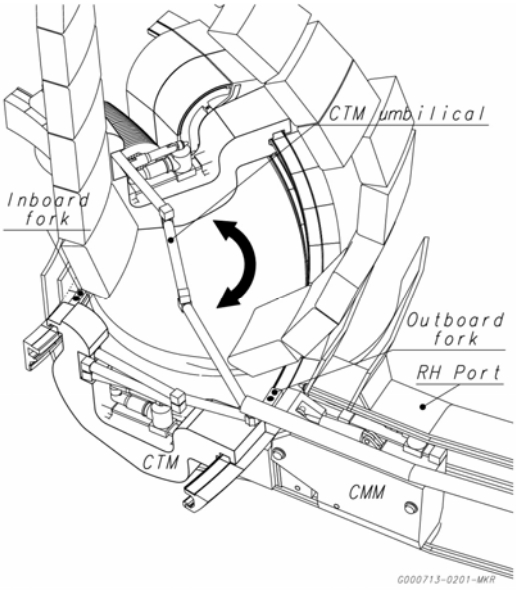


Figure 2 : The ITER in-vessel cassette handling scheme. (Note. CTM shown at both entry and deployed positions).

From the earliest research and design efforts among the different international ITER partners, the European home team has generously contributed to the development of the divertor system and its maintenance scenarios [3]. The most important function of the divertor system is to exhaust the major part of impurities and other particles from the plasma [4]. As the main interface component under normal operation between the plasma and material surfaces, it must tolerate high heat loads while at the same time providing neutron shielding for the vacuum vessel and magnet coils in the vicinity of the divertor. The replacement of the divertor and its refurbishment in a hot cell are foreseen a few times during the ITER lifetime. To meet this requirement, a cassette-type divertor has been selected, which will be replaced and transported with the help of different tools, such as the

Cassette Multifunctional Mover (CMM) and the Cassette Toroidal Mover (CTM), as illustrated in Figure **2**. Conservative estimations of the activation levels made during the final design show that the RH equipment will be exposed to ionizing dose levels of 1-10 MGy and temperatures up to 200 °C [5].

Connecting remotely operated actuators and sensors with the control room conventionally requires bulky and shielded umbilicals. Their size could be reduced by applying radiation tolerant communication links with multiplexing capabilities. Fibre-optic technology is considered as a potential EMI-free solution, since individual components such as optical fibres and couplers, light emitters and photo detectors have thus far shown promising results up to MGy dose levels [6],[7],[8]. The long-term reliability of optical fibres and cables also depends on the evolution of their mechanical properties, information about which only little is known from literature at MGy dose levels. Furthermore, the driving electronics necessary for controlling either the semiconductor light-emitting or light-receiving devices up to these high total dose levels is not commercially available. Over the past several years we therefore focussed our efforts on assessing the optical and mechanical radiation tolerance of optical fibres, on studying radiation effects on different state-of-the-art laser diodes, and on designing and developing dedicated electronic drivers. This paper is hence structured as follows. After dealing with a number of experimental details in the next section, we highlight our recent results on optical fibres, on opto-electronic transmitters, as well as our irradiation experiments with photodiodes, and finally summarize our latest results on driving electronics, from discrete components to ASICs.

II. Experimental details

All irradiations are performed in the facilities of the Belgian Nuclear Research Centre SCK·CEN. Different gamma irradiation facilities are operated using mainly sealed ^{60}Co sources. They offer a wide gamma dose rate ranging from 0.1 Gy/h up to 80 kGy/h, environmental control (e.g. heating up to 200 °C) and on-line instrumentation [9]. Neutron irradiations of remote-handling components are performed in the BR1 reactor, which is a gas-cooled and graphite moderated reactor, fuelled with natural Uranium [10].

The radiation assessment of single mode optical fibres was achieved with in-situ radiation-induced attenuation measurements in the range of 1.2 µm – 1.7 µm, with the help of a tuneable laser source and a photodetector. The mechanical properties were measured before and after irradiation with both tensile tests and strength measurements, at two different facilities for comparison, i.e. at the Draka Comteq facilities in Eindhoven (The Netherlands), and at the University of Birmingham (UK). The dynamic stress corrosion susceptibility of the samples was determined by the two-point bending method, according to the IEC 60793-1-33 standard (method B). This method is used to determine the strength (50% failure stress σ_f) and the dynamic fatigue factor (stress corrosion parameter, n_d), particularly for high strength optical fibres.

InGaAs photodiodes were also characterized in-situ, before, during and after irradiation. We measured the dark current, as well as their wavelength dependent photocurrent between 0.98 µm and 1.65 µm.

More recently, long-wavelength VCSELs, emitting in the 1.4 µm – 1.7 µm range were also evaluated. We recorded before and after irradiation the output optical power and the forward voltage as a function of both the injected current and temperature between 20 °C and 50 °C, using a laser diode controller from ILX Lightwave (model ILX LPA-9080) and an optical integrating sphere for measurements (model ILX OMH-6745B). During irradiation, the devices were unbiased, which left them in worst case test conditions, since current annealing is not allowed.

Finally, various Si-based transistors, including Si and SiGe bipolar transistors, as well as CMOS transistors were assessed up to MGy dose levels with in-situ measurements of their output characteristics and other main parameters.

The main results obtained with this list of passive and active photonic components and their associated driving electronics is presented in the following 3 chapters.

III. Passive fibre optical components

The main long-term effects induced by ionizing radiation on passive fibre optical components are wavelength dependent optical losses and a mechanical degradation of their protective packaging (polymer coating) materials.

A. Radiation induced attenuation in optical fibres

The typical radiation induced attenuation (RIA) in optical fibres measured in-situ in different commercially available multimode fibres is illustrated in Figure 3. It is well known that the RIA, commonly expressed in dB/km, depends on many environmental parameters such as total dose, dose rate and temperature, …, but also on various fabrication parameters including the glass composition and coating materials as well as the fibre drawing speed and tension.

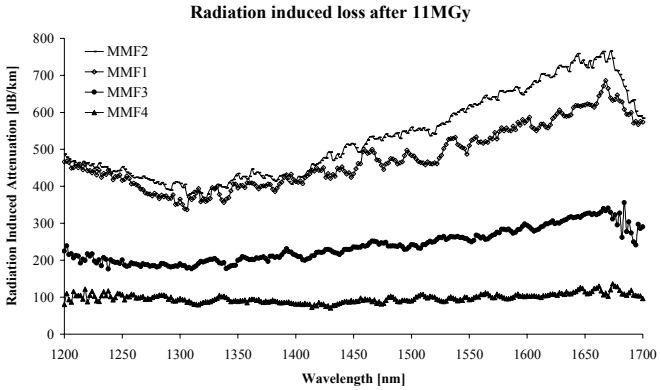


Figure 3 : radiation induced optical losses as a function of wavelength, measured in-situ in 4 different commercially available multimode fibres after a cumulated dose of 10.7 MGy

While these gradient index fibres were exposed at a dose rate of 15 kGy/h up to a cumulated dose of 10.7 MGy at a controlled temperature of 60 °C, their RIA can vary between 0.1 dB/m and 0.8 dB/m. We also observe that at these total

dose levels, the operating wavelength is best chosen in the 1.3 µm region, except for the least sensitive fibre MMF 4, which presents a RIA that is almost wavelength independent.

B. Mechanical degradation of optical fibres

In addition to the numerous assessments presented in literature of the radiation-induced optical property changes in optical fibres, we investigated the impact of MGy dose levels on the mechanical properties of different single and multimode fibres . We compared the tensile test and two-point bending test results with commercially available optical fibres before and after irradiation up to 15 MGy [14].

Figure 4 presents tensile tests results obtained with a standard single mode fibre exposed to different total dose levels and which are compared with an identical sample that was only thermally aged. The 95 % confidence limit (vertical bars) was calculated using a t-distribution. It is clearly seen, in comparison with the thermally aged samples, that the average strength drops with increasing radiation dose beyond 1 MGy. Our results show a significant strength reduction of about 50 % at higher dose levels, relevant for particular applications in nuclear power facilities and in future large nuclear physics experiments. The width of the distribution in the confidence limit also increases. Moreover, the Weibull distribution (not shown here) indicates that the increase of the dose causes the creation of a second failure mode, which is responsible for the decrease in strength and the increase in the standard deviation. This radiation effect can be related to the nucleation of flaws on the surface of the fibre if the fibre is flawless and/or the growth of the flaws size. It can also explain the radiation-induced presence of the second failure mode in the Weibull distribution.

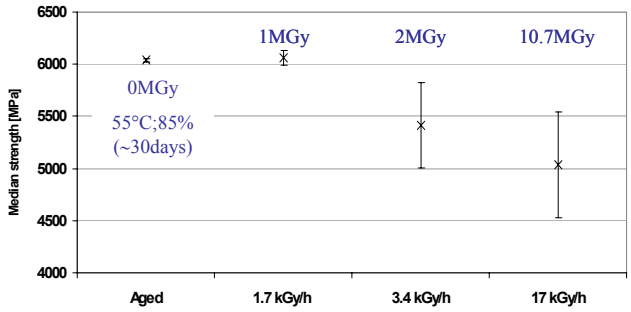
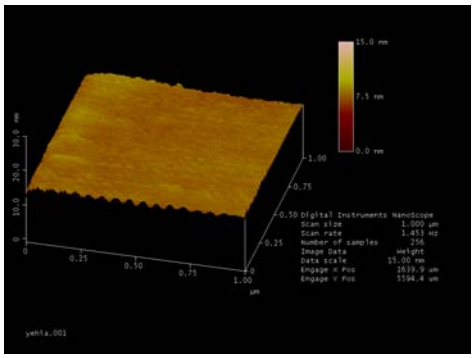
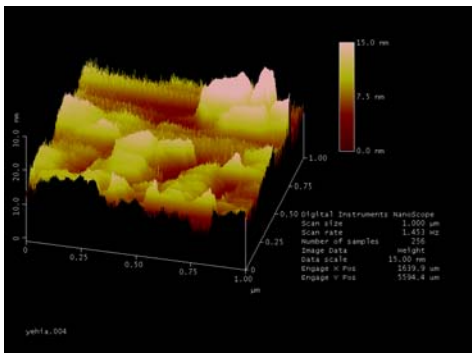


Figure 4: The average strength of four differently treated samples of a single mode fibre. Also shown is the 95 % confidence limit calculated using the t-distribution. (Measurements performed at Univ. of Birmingham.) [14].

In order to better understand the cause of degradation under radiation, the fibre was stripped from its coating using hot sulphuric acid. The mechanical strength reduction observed seems to depend on both the coating materials and the test conditions, as suggested by the roughening of the outer glass surface of the optical fibre, observed with atomic force microscope (AFM) images and illustrated in Figure **5**. The mean square roughness (a) before irradiation was 0.537 nm and (b) increased drastically to 3.314 nm after the combined thermal-radiation treatment. The surface roughness can act as cracks or flaws at the surface and hence explain the observed weakening.



(a)



(b)

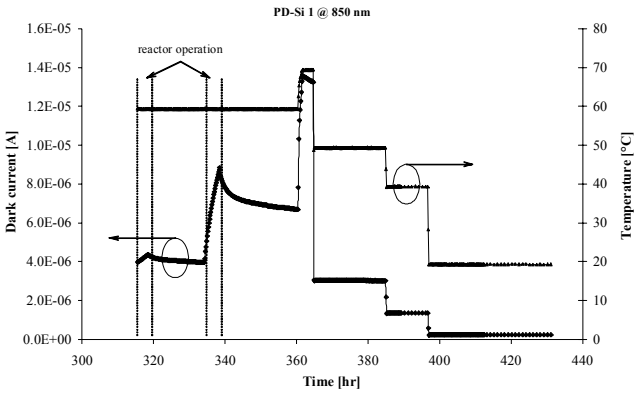
Figure 5 : AFM pictures of the glass surface of a single mode fibre (a) before and (b) after irradiation up to 15 MGy. The increase in surface roughness is the cause in the lower strength of the fibre.

IV. Active Photonic Components

A. P-i-n type Photodetectors

COTS photodiode assemblies were evaluated under radiation for their use in bidirectional fibre optic links [8]. Si and InGaAs PDs were assessed up to 10 MGy, and the Si PDs were also exposed to a thermal neutron fluence of about 10^{15}n/cm^2, as illustrated in Figure 6.

Figure 7 presents the radiation-induced increase of the dark current measured at a reverse bias of -5 V for InGaAs photodiodes. During irradiation we observe a substantial monotonous increase of the dark currents, as compared to the more limited growth observed for the Si photodiodes. At a cumulated dose of 10 MGy, the dark currents have grown by a factor 500 to 700, while the growth does not show any sign of saturation as opposed to the Si-PD's. When the irradiation is halted, the dark currents decrease promptly by about 10-20% (1-1,5 µA at -5 V), which can be interpreted as a radiation-induced current in the PD [8]. After almost 4 days of recovery at 60 °C, the dark currents are monitored at different temperatures between 40 °C and 70 °C. When the temperature is again raised to 60 °C, we observe a limited reduction of the radiation induced dark currents by about 5-10%. These iso-thermal measurements can be used to verify the long term reliability (wear-out) of the photodiodes under radiation. The authors in [17] demonstrate that for gamma doses of 100 kGy, this radiation damage does not affect the wear-out rate of the devices and hence that it has no impact on their long term reliability.



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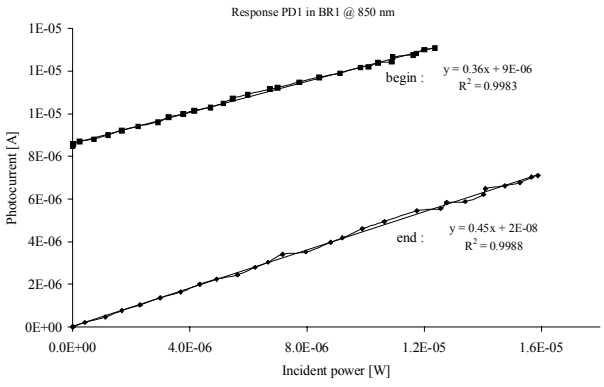


(b)

Figure 6 : (a) Evolution in time of the dark current in a Si PD at the end of the experiment in the BR1 reactor and during the subsequent isothermal recovery test. (b) Response of a Si-PD before and after the exposure to a thermal neutron fluence of $7 \cdot 10^{15} n/cm^2$ and a background gamma dose of 20 kGy. Note : these PD's were first gamma irradiated up to a cumulated dose of 2 MGy.

We also monitored in-situ the wavelength dependence of the photodiode response, in order to verify whether wavelength multiplexing possibilities were still within reach. We observe no catastrophic failure for any of the InGaAs devices nor for the Si devices at these total doses, and their response remains linear. Our in-situ measurements also show that ionizing radiation damage has no significant influence on the wavelength dependence of the photodiode response in the region of interest, which should allow the use of coarse wavelength division multiplexing (CWDM) architectures under high gamma doses.

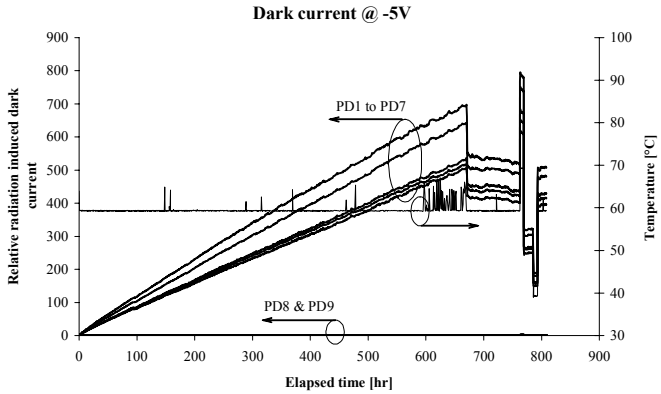


Figure 7: Relative increase of the dark currents measured as a function of time for 7 InGaAs-PD's at a reverse bias of -5 V, a gamma dose rate ~ 15 kGy/h, temperature 60 °C. PD 8 and PD 9 were used as reference, outside the irradiation container.

In conclusion, both dark current increase and responsivity decrease characterize the photodiodes main degradation mechanism, with the former effect dominating. Moreover, the damage resulting from displacement effects caused by neutrons is much more significant in comparison with the damage observed under gamma radiation as observed by many other authors (e.g. [18],[19]). In the absence of neutrons, which are only considered for ITER maintenance tasks if the maintenance equipment has to be stored inside the bio-shield during plasma burns, one should prefer the use of Si photodiodes rather than InGaAs devices to build communication links that can withstand total doses up to 10 MGy, since their dark current increase is much more limited.

B. Surface-emitting Laser diodes

1) Multimode VCSELs

We first reported on high total dose gamma and neutron irradiations of 850 nm vertical-cavity surface-emitting laser (VCSEL) assemblies at a constant temperature of 60 °C [20]. The devices confirm their excellent tolerance to gamma radiation up to a total dose of 20 MGy, obtained in 2 steps of 10 MGy. The optical power loss at nominal forward current is below 2 dB, the threshold current remains unaltered and no influence on the I-V characteristics can be seen. Applying a continuous forward bias to the VCSELs seems beneficial in terms of a lower optical power loss. There is no sign of recovery in the 24 hours following both 10 MGy irradiation stages. The results stress the importance of conducting in-situ experiments, of controlling the bias of the VCSELs in between measurement cycles and they also emphasize the need to take specific care for the design of the VCSEL assembly.

A neutron irradiation was then conducted up to a total fluence on the order of 10^{15} $n \cdot cm^{-2}$, at a constant ambient temperature of 60 °C. The devices here were new unlensed VCSEL assemblies as well as those previously exposed to the 20 MGy gamma dose. As illustrated in Figure 8, the devices experience a dramatic increase of the threshold current which rapidly exceeds the nominal operating forward current. This results in an almost 100 % optical power loss at I_f = 15 mA for fluence levels of a few 10^{15} $n \cdot cm^{-2}$. VCSELs previously exposed to gamma rays exhibit an accelerated degradation under neutron radiation compared to not pre-irradiated devices (not shown here). This conclusion should be taken with specific care as the pre-irradiated VCSELs were obtained from another manufacturer, but it indicates that care should be taken when interpreting results for mixed ionizing-particle radiation environments. The beneficial effect of applying a continuous forward bias to the VCSELs during the irradiation is also evidenced. In contrast to the gamma radiation, the (I,V)-curves are now also affected by the neutrons. Again, the behavior of the (I-V) characteristics is different for the pre-irradiated and the unirradiated devices.

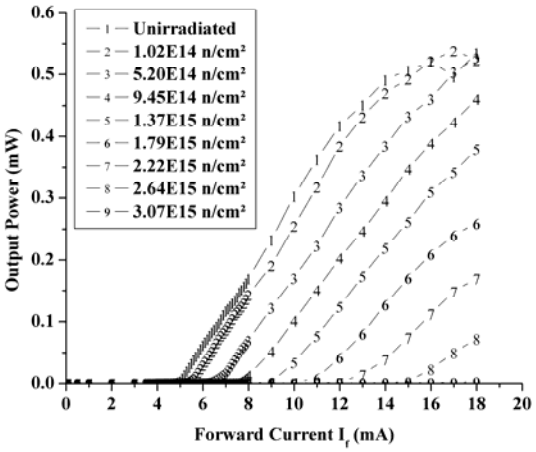


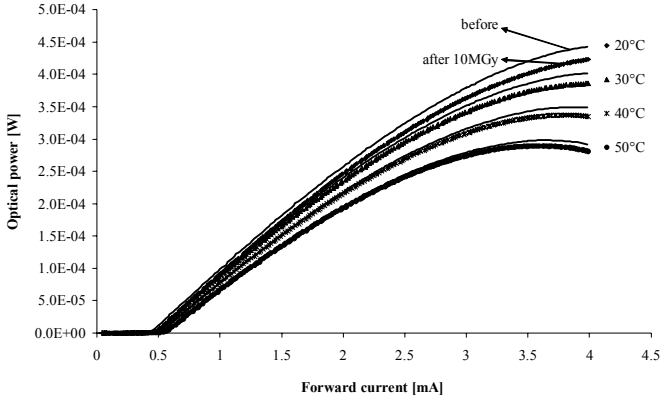
Figure 8: P-I curves of a 850 nm VCSEL assembly at different neutron fluence levels and 60.0 °C ± 1.5 °C.

Since the VCSEL assemblies still operate in a satisfactory way at this 20 MGy gamma dose and at a 10^{14} n•cm^{-2} neutron fluence level, we believe that they are excellent optical emitter candidates for fiber-optic communication links in ITER.

2) Long-wavelength VCSELs

As an alternative to multimode links, one also needs to assess the radiation behaviour of state-of-the-art single mode VCSELs that became recently available, since they would allow a more straightforward optical MUX architecture with largely deployed fibre optic components.

We preformed a first gamma radiation assessment of long-wavelength VCSELs emitting in the 1,4-1,7 µm region, up to 10.1 MGy [22]. The results obtained for a 1.52 µm VCSEL are shown in Figure 9. We observe only a very limited damage, which is somewhat more pronounced at lower temperatures, which suggests a thermally activated recovery. The ionizing radiation induces an increase of the threshold current and a reduced output efficiency. Their temperature dependence is shown in Figure 9 (b). The difference in temperature dependence of both the current gain in the active region and the cavity resonance explains the intrinsic non-linear relation of the threshold current and the output efficiency with temperature. At 25 °C, the threshold increases by 9 %, while the efficiency drops about 6 %. This radiation damage is generally attributed to non-radiative recombination centres, which are created in the active region through displacement damage, requiring an increased forward current before the device starts to lase, but with no significant effect on the slope efficiency. However, the temperature dependence in Figure 9 (b) suggests that there are two competing radiation-induced mechanism, since the threshold changes become less significant at higher temperatures, contrary to the slope efficiency which further decreases as the temperature is raised to 50 °C. This was confirmed by analysing the (I,V)-curves in more detail in [22].



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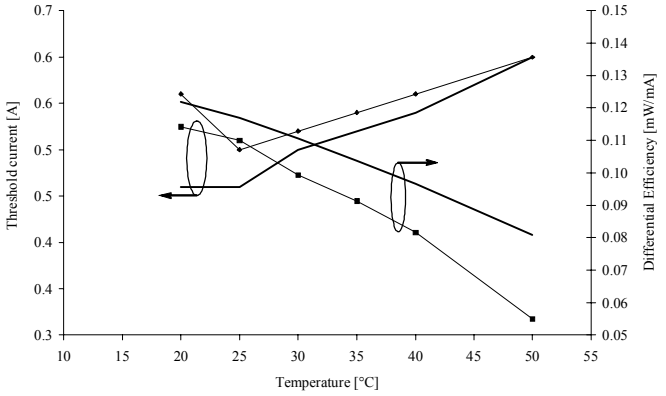


(b)

Figure 9: (a) The (L,I)-curves measured between 20°C and 50°C before (solid lines) and after irradiation up to 10 MGy (dotted lines) for a TO-46 canned VCSEL operating at 1,52 µm. and (b) the threshold increase (left axis) and decrease of output efficiency (right axis) as a function of temperature before (solid lines) and after irradiation (dotted lines).

V. RADIATION TOLERANT DRIVING ELECTRONICS

Robust fibre optic transmission systems up to MGy dose levels require the development of associated electronic circuits, such as laser drivers and amplifiers for the photodiodes. Our first designs were assembled and assessed using discrete bipolar transistors. Later on, this allowed us to migrate towards ASICS.

A. Discrete commercially available transistors

1) Si bipolar transistors

We first developed a VCSEL driver based on discrete Si bipolar transistors (cf. [15] and references therein). The design was based on an adapted SPICE model of the COTS transistor, that described the radiation induced damage as a supplementary time-dependent base current and hence a reduced current gain, and a time-dependent diminishing collector-emitter saturation voltage. This driver consisted of a consists of a current source and a differential amplifier. The driver uses standard TTL input signals and delivers a forward current of 12 mA to a pigtailed 840 nm VCSEL. SPICE simulations show that the driver still delivers a sufficient forward current to the VCSEL, in spite of the radiation induced degradation of the hfe and VCEsat values of the

transistors. These simulations were verified by our experiments. At a total dose of 1 MGy, the measured decrease of the forward current was only about 8 %. During this experiment, we transmitted digitized and serialized data from position sensors with both this optical transmitter and with an LVDS (Low-Voltage Differential Signaling) transmitter. It allowed us to compare the performance of both transmission schemes up to 4.5 MGy [23].

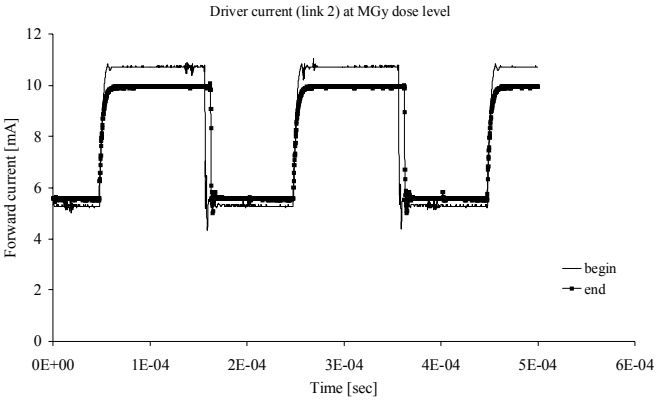
In an attempt to build a robust bi-directional multimode link with these VCSELs, we also assessed a fibre optic transmitter, consisting of a pulse-width modulator (PWM), a rad-hard current driver (cf. also further) and a VCSEL [16]. These assemblies were irradiated up to 10 MGy at 60 °C. As illustrated in Figure 10, our in-situ measurements with carrier signals at 5 kHz and 30 kHz show that this link is a suitable option for the transmission of slowly varying sensor signals (e.g. temperature, position, ...) in a harsh environment, with optical multiplexing possibilities.

The degradation of the driver current source is illustrated in Figure 10 (a). These data were acquired with a trigger signal of 5 kHz and an input voltage of 4.2 V. We observe a small increase of the duty cycle, which can be attributed to the behaviour of the PWM. Furthermore, the high and low output current levels have each evolved by a few percent [16]. The higher level has dropped monotonously by about 8 % after 10 MGy, whereas the lower level has grown with 4 %. The former is attributed to a degradation of the current source, whereas the latter could be explained with a leakage current increase in the output stage of the driver. Nevertheless, this driver circuit hardened by design still functions properly and is yet able to forward a current that will turn the optical emitter on or off. The post-irradiation measurements show also a limited recovery of about 2 % in 3 days.

The degradation of the VCSEL output is presented in Figure 10 (b). We observe a total loss of 60-80 % (4-7 dB) for 3 DUTs, which shows a dispersion common to COTS devices, and confirms our earlier results [21]. The overall radiation induced loss stems from the individual contributions measured separately and during previous experiments, which can be attributed in part to the driver current source and its amplifying stage, as well as to the optical power losses in the pigtailed laser diode. Hence, we do not observe additional radiation damage due to the system integration.

2) SiGe heterojunction bipolare transistors (HBT)

Unfortunately these Si BJT's are currently no longer available. A viable alternative was sought in a VCSEL driver based on bandgap-engineered SiGe Heterojunction Bipolar Transistors (HBT's) [24], for which we first adapted a SPICE model to include radiation damage [25], and which was recently extended with a more physically based description [26]. The model is based on the presumably dominant physical degradation mechanism, obtained from early experiments which showed that the reduction in current gain owes to an increase in Shockley-Read-Hall recombination in the base-emitter space charge region. This is due to the production of G/R-centers caused by radiation induced lattice defects. As a consequence, the base current of the transistor is increased. This presumption is supported by the fact that the excess base current during irradiation has been shown to be inversely proportional to the square root of the collector current. This insight was used to reduce the model complexity to only five coefficients. The resulting model has a very broad range of validity covering the entire design-space of interest.



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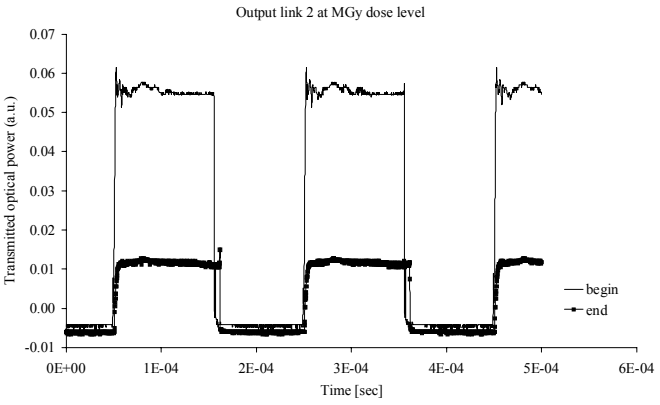

(b)

Figure 10: (a) Comparison of the pre- and post-irradiation output signals of the current driver circuit, at 60°C. (b) Comparison of the pre- and post-irradiation output signals of the optical emitter (VCSEL).

A digital VCSEL driver was then realized using these discrete SiGe HBT's (cf. Figure 11). Simulations, based on the SPICE model developed in [26], were used to design the circuit and predict its behavior under radiation. Note that by adding a diode (D_1) in the divider chain largely reduces this temperature dependence. Simulations predicted a current increase of only 2 % when temperature is raised from 20 °C to 90 °C; a reduction by a factor 10 compared to pure resistive biasing.

The driver tolerates high levels of gamma radiation, up to a total dose of 12 MGy, and features less than 2 % drift in the forward current of the VCSEL. The output duty cycle measured in-situ showed about 1 % decrease at 200 kHz.

Off-line measurements were performed to describe and explain the circuit's operation at elevated temperatures. Before irradiation, the output current of the driver (12 mA at 25 °C) increases less than 1 % up to a temperature of 85 °C which fits well with our simulations. After irradiation, the temperature tests revealed a recovery effect which is linked to the recovery of the individual transistors' current gain. Finally, measurements at an operation frequency of 10 MHz have demonstrated the usefulness of the SiGe transistor and particularly of this design for low frequency optical

communication in extremely harsh radiation environments, up to 10 MGy.

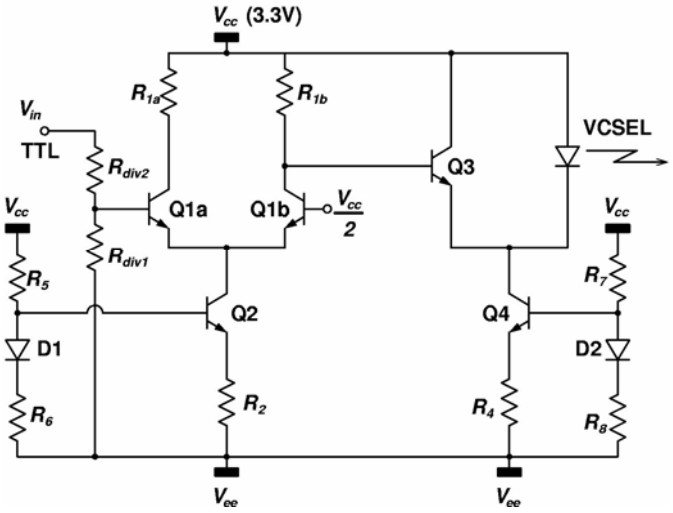

Figure 11: Schematic diagram of the proposed SiGe HBT-based circuit-hardened digital VCSEL driver.

B. Towards radiation tolerant IC's

As a first step towards further miniaturization, we designed a TTL compatible CMOS VCSEL driver as a fully integrated alternative to the discrete SiGe VCSEL driver presented in the previous section. The circuit can operate at least up to a frequency of 155 Mbps and is hence suited for the SONET OC-3 standard. This circuit was implemented in a mainstream 0.7 µm CMOS technology. The design of the circuit tackles the damaging radiation effects both at circuit and layout level. For the layout a dedicated component library was built. The circuit features a replica based current correcting feedback mechanism (cf. Figure 12) for compensation of radiation induced shifts in the device characteristics [27].

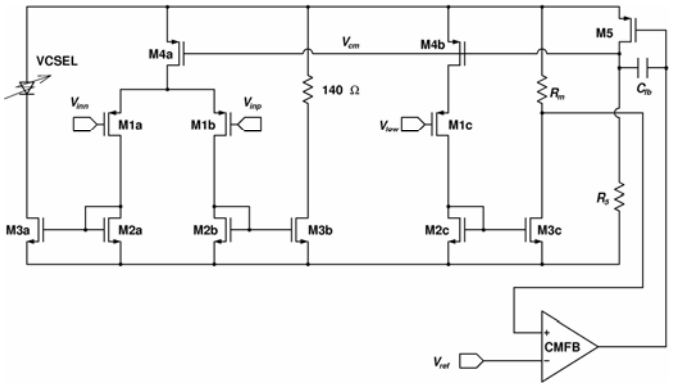

Figure 12: Schematic of the TTL compatible CMOS VCSEL driver.

Note that the input differential pair was implemented with PMOS transistors as is current source transistor M4a. The latter holds the main reason for this choice. The threshold voltage of this PMOS transistor can only decrease in response to radiation. This observation allows optimization of the feedback mechanism which aims to keep the value of this current constant.

Low dose rate experiments with DIL40 packaged driver IC's up to a total dose of 3.7 kGy (370 krad) have shown that the 90 % decrease in VCSEL current without the feedback loop is limited to only 2 % when the feedback is included. The eye diagram of the circuit at 155 Mbps showed no apparent degradation. A complementary experiment at a dose rate of 21 kGy/hr up to a total dose of 13.5 MGy has shown that the VCSEL current only drops by 10 % after a TID of 3.5 MGy (350 Mrad). This is illustrated in Figure 13, which compares the relative VCSEL current from the driver output in the on-state as measured in-situ, during irradiation, with and without the feedback.

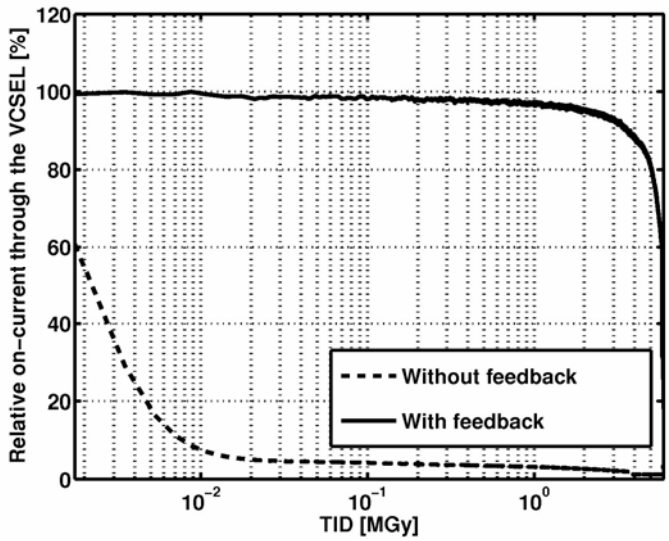

Figure 13: Measured relative VCSEL current from the driver output with the feedback network either activated or disabled. Dose rate of 21 kGy/hr.

Again, the circuit loses functionality quickly when the correcting feedback circuit is disabled. The output current through the VCSEL has already dropped to 60 % when the first measurement is taken after the irradiation started. It drops further to 10 % after 8 kGy. With the feedback network enabled, the output current drops only 10 % after 3.5 MGy. The circuit starts to break down and looses its functionality completely after 6 MGy.

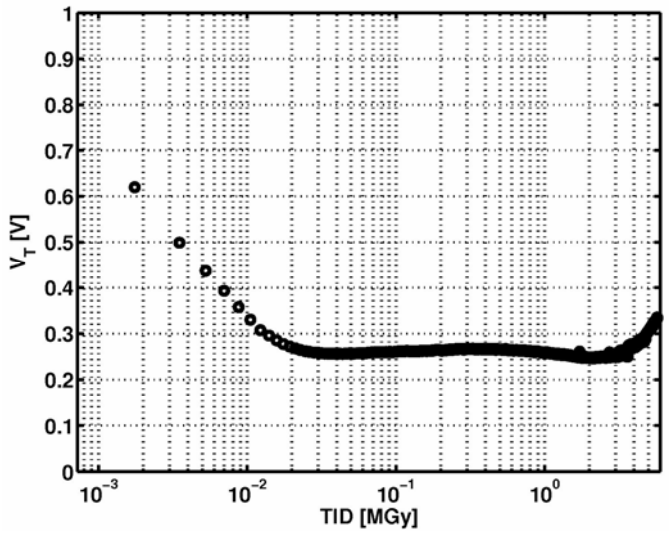

Figure 14: NMOS threshold voltage V_T as a function of TID. Dose rate of 21 kGy/hr.

The threshold voltage is plotted as a function of accumulated dose in Figure 14. For cumulated doses below 100 kGy, we obtain a reduced V_T. This is caused by the rising number of positively charged hole traps in the gate oxide which 'helps' to turn on the transistor. After roughly 3 MGy,

the V_T starts to increase again. This rebound is known to be caused by an increase in the number of negatively charged interface states at the boundary between the Si channel and the SiO_2 gate oxide. These negative charges counteract the positive holes, trapped in the gate oxide and hence cause an increase in V_T. Our results also suggest a decreased mobility for the electrons in the channel, tentatively explained as a result of lattice defects created by high-energy compton electrons.

Depending on the envisaged application, more advanced integrated technologies could be considered as well, such as strained Si and SOI, which have even smaller feature sizes (65 nm and below). The applied tensile-strain inducing techniques boost the device performances as they increase the mobility of electrons, which is particularly of interest to NMOSFETs. Initial proton irradiations were performed, where a global technique using strained SOI was compared to a local technique, where strain is induced by a strained Contact Etch Stop-Layer (sCESL) [28]. These results have shown that irradiation has a different impact on some device characteristics, such as the threshold voltage shift and the behaviour of the parasitic back-channel transistor, depending on which tensile-strain-inducing technique is used. The main effect of proton irradiation is the creation of interface traps and positively charged holes trapped in the buried oxide. It was shown that the combination of strained Si with sCESL on a NMOS device will lead to the lowest radiation sensitivity, whereas PMOSFETs have a better radiation behavior when a strained Si-channel is used. For practical PMOS transistors, it is only relevant to evaluate the tensile strained Si, because in practice a compressive sCESL will be used instead of the tensile sCESL, which was studied in this paper. While these results are relevant for potential space applications, the high dose radiation assessment of these strained technologies is still to looked at.

VI. Summary

Maintenance tasks in the future ITER reactor will have to be performed in harsh radiation environments, requiring robust instrumentation and control equipment that can withstand MGy dose levels. Opto-electronic communication links between these maintenance tools and the control room present an interesting option as they would offer wavelength-encoded multiplexing possibilities. In this paper we summarized the main results obtained at SCK•CEN over the past years towards the development of radiation tolerant fibre-optic communication links, including the individual optical components such as optical fibres, laser diodes and photodetectors, as well as their associated electronic driver circuits. As our current efforts aim at further miniaturization and integration with rad-hard ASICs, the ITER community should benefit from their potential use in other radiation environments, such as the future SLHC, which will impose higher radiation levels to the equipment used up to several MGy. This possible common market supports the interest of a shared R&D program for future developments of O/E communication links for both high energy physics experiments and thermonuclear fusion reactor applications.

VII. Acknowledgements

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State of the art technologies for front-end hybrids

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Abstract

The front-end hybrids for solid state and gas detectors will be crucial components of the next generation particle detectors. Requirements such as high-density and high-speed interconnects, low mass, radiation resistance, high-current and high-power dissipation capabilities are examples of the challenges to be solved concurrently.

The technologies for front-end hybrids developed at CERN are presented and future possibilities such as embedding active and passive circuits are described. Comments are made concerning the ability to use these technologies for large scale production by industry.

I. Existing Technologies

To make hybrid interconnection circuits there are many different technologies available on the market (Figure 1). They can be split in two families: organic and mineral. The most used is the Printed Circuit Board (PCB) technology. For cost reasons other technologies are often only chosen when a higher density is needed.

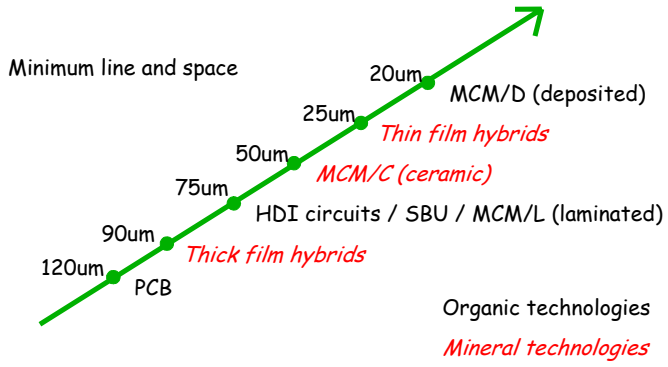

Figure 1: Hybrid circuit technologies

A. PCB

Printed Circuit Board technology is the one that has seen the largest improvements in the past ten years. The production process itself has not significantly changed but many new materials appear and automation equipment is now available to reduce the production time. The biggest interest in this technology is the low production cost and low to high volume capability.

PCB technology is limited by the mechanical drilling as the minimum hole size that can be obtained is around 0.15 mm. Minimum line width and spacing are around 100 µm depending on the supplier.

B. HDI

High Density Interconnect (HDI) technology is an improvement of PCBs were the mechanical drilling in the high density parts of a board has been replaced with laser drilling or plasma ablation. All the other processes stay similar to PCBs. It is clear that these circuits are interesting in many aspects for high-energy physics as it provides reliable high density circuits for a low cost. A further advantage is that HDI technology is available from many companies. The size of the via holes can be reduced down to 50 µm allowing a pad size of 150 to 200 µm. Small vias of this size are also known as micro-vias. Usually the boards are smaller than PCBs which permits to reduce the track width down to 40 to 70 µm. The thicknesses of the metal layers are also reduced down to 15 µm instead of the minimal 35 µm used in PCB technology.

C. Thick film and MCM/C

Thick film ceramic hybrids have been used in the past in physics because of the possibility to build circuits with a higher connection density than PCBs. With etched metals and photo-imageable dielectrics it still is possible to have a higher density than HDI circuits. The other advantages come from the fact that it is a full mineral technology allowing high operating temperatures with low degassing and the best long term stability of all technologies. However, the price, the difficulty to build in large volumes and the more complicated assembly process make that this technology is mainly used in vacuum and high temperature (e.g. power) applications.

D. Thin film and MCM/D

The use of vacuum metal deposition and liquid polyimide gives the possibility to make tracks down to 20 µm and micro-vias down to 25 µm in size. These technologies are used in very high density compact modules and are compatible with direct silicium chip bonding. The production costs are higher than the other technologies because of the use of glass masks and the need for special equipment for alignment. The dielectrics need a high temperature of around 300 °C to be properly cured.

II. Pitch Adaptors

In many physics applications silicon chips with a bonding pitch of 45 µm are used. This pitch needs tracks and spacing of 20 µm on the supporting circuit. The only technologies that can reach this density are thin film and MCM/D.

Thin film allows making even smaller lines but always with only a single layer on a glass or ceramic substrate. In this

case the high density connection circuit should be added by gluing the pitch adaptor to an HDI or PCB substrate and then they should be wire bonded together. This assembly is delicate due to the precise positioning needed.

With MCM/D the pitch adaptor can be directly routed in the circuit. This solution is most of the time not cost effective because the full circuit area will be made with a very high density process.

A third solution consists in keeping a conventional thick film or HDI technology circuit and split the dense area in many layers. This is easily obtained with thick film were one can stack up to three layers at a pitch of 80 µm and make openings to reach all the contacts. With HDI circuits it is possible to do this with laser, plasma or chemical ablation. The principle is still the same: split the high density part in many layers to be compatible with the technology and open the dielectrics to make the contacts reachable by wire bonding. Figure 2 shows different examples of pitch adapters.

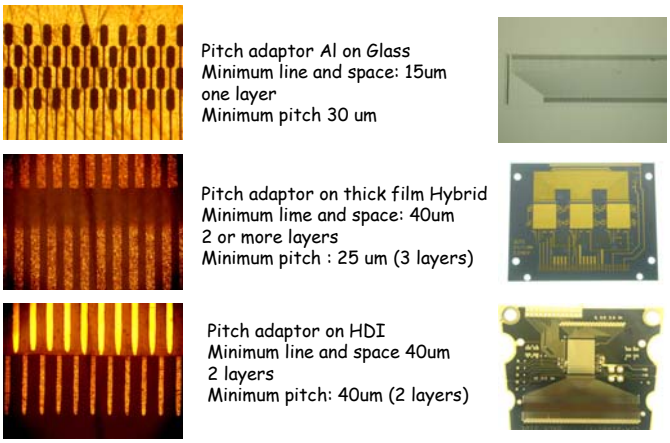

Figure 2: Pitch adapters made in different technologies

Other advantages to build the pitch adaptor in HDI technology are: lower cost, possibility to have thinner materials, better dielectrics and the possibility to cut the circuit in any shape, including round ones.

III. Trends of future Circuit materials

Many new materials are now available or in development to build PCBs and HDI circuits. For each new project five topics need to be addressed in order to make an optimal choice: manufacturability, reliability, environmental considerations and miniaturisation (Table 1).

Table 1: Circuit material selection criteria

Manufacturability	Reliability	Environmental	Functionality	Miniaturisation
Process compatibility Registration Drilling compatibility	Low CTE Fillers High TG CAF-resistant	Halogen free Lead Free	Low Dk Low Df Embedded components	Embedded component Metal core

A. *Manufacturability*

Woven glass epoxy composites such as FR4 are still the easiest materials to process. But with the introduction of laser drilling new concerns have appeared: shape of the micro-vias, difficulty to process anisotropic materials, cleaning of the micro-vias and the metal adhesion to the dielectrics.

Many developments have been carried out to find glass or Kevlar reinforced materials with the same laser drilling behaviour as can be obtained with homogeneous materials like pure epoxy or polyimide. As a result it is nowadays possible to drill these materials by laser as for example a homogeneous glass cloth has been developed.

The dimensional stability throughout the production processes is also an issue when density is increased. In conventional technologies a mismatch of 100 to 200 µm is still acceptable over a board of 400 mm x 400 mm in size. In HDI boards the alignment mismatch should be kept below 50 µm to fit with the photolithographic possibilities. This dimensional stability limits the use of existing materials. For example standard polyimide, which is one of the best materials for HDI processes concerning patterning and laser drilling, was one of the worst concerning large boards registration. New polyimides are now available with a better mechanical stability but on large boards it is still difficult to realise the full density potential of these materials.

B. *Reliability*

For the best reliability the materials should have a thermal expansion coefficient (CTE) that is in the X and Y axis as close as possible to the components attached to the board (4 ppm/°C for chip on board and around 15 ppm/°C for encapsulated components), and should have a well controlled CTE in the Z-axis. In most of the composite materials there is a matrix that constraints to a low CTE in the X and Y axis but it leaves the expansion in the Z-direction free. New materials have been developed with high Tg resins, with in some cases special fillers to avoid any cracks in the metalised holes. For long term stability the conductive anodic filament (CAF) resistance should also be taken in account in the material choice. CAF is a phenomenon of copper migration through the glass fibres in the circuit board [1].

C. *Environmental*

The regulations concerning the use of materials containing heavy metals and containing halogens have changed in 2006. Firstly the European Community RoHS regulation imposes to PCB manufacturers to remove all heavy metals like lead in circuits. In PCB production lead was fortunately only used to create the finishing layer and this problem was easily solved by using Ni/Au or Immersion Tin finishes instead of Tin/Lead. The biggest concern comes from assembly. The new lead-free alloys used to solder the components have a fusion temperature that is 50 degrees higher than classic Tin/Lead solders. The use of PCB materials with a higher Tg and controlled CTE are now mandatory to avoid board destruction during assembly [2].

Concerning halogen-free materials there is no formal obligation in the European Community to use them. However, to prevent toxic fumes to be generated during a fire in for example one of the tunnels, CERN's safety regulations impose the use of halogen free materials in electronics boards. Unfortunately not all PCB vendors can provide this type of material.

D. Functionality

The most important electric parameters in the choice of isolating dielectrics are the dielectric constant and the dissipation factor [3]. These two parameters define the impedances of a board and the quality of signal transmission and therefore the maximum reachable speeds.

Many producers of base materials are trying to build improved materials that can be processed with conventional production lines. We start to see for example glass epoxy materials with one order of magnitude reduction in the dissipation factor. For low dielectric constants only special materials such as PTFE and Polyimide can be used.

The functionality of boards can also be increased by the use of buried components such as embedded resistors and capacitors.

E. Miniaturisation

Miniaturisation can be increased by the use of embedded components. The area gain is clear with resistors while with capacitors the decoupling between power layers can save board space and routing area. However, increasing the miniaturisation increases the problem of thermal cooling. In many applications the power dissipated by the components cannot be removed by convection alone. Adding a thermally conductive core can often solve this problem.

IV. Cooling

Metals, carbon composites or graphite and ceramics are the three material families that can be used for thermal management in hybrids (Table 2). The perfect material should have a thermal expansion coefficient close to that of silicon (4 ppm/°C), a high isotropic thermal conduction, a high radiation length and should be easy to process and all this at a reasonable cost.

A. Metals

Metals are often used because of their price and the ease of processing. Some of them have very interesting CTE and thermal conductivity characteristics. CIC (copper/invar/ copper) is a composite that can be introduced directly in the hybrid circuit to reduce the CTE and functions as a thermal drain at the same time. It can also be used as a conductive layer. CIC is not used as a substrate as it is too flexible. Aluminium is more critical if one wants to embed it in the circuit: the CTE is too large to create a reliable structure. It should be used as a substrate onto which a hybrid can be glued with special elastic glues. Al/Si alloys have been developed to create a material that is stiff enough to be a substrate with a good thermal conduction and with a controlled CTE at the same time.

B. Carbon based materials

There are no materials with better properties than carbon for thermal management. Carbon is light and carbon fibre can be used as a stiff substrate while the CTE is low which is interesting for chip on board applications. Pyrolytic graphite can have a thermal conductivity of up to 1600 W/m°C which is about eight times the thermal conductivity of aluminium. The disadvantages of these materials are the price, the complexity of the processes to obtain a good adhesion and their anisotropic properties. The temperature range for structures containing carbon is often limited compared to metals or ceramics.

Table 2: Materials used for thermal management

	CTE [ppm/°C]	Thermal conductivity [W/m°C]	Process	*Price*
CIC	5	170	easiest	low
Aluminum	22	220	easy	low
Al/ Si	6-15	120	easy	medium
Carbon fibre	2	Up to 1000/ z 10	difficult	medium
Carbon carbon	2	600/z 300	difficult	high
PG	0	600/z 8	difficult	high
TPG	0	1600/z 8	Very difficult	Very high
Alumina	7	22	easy	low
Berylia	8	300	easy	high
AlN	4	100-230	difficult	medium

C. Ceramics

Ceramics have been widely used in thick film and thin film technologies. They can also be used as substrates for HDI hybrids. Their CTE can be closely matched with silicon which makes them the best type of substrate for high reliability applications. Alumina remains the most frequently used material but its thermal conductivity is the limiting factor. Berylia is not only used for its good thermal conductivity but also because the material has a very high radiation length which means it does not easily stop particles when used inside a particle detector. AlN (aluminium nitride) is the best material for high temperature and high reliability modules due to its perfect CTE match with silicon.

V. Low Mass

High energy physics has a particular demand for low mass circuits. When used inside a particle detector, a circuit made of copper or heavy heat sinks can stop particles or create multiple scatterings which degrades the precision of the detector. Therefore at CERN a project was undertaken to develop a process to build low-mass circuits that are usable inside particle detectors [4].

Table 3 shows a few materials used in electronics with their principal characteristics concerning radiation transparency. Beryllium is the lightest metal but due to its toxicity it is impossible to use it. Aluminium is still close to 6.5 times more transparent than copper and offers the best

compromise between transparency and conductivity. With dielectrics the difference is not so large depending on the type of material. The choice is driven more by the radiation resistance and in this field Polyimide is still one of the best materials.

Table 3: Some physical parameters of base materials

Material	Radiation length [cm]	Density [g/cc]	*Resistivity [µOhm*cm]*
Aluminium	8.9	2.7	*2.7*
Copper	1.4	9.0	*1.7*
Beryllium	35.3	1.9	*3.3*
Gold	0.3	19.3	*2.4*
Glass epoxy	19.4		
Polyimide	29.0		

The newly developed process converted the conventional HDI micro-via technology into a low mass technology with design rules and structures similar to copper HDIs. The main challenge was to replace the conventional copper layers by aluminium. Copper can be deposited chemically on dielectrics or electrochemically on metals. Unfortunately aluminium can only be deposited by vacuum deposition. After a long period of study and many trials we have been able to deposit in a reliable way a 15 µm aluminium layer on polyimide and also plate micro-vias at the same time.

The first application of such a low-mass circuit is the ALICE pixel bus. More than 120 buses have been produced. This 160 mm by 14 mm sized bus has five aluminium metal layers with lines and spacing down to 70 µm. The total thickness is less than 250 µm with two aluminium layers of each 50 µm thick for carrying the power and three 12 µm thick layers carrying the signals.

VI. BURIED COMPONENTS

Buried passive components are quite common in some technologies such as thick film and thin film. In thick film technology the resistors are obtained by screen printing ruthenium oxide pastes. These resistors are in fact made in the same way as SMD discrete resistors. For capacitors high dielectric constants materials with an ε_r of up to 10000 are used. With thin film technologies only resistors can be made easily. In this case a thin layer of Ni/Cr is vacuum deposited and patterned chemically. The thermal stability of these resistors is in the range of a few ppm/°C but the absolute value is limited compared to thick film. In thick film technology, resistors from milli-Ohms to Giga-Ohms can be obtained while in thin film technology the maximum value is around a few hundred Kilo-Ohm.

Producers of PCBs have tried to do the same with organic technologies (PCB, HDI). Since roughly ten years materials are now available to create buried resistors and capacitors, while developments are still in progress to embed active silicon. In all the technologies also inductors have been embedded but the use is more marginal. A successful application of buried components however is the integration of antennas in printed circuits.

A. Embedded resistors in PCBs

The principle of embedding resistors in printed circuit boards is close to that used in thin film technology. The resistive layer is deposited or chemically grown on a copper foil. Values up to 250 ohms per square can be obtained. This foil is then with the resistive part inside glued to one layer of a PCB (Figure 3, step a). Three steps of photolithographic processes are then following in order to create the resistor. Step b defines the tracks and the outside shape of the resistor, step c removes the non used resistive area and step d opens the real resistive area. The accuracy of these resistors is about ±10% after etching. The resistor can then be trimmed with a laser to reach ±1%. This trimming plus the special etching processes steps are the limiting factor for low and medium volume production.

The main advantages of these embedded resistors are the possibility to increase the board density, the reduction cost of the PCB assembly, an improvement in impedance matching, the reduction of series inductance, and a lowering of crosstalk and noise levels.

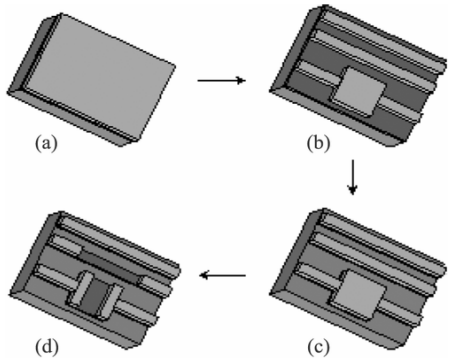

Figure 3: Process steps for embedding resistors

B. Embedded capacitors in PCBs

Embedding capacitors simplifies the assembly, gives the possibility to increase the board density and gives better high frequency properties to the board.

To embed capacitors in PCBs, the principle is the same for all technologies: create two electrodes facing each other in two successive layers. The value is defined by the area of these electrodes, the thickness of the dielectric and the dielectric constant. The dielectric thickness has been reduced to 10 µm by some producers which increases the capacity with a factor of five compared to standard dielectrics (e.g. ZBC2000 material from Sanmina corp). The other way to raise the value is to increase the dielectric constant. This is achieved by loading the dielectric with ceramic particles. For example the company OAK-MITSUI has developed a material with an ε_r of 30 which makes capacities of 1.7nF/cm^2 possible.

It is still difficult to create discrete capacitors but for power decoupling this technology is able to create capacitors in the µF range.

C. *Embedded active silicon in PCBs*

One can also embed silicium ICs in a PCB. The principle is to glue a thinned chip to a standard PCB and to glue on top of it a layer of resin coated copper (RCC) thicker than the chip using standard processes [5].

Figure 4 shows a 50 µm chip buried in a 100 µm RCC layer (build-up 2). The connections to the chip are created with laser micro-vias followed by a classical chemical copper metallization and electroplating reinforcement. The difficulty at this stage is to stop the laser ablation on the chip metallization.

Some tests have been performed on chips with reinforced copper metallization to avoid any destruction of the chip by the laser. The second problem comes from the thermal expansion mismatch between the chip and the RCC (60 ppm/°C for RCC and 4 for silicon). This problem can be avoided by using glues with fillers such as aramid epoxy.

The main advantage of this technology is that all connections to the chip are made directly inside the board, therefore eliminating the need for wire bonding. Chips even may be stacked and thermal management is easier as heat can be removed from both sides of the chip.

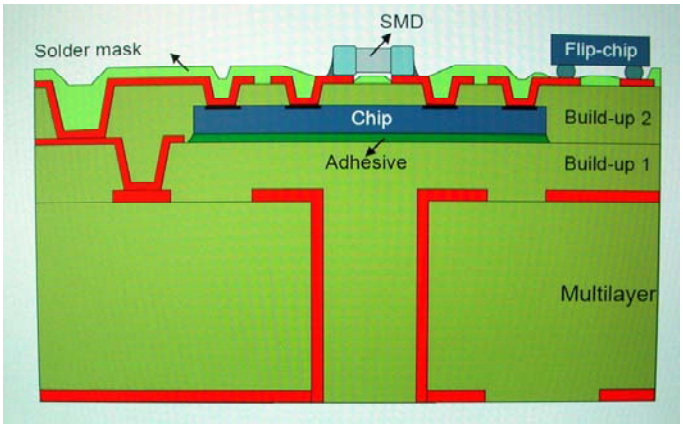

Figure 4: Embedded Si chip not needing wire-bonding

VII. CONCLUSIONS

The most appropriate technologies for front end electronics are HDI and SBU. These technologies offer a high enough density for a good price as many companies are now able to build these components in mass volume. In some applications the required density is higher than usual but even in these cases it is possible to increase the density locally so that the high precision alignments are only needed in a specific area.

Many materials are available for thermal management. The choice should be driven not only by the thermal characteristics of these materials but also by their processability. Simulation tools exist to test several options.

With the CERN developed process, low mass circuits with aluminium tracks and thin polyimide dielectrics are now available for low to medium volume production. The design rules and possible structures are close to conventional copper HDIs.

In order to increase the density or to improve the functionality it is possible to embed resistors, capacitors and more recently some companies have tried to embed even silicon in the PCBs.

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Plenary Session 4

HEP electronic and ASIC trends

Development of 3D Integrated Circuits for HEP

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Abstract

Three dimensional integrated circuits are well suited to improving circuit bandwidth and increasing effective circuit density. Recent advances in industry have made 3D integrated circuits an option for HEP. The 3D technology is discussed in this paper and several examples are shown. Design of a 3D demonstrator chip for the ILC is presented.

I. Introduction

Requirements for High Energy Physics front end electronics and detectors continue to push the limits for lower mass and power, and higher resolution. One example is pixel vertex detectors, where multiple scattering within the readout electronics and detectors limits track resolution. Low mass is required to limit multiple scattering making cooling difficult and leading to low power designs. Higher granularity is needed for more precise tracking which leads to higher function density within the pixel cell.

Significant progress has been made in the last decade to address these issues by integrating sensors and front end electronics within the pixel cell. MAPS (Monolithic Active Pixel Sensors) began the move toward integrated sensors and readout electronics. More recently success has been demonstrated in integrating sensors and CMOS circuitry using SOI technology. Now, 3D integrated electronics is offering exciting new possibilities.

A. Monolithic Active Pixel Sensors

MAPS have generated much interest within the HEP community. To reduce mass, MAPS combine detector and front end electronics on the same substrate in a commercial CMOS process. Currently, numerous groups are working on MAPS development.

As impressive as MAPS are, there are several practical limitations. First, the size of the detector signal is generally small and dependent on the thickness of an epi layer which varies from process to process. Due to the nature of the process, only NMOS transistors can be easily used. Addition of PMOS devices in an N-well reduces the charge collection efficiency and affects the spacial resolution. Finally, the functionality that can be squeezed into a small pixel for higher resolution is limited.

B. SOI Integrated Detector Development

SOI detector wafers are formed by bonding together a top wafer with low resistivity and a bottom wafer with high resistivity, using a silicon oxide bond. A buried oxide is formed between the wafers. After bonding, the top wafer is thinned to just a few microns using one of several different techniques. Later, vias are etched through the buried oxide to implant diodes in the bottom wafer and CMOS circuitry is built on the top wafer.

SOI integrated detectors have several advantages over MAPS. One big advantage is that both NMOS and PMOS transistors can be easily accommodated in the design. The devices inherently can have larger detector signals since the thickness of the depleted detector substrate can be controlled. Finally, since the substrate can be fully depleted, less charge spreading and higher speed is possible compared to MAPS.

Early detector work was done in a 3 micron SOI technology [1]. Recent work has been done in the OKI 0.15 micron SOI process [2]. Fermilab has an arrangement to work with American Semiconductor Inc. and OKI on future SOI detector developments.

Although SOI has significant advantages over MAPS, the functionality that can be placed in a small pixel cell is still rather limited. 3D circuit integration reduces that limitation.

C. 3D Integrated Circuit

A 3D integrated circuit is generally referred to as a chip comprised of two or more layers of semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit. Often the layers (sometimes called tiers) are fabricated in different foundry processes.

Industry is moving toward 3D circuits which permit shorter interconnects to reduce R, L, and C and provide higher speed. 3D also provides higher functionality per unit area and can reduce interconnect power and crosstalk.

3D integrated circuits represent the physicist's dream of combining large functionality with processes optimized for high performance, in a very small area as shown in Figure 1.

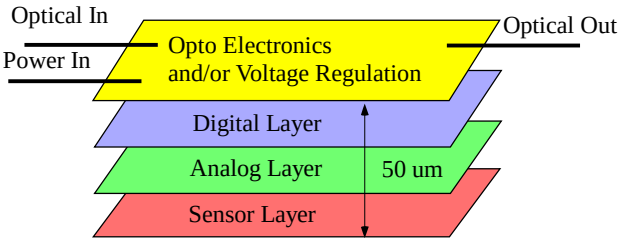

Figure 1: Thin 3D circuit with multiple tiers for HEP

Much work is being done on pixel arrays using 3D integration that could make this dream come true.

II. 3D Circuit Development

Work sponsored by United States Department of Energy under contact No. DE-AC02-76CH03000.

A. Advantages

A good way to see the advantages of 3D integration is to look at the layout of a conventional MAPS device and an equivalent 3D device as shown in Figure 2.

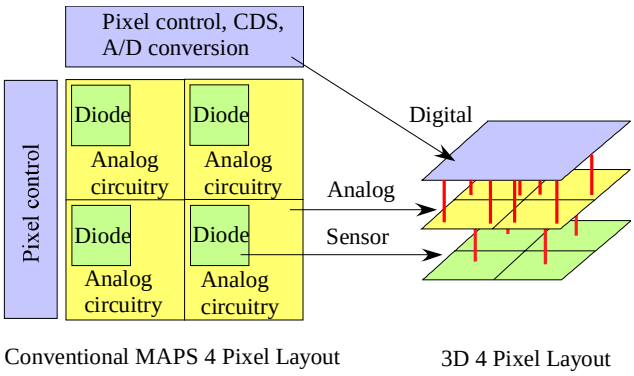

Figure 2: Comparison of MAPS and 3D Pixel Layout

By placing circuitry on a separate layer from the sensor diodes, both NMOS and PMOS transistors can be used in the circuit design. Having a separate layer for digital functions, allows most of the circuitry usually placed around the periphery of the array to be placed above the array, providing a large amount of functionality in each pixel.

B. Key Technologies

Dozens of companies and organizations are working on 3D integrated circuits in the United States, Europe, and Asia. Companies such as IBM, Intel, Phillips, STM, Toshiba, and Samsung, and organizations such as MIT Lincoln Labs and the Fraunhofer Institute IZM-Munich are very active in 3D. Each of them has their own approach to working on the four key technologies needed for 3D: 1) bonding between layers using oxide to oxide fusion, copper tin eutectic bonding, or polymer bonding, 2) wafer thinning using a combination of grinding, lapping, etching and CMP, 3) through wafer vias using different processes (some of which need to include hole passivation), and 4) high precision alignment of parts before bonding [3].

C. Approaches for HEP

There are two different approaches that are useful for HEP as shown in Figure 3. The first approach uses a die to wafer or die to die bonding technique. Dice are tested and sorted before being bonded to a target wafer, resulting in a higher overall yield. This approach is conducive to using devices from different processes. Thus one can bond SOI to CMOS, CCDs to CMOS, or DEPFETs to CMOS, etc.

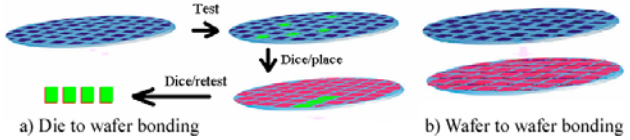

Figure 3: a) Die to wafer bond b) wafer to wafer bond

In the second approach, wafers are bonded to other wafers. For efficient use of silicon, the dice on the different wafers should be of the same size. Tight alignment tolerances are required over the entire wafer area and overall yield will be lower. The wafers could be of different technologies but there are significant advantages if the wafers are all made in an SOI process. The SOI process allows the wafer to be easily thinned to the buried oxide layer, resulting in active circuit layers that are less than 10 microns thick. Furthermore, the via formation in SOI is easier than in CMOS processes.

1) Die to wafer bonding:

With the die to wafer approach, the parts may be bonded face to back (circuit side to substrate side) or face to face. Figure 4 shows one way in which the devices are bonded and the vias are formed. It is necessary in the design to leave space for the inter-device vias. If vias pass through a CMOS layer, the vias must be insulated from the substrate.

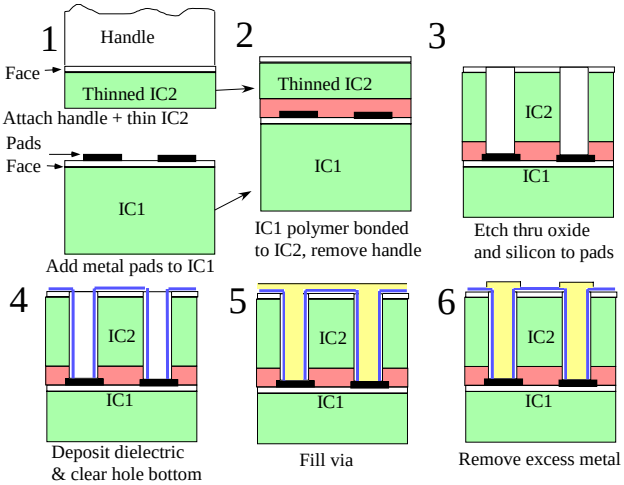

Figure 4: Steps showing polymer bonding and via formation for die to wafer process.

The polymer bond technique was used by RTI International to build a 3D infrared pixel array [4]. The array is a stack of 3 layers fabricated in three different processes: 1) the sensor is HgCdTe, 2) the analog circuitry (30 um thick) is made in 0.25 um CMOS, and 3) the digital part is made in a 0.18 um CMOS process. The array is 256 x 256 with 30 micron square pixels. Vias (4 µm dia.) were etched using the Bosch process. A chip cross section is shown in figure 5.

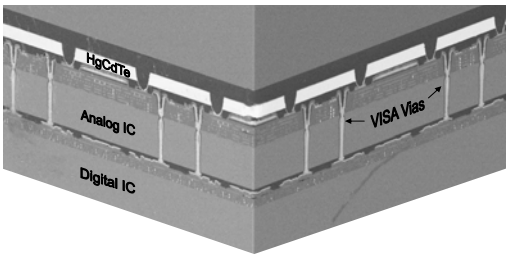

Figure 5: Cross section of 3D infrared pixel array

Face to face bonds can be made using a Cu_3Sn eutectic bond for both the electrical and mechanical connections between devices. This could be a possible replacement for conventional bump bonds. In applications to date, the Cu/Sn bonds cover a large portion of the mating surface areas with about 10 µm of copper. Because 10 µm of copper is 0.07% of a radiation length, Fermilab is investigating procedures to reduce the copper coverage to less than 10% of the mating areas. Our goal is to have 7 µm bumps on a 20 µm pitch.

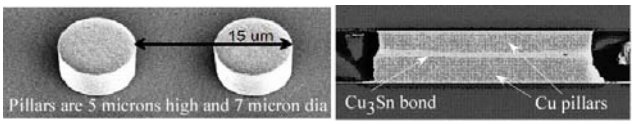

Figure 6: Cu pillar on 15 µm pitch and bond cross section.

RTI has made test structures, shown in Figure 6, which suggests that fine pitch Cu/Sn bonds are possible.

The process for the Cu/Sn bond is shown in Figure 7. A double handle transfer is required as shown in steps 2 and 3.

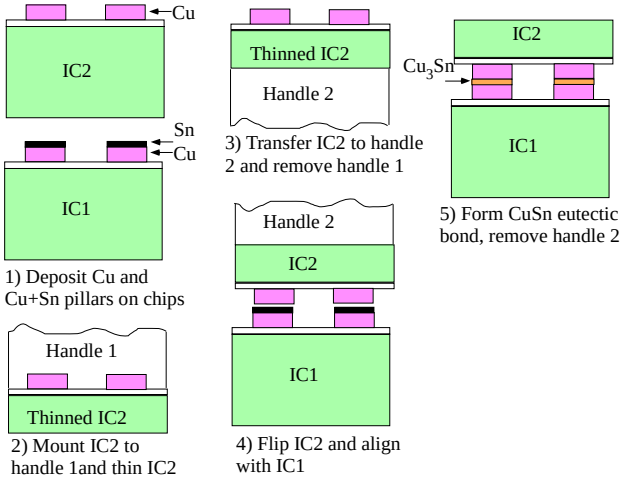

Figure 7: Face to face bond using Cu_3Sn

The IZM Fraunhofer Institute has used the Cu_3Sn bond technique to attach 10 µm thick chips to a target substrate [5]. In this case, the Cu bonds cover a large portion of the mating surfaces to provide mechanical support during processing. See figure 8.

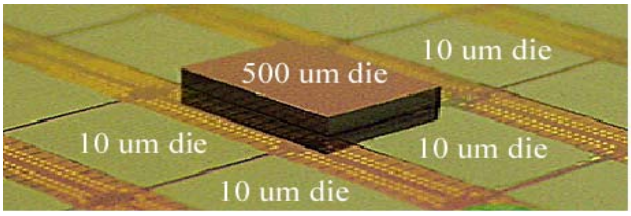

Figure 8: Chips 10 µm thick mounted on target substrate using Cu_3Sn along with unthinned 500 micron die for comparison.

2) Wafer to wafer bonding:

Wafers are frequently bonded together using an SiO_2 bond. For good bonding, the wafers must be very flat and the surfaces must be extremely clean. The techniques used for SOI detector wafer bonding and 3D wafer bonding are similar. For SOI detector design, the processing of each wafer is done after bonding. For 3D circuit design, processing of each wafer is done before bonding.

SOI wafers have several advantages for 3D wafer stacking. Each wafer can be easily thinned to the buried oxide layer (BOX) since the buried layer acts as an etch stop. Wafers have been thinned to 6 microns as shown in Figure 9.

3D wafer to wafer stacking has been used to build large pixel arrays. Lincoln Laboratories has built a two tier, 1024 x 1024 pixel array, CMOS image sensor with 8 µm square pixels [6]. Two 150 mm wafers were stacked using oxide

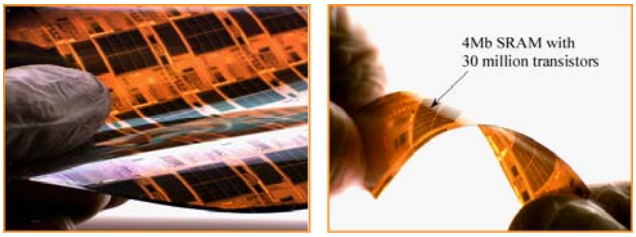

Figure 9: Wafer thinned to 6 microns and mounted to 3 mil kapton (courtesy of MIT Lincoln Labs)

bonding. The first tier has the sensing diodes in a 3000 ohm-cm substrate, 50 micron thick. The second tier, which is only 7 microns thick, is made in a 0.35 µm SOI CMOS process. Vias (2 µm dia.) were dry etched and filled with tungsten. Each array has one million 3D vias with 99.999% yield. Figure 10 shows a cross sectional representation of the chip.

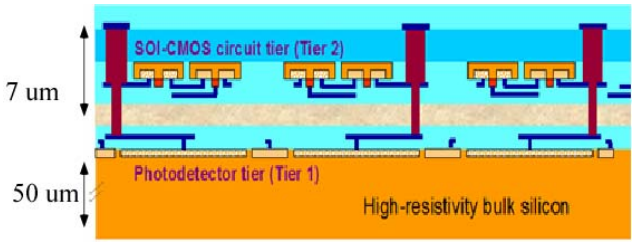

Figure 10: Cross section of CMOS imager showing 3D vias [7]

Stacking of three SOI layers has also been demonstrated by Lincoln Laboratory in a 3D Laser Radar Imager chip [8]. The chip is a 64 x 64 array of 50 µm square pixels. The first layer or tier is the high resistivity substrate with Geiger-mode APD light sensors. The second tier is made in a 0.35 µm SOI process using high voltage devices for control of the APDs. The third tier uses a 0.18 µm SOI process for maximum density of the digital circuitry. There are six 3D vias in every pixel cell. Figure 11 shows a cross section of the chip.

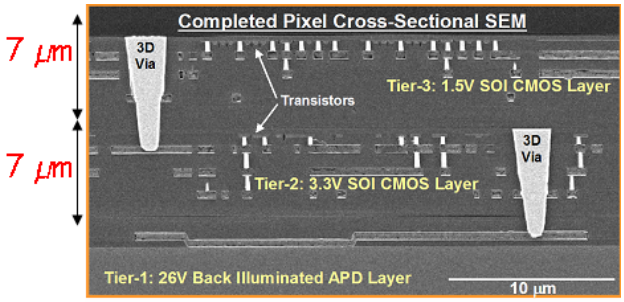

Figure 11: Cross section of 3 tier Laser Imager chip.

III. Design of a 3D ASIC for HEP

To show the capability of the 3D process for HEP, design of a readout chip has been undertaken. The ILC (International Linear Collider) vertex pixel detector has been chosen to demonstrate 3D design.

A. ILC Vertex Pixel Requirements

The ILC is expected to have a beam structure with 2820 crossings in a 1 msec beam train, occurring 5 times/sec. The pixel detector is comprised of 5 small concentric cylinders of pixels wrapped around the beam crossing point. It is assumed

that 0.03 particles will pass through each square millimeter on the surface of the inner most cylinder for every beam crossing. To allow for charge spreading, hits between pixels, and magnetic field effects, it is assumed that there are 3 hit pixels for every particle. Thus the hit rate on each cylinder is 252 hits/beam train/mm [9].

Resolution for the pixel detector should be 5 microns or better. For 15 micron pixels, the resolution for a simple binary readout system would be 4.3 microns. For 20 micron pixels, the resolution would be 5.8 microns.

Sparsification is highly desirable to reduce the volume of data being transmitted off the chip and to reduce the digital power dissipated in the chip. Even though the expected occupancy per pixel is quite small, physics would benefit from time stamping. The pixel hit time is used for reconstructing a particle track in association with data from other detectors.

As mentioned, the occupancy in a given pixel cell is expected to be very low. In a 15 micron square pixel, the number of hits/ bunch train would be 250 hits/mm^2 x (15 µm x 15 µm) = 0.056 hits/bunch train. Thus the chance of a pixel being hit twice in a bunch train is 0.056 x 0.056 or only 0.3%. If just 1 hit is recorded for each pixel, it follows that 99.7% of the hits are recorded unambiguously. Similarly, if the pixel is 20 microns, 99% of the hits are recorded unambiguously.

B. Demonstrator Chip Design

A number of design choices have been made which demonstrate the functionality that can be contained in a small pixel cell. The chip was originally designed for a binary readout, but an analog readout was added in the event that analog information proves useful. The hits for the ILC bunch train have been divided into 32 time slices. Expansion to 64 or more time slices is possible. The time slice information is stored within the pixel cell. A look-ahead token passing scheme was incorporated to sparsify the hit data on the chip. To reduce the size of the pixel, the pixel addresses are stored on the periphery. The chip design was divided into 3 tiers for fabrication in a MIT Lincoln Laboratory multi-project run. Since a detector layer is not available in this run, the intention is to mate the demonstrator chip to a detector at a later time. The chip is designed for a 1024 x 1024 array, but for economy has been laid out as a 64 x 64 array.

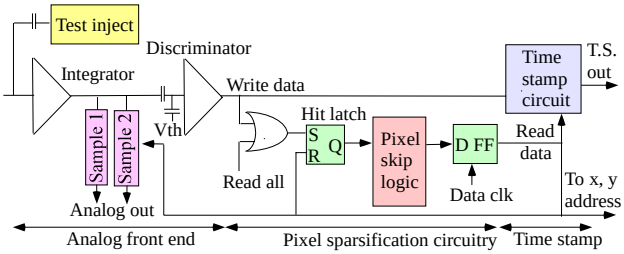

Figure 12: ILC Demonstrator Chip Pixel Cell

A simplified diagram of one pixel cell is shown in Figure 12. The front end consists of an integrator and a double correlated sampler. The signal is capacitively coupled into a discriminator that has a chip-wide settable threshold. Output of the discriminator is fed to the time stamp circuit, and through an OR gate to a Hit Latch. The OR gate allows all cells to be read regardless of the input signal. The Hit Latch along with the pixel skip logic and D flip flop performs the data sparsification. A programmable register is used to inject a test signal into every pixel cell.

The time stamp block shown in Figure 12 contains both a digital and an analog time stamp. This is done only for test purposes. The digital time is generated by a slow 5-bit Gray code counter on the perimeter which is clocked at about 30 µsec/step. The counter time is sent to all cells, where it is latched by the pixel hit signal. The hit time stored in the cell is read out on the same 5-bit bus after the beam train is over. The analog time stamp is formed from a slow voltage ramp that is sent to all pixels and sampled by the pixel hit signal. After the beam train, the stored analog voltage is read out on a separate bus to an external ADC. The digital time stamp has the advantage of not requiring calibration while the analog time stamp has the advantage of requiring less silicon area.

A 1000 x 1000 pixel array is shown in Figure 13. During data acquisition, a latch is set in each pixel that is hit. After a beam train, sparse readout is performed row by row. To start readout, all hit pixels are disabled except the first hit pixel in the readout scan. The pixel being read out points to the X and Y addresses that are stored on the perimeter. At the same time the digital time stamp in the cell and all the analog information stored in the cell is sent to the edge of the chip.

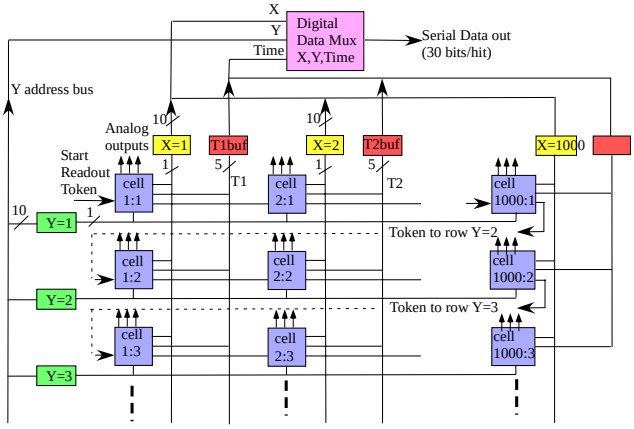

Figure 13: Demonstrator Pixel Array for ILC

While a pixel is being read, the token scans ahead, looking for the next pixel to read. To assure finding the next hit pixel before the token arrives, the chip is set to always read out at least 1 pixel per row regardless of the hit pattern. The token passing speed is 0.2 nsec per pixel. If there are 1000 cells in a row, the maximum time to reach the next cell to be read is 200 nsec. All the digital information is serialized on the perimeter of the chip for transmission off the chip. It is assumed that the serializer runs at a very reasonable 50 MHz. Thus, allowing 10 bits for the X and 10 bits for the Y addresses, along with 10 bits for the digital time stamp and status, a hit pixel is read out in 600 nsec, which is far more than the time required to find the next hit pixel.

For the ILC pixel vertex detector, there is 200 msec to read out the hits in a bunch train before the next train arrives. Assuming a 1000 x 1000 array of 15 µm pixels, the maximum number of hits in the hottest part of the detector is calculated to be about 56,250. If one extra pixel is readout in each row, the maximum number of pixels to be read is 57,250. To read

57,250 pixels with 30 bits/pixel at 50 MHz takes 34 msec. For a Megapixel chip with 20 micron pixels, the readout time would be 60 msec. Thus the readout time is far less than the ILC allowed 200 msec. Therefore the readout clock can be even slower, or several chips can share the same readout bus. Since the digital outputs are CMOS, the power is only dependent on the number of bits being read, and not the length of time needed for read out.

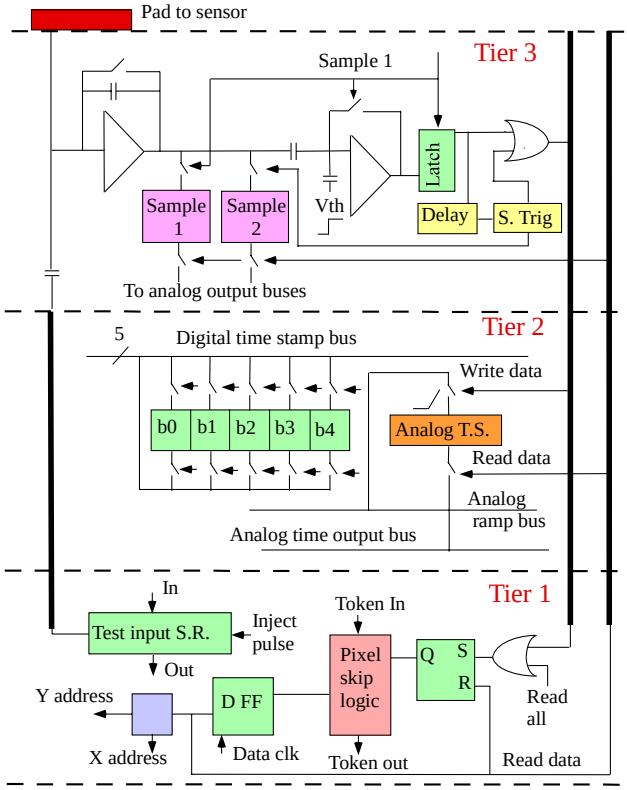

Figure 14: Division of ILC pixel design into 3 tiers.

Figure 14 shows how the pixel readout chip is divided into 3 tiers. Tier 3 contains most of the analog circuitry (38 transistors + storage capacitors), tier 2 contains all of the time stamp circuitry (72 transistors), and tier 1 primarily contains the sparsification logic (65 transistors). The thick vertical lines show the vias that are formed to interconnect the tiers. Figure 15 shows roughly how much area was required by the different circuit elements on each of the three tiers in the design. Each pixel cell is 20 µm x 20 µm.

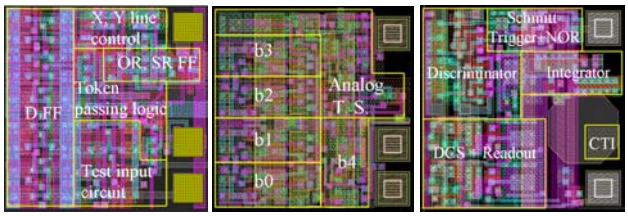

Figure 15: Tier layouts from left to right: sparsification, time stamp, analog.

The demonstrator chip is a multifunctional device to be used a proof of the 3D principle for HEP. It is a 64 x 64 array that can be expanded to 1000 x 1000. There are 175 transistors in each 20 micron pixel. The active thickness of the 3 combined layers is only 22 microns. A choice will be made for future applications that will select analog or binary readout and one of the two time stamp approaches. The current chip has provision for a test input signal which can be expanded to include a pixel disable circuit with little extra circuitry. The power dissipated by a full scale version of this chip is consistent with air cooling of the ILC pixel vertex detector. The support logic around the perimeter of this chip is small. In future designs, this can be reduced further. The chip is to be submitted for fabrication in a multi-project run at MIT Lincoln Labs on October 1, 2006.

IV. Conclusion

Industry is moving toward three dimensional integrated circuits. 3D is a natural progression for higher performance and higher functionality and is opening new approaches for HEP applications such as pixel arrays. Several approaches, such as die to wafer bonding, wafer to wafer bonding, or a combination of the two, are possible for pixels. Fermilab is working on a number of these ideas for 3D integration.

V. Acknowledgements

The author would like to acknowledge the work done by the designers of the 3D demonstrator chip, Gregory Deptuch, Jim Hoff, and Tom Zimmerman, who completed the entire design in just 3 months.

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Technology Scaling and CMOS Analog Design

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Abstract

Modern and future ultra-deep-submicron technologies make challenging the analog design especially when power consumption must match digital counterparts. The decrease of the supply voltage reduces the voltage headroom in analog circuits, the gate leakage current increases, the voltage gain decreases in planar bulk transistors, $1/f$ noise deteriorate when using new high-k gate dielectrics. The transistor and passive components mismatches give rise to large inaccuracies. Only some of these problems can be solved at the technology level; others require new circuit topologies and design techniques. The increased digital processing capability not only pushes the analog-digital interface toward more and more digital, thus limiting the analog design to very first interfaces and data converters, but also enables to use digital methods for the correction and digital assisted analog design. Several of the solutions currently proposed for analog pre-processing and data converter design are discussed in this paper.

I. Introduction

In past decades the well known Moore's law has governed the microelectronics evolution [1]. The constant pace of advancements in device and fabrication technology has lead to an exponential progress rates in transistor miniaturization and integration density. As shown in Fig. 1, the number of transistors per chip has increased by 4 order of magnitudes in three decades and very soon the technology progress will allow the integration of 1 billion transistors on a single chip.

The astonishing evolution started in *1958* when J. Kilby at Texas Instruments realized the first *IC* followed few months lather by a similar realization of R. Noyce at Fairchild. The first analog and digital planar products were quite simple like the ones shown in the microphotographs of Fig. 2. Presently, even not taking into consideration memories and pure digital circuits it is quite common to integrate on a single integrated circuit millions of transistors.

The *IC* complexity increases thanks to the technology scaling boosted by the continued improvements in optical projection lithography that enables printing ever finer features, the smallest feature size decreasing by about *30%* every two years. Process technology is now in sub-wavelength mode that with extreme Ultra-Violet (*EUV*) lithography (Fig. 3) obtains the patterning of lines below $50\,nm$ dimensions.

Actually, at the same time, we have a constant reduction of minimum feature size, oxide thickness, supply voltage and

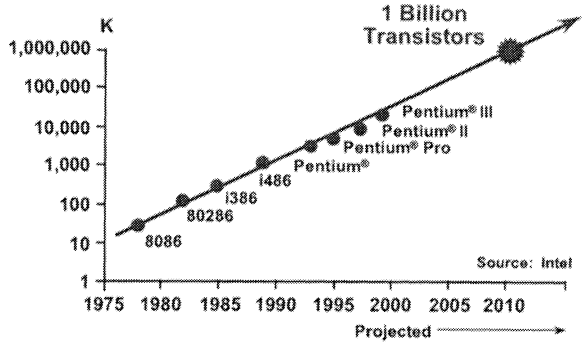

Fig. 1. Number of transistor per chip versus time.

transistor thresholds. The reasons are in the device physics of scaling the bulk *MOSFET* structures. Key challenges are controlling short channel effects like the V_{Th} roll-off and Drain-Induced Barrier Lowering (*DIBL*). Since for minimizing these short channel effects the planar and the lateral aspect ratios of transistors must be preserved, the technology evolution from one generation to the next should scale down all together gate oxide thickness, junction depth and depletion depth.

A major problem that limits the scaling of the oxide thickness is the leakage through the gate oxide by direct band-to-band tunneling. Indeed, if a not negligible current flows from source to drain of an *MOS* transistor highly energetic carries generate electron-hole pairs leading to charges trapped in the oxide. By a positive feedback mechanism the oxide tunneling current steadily increases in time until, eventually, the oxide breakdown occurs. Moreover, before the breakdown occurs the threshold voltage steadily degrades.

Supply voltage reduces each technology generation and contributes, on one hand, to lower the power dissipation but, on the

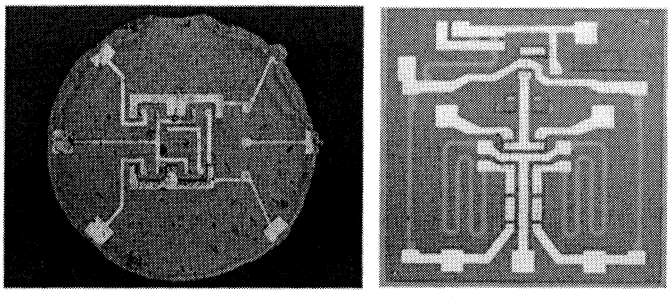

Fig. 2. First planar integrated flip-flop (Fairchaild, 1961) (left) and first analog integrated circuit (μA 702, Faichild -1962) (right).

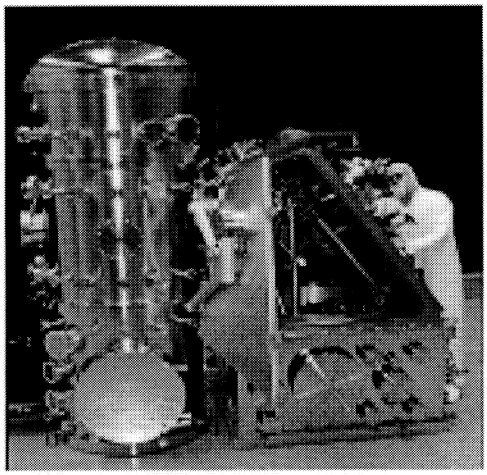

Fig. 3. Equipment for EUV.

other hand, worsens the signal-to-noise ratio (*SNR*) of analog circuits. As the supply voltage reduces the transistor threshold voltage should also reduce at the same rate to maintain enough gate overdrive without reducing the signal swing by more than the shrinking factor. However, lower threshold causes an exponential increase of the sub-threshold leakage that augments the leakage power and, more critical, dissolves the analog signals stored on capacitors. A possible remedy is using a dual threshold technology that reduces the leakage in high threshold devices by orders of magnitude but is much more expensive than the normal technology (one extra mask is required) and complicates the design and the layout routing.

The above points indicate that the push toward deep submicron technology is not so attractive for analog functions that, when implemented alone or with a small digital part, are more conveniently obtained with "analog" technologies whose line-width is *2–3* times larger than the one used for digital. The challenge (technical and cultural) for the analog designer is with large digital systems integrated in deep submicron technologies requiring limited analog functions.

II. Consequences of Scaling on Analog

The future evolution of *CMOS* technologies is predicted by companies and other organizations. According to them it is reasonable to assume that in the next *5–10* years the minimum line-width will go down to *35–25 nm* with equivalent oxide thickness as low as *1–1.5 nm*. If the gate oxide breakdown field will not increases properly, the values for V_{DD}, limited by reliability consideration, will drop well below 1 V [2]. Therefore, since designing high performance analog functions at this voltages is problematic, even for analog is important to find new replacements of silicon dioxide for increasing the maximum field strength and supply voltage.

In addition to the problems caused by a very low supply voltage there are other consequences on the transistor features that, by turns, limit the analog performance.

A. Transconductance

As known the transconductance is the key parameter for analog design whose desirable high value is typically obtained at the cost of an increased bias current. However, for very short channel the carrier velocity quickly reaches the saturation limit at which the transconductance also saturates becoming independent of gate length or bias

$$g_m = \frac{W_{eff} C_{ox} v_{sat}}{2} \tag{1}$$

Since for $T_{ox} = 1.5/, nm$ C_{ox} is about $16 fF/\mu^2$, assuming that v_{sat} of electrons at the oxide semiconductor interface is $3.2 \cdot 10^{10} \mu/s$, the transconductance of a transistor with $1\,\mu m$ effective width is at most $0.25\, mA/V$.

A limited transconductance is problematic for analog design: for obtaining high gain it is necessary to use wide transistors at the cost of an increased parasitic capacitances and, consequently, limitations in bandwidth and slew rate.

B. Output Resistance

The output resistance is another important analog parameter. It is influenced by channel length modulation, static feedback and, for deep submicron devices, the weakavalanche effect. The output resistance decreases quickly at gate lengths below $0.1 \mu m$ (much faster than L). Fig. 4 shows a possible plot of output resistance versus the effective submicron length.

The output resistance degradation and the saturation of g_m affect the intrinsic gain: using a transconductance limit of $0.25\, mA/V$ when the output resistance becomes $4\, k\Omega$ the intrinsic gain $g_m r_0$ becomes unity and the device cannot be used anymore for amplification purposes. Even using longer lenghts obtainig gain with deep submicron technologies is difficult: it is typically necessary using cascode structures with stack of transistors or circuits with positive feedback.

C. Diffusion and Gate Capacitances

Since with scaling the gate oxide becomes thinner, the specific capacitance C_{ox} increases as the shrinking factor. However, since the gate area decreases as the square of the shrinking factor, the gate-to-source and gate-to-drain parasitics lower as as the process feature size shrinks.

Reducing transistor parasitics is positive but the benefit is contrasted by the increased parasitic capacitance of the interconnections that compensates for the reduction of the

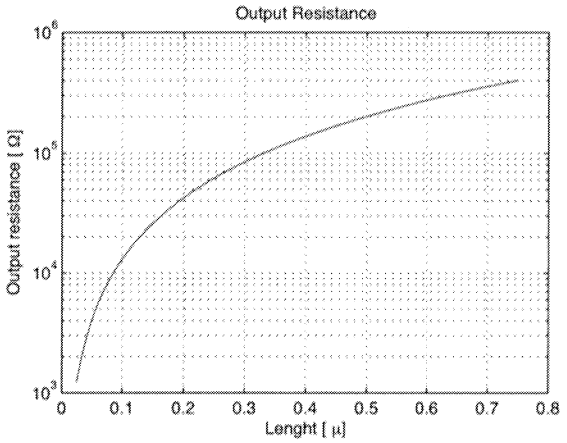

Fig. 4. Output resistance as a function of the effective gate lenght.

gate capacitance or perhaps brings about a larger parasitic contribution. The global effect is that shrinking does not help much in increasing the speed of analog circuit as the position of the non-dominant poles is almost unchanged.

D. Speed

The unity gain frequency of an *OTA* is approximated by $g_m/(2\pi C_L)$, where C_L is the load capacitance. Assume, for simplicity, that the fundamental kT/C limit establishes the value of the load capacitance and that the requires *SNR* is $62\,dB$. With a $0.5\,V$ input signal the noise power integrated over the Nyquist interval must be lower than $144\,\mu V$. Therefore, the value of C_L must be at least $0.2\,pF$.

The required transconductance for securing $f_T = 2\,GHz$ is $2.52\,mA/V$, a larger value than the saturation value of a $1\,\mu m$ wide transistor. Accordingly, the aspect ratio necessary for the input differential pair must be fairly large, in the hundred range.

E. Matching Accuracy

The offset of any analog circuit and the static accuracy of data converters critically depend on the matching between nominally identical devices. The stochastic nature of physical and chemical fabrication steps causes a random error in electrical parameters that gives rise to a time independent difference between equally designed elements. The error typically decreases as the area of the devices. It can be assumed that the stochastic mismatch between the parameters p_1 and p_2 of two elements placed at short distance is given by

$$\sigma(\Delta p)^2 = \frac{A_p^2}{W \cdot L} + S_p^2 d^2 \qquad (2)$$

where A_p and S_p are the process-dependent matching parameter at unity area (normally in μm^2) and unity distance between elements (normally in μm). d is the distance between the centroids of the two identically designed elements.

The value of various A_p and S_p depend on the process accuracy and the technology minimum line-width. Namely, the threshold mismatch parameter $A_{V_{th}}$ decreases almost linearly with the oxide thickness reduction, equal to the shrinking factor.

For capacitors, expressing the absolute accuracy by

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \epsilon_r}{\epsilon_r}\right)^2 + \left(\frac{\Delta A}{A}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 \qquad (3)$$

it can be assumed that the first term is negligible; the second term, inversely proportional to the area, improves with the accuracy of the perimetrical region whose definition enhances with scaling. The last term is almost constant and can be incorporated in the second term of equation (2). Summing up, A_C^2 decreases almost linearly with scaling.

The inaccuracy of integrated resistor depends on specific resistance and geometrical dimensions

$$\left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta R_\square}{R_\square}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 \qquad (4)$$

$\Delta R_\square$, that improves with the square root of area, depends on physical and technological parameters whose accuracy linearly improves $A_\square^2$ with shrinking. The other two terms are proportional to $1/\sqrt{A}$ and improve with scaling. Their effect becomes important for deep submicron technologies and give rise to an extra term in equation (2) inversely proportional to the perimeter.

Since at deep submicron the second term of (2) is negligible, for preserving matching the area of transistor or capacitor should diminish as the shrinking factor (and not as its square), while the area of resistors should diminishes less because of the perimetrical term.

F. Substrate and supply noise

In mixed signal applications the substrate noise and the interference between analog and digital supply voltages caused by the switching of digital sections are problematic. The situation becomes more and more critical with scaling as smaller geometries induce higher coupling. Moreover, higher speed and current density augment *EM* issues.

The use of sub-micron technologies with high resistive substrates is advantageous because the coupling from digital sections to regions where the analog circuits are located is partially blocked. However, the designer must face the bounce of the V_{DD} and V_{SS} digital lines which can have values up to hundreds of mV. The use of separate analog and digital supplies is a possible remedy but its effectiveness is limited by the internal coupling between close metal interconnections.

The substrate and the supply noise cause two main limits: the in-band tones produced by non linearities that mix high frequency spurs, and the reduction of the analog dynamic range required for accommodating the common-mode part of spurs. Since the substrate coupling is also a problem for pure digital circuit the submicron technologies is evolving toward *SOI* and trench isolation options.

G. Signal Swing

The continuous shrink of modern process reduces the supply voltage. Since it is necessary to ensure a suitable headroom for keeping transistors in saturation, even if the number of transistors piled up is kept at the minimum the swing of signals cannot be closer to V_{DD} or ground by more than one or two hundred mV. Therefore, the trend of *CMOS* features shown in Fig. 5 predicting supply voltages well below $1\,V$ in the next few

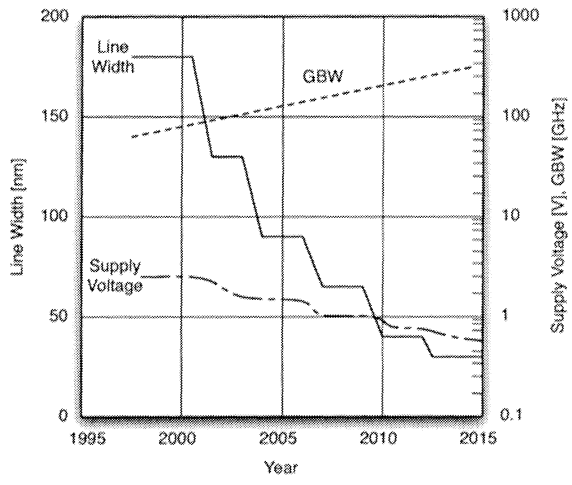

Fig. 5. Trend of analog features in CMOS technologies.

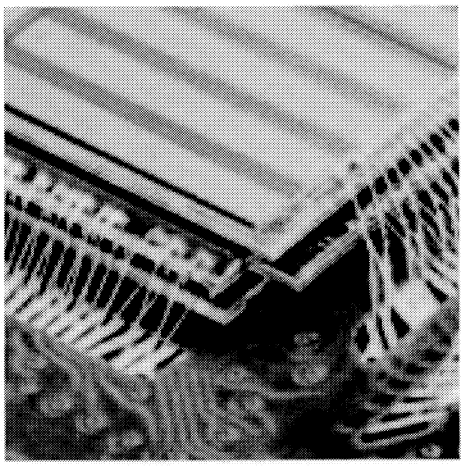

Fig. 6. Stack of chips.

years, also conceives a signal swing as small as few hundred of *mV*, fairly low if it is necessary ensuring a reasonable *SNR*. Low voltage is also problematic for driving *CMOS* switches especially for the ones connected to signal nodes as the on-resistance can become very high or at the limit the switch does not close at all in some interval of the input amplitude.

Different options and scenarios are possible. The most obvious solution is the multi-chip solution, with different circuits possibly assembled on the same package using, in some cases, a stack of chips (Fig. 6). Digital functions and memories are implemented by a single or multiple chips, the analog processing is obtained by a separate chip with suitably high supply voltage and reduced analog digital interference.

The use on the same chip of two supply voltages, one for analog and the other for digital, is another possibility. In some cases the higher voltages is generated on-chip with a charge pump. Obviously the technology or the transistors used in the analog part must be able to sustain the higher analog voltage. Moreover, it is necessary to design suitable analog-digital interfaces for the interactions between the two parts.

The already mentioned multiple threshold technology is another option. The use of a low or, at the limit zero, V_{Th} is good for many analog functions except the switching of voltage that needs medium V_{Th} devices for ensuring the *off* condition.

III. Circuit Design Techniques

Scaling-down the process certainly shifts the boundary digital/analog toward digital. However, analog circuits remain irreplaceable components. Besides the obvious data conversion, it will be always necessary to perform a variety of critical tasks before and after the analog-digital interface, such as amplification, prefiltering, demodulation, signal conditioning for transmission, generation of absolute values (voltages, currents, frequencies). In addition, analog will retain for a long while its advantage over digital when very high frequency and very low power consumption are required [3].

The key limitation of analog circuits is that they operate with electrical variables and not simply with discrete numbers that, in circuit implementations, gives rise to a beneficial noise margin. On the contrary, the accuracy of analog fundamentally relies on matching between components, low noise, offset, and low distortions. For deep submicron technologies the most challenging design issues are:

- Ensure good matching for low-offset and performant *ADC*.
- Obtain high *SNR* with low-voltage supplies.
- Contrast the degradation of analog performances caused by shrinking.

A. Matching of Elements

Since many circuit techniques exploit the equality of two components it is important for a given process obtaining the best matching especially for critical devices. Some of the rules that the designer must follow are common sense or obvious; nevertheless it is important to have them well in mind [4]:

- Devices to be matched should have the same structure and use the same materials.
- The temperature of matched components should be same. For chips consuming significant power the devices to be matched should be located on the same isotherm, which is obtained by a symmetrical placement with respect to the dissipative devices.
- The distance between matched devices should be minimum for having the maximum spatial correlation of fluctuating physical parameters.
- Common-centroid geometries like quad configuration used to implement a pair of transistors should be used to cancel the gradient of parameters at the first order.
- The same orientation of devices on chip should be the same to eliminate dissymmetries due to unisotropic fabrication steps, or to the unisotropy of the silicon itself.
- The surroundings in the layout, possibly improved by dummy structures, should be the same to avoid border mismatches.

Matching must be extended to the case of non-unity *n/m* ratios by separately grouping *m* and *n* matched devices. For ratios that are not a fraction of integer numbers a slight alteration of one of the unity devices for giving 1 plus the fractional part obtains the optimum solution.

B. Low-Voltage Design

A low-voltage supply can be augmented using a charge pump boosting on-chip voltages beyond the available supply; this relaxes the design but may lead to reliability problems in some cases. In addition a number of circuit techniques make possible true low-voltage operation without voltage boosting [5]; these include the use of transistors in the weak inverted region, the use

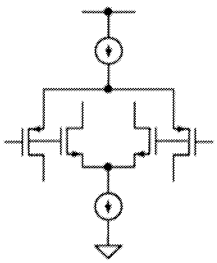

Fig. 7. Complementary differential pair.

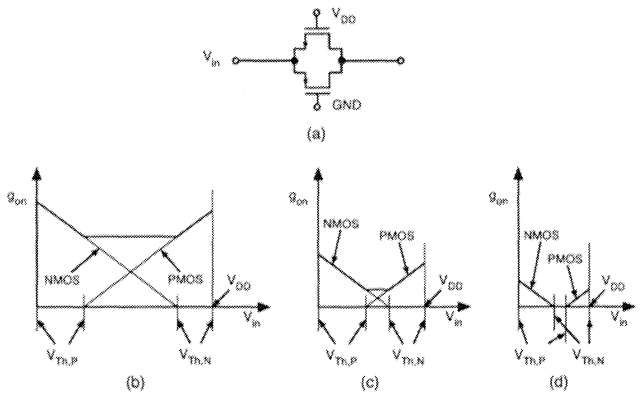

Fig. 8. a) Complementary switch and its on-conductance for scaling supply voltages (b), (c), and (d).

of the body node as a fourth control or signaling terminal, and the use of circuit topologies that eliminate stack of transistors.

For some circuits like the sample and hold the challenge is obtaining an input stage with a rail-to-rail common-mode voltage range. A solution is using complementary p-channel and n-channel parallel pairs (Fig. 7) with a control of the bias currents for extending the common mode input region with constant g_m. Thus, for example, a low-voltage *CMOS* op-amp can be fully-differental with an input stage made by the combination of n-channel and p-channel differential pairs for achieving a wide common-mode input voltage range, a differential output stage made by a low-voltage, class-*AB* rail-to-rail architecture with symmetrical output drive capabilities, and a switched-capacitor common mode feedback.

Sampled-data circuits use switches whose *on* condition is problematic at low voltage supply. Indeed, as shown in Fig. 8, the switch conductance can go to zero if the supply voltage is less than $V_{th,n} + V_{th,p}$. The problem can be resolved by using the switch boosting method and the switched op-amp technique. Fig. 9 shows the conceptual scheme of the switch boost [6]. During the phase at which the switch is off a capacitor C_B is pre-charged to the supply voltage; it is then connected during the complementary phase across source and gate of M_S for giving $V_{GS} \simeq V_{DD}$. The switched voltage should be lower than the supply. However, for special applications is also possible to switch voltages above the supply [7].

The switched op-amp technique is illustrated with the help of Fig. 10 that shows a flip-around $S\&H$. The left terminal of the sampling capacitance C_s is connected to the input during the sampling phase and also to output of the op-amp. During this phase the second push-pull stage of the op-amp is switched-off

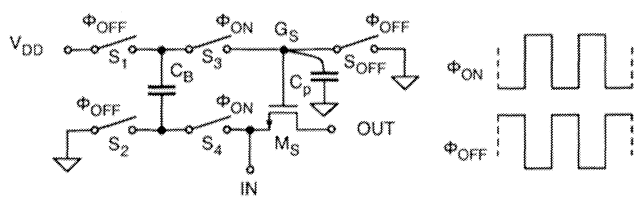

Fig. 9. Conceptual scheme of the switch boosting method.

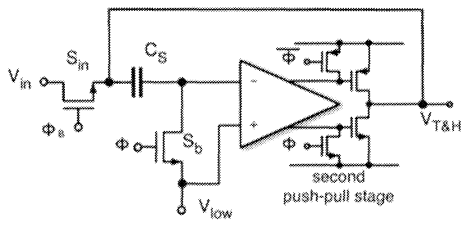

Fig. 10. Flip-aroud S&H with input common-mode voltage and switched OTA.

and becomes active only during the hold period. The switching *off* of the second stage can be obtained without boosting as the used transistors are connected to V_{DD} and ground.

C. Performance Enhancement and Tolerant Architectures

Poor analog performances that are caused by the use of a deep submicron technology are overcame by special analog techniques that, for example, foresee the storing of errors on capacitors afterward used for correcting the limit or by using architectures that are tolerant of analog limitations.

For example, the low gain of op-amps used in sigma-delta modulators is less critical than the first stages of a pipeline scheme. A continuous-time filter is less slew-rate demanding than a switched-capacitor counterpart. Therefore, the analog design trade-offs must include the limits that the deep submicron technology entails.

IV. Digital Assisted Techniques

The rapid advancement of digital technology motivates an increasing use of digital methods that improves the performance of analog circuits and data converters by correcting or calibrating the static and possibly the dynamic limitations.

Since the use of digital enhancing techniques reduces the need for expensive technologies with special fabrication steps, a side advantage is that the cost of parts is reduced while maintaining good yield, reliability and long-term stability. Indeed, the extra cost of digital processing is normally affordable as the use of submicron mixed signal technologies allows for efficient usage of silicon area even for relatively complex algorithms.

The methods are classified into the following categories:

- Digital correction.
- Foreground calibration.
- Background calibration.
- Dynamic matching.

A. Error Measurement and Correction

The basis of digital corection methods is in the measurement of errors. Accurate error measurement allows for their correction by trimming, or by the storing of errors for a successive digital correction or analog calibration.

Suppose, for example, it is required estimating the difference between capacitors that are expected to be equal [8]. Fig. 11 illustrates a two phase scheme for measuring the difference between C_1 and C_2. During Φ_s the capacitance C_1 samples the voltage V_B, and C_2 and the auxiliary capacitance C_3 are

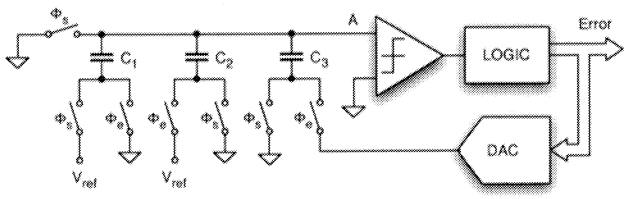

Fig. 11. Circuit for error measurement.

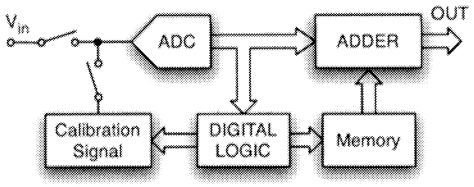

Fig. 12. Conceptual scheme of a foreground calibrated ADC.

connected to ground. During Φ_e the switching of the roles of C_1 and C_2, and a *DAC* output of zero give rise to a voltage at node A of

$$V_A = V_{ref}\frac{C_2 - C_1}{C_1 + C_2 + C_3} \tag{5}$$

which is proportional to the mismatch. Observe that the *DAC* and the logic form a successive approximation loop that through the action of C_3 can bring the error to zero. The *DAC* voltage at the end of N successive approximation cycles (the number of bits of the *DAC*) is

$$V_A = \frac{V_{ref}(C_2 - C_1) + (V_{DAC} + \epsilon_Q)C_3}{C_1 + C_2 + C_3} \tag{6}$$

where ϵ_Q is less than the *LSB* of the auxiliary *A/D* conversion.

If $\pm V_{ref}$ and $\Delta = V_{ref}/2^{(N-1)}$ are the references and the quantization step of the *DAC*, the range of measurement and its accuracy are

$$|(C_2 - C_1)|_{max} = \frac{V_{ref}}{V_B}C_3; \quad \Delta C_{mism} = \frac{\Delta}{V_B}C_3. \tag{7}$$

Assuming that $V_B \simeq V_{ref}$ the value of C_3 must be larger than the expected mismatch; the number of bits of the *DAC* gives the accuracy of the measure with C_3 as full scale.

The previous method aimed at obtaining a digital measure of an error that is to be accounted for in a digital correction section. Another possibility is using the measure for trimming. The method slightly changes the value of one or more elements to ensure the required analog accuracy. The trimming method was widely used in integrated filters to regulate the time constant of integrators or other parameters for ensuring an accurate frequency response. The use of metal thin-film resistors realized on the top of the passivation layer and a laser trim regulates the resistance values after fabrication, but before packaging. The method is expensive and does not account for temperature and aging effects.

Another form of trimming is to adjust a component value by discrete steps using fuses or anti-fuses that permanently open or close connections. Also, it is possible to use *MOS* switches whose *on* or *off* state is stored in a memory. When trimming with discrete steps it is obviously necessary to use an array of small elements, possibly binary weighted, connected in series or in parallel for connecting or disconnecting them according to a suitable control algorithm.

B. Foreground Calibration

The foreground calibration, typical of *ADC* [9], interrupts the normal operation of the converter for performing the trimming of elements or the mismatch measurement by a dedicated calibration cycle normally performed at power-on or during periods of inactivity of the circuit. Any miscalibration or sudden environmental changes such as power supply or temperature may make the measured errors invalid. Therefore, for devices that operate for long periods it is necessary to have periodic extra calibration cycles.

Fig. 12 shows the conceptual scheme of a foreground calibrated *ADC*. During the measure phase the input connection is disabled and a suitable input is applied to the *ADC*. It can be an analog linear ramp, a sine wave or pseudo-white noise, possibly generated by a slow and accurate on-chip *DAC* driven by an on-chip digital signal. In this case, since the signal is generated by the system itself, the method is called self-calibration.

Various types of inputs can be used to obtain the input-output characteristics and, in turn, the integral non-linearity (*INL*) error. How the differential inputs are generated, and how they are processed to produce the the *INL* are not discussed in detail here being sufficient to know that the calibration provides the *INL* to be stored in a memory. The input switch restores the data-converter to normal operational after the mismatch measurement and every conversion period the logic uses the output of the *ADC* to properly address the memory that contains the correction quantity. In order to optimize the memory size the stored data should be the minimum word-length which, obviously, depends on technology accuracy and expected *A/D* linearity.

The digital measure of errors, that allows for calibration by digital signal processing, can be at the element, block or entire converter level. The calibration parameters are stored in memories but, in contrast with the trimming case, the content of the memories is frequently used, as they are the input of the digital processor.

C. Background Calibration

Methods using background calibration work during the normal operation of the converter by using extra circuitry that functions all the time synchronously with the converter function. This makes the measurement hidden in the background and does not interfere with the normal converter operation.

Often these circuits use hardware redundancy to perform a background calibration on the fraction of the architecture that is not temporarily used. However, since the use of redundant hardware is effective but costs silicon area and power consumption, other methods aim at obtaining the functionality by borrowing a small fraction of the sampled-data circuit operation for performing the self-calibration.

For example, the method of Fig. 13, used for the on-line calibration of an *ADC* obtains the necessary room using a conversion rate higher than the sampling rate [10]. Assume, as

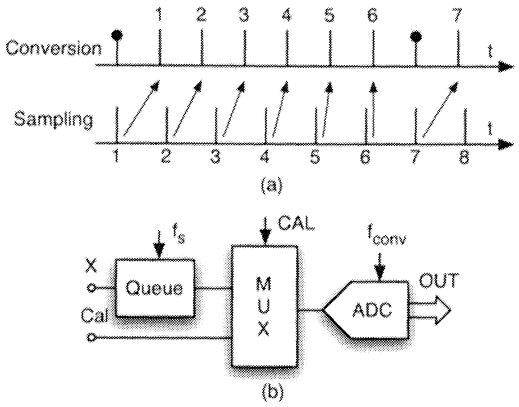

Fig. 13. (a) Timing scheme of a queue based background calibration. (b) Block diagram of a possible implementation.

shown in Fig. 13 (a) that the sampling and conversion frequency are such that $f_{conv} = 7f_s/6$. Therefore, the lower sampling frequency accommodates for 7 conversions in 6 sampling periods, thus making the converter available one extra slot every 7. The shift between sampling and conversion times is managed by a queue as shown in Fig. 13. The queue consists of one or more *S&Hs* used for storing the input sample between the sampling instant and the time of its conversion.

A method used in systems that use only a fraction of the available band consists in modulating the error and moving it at an out-of-band frequency [11]. A dedicated circuit performs the band-pass error measure and the possible trimming.

D. Dynamic Matching

The dynamic matching method is another possibility for calibrating unity elements. The goal of the approach is to equal the elements on average instead of performing a static correction of the values. As well as correcting the mismatch, the dynamic matching is also effective for canceling the variations caused by drifts like temperature changes and aging effects.

Consider just two nominally equal inter-changeable elements X_1 and X_2. Assuming $X_2 = X_1(1+\delta)$ and $X_1 + X_2 = 1$, the use of only one element gives rise to

$$Y_1 = \frac{1}{2+\delta} \quad or \quad Y_2 = \frac{1+\delta}{2+\delta} \tag{8}$$

depending whether the element X_1 or X_2 is used. The resulting errors are equal and opposite

$$\epsilon_{1,2} = \mp\frac{\delta}{2+\delta} \tag{9}$$

The dynamic averaging uses one or the other element under the control of a random bit-stream. Accordingly, the error is randomly positive or negative with spectrum given by the bit-stream control. The total power is approximately given by $\delta^2/[(2+\delta)^2 \cdot 12]$ and is almost uniformly spread over the Nyquist interval.

The method is described by using the scheme of Fig. 14 (a) where the current source I_{ref} is splitted into two nominally equal parts by the transistor pair $M_1 - M_2$. The degeneration resistances R_1 and R_2 improve the matching by attenuating the possible limit given by the thresholds mismatch. However, since the current divider is also limited by the resistor mismatch, the accuracy of the division is not enough for high resolution.

The four switches on the top of the current divider obtain the dynamic matching. They use a randomizing signal V_R similar to the one of Fig. 14 (b). To make the average of the output currents I_1 and I_2 equal it is required that the number of 1 equals the number of 0.

The method, illustrated for two elements, can be extended to many elements by using a proper algorithm for randomizing the selection pursuing the goal of transforming the mismatch error into a noise-like term [12]. If only a fraction of the Nyquist band is used a possible shaping of the noise-like spectrum further reduces the mismatch limit.

The control of the dynamic matching of many elements as used in *DACs* with a thermometric selection of unity elements can be problematic. Typically, equal resistors, capacitors or current sources, are summed up using a random representation of the thermometric input. The selection of the unity element is defined by the randomizer that receives N thermometric ones out of M input lines and generates a scrambled set of M controls, N of which are one and the others are zero. However, the number of possible scrambled outputs is $M!$ which is a very large number even for a relatively small number of levels: it is 5040 for $M = 7$, 40320 for $M = 8$ and more than 3.6 million for $M = 10$. Such a large number of connections is difficult to code but also are not strictly necessary for obtaining a random result.

What is actually necessary is avoiding frequent repetitions of the same or similar code which would produce tones and not noise-like spectra. Since it is enough to randomize the elements with a subset of possible connections, a very simple solution uses an M-port barrel shifter which rotates one increment after each clock. A more effective way is the butterfly randomizer shown in Fig. 15 consisting of a series of butterfly switches coupling inputs to outputs [13]. The use of $log_2 M$ butterfly stages, as done by the scheme of Fig. 15, ensures that any input can be connected to any output; adding more butterfly stages increases the number of possible connections. The control of the butterfly switches can be done using $log_2 M$ bits of a *k-bit RNG* (random number generator) ($k > log_2 M$). More simply the control can be done by successive divisions by 2 of the clock. In this case the method is called *clocked averaging*.

The randomization of elements transforms the mismatch error that produces tones in the output spectrum into a pseudo

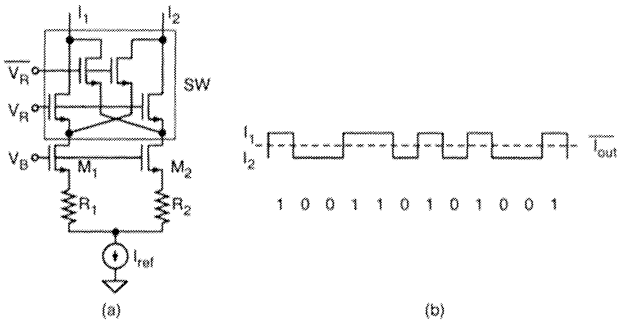

Fig. 14. (a) Current splitting and dynamic matching of the outputs. (b) Bit-stream control and I_1 current.

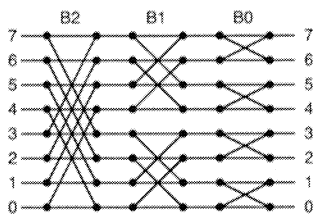

Fig. 15. Three stage butterfly randomizer of 8 elements with three bit control.

noise. Since the result smoothes the tones but does not achieve a reduction in the total error power, then for Nyquist rate data converters the signal plus distortion remains almost unchanged while the linearity improves.

For circuits that use a small fraction of the Nyquist interval it would be more effective having small the noise caused by the mismatch in the used band as the noise out of the band of interest can be removed by filters. This result is obtained by special dynamic matching schemes that achieve a low-pass shaping of the noise. The techniques, used in sigma-delta converters, are the individual level averaging (*ILA*) [14] and the data weighted averaging (*DWA*) [15]. The *ILA* approach aims at exercising each unity element with equal probability for each digital input code. The *DWA* performs a rotation of the elements used by using a starting index that is updated by the addition of the new input code to the content of the index register.

Both methods works well with busy input signals. The *ILA* is more effective for a small number of elements while the *DWA* method works well for 7 or more elements.

V. Conclusions

The design of analog functions using deep submicron technologies is source of new challenges that are faced with different approaches: solving the problem at the circuit level using at the best the analog feature of the technology and staying away from the minimum feature sizes, studying architectures that are tolerant to analog limits, and, more effective, exploiting the increasing digital processing capabilities and use digital circuits to assist the analog performances. Indeed, digitally assisted analog circuits avoid the disadvantages of technology scaling by delegating matching requirements to a digital processor and compensating for non idealities. The relaxed analog circuit constraints translate into higher overall system performance such as higher resolution and better circuit speed.

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Plenary Session 5

LHC experiment electronic upgrades

Informal comments on SLHC machine issues

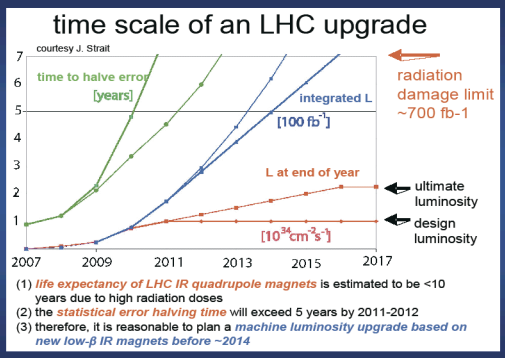
Andy BUTTERWORTH

CERN

Informal comments on LHC upgrade: Impact of reduced bunch spacing

Andy Butterworth AB/RF

time scale of an LHC upgrade



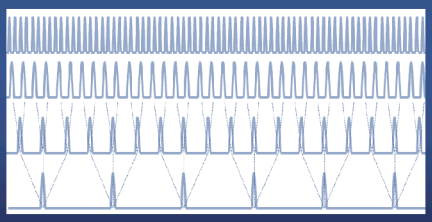
(1) *life expectancy of LHC IR quadrupole magnets* is estimated to be <10 years due to high radiation doses
(2) the *statistical error halving time* will exceed 5 years by 2011-2012
(3) therefore, it is reasonable to plan a *machine luminosity upgrade based on new low-β IR magnets before ~2014*

Upgrade phases

- Phase 0: Maximum performance without hardware changes
- Phase 1: Maximum performance with hardware changes in insertions and injector complex
  - IR magnets & layout
  - Crossing angle
  - Protons per bunch N_b up to ultimate intensity
  - High harmonic RF system 1200MHz → bunch shortening
  - Double number of bunches
- Phase 2: Maximum performance with major hardware changes (HPS, SC PS etc.)

Current scheme

- 6 PS Booster bunches → PS
- Successive bunch splittings in PS → 72 LHC bunches
- Bunches with 25ns spacing captured on 40MHz (h=84)
- 80Mhz used for bunch length compression



n_b	h	f(MHz)
72	84	40
36	42	20
18	21	
6	7	

Current scheme

- SPS 200MHz → 450 GeV
- Injected into LHC on 400MHz or 200 MHz capture RF (for ultimate intensity beam)

Closer bunches

- All RF manipulations asumed to be done in the PS
- 12.5 ns spacing: 12.5 ns is not a whole number of 200 MHz RF periods
  - PS: one more splitting to be done, needs more RF voltage at 80 MHz for bunch length
  - SPS: 200 MHz no longer works, so need a new RF system (160 or 240 MHz)
  - LHC: need a new capture RF system in LHC (200 MHz no longer works)
- 10 ns spacing:
  - no changes in SPS
  - new RF system in PS (95.4 – 100 MHz)
- 15 ns spacing:
  - no changes in SPS
  - new RF system in PS (63.5 – 66.7 MHz)

Closer bunches – other issues

- **Beam brilliance (Brilliance = N_b/ε_n)**
  - Ultimate intensity requires increase of beam brilliance in the PSB by 1.7 (brilliance = N_b/ε_n)
  - Reduced bunch spacing requires increase of brilliance in PSB by a similar factor
  - Various schemes to increase brilliance (batch compression in PS, LINAC4 160 MeV → PSB)
- **In the SPS more problems with e-cloud (V-emittance blow-up) and coupled bunch instabilities.**
- **Beam loading in SPS RF 200 MHz and 800 MHz systems**
  - tests with high power pulsing over ⅓ ring
  - upgrade of power plant and couplers

RF upgrades and tentative cost for different LHC bunch spacings

(F. Ruggiero, LHC-LUMI-05 – Session 2: High Intensity Effects)

- 12.5 ns
  - **PS: double RF voltage at 80 MHz ~ 2 MSfr**
  - **SPS: more RF power and new RF cavities at 160 or 240 MHz ~ 75 MSfr**
    new Faraday cage and infrastructure ~ ?
  - **LHC: new capture cavities at 160 or 240 MHz (2x3 MV) ~ 5 MSfr**
    new BPM electronics (MSfr + manpower + time)

    TOTAL (12.5 ns) > 82 MSfr
- 10 or 15 ns
  - **PS: new RF system at 66 or 100 MHz ~ 5 MSfr**
  - **SPS: double RF power at 200 MHz + new couplers ~ 20 MSfr**
  - **LHC: no new capture cavities**

    TOTAL (10 or 15 ns) ~ 25 MSfr
- **Any bunch spacing shorter than 25 ns requires new electronics for the LHC BPM system, upgraded transverse feedback, collimation, cryogenics, beam dump, …**

DC to DC Power Conversion

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Abstract

We present results from a capacitor charge pump DC-DC converter prototype using 0.35um HV-CMOS technology fabricated in April 2006. The purpose of this prototype is to test the switch technology both for achievable efficiency and for radiation tolerance. The IC of this test device contains only switches, with all clocks being externally supplied and driven and the capacitors also external. The configuration used is a 4 capacitor stack producing a nominal x4 input current multiplication factor. The goal for this type of device is to be of low enough mass and high enough radiation tolerance to be placed on individual modules in the innermost layers of the Atlas collider detector. Irradiation results will be presented if available. A prototype test card for use with a silicon strip stave prototype is under development.

I. Introduction

This paper describes the progress in our program to develop a switched capacitor DC to DC power conversion module to decrease the amount of current which must be supplied to the ATLAS inner tracker. Over the last two decades the density of silicon tracker modules has increased in each new detector and the proposed upgrades for the LHC detector continue this trend. At the same time the reduction in feature size of the ASICs used in the front end electronics has resulted in lower power supply voltages. The ABCD chip used in the ATLAS SLT tracker uses a 3.3 volt power supply and the proposed upgrade for the pixel detector will use a 1.3 volt power supply [1]. These factors have conspired to increase the current in the power supply busses to the point that the mass of the cables required to transport the power is a determent to the detector. Fig. 1 shows the pixel detector radiation length as a function of pseudorapidity. The green and yellow areas are dominated by power cables. Fig. 2 shows the estimated voltage drop in the cables supplying 2 volts to the pixel detector. Clearly, only 25% of the power is delivered to the detector. Also shown is the corresponding line for a module with a 4:1 power converter that would deliver 62% of the power to the detector and reduce the mass of the supply lines by a factor of 4.

There are two other programs to attack this problem underway. (1) Groups at Bonn and Rutherford Appleton Laboratory have connected up to six modules in series with appropriate shunt regulators to 'reuse' the current [2]. Their work has been reported at the 2006 Hiroshima conference at Santa Cruz. (2) Satish Dhawan at Yale has a contribution to this conference describing a 'buck' regulator to accomplish DC to DC conversion.

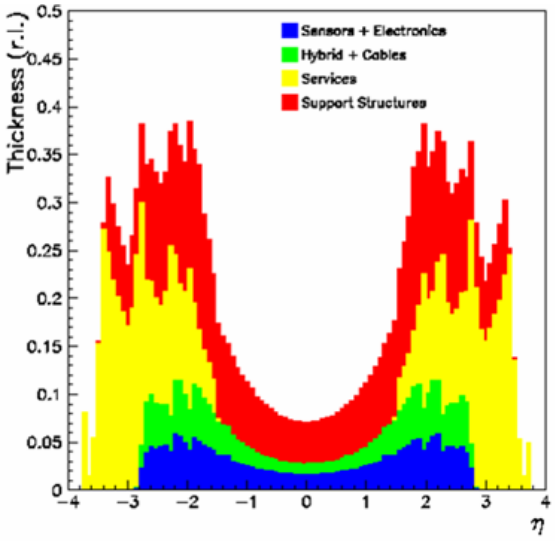


Figure 1: Radiation thickness of ATLAS pixel detector vs. pseudorapidity.

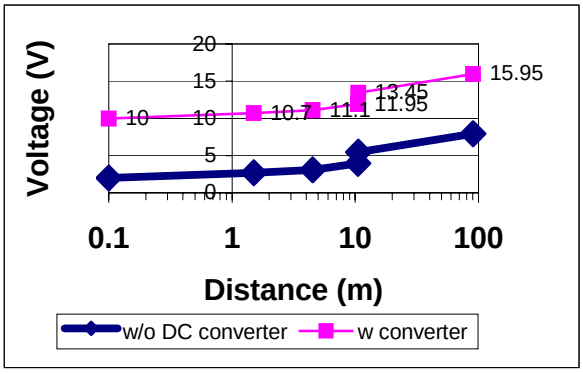


Figure 2: Voltage vs distance from pixel detector on proposed pixel power line.

II. Switched Capacitor Options

Switched capacitor circuits are used frequently in industry to step up voltage for displays, a low current application, however devices which step down are rare, mostly divide by two and are not radiation hard at the level required by LHC inner detectors.

There are many circuit topologies that accomplish the same task. They vary by the number of transistors, the number of capacitors and the maximum voltage swings incurred during the operation. M. Makowski and D. Maksimovic [3] have analyzed the general problem. We have selected the circuit shown in Fig. 3 for prototyping because it is efficient in the sense that the charge accumulated in the charging half-cycle is transferred to the output node in the

following half-cycle and because the capacitors, in normal operation, have the lowest potential.

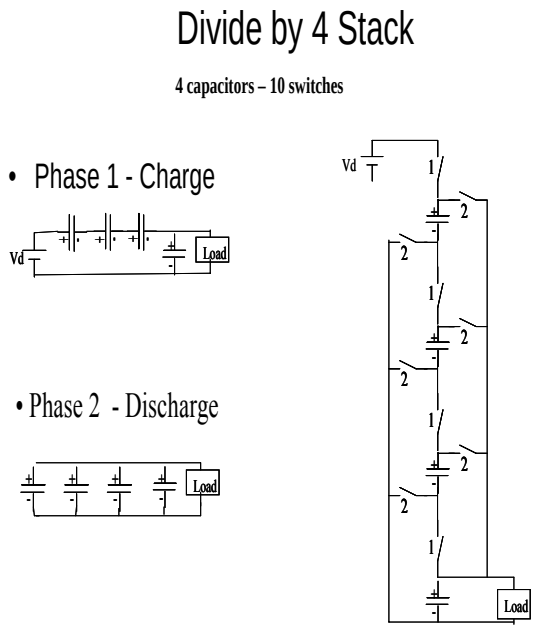


Figure 3: A divide by four switched capacitor circuit.

In order to achieve the desired level of radiation hardness, the cmos switches have to be fabricated in a submicron technology with a thin (<10nm) gate oxide but the maximum drain-source voltage in normal processes is less than five volts. We have designed our first prototype using a commercial high voltage process (H35) that uses an extended drain structure that will hold off up to 50 volts, has a 0.35 micron minimum feature size and has a 9nm gate oxide. Table 1 is a partial list of the transistors available in this including the transistors used in our prototype.

Table 1: H35 process transistors

Device Name	Min. L(μ)	Max. Vgs(v)	Max Vds(v)	On Res. L = min W= 50mm	Cg (pf)
NMOSI	0.5	3.6	3.6	0.06	125
NMOS50T	0.5	3.6	50	0.54	364
PMOS50T	1.0	3.6	50	0.73	369

The NMOSI transistor is not a high voltage transistor but it is isolated in a triple well whose potential can be moved from ground to the input potential (Vdd). It has a significantly smaller 'on' resistance.

III. Circuit Simulation

The circuit in Fig. 3 has been simulated with Iout = 1 amp using the design kit provided by the foundry. To keep the total mass small, the switched capacitors have a value of 0.2 uf. The output capacitor is chosen to be 4.7 uf to reduce the ripple.

The figures of merit that we use to judge the circuit are:

- Voltage efficiency – $\varepsilon_V = 4*Vout/Vin$
  - Vout is a function of the load, Vout = Vin/n for no load
- Current efficiency – $\varepsilon_I = Iout/4*Iin$
  - Charge is lost charging the gate capacitance of the switches
- Power efficiency - $\varepsilon_P = \varepsilon_V * \varepsilon_I$

Fig. 4 shows the power efficiency vs transistor width (with minimum length) for three frequencies and Fig. 5 shows the voltage and current efficiency as a function of period for transistors with the optimum width.

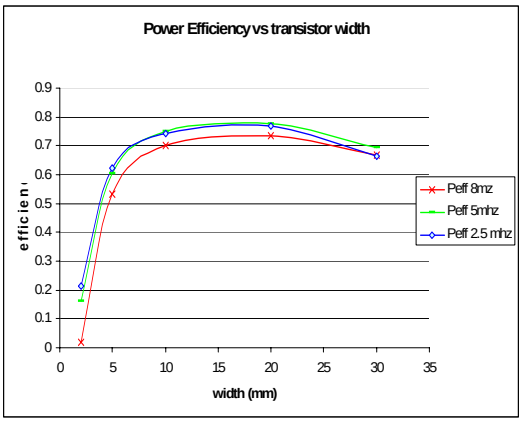


Figure 4: Power efficiency vs transistor width for clock frequencies of 8 Mhz, 5 Mhz and 2.5 Mhz.

At a operating frequency of 5 Mhz the maximum voltage effiency is 82% and the maximum current efficiency is 92%. The ripple was 1.2% and the output impedance is 0.25 ohms. A final circuit must include a clock generator and probably a post regulator which will reduce the efficiency by at least 10%.

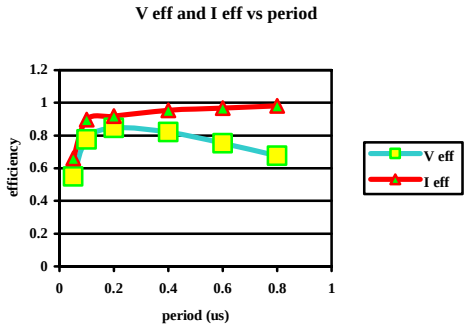


Figure 5: Voltage efficiency and current efficiency vs period.

IV. DC2DC_0 Prototype

We are preparing a fully functional design for submission next year. In the meantime we were able to submit a test chip, DC2DC_0, for a divide by four stack sized to supply 0.25 amps. The purpose was to test the concept, characterize the transistors and test the radiation hardness of the transistors. The circuit is shown in fig. 6.

Fig. 7 shows Vout vs Vdd for output loads of 10 ohms and 100 ohms. Unfortunately the ratio of the input current to the

output current is approximately one due ta parasitic transistor in the MODNI transistors during the discharge cycle. This feature is known to the present design kit but was announced after our submission. This problem can be fixed in the next submission by adding bulk bias control to the triple well transistors.

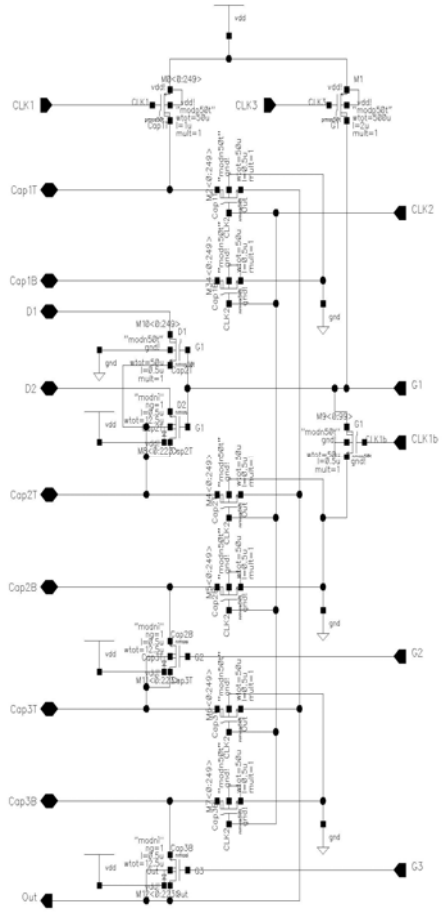


Figure 6: DC2DC_0 circuit diagram

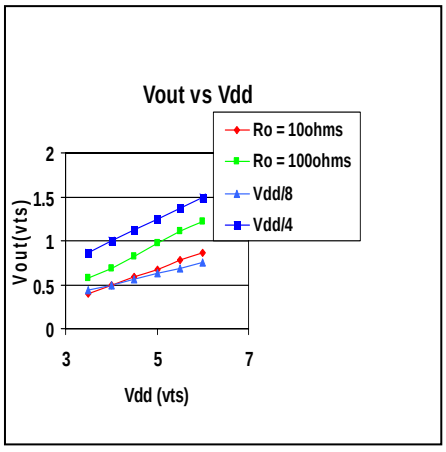


Figure 7: Vout vs Vdd for DC2DC_0 configured as a divide by four stack.

Each of the transistor types have been characterized using an Agilent 4156C and the results were compared with the models supplied by AMS for both hspice and eldo. Fig. 8 shows two curves for the NMOS50T. In general the models for the n channel devices compare poorly. In particular the 'on' resistance of the switches, the rds at low vds, is nearly 40% greater than the models predict. This will lead to larger transistors in the final design.

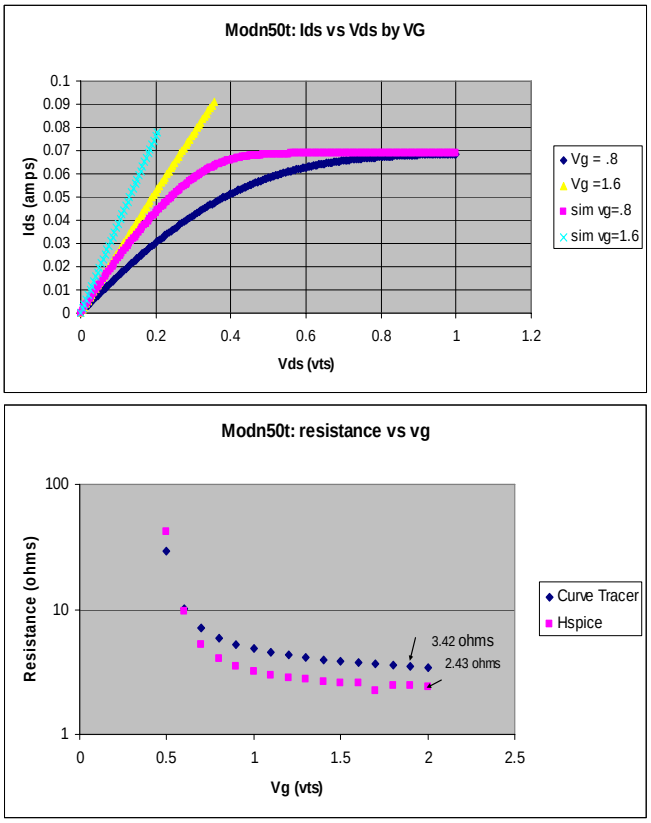


Figure 8: Comparison of (a) the measured and simulated I-V curves for a nmos50t (Modn50t) and (b) the resistance (rds at low vds) vs Vg.

V. Radiation Tests

After the conference we exposed one chip to the 55 Mev proton beam at the 88" cyclotron at LBNL. A beam current of 30 na was focused to approximately 1 cm in diameter and, over a period of about 4 hours, the delivered dose was about 70 Mrad. Three transistors, a nmosi, a nmos50t and a pmos50t, were powered with a Vdd of 4 vts in a diode configuration and the gates (and drains) were clocked at 1 Khz to about 0.8 vts. The results are still being analyzed but in general all transistors seem to have survived with threshold shifts of less than 0.2 volts. The transistors were characterized after the radiation and figures 9a and 9b show the before and after IV curves for the nmos50t. The most important result affecting the circuit is that the rds has increased by about 10%. . The tests were conducted at room temperature and the chip was not refrigerated after the test.

The leakage current during the off state of the switches was monitored during the run and for five days after the run. The currents started in the nanoamp range and quickly increased to a maximum of 4 microamps. Two days after the run all of the leakage currents had decreased to less than 0.6 microamps and they remained steady for the next three days.

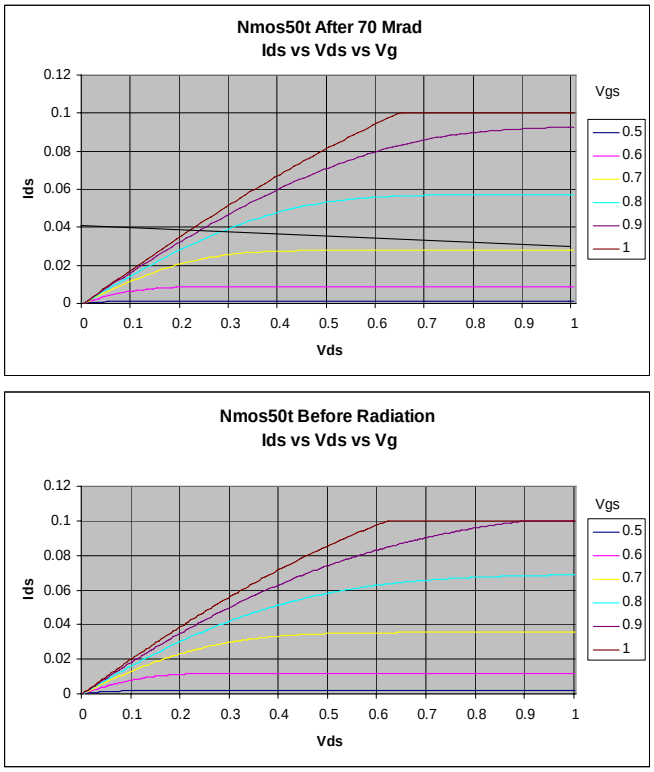


Figure 9: Characteristic curves for a nmos50t transistor before and after radiation with 55 Mev protons to a dose of 70 megarads.

VI. Conclusions

We have tested a prototype switched capacitor DC to DC converter fabricated with a commercial CMOS 0.35 micron high voltage process (H35). The resistance of the switches falls within the parameter variations of the process but is 40% greater than the models predict. The chip was exposed to a 55 Mev proton beam to a dose of 70 Mrad and the transistors survived with threshold shifts of less than 0.1 vt.

The next generation of this chip is being designed to supply one ampere. It will have internal clock generation, bulk bias control and post regulation. We plan to submit it for fabrication in February 2007.

VII. References

[1] F. Campabadal et al., “Design and performance of the ABCD3TA ASIC for readout of silicon strip detectors in the ATLAS semiconductor tracker,” Nucl. Instrum. Meth. A552: 292-328, 2005

[2] “Sixth International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors,” Carmel Mission Inn, California September 11-15, 2006

[3] M. Makowski, D. Maksimovic, "Performance limits of switchedcapacitor DC-DC converters," IEEE PESC, 1995 Record, pp. 12151221

The GBT Bi-directional Link and Data system

Paulo MOREIRA

CERN

A Versatile Bi-Directional Link System

A. Marchioro, P. Moreira, G. Papotti and A. Raposo
CERN PH-MIC

12th Workshop on Electronics for
LHC and Future Experiments
25-29 September 2006, Valencia SPAIN

Outline

- Links in HEP
  - Is a different approach viable?
- A Versatile Bi-Directional Link System
  - The concept
  - The GBT ASIC
  - Link configurations
  - Bandwidth
  - Handling SEUs
- The GBT as a "Communications Controller"
- Prototypes
- Summary

Links in HEP

- Data transmission roles in HEP:
  - Data Acquisition (DAQ)
  - Timing, Trigger (TT)
  - Experiment Control (EC)
- LHC Era:
  - A different architecture for each function
  - A dedicated physical support for each architecture
  - Experiments shared some common developments:
    - TTC system
    - GOL
  - But a lot of effort went in developing several similar systems for each of the four LHC experiments!

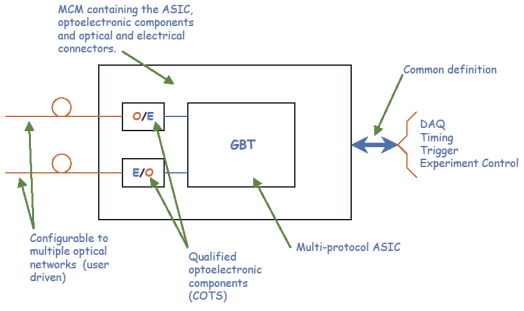
Future HEP Links

- Can we develop a one-size fit-all solution?
  - Same support hardware?
  - Same link architecture?
- An "universal" link requires:
  - The experiments to agree on a common interface!
  - A well defined set of specifications (requirements):
    - DAQ
    - TT
    - EC
    - ASIC
    - OPTOELECTRONICS
- The system has to be Versatile:
  - It has to accommodate several topologies
  - But the physical support can be "shared"
    - Same electronics (ASIC)
    - A limited set of optoelectronics 'flavours'
    - Same MCM

Versatile Bi-Directional Link System

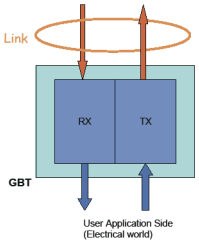
- The objective is to build a system based on a single ASIC which can provide a complete link solution for:
  - Timing
  - Trigger
  - Experiment Control
  - Data Transmission
- What's the target:
  - Implement versatile link topologies
  - Higher bandwidth
    - Data, Timing, Trigger and Experiment Control
  - Bi-directional links
    - Data, Timing, Trigger and Experiment Control
  - Robust handling of irradiation effects
    - Total dose
    - SEU
  - Common development
    - Better use of human/economical resources

Transceiver Module



GBT

- Such a Versatile system requires:
  - Multi-protocol transceiver:
    - 1-to-1
    - 1-to-N
    - N-to-1
- Operation modes:
  - Trigger:
    - TTC functions
  - Link
    - General purpose
    - Simplex/Duplex
- Data transmission modes:
  - Continuous
    - Data is continuously transmitted
  - Packet
    - Data is transmitted in bursts of packets

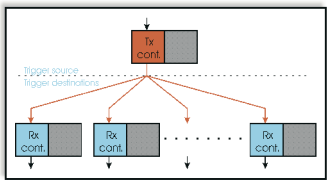


GBT Operation Modes

- Continuous mode (think about a traditional optical link):
  - Each link is 100 % occupied by a single transmitter.
  - The transmitter/receiver pairs are fully synchronous
  - This is the case for:
    - A trigger source sending data to several trigger destinations
    - Synchronous point-to-point data link
- Packet mode (think about a backplane bus):
  - Common Transmission medium is shared:
    - A transmitter can only send data upon the request of a master transmitter
  - Several devices can share the same medium and thus communicate with the same destination without collisions
  - This is the case for:
    - Trigger return link (bus)
    - Asynchronous point-to-point data link

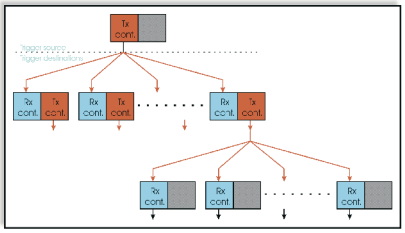
Link Configuration 1: Broadcast Network

- Down-path: Passive Optical Tree
  - Current TTC system architecture
  - One source to N destinations
  - For large N, an high optical power source is required
  - Operation mode: continuous



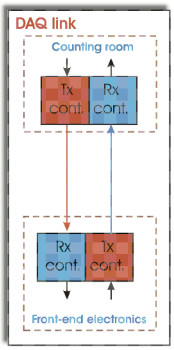
Link Configuration 2: Broadcast Network with O/E/O Repeaters

- Down-path: Passive/Active Tree
  - Passive power splitting with electrical regeneration
  - One source to N destinations
  - Optical or electrical: 1-to-16
    - Moderate optical power at each transmitter
  - Operation mode: continuous
  - Moderate increase in latency: o/e-r-e/o



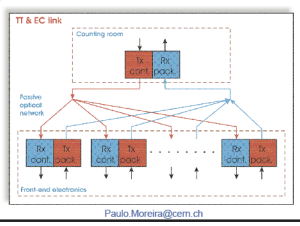
Link Configuration 3: Point-to-Point

- Up/Down-paths: Optical
  - Full bandwidth available for data transmission
  - Simplex/Duplex operation
  - Operation mode: continuous



Link Configuration 4: Bidirectional One-to-N / N-to-One

- Down/up-links: Passive Optical Trees
  - Passive optical tree in both directions
  - Down-link: 1-to-16
  - Fan-In-Out: 16-to-1
    - For moderate power optical source
  - Operation mode:
    - Down-link: continuous
    - Up-link: packet
    - Up-link under control of the master transmitter



Data Rate and User Bandwidth

- Data rate and word size will depend on the SLHC frequency
  - Still not decided!
  - Numbers below assume $f_{SLHC} = M \times f_{LHC}$ (not necessarily true)
- Transmission data rates must be multiples of the (S)LHC bunch crossing frequency:
  - Trigger system remains synchronous with the accelerator cycles
  - Fixed latency communication channels
  - 130 nm CMOS technology:
    - Raw 3.2 Gbit/s OK, (~5 Gbit/s maybe feasible)
    - Transmission of 88-bits encoded at 40 MHz (the LHC rate)
    - Effective data bandwidth of 2.56 Gbit/s (for 3.2 Gbit/s raw)
  - 90 nm CMOS technology:
    - Raw 6.4 Gbit/s OK, (~10 Gbit/s maybe feasible)
    - Transmission of 128-bits properly encoded at 40 MHz (the LHC rate)
    - ... or transmission of 64-bits encoded at 80 MHz (the SLHC+ rate)
    - Effective data bandwidth of 5.12 Gbit/s (for 6.4 Gbit/s raw)

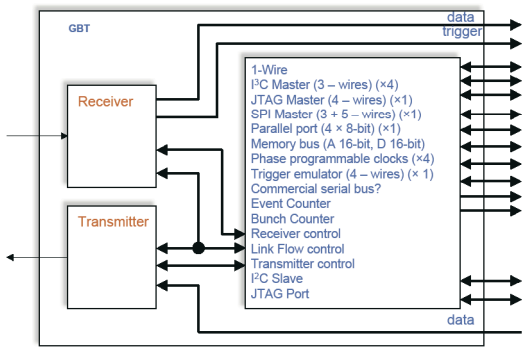
Line Codes and Error Correction

- High SEU rates are expected for SLHC
- SEU errors at the optical receiver (PIN-Preamp) will be detected as corrupted data bits
- Traditional Error Coding followed by Line Coding will not work!
  - The order of operations must be reversed
- To deal with higher SEU rates in SLHC the following scheme is proposed (illustrative example only):
  - 64-bit data is first scrambled for DC balance
  - The scrambled data is Reed-Solomon encoded: 16-Bit FEC field
  - An 8-bit redundant header is added to form a frame
  - This results in an 88-bit frame.
    - Line rate → 40 MHz × 88-bit = 3.52 Mbit/s
  - To minimize the dead-time due to a loss of synchronization the scrambler is designed as self synchronizing:
    - One LHC clock cycle is enough to synchronize the scrambler
  - The efficiency of the line encoding is: 64/88 = 72.7 %

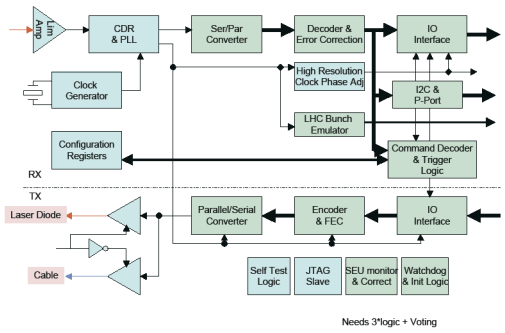
(Further details were given by Giulia Papotti this morning)



The GBT as a TTC and Communications Controller



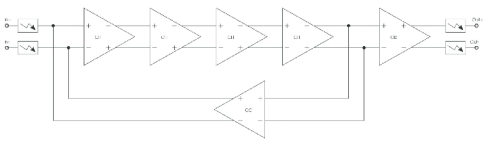
GBT Block Diagram



Prototypes

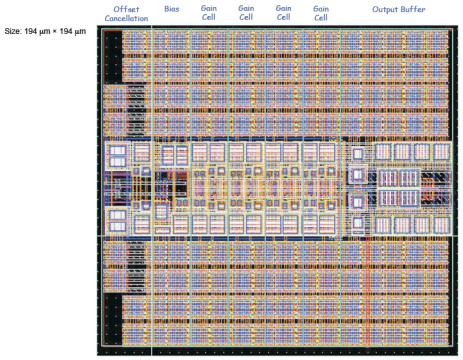
- Three GBT building blocks were prototyped in 130 nm CMOS:
  - Laser driver (Gianni Mazza, INFN Torino)
  - Encoder / decoder (Giulia Papotti, CERN) (Presented this morning)
  - Limiting Amplifier (Paulo Moreira, CERN)

Limiting Amplifier

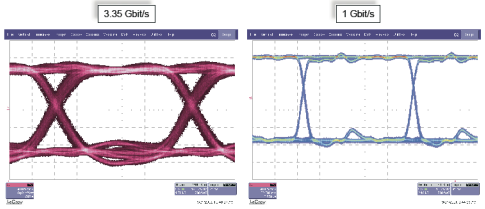


Specifications:
- Data rate: 3.60 Gbit/s
- Gain: > 55 dB
- Bandwidth > 2.52 GHz
- Equivalent input noise: < 1 mV
- Minimum input signal (differential): 10 mV
- Maximum input signal (differential): 600 mV

Limiting Amplifier



Limiting Amplifier



Summary

- We propose a Versatile Link solution for:
  - Timing Trigger Links;
  - Data Acquisition Links;
  - Experiment Control Links.
- The system allows flexible link topologies:
  - Bi-directional
  - Uni-directional
  - Point-to-Point
  - Point-to-Multipoint
- Specifications and Interfaces are still evolving for which we **need** the feedback of the potential users
- Some universal building blocks have already been prototyped:
  - Laser driver
  - Encoder/decoder: Line code and FEC
  - Limiting amplifier
- The Versatile Bi-Directional Link project has been proposed by the Microelectronics group as a CERN common development.

Future options for optical links

François VASEY

CERN

Options for Optical Links at SLHC

Francois Vasey, CERN/PH-MIC
with input from ATLAS and CMS colleagues

- Margins of existing ATLAS and CMS TK OL
- Options for OL upgrades
- Some proposals
- The joint optoelectronics working group
- Conclusion

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Optical Links for the ATLAS and CMS Trackers

ATLAS

Digital links
(40/80Mb/s)

17.5k Channels
VCSEL 850nm MM

CMS

Analogue readout links
(40MS/s, 8bits)

Digital control links
(80 Mb/s)

40k+ 3k Channels
EELaser 1310nm SM

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The Optical Link Margins (1: Tx)

- Tx Radiation Hardness
  - Operating point shifts
  - Thermal management becomes crucial
    - Thermal resistance
    - Annealing
  - Compliance voltage

Results – Threshold Shift (After-Before)

Preliminary

BEFORE annealing

Optical Output Power [W]

Input Current [mA]

Threshold Is [mA]

Slope Efficiency [W/mA]

Eff of LD1

LHC 1.0 2.0 3.0 4.0

Fluence [10^{14}n/cm^2] 20MeV

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The Optical Link Margins (2: Rx total)

- Rx Radiation Hardness
  - Leakage current damage definitely appears to be 'saturating'
  - Responsivity going to zero
  - No significant annealing
  - Ultimate limit reached

PIN responsivity I(t)/I(0)

av. current/2min

Fluence

Cernonix

Truelight

Time (sec)

Fluence (200 MeV) p/cm^2 E14

leakage current (A)

fluence (10^{14}n/cm^2)

annealing time (hrs)

photocurrent at 100uW (uA)

LHC

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Optical Link Margins (3: Rx SEE)

- Rx SEE cross-section
  - Bit rate dependent
  - Incidence-angle dependent

300MeV/c π^+
350MeV/c π^+
405MeV/c π^+
405MeV/c p

bit-error cross-section (cm^2)

59MeV protons

signal amplitude (dBm)

Figure 5: Cross-section measured with 59MeV protons for various incident angles.

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Optical Link Margins (4: fiber)

- Fiber Radiation Hardness
  - (0.05-0.1dB/m)
  - To be reconfirmed

Dose Rate during radiation = 4 kGy/h

Loss (dB/m)

Dose (Mrad)

Dose Rate: 720Gy/hr

Induced Loss (dB/m)

Dose (kGy)

Corning
Siecor
OF Spool 1
OF Spool 2
OF Spool 3
Sumitomo PSC
Fujikura
Plasma
Lycom
TrueWave

Unrecovered loss fraction

Recovery Time (hrs)

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Optical Link Margins (5: link)

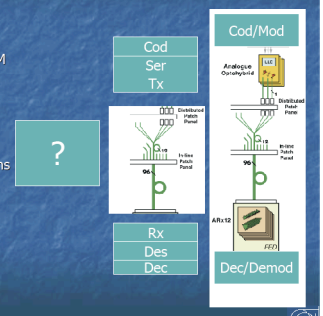
- Fiber Capacity
  - ATLAS SIMM: 50-80 MHz·km
  - ATLAS GRIN: 1000 MHz·km
  - CMS SISM: >>10GHz·km
- Electronics
  - Binary 40/80MBps
  - Analogue 100MHz
  - Digital 80MBps
- Geometry
  - 18cm from beam axis
  - 20cm from beam axis

Margins for operation at SLHC (6: summary)

- Tx and Rx need careful study
  - Are we reaching the limit?
  - Rx SEE sensitivity to be mitigated
- Fiber
  - Radiation tolerance probably OK
  - Capacity increase OK in SM, NOT OK in SIMM, OK in GRIN
- Electronics
  - Generalized Bottleneck
- Geometry
  - Possibility to move away from beam axis to gain margin against radiation damage
- Good overall agreement between ATLAS and CMS observations

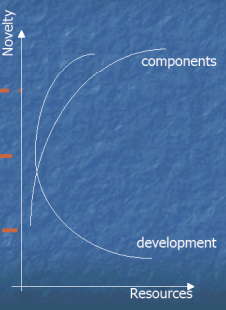
The Options for an Upgrade (1)

- Reuse the existing system
  - Check margins carefully
  - Boost analog link capacity by developing CODEC and MODEM
    - See paper by S. Dris
- Reuse the fiber plant only
  - Develop TRx, SERDES and CODEC
    - See paper by P. Moreira
  - Check compatibility and margins of legacy fiber and connectors
- Start from scratch
  - Possibly using components identical to existing ones
- A combination of the above
  - Geometry dependent system implementation



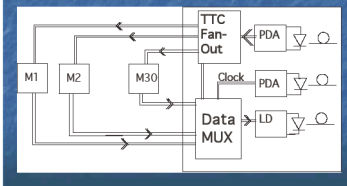
The Options for an Upgrade (2)

- Start from scratch
- Reuse the fiber plant only
- Reuse the existing system



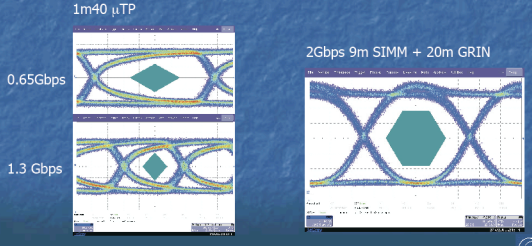
Proposal 1: The ATLAS SCT Straw-Link

- (T. Weidberg, Oxford, Oct 05)
  - 2500 links
  - 2.5Gbps
  - Start from scratch



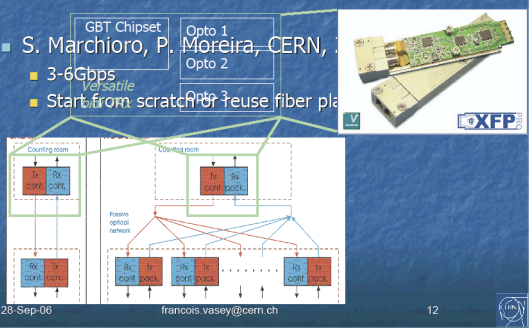
Proposal 2: ATLAS Pixels

- K.K. Gan, Ohio State University
- Reuse existing cable plant
  - 1m micro twisted pair, 8m SIMM fiber, 70m GRIN fiber, 1Gbps



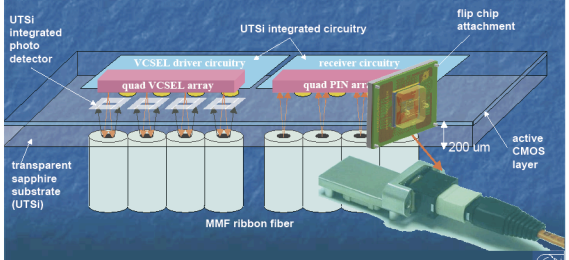
Proposal 3: The versatile bi-directional digital link

- S. Marchioro, P. Moreira, CERN,
  - 3-6Gbps
  - Start from scratch or reuse fiber pla

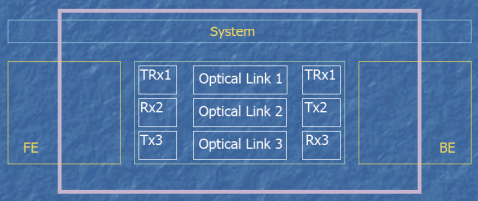


Proposal 4: Flipped OE devices on SoS substrate

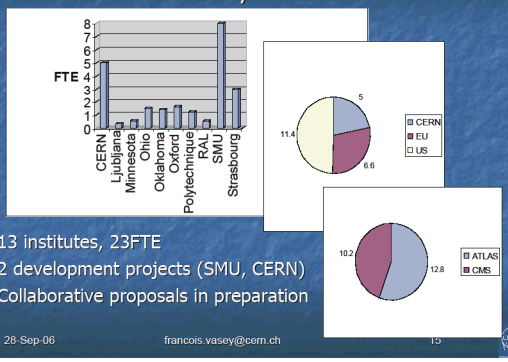
- Ping Gui, Jingbo Ye, SMU, 2005
- Start from scratch or reuse fiber plant



The Joint Optoelectronics Working Group



Joint Optoelectronics Working Group Survey Result



- 13 institutes, 23FTE
- 2 development projects (SMU, CERN)
- Collaborative proposals in preparation

Conclusions

- Options for Optical Links at SLHC are:
  - Reuse existing system (open to CMS only)
  - Reuse fiber plant only (open to CMS and ATLAS Pixels)
  - Start from scratch (possibly using components identical to existing ones).
- Check margins of existing components thoroughly
  - Investigate Laser and PIN diodes in depth
    - Will we reach the total dose limit at SLHC?
  - Draw a line of usability at SLHC, with safety margin.
  - Investigate electronic mitigation techniques (total dose and SEE).
- For new components, concentrate on only very few options.
  - Generic and versatile
  - The joint optoelectronics working group has the potential to coordinate a few parallel projects across experiments.
  - System level aspects to be addressed by the experiments.

Plenary Session 6
LHC Machine

RF Issues and Developments at the LHC Machine

A. Butterworth, L. Arnaudon, P. Baudrenghien, J. Molendijk

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andrew.butterworth@cern.ch

Abstract

The main RF system of the LHC, which uses 400MHz superconducting cavities, will be used to capture, accelerate and store the injected beam. A separate transverse damper system using electrostatic deflectors will be used to damp transverse oscillations. The associated low-level RF (LLRF) equipment is responsible for fast control of the accelerating voltage and phase in the cavities, the phase and radial position of the beam, and the synchronization of beam transfers between SPS and LHC. The LLRF system combines high-frequency analogue components with digital signal processing using FPGAs and DSPs. The extensive use of digital technology allows not only to achieve the required performance and stability but also to provide full remote control and diagnostics facilities needed in a machine where most of the RF system is inaccessible during operation.

I. INTRODUCTION: THE LHC RF SYSTEMS

The LHC will have one RF acceleration system and one transverse damping system. An additional RF system is foreseen for future high intensity operation:

1. *The 400 MHz main acceleration system* [1], which is used to capture, accelerate and store the beams. There are 2 independent RF systems, one per ring, each using 8 Cu/Nb superconducting cavities cooled by liquid helium at 4.5º K. Each tunable cavity is driven by a 300 kW klystron amplifier, and has a variable main power coupler allowing it to produce 1 MV at injection and 2 MV at top energy.
2. *The 200 MHz capture RF system* [2], which facilitates capture of the injected beam coming from SPS. The large 200 MHz bucket allows capture of beams with a longitudinal emittance of 1.0 eVs.. However, up to nominal intensity, the SPS is capable of producing beams with an emittance of 0.6 eVs which can be injected directly into the 400 MHz bucket [3] and so this system will only be installed, if necessary, at a later stage. The 200 MHz system uses room temperature copper cavities developing 0.75 MV per cavity, each powered by a 300 kW tetrode amplifier.
3. *The transverse damper system* [4], which uses electrostatic kickers to damp transverse beam oscillations. The beam position and angle are inferred from two beam position pickups and the trajectory is corrected on the following turn by the kickers. The feedback has a power bandwidth of around 3 MHz to damp injection errors and a low power bandwidth of 20MHz to damp all possible coupled bunch modes, the bunch frequency being 40 MHz. The damper can also be used to excite the beam for measurements and to clean particles out of the abort gap.

II. SLOW CONTROLS

Slow controls for the high-power RF equipment, which includes high voltage power supplies, klystrons, RF waveguide power distribution, cryostats and ancillary equipment, is based on industrial controls using Schneider PLCs [5]. PLC supervision is implemented using the tools provided by the CERN/AB controls group [6]. The system uses industrial components, with the exception of a small number of in-house hardware developments:

- RF power meters with a bandwidth of 50 MHz to 2.7 GHz.
- Optical arc detectors for protection of the waveguide distribution system from damage due to discharges.
- A universal temperature conditioner capable of driving the wide variety of temperature sensors used in the cavity cryo-modules.
- A fast interlock system, opto-isolated with readout via Ethernet or a variety of fieldbuses.

Sequencing and scheduling of equipment for accelerator operation is accomplished via the accelerator control system using the FESA (Front End Software Architecture) framework [7] and its interface with the General Machine Timing system [8].

III. LOW-LEVEL RF SYSTEMS

The RF systems require many feedback loops for fast control of the RF and beam parameters, as well as fast timing for synchronization between accelerators. These fast RF controls are referred to as *Low-Level* RF (LLRF) systems.

A. Challenges of the LHC beam

High beam current: At high beam intensity (0.56 A DC at nominal intensity), beam-induced fields due to the cavity impedance result in beam instability, and fast RF feedback loops around the cavities are required to reduce the impedance seen by the beam [9].

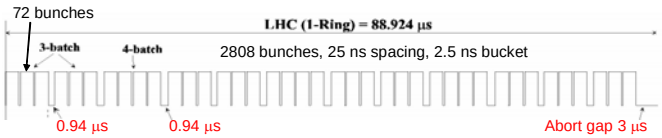

Figure 1: Longitudinal LHC beam structure. 3 or 4 PS batches of 72 bunches are transferred at each injection from the SPS.

Transient beam loading: The uneven distribution of the beam around the LHC circumference (Figure 1), with gaps between the injected batches, means that the cavity is subject to frequent large step changes in the beam current, which must be compensated by fast feedback, with consequent large power transients in the RF equipment [10].

Negligible natural damping: The longitudinal damping time in LHC due to synchrotron radiation for protons at 7 TeV is about 13 hours. In order to retain control of the longitudinal emittance blow-up due to RF noise, the phase noise (jitter) in the total RF system as seen by the beam must be limited to below 0.17° rms, or about 1 ps at 400 MHz [11].

B. *The RF Low-Level system layout*

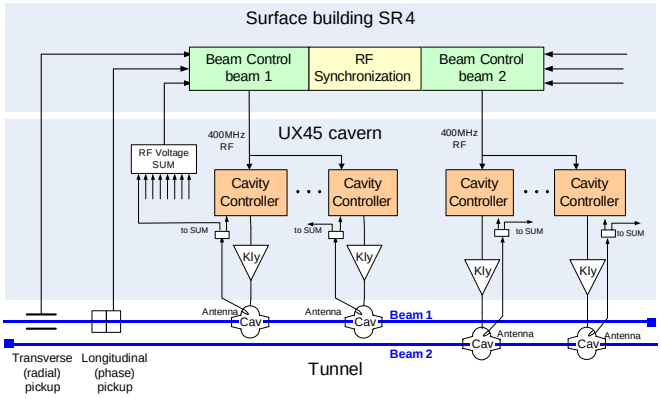

Figure 2: 400 MHz Low-Level system layout (simplified)

A schematic layout of the 400 MHz LLRF system is shown in Figure 2.

The cavity controller implements feedback loops to control the phase and amplitude of the accelerating field in the cavity, using a field measurement from an antenna in the cavity and generating the corrected RF signal which is fed to the klystron. A fast analog feedback path, designed to reduce the effective cavity impedance, with a total delay of around 600 ns, operates in parallel with a slower digital path, designed to give precise control of the 400 MHz fundamental. This direct feedback gives an impedance reduction of a factor 10. A third path, with a one-turn delay, serves to reduce the impedance by a further factor of 10 at the revolution frequency harmonics. The cavity controller also contains slower loops for cavity tuning, which maintains the cavity resonant frequency at the correct value, and for linearization of the klystron amplifier response.

The beam control system implements feedback loops to control the phase and radial position of the beam, measuring by means of longitudinal and transverse beam pickups, and acting on the RF frequency which is sent to the cavity controllers. In addition, the beam control system implements the frequency program which tracks the accelerator's magnetic field during acceleration.

The RF synchronization system provides synchronization between the two LHC rings and fast timing for bunch-into-bucket transfers from the SPS. The synchronization system also provides revolution frequency and bunch clocks to the experimental detectors [12].

IV. Technology Choices for Low-Level RF Implementation

As described above, the LLRF is implemented as a hybrid analog and digital system. FPGAs (mostly Xilinx Virtex-2 and 4) are used to perform fixed-point calculations at 40 or 80 Msamples per second, synchronous with the RF frequency. Examples of the algorithms concerned are digital filters: FIR, IIR, CIC, Half-band, Hilbert etc. and the CORDIC (COordinate Rotation DIgital Computer) algorithm which is used for trigonometric operations and phase comparison. Board control logic, including the VME interface, is implemented in the same FPGAs, usually at an independent clock frequency of 50 MHz.

DSPs (TigerSHARC from Analog Devices) are used for floating-point calculations at the revolution frequency (11kHz) or slower. Examples include the cavity tuning loop, where the frequency response is limited by the mechanical stepper motor actuator to a few Hz, and the beam control loops which must be fast only with respect to the synchrotron frequency, which in LHC varies between 21 and 62 Hz.

High Frequency analog electronics is used where the highest bandwidth and lowest group delay are required.

A. *Integration: crate and form factor*

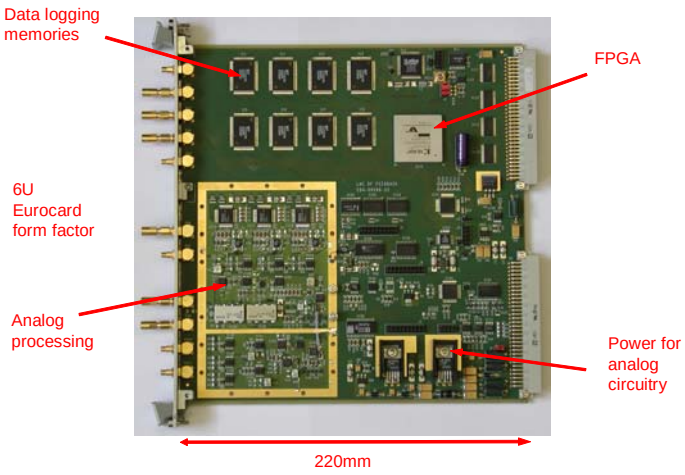

Figure 3: Typical RF Low-Level module: RF feedback

The use of digital technology promises to reduce drastically the amount of space required, as the equivalent of many analogue modules can now be implemented in a single FPGA. However, when considering the physical layout for the LLRF electronics, a number of requirements were identified:

- RF front-end electronics with shielding boxes take up a lot of board space, and the standard VME 160mm Eurocard format was judged by the RF designers to be rather restrictive.
- Large numbers of inter-board connections are required, with multiple clocks, triggers and digital signals.

- High quality linear power supplies are required for the analog RF circuitry.

After considering a number of options, it was decided to define a custom 6U Eurocard format with a depth of 220 mm (Figure 3). A P1-only VME backplane provides an A24/D16 interface, with a custom P2 backplane providing the LLRF-specific interconnects [13].

The custom crate is shown in Figure 4. The four leftmost slots have a card depth of 160 mm and are used to house the PowerPC CPU board and other standard VME modules such as General Machine Timing receivers. A short VME P2 bus is present in these slots to provide an A32/D32 interface. The 15 remaining slots are 220 mm deep with the custom P2 backplane and are used for the LLRF-specific boards.

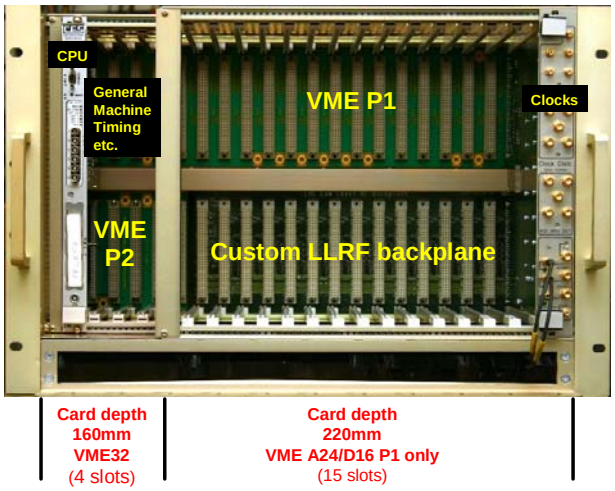

Figure 4: Custom LLRF VME crate

The custom LLRF backplane has a number of features:

- Timing and triggers
- Boot status and cold reset for FPGAs
- Interlocks and alarms
- Beam synchronous 20 and 40 MHz clocks and revolution frequency
- Absolute 10 MHz reference clock for frequency generation
- Digital data exchange between neighbouring boards at 1 Gbit/s
- Serial encoded distribution of function data at 1kHz, 16 channels
- JTAG daisy-chain for reconfiguring FPGAs
- Linear power supplies +/-12V, +/-6V
- 3.3V switched-mode supply for digital electronics

A module serial number bus is also provided, based on Dallas ID chips installed on each board. This allows the serial numbers of all the boards installed in the crate to be read remotely, and gives the possibility of implementing a database-driven management system for calibration data.

V. EMBEDDED DIAGNOSTICS

Since a large part of the RF equipment is inaccessible during beam operation, the provision of adequate remote control and diagnostics is essential. All LLRF VME boards are equipped with on-board data logging memory used to implement "virtual oscilloscopes" to acquire data from "virtual test points" inside the digital signal processing logic. Two parallel sets of memory buffers are provided. One is dedicated to Post-Mortem capture, and runs continuously at full rate until frozen by a Post-Mortem trigger from the backplane. The other, the "observation" buffer, is available for user diagnostics, has configurable sampling rate, and is triggered by a separate backplane trigger line which can be used to synchronize acquisitions between boards in a crate. An example is shown in Figure 5.

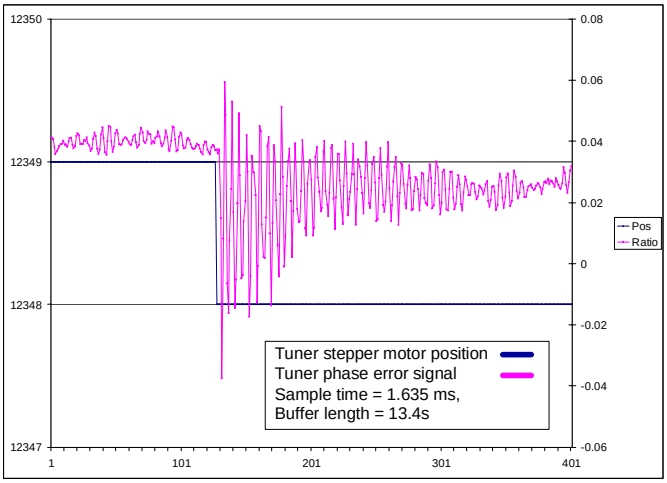

Figure 5: Mechanical resonance of cavity at 144 Hz observed on tuner error signal after motor step

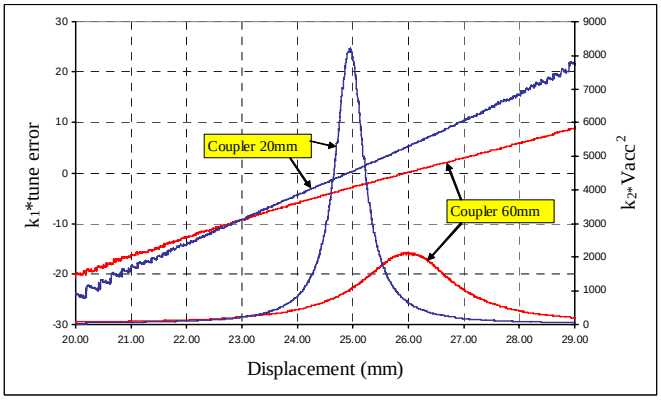

Figure 6: Automated cavity tuner resonance calibration scan

This embedded signal acquisition also enables automation of measurement and calibration procedures (Figure 6).

The logging memory is implemented using PC industry standard cache memory chips, with sufficient depth for acquiring 64 LHC turns at 40Msamples/s. The data is tagged with a revolution frequency marker for time-axis correlation purposes.

VI. HARDWARE DEVELOPMENT STRATEGY

A. Tools

For FPGA programming, the project team has standardized on Visual Elite [14], a graphical environment on top of VHDL which provides a structured design flow, graphical functional simulation and facilitates code reuse. Design portability is important, as although the target devices are mostly Xilinx, some Altera Stratix are also used.

Cadence [15] is used for board design, and its automated FPGA symbol creation facility allows efficient integration of the FPGA designs. The hierarchical features of Cadence allow concurrent design effort, for example development of the RF and digital parts of a board in parallel.

B. Design re-use

In addition to re-use of design components, the flexibility of FPGA-based systems has allowed many entire board designs to be re-used for diverse applications with only firmware modifications. For example, the tuner control DSP board is re-used as the beam control loops processor, the Direct Digital Synthesizer board used for cavity conditioning is re-used for the frequency program, and the 1-turn RF feedback board is re-used in the transverse damper.

VII. RADIATION ISSUES

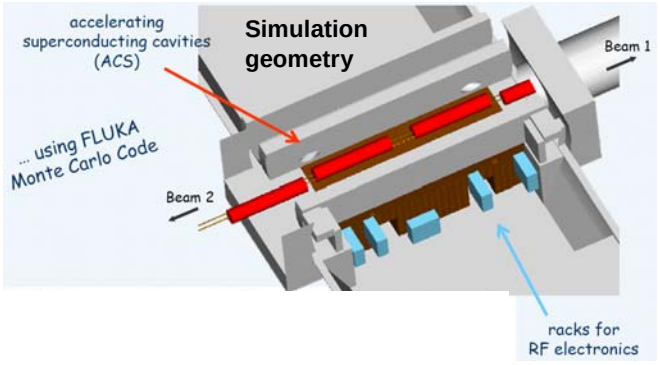

Figure 7: Geometry for FLUKA simulations [16]

Although the RF systems were designed from the outset without active semiconductor electronics in the beam tunnel, the racks containing the LLRF electronics were foreseen, to minimise cable delays, to be placed on a platform close to the cavity modules and shielded only by a 1.2 m thick concrete wall. The shielding was designed for personnel protection from X-rays generated by the cavities during high-power conditioning, but was not foreseen to shield against high-energy hadrons produced during beam operation. With a total of around 250 large SRAM-based FPGAs (typically 1 or 2 million gate Virtex devices) in the racks, it was important to estimate the risk of single-event errors, since a spurious re-configuration of one of these devices could result in the loss of a feedback loop and subsequent beam instability and dump.

A programme of simulations was undertaken using the Monte Carlo code FLUKA [17], to estimate the hadron flux produced by proton interactions with the residual gas in the beam pipe. The geometry used is shown in Figure 7. The results of the simulations showed, as expected, that the risks of radiation damage due to total integrated dose and displacement damage were negligible [16]. However, the expected number of single-event errors due to high-energy neutrons in the FPGA configuration latches was estimated at between 20 and 200 per year under nominal beam and vacuum conditions. This was judged incompatible with reliable beam operation. Since the physical layout precluded the installation of additional shielding around the racks, a decision was taken to relocate them to a position further away from the beam axis and behind an additional shielding wall. In the new location the neutron flux is calculated to be lower by a factor of 4 and there is sufficient space to install additional shielding, should it prove necessary.

Single-event mitigation techniques such as triple modular redundancy were also considered. However, it was decided to avoid the additional complexity of this approach initially, but to ensure that the unused capacity of the devices is sufficient to add redundancy for critical blocks if required at a later date. A hard reboot of all devices will be performed at the end of each LHC fill.

VIII. CONCLUSION

The principal components of the two systems required for LHC startup, the 400MHz RF and transverse damper, are currently being installed in the LHC tunnel. A new, mainly digital, Low-Level system is under construction, implemented using FPGA and DSP technology in a custom VME format with a LLRF-specific crate. The basic functionality of the cavity controller has been successfully tested; the beam control and RF synchronization systems are not yet fully implemented, but must be available for the LHC engineering run at the end of 2007. Extensive embedded signal diagnostics have been designed into the system for remote operation. Possible radiation problems have been considered and precautions taken to avoid them.

IX. ACKNOWLEDGEMENTS

Hardware developments for the LHC Low-level RF, damper and controls: D. Glenat, G. Hagmann, W. Hofle, D. Landre, R. Louwerse, A. Rohlev, V. Rossi, D. Stellfeld, D. Valuch, U. Wehrle. FLUKA simulations: K. Tsoulou, V. Vlachoudis, A. Ferrari.

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The LHC beam loss monitoring system's data acquisition card

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Abstract

The beam loss monitoring (BLM) system [1] of the LHC is one of the most critical elements for the protection of the LHC. It must prevent the super conducting magnets from quenches and the machine components from damages, caused by beam losses. Ionization chambers and secondary emission based beam loss detectors are used on several locations around the ring. The sensors are producing a signal current, which is related to the losses. This current will be measured by a tunnel electronic, which acquires, digitizes and transmits the data via an optical link to the surface electronic. The so called threshold comparator (TC) [2] collects, analyzes and compares the data with threshold table. It also gives a dump signal through the combiner card to the beam inter lock system (BIC).

The usage of the system, for protection and tuning of the LHC and the scale of the LHC, imposed exceptional specification of the dynamic range and radiation tolerance. The input current dynamic range should allow measurements between 10pA and 1mA and it should also be protected to very high pulse of 1.5kV and its corresponding current. To cover this range, a current to frequency converter (CFC) is used in the tunnel card, which produces an output frequency of 0.05Hz at 10pA, and 5MHz at 1mA. In addition to the output frequency, the integrator output voltage is measured with a 12bit ADC to improve the resolution.

The location of the CFC card next to the detector imposes the placement of the card in the LHC tunnel, exposing the card to radiation. The radiation tolerance was defined by assuming a 20 year operation period corresponding to 400Gy. A mixture of radiation tolerant Asics from the microelectronic group at CERN, and standard component was chosen to cope with these requirements.

I. INTRODUCTION

There will be several systems installed for the protection of the LHC, but one of the most critical is the beam loss monitoring system. The system consists of around 4000 detectors, ionisation chambers and secondary emission monitors. A total of 650 data acquisition cards will be installed in the LHC arcs and side tunnels next to the straight sections of the ring. In the arc, the CFC card will be placed in small racks located below each quadrupole magnet. Due to the high radiation in the straight sections, the CFC cards are concentrated at two locations at each LHC interaction region. The CFC data will be transmitted via an optical link to the surface electronics. It consist of 340 TCs with optical receiver mezzanine, situated in 25 VME creates, distributed in the surface buildings around the LHC. The VME creates will also host the PowerPC, a combiner card, and two timing-cards. The PowerPC collects the running sum values of the TC, and sends it to a database. The combiner card has a hardwired link to the BIC, which transmits the beam dump signal to kicker magnets.

A. *Specification of the data acquisition card*

The exposition to radiation leads to the requirement of a tolerance of a maximum of 400Gy integrated dose for 20 years LHC life-time. For the system and the performed tests a maximum value of 500Gy was chosen to ensure a safety margin.

The employment of the system for the LHC protection requires a high reliability of the CFC card. To achieve a reliability level SIL3 [3] (10^{-7} to 10^{-8} failure/h) of the system, several different test modes, status information, protection circuits and a redundant data transmission are implemented. For the verification, different tests have been performed, like irradiation, temperature and burn-in test. An additional test in magnetic field was included.

Table 1: Specifications requirements

Current measuring range	2.5pA	1mA
Error down to 10pA	-50%	+100%
Error down to 1nA	-25%	+25%
Maximal input current	561mA	
Input voltage peak	1500V @ 100us	
Radiation	500Gy in 20yr	
Digital supply	+ 2.5V	
Analogue supply	+/- 5V	
HV monitor input	0V	+5V

B. *The data acquisition card*

To measure a current over this high dynamic range, a CFC (figure 1) has been chosen, which is based on the balanced charge integrating techniques. In comparison with other switching techniques, the CFC advantage is given by no dead times and no losses of charges [4]. Since the output frequency depends on the input current (small current correspond to a very low frequency), an addition analogue to digital converter (ADC) is added to measure the output voltage of the integrator and to calculate partial counts in the TC. This measure decreases the response time and increases the dynamic range. The counting time window of the system is 40µs. The data including the counted CFC pulses and the integrator output voltage are transmitted every 40µs to the TC. The requirements of a small leakage current and a fast charge/discharge led to the choice of the OPA637 as the

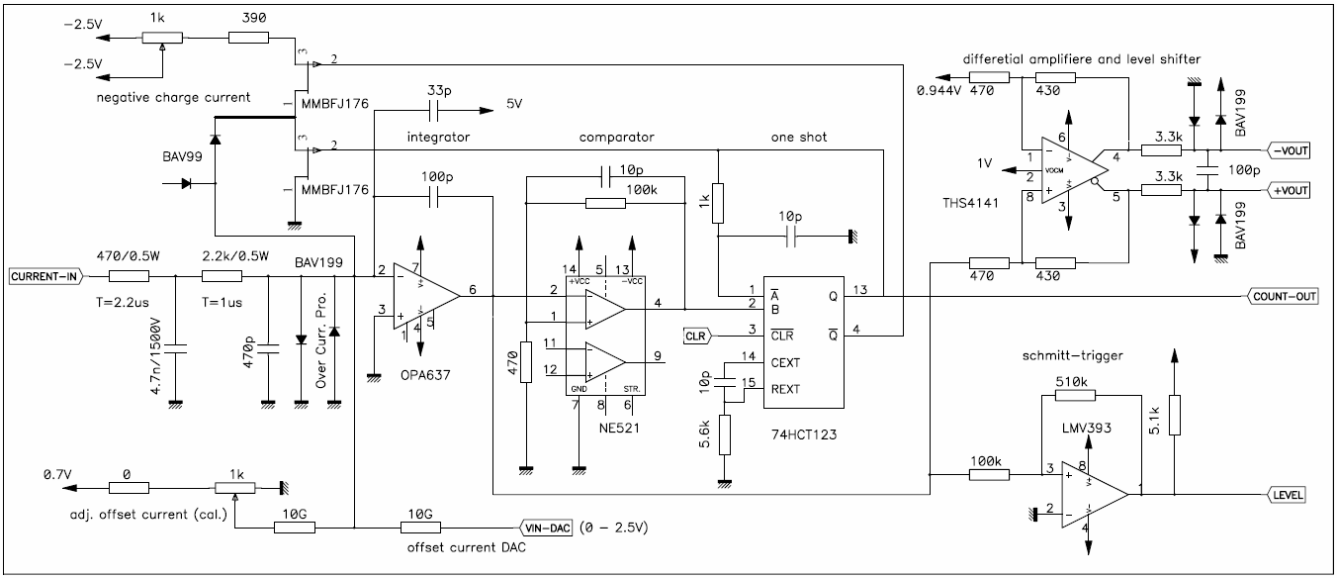

Figure 2: Circuit diagram of the CFC for one current input

operational amplifier in the integration circuit. The radiation tests showed that the chosen amplifier OPA637 did resist the irradiation. But the input offset current increased from typically 2pA to -50pA to -80pA with an integrated dose of 500Gy. Conversely, the amplifier maintained its functionality even with a dose of up to 1500Gy. The JFET J176 used for the switch discharge circuit was adding a positive leakage current of +150pA under radiation, but this current could be removed with the insertion of a diode BAV99 into the current path. The irradiation of the comparator NE521 and the one shot 74HCT123 produced an error of less than 0.5%. Standard ADCs have been irradiated and failed already with a small dose. The radiation tolerant ADC AD41240 [5] produced by MIC showed no decrease in functionality under radiation. The AD41240 is used together with the deferential line-driver CRT933 (from MIC), which is needed as level shifter between the ADC and FPGA. To connect differential analogue input of the ADC to the single ended output of the integrator, a THS4141 is used.

For the data conditioning, a FPGA has been chosen. To achieve a higher radiation tolerance, an antifuse type is used instead of a flash based FPGA. Actel provides a standard type A54SX72A and a radiation hard type RT54SX72A, but the RT54SX72A are far too expensive for such a system, which requires 750 pieces. The FPGA did withstand a total dose of 480Gy to 790Gy.

For the data transmission, an optical link is chosen instead of a copper based one, because the distance between the transmitter and the receiver, can be up to 2km. Several standard systems from the market have been tested but all of them failed while irradiation. Here again, the MIC provided the solution. For the CMS experiment, they produced a gigabit optical link (GOL) [6], which is utilised in the gigabit optical hybrid (GOH). For the BLM system a special GOH with an E2000-APC optical connector was produced.

To survey the specified function of the CFC card several status bits are constantly checked and transmitted together with the data frame. All the voltage supplies, including the external high voltage, are monitored with a comparator circuit using a LMV393. Two independent monitoring systems are used for the CFC. A Schmitt trigger circuit, using a LMV393, monitors the integrator output level and sends a flag if it exceeds 2.4V. The second survey technique for the CFC introduces a constant input current of 10pA, which corresponds to one count every 20s. The counts are monitored, and in case of 120s without a count, an error flag is generated and transmitted.

Due to increasing negative leakage current of the OPA637 with the radiation dose, an active compensation has been added to ensure a constant 10pA input current. The compensation current is produced using an 8 bit digital to analogue converter AD5346 with a 10G resistor connected to the input of the CFC.

The complete CFC card has been irradiated up to a total dose of 500Gy. To detect SEU, the redundant CRCs had been verified and compared at the receiver part. No SEU was detected up to $1x10^{12}$ p/cm^2.

C. Functional description of the FPGA

The functionality is shown in figure 2. All input signals are registered with 40MHz, due to some malfunctions of finite state machines (FSM) and other logical parts of the FPGA. For example, the counter input, which was connected directly to the input buffer, produced random values at the counter output with a well defined input frequency. Adding a register solved the malfunctioning of the input buffers. Due to the limited FPGA size (an overall of 6036 cells), only the CFC counters, which are most critical, have been tripled. The ADC values are insignificant for the threshold value comparisons. Tripling will decrease the probability of a fault beam dump provoked by a SEU. The system reset is also tripled but all the remaining logic is not tripled. The two GOH interfaces are redundant blocks, which are connected to the GOHs. The 40MHz system clock is connected to the hardwired HCLK and to the 4 quadrant QCLK. This opens the possibility to distribute the 40MHz internally in accordance to the importance of the blocks. The HCLK is used for the GOH interfaces, because of speed considerations, and for the counter block, because it is less sensitive to SEU.

The entire clock, timing, enable and other control signals, which are used in the FPGA, are produced in the clock divider. This includes several counters to produce enable signals of 200ns, 40µs and 1s. With these counters all control signals are produced. There is also a 16 bit counter that produces the frame identity number (FID) which increments every sent frame and is checked at the receiver part.

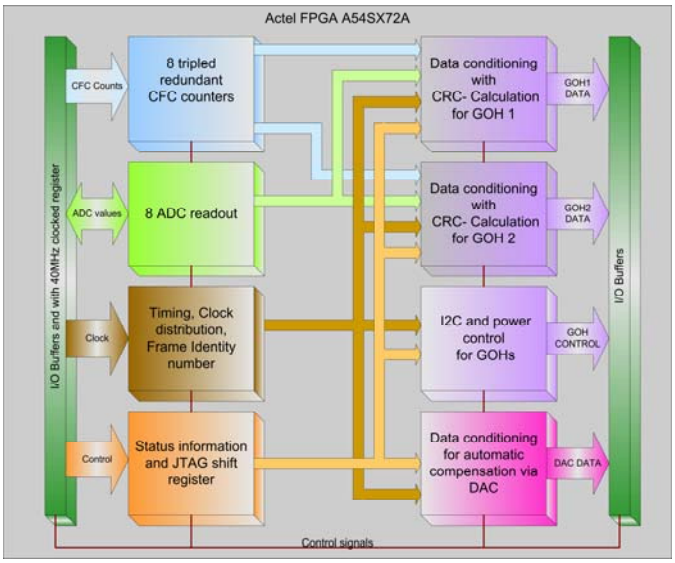

Figure 2: Block diagram for FPGA

In the status block, all the status bits coming from the pins and produced internally are registered every 40µs. A shift register is introduced to read out the card identity number (CID), which is stored as the silicon signature of the FPGA. The signature is programmed into each single chip and readout via the JTAG. This CID is read and checked for every frame in the TC.

As there are 8 similar current inputs and CFCs, the block shown in figure 3 exists 8 times. The count signals coming from the one shot are physically connected to 3 I/O pins and all the logic is tripled inside this block.

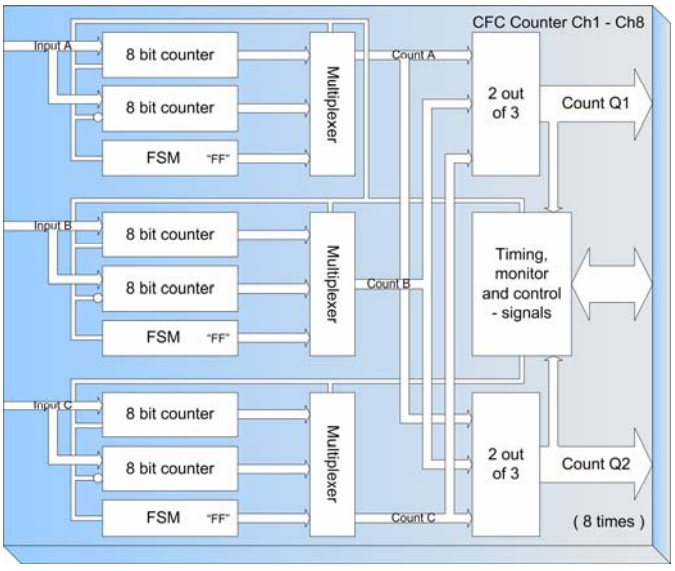

Figure 3: Block diagram for CFC counter (1 channel)

This counter signals are connected to two similar 8 bit counters. The counter used is a fast balanced counter produced by the Actel SmartGen macro builder. The enable signal is gated with a 40µs signal. One of the enable signals is inverted, therefore the counters work in chopper mode. This design has been chosen in order to have one less time critical part, as there is 40µs gap available instead of 25ns to read out the information. Since the selection in the SmartGen is poor concerning the types of counters and In and Output configurations, the addition of a FSM was necessary to ensure that in case of overflow the output would stay 255. The counter outputs are connected to a multiplexer, which switches between the two counters every 40µs, except in case of overflow when the third input is selected. This counter value is produced 3 times per CFC channel. These 3 values are sent to two 2-out-of-3 voters, each of them feeding one GOH interface.

The ADC is connected via two 12 bit data lines (figure 4), the information of two channels is multiplexed and changes with the rising or falling edge. Rising edge corresponds to ch0 and ch2; falling edge to ch1 and ch3. The sampling frequency of the ADC is 5MHz but the readout of the system is every 40µs.

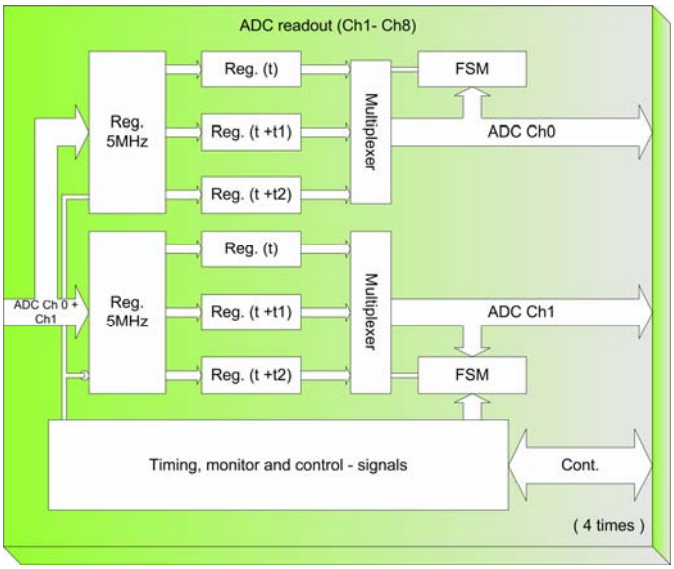

Figure 4: Block diagram for ADC readout

To separate the multiplexed ADC values the readout of the two channels is shifted by half a period of the clock frequency. A special logic has been implemented in case the CFC pulse is close to the readout of the ADC. It was observed that the CFC plus was counted in the specified 40µs window, but the ADC value was near zero instead of the maximum value. The delay between the positive edge of the CFC pulse and the integrator output causes this effect. A FSM was introduced to check if there is a count in a defined time window of 100ns, and a second FSM checks the ADC value. In case a pulse appears in this 100ns time window, the next readout value will be chosen. Due to the rise time of the integrator signal, a wrong ADC value can still appear. Therefore, a second FSM compares the value with a threshold and if necessary, it uses the 2nd ADC readout. The 3 readouts are always registered and connected to a multiplexer. The two FSMs select the correct value.

There are two redundant GOH interfaces. To increase the reliability of the data transmission, both interfaces calculate a 32 cycle redundancy check (CRC), which is transmitted together with the data. The incoming data are combined to 16 bit words and then connected to a 20 * 16 bit multiplexer.

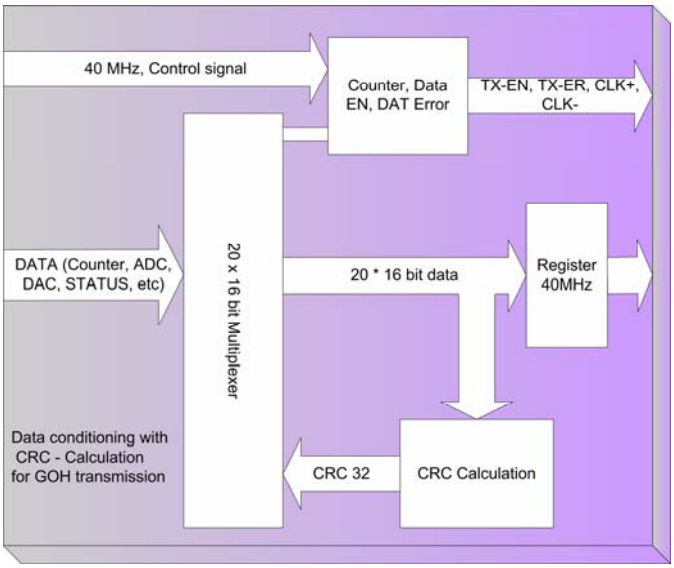

Figure 5: Block diagram GOH interface

The last two input ports are connected to the output of the CRC calculator. The output of the multiplexer is connected to the input of the CRC calculator block and to a register clocked with 40MHz, which connects to I/O buffer. A data enable and data error signal, which are produced in this block, are needed to control the GOH transmission. The transmitted data frame is shown in table 2.

Table 2: Data frame

CID (card identity number)	
STATUS 1	
STATUS 2	
Count 1	ADC 1
ADC 1	Count 2 / ADC 2
ADC 2	Count 3
ADC 3	Count 4
Count 4	ADC 4
Count 5	ADC 5
ADC 5	Count 6 / ADC 6
ADC 6	Count 7
ADC 7	Count 8
Count 8	ADC8
FID (frame identity number)	
DAC1	DAC2
DAC3	DAC4
DAC5	DAC6
DAC7	DAC8
CRC	
CRC	

The GOH includes the possibility to receive commands via the I2C. While carrying out a temperature test, some CRC errors have been observed while transmitting data. This has been improved by changing the laser diode current. The two temperature signals coming from two sensors placed on the PCB are used to switch from nominal current 11.4mA to 16.2mA, via the I^2C bus. In addition, the GOH-reset and the two GOH-flag signals allow switch off and restart the GOH. This is useful in case of the GOH malfunction.

There is an active compensation using a parallel interfaced 8 bit DAC. The DAC is controlled by the DAC interface shown in figure 6. Each counter value from both 2-out-of-3 voters are connected to the first stage, which is producing a reset signal for each arriving count. This reset pulse is used to reset the 20 second timer. If there is no reset, the following 8 bit counter will receive an enable signal and increase the counter by 1. This process is repeated till a count appears every 20s at their outputs. These 8 values are multiplexed and sent to the data input of the DAC. Together with the control signal and the address, it will set the currents on the different input channels. The same enable signal is connected to a 3 bit counter and increased also by 1. In case this value reaches 6 an error flag is set, which indicates a problem with one of the CFC input circuits. The counter will be also reset when a count will arrive.

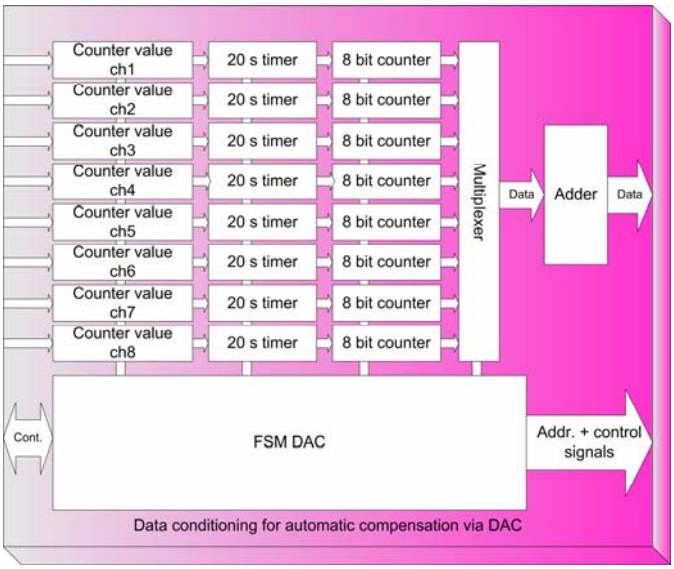

Figure 6: Block diagram DAC interface

Since the optical link is unidirectional for communication between surface and tunnel equipment (TC to CFC), the high voltage (HV) supply connection is used (bias voltage for all the ionisation chambers). All tunnel cards are connected to the HV because its level is part of the status checks. Four comparators circuits with increasing HV thresholds are connected to the FPGA. The Status_HV is used as HV monitor. The CFC_TEST, RST_DAC, GOH_RST and the LEVEL1-8 are the inputs for the FSM (figure 7). If the 3 pins are at '0', the FSM is in the default state "wait_for_cfc_test". If the CFC_TEST = '1', a counter is started. If the input is constantly '1' for 120s, then the state changes to "CFC_TEST_ON". In this state an adder in the data path of the DAC is increasing the DAC value by 100 corresponding to an input bias current increase of 100pA. The state will remain till the pin CFC_TEST changes to '0' (HV_{nom} = 1500V) and the LEVEL1-8 are at '1' (integrator voltage <1.8V). The LEVELs are included to ensure the CFCs are working correctly. For the DAC_RST and GOH_RST the same sequence needs to be followed and also 100pA is added.

The difference is an additional state which, is just before entering into the default state. As a consequence of this procedure, all the CFCs will work as defined, before the DAC is being reset or the GOH is being restarted. The active compensation is blocked as soon the FSM enters to a test or reset state.

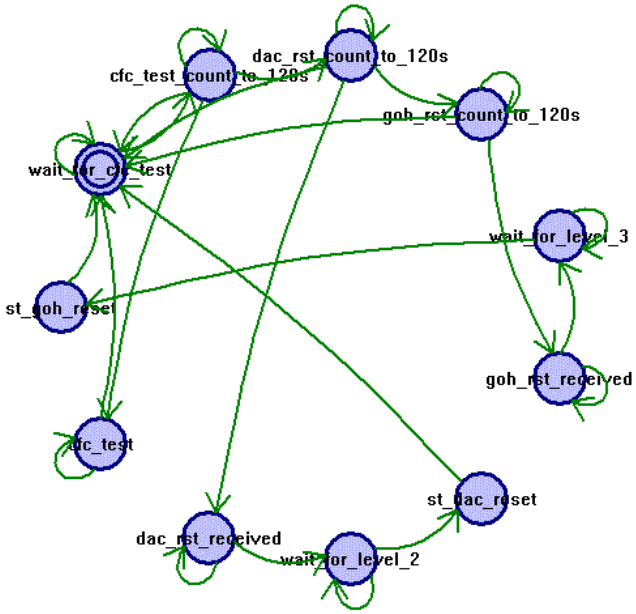

Figure 7: FSM DAC

D. Tests, test-modes and error detection

To ensure the system is working properly and to increase the reliability, several tests, test modes and error detection system have been added.

Before the installation, a calibration and an initial test are performed using a BLECFT [7] USB card, which performs an automatically generated functional test pattern. This system will also be used for additional tests after tunnel installation.

The constantly performed test using 10pA offset current, provides a count every 20s. After absence of the count for more than 120s, an error bit is activated.

For the data transmission a CRC is added, which will be verified at the TC. Due to the redundant link, even if one transmission is corrupted, data are still available.

The CID is sent and checked every transmission to ensure the used threshold table belongs to the correct chamber. Lost data transmission will be detected by the check of the FID at each data transmission.

With the CFC_TEST activated (HV ≥ 1655V for 240s), 100pA are added on the input of the CFC, to test the corresponding response of the acquisition chain. It is foreseen that this test will be carried out before each beam fill.

A HV modulation test uses capacitive current injection via chamber electrodes to detect the degradation of the complete acquisition chain. This test will be carried out before each beam fill.

There is also 32 status bit (table 3) which are sent and readout every transmission. Depending on the indicated malfunction a beam-dump is initiated.

Table 3: Status bits (E =error, W=warning, I=information)

Status 1			Status 2		
Status_P5V	E	<4.73V	CFC-ERR1	E	>120s
Status_M5V	E	>-4,72V	CFC-ERR2	E	>120s
Status_P2V	E	<2.25V	CFC-ERR3	E	>120s
Status_HV	E	≥ 3.183V	CFC-ERR4	E	>120s
TEST_CFC	I	≥ 3.633V	CFC-ERR5	E	>120s
TEST_ON	I	(≥ 1655V)	CFC-ERR6	E	>120s
RST_DAC	I	≥ 4.006V	CFC-ERR7	E	>120s
DAC_RST_R	I	(≥ 1825V)	CFC-ERR8	E	>120s
RST_GOH	I	≥ 4.390V	LEVEL 1	W	>2.4V
GOH_RST_R	I	(≥ 2000V)	LEVEL 2	W	>2.4V
TEMP 1	W	>35ºC	LEVEL 3	W	>2.4V
TEMP 2	W	>60ºC	LEVEL 4	W	>2.4V
GOH 1 ready	W	"0"	LEVEL 5	W	>2.4V
GOH 2 ready	W	"0"	LEVEL 6	W	>2.4V
DAC_155	W	>155	LEVEL 7	W	>2.4V
DAC_OVER	W	255	LEVEL 8	W	>2.4V

E. Conclusion

An acquisition system to measure current in the range of 2.5pA to 1mA has been constructed and tested. An error smaller than the +96% down to 10pA and +6.5% down to 1nA has been measured and can still be improved by a more accurate calibration. A radiation tolerance of 500Gy has been achieved for all components except two components. The one shot 74HCT123 showed some malfunction at 340Gy but it recovered after stopping the irradiation. The antifuse FPGA form Actel did withstand radiation between 480Gy to 790Gy, no SEU was detected up to $1x10^{12}$ p/cm^2. Several protection and supervision circuits are build in and were tested successfully. The optical link is radiation tolerant due to its design and in a test setup installed in HERA no CRC occurred for several months. The system passed a temperature test (0 to 70°C) which caused some CRC errors while data transmission. The complete system was also tested in a magnetic field up to 1000Gauss with a small offset current change.

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On line radiation monitoring for the LHC machine and experimental caverns

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Abstract

With an unprecedented amount of electronic systems exposed to radiation, reduced operational efficiency due to radiation induced failures in electronic equipment has become a serious issue for the LHC. The RADMON radiation monitoring system presented here has been designed to measure radiation at the location of equipment and to provide an early warning as radiation levels start to increase. Nearly 300 monitors will provide on line measurements of the dose, dose rate, particle flux and particle fluence. The data can be visualised in real time in LHC control rooms and is stored in a database at a rate of 1 Hz. It will be shown that the system allows studying the spatio-temporal distribution of the radiation fields in the LHC.

I. INTRODUCTION

Radiation tolerance assurance of equipment has become a serious issue for the LHC. The LHC will operate with very high stored energy in the beams and a large amount of equipment in the vicinity of the beams will be exposed to radiation. Throughout the years there has been a growing awareness that radiation tolerance needs to be taken into account as an engineering and operational constraint in the LHC design [1]. This resulted in, for example, the reinforcement of radiation shielding, optimised integration of tunnel electronics and the widespread use of radiation tolerant electronic components and materials.

Radiation monitors were proposed in 2003 [2] with the aim to measure radiation at the location of the equipment and to evaluate the performance of technical equipment under irradiation. The monitors measure three components of a complex radiation field independently which allows to separate between the three different radiation damage effects. Experience from other proton colliders [3] had shown that monitoring is indeed very useful to characterise radiation induced failures, to provide insight into the way the machine is operating and to measure the efficiency of the shielding structures.

At present, a total of 284 monitors are being installed in the LHC of which 35 are located in the experimental areas and 249 in the LHC tunnel and the underground areas. The monitors are radiation tolerant to 200 Gy TID and can operate in a magnetic field inferior or equal to 4.6 kGauss. Each monitor has a total of 9 radiation sensors on board : 2 radiation sensitive p-channel MOSFETs ('Radfets') from NMRC [4] to measure the total ionising dose (TID), 3 photodiodes in series to measure the 1 MeV equivalent neutron fluence and 4 x 4 Mbit of static RAM to measure the hadron flux for hadrons with an energy above 20 MeV.

The controls architecture for the radiation monitoring system is using the accelerators controls standard [5] which is based on a three tier architecture, common for present day industrial J2EE applications. The gateway software has been developed in the FESA software development environment [6] for LHC front-end computers which is supported and maintained by CERN. During normal operation, data is send at a maximum rate of 80 Hz via a WorldFIP® fieldbus link to gateways located at the surface.

In what follows, a brief review of the design of the RADMON monitoring device will be given. The controls infrastructure will be described together with the data storage and data displays foreseen for LHC operations. Finally, a few examples will be given on how this system can be used in accelerator operations to reduce the risk of radiation damage to equipment.

II. *RADMON* RADIATION MONITORS

A. Complex radiation fields

The complex radiation field in the LHC underground areas is composed of different particles at various energies. Electronic components and systems exposed to such a radiation field will experience three different types of radiation damage which are displacement damage or Non Ionising Energy Loss (NIEL), Single Event Error rate (SEEs) and damage from the Total Ionising Dose (TID). The damage is proportional to, respectively, the 1-MeV equivalent neutron fluence, high energetic hadron flux (E > 20 MeV) and the Total Ionising Dose (TID).

For the radiation monitoring system, the complex radiation field is decomposed in terms of these 3 physical parameters (figure 1) which are considered orthogonal in the region of interest.

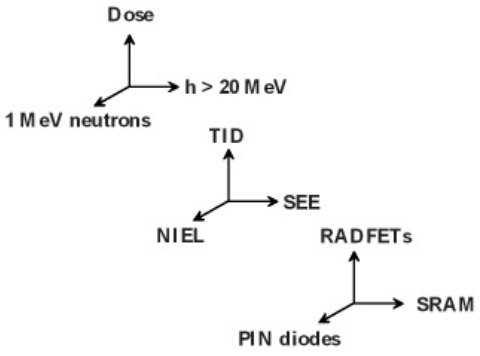

Figure 1: Parameterisation of a complex radiation field and the associated types of radiation damage and radiation sensors.

The radiation monitors measure these three parameters individually and independent of each other. The fluence to dose ratio provides information on the radiation spectrum and can be compared to Monte Carlo simulations. As will be shown in the last section, variations in the radiation spectra due to, for example, a modification in the geometry can be measured.

All measurements are tagged with UTC time (Universal Time Coordinates) and can be directly related to changes in the machine settings. The rate of data storage is 50 Hz for periods of 30 minutes or 1 Hz continuous.

B. Radiation Sensors

Each RADMON radiation monitor is equipped with 2 discrete p-channel MOS Field Effect Transistors or Radfets to measure the total ionising dose. Radfets are very sensitive to radiation because they have very thick gate oxides that enhance the trapping of radiation induced holes. For the RADMON system, 3 different types of Radfets are available with oxide thicknesses of 100 nm, 400 nm and 1 μm that provide a resolution of 100 rad/bit, 4 rad/bit or 1 rad/bit. Although any combination of these 3 types is possible, most monitors have either a 400 nm and a 100 nm or a 1000 nm and a 400 nm Radfet on board as these combinations provide the maximum resolution for a given total dose. The first combination is mainly used in areas with high radiation levels (i.e. 1 kRad or more per year).

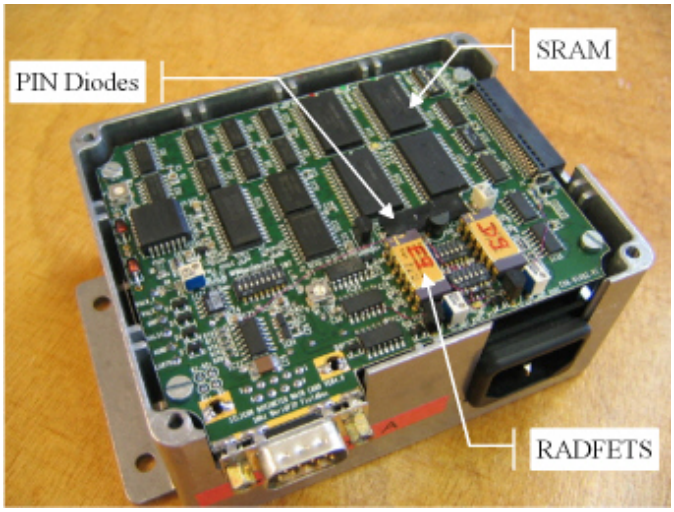

Figure 2: RADMON radiation monitor V4.1

Since their introduction in the 1970's, Radfets have found numerous applications in space, nuclear industry, research and radiotherapy. The devices used in the RADMON monitors are produced by Tyndall National Institute [7] and are equally used for space and medical applications. The response curves for various types of particles are therefore very well known and readily available [7,8].

The 1 MeV equivalent neutron fluence is measured with 3 BPWFS34 photodiodes from SIEMENS. These PIN photodiodes are well known to be sensitive to displacement damage from low energetic neutrons while unaffected by damage from TID damage. When irradiated with 1 MeV neutrons, the variation of the carrier concentration and the change in conductivity in these diodes is such that the forward voltage shift at constant current varies linearly with the neutron fluence. This makes these devices extremely attractive for direct measurements of the 1 MeV equivalent neutron fluence.

Each RADMON monitor has 3 PIN photodiodes. For high neutron fluences, it is sufficient to measure the change in the forward voltage of a singe diode. For lower fluences, the resolution needs to be increased by measuring the voltage of 3 diodes in series. In the latter operational mode, 1 bit corresponds to a neutron fluence of $9x10^9$ n/cm^2 (1 MeV eq.)

The monitors can equally measure the high energetic hadron flux and fluence with 16 Mbit of static RAM (Toshiba TC554001AF-7L). Hadrons with sufficiently high energy can change reverse the data state of a memory cell without permanently damaging the circuit (Single Event Upset or SEU). The number of memory cells that change their logical state is linearly depended on the hadron fluence to which the devices are exposed.

In the LHC, the hadron flux consists of mainly of neutrons. The SEU cross section of the SRAM memory is very low for low energetic hadrons but rises sharply at 20 MeV and remains approximately constant above this energy [9]. The proton and neutron calibration curves are used to convert the observed SEU rate in the equivalent hadron flux. The SEU sensitivity of the memories can be increased by lowered the bias voltage.

C. RADMON Functional description

The RADMON radiation monitors have been designed to stand at least 10 years of radiation in the LHC arcs assuming nominal operation of the LHC. The tolerance of each device is expressed in the usual 3 parameters is 200 Gy (TID), $2x10^{12}$ n/cm^2 (1 MeV eq.) and $2x10^{11}$ h/cm^2 (E > 20 MeV).

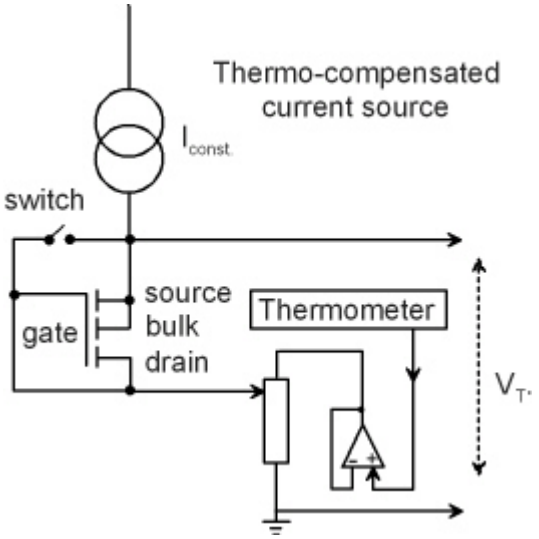

Figure 3: Schematic for the reader circuit of RADFETs during readout phase (switch open)

One of the prime concerns in the design has been the avoidance of error propagation due to Single Events in the readout and field bus communication circuitry. The design was therefore kept as simple as possible using a minimum of components. The monitors do not use programmable devices

or CPUs in the design and nearly all registers have been made triplicate modular redundant.

Another important point in the design is the thermo compensation of the analogue read out circuitry required for the Radfets and PIN diodes.

The readout configuration for the Radfets is shown in figure 3. During irradiation, the switch is closed and all terminals are grounded. To readout the Radfet, the switch is opened, and a thermo compensated constant current of 8.7 μA flows from the source to the drain. The threshold voltage needs to be thermally compensated before being converted by the on board ADC. The conversion of the threshold voltage V_T into accumulated dose occurs at the level of the equipment gateway.

The readout mechanism for the PIN photodiodes is essentially the same as the one for the Radfets. The only difference is that the readout current is 1 mA and that the PIN diodes require more important temperature compensation. More details on the analogue readout circuitry, the selected components and their radiation tolerance can be found in [10].

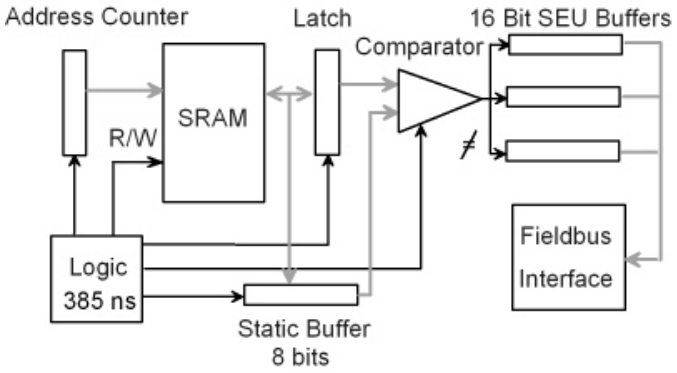

Figure 4: Schematic for the readout of the SEU counters of the RADMON monitors

The schematic for the readout of the Single Event Upset rate in the SRAM memory is given in figure 4. Each monitor has a total of 16 Mbit SRAM on board. The logic generates read-compare-write cycles every 385 ns and takes 700 ms to scan the entire on board memory.

During the reading phase, 8 bits of data are read in parallel from a specific address in the memory and latched into a register. At the same instant, the 8 bit reference pattern is written back at the same location in the memory. The latched bit pattern is checked for radiation induced errors by the comparator. If a SEU has occurred, the contents of all three 16 bit SEU buffer registers are increased by one. Triplication of the registers was needed here because the contents of these registers itself can be corrupted by single events.

D. RADMON system architecture

The RADMON system has a 3-tier architecture consisting of a resource tier, a communication tier and a presentation tier (figure 5). The resource tier consists of 284 RADMON radiation monitors on a total of 20 WorldFIP field bus segments (figure 5). The maximum number of monitors on a segment was deliberately limited to 32 to keep the response time sufficiently low.

A WorldFIP segment can be several kilometres long and may use optical fibres or copper as a transport medium. The line speed for the RADMON system is 1 Mbit/s. Each WorldFIP segment is connected to a gateway (an industrial Intel PC) and there are 20 gateways in total. Each gateway is connected to the CERN gigabit Ethernet backbone and to the machine timing network.

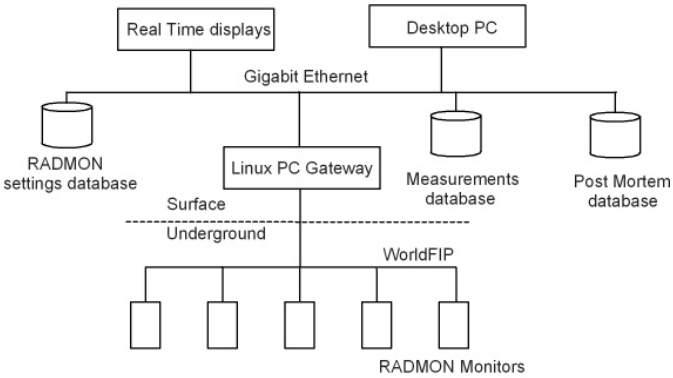

Figure 5: Schematic view of the RADMON system architecture

The entire system is database driven. At start up, the application software on each gateway loads the current settings data from the settings database. The settings file contains information on, for example, the calibration of the sensors and the hardware setting of each device. During the initialisation phase, the hardware address of each monitor is read. The hardware address allows finding the correct settings for that specific monitor in the configuration file.

During operation, measurements are stored in the LHC (oracle) measurement database at a rate of 1 Hz and in a local circular buffer in the gateway at a maximum rate of 50 Hz. The data in measurements database can be accessed by any user at CERN at any time. The contents of the circular buffer are made available upon request. Such requests can be a user request via the Ethernet network or it can be a trigger that arrives via the timing network (a post mortem trigger following a beam loss for example). All data is tagged with Universal Time Coordinates (UTC time) and with the operational status of the machine.

The engineer in charge in the LHC control room can visualise the radiation data on a set of real time displays which are updated at a maximum rate of once per second. There is the possibility to visualise the accumulated dose or fluence per fill for the entire ring or to focus on a specific area of the machine (such as the Long Straight Sections or the injection areas). It is equally possible to display the hadrons flux measured by the SEU counters in the monitors.

III. RADIATION MONITORING IN PRACTICE

A. Monitoring in the SPS

At CERN, the monitors have been extensively used in the target hall of the SPS. In this area, the proton beam from the SPS is sent on various primary targets to create secondary particle beams for the physics experiments located further downstream. Monte Carlo simulations [11] have shown that

the radiation field in this area is very similar to that which is expected in the LHC regular ARCs.

During the SPS proton in 2006, a single series produced monitor was placed in this area. During the startup of the SPS, the intensity of beam slowly increased and the monitor observed the associated increase in the radiation levels (figure 6).

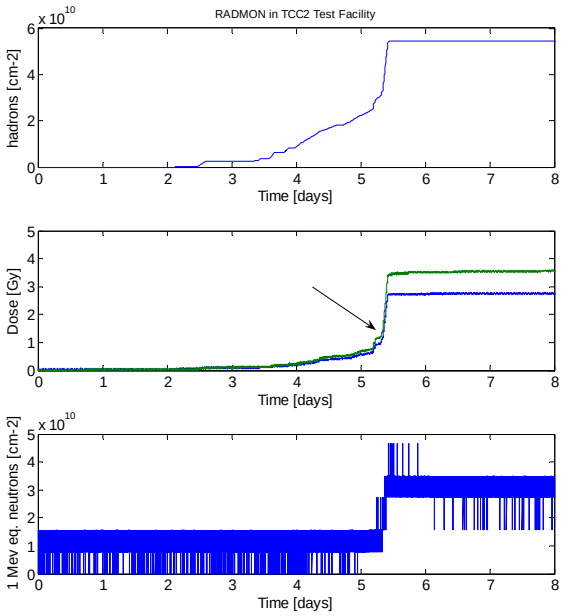

Figure 6: On line radiation measurements in the SPS North Experimental Area during the 2006 proton run.

Five days after the start of the data acquisition, the monitor observed a sharp increase in the dose rate (indicated by the arrow in figure 6) and a simultaneous sharp increase in the hadron flux and the 1 MeV eq. neutron flux. SPS operations were stopped one day later because the beam parameters for the physics experiment further downstream were incorrect. The reason for this anomaly was found to be a faulty bending magnet. The magnet in question deflected the proton beam in the vertical direction by a too large angle. The radiation monitor detected the hadronic shower caused by the losses of the primary protons further upstream.

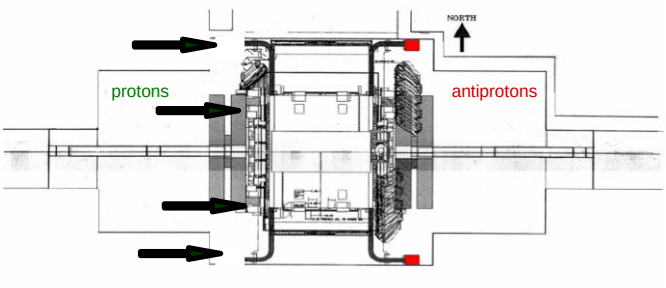

Figure 7: Top view of the CDF detector at FNAL. The 4 large arrows indicate the location of the 4 RADMON monitors

At Fermilab (FNAL), a set of 4 monitors was installed in the collision hall of the CDF experiment (Collider Detector at Fermilab) [12]. CDF is one of the main particle detectors of the Tevatron accelerator which collides protons with antiprotons. At CDF, a number of radiation induced failures have been observed [13] in the electronics in and around the detector and the monitors were installed to identify the various sources and to provide additional information on the composition of the radiation.

Figure 7 shows how the 4 monitors are placed symmetrically around the west side of the detector from which the proton beam is incident (Inner/Outer North West and Inner/Outer South West). Radiation levels at this side of the detector are higher because the proton beam is on average 10 times more intense than the anti-proton beam.

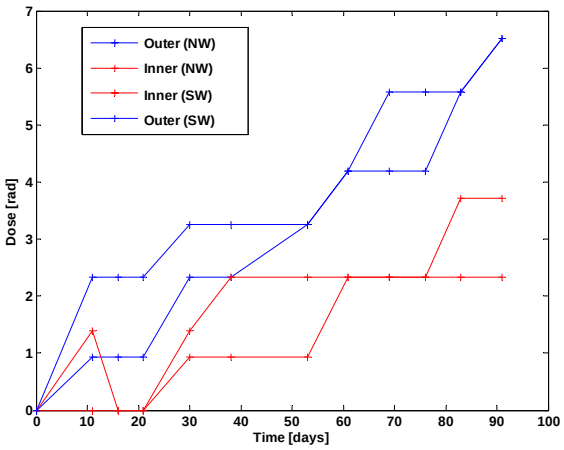

Figure 8: Evolution of the dose in the CDF collision hall during 100 days of luminosity running in 2005.

Figure 8 shows the evolution of the radiation level over a period of nearly 100 days of luminosity monitoring. The radiation levels are relatively low (a few rads) and linear depended on the integrated luminosity as expected. The fluence to dose ratio on the wall of the CDF collision wall was found similar to what has been simulated for the ATLAS cavern wall [14]

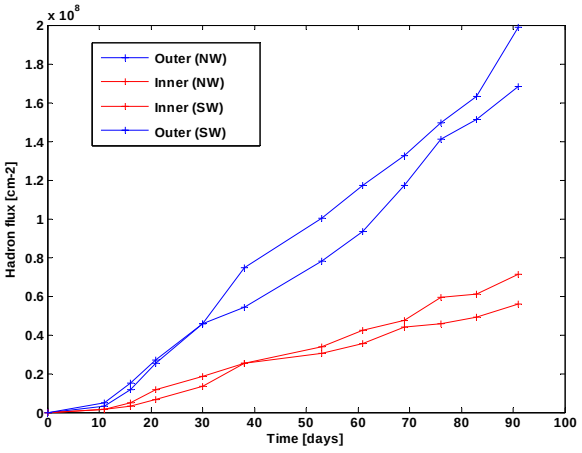

Figure 9: Evolution of the hadron fluence in the CDF collision hall during 100 days of luminosity running in 2005.

Figure 9 shows the evolution of the hadron fluence for the same period. Having a much higher resolution, the SEU counters allow distinguishing the inner and outer detectors regions but they also register small beam losses which are not

necessarily related to luminosity. For example, when one of the electrostatic separators (ES) in the Tevatron sparked a small fraction of the beam ended up in the CDF collision hall. The very small losses was detected in some of the SEU counters (Inner SW and Outer SW) but were invisible on the signals from either the Radfets or the PIN diodes. The data register for the Inner and Outer NW/SW detectors read :

```
ONW INW ISW OSW    Time

011 009 167 388    Nov 21 16:12:51 2005
011 009 168 392    Nov 21 16:13:06 2005
```

Other diagnostics determined that the beam abort occurred at 16:13 hrs local time. The increase in SEU counts measured by the monitors in the OSW location for this particular event corresponds to a fluence of 1 x 10^7 hadrons/cm^2.

IV. Summary and Conclusions

A certain number of precautions have been taken to deal with the issue of radiation and radiation damage to equipment in the LHC tunnel and experimental areas.

Firstly, radiation tolerant components and radiation tolerant design techniques have been used for all underground equipment that will be exposed. Secondly, radiation sources have been shielded whenever this was reasonably achievable and finally, radiation monitors have been installed to measure radiation levels at the location of the equipment from day one.

In total, nearly 300 monitors are being installed in the LHC underground areas and in the experimental caverns. Each monitor can be read out remotely over a distance several kilometres at frequencies between 1 and 100 Hz. The WorldFIP fieldbus protocol is used to communicate between the monitors in the underground areas and the equipment gateways at the surface buildings. Each gateway is connected to the machine timing network and to the gigabit Ethernet backbone and the gateway software stores data in the LHC measurement database at 1 Hz or in the Post Mortem database at 100 Hz. Measurements are also made visible via real time displays in the control rooms.

An important effort was required to assure the radiation tolerance of the monitors up to a total dose of 200 Gy and a neutron fluence of 2x10^{12} cm^{-2} (1 MeV equivalent neutrons). The reason is that the electronics design of a monitor is based entirely on Commercial of the Shelf components whose radiation tolerance needed to be verified via radiation tests outside CERN.

Another important issue in the design has been the thermo stabilisation of the various current sources and the automated thermo compensation of the readings from the radiation sensors.

A number of monitors have been used successfully in the primary target hall of the SPS accelerator at CERN and in the collision hall of the CDF detector at Fermilab. In both cases, the resolution of the monitors was sufficient to provide early warnings if the radiation levels were rising abnormally fast. The combination of

V. References

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Plenary Session 7
Beam, SLHC

Beam Phase and Intensity Monitor (BPIM) for the LHCb Experiment

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Abstract

The LHC bunch clock is transmitted over kilometres of fibre to the experiments where it is distributed to thousands of front-end electronics boards. In order to ensure that the detector signals are sampled properly, its long-term stability with respect to the bunch arrival times must be monitored with a precision of <100ps. In addition it is important to monitor the trigger conditions by measuring the intensity of each bunch locally in the experiment.

For this purpose a beam phase and intensity acquisition board (BPIM) has been developed for the Button Electrode Beam Pick-ups which will be installed on both sides of the LHCb interaction point. The board measures the two quantities per bunch, and processes the information in an onboard FPGA. The information is read-out by the Experiment Control System and is directly fed to the LHCb Timing and Fast Control (TFC) [1]. In the TFC system the information is included in an event data bank but may also be used as a bunch crossing trigger or gate.

I. Introduction

The LHC bunch frequency of 40 MHz is transmitted to the experiments via a network of optical fibres which is mostly based on non-phase-stabilized fibres located at a depth of about a metre. In the case of the LHCb experiment the total distance is about 14km. In LHCb the bunch clock is locally distributed by the Timing and Fast Control (TFC) system to all the detector front-end electronics where it is used to sample the detector signals which typically have plateaus of the order of a nanosecond. Thus it is of extreme importance that the phase of the LHC clock remains stable with respect to the bunch arrival times. However, several effects such as temperature variations influence the phase. Measurements show that the time drift on the transmission fibres could be as large as 200ps over a period of 24 hours, and up to 8ns have been observed over a period of a year (Figure 1[2]). Clearly the phase must be monitored and regular timing alignments must be performed. The TFC system provides several means of making a complete timing alignment at the level of 50ps.

In order to monitor the bunch arrival times with respect to the bunch clock a Button Electrode beam pickup (BPTX) [3] has been installed 146m away from the LHCb interaction point on each side for exclusive use by LHCb. In order to be largely independent of the position of the beam, the pulses of the four buttons of each pick-up is summed. As a result the current of the individual bunches may also be measured. This is of high interest since it allows monitoring the LHC bunch structure to detect possible ghost or displaced bunches, and will be of great help in the coarse timing alignment of the experiment. This also is of particular interest in LHCb since the interaction point is off the nominal interaction point by 7.5m and will therefore have single bunch crossings also.

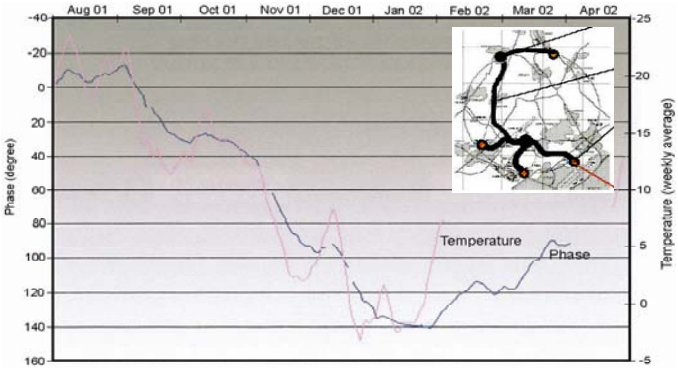

Figure 1: Effect of temperature variations on the clock distribution fibres [2].

The individual intensity measurement also allows checking the bunch intensities against the actual physics triggers and therefore allows verifying that the trigger and the detector front-ends are correctly synchronized. Directly interfaced to the Timing and Fast Control system of LHCb the information may also be used to produce a bunch crossing trigger or a gate for special running modes.

II. Beam Pick-Up and Signal Transmission

Out of the 1158 beam pick-ups of the Button Electrode type around the LHC, two have been installed per experiment for local beam monitoring (Figure 2). The pulses from the four buttons are summed giving the total amplitudes presented in Table 1 for three different beam scenarios. The pulses are bipolar with a typical length of 2ns (Figure 3 and 4).

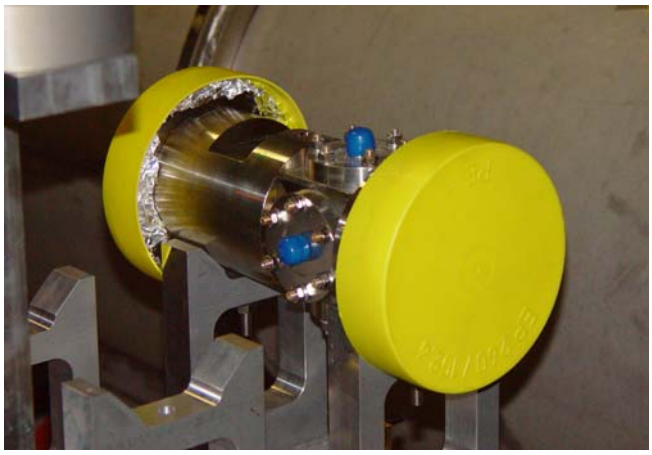

Figure 2: Picture of one of the two Button Electrode beam pick-ups at LHCb

Table 1: Expected total signal levels in three different beam scenarios at injection (450 GeV) and in physics mode (7 TeV).

Beam intensity (ppb)	BPTX [V]		200 m CMA50 [V]	
	450 GeV	7 TeV	450 GeV	7 TeV
Pilot ($5*10^9$)	-1.3 / 2.2	-1.7 / 3.7	-0.6 / 1.2	-1.2 / 2.4
Year 1($4*10^{10}$)	10 / 18	-14 / 30	-4.4 / 9.6	-10 / 19
Nom($1.15*10^{11}$)	-29 / 51	-39 / 85	-12 / 28	-30 / 55

The pick-up signals from the two BPTXs around LHCb (BPTX.5L8.B1 and BPTX.5R8.B2) are transmitted to the counting houses in LHCb by means of a ~200m Nexan ½" CMA50 coaxial cable with a nominal attenuation of 3.3dB/100m at 160 MHz and 5.9dB/100m at 450MHz. Table 1 gives the expected total signal amplitudes before and after the cable for three different beam scenarios. The bunch length is assumed to be σ_{beam} = 375 ps at 450 GeV (injection) and σ_{beam} = 250 ps at 7 TeV (physics beams) and the shape Gaussian.

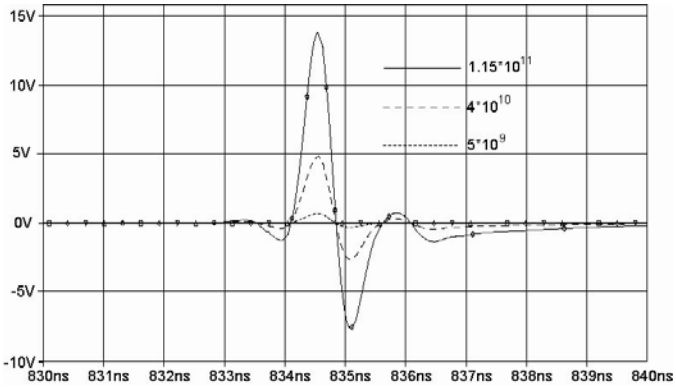

Figure 3: Expected signal for single button after 200m of the transmission cable in the three beam scenarios at 7 TeV.

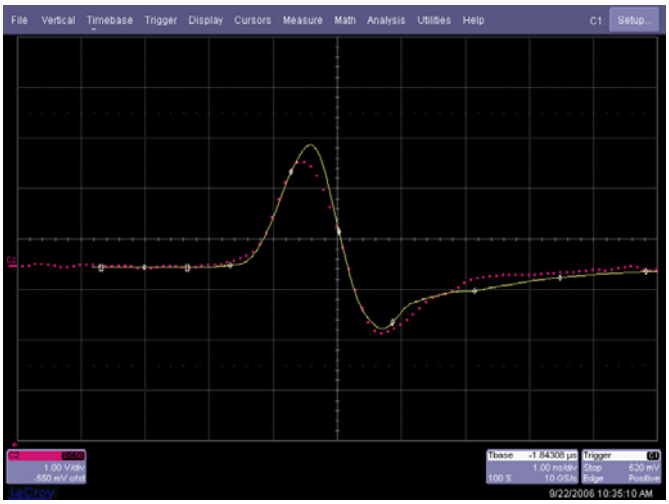

Figure 4: Pspice simulation of the signal pulse from a single Button Electrode including cable compared to a real pulse from a provisory pick-up at the CERN-SPS.

III. Acquisition Board

The acquisition board consist of a custom-made 6U VME board, currently one board per beam. The block diagram is shown in Figure 5. The analogue unit of the board consists of a separate circuit for the phase measurement and the intensity measurement. The board performs the intensity and the phase measurement continuously at 40 MHz and outputs the intensity information on the front-panel. Accumulation of data for all bunches of a full LHC turn (3564) may be triggered via the controls interface and synchronizes on the following LHC orbit pulse. The information may then be read-out via the control interfaced, processed, and used in the monitoring of the experiment.

Logically the device may be divided into the following blocks:

- clock adjustment and distribution,
- input pulse normalizer and buffer,
- intensity measurement circuitry,
- phase measurement circuitry,
- digital processing and data accumulation,
- I/O interfaces,
- and board control

A. Clock Distribution

The logic of the entire board is solely driven with the LHC bunch clock and the orbit signal. The LHC orbit signal serves as a reference for the accumulation of data for one full LHC turn. The bunch clock is AC-coupled and properly reshaped at the input. Since the analogue signal from the beam pick-up and the bunch clock are tightly coupled in the time domain, the relative phase of the two signals at the inputs has to be carefully adjusted once and for all. In order to start out with a maximum available range for a negative/positive phase shift, the best location for the beam pick-up pulse is in the middle of the clock period.

The clock adjustment is accomplished by means of three cascaded active delay lines (ONSEMI 100EP196). Together they cover the entire clock period and the delay is completely programmable via the control interface.

The delayed clock train is distributed by means of a clock fan-out to all the crucial nodes of the module:

- ADC sampling clock
- TDC reference clock
- TDC start clock (bunch clock divided by eight)
- Main and Auxiliary (VME interface) FPGA base clocks
- Intensity FIFO write clock
- Phase FIFO write clock
- Local Bus clock (bunch clock divided by two)

The distribution is entirely based on differential LVPECL. The discharge circuit of the integrator is driven by the bunch clock as well on a separate output of the fan-out.

B. Analogue Signal Input Stage

Due to the very large range of amplitudes in the different beam scenarios, the intensity measurement circuit contains an attenuator at the input of the pick-up signal with two different attenuations, one for pilot and the first year of beam, and the second for the nominal beam. The attenuator stage is meant to

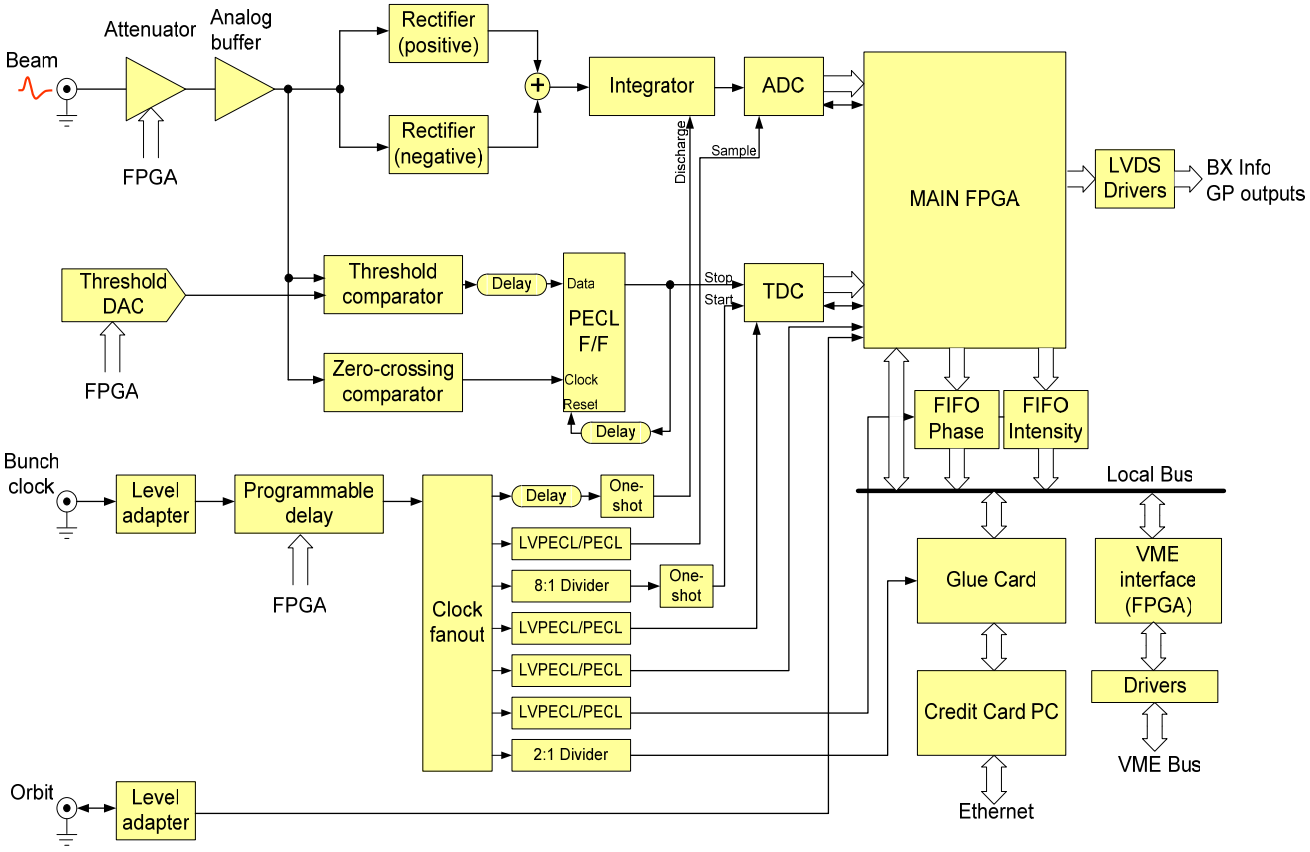

Figure 5: Complete block diagram of the Beam Phase and Intensity Monitor.

normalize the incoming analogue pulse to an amplitude of approximately +5V. The two different ranges of amplitude normalization may be changed by means of changing a resistor if needed. The ranges are switched via the control interface with the help of special RF relay from Omron. The output from the attenuator stage (THS3201 Operation Amplifier) is buffered by an ultra-fast unity gain device (LMH6559).

C. *Intensity Measurement*

In order to measure the intensity of the individual bunch crossings the entire area of incoming bipolar pulse is integrated. Thus the output from the unity gain buffer is passed through a full-wave rectifier. To achieve symmetry, both halves of the pick-up pulse are rectified by identical but individual active circuits, one of which acts on an inverted primary pulse. The outputs signal from the two rectifiers are summed and passed to an active integrator.

The accumulated charge is constantly sampled by a 12-bit A/D Converter (AD9432) preceded by an ADC Driver (AD8138) which makes the data acquisition mode differential. The converter is equipped with an ultra fast on-chip track-and-hold circuit. The amplitude from the integrator is sampled by the ADC on the rising edge of the *Sample* pulse which is a replica of the bunch clock. The ADC pipelines the samples meaning that, on every sample edge, the ADC outputs the data of the sample taken ten clock periods earlier. The output data is immediately read by the FPGA.

Two nanosecond after the rising edge of the bunch clock, the integrator is discharged with a 2.5 ns resetting pulse which closes an RF MOSFET transistor.

A simulation of the intensity measurement circuit is shown in Figure 6.

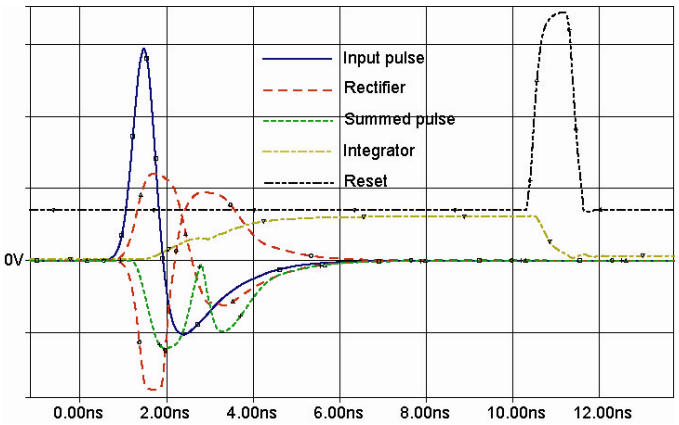

Figure 6: Pspice simulation of the intensity measurement circuit.

D. *Phase Measurement*

The heart of the phase measurement circuitry is an ultra-high performance 8-channel Time-to-Digital Converter from Acam (TDC-GPX). The current design uses the “R” operational mode in which the TDC may operate in a multi-hit mode at 40 MHz with a resolution of 27 ps over a period of 10 µs. The TDC works in a retriggered manner in which the start signal is supplied every eight bunch clocks at its rising edge. The stop pulse is formed by a zero-crossing discrimination of the attenuated analogue pick-up signal. Low amplitude parasitic pulses are eliminated with the help of a programmable threshold provided by a DAC. A simulation of the phase measurement circuit is shown in Figure 7.

Although it is known that the zero-crossing point is not fully suitable for a high precision reference of the bunch passage, this method was chosen for the first version. The zero-crossing point varies slightly with bunch length and shape and may vary up to 100ps between injection and start-of-physics.

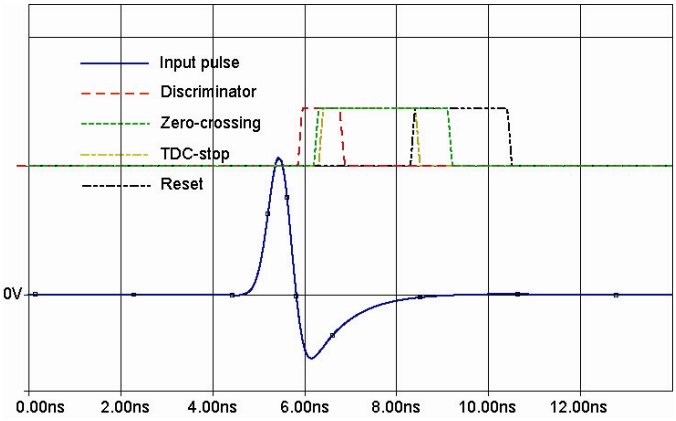

Figure 7: Pspice simulation of the phase measurement circuit.

E. Digital Processing

The digital processing of the board is performed by an FPGA (Altera APEX20K200EQC240-1X). The FPGA reads out the ADC and TDC continuously and performs linearization of the converter characteristics.

The FPGA subsequently outputs the intensity measurements as compressed on either eight or four-bits as LVDS. It may also be programmed with a digital threshold to output a "bunch crossing trigger" or any type of signal needed on the general purpose outputs

Data accumulation of the intensity measurements and phase measurements is triggered via the control interface. The FPGA synchronizes the accumulation to the orbit signal and fills simultaneously the two quantities for each bunch in two FIFOs for 3564 (full LHC turn) consecutive bunch crossings.

The FPGA also provides full control of the attenuator selection, the discriminator threshold, and the programmable clock delays via the Local Bus (see next section).

F. Board Control

In LHCb the electronics boards will all be controlled from the overall Experiment Control System (ECS). In order to access the actual board resources, an ECS interface will be located on each board. The ECS interface is connected to the control network and performs directly all device programming, configuration, control and monitoring of each electronics board. The BPIM is equipped with the same interface as all the electronics in the LHCb counting houses behind the shielding wall. It is based on a commercial Credit Card PC (CCPC) with Ethernet from Digital Logic, AG, Switzerland [4].

All the board resources are accessed via the PCI bus of the CCPC. In order to facilitate interfacing to different types of board control buses, a small intermediate mezzanine card with "Glue logic" has been developed [5]. The glue card is connected to the PCI bus and forms a standard set of simple interfaces needed by all the different electronics boards, such as a parallel 32-bit Local Bus, I^2C, JTAG and an 8-bit General Purpose I/O interface.

The configuration of all the functions implemented in the main FPGA is controlled via the 32-bit Local Bus, including access to the programmable clock delay, the attenuator selection and the discriminator threshold. The data accumulation is also triggered via the Local Bus, and the Phase and Intensity FIFOs are read out via the Local Bus. I^2C is only used to access an onboard memory storing the board identifier.

The main FPGA and its configuration device may be programmed via JTAG directly from the CCPC. The VME interface FPGA is programmed using an onboard JTAG header

Alternatively, a VME interface has been implemented onboard in an auxiliary FPGA to allow the device to be used in a VME-based control environment. It is directly interfaced to the Local Bus of the board. In this environment the configuration device for the main FPGA may only be programmed via an onboard JTAG header.

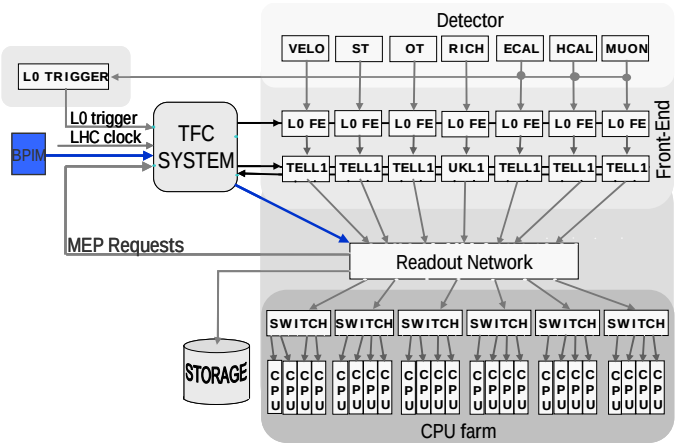

Figure 8: Overview of the LHCb online system with the BPIM interfaced to the LHCb readout supervisor "ODIN" in the TFC system allowing the bunch crossing information to be used in the control of the trigger and to be included in the event data.

IV. Conclusion

The current paper proposes a beam phase and intensity acquisition board (BPIM) for the Button Electrode beam pick-ups installed at each of the LHC interaction points for the experiments. The acquisition board is capable of performing simultaneously measurements of the individual bunch intensities with a 12-bit resolution and the bunch arrival times with respect to the LHC clock with a precision of approximately 100 ps at 40 MHz. In addition to reading out the measurements via the control interface, they are also output on the front-panel of the board at 40 MHz. The latter allows directly interfacing the board to the Timing and Fast Control system of LHCb (Figure 8) in order to add the bunch current information to the data of each event. It also allows the information to be used in the control of the trigger and as a bunch crossing trigger/gate.

V. Acknowledgements

We would like to thank Rhodri Jones and Eva Calvo Giraldo in the CERN-AB/BI group for their help in understanding the Button Electrode beam pick-ups and providing us with a simulation model of the buttons. We would also like to thank Greg Kasprowicz who started this project as a summer student. Last we would like to thank Thilo Pauly for useful discussions and real data from a provisory pick-up on the CERN-SPS.

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Proposal for a First Level Trigger using pixel detector for CMS at Super-LHC

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Abstract

A proposal for a pixel based Level-1 trigger for the Super-LHC is presented. The trigger is based on fast track reconstruction using the full pixel granularity exploiting a readout which connects different layers in specific trigger towers. The trigger will implement the current CMS High Level Trigger functionality in a novel concept of intelligent detector. A possible layout is discussed and implications on data links are evaluated. Finally the performances are shown.

I. Introduction

The CMS collaboration [1] at the LHC is currently in the final stages of construction and commissioning of the CMS detector and an intensive effort is being devoted to finalize the online and offline software required for data taking and analysis. LHC will start its operations in Summer 2007 and will increase its luminosity to the design limit of 10^{34} cm^{-2} sec^{-1}. However, to further continue the investigation of exotic rare phenomena and to assess the properties of new particles possibly found at LHC, upgrades are being foreseen that would increase the luminosity up to a maximum of 10^{35} cm^{-2} sec^{-1}[2], with a collision frequency of 80 MHz, and have the same centre of mass energy. This second phase of LHC operations is called Super-LHC (SLHC). The increased luminosity will require a general redesign of the existing experiments in order to cope with the increased number of particle fluxes into the detector elements.

II. Trigger at SLHC with the Tracker Detector

In the CMS design, the First Level Trigger (FLT) will filter the 40 MHz input rate of proton-proton crossings down to a maximum of 100 kHz of accepted events. The trigger is based on a set of specialized processors working on small subsets of the calorimeter and muon chamber information. The next selection step, the High Level Trigger (HLT), will receive, on average, one event every 10μs. In this time the rate must be reduced to 100 Hz, which is the estimated bandwidth that can be put on tape.

At SLHC luminosity there will be about 100 proton-proton collisions occurring every 12.5 ns, in contrast to only 22 collisions for normal LHC operations. This would correspond to about 10 billions of collision events per second, to be compared to the rare physics phenomena which will occur at about few Hertz or lower. Each proton bunch crossing will generate much more than the present 1MB of data, and the expected data transfer to disk will not exceed the rate of about 100 Hz. Hence, the increased luminosity will also require a drastic revision of the existing trigger strategies.
As an example, Fig. 1 shows the rate of the single muon trigger as a function of the muon p_T threshold [3]. The performance at FLT suffers from poor transverse momentum resolution at high p_T. The use of the Tracker information at HLT (labelled as Level 3 in Fig. 1) allows a drastic change in the slope of the rate.

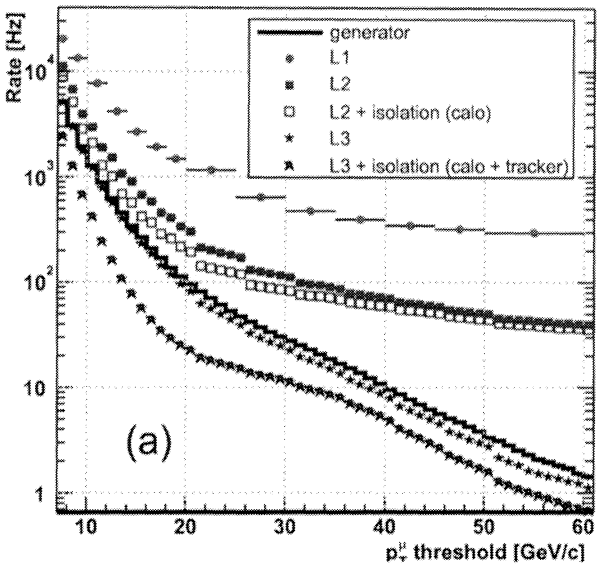

Figure 1: The FLT and HLT single-muon trigger rates as a function of the p_T threshold. The rates are shown separately for Level-1 and HLT (Level-2, and Level-3), with and without isolation applied at Levels 2 and 3. The rate generated in the simulation is also shown.

Due to the shape of the underlying background distributions, the required FLT rate reduction for SLHC cannot be achieved by increasing the redesigned FLT thresholds, even if one is willing to pay the price of cutting useful physics. Gain in background reduction can only come from improving the FLT algorithms for selection of physics signals. Furthermore at the SLHC the FLT efficiency and purity to select Higgs and other exotic signals will degrade due to the increase of the minimum bias events by at least a factor of 5. Given that the current FLT design already uses information from all detectors but the silicon tracker, any improvements in background reduction efficiency and purity can only come by including tracking information at the FLT. Hence, the need for a First Level Tracking Trigger.
Using tracking information at the FLT algorithms will more than compensate for the factor of 5 increase of the backgrounds. The largest benefit is obtained by using the tracks/hits and vertices found by the vertex detector, which in turn creates severe challenges for any tracking trigger due to the stringent constraints in terms of power, radiation hardness and data volume and speed.

III. Tracker Trigger Strategy

The basic idea which drives the FLT based on Tracking is to port as much as possible what HLT Tracking has shown feasible now [3], and design new algorithms reflecting tracking trigger capabilities.

The proposed trigger strategy will influence the layout of the tracker detector and *viceversa*. The requirements on the hardware are, however, minimal. The proposed strategy makes use of binary readout of the front end electronics, followed by transfer of the full granularity data using fast and radiation hard fibers to the barracks where dedicated processors will reconstruct tracks.

The tracking trigger aims to provide tracks above a given momentum threshold that could be matched with FLT muons or electrons in the Global Trigger.The most important feature of the trigger, relies upon the usage of established detector and electronics technologies to get a robust project stretched beyond the current limits thanks to the miniaturization of the electronics. That implies using the current hybrid pixel technologies [4] for the sensors, expand existing Tracking Triggers (SVT) [5] based on the use of Associative Memories chips[6] and finally making use of more radiation hard optical fibers technologies.

In particular, as far as the logic running the tracking algorithms in the barracks is concerned, the proposed system is an evolution of the Silicon Vertex Tracker (SVT) built for the CDF experiment, at the Tevatron Collider, where real time tracks are reconstructed. The implementation that is envisaged here, is mainly used for best momentum reconstruction.

A. Design considerations

The main usage of a Tracking Trigger is for reconstruction of particles exceeding a given transverse momentum (p_T) threshold. What is therefore needed are detectors with low occupancy (based on pixelized detectors) providing sufficiently distant measurements, rather than brilliant space-point resolutions. Equipping large areas with small pitch detectors is cost demanding, hence a compromise between the two requirements should be found. The charged track multiplicity at SLHC is foreseen to be about 600 tracks per rapidity bin, hence a good pattern recognition is required. If the Tracker material budget will not decrease by a sizeable amount, then multiple scattering will drive the momentum resolution below about 10 GeV/c hence a point resolution of no better than a few tens of microns is needed in the $r-\phi$ coordinate to determine the momentum with about 10% precision for order of half a meter lever arm.
To limit the amount of data to be transferred to the Trigger logic, a binary readout for each channel is proposed. To profit of the best pattern recognition we assume that full granularity pixel data is available for processing. This assumption is the real challenge of the proposed trigger strategy and dictates the more serious requirements on the hardware as well as on fast links to transport the data to the FPGAs in the barrack. In addition, the same data links as of the data readouts could be used for trigger signals, avoiding duplication of fibers. In order to cope with the large data volume to be processed, the proposed approach makes use of the information coming from the radial region from 25 to 50 cm, that shows radiation levels where current hybrid pixel technologies and optical fibers could work without challenging technological efforts. The large radius would in addition provide the large lever arm required for momentum measurement, with the addition of the precise beam spot information in the r-ϕ plane.

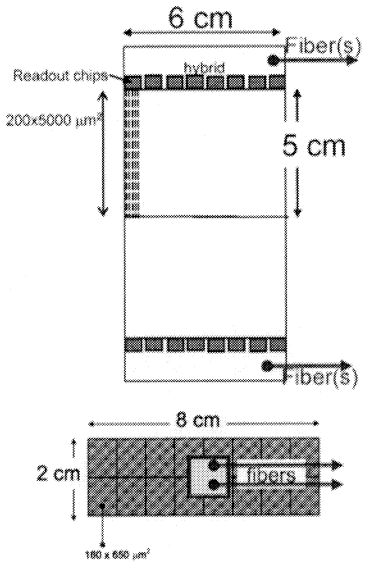

Figure 2: Module for the outer (up) and inner (low) radius layers.

B. Tracker Layout

In the current proposal, for sake of simplicity, only a barrel region is considered, covering the pseudorapidity region of $|\eta| < 1.5$. The considered Tracker Trigger region is composed by four layers at radii of 26, 34, 42, 50 cm from the beam line, at exactely the same locations as the present CMS Silicon Strip Inner Barrel (TIB)[8]. All problems linked to the mechanics, cooling or silicon sensor technologies, go beyond the scope of this contribution. It is sufficient to state that in this region, both the radiation hardness as well as services will not be as dramatic as in the layers below 15 cm radius, and is widespread belief that would not be insormountable technological problems.

Following a proposal from R. Horisberger[4] the innermost layer of the four, is equipped with hybrid pixel modules of dimensions of about 2 (r-ϕ) $\times$ 8 (z) cm^2 and composed of 16 readout chips (2 in r-ϕ and 8 in z),as they are in the current CMS design. The cell dimensions, however, will be 200 (r-ϕ) $\times$650 (z) μm, in order to allow for reduced costs in the bump-bonding. At a radius of 25 cm there will be about 14 modules in each ladder in z and 80 modules in azimuth. The other three layers will be equipped with large elongated pixels of 200 (r-ϕ) μm $\times$ 5 (z) mm and a sensor area of 6 (r-ϕ) $\times$ 12 (z) cm^2. A possible layout of the modules is sketched in Fig. 2. Each module is equipped with radiation hard fibers and laser drivers having the largest speed as possible. For fiber lengths of about 100 meters (the distance from the modules to the barracks) the VCSEL technology is already able to provide radiation hard fibers with about 2 Gbps[9], with a power consumption of about 1W. It is not impossible that R&D will deliver a speed of 4 to 5 Mbps radiation hard fiber technology in a few years time, in time for

SLHC.[7] As previously stated, the real problem in the proposal is to make such a large amount of data available to single tracking processors in time. The input bandwidth sets and upper limit either on the event rate or on the size of the detector connected to it. We envisage to send data to the trigger exploiting a parallel readout of the detector layers on four buses. Nevertheless, in order to sustain very high event rates, it is necessary to organize the tracking processor as a set of independent engines, each working on a different sector of the silicon tracker. The detector will be divided into azimuthal sectors. Each sensor of every layer in the sector will send the information to the specific engine working on it, located in the barrack, which will combine the information from at least 3 layers out of 4 to determine the track momentum with a resolution better of about few (<10)% at 10 GeV/c.

The sector granularity has been chosen taking into account the minimum measurable p_T for triggering purposes, without efficiency loss. The innermost layer is divided into about 80 azimuthal sectors, matching the width of a module. This width well covers the bending of a track of 5 GeV/c p_T and above.

Table 1: Layout of the pixel layers, giving the radius from the beam line, the number of modules is z and r-ϕ.

Radius (cm)	No. Modules in z	No. Modules (sectors) in r-ϕ
26	14	81
34	9	36
42	9	44
50	9	52

The number of sectors in the three outermost layers will also follow the sensors widths. Table 1 shows the number of modules per sector in each layer. 20 bits will be sufficient to locate any hit in each layer of the sector. In the barrack, the hit information from suitable overlap regions of neighboring sectors could be sent to more than one engine to decrease efficiency losses in the boundaries between sectors.

C. Simulation results

The results are based on about 3000 minimum bias (MB) events and 250 top events generated with Pythia 6.227 with default settings. Chunks of 100 MB events have been passed through a complete GEANT4 simulation of the Tracker detector and digitized and the resulting occupancies are studied. Table 2 shows the expected mean and rms number of hits per sensor per bunch crossing (12.5 ns) in the different layers. It is important to notice that the largest contribution to the occupancy comes from the primary tracks. In case of $t - \bar{t}$ events at SLHC, the largest increase in the occupancy is smaller than the rsm of the hit rate coming from MB events. The largest hit rate per module occurs at the second layer with an average of 8.5 hits/sensor. The large fluctuations occurring in the module occupancy could be accomodated by using pipelines in the readout electronics.

Table 3 shows instead the data rate traffic on the fibers (using 20 bits/hit encoding) together with the estimated number of fibers per layer, with the assumption of a fiber link speed of 5 Gbps. It is noticeable that the required amount of fibers is comparable (and even smaller) of the current CMS Inner Tracking Barrel (2000 in the innermost layer and 2600 in the second layer), giving confidence that such a system will not become more complex even in the case of lower speed links. The power density contribution from the laser drivers is estimated to be of the order of 60 mW/cm^2 in the innermost layer, that has the largest density, to be compared with about 200 mW/cm^2 for the current CMS pixel electronics.

Table 2: Mean and rms number of hits in each module and layer per bunch crossing (12.5 ns) in Minimum Bias events.

Radius (cm)	No. hits/module/bx (RMS)	No. hits/sector/bx
26	3.1 (1.4)	43
34	8.5 (4.5)	78
42	5.3 (3.5)	49
50	3.7 (2.0)	34

Table 3: Mean data rate per each sector every bunch crossing (12.5 ns) in Minimum Bias events, together with the number of fi bers needed to bring the signal out (5 Gbps speed).

Radius (cm)	Data rate per sector/bx (Gbps)	No. data links/layer
26	69	1100
34	125	900
42	78	700
50	55	600

IV. Dimensioning the Tracker Trigger Hardware

Each engine working on a particular ϕ sector, located in the barracks, will receive the hits from each layer and will produce track candidates. We propose to implement the engine with an associative memory chip (AM chip) where a set of all possible tracks exceeding a given p_T cut and originating from a certain luminiosity region compatible with the beam spot, has been previously loaded. Tracks are pre-calculated taking into account multiple scattering. These are referred as banks of patterns. Each stored hit pattern is provided with the necessary logic to compare itself with the event. The AM pattern bank is limited by the size of the hardware, mainly consisting of low-density content-addressable custom memories. The size of the bank pattern depends on the number of detectors in each Trigger sector and on their granularity. The estimated number of patterns to be stored for the current proposal is about 25,000 for a lower momentum cut of 5 GeV/c. This is compatible with the capacity of a next generation single chip.

The AM chip used in SVT has about 5000 patterns for 6 tracking planes in UMC 0.18 μm CMOS 1P6M logic by IMEC [6]. Once developed in 90 nm technology, each AM chip could accommodate about four more patterns. The same memory can be reorganized to fit 30,000 patterns for 4 triggering planes.

The current AM chip runs at 50 MHz with 6 parallel buses of 18 bits encoding each. The future evolutions of the AM chip will run at 100 and 200 MHz, so each one is expected to support a rate of 3.6 Gbps while the largest flux from the second layer is about 40 times larger. In order to be able to run in such

conditions, we envisage that the flux coming from the detector is sent to a switch that distributes the hits coming from the detector into different sets of storage units depending on the event number, enough to store up to 40 events at the same time. In this way 40 AM chips will work in parallel on different events, being able all together to sustain the input rate, 40 times larger the input bandwidth of a single chip. Figure 3 shows a conceptual design of the Trigger Logic.

About 80 boards with 40 AM chips each will be required, for a total of about 3200 chips. The current cost of a batch of 3000 AM chips in 0.18 μm technology (which has a yield of about 75%) is 30K$.

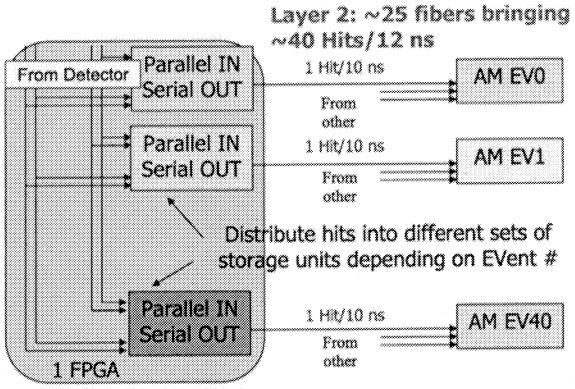

Figure 3: Conceptual design of a possible Tracker Trigger logic using a switch that distributes hits coming from the four pixel layers in a Trigger sector to 40 Associative Memories, one per each event.

The latency budget for a FLT at SLHC is 256 bunch crossings. In the current layout a fair fraction of the latency unavoidably comes from the fiber length of about 100 meters, which corresponds to about 25 bunch crossings. The biggest component comes from the swicth and the AM which are estimated to take about 80 bunch crossings. In order to cope with the allocated budget the detector readout electronics should be executed in less than about 80 bunch crossing, allowing for number of hit fluctuations in the detectors and a margin for the Global Trigger to be executed. This limit does not seem impossible to achieve with existing technologies.

V. Results and Conclusions

A fast estimate of the Tracking Trigger capability has been developed taking into account its possible use together with a single muon FLT. The effect is shown in Fig. 4, where a sizeable reduction is visible at p_T larger than 10 GeV/c, and even lower. The results are preliminary, but as can be seen, the immediate benefit of the usage of a First Level Tracking Trigger combined with muons will bring the single muon rate to a level of about 10 KHz at 10 GeV/c muon p_T.

Further studies are required to evaluate possible other applications as well as complete implications both in electronics and in power density.

This work has shown that a first level trigger based on full granularity information of four barrel layers is feasible. The trigger is capable to reduce the FLT rate to manageable levels to be further scrutinized by HLT algorithms running in the filter farms.

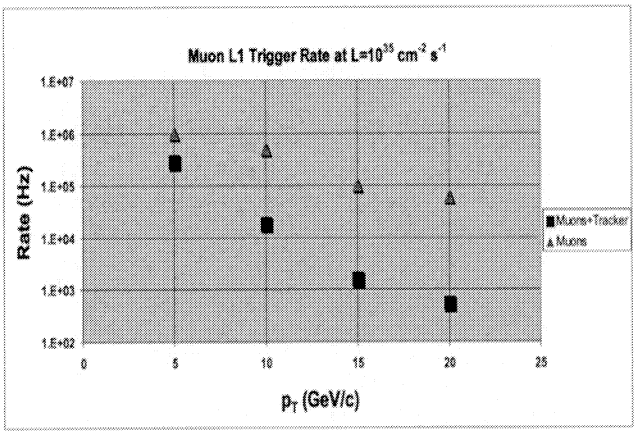

Figure 4: First Level Trigger Rate for single muons at SLHC as a function of the measured Muon p_T. Triangles show the estimated rate from the Muon system alone, while squares show the combined Muon plus Tracker First Level Trigger.

VI. Acknowledgments

I wish to thank the Conference organizers for having accepted the contribution and the fantastic venue. This talk could not have been possible without useful interactions with Paola Giannetti, Marcel Vos, Mauro Dell'Orso, Roland Horisberger and Francois Vasey.

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Stacked Tracking for CMS at Super-LHC

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Abstract

We report recent work on the design of a pixel detector for CMS at the Super-LHC. This work builds on previous studies of a tracking detector capable of providing track stubs to be used in the Level-1 Trigger (L1T). We now focus on the use of two 'superlayers' of tracking; each comprising a pair of pixel sensors with $50\times50\times50\mu m^3$ pitch ($z\times\varphi\times r$) separated by a few millimetres. Preliminary work on track reconstruction in Field Programmable Gate Arrays (FPGAs) is also presented.

I. Overview

The current design of CMS is based on the nominal beam luminosity $10^{34}cm^{-2}s^{-1}$. It is anticipated that after running for several years, both LHC and the detectors will be upgraded to operate at a luminosity of $10^{35}cm^{-2}s^{-1}$ [1]. This presents a great challenge both in terms of radiation hardness and the increased data rates that will have to be sustained by the detectors and their corresponding DAQ systems.

The background to these issues and the stacked tracking principle were presented in LECC 2005 [2,3], and only a summary is stated here for completeness. Apart from jet vetoing by multiplicity, the simplest useful tracking contribution is a stub from two consecutive barrel layers. The stub can be used in coincidence with the outer detector to indicate whether the hit in the outer detector was caused by a high-p_T particle. The quality of the stub (i.e. whether the hits are matched correctly between the two layers) is dependent on the layer separation; for layer separations of greater than a centimetre (see figure 1), tracks from different events will overlap, producing a large number of track combinatorials during reconstruction.

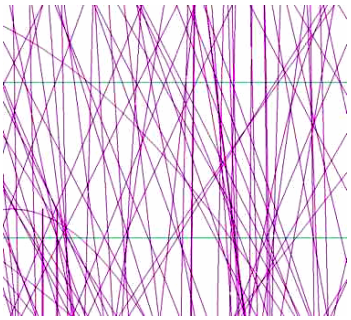

Figure 1: Track overlap in y-z plane (detector coordinates – see Fig. 3). 1cm layer separation is denoted by the two cyan lines. Note the significant overlap of tracks between these two layers, which will hinder tracker reconstruction.

An alternative approach to the combinatorial problem involves bringing two pixel layers together (hereafter refered to as a stack) so that they are separated by a few millimetres. The combinatorials then become manageable; even the limited knowledge of the interaction point is sufficient to make a 1:1 match between many of the hits in the two layers. This enables fast reconstruction using simple binning techniques, which could be implemented in an FPGA off-detector or a radiation-hard ASIC on-detector.

The basic layout of a stacked pixel detector is shown in figure 2. In order to ensure that the signal efficiency is high, the design is hermetic using overlapping segments of detector.

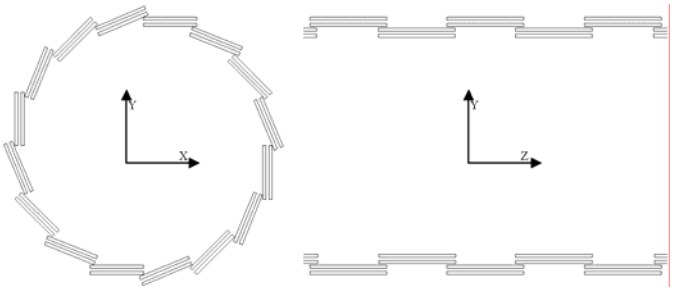

Figure 2: Basic layout of a stacked tracker (not to scale). Left is an x-y view, right is a y-z view.

The single stack approach, while useful for reducing the on-detector data rate, results in several complications. Firstly it increases the material budget in the inner detector; while this can be mitigated with modern materials [4], this is a trade-off that will have to be considered in the design of any new pixel system.

The second issue is fundamental to the stack design. As stated in [2], the ability to cut on transverse momentum by difference analysis of column pixels comes at the price of a lack of ability to actually measure p_T. This follows from the close proximity of the stacks, reducing the lever arm to such and extent that neither transverse momentum nor charge are measurable.

Tied to the ability to measure p_T is the ability to correctly project a track onto a calorimeter trigger tower [5]. While this was previously shown to be possible for particles with transverse momentum greater than approximately 20GeV, the lower momentum particles that are passed through the correlator ASIC are indistinguishable from the higher momentum ones. This results in a potentially serious inefficiency and also results in a high rate of ghost states.

A. The Double Stack Method

The latter issues can be either resolved or at least improved upon by the use of more than one stacked detector. The principal benefit of a stack is the massive reduction of data-rate before leaving the detector. By using two sets of stacked sensors or 'superlayers', one can still benefit from the rate reduction in each individual super-layer by using a geometrical p_T cut, but can also reconstruct stubs in a similar way to a more traditional pixel detector .

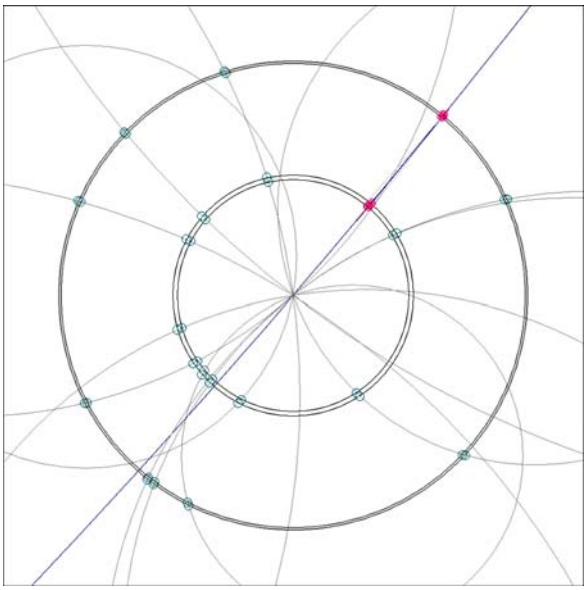

Figure 3: A double stacked detector. One of the layers is placed at a radial distance of 10cm from the beam pipe, and the second super-layer is placed 20cm from the beam pipe.

An example of this detector configuration is shown in Figure 3. For reasons that will later become apparent, the pixel pitch has been relaxed to $50\times50\times50\mu m^3$. While a finer pitch is preferable it is no longer strictly necessary, and larger pixels are easier to design. The inner super-layer is placed at r=10cm with a layer separation of 4mm, while the outermost layer is located at r=20cm with a layer separation of 2mm. The difference in layer separation compensates for the different radii, making the p_T cuts similar for each superlayer (approximately 3GeV).

The fundamental benefit of this design over those previously proposed is that it requires no on-detector communication between the superlayers. Interlayer communication is a crippling limitation of any design due to the limited space available for services and the additional power consumption of interconnections between widely-spaced layers.

B. Double Stack Reconstruction

The reconstruction method for a double stack configuration is similar to that for a single stack (Figure 4). One significant difference is that the performance becomes more significantly affected by the z pitch of the pixel than by the φ pitch. The reason for this is that the z-coordinate of the tracker hits is unaffected by the magnetic field from the solenoid and so the track follows a straight-line path in the r-z coordinate system. On the other hand the B field reduces the resolution of the track in the r-φ plane and therefore the search window for matching stubs between the superlayers becomes too large. While it is still used, the z-reconstruction becomes dominant and as a result, the reconstruction purity is determined by the intrinsic resolution of the sensor.

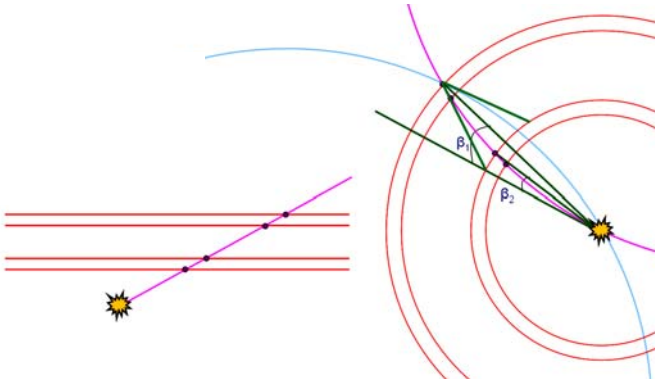

Figure 4: Double stack reconstruction. The track reconstruction in the r-z view is more accurate due to the parallel B field in that coordinate system. The back-searching method is still used in the r-φ plane as an aid, but is insufficient to pair hits on its own.

An additional benefit of this reconstruction is that it gives the precise location of the primary vertex for the event. It should be noted however that there will be an associated inefficiency due to the incorrect management of any secondary vertices, the detection of which is considered too difficult to implement in this design.

The estimated performance was calculated using a Monte Carlo simulation derived from the one used in [2].

C. Double Stack p_T Measurement and Track Projection

The projection of a reconstructed track in the r-z plane follows directly from the reconstructed track stub. However, to perform r-φ reconstruction requires the calculation of the transverse momentum. As the inner layer of each stack is very close to the outer layer, the transverse momentum can be calculated to the nearest approximation by using just one hit from each super-layer. The current implementation takes this approach although using both pixel coordinates would provide a small additional benefit, either by the use of linear interpolation or by more complex algorithms that weight the pixels optimally. Only the simplest case is considered here as the algorithm must operate efficiently in hardware.

As there are only two superlayers in this design, the beam spot must be used as an additional constraint. In the simulations described later in this paper, the following 3-point reconstruction equation is then used:

$$p_T = \frac{r_{out}^2 Bc}{8 r_{in} \sin(\Delta\varphi)}$$

Where r_{out} is the radius of the outer super-layer, r_{in} is the radius of the inner super-layer, B is the magnetic field strength in Tesla, c is the speed of light, p_T is measured in eV and Δφ is the angular separation between the hits in the two superlayers. This is an approximation relying on the layers being equidistant and can be optimised.

Once this value has been calculated the track can be projected onto an ECAL trigger tower for matching with detected hits, or forwarded to the muon system for matching with tracklets built using information from those detectors.

In simulation one can calculate the difference between the impact location of the reconstructed track and the 'true' track. Figure 5 shows the momentum resolution. Δφ is calculated as:

$$\Delta\varphi = \frac{p_T^{reco} - p_T^{real}}{p_T^{real}}$$

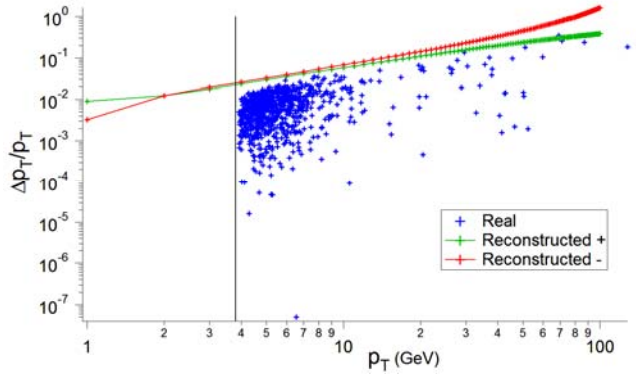

Figure 5: Resolution of reconstructed transverse momentum plotted as a function of real transverse momentum. The black line represents the reconstruction cut, the 'real' points are from simulation and the red and green lines represent the largest possible ±Δφ variation and therefore the worst-case momentum resolution.

For this example the momentum resolution is very good, increasing to approximately 20% at p_T = 100GeV. The approximately exponential degradation of resolution at 100GeV shown by the red curve is the result of the angular separation of the track approaching the intrinsic resolution of the pixel system. The reconstructed position resolution on the ECAL face in Δφ is shown in figure 6.

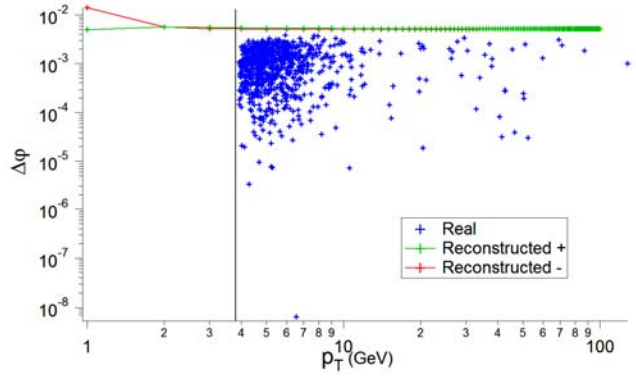

Figure 6: Reconstructed angular resolution at the ECAL-Tracker interface plotted as a function of real transverse momentum. The black line represents the reconstruction cut, the 'real' points are from simulation and the red and green lines represent the largest possible ±Δφ variation and therefore the worst-case momentum resolution.

This plot shows approximately flat behaviour over the p_T range of interest. At higher p_T the transverse momentum resolution becomes less important as the track becomes approximately straight, and therefore the position error, as for the transverse momentum case, becomes dominated by the intrinsic resolution of the pixels. In any case it should be noted that the error is far smaller than the size of an ECAL trigger tower, being approximately 0.003 radians, or 4mm when projected (this is in fact smaller than a single ECAL crystal).

The resolution in the z-direction can also be calculated, and is naturally better than for the transverse projection as it only depends on the pixel size and super-layer separation. Figure 7 shows the result for the geometry described previously. The worse case here is in the central region of the detector where the separation between the hits is smallest, and vice versa for the forward region. Even in the central region the resolution is approximately 0.001 in pseudorapidity or approximately 1.3mm, again far better than required.

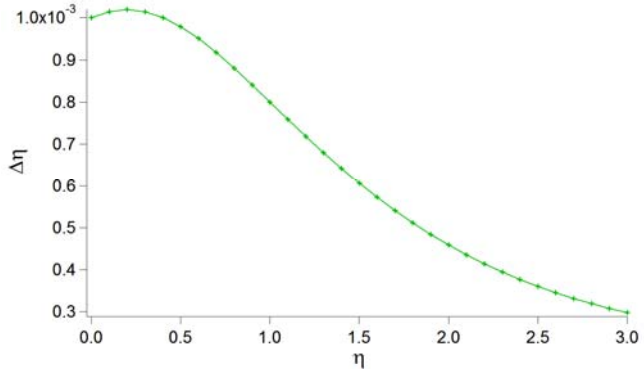

Figure 7: Reconstructed pseudorapidity resolution plotted as a function of hit location.

It is noted that the above methods do not take into account multiple scattering. Although such effects can be minimized by good detector design and low material budget construction, this will also need to be taken into consideration in the development of optimal algorithms. Full Monte Carlo studies for the purpose of testing such algorithms would be of limited value while the design of any future tracker (stacked or 'traditional') is still undecided.

II. Design Considerations

The use of two stacks introduces additional complications in the detector design. While the basic architecture of an individual super-layer remains relatively unchanged from that described in [2], the off-detector processing necessarily becomes more complex as one moves from a stub generator to a simplified form of track reconstruction. The requirement for more precise calibration of the correlation and compensation for mechanical alignment issues necessitates a more comprehensive on-detector processing solution.

A. Detector Structure

As discussed previously, a significant problem is the sensing element for the new detector. At a radius of 10cm from the interaction point the required radiation tolerance is 10^{16}p/cm^2, 300Mrad. This makes full depletion impossible using thick sensors. Furthermore a charge collection speed of

<5ns will be required if SLHC operates in an 80MHz bunch crossing mode.

In this paper a different approach to radiation tolerance is taken. As it is not clear whether a technology exists that can withstand this dose for several years, an alternative approach would be to use a 'throwaway' detector. In this case one should pick an industry-standard technology with proven radiation tolerance approaching but not necessarily meeting the level required to operate in the SLHC environment for several years. Monolithic Active Pixel Sensors (MAPS) [6] are one example of this kind of technology. Some cost studies [7] have shown that in bulk production the technology is significantly cheaper than the custom hybrid pixel technology currently used in CMS [8].

The use of a standard technology such as MAPS also affords the use of fabrication techniques such as stitching. In the design considered here this is taken advantage of to manufacture wafer-size sensors of dimensions 2x10cm^2. This allows one to reduce the material budget by minimising the amount of wastage caused by overlapping detector segments.

Another proposed technology is a lower material budget support structure such as carbon fibre–Kevlar laminates, as currently used in BaBar [4]. By using thin sensors and newer support structures it should be possible to minimise the impact of the new detector on the total material budget. A possible detector layout is shown in Figures 8 and 9.

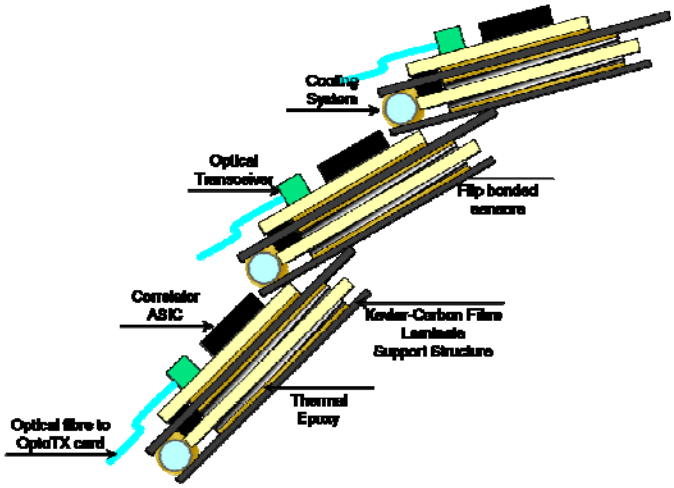

Figure 8: Possible detector structure for a stacked pixel array

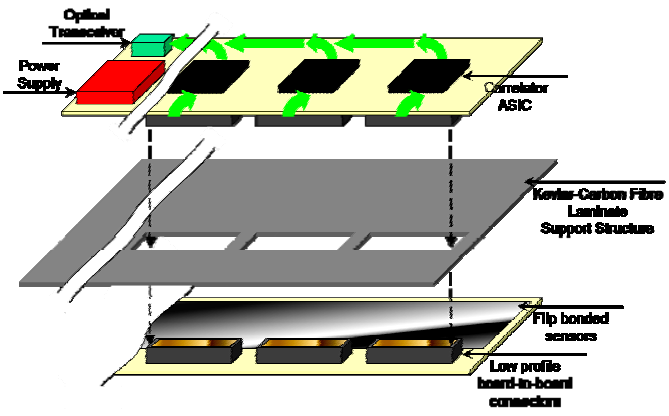

Figure 9: Possible stack-up for a stacked pixel array

While MAPS are a standard technology that offers good prototyping potential and low cost, one should be prepared to follow industry and change technologies if a superior cost-effective one becomes available. One example of this is 3D ASIC technologies [9].

III. Correlation Logic Implementation

It was shown in the previous study[2] that the correlation logic could be implemented using a difference analysis technique. While this is a good starting point, it results in two complications. Firstly it does not allow for calibration against the mechanical placement of the detector. This would be useful in order to compensate for fact that the detector is comprised of non-ideal flat segments, as opposed to being a perfect cylinder. Secondly the difference analysis relies on the beam spot location being at or close to r=0.

An additional gain (approximately a factor of four) in detector data rate can also be achieved by filtering in z, by loading calibration into each correlator and filtering in φ and z. It is now assumed that this processing and pixel clustering will be performed on-detector. By encoding only the clusters and the correlated pixel columns in φ rather than the absolute column address, it should be possible to reduce the data rate by a further factor of two. This would require the storage of 1024 calibration constants of 8 bits each for a 256x256 pixel array (8kb).

B. Track Reconstruction Implementation

Once the data has been processed by the correlators on the detector, the data is sent off-detector and drawn into SNAP12 fibre bundles at 40Gb/s/bundle, increasing the data density. By this means the data rate into the first stage of processing can be increased to approximately 200Gb/s/board using five SNAP12 receivers. Figure 10 shows the on-off detector data flow.

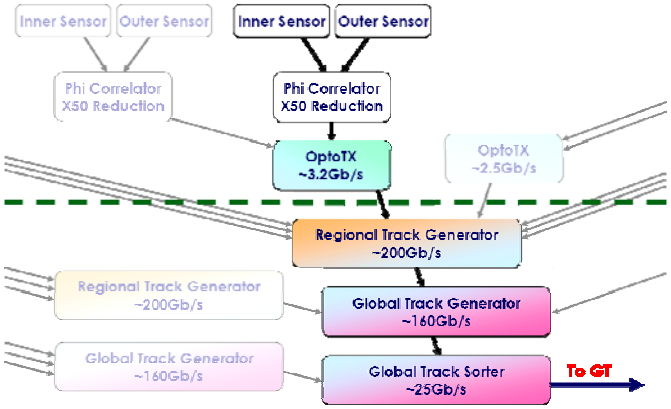

Figure 10: Illustration of different stages of data processing both on and off-detector. The top half of this diagram represents on detector electronics whilst the bottom half is off detector.

1) Regional Track Generator (RTG) – 200Gb/s

The first stage of reconstruction is managed by the RTG. Current firmware development has focused on this part of the system, and began first with an implementation of the correlator. This involves a combination of a column difference analysis and a z-binning method using constants

loaded into the internal FPGA RAM. In the final version of the firmware this is more likely to just use calibrated search windows for both sensor axes. Each RTG handles a single ring of sensors in the r-φ plane.

It is assumed that the data will be channelled directly into FPGAs on the RTG using the Multi-Gigabit Transceivers (MGTs) that are often integrated in modern devices. The Global Calorimeter Trigger Leaf Card [10] offers a possible prototyping platform for this board.

Implementation studies have shown that a serial correlator algorithm can be implemented that can pipeline-process hit pairs at 120MHz (~4Gbit/s/correlator), occupying approximately 0.8% of a Xilinx Virtex-II Pro 70 FPGA. In later generations of FPGAs this will operate at a higher clock speed and the algorithm itself will be further optimised in the future. It is unclear whether this part of the algorithm will be duplicated in the RTG or only implemented in the correlator on-detector.

The second purpose of the RTG is to pass paired hits in each super-layer forward to the Global Track Generator (GTG) for track building. The method used to achieve this is to project hits from the outer super-layer to the inner super-layer and subdivide the processing into pseudorapidity segments. For inner super-layer pairs the data in that segment is also forwarded to the same GTG. In this way all the possibly matching stubs naturally go the same card.

2) Global Track Generator (GTG) – 160Gb/s

The GTG finishes track building by pairing stubs from the two superlayers, calculating the transverse momenta for each track found and applying a second p_T cut at the detector level. The reduction in rate extrapolated from Monte Carlo studies is approximately a factor of forty, although this depends somewhat on the initial detector rate for each stack. Track candidates from this board are forwarded to the Global Track Sorter.

3) Global Track Sorter (GTS) – 25Gb/s

After the GTG the final rate decreases to a more manageable value. The card is responsible for housekeeping duties in this design and any final processing required. It also sorts the candidate tracks by detector region and measured transverse momentum. These candidates are then forwarded to the Global Trigger to be combined with track candidates from the Global Muon Trigger and hit candidates from the Global Calorimeter Trigger.

IV. Possible Detector Improvements

The double stack method described above shows several benefits over the single stack method, most notably the proper (albeit crude) calculation of p_T and accurate projection of tracks to the calorimeter.

The design still leaves questions of mechanical calibration. By using a correlation based on calibration coefficients it will be possible to compensate for non-ideal detector geometry and misalignment of the detector. It also offers the possibility of compensating for beam vertex misalignment in the r-φ plane. This needs studying and is not discussed further here.

V. Summary

It has been shown that the use of small layer separations in a pixellated detector system can be used to both reduce tracker combinatorials and reduce the data rate from the detector by means of a simple correlation algorithm. This algorithm could be implemented on-detector using relatively simple electronics; more advanced algorithms could be implemented off-detector in FPGAs.

By the use of more than one stack in several superlayers, the rate reduction can be achieved, and high-resolution track reconstruction and transverse momentum measurement also becomes possible. The design also provides a margin to compensate for real-world inefficiencies such as non-optimal resolution, malfunctioning pixels and system noise.

Our current work involves further development of the off-detector firmware and feasibility studies. Future work will require more refined simulation studies based on technologies such as MAPS. We are also considering a full-scale replacement of the tracker based on a minimum of four superlayers and new materials that can be used to reduce the material budget of the detector.

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Parallel Session A1

Readout, commissioning and integration

Overview of LHCb electronics installation aspects

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Abstract

The infrastructure for the electronics, such as cabling, mains power distribution, low and high voltage power supplies, detector safety system, grounding and its installation in the LHCb experimental cavern is presented. In addition, racks, cable ducts installation and optical fiber link tests are described.

I. Introduction

LHCb presents some particularities compared to other LHC experiments due to its geometry (forward coverage only). This geometry offers the advantage that most sub-detectors are constructed in two halves that can be opened for maintenance. Accessibility to the on-detector electronics is therefore reasonably easy and equipment such as power supplies can be installed relatively close to front-end electronics. On the other hand, the fact that sub-detectors can be opened implies specific constraints for cabling and grounding of sub-detectors.

A 4 meter thick shielding wall made of concrete blocks protects DAQ interface electronics and a large PC farm of ~2000 computing nodes against radiation. The PC farm and DAQ interface electronics are installed in racks in barracks on 3 levels (counting house). Cabling from sub-detector specific in/on detector front-end electronics to the protected counting house has lengths of 50 to 110 meters. The shielding wall acts as an important obstacle for all power, readout and control services that have to pass through a narrow chicane.

II. Racks

Two types of standard 19” racks are used in LHCb; one with standard vertical closed air flow for the front-end electronics and another with open horizontal air flow for the computing farm PCs. The front-end electronics racks (~50 units) use the common LHC turbine units, heat exchangers and deflectors while a custom ventilated and water cooled rear door has been developed for the PC racks (~80 units). This water cooled and ventilated rear door unit is also used by the Alice experiment and similar system is used in CMS and Atlas. Rack mountable PC units need to be cooled by horizontal air flow. PC units are hermetically closed on top and bottom and are designed to suck fresh air via their front panel.

The two bottom levels of the counting house are used for the computing farm and its main components while the third floor receives the front-end and DAQ interface electronics of the sub-detectors.

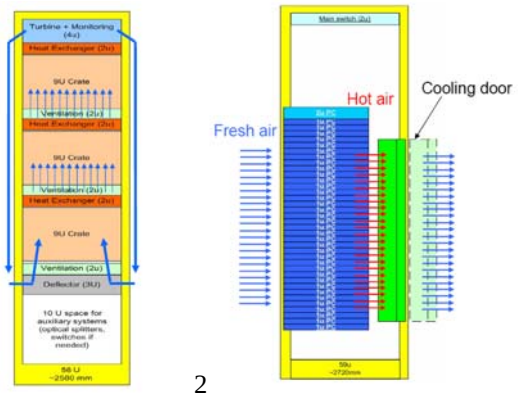


Figure 1: Front view of front-end racks (1) and side view of PC racks with rear cooling door unit (2)

III. Rack control and monitoring

The rack control and monitoring system consists of different infrastructure systems: the mains electrical distribution network and its remote control, the Detector Control System (DCS), also called Experiment Control System (ECS), the Detector Safety System (DSS), the rack monitor board (in the turbine units) and their ELMB based sensors and the smoke detector network and its PLC [1]. The system monitors principally the temperature, the rotation of the turbine motors and the presence of smoke in the racks. The control part can cut the mains power in racks via the DCS (soft manner via the local mains electrical power supervision system) under normal conditions or via the Detector Safety System (DSS) (brute force manner via interlocks) in emergency cases. In the frame of the rack control and monitoring system, DSS also offers the possibility to manually and remotely trigger the fire extinguisher in a given group of racks. Two different fire extinguisher systems are used in LHCb. Individual CO2 injection for the front-end electronics racks and a water mist system for the entire barracks where CPU farm racks are installed.

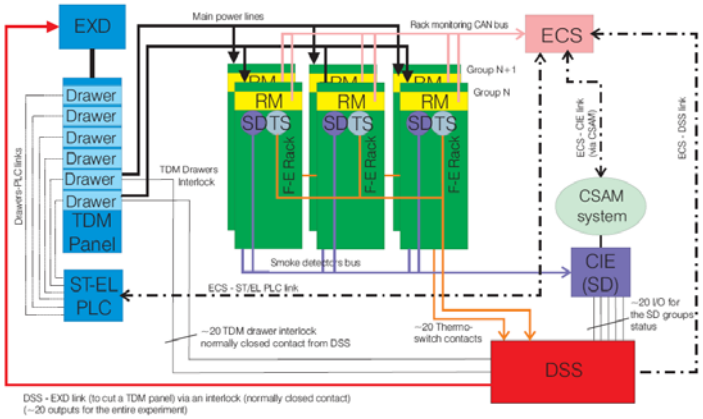
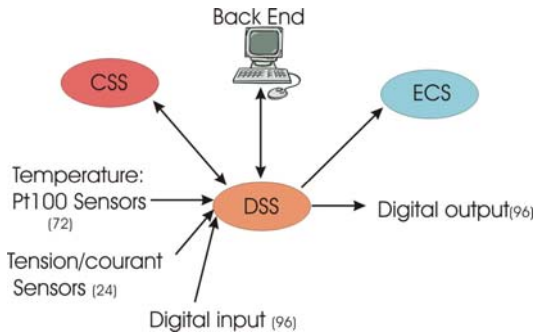


Figure 2: Rack control and monitoring working principle

IV. Detector Safety System (DSS)

The basic detector safety system is a common project used in all 4 LHC experiments. However, it is used in different manners across experiments. The purpose of this system is to intervene in case of emergencies when ECS has not intervened in time to protect expensive or rare equipments in the cavern and counting house (example: cut power when over temperature is detected, stop water cooling in case of leakage, etc.). Its actions are based on a number of sensors placed in critical locations. In LHCb it has been decided to use this safety system for the detector in a simple and unified manner across sub-system to get a reliable system [2].

Figure 3: DSS and its main links



The number of inputs and outputs available per sub-detector is limited in order to keep the system simple. This has the advantage, in addition of keeping the system at a reasonable size, of simplifying the cabling and reducing the possibility of errors. Only certain types of sensors are proposed to sub-detectors. Unified approach is given to sub-detectors for the choice, number and placement of their sensors. Thermo-switches are installed and trigger an alarm when a certain temperature is reached. Thermo-switches are daisy chained in groups and are placed where overheating can possibly damage equipment. PT100 measuring temperatures are limited to a few per sub-system. Water leak detection sensors are fixed where water cooled equipment are located. Based on these sensors, the DSS has the possibility to automatically cut mains electrical power to equipments, close the valves of the cooling network or shut down HV for a given or a group of sub-detector(s).

V. Mains Electrical Power Distribution

The mains power distribution network supplies all the permanent consumers that are directly related to the experiment itself. This includes the front-end electronics, the data acquisition system as well as other services and sub-systems such as cooling, gas and vacuum systems [3].

It has been decided to separate electrically the computing farm and the front-end electronics racks by using two 1.25 MVA transformers due to the fact that the online computing farm made of approximately 2000 PCs is expected to be a "bad" consumer (with poor quality power factor correction, PFC), inducing a non negligible dose of harmonics [4]. This has been made to avoid mains electrical power with high harmonics disturbing the sensitive front-end electronics.

Power from the mains transformers is distributed to the sub-system via 2 levels of distribution panels. The granularity for the power system is for groups of maximum 3 racks. Groups have been made for sub-detector halves (left/right separation) or for entire sub-detector (for smaller sub-systems). A local supervision system (PLC based) offers monitoring and basic control capabilities. DSS can turn off groups on emergency cases (via interlocks) when DCS or supervision system are not able to intervene. In the racks power is locally distributed via a 3U distribution box with 7 single phased outlets.

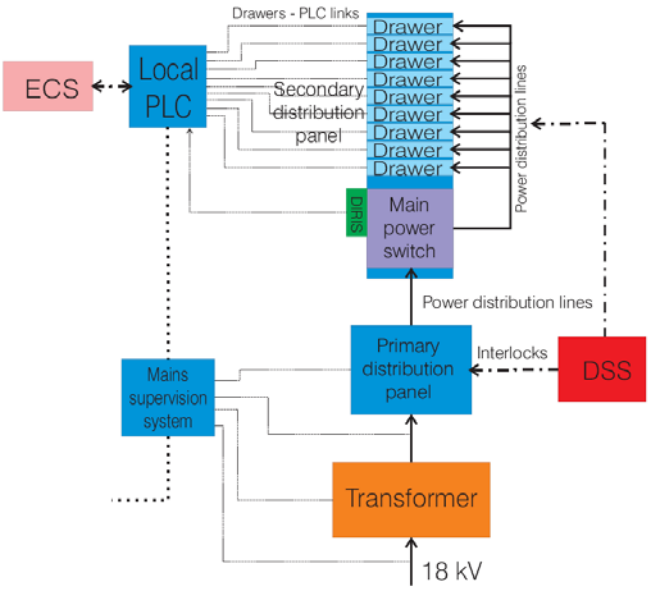


Figure 4: Overview of mains electrical power distribution principle

Front-end power supplies are all of the switching mode type and equipped with soft start system to limit inrush current and with active power factor correctors (APFC) [5]. PCs are most often not equipped with soft start systems and have been seen to have important inrush currents when turned on.

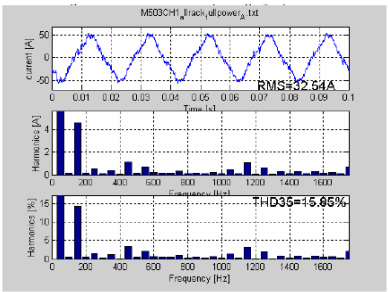


Figure 5: Measurement of total harmonic dose (THD) on a PC farm rack

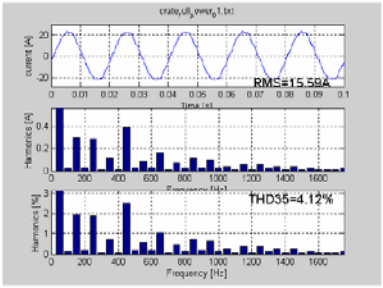


Figure 6: Measurement of THD on a standard crate low voltage power supply

It has been decided to implement adjustable temporization relays in the in-rack distribution boxes as the possibilities offered by the different standard types of circuit breaker trigger curves were not sufficient to deal with important inrush currents of the computing farm racks. In addition, rack groups (maximum 3 racks) are cascade started one after the other using the remote control feature of the distribution panels.

In the counting house, mains electrical power cables are installed on the ceiling in order to separate them from the sub-detector cables in the false floor. This reduces the risk of 50Hz parasitic coupling with sub-detectors sensitive cables.

VI. Low voltage power supplies

Recommendations have been made to LHCb sub-detectors to standardize as much as possible the type of low voltage power supplies used in the experiment. This, in addition to offering the possibility of organizing common spare parts across the sub-detectors gives us the following advantages: standardizing cable infrastructure and patch panels; possibility for all users to exchange knowledge and experience with equipment; standardizing the control (with DCS, PVSS) of those LV units.

Except the Vertex locator because of its requirements (large number of low power channels), all LHCb sub-detectors use the Wiener power supply system with radiation tolerant DC-DC converter (380Vdc to very low voltage, 2 to 8 Vdc for example). These DC converters can house a maximum of 12 channels of 300W maximum each and are installed relatively close to the on-detector front-end electronics as the geometry of LHCb favourably offers some locations with limited radiation level (few kRad).

All DC/DC converters used in LHCb are cooled by mixed water due to the important magnetic field present in the experimental cavern (fan cannot be used). The DC converter offer basic remote control and monitoring capabilities. The remote monitoring and control rely on a number of differential links per channel. AC-DC converters with APFC as well as the control modules are installed in the counting house racks, approximately 70 meters from the DC converter. 2 control cables and 1 power cable of reasonable thickness (current limited because of the relatively high voltage 380Vdc) are required per power supply.

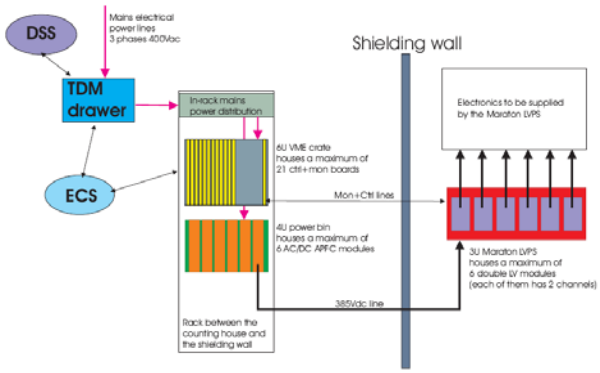


Figure 7: Low voltage power supply schema

All sub-detectors use radiation tolerant linear voltage regulators. These regulators are used to supply all local front-end electronics. Low voltage regulators form an additional filter for possible ripple at the input of the front-end electronics.

VII. Cabling

Chicane passages are present on both sides of the 4 meter thick shielding wall made of concrete blocks. These two chicanes of approximately 4 meter high by 350 mm large form two sections allowing the passage of all services going from the sub-detectors to the protected area where experiment and infrastructure electronics and control modules are installed. This includes, apart from the copper and optical fiber cables for data-readout, power and control (occupying half of both chicanes), all cooling, ventilation and gaz pipes and all mains electrical power distribution cabling. Due to the large amount of sub-detectors cables with important cross-sections, an existing groove in the cavern concrete floor is used as well for routing the cables.

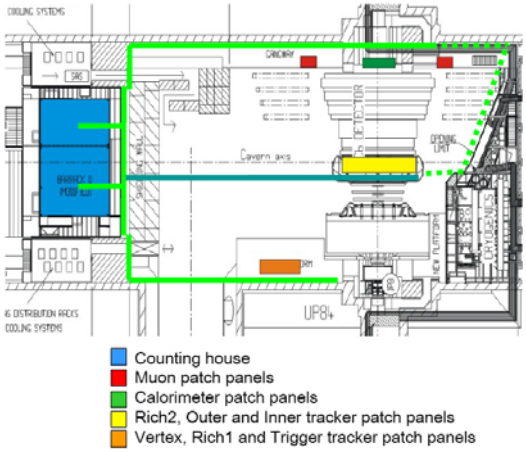


Figure 8: Overview of main cable routes in cavern

Patch panels decoupling the long distance links going to the counting house from the moveable parts of all links are used [6]. This offers the possibility of exchanging possible broken links easily in the moving cable chain where probability of broken cables is high. At the same time it offers the possibility to install spare links in the movable cable chain where installation is difficult due to the poor accessibility.

All commonly used cables, across sub-detectors, (for LVPS, CAN bus and other control links) are chosen with

shielding for EMC reasons. Recommendation is made to all sub-detectors to use shielded cables.

All experiment cables (for sub-detectors, ex.: readout, control and power) are supported by metallic closed (covered) cable ducts for EMC reasons. Each sub-detector has its cables installed in a cable duct separated from other sub-detector's cables. When and where possible, one cable duct is used for each cable type (power, control and readout) otherwise a metallic separator is installed in the cable duct in order to avoid different cable types being installed close to each other.

All long distance copper cables from sub-detector patch panels to counting house are first pulled without connectors. Connectors are then installed on cables in a second phase. This gives the possibility to optimize cable length in order to avoid storing extra length under racks which is not possible in LHCb due to space limitations. Another advantage of this installation method is that probability of damaging cables when they are installed is less important (no risk to pull out wires in a connector).

After connector installation, all copper cables are electrically tested (continuity and short).

VIII. Optical fiber links

A total of more than 7000 optical links is foreseen to be installed in the LHCb experiment. A relatively thick trunk fiber cable with 96 optical fibers organized in 8 groups of 12 fibers each is chosen for the long distance installation. On both ends, near the sub-detectors in racks and in the counting house, this cable ends in optical patch panels. The reason for this choice of cable has been made for the following reasons: reduce cross-section; a trunk cable thicker than individual optical fibers is more robust; all electronics readout boards have MPO-12 connectors with 12 fibers per connector.



Figure 9: Picture of one end of a multi-ribbon optical fiber trunk cable

The links connecting the detector with the counting house do generally not allow for retransmission of corrupted data and transmission errors will therefore result in erroneous event data. It is therefore mandatory to achieve the lowest bit error ratio (BER) possible both at installation and during operation.

Using the GOL serializer in fast 32bit mode, clocked by the LHC frequency, results in a physical serial data rate of 1.6 Gbit/s per optical link. This means a total bandwidth of 11.2 Tbit/s. Assuming a BER of 10^{-13} errors/bit results in ~1 error/s over the 7000 links. It is therefore clear that a BER, orders of magnitude better than 10^{-13} must be achieved. Therefore, particular care is taken during and after installation. Optical fiber handling [7] recommendations are given to users and extensive tests are performed. To keep testing time within acceptable limits and still assure link reliability as high as possible, a qualification scheme introducing extra attenuation has been chosen. The aim is to verify a BER of 10^{-12} with an additional attenuation of 6dB. These test conditions should assure that a much higher BER will be achieved in normal operation [8].

After installation of all multi-ribbon optical fiber cables, every single fiber link is tested (basic optical attenuation measurement). More extensive in situ tests and BER measurements are possible with final electronics modules as they contain this functionality.

IX. Grounding

In addition of its essential role in safety, the earth network connecting all metallic structure as well as the electrical equipments in an experiment as LHCb can serve as a base to install a heavily interconnected grounding network [9]. The purpose of such a grounding mesh in the experimental cavern is to reduce as much as possible the impedance between sub-detectors and counting house and more generally between equipments communicating to each other.

The safety earth cabling in LHCb connects all metallic structures and electrical equipments to the secondary star points of the mains transformers as well as an earth cable running along the cavern walls. This safety earth is also linked to the LHC machine earth underground and a connection is made at every LHC pit to the surface where earth electrodes are installed in the soil.

In order to complete this earth network to make a proper grounding network in LHCb, all metallic structure (rolling bridge beams, metallic supporting rails, other structures) are interconnected when possible on both sides of the cavern, detector side and counting house side [10]. In addition, a ground conductor of 120mm2 is installed every 4 cable ducts along the cavern walls. Cable ducts are connected to this ground every 5 meters.

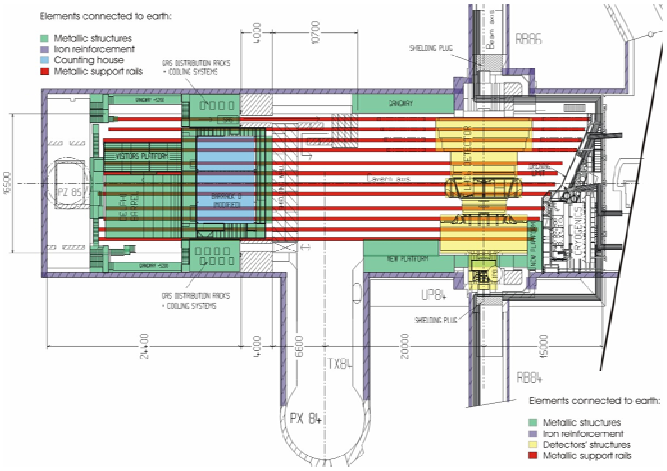


Figure 10: Overview of grounding in the experimental cavern

At all levels of the counting house, beams supporting racks in the false floor are interconnected to copper ground bars and cooling pipes. These copper ground bars interconnect

all electronics racks. This ground structure in the counting house is connected to the general grounding in the cavern via ground conductors, metallic structures and cable ducts.

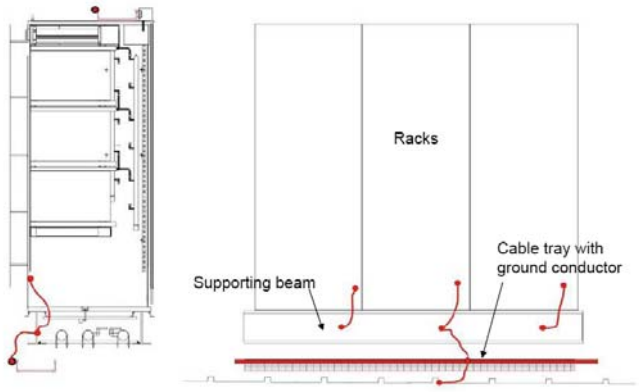


Figure 11: Side view of the rack grounding in the counting house false floor

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Testing, time alignment, calibration and monitoring features in the LHCb front-end electronics and DAQ interface

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Abstract

An overview of time alignment, testing, calibration and monitoring features in the front-end electronics of LHCb is given. General features for this are defined and examples are given of how this has been implemented in the LHCb front-end electronics and DAQ interface.

I. Introduction

A sufficient level of timing alignment, monitoring and built-in testing features in the front-end electronics system of a large scale experiment will be vital during the different phases of a HEP experiment to obtain a reliably working system. The electronics systems of a large experiment consist of thousands of complicated modules interconnected by thousands of communication interfaces (LHCb: ~7.000 optical links). It will be a significant challenge to get all these different types of modules (LHCb: ~50 different board types for a total of ~25.000 modules) to work correctly together during a long time period (10 years) in a hostile environment (noise, magnetic fields, radiation, etc.). Modules used to build a local sub-system will be tested together in a well controlled lab. environment beforehand but may still show problems when installed in the final "hostile" environment. The global integration of individual sub-systems will in many cases not occur before the whole experiment has been fully installed and final commissioning is started. Calibration and monitoring features are needed to continuously verify that the systems work correctly with the required precision. Extensive test and debugging features are needed during the initial commissioning phase and also to perform long term maintenance and repairs [3].

II. Front-end and DAQ architecture

The LHCb front-end architecture [1,2] shown in Figure 1 consists of analogue front-ends for analogue data treatment followed by a 160 clock cycles deep first level pipeline buffer (called L0 in LHCb). All LHCb front-ends have programmable length latency buffers so local adjustments of this can be made if needed. L0 trigger accepted events are stored in a 16 deep derandomizer buffer before readout to the DAQ system at an average rate of up to 1 MHz. Event data is at this level transferred on optical links (with the exception of the Vertex detector using multiplexed analogue copper links) to a DAQ interface located in the counting house. Each event block consists of 32 words of detector data and 2 – 3 words of event header information and finally an event separator adding up to a maximum event readout time of 900ns. The FPGA based DAQ interface module verifies the received event fragments and perform sub-detector specific zero-suppression and/or data compression before sending it to the DAQ system. The DAQ system is based on a large CPU farm (~ 2000 CPUs) and a large Gigabit Ethernet based readout network as shown in Figure 2. Multiple event fragments (8 – 16) are merged into Multi Event Packets (MEP) in each DAQ interface module to assure good GBE link utilization at the high LHCb trigger rate. Each DAQ interface module has four GBE outputs to cope with the high readout rate (total LHCb data bandwidth: ~0.5Tbit/s). The front-end, trigger and DAQ systems are controlled from the Experiment Control System (ECS).

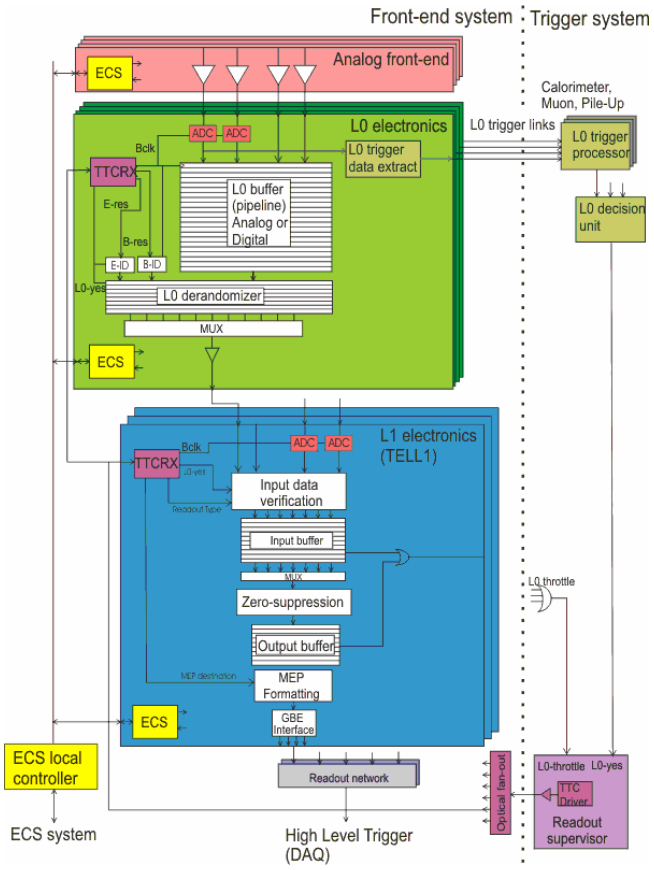

Figure 1. LHCb front-end architecture.

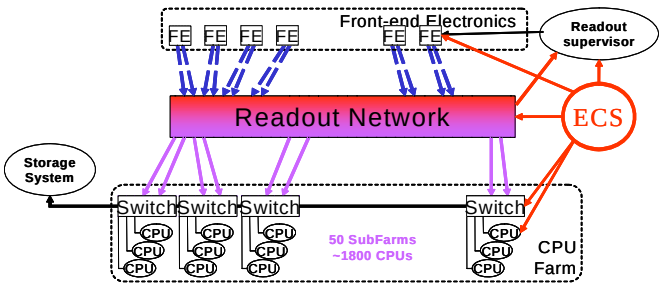

Figure 2. LHCb DAQ architecture

A. *Timing and Fast control*

Timing and fast control signals are distributed to all front-end electronics and DAQ interface modules via the TTC system based on optical fibre fan-outs and the TTCrx receiver chip. The TTC fibre distribution is driven from a bank of up to 16 readout supervisor modules that generates the necessary timing and trigger signals to the front-ends in a way that assures that all front-ends maintain full synchronization (e.g. applying restrictions to trigger preventing buffer overflows). Each of the available readout supervisors can drive local partitions or the global experiment via a programmable TTC switch/fan-out. LHCb has 16 TTC partitions that can be used to test and commission individual sub-detectors independently. During normal physics running only one readout supervisor drives the whole LHCb front-end and readout system. This implies that all the different sub-systems must interpret all TTC signals and broadcast messages in a unified fashion across the whole system. This is different from some of the other LHC experiments where each partition is controlled from individual TTC controllers, even when working as one global system. Such an approach can in principle allow sending different signals and broadcasts to different partitions but this must be done with great care to assure that different partitions are maintained fully synchronized to each other

III. FRONT-ENDS

Specific features in the LHCb front-end architecture related to timing alignment, calibration, testing and monitoring are indicated in Figure 3 below.

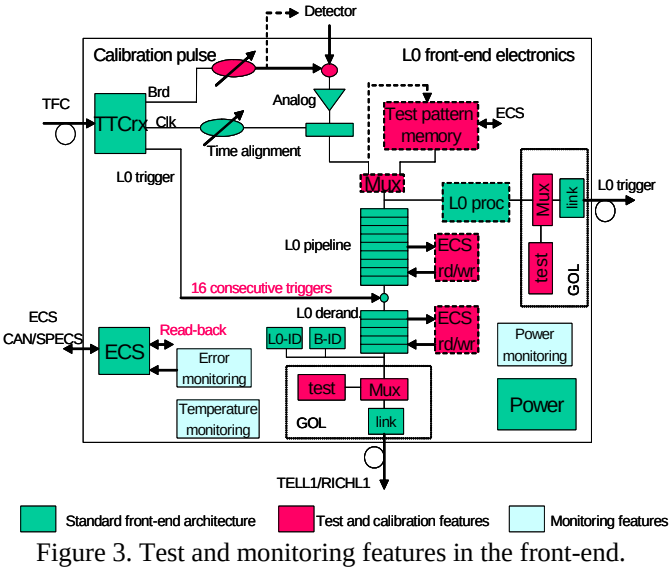

Figure 3. Test and monitoring features in the front-end.

Major features related to time alignment, calibration, testing and monitoring are described below. Some sub-detectors have included additional testing and debugging features which allows the Experiment Control System (ECS) to have direct read/write access to the L0 latency buffer and/or the derandomizer buffer. ECS read access to the derandomizer buffer has allowed some sub-systems to perform extensive front-end module tests via the ECS interface alone (no DAQ system needed).

A. *Timing alignment*

All sub-detectors have basic time alignment features based on the programmable delays of the TTCrx chip to capture detector signals with the correct phase and in the correct bunch cycle. The LHCb experiment located in an underground cavern and with a horizontal orientation can unfortunately not rely on cosmic muons to perform initial time alignment and detector alignment as the rate of muons traversing multiple sub-detectors in LHCb is extremely low. LHCb therefore depends critically on real beam collisions (or beam gas events) to perform the global time alignment. For small sub-detector systems (Vertex, Inner tracker, etc.), or local regions of large detector systems, only very small local time differences between channels will exist and can therefore to a first approximation be assumed to be time aligned between local channels.

To perform time alignments on real beam interactions a basic interaction trigger will be needed that is internally well time aligned from the beginning. In LHCb such an interaction trigger will be made from the Hadron calorimeter that has an internal time alignment system based on LED light pulse injection into its PMT's via known lengths of fibre. Global fine time alignment will be based on this trigger using detailed timing histograms to obtain a fully time aligned experiment. This will require a significant number of real interactions and software tools to obtain time alignment will be critical to minimize the use of sparse beam time available in the initial running of LHC during 2007 – 2008. The initial verification without LHC beams of such a time alignment system can be made using the basic pulse injection scheme with programmable delays as described below.

B. *Calibration pulse injection*

A common calibration pulse injection scheme has been defined across all sub-detectors based on a short TTC broadcast message [1]. The message encoding used allows up to four different types of calibration pulses. One of these calibration pulse types has been defined as a common type with a pre-defined timing in relation to the corresponding trigger accept as shown in Figure 4 below.

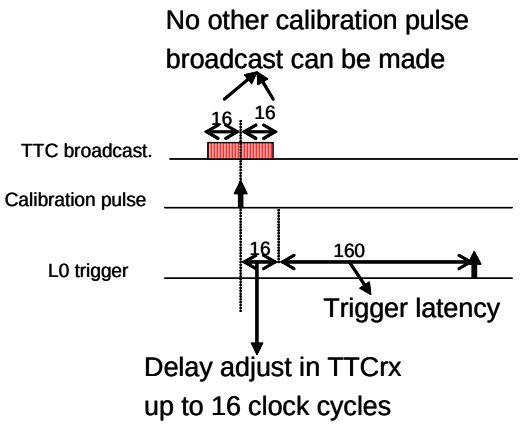

Figure 4. Common calibration pulse injection timing.

The three remaining calibration pulse injection types are available for sub-detector specific use if needed during local testing and commissioning. The corresponding trigger to the common calibration pulse has been defined to have a delay of 16 clock cycles plus the L0 trigger latency (160 clocks). This allows all sub-detectors to have enough time in the front-ends for the generated calibration pulse to enter their pipeline buffers for correct extraction with the corresponding trigger accept. All LHCb sub-detectors have implemented calibration pulse injection schemes for all detector channels based on the common type. This allows the common calibration pulse injection to be used globally in the whole LHCb system. The detailed characteristics of the calibration pulse injection is very sub-detector dependent caused by the specific nature of each sub-detector (Light injection in detector, pulse injection in analogue front-end, fixed or variable amplitude, etc.). All sub-detectors can adjust the time of the pulse injection locally over a dynamic range of 16 clock cycles allowing to verify that timing alignment features (hardware and software) is correctly working before having final beam collisions.

Certain sub-detectors rely on the use of the common calibration pulse type injection during normal physics running to closely monitor the gain and stability of the detector and its analogue front-end electronics (e.g. calorimeters). Only a limited number of detector channels can be exercised per calibration pulse injection to correctly monitor the detector performance without problematic crosstalk effects. Such events can if needed skip local zero-suppression in certain sub-detectors. Local round robin schemes have been implemented for such detectors to scan all detector channels within a reasonable time window (few minutes).

C. Consecutive triggers

LHCb has a first level trigger accept rate of up to 1.1MHz which is a factor ~10 higher than ATLAS/CMS. The high trigger rate is caused by the difficulty of making efficient hardwired trigger systems for B physics at LHC. This has implied the use of a relative large derandomizer buffer in the front-ends (16 compared to ~4 in other LHC experiments) and the use of a significant number of radiation hard optical links to transport acquired data from the experiment to the counting house. At this high trigger rate enforced spacings between trigger accepts results in a ~2.5% loss in physics per enforced gap. It was also in the early phase of LHCb considered very useful to trigger a whole sequence of consecutive triggers (max 16) to have an efficient way to perform a first coarse time alignment between channels and also directly measure pulse width, spill-over and baseline shift effects as indicated in Figure 5.

Handling of consecutive triggers is particular difficult for detectors with relative long pulse shapes and detectors with drift times covering several bunch crossing periods. Specific features in the front-end electronics of such sub-detectors have though allowed consecutive triggers to be supported (calorimeter and outer tracker). During recent system tests it has though unfortunately been discovered that one of the LHCb sub-detector front-end ASIC's does not handle correctly consecutive triggers. Consecutive triggers are still planned to be used extensively during first steps of local and global commissioning tests with dedicated software tools to acquire data and analysis it. The specific sub-detector requiring a single gap between triggers will have to handle such commissioning tests in a dedicated manner. Final physics running will be made with a minimum trigger gap of one to assure correct readout across all sub-detectors.

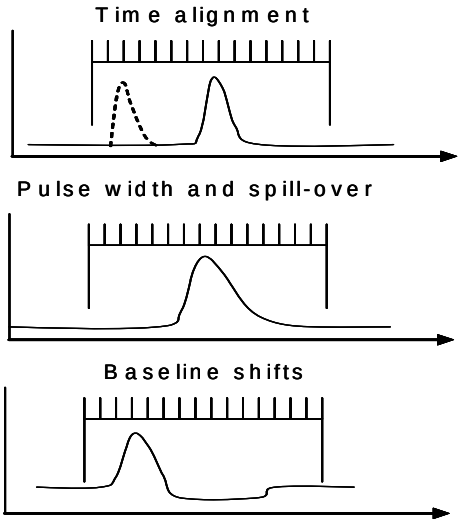

Figure 5. Use of consecutive triggers

D. Synchronization and Data monitoring

To assure correct data taking during extended physics running it is extremely important that the whole front-end and readout system is synchronized. A local de-synchronization could pass unnoticed for extended periods if the front-end and trigger systems are not capable of continuously verify their correct synchronization. In the first level trigger system, and in the extraction of accepted events, the systems must be perfectly synchronized at the clock level. For the interface to the DAQ system it must be assured that only event fragments from the same event are merged in the global event building. Careful monitoring of this is particular needed when the front-end electronics is located in locations with high radiation levels and may get de-synchronized by single event upsets (SEU).

For communication interfaces (e.g. optical links) in the L0 trigger systems specific idle/synchronization patterns are introduced each machine cycle to allow local systems to verify their synchronization and re-synchronize if needed. In addition all trigger data carries a few bits of bunch ID information as indicated in the figure below.

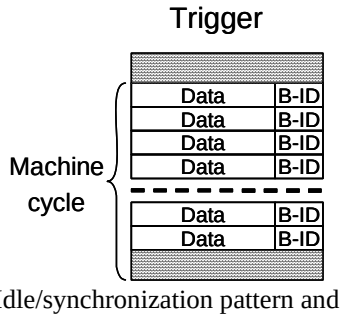

Figure 6. Idle/synchronization pattern and bunch ID information on trigger links.

For the readout path it is enforced that all event readout after the first level trigger accept must have an event header with bunch ID and Event ID information. This allows the DAQ interface to check the correct event synchronization of each data source, comparing the received information with reference information received from its TTC interface (this part not in radiation area so no SEU effects). To ensure event synchronization even in case of bit or word errors on readout links, it is enforced to transmit an idle/synchronization pattern between each event fragment.

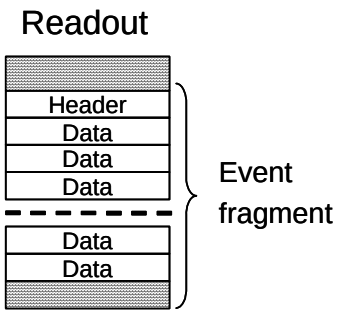

Figure 7. Event tagging and event separation.

It has been verified with radiation tests that trigger and readout links can re-synchronize on a single word idle/synchronization pattern when the transmitter or receiver PLL's have not lost frequency lock (word consisting of four 8B/10B idle characters). Tests have been made to confirm that the transmitter and receiver PLL's do not loose lock from single bit or word errors.

E. Pattern and spy memories

In sub-detector systems involved in the first level trigger (calorimeter, muon and pileup veto) testing features based on built in pattern generation and pattern acquisition (spy) memories are used. Specific hit patterns can be written from ECS to pattern generation memories in the front-ends as indicated in Figure 4. These hit patterns can then be applied in a pattern by pattern scheme trigger by TTC broadcasts or can be used in a continuous circular fashion in special testing modes. Spy memories at the output of the local trigger systems and at key internal locations can capture the detailed response of the systems to verify their correct function or to determine the cause of mal functions.

F. Optical links

~7000 optical links are used in LHCb for first level trigger systems and for data readout after the first level trigger accept. All link transmitters on the detector are based on the radiation hard serializer chip GOL from the CERN Microelectronics group [4]. The global reliability of the LHCb experiment will depend critically on the reliability and error rates of these links. Assuming the commonly accepted Bit Error Rate (BER) of 10^{-12} - 10^{-13} for optical links, the total system will have transmission errors at the rate of 1-10 per second. It is therefore clear that the effective error rate of the links must be much lower than this and that basic link transmission errors must not generate problems at the system level. The enforced use of regular idle/synchronization patterns ensures that the sub-systems can remain functional and recover by them self within very short time intervals (e.g. single event fragment corrupted or part of L0 trigger system not fully functional until next machine cycle).

The GOL chip itself is assumed SEU immune as it uses full internal triple redundant logic. It has been seen that 12way optical transmitters used in some of the LHCb sub-detectors has a small SEU upset rate caused by some simple internal circuitry. The use of regular idle/synchronization patterns have been demonstrated to resolve this problem in a fully satisfactory fashion [5].

To assure that all optical link receivers, transmitters and installed fibres are working in a fully satisfactory fashion it is required that all links are verified to work with a BER below 10^{-12} (test takes ~10 min) when an additional 6db optical attenuation is inserted (in addition to fibre and patch panel losses). This has been seen to assure that the optical links work with a BER rate lower than what can practically be measured. Measurements of BER with 9 and 12db optical attenuation are also required in the design qualification of transmitter and receiver modules [6]

It is required that all optical links must be capable of measuring BER in situ. A simple pattern generator function in the GOL allows to send a continuous counting test pattern and all receiver modules are required to have a simple pattern verification and error counting function on all optical link inputs.

During normal operation single bit errors (that translates to the loss of a whole word) are normally detected by the 8B/10B encoding used on the link and word resynchronization is a previously mentioned in section D obtained by the use of regular idle/synchronization patterns.

IV. DAQ INTERFACE

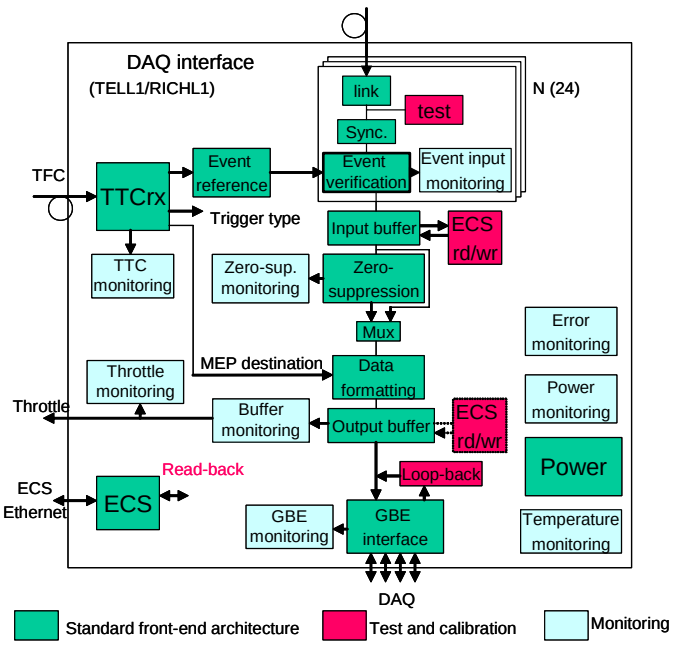

Figure 8. Data flow in DAQ interface.

A generic data flow model of the DAQ interface is shown above with the marking of specific testing and calibration features and general monitoring. The DAQ interface is implemented with the common module called the TELL1 [7]

for all sub-detectors, except the RICH detector that have chosen to make a dedicated module. The TELL1 is based on power full FPGA's with a generic firmware VHDL framework handling the global data flow, buffering and system interfaces. Only the zero-suppression is sub-detector specific as it depends strongly on the type of detector data.

Received event data are on each input verified against an event reference from the Local TTCrx receiver, as described in paragraph III.D, before being passed to the zero-suppression processing. Zero-suppression can be disabled in a static fashion from the ECS or can be disabled in a dynamic fashion for specific event types (e.g. calibration events). It is also possible for specific trigger types to read out both non zero-suppressed data and zero-suppressed data to allow extensive verifications of the zero-suppression function. Event data is then buffered and a given number of events are merged into a Multi Event Package (MEP) to be sent to the DAQ system. The destination address of the MEP is received via a long TTC broadcast message that also contains a few bits of event identification verification information. MEP's are finally sent to the DAQ processing farm over a large GBE based readout network via a standardized GBE plug-in card with 4 GBE ports [8].

A. Testing and debugging features

Extensive testing and debugging features are built into the generic VHDL framework and are therefore available across all sub-detectors in a unified fashion. The simple BER test function is available in all optical inputs as previously described. Raw received input data can in dedicated testing modes be accessed via the ECS interface and emulated raw data can also be inserted to allow the full processing of the board to be verified. The zero-suppression can be enabled or disabled in a static or dynamic form as described above. Fully formatted MEP packets in the output buffer can be accessed from the ECS interface for verification or for injecting specific MEP packets for system testing. The quad GBE interface plug-in card, based on commercial MAC and PHY chips, can make data loops at multiple levels between incoming and outgoing GBE traffic on each port. In addition a LHCb specific packet mirroring function is implemented in the FPGA's that allow a received encapsulated MEP packet to be retransmitted to any of its four ports to a destination defined in the packet itself. This packet mirroring allows extensive verification of the DAQ readout network at high rates driven directly by the CPU farm itself.

B. Monitoring and local ECS interface

Data, event and error monitoring counters are used extensively throughout the data flow to allow detailed monitoring and tracing of system failures. The number of events and data words that have passed key locations in the data flow is counted (input links, TTC messages, output of zero-suppression, data buffering and output to the readout network). Sub-detector specific monitoring of the zero-suppression is included according to the needs of each sub-detector.

General monitoring, testing and debugging of the TELL1 module are performed via the ECS interface based on an small plug-in credit card PC running Linux. Direct access to all control and monitoring features of the board is made via a DIM server on the CC-PC. Local running monitoring programs can also perform local intelligent monitoring and built locally histograms without loading the global ECS system with such trivial tasks. Local monitoring tasks are though in general not yet well defined but several sub-detectors plan to use such features.

V. SUB-DETECTOR SPECIFICS

Main features for time alignment, calibration, and monitoring have been defined globally but large differences exist between sub-detectors in the detailed function of these. Many of these differences have been dictated by specific features of the individual detector technologies (e.g. binary or analogue readout) and some have been determined by design choices for the front-end electronics (e.g. ECS access to pipeline and derandomizer buffers). Such implementation choices normally have very good justifications seen from the local sub-system point of view, but may in some cases be impractical at the global system level. Some sub-systems have implemented specific features to allow the pulse injection to be usable during normal physics running were other systems have been made such that this will be difficult or impractical. An example of this is the question of how the pulse injection is made. In the Beetle silicon strip front-end chip [9] the calibration pulse injection has opposite polarity between neighbour channels and changes polarity every second calibration pulse. This calibration pulse injection scheme has been found useful for the detailed characterization of the front-end chip, but must be considered impractical at the system level to generate specific hit patterns on channels to test and verify the Vertex pileup veto trigger system.

The muon detector has a particular problem with low hit rates and a relative large fraction of the hits being out of time background hits. To ensure efficient time alignment of all muon detector channels dedicated time histogram memories have been built into the TDC front-end ASIC.

VI. CONCLUSIONS AND LEASSONS LEARNT

Features for testing, time alignment, calibration and monitoring have been defined to have a global set of tools to be used during commissioning, running and maintenance of the LHCb experiment. It is important to define such features as early as possible to allow the necessary support for it to be built into the front-end electronics of each sub-system. Such global features must though also have sufficient flexibility to cover the specific characteristics of the different sub-detectors and to cover potential problems and imperfections in all the different sub-systems. Key features must be strongly enforced across all the sub-systems, to allow efficient system running, even in cases where local sub-systems insist that they do no see the need for such features.

It was in LHCb realized relatively late that optical links could become a major system reliability problem. Fortunately an un-documented pattern generation feature of the GOL link serializer was identified which is now part of a standardized link test and qualification procedure.

All testing, calibration and monitoring features need extensive software support to allow its efficient use at the global system level. Much of this software still needs to be finalized at the local and global level. Final verification of all the required features across sub-detectors will to a large extent not be made before starting the final commissioning of the experiment.

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A Readout System for the LHCb Outer Tracker

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Abstract

The LHCb Outer Tracker is composed of 55 000 straw drift tubes. The requirements for the OT electronics are the precise (1 ns) drift time measurement at 6 % occupancy and 1 MHz readout. Charge signals from the straw detector are amplified, shaped and discriminated by ATLAS ASDBLR chips. Drift-times are determined and stored in the OTIS TDC and put out to a GOL serializer at L0 accept. Optical fibres carry the data 90 m to the TELL1 acquisition board. The full readout chain performed well in an e- test beam.

I. Overview

55 000 straw drift tubes of 5 mm diameter mounted perpendicular to the bending plane behind the magnet form the Outer Tracker of LHCb [1]. A track resolution of 200 µm in the bending plane leads to a demand for a drift time resolution of better than 1 ns. The readout electronics is based on three ASIC chips, the ASDBLR [2][3][4][5][6] amplifier from ATLAS, the OTIS TDC [7][8] developed at the ASIC lab in Heidelberg and the GOL [9] (gigabit optical link) serializer from CERN EP. All on-detector electronics for one module end is housed in a shielded metal box.

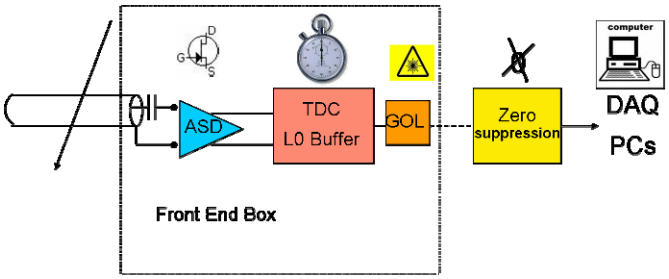

Figure 1: Block Diagram of OT Electronics

The charge signal from the straw anode wires is amplified, shaped and discriminated by an 8 channel ASDBLR chip with 12 ns shaping time. Four ASDBLRs on 2 PCBs are connected to one OTIS TDC. The relative time between the discriminated hit signal and the bunch clock is determined by the OTIS TDC with the help of a delay locked loop. The 64 inverters in the DLL lead to a time resolution of 25 ns/64 = 390 ps. Drift times are 6-bit encoded and written to a 240 bit wide L0-buffer. At L0-accept hits within a 75 ns window are readout and a header containing OTIS location, L0-id, Bunch-Id plus status is prepended. L0 accepted data from 4 TDCs runs to the GOL chip. The GOL serializes 32 input bits to a 1.6 Gbit/s output, driving a VCSEL diode. Optical fibers carry the data 90 m to the TELL1 [10][11] acquisition board. On the TELL1 daughter boards with 12 inputs each convert the optical serial data back to parallel electrical data. FPGAs on the TELL1 are programmed to synchronize, zero suppress and reformat the data. At 1 MHz events are transmitted through multiple Gigabit ports to a more than 1000 CPU computing farm.

The newly developed outer tracker electronics was used for data taking in an e- test beam. Reading out 512 channels the full chain proved excellent performance.

II. Amplifier

The ASDBLR Amplifier Shaper Discriminator with Base Line Restoration is an ASIC developed for the ATLAS TRT straw detector by Michael Newcomer (University of Pennsylvania). It is implemented in the DMILL bipolar process. Basic characteristics are the fast peaking time of 7 to 8 ns, radiation hardness withstanding 3 MRads of ionizing particles and 10^{14} Neutrons/cm^2, low cross talk of 0.2% and low noise of < 1fC equivalent charge.

After a pre selection discarding chips with malfunction such as broken channels the analogue performance is tested. In a threshold scan with fixed charge injection sensitivity-spread and noise of each channel is measured and the best 30% of the working ASDBLRs are chosen, see Figure 2:

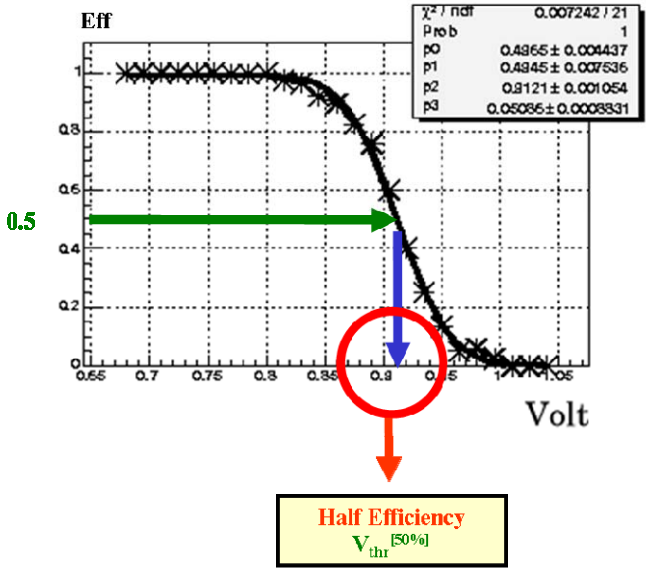

Figure 2: Amplifier Threshold Scan

The sensitivity is measured by the position of the 50% efficiency (vs. threshold) and the noise level can be deduced from the steepness of the step function.

Two ASDBLR chips share the same board, see Figure 3:

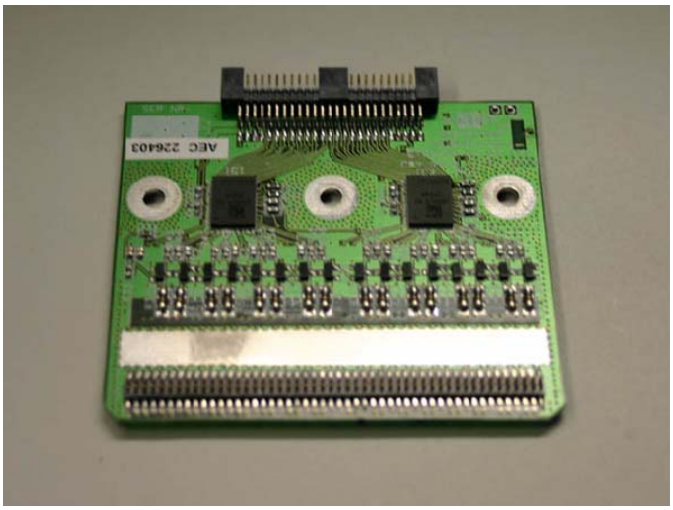

Figure 3: Amplifier Board

The board design was optimised for grounding and good heat dissipation. To achieve better grounding the 16 input signals are connected via a 100 pin connector, all non signal pins carrying ground. Non standard 100 µm copper planes inside the PCB and numerous cooling via allow operation of the chip at below 45 °C with standard water cooling of the electronic box.

III. Time to Digital Converter

The TDC called Outer Tracker Time Information System OTIS is a 0.25 µm CMOS ASIC.

It allows the drift time measurement of 32 detector channels with an accuracy of better than 1 ns.

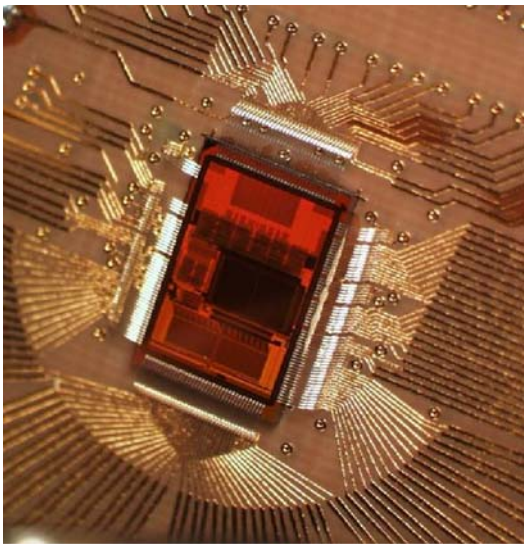

Figure 4: OTIS TDC

The bunch clock of ca. 40 MHz is running through a delay locked loop with 32 delay elements of two stages each, with a tab after each stage. Each tab delivers a time reference shifted in respect to the bunch clock. This leads to an intrinsic resolution of 25ns /64 = 390 ps. When one of the 32 differential inputs of the OTIS senses a hit signal, the state of all tabs is latched into the hit registers of this channel and the first 0 1 transition is encoded into 6 bit. Every 25 ns a bit signalling if a hit was sensed in this channel, the timing information, and the bunch counter are input to the L0 pipeline. The L0 pipeline is implemented as radiation hard dual port SRAM [12] of 164 rows and a width of 240 bit. At a positive trigger decision the relevant data is copied to the derandomizer buffer. The OTIS chip allows the readout of 3 consecutive bunches at one L0 accept such covering 75 ns. The data is reorganized into a header containing the number of the bunch crossing, the event number and error conditions followed by the drift time information. In the standard scheme 32 header bits are followed by 32 bytes of drift time information. In this scheme each byte carries the drift time of 1 channel. The data of one TDC is send through 8 differential CMOS outputs to the serializer chip (GOL).

Each OTIS is bonded to one PCB, interfacing to two ASDBLR amplifier boards and the GOL auxiliary board. The TDC has an I^2C [13] control bus interface and carries eight digital to analogue converters supplying the threshold voltages to the four connected ASDBLR and the settings for the initialization and monitoring of the delay locked loop.

The performance of the TDC has been studied both using random hit signals and signals with a well defined delay in respect to the bunch clock. The relation between input signal delay and measured drift time is shown in Figure 5:

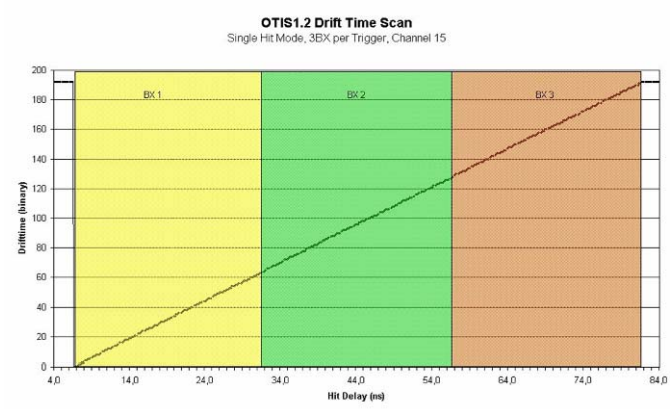

Figure 5: Delay [ns] vs Drift Time [bin]

IV. Gigabit Optical Link

The data accepted by the L0 trigger is output by the TDC in 36 bytes @ 40 MHz. Data from four TDC chips is serialized with the help of one Gigabit Optical Link (GOL) chip, resulting in incoming 32 bits parallel. The GOL is used in Gigabit Ethernet mode, encoding all bytes in 10 bit words that are chosen to balance the number of high and low bits at the serial output. The data is finally fully serialized and output to a Vertical-Cavity Surface-Emitting Laser (VCSEL) at 1.6 Gbit/s. The VCSEL diode is a type from ULM photonics (ULM850-05-TN-USMBOP). The bias current for the VCSEL can be set via the I^2C bus interface of the GOL chip, a good choice was 1.8 mA. The GOL output was moved as close as possible (<3 mm) to the VCSEL, the connection is impedance matched to 22 Ohm. The performance of the optical link is determined by a bit error rate test BERT. The GOL chip has a build in 16 bit counter that can be activated as data source via I^2C. Alternatively the optical signal was measured with the help of an optical probe [15][16]. Sampling a few thousand bit transitions into an eye diagram shows how good the high and the low value of the digital signal are separated, see top left in Figure 6:

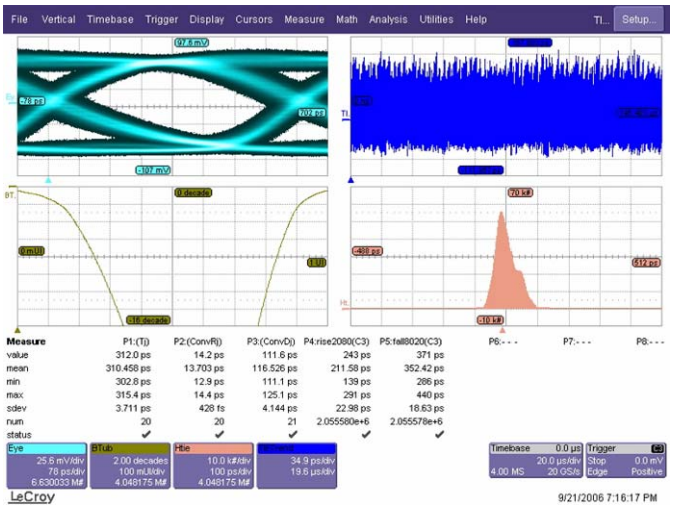

Figure 6: Eye Diagram of Serial Data

The GOL chip is mounted in a 100 pin BGA package on the GOL auxiliary board [17]. In order to guarantee the performance of the GOL chip a clock filter QPLL [18] and a four transistor power switch CRT4T have been added on the GOL auxiliary board. The QPLL filters the clock signal driven by the TTCrx [19] fast control receiver chip to below 50 ps peak to peak. The lock rage of the QPLL is 3.7 kHz around the reference frequency of 40.0786 MHz. Especially its connection to the controlled quartz must carefully respect pad and line capacities. The CRT4T switches the power at the GOL inputs fully off, so avoiding partial powering of the phase locked loop.

The GOL auxiliary board also distributes low voltage, fast control signals and I^2C slow control bus. The low voltage 2.5V, 3V and -3V regulated by three radiation hard power regulators from ST microelectronics, type 4913 [20] and 7913 [21][22]. The input voltage is +6V and -6V. The water cooling line of the front end electronic Box (FE-box) is directly under these power regulators. To reduce the risk of oscillation of especially the negative type 7913, extra 100 µF capacitors have been placed both at the ±6V inputs and at the -3 V output. The 2.5V serves as supply for the OTIS TDC, the GOL, the QPLL and the CRT4T while the +3V and -3V are used for the ASDBLR amplifiers. As a few LVDS receivers and the VCSEL diode need +3V too, their supply voltage is decoupled by series resistors (C-R-C-R-C low pass).

The fast control signals clock, trigger, test pulse and synchronous resets for bunch and event counters arrive as LVDS signals on the GOL auxiliary board and are distributed to the 4 OTIS boards using current dividing resistors.

I^2C is transmitted via LVDS lines from and to the control box on the detector frame and converted to a single ended signal on the GOL auxiliary card.

V. Front End Box

The front end electronics consisting of 4 HV boards, 8 ASDBLR board, 4 OTIS boards and 1 GOL auxiliary board is mounted in the FE-box see Figure 7:

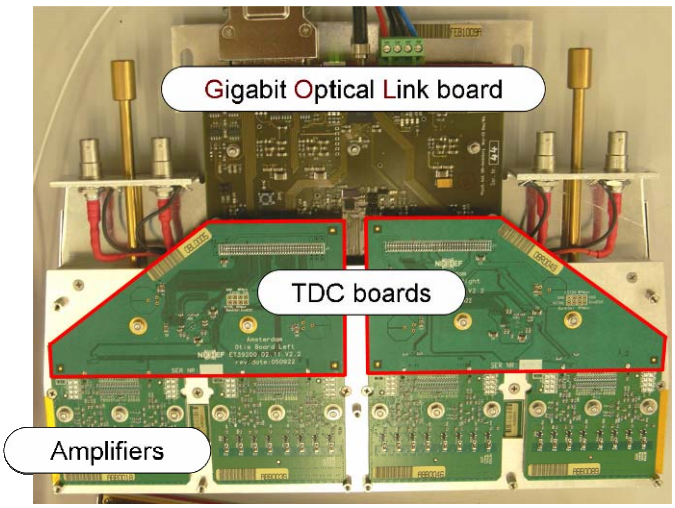

Figure 7: Front End Electronic Box

Each front end electronic box serves the 128 channels on one end of a straw detector module. It has 4 HV inputs, a 50 pin SCSI controls input, a 4 pin LV input, but only one optical

fibre data output. The FE-box is mechanical and electrical protection and conducts the heat to the water cooling.

VI. TELL1 BOARD

The data from the Outer Tracker on detector electronics is transmitted over 432 fibres to the counting house. There a LHCb wide established 9U DAQ board (TELL1) receives the data, does zero suppression and reformatting before sending it at the same rate of 1.1 MHz over four Gigabit Ethernet ports to the CPUs of the online filter farm. The TELL1 board is based on four FPGA chips on the input and one FPGA for the data output see Figure 8:

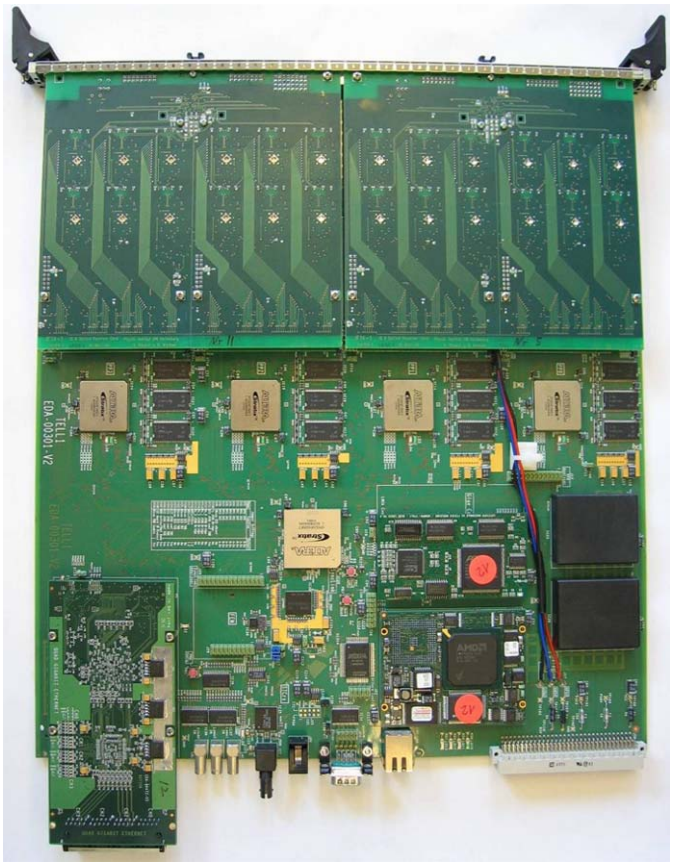

Figure 8: TELL1 DAQ Board (Lausanne)

As both analogue and digital data transmission from the detector to the counting house are implemented in LHCb two different input cards have been developed. The OT uses the optical receiver Card (O-RxCard). The O-RxCard [23] houses a 12 way optical receiver and 12 TI TLK2501 [24] deserializers. The O-RxCard has been developed in Heidelberg and produced in Beijing. As the OT has a high average occupancy only 9 out of 2x12 optical inputs will be used per TELL1 board.

VII. PERFORMANCE AT TEST BEAM

In the beginning of 2005 a test of the full OT electronics took place at DESY using a 5 GeV electron beam. 4 short detector modules from the series production have been mounted and read out. The electronics consisted of FE-boxes from the preproduction, the TTC [25] system, I^2C slow control and a FPGA based DAQ [26][27] using the O-RxCard and a commercial PCI acquisition board [28]. The trigger and time reference was coming from scintillators in the beam axis after the detector modules. After a few days of setup the electronics was running stable until the end two weeks later. The numerous data sets where used to validate the noise, x-talk and timing of the electronics as well as to study the tracking resolution of the overall detector [29].A histograms of the drift time can be seen in Figure 9:

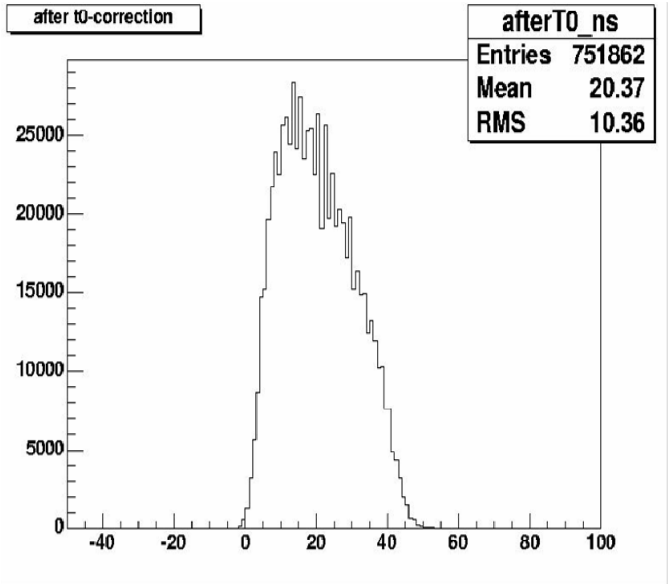

Figure 9: Drift Times t0 corrected

The efficiency was above 94%, the timing resolution better than 0.5 ns and the spatial resolution better than 175 ns.

VIII. SUMMARY AND OUTLOOK

The readout electronics of the LHCb Outer Tracker has been developed and successfully tested to achieve good resolution at a high efficiency and low noise. All ASIC chips have been produced and tested by now. The production and test of the boards is reaching the 20 % level at the moment and the installation and commissioning has started in the LHCb cavern.

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The Front End Electronics of the Scintillator Pad Detector of the LHCb Calorimeter

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Abstract

In this paper the Front End electronics of the Scintillator Pad Detector (SPD) is outlined. The SPD is a sub-system of the Calorimeter of the LHCb experiment designed to discriminate between charged and neutral particles for the first level trigger.

The system design is presented, describing its different functionalities implemented through three different cards and several ASICs. These functionalities are signal processing and digitization, data transmission, interface with control and timing systems of the experiment, low voltage power supply distribution and monitoring. Special emphasis is placed on installation and commissioning subjects such as cabling, grounding, shielding and power distribution.

I. INTRODUCTION

LHCb calorimetry [1] unfolds into four elements: a hadronic calorimeter (HCAL), an electromagnetic calorimeter (ECAL), a Preshower detector (PS) and a Scintillator Pad Detector (SPD). The system provides high energy hadrons, electron and photon candidates for the first level trigger (called L0 trigger) of the experiment.

The PS and the SPD are designed to distinguish electrons from pions and charged particles from neutrals respectively for the L0. PS as well as ECAL and HCAL measure particle energy, whereas SPD is a binary output detector. SPD information is also used to introduce a cut in the L0 on the SPD hit multiplicity for removing the tail of the hit multiplicity distribution (high multiplicity events might clog up CPU nodes), while keeping the same signal efficiency and minimum bias retention.

SPD and PS are two sub-detectors in front of ECAL separated by a 1.4 cm thick layer of lead. They consist in a layer of 6000 plastic scintillator (Bicron BC-408) tiles with a Kurarai Y11 WLS (wavelength shifting) rolled fibre to collect the light emitted by the scintillator when a charged particle goes through it. Charged particles will produce, whereas photons will not, ionization on the scintillator. The light is transmitted through a clear fibre to the SPD readout system. The signal of the scintillator pads, both for PS and SPD, is processed in a Very Front End (VFE) unit. These units are placed on metallic boxes on the top and on the bottom of the respective scintillator walls.

An overview of SPD sub-system and its main connections are shown in Figure 1.

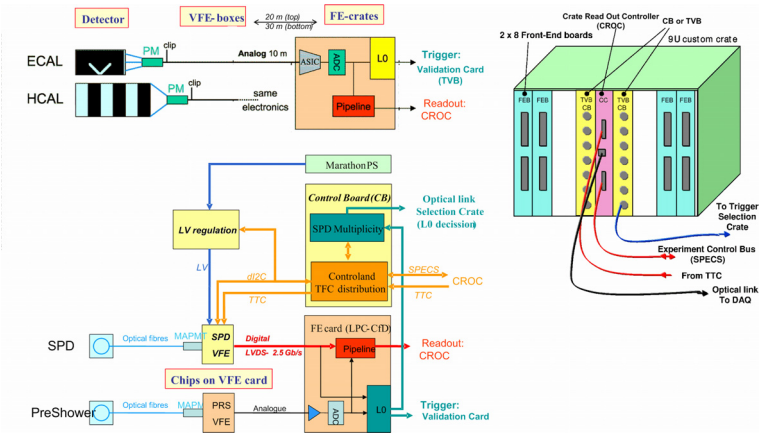

Figure 1. Block diagram of the SPD front-end elements.

The front-end electronics of the LHCb calorimeter [3], except the VFE cards, will be placed in crates at the top of the calorimeters. The total radiation dose expected there is about 6 krads over 10 years thus allowing the use of commercial components, provided that the most critical of them have been tested in a beam. 14 ECAL and 4 HCAL crates receive respectively 6000 and 1500 channels. 8 PS crates receive a total of 6000 channels both from the PS's and the SPD's VFE.

The ECAL/HCAL PM signals are connected directly to the front-end boards (FEBs) through 10 meters of coaxial cables, whereas 20 m to 30 m differential pairs are used to send the output of the PS (analogue) and SPD cards (digital) VFE cards to a common PS/SPD FEB [4]. There are 16 FEBs in the crates, each receiving 32 signals for ECAL/HCAL crates and 64 signals from each detector for PS/SPD crates.

The FEBs have two different data paths: the trigger one and the readout one. The outputs of these boards are connected to the standardized custom backplane, sending signals using LVDS levels to the Calorimeter Readout Controller (CROC) for the readout data path and to the Validation boards for the trigger data path. The CROC also receives the Experiment Control System (ECS) implemented under SPECS protocol [5] and the 40 MHz bunch crossing clock, trigger and synchronous commands from the LHCb Timing and Fast Control system (TFC) [6] and there from distributes them over the whole crate.

The CB is placed in the FE crates; there are two for each of the 8 crates corresponding to the PS/SPD subsystem. The purpose of the CB is twofold:

- To provide to the VFE cards a link to the ECS and TFC system. A phase alignment of the experiment clock [6] is also performed in the CB.
- Each PS/SPD FEB counts the number of SPD hits in the corresponding SPD VFE card. Up to 8 PS/SPD FEBs send this number to 1 CB through the backplane. The CB sums the 8 numbers and sends the result to Selection Crate in barracks.

A water cooled magnetic field and radiation tolerant floating power supply system (MARATON) [7] feeds the crates and the VFE cards. The long distance between FE crates and VFE cards force to use local regulation close to the sensitive electronics. Regulator cards have monitoring capabilities and are also connected to ECS through the CB.

II. VFE Board

As depicted in Figure 2 the VFE board [8] includes a photomultiplier (PMT) to convert the light pulse into charge, the electronics to perform the discrimination between electron and photon signals, a control unit and a LVDS serializer to send the information to the PS/SPD FEB.

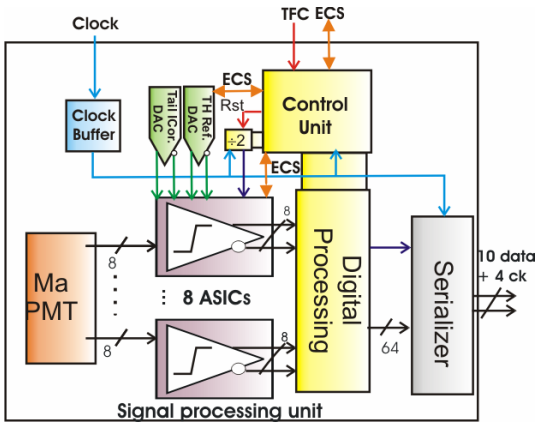

Figure 2. Block diagram of the VFE card

There are two external (no on-chip) DAC with I2C interface to set some analogue references for the signal processing part. The control unit, the digital processing and clock divider to obtain the 20 MHz clock that controls the ASICs operation are implemented through a re-programmable FPGA, the ProAsic Plus Actel APA300. Triple Voting Registers (TVRs) are used to minimize the SEU errors. The digital processing consists on mapping the PMT channel to given serializer channel to match the PS and SPD detector cell (2 different mappings selected by ECS) and to inject arbitrary patterns to test the detector data flow.

The control unit continuously controls SEUs in all VFE registers and signals the errors in a status register. It also allows to power cycle the DACs to recover from SEU hard errors ([2]) in their I2C logic, and provides interface with:

- ECS system between CB and VFE board chips (I2C). According to global LHCb requirements [6], any register can be read back from the ECS.
- TFC system to provide a synchronous reset of the clock divider and trigger for the pattern injection.

A. Signal processing

For economical reasons a multianode (Ma)PMT is chosen as photo detector, being the Hamamatsu R7600-M64 the selected candidate. Acceptance test has been carried out to ensure that the 100 PMTs comply with the specifications [9]. All of the PMT were within specifications for linearity, gain, and uniformity, but not for crosstalk, for which the requirements were not fulfilled for a 10% of the tubes.

The PMT signal is amplified, shaped and discriminated through an 8 channel ASIC [10] (AMS BiCMOS 0.8 µm technology). Figure 3 shows the functional architecture of each channel. The configuration is based on two interleaved processing units per channel to avoid any dead time and to be able to perform the pile-up compensation. The bunch-crossing clock is divided (outside the chip) and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalk on sensitive analogue parts, all the blocks are fully differential. Each path uses an independent DAC to be able to compensate the offsets due to process variations between different subchannels.

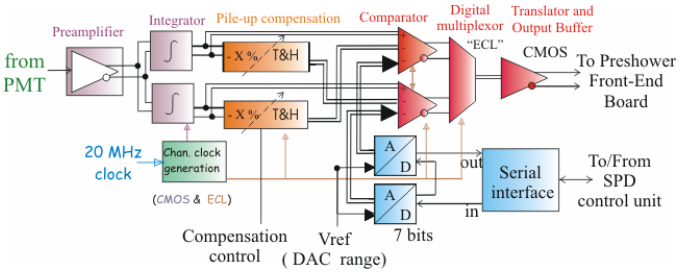

Figure 3. Functional diagram of a discriminator channel.

Techniques were applied to improve the radiation tolerance: place guard rings for MOS transistors to prevent latch up, use NAND gates instead of NOR gates and TVRs to minimise the SEU effects. The chip has been qualified for the LHCb radiation levels [2].

An engineering run was shared with other calorimeter chips to produce about 2000 units, 1300 have been packaged on an EDAQUAD QFP64 package and tested obtaining a yield of the 80 %. Table 1 summarizes the test results of the produced ASICs, for a MaPMT load resistor of 470Ω. A MIP signal will be adjusted through the HV on a 30 to 100 fC range depending on the MaPMT uniformity.

Table 1. ASIC performance

Noise (ENC)	2 fC rms
Gain	1.16 mV/fC
Gain spread	< 5 %
Offset spread	65 mV rms
Correction matching	< 2 %
Linearity Error	< 10 mV (1 %)
Power Consumption	500 mW (3.3 V)

B. Card implementation and performance

As a result of room constraints, the actual design of the VFE board has been split into three different boards as shown in Figure 4.

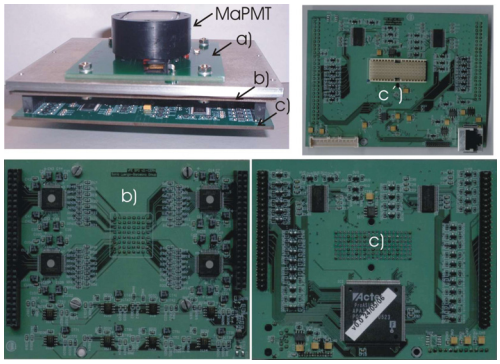

Figure 4. VFE card: a) PMT base board, b) ASIC's board and c) FPGA board (c' is the bottom view of c).

a) *PMT base board*: This board hosts an active base for the photomultiplier.

b) *ASICs board*: This board contains the eight ASICs and its associated circuitry, the part of threshold reference and subtractor reference.

c) *IO/Logic board*: The last board contains the FPGA, the serializers and the connectors.

All components passed radiation tests (see [2] and [11]) in order to obtain the radiation qualification (single event effects and cumulative effects).

A 10% pre-series of a total production of 120 has been produced and tested. The performance of the signal processing in the card is in agreement with ASIC performance summarized in Table 1. The electrical crosstalk is found to be smaller than the 2%. The pedestal short term stability (10 hours operation) is better than 2 mV. A prototype of the card has been tested in SPS facility (X7 area) using a 25 ns clock synchronous with the beam. Although the light yield was low (12 phe/MIP) due to problems with optical connections, a trigger efficiency of 93 % and a fake trigger ratio of 1 % have been measured, setting the threshold at 0.5 MIP. Tail correction and beam phase synchronization were also tested successfully. A total of 9 burn-in cycles of about 8 hours between 0 to 50 ° C have been performed to the pre-series cards and no problematic component has been identified. During the cycles a card was continuously monitored; remaining functional.

C. *Long distance LVDS serialized transmission*

The 64 channels and the 20 MHz clock are sent to the PS/SPD FEBs. The serializing factor in DS90CR215 chip is 7; thus 4 serializers are needed. Since each serializer has 3 data pairs and 1 clock pair, using standard shielded twisted pair (SSTP) LAN cables seems an economic solution.

The skew margin of the serializing chipset is only of 500 ps, and the skew of 30 m long commercial cables is higher than 2 ns, even for category 7 Ethernet cables. However, we observed that the skew between consecutive 30 m cuts of the same pair is very low, usually lower than 500 ps. Taking benefit from the fact that 4 serializers and 4 cables of 4 pairs are needed, we designed a link with a custom board (see Figure 5) implementing a cross-connection scheme to send each pairs corresponding to a given serializer through a different cable but through the same pair.

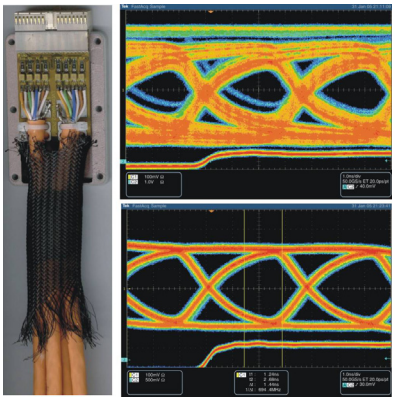

Figure 5. Left: view of the transmitter end of the link. Right: eye diagrams for a category 7 30 m long cable: un-compensated (top) and equalized (bottom) using random patterns.

Since serializer has no pre-emphasis circuit, the card of Figure 5) has a passive (inductor in series with a resistor) pole-zero network to equalize the cable response. An eye opening of 1.44 ns between LVDS thresholds (±100 mV) has been obtained (see Figure 5).

A total number of 120 links have been produced, 64 for the top part (18 m long) and 56 for the bottom part (27 m long). The skew between each data pair and the corresponding clock has been measured. The skew for top cables was smaller than 500 ps. For bottom cables out of 540 data pairs, 2 have a skew between 500 and 700 ps, and 2 a skew of about 800 ps. Only for the pairs with 800 ps skew, errors have been found for some patterns, for other cables BER<10^{-12}.

Furthermore, the frequency clock of the system has been increased up to the limit of the test system which is 60 MHz, without noticing errors for a 30 m long cable. This means that using simple electronics and standard ethernet cables, a copper link can transmit at 480 Mbits/s per pair over 30 m with BER<10^{-14}. The sensitivity of the link to common-mode differences between serializer and deserializer has been also tested, no problem was found in ±0.5 V range.

III. Control Board

Figure 6 shows the block diagram of the CB, which is an 8 layers 9U card. As said before we can distinguish between trigger and control functionalities of the CB.

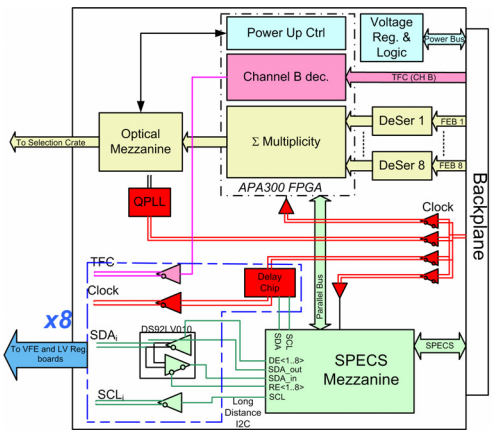

Figure 6. Block diagram of the CB

The trigger functionality consists on receiving and deserializing (DS90CR216) the multiplicity data from up to 8 different PS/SPD FEBs trough LVDS serialized point to point backplane links, adding these numbers and transmitting the information to the barrack through an optical link. The addition is performed through an Actel APA300 FPGA. The optical transmitter is implemented as mezzanine card used in other Calorimeter parts [12]. Data coming from the deserializers can be sampled either at the clock rising or falling edge, this assures a correct sampling provided that the skew between different FEBs is less than half clock period. The multiplicity part has been tested with PS/SPD FEBs placed in all possible slots of the crate.

The control functionality consists on providing ECS and TFC interface for up to 8 VFE elements, either a VFE board or a LV regulation board. The communication between the CB and the VFE element is through SSTP ethernet cables using shielded RJ45 connectors. Therefore, 4 pairs are available: 1 for the 40 MHz clock, 1 for the TFC signal and 2 for the ECS interface.

The SPECS slave is implemented trough a SPECS mezzanine card which is an LHCb standard ECS interface [5]. The SPECS mezzanine provides a standard local I2C bus and a long distance I2C bus. A differential long distance I2C bus over 2 LVDS pairs is the ECS interface for VFE.

The FPGA used for the multiplicity also decodes the channel B lines of the TFC system, where synchronous commands such as resets or calibration pulses are coded. The FPGA serializes a reduced set of commands (see VFE board section) and sends them to the VFE trough a dedicated pair in the control cable.

The remaining pair on the cable transmits the 40 MHz clock to the VFE after being delayed by a programmable clock distribution ASIC [15] to phase align the sampling of the analogue detector signals (integrator's gate is the 20 MHz clock) to the bunch crossings [6]. This chip generates 4 differential outputs and each of them can introduce a maximum delay of 25ns to the clock, with 1 ns steps.

In addition to the trigger multiplicity and channel B decoding, the FPGA perform other tasks. On the one hand, for testing and debugging purposes, the multiplicity data can be spied at the output of the multiplicity part and read through the parallel bus of the optical mezzanine On the other hand, it controls the power start-up sequence of the GOL.

To assure a high quality clock distribution the LVDS clock transmitted through the backplane is point to point buffered with differential drivers placed very close to the input connector. Special care is taken for the clock driving serializers, those for the optical mezzanine and those placed in the VFE card. First problem is addressed filtering clock jitter with a QPLL chip [14] at the input of the optical mezzanine. For the VFE clock a fully balanced differential amplifier (AD8138) is used to drive the twisted pair cable with a pole-zero cancellation network to improve the rise-time of the signal (from 1.2 ns to 600 ps). Table 2 shows jitter measurements for the most important points of the clock network, no degradation is observed neither on the CB itself nor on the VFE board.

Table 2. Jitter results

	Peak to Peak	RMS
Input (test system)	37 ps	4.6 ps
Opt. Mez. Input	33 ps	3.6 ps
VFE (22 m cable)	57 ps	7.9 ps
VFE (29 m cable)	61 ps	9 ps

IV. Grounding, Shielding and Power Distribution

A. Grounding

The calorimeter ground configuration is a heavily interconnected ground network (mesh structure) as recommended in [17]. The electronics of the calorimeter is distributed in many different locations: the front end racks, the PS VFE and the SPD VFE. Although differential signals have been used wherever possible, the input stage of the ASICs is DC coupled to the PMT and it is a single ended signal by definition. Thus, ground parasitic currents should be minimized. This goal should be achieved with a mesh structure with very low impedance from DC to few hundreds of MHz. All cables will be shielded twisted pair.

B. Power distribution

In Figure 7 it is shown the precise power distribution scheme for the SPD. The main power supplies modules are floating and the ground connection is done at the load (regulator card and VFE unit) to avoid returning currents through the ground network.

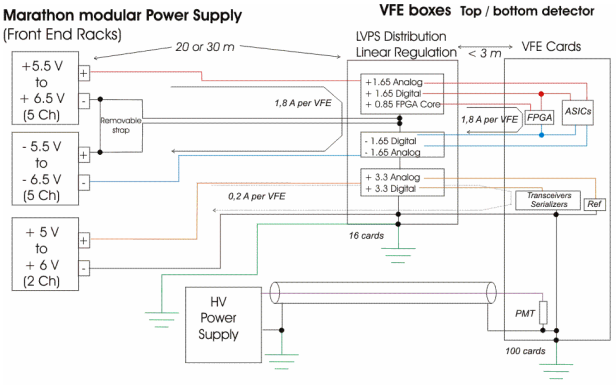

Figure 7. Power supply distribution

Different regulators are used for digital and analogue supply voltages, even if they do have the same value, to minimize conducted interference. It is intended to minimize the current return through the ground network using separated connections for ground and for the current return (neutral conductor) of each power supply. Each power line derived in the Marathon Power supplies and in the regulator card will be protected with a fuse properly tailored to the corresponding operating current to avoid fire or other potential risks in case of short circuit. For the power supply to local regulation connection, shielded twisted pair cables with 4 mm^2 conductor (IEC 60228 class 5 flexible) section will be used. For the local regulation to VFE units short connection, shielded twisted pair cables with 0.5 mm^2 conductors will be

used. Due to the very specific requirement all LV cables are specially manufactured for this application.

C. *Electromagnetic Compatibility*

The metallic box that houses VFE units and regulator cards should act as a Faraday Cage. The MAPMT/VFE boxes material is iron (5 mm thick).

A potential source of significant inductive noise in the LHCb environment is the coils of the main magnet. The main victims of this interference in SPD VFE could be:

- The MaPMT. The iron box plus a special μ-metal shielding around PMT protect the PMT.
- The inductors used for cable equalization. Special test has been done at Orsay, showing effects smaller than a few % on the inductance up to 400 gauss (worst orientation)

It is not foreseen a specific power filtering for the low voltage connection, the use of local regulation (inside the Faraday cage) is considered to be safe enough. Power filtering is foreseen for the HV in the PMT baseboard.

A VFE box was fully equipped with VFE and LV regulator cards, cabled and tested. No degradation was observed on noise and pedestal stability. The VFE box incorporates a water cooling system that has also been tested with success.

V. LV Regulation Board

LV regulation cards, based on CERN-ST Radiation Hard voltage regulators [16], will be installed in the VFE boxes. The VFE card requires many different supply voltages as reported in section IV.B (Figure 7), making necessary the use of several regulators per card. In order to optimize the usage of the power regulator each regulator card will power up to 7 VFE cards. It results on a complex power distribution system, advising monitoring to be integrated in the same board. This is done using an FPGA which performs periodic analogue readouts of voltages and currents. LV card also performs temperature measurements using onboard probes and probes embedded in VFE cards. A block diagram of the board is shown in Figure 8.

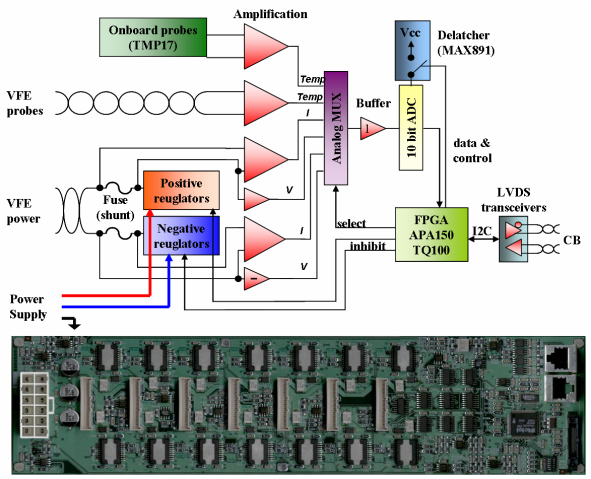

Figure 8. Block diagram and top view of the LV regulation board.

The probability of a SEL is very low but not zero for the serializers (DS90CR215) [11]. In a case of a SEL a real time monitoring system will switch off the regulators. Each power line is also protected with fast fuses. The FPGA also controls the start-up of the logic of VFE board.

A pre-series of the regulation board has been produced and tested. The monitoring instrumentation has been calibrated within a precision better than the 1 % for currents and voltages and of 2º C for temperatures. The same burn-in procedure of the VFE board has been applied. A LV regulation board was continuously monitored through the ECS, remaining operational during the burn-in.

VI. Acknowledgements

We would like to thank the members of the LHCb calorimeter for their collaboration in the development of this design, especially to the groups of LAL (Orsay) and LPC (Clermont Ferrand). We acknowledge also the Spanish CICYT by the financial support (FPA2005-068889-C01-01)

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Front-end Electronics Test for the LHCb Muon Wire Chambers

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Abstract

This document describes the apparatus and procedures implemented to test Multi Wire Proportional Chambers (MWPC) after front-end assembly for the LHCb Muon Detector. Results of measurements of key noise parameters are also described. Given a fully equipped chamber, this system is able to diagnose every channel performing an analysis of front-end output drivers' response and noise rate versus threshold. Besides, it allows to assess if the noise rate at the experiment threshold region is within appropriate limits. Aiming at an automatic, fast and user-friendly system for mass production tests of MWPC, the project has foreseen as well electronic identification of every chamber and front-end board, and data archiving in such a way to make it available to the Experiment Control System (ECS) while in operation.

I. Introduction

A. Chamber Readout Overview

The LHCb Muon System [1] is made of 19 geometrically different MWPC types. Depending on the chamber, the input capacitance as seen by the front-end electronics (FE) can vary from roughly 40pF to 250pF. Signals are collected from either anode or cathode; therefore a dedicated 8-channels Amplifier, Shaper and Discriminator (ASD) rad-hard chip, named CARIOCA [2], has been developed to process both polarities by means of two different pre-amplifiers in the ASD input stage. They show slightly different signal responses depending on the chosen polarity of operation. The on-detector circuitry is composed generally of two boards: Spark-Protection (SPB) and CARDIAC. The former board makes use of passive components while the latter processes and digitalizes chamber signals. A front-end card accommodates two CARIOCAs and a chip named DIALOG, [3] which has been developed to readout and control the CARIOCA chip. One DIALOG has one DAC per channel to control thresholds, 16 24-bit internal counters and features for timing adjustments of signals. An LHCb Muon specific software suite [4] was developed to study the behaviour of equipped chambers providing fully access to FEB features.

The main features of CARIOCA are:

- Sensitivity: 8-16 mV/fC
- Equivalent Noise Charge: 0.3-2 fC
  - 2240+42 e-/pF negative amplifier
  - 1880+45 e-/pF positive amplifier
- Offset: 795.6 ± 9.9 mV *(-35 ± 5.5 mV)*
- Residual bias: 35 ± 5.5 mV
- Max. Rate: 10-25 MHz (depending on polarity)

A 9.9 mV RMS offset can generate a large error while setting thresholds, as a consequence one separate threshold per channel can be set. A CARIOCA discriminator makes use of a Differential Threshold Voltage (DTV) circuit (1 per channel). It is able to provide a differential threshold from a reference voltage with single polarity. Apart from the offset spread there is a cut on the threshold range which does not allow setting values below a minimum (see Figure 1). This parameter has a charge value varying in the 2-4 fC range, depending on the input capacitance (for single input capacitance values measurements yield a RMS of 0.4 fC). Such a value can also be evaluated in terms of residual bias (discriminator characteristic). Theoretically this value is not correlated to the input capacitance and has a value of about ResBias = 35 ± 5.5 mV.

The noise (in Volts) and the threshold cut value can be directly measured by a threshold scan procedure as described in the next section. The threshold cut and the residual bias values can then be utilized in order to find the offset value of an ASD channel (the value at which the threshold is equivalent to zero Coulomb).

B. Front-end Electronics Noise

Considering a charge sensitive amplifier, noise affects amplitude measurement resolution and, consequently, the minimum detectable charge value. Due to noise, the amplifier response has a certain statistical distribution. The probability density function describing the amplifier response in the presence of Gaussian noise can be expressed by:

$$f(V) = \frac{1}{\sqrt{2\pi}\sigma_n} e^{-\frac{1}{2}\frac{V^2}{\sigma_n^2}} \qquad (1)$$

Given a discriminator threshold V_{th}, the probability that a sample results to be higher than such a threshold is given by:

$$P = \int_{V_{th}}^{\infty} \frac{1}{\sqrt{2\pi}\sigma_n} e^{-\frac{1}{2}\frac{V^2}{\sigma_n^2}} dV \qquad (2)$$

The noise voltage (V_n as seen at the discriminator input), can be obtained from the sigma value of the function (2).

Theoretically a white noise process contains all frequency components with uniform amplitude. In practice, given some noise occurrence in a system, if its power level does not vary with frequency over the system operating range, the noise can be treated as a "white noise" process. Because power spectrum characteristics of this noise process are well known,

evaluating the response of a circuit it is possible to reconstruct the characteristics of its own bandwidth behaviour.

Considering a Gaussian noise presence in a discriminator input, and not taking into account bandwidth limitation, one can expect a threshold to noise ratio as represented by equation (3). Such an equation corresponds to the noise rate exceeding threshold level; with a signal baseline equal to V_{offset}.

$$f(V) = f_n \int_{V_{th}}^{\infty} e^{-\frac{1}{2}\frac{(V-V_{offset})^2}{V_n^2}} dV \qquad \text{for } V_{th} \geq V_{offset} \quad (3)$$

where V_{th} is the threshold, V_n provides the noise in Volts and f_n is the sum of amplitude occurrences up to the mean value of the noise Gaussian amplitude.

Considering a Gaussian time distribution, the noise rate as a function of threshold can be approximately represented as follows:

$$f(V_{th}) = f_{n0} e^{-\frac{1}{2}\frac{(V_{th}-V_{offset})^2}{V_n^2}} \qquad f_{n0} = \sqrt{\frac{1}{3}\frac{f_2^3 - f_1^3}{f_2 - f_1}} \qquad (4)$$

Using formula (4) [5,6], the maximum noise rate f_{n0} (vertex frequency) can be calculated in terms of cutoff frequencies bandwidth parameters. Hence the vertex frequency can provide information about FE circuit bandwidth.

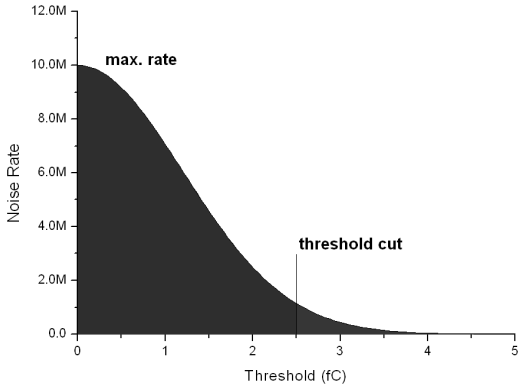


Figure 1 - Threshold scan for an offset equal to zero and considering bandwidth circuit characteristics.

It is possible to achieve a more precise value of V_n if it is considered noise rates below a certain frequency value, where the circuit bandwidth begins to affect the circuit response, and computing each of those measured noise rate values as follows: $R_i = R_i - R_{i-1}$ (with $V_{th(i)} > V_{th(i-1)}$). Using this procedure, V_n can be obtained from formula (1) parameters.

Since, it is only possible to make measurements above the threshold cut value (Figure 1, top); the formula below is used because it has been shown to be an efficient method to fit the noise curve. Figure 2 shows an example of the noise measurement method applied to analysis.

$$f(x) = e^{A - Bx} \qquad x = V_{th}^2 \qquad (5)$$

$$V_n = \sqrt{\frac{1}{2B}}$$

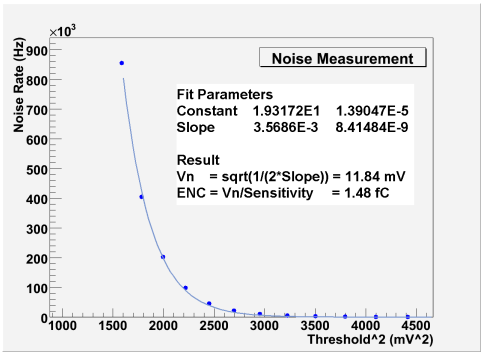


Figure 2 - Example of the noise curve measurement method.

By means of a threshold scan it is possible to obtain information about 2 important parameters of the circuit located before the discriminator: bandwidth and noise. An analysis as described above has been implemented in order to evaluate the method efficiency and has been utilized as a diagnostic tool for LHCb Muon Chamber Readout Electronics.

C. *Cdet Measurement*

The front-end input capacitance (Cdet) is a fundamental parameter in the chamber readout test. A threshold scan procedure permits a direct measurement of noise in Volts and, as a result, an estimation of capacitance at the FE inputs (Cdet) through a direct conversion using a calibration curve (Figure 4). Fits of the known characteristics sensitivity and ENC curve of the ASD chip have been plotted (Figure 3), in order to use them analyzing the parameters of each CARIOCA, and to obtain the noise voltage value at the discriminator input for a given external threshold.

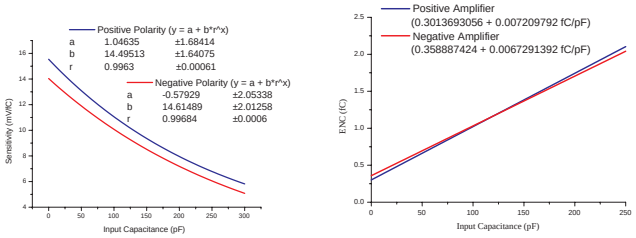


Figure 3 - CARIOCA sensitivity and noise curve (fit).

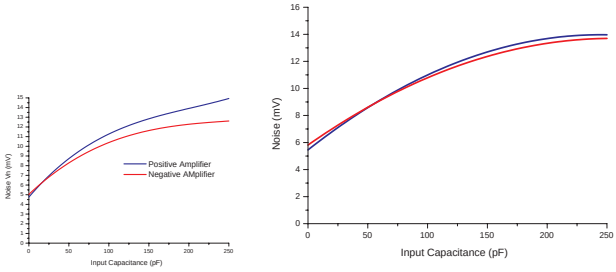


Figure 4 - CARIOCA noise at the discriminator input using the known sensitivity and noise curves (left) and directly measured.

The calibration curve (Figure 4 left side) obtained from sensitivity and noise characteristic curves are slightly different from the results of our measurements of noise voltage at the discriminator inputs. The calibration curve (Figure 4 right side) based on those measurements is used for the tests shown below.

II. Testing Setup

The test setup consists of a MWPC equipped with front-end boards (DUT's), a barcode reader and control and readout circuitry, all supervised by a PC.

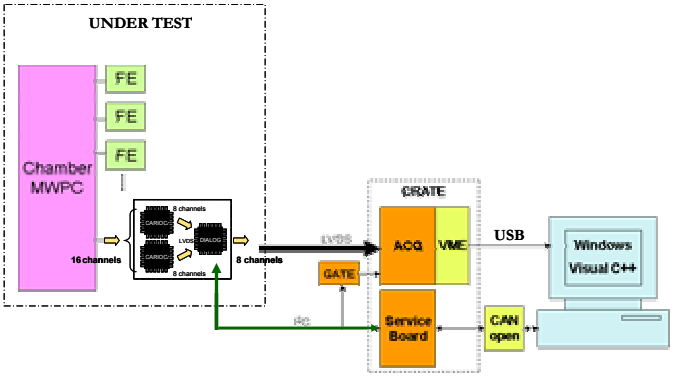


Figure 5 - Testing setup scheme.

A. Control Equipment

Control is performed by means of a Service Board [7]. It can access in parallel all FEBs belonging to a chamber, generating pulses to be used mainly to inject signals and to control internal and external counters. This board is accessed using the CANopen protocol. To do so a commercial adapter manufactured by Kvaser Company has been used.

B. Readout Electronics

There are 2 ways to readout the FEBs: by means of DIALOG internal counters or using the 64-channels counting module ACQ [8]. A gating board has been designed and used in order to translate the SB gate signal sent to the front-end into a pattern compatible with ACQ logic.

C. Barcode Reader

During the chamber assembly, a ROOT (CERN analysis software) based program is used to identify and archive barcodes of chambers and their front-end boards. Afterwards, the Faraday cage (metal enclosure) is put into place, therefore not consenting direct access to the FEBs and their barcodes. The barcode information related to each FEB will be used later by analysis programs to access the database created as a result of FEB's production tests.

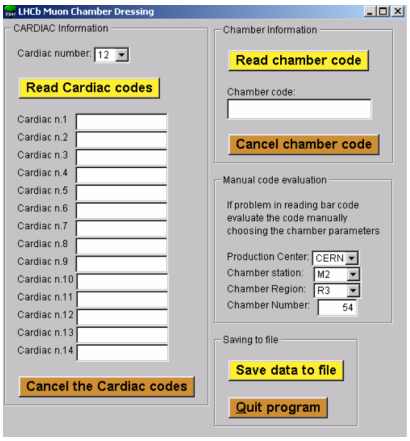


Figure 6 - Barcode reader program.

D. Software

A Visual C++-ROOT integrated software tool has been developed to control all circuits, performing a diagnostic analysis of chambers and visualization of results.

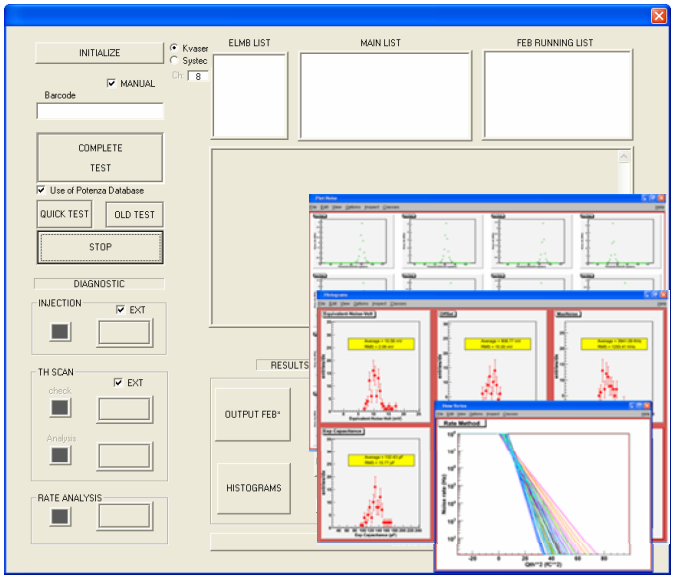


Figure 7 - Control, analysis and diagnostics software.

III. Procedures and Diagnostics

A. Cable checking and Auto-Injection

Once all the control and readout cables are connected, by means of injecting signals into the FEBs in a known sequence it can be verified that the cables are not inverted or there are false contacts.

Another procedure, checking if all FE channels respond to auto-injected generated signals, allows validating functionalities such as: auto-injection, internal counters and output drivers' response, making a comparison with the content of ACQ counters.

B. Threshold Scan

With a threshold scan, a curve of threshold versus noise rate is generated, as shown in Figure 8. The threshold is in a range encompassing both polarities and, as shown before, it is performed in a range outside ±35 mV.

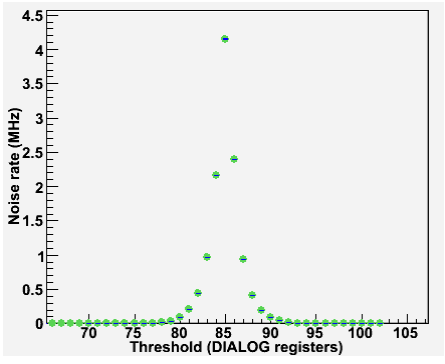


Figure 8 - Threshold scan curve. *Th(mV) = Th(plot)*2.42 + 625*

1) Noise presence and offset

A first analysis is carried out checking if the number of measured points obtained during the threshold scan is sufficient in order to fit the data. This is a useful tool to single out dead channels: if no points at all are found, the channel is marked as dead.

The offset value corresponds to the threshold value with the maximum rate of noise (from now on the term offset is used to indicate actually the value related to the threshold cut). Finally, the procedure verifies if the offset value found is within the limits given by the ASD characteristics (acceptance window), see Figure 9.

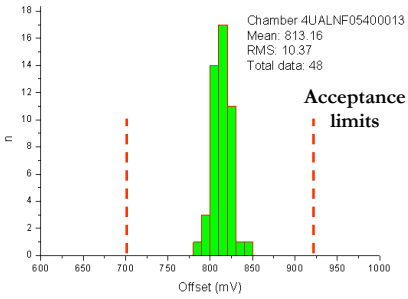


Figure 9 – Offset distribution example for the boards on an M5R4.

2) Noise rate versus threshold

After a fit of experimental data made using (5), the noise voltage (V_n) parameter is calculated. Using the calibration curve (Figure 4) this value is converted directly into an estimate of detector capacitance. Then, the calculated capacitance values for all channels are averaged and the mean value should be within 3*RMS from the nominal capacitance for the specific type of chamber under test.

The diagnostic routine subsequently verifies if Cdet of every channel is inside a 3 rms window (see Figure 10). If one or more channels are out of range, an alarm is raised; abnormal values are printed specifying their source.

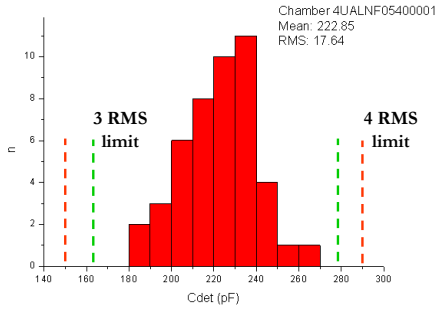


Figure 10 – Example of an estimated channel Cdet distribution for an M5R4 chamber.

3) Offset pattern recognition

From the threshold scan, a sequence of offset values can be obtained for the 16 channels of each FEB. This pattern is compared with the results obtained in the front-end mass production test, in order to check if the FEBs on the chamber have been correctly identified. Measurement data is archived to be used later; such data can be also utilized to identify chambers during their assemblage on the wall.

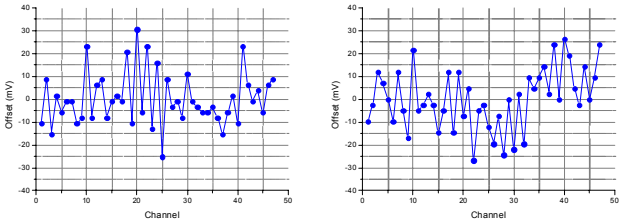


Figure 11 –Pattern (subtracting the average) of 2 M5R4 chambers.

C. *Noise rate at the nominal threshold region*

The LHCb Muon TDR [1] requires a maximum noise rate of 100Hz per channel for MWPCs. Recent studies of LHCb Muon Detector have shown that channels with a noise rate up to a few kHz are not critical.

The diagnostic tool is able to measure the electronics noise rate at different thresholds (in the vicinity of the nominal value). If the noise rate measured at (Thnom + Δ) is higher than 1 KHz, an error condition is signalled.

IV. Estimation of Cdet Measurement Error

The error of Cdet measurement has been estimated considering single channels tested at 4 different known capacitances (56, 100, 180 and 220 pF) with about 90 measurements per capacitance value (4 16-channels capacitor boards were built in order to perform such tests). The results showed that it is possible to measure a channel input capacitance with a precision better than 7 pF if all channels had been calibrated before executing tests; however, this is impractical due to the huge number of channels to test.

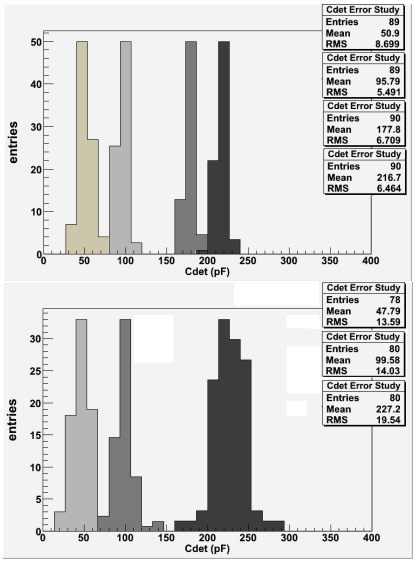


Figure 12 - Error measurement for a calibration curve per channel and per a group of channels.

When evaluating different channels of a group of boards the system becomes less accurate due to the spread on FE channels characteristics. The error found in this case was estimated to be 20 pF; Figure 12 shows measurement of 5 different FEBs with capacitances of 47, 100 and 220 pF. The accuracy of the measurements presented is satisfactory to evaluate chamber capacitance and single channels.

V. RESULTS

About 120 MWPCs from INFN production sites (Ferrara, Firenze and Frascati) have been tested to date; the results are presented here. During the tests, chambers with out of acceptable range values have been repaired. Therefore, all parameters shown in the measurements below are within specification.

A. M5R4 Frascati

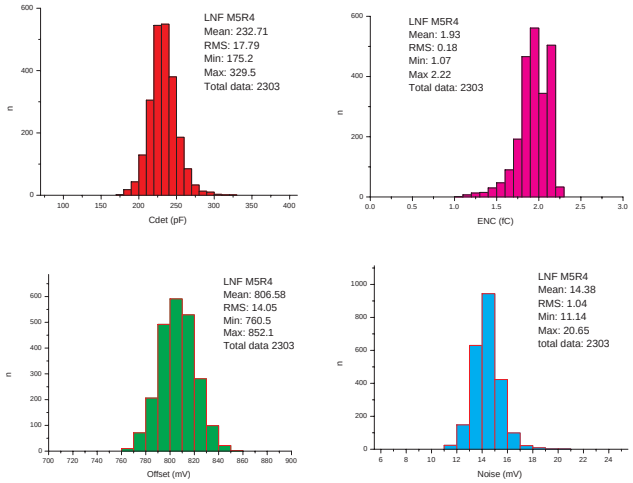


Figure 13 - Results for the LNF M5R4 chambers.

B. M5R3 Frascati

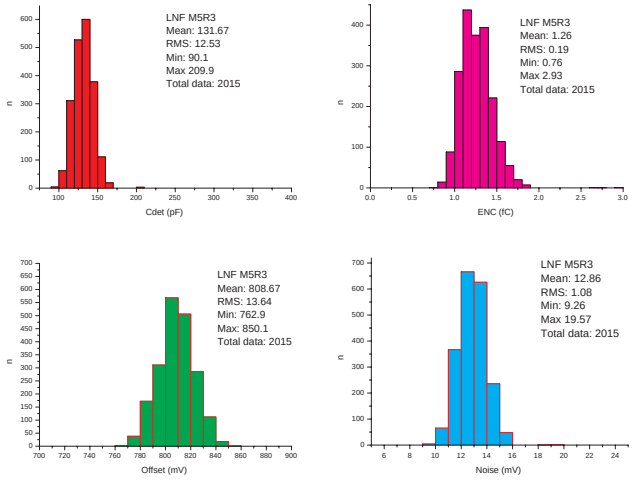
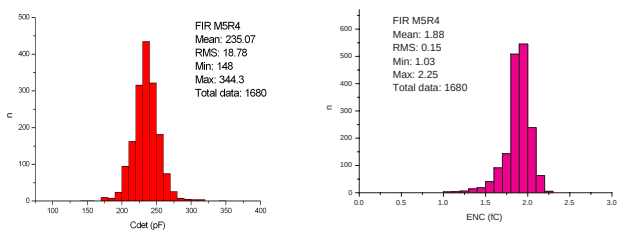


Figure 14 - Results for the LNF M5R3 chambers.

C. M5R4 Firenze



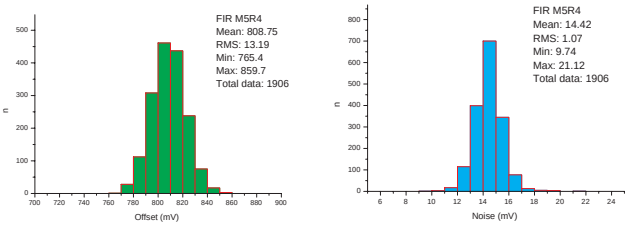


Figure 15 - Results for the Firenze M5R4 chambers.

D. M5R2 Ferrara

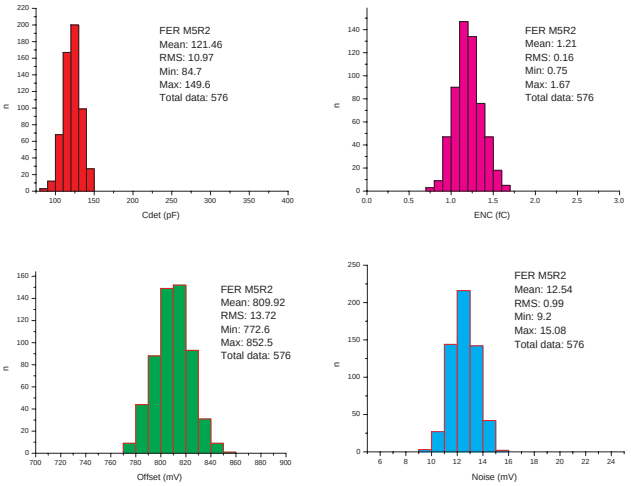


Figure 16 - Results for the Ferrara M5R2 chambers.

VI. CONCLUSION

The goal of this project was to implement an automatic and fast system (accessible also to non experts) for the mass production tests of LHCb Muon MWPCs. Chambers that do not pass the tests must be the object of remedial action. By means of using the diagnostic method presented, we aim at reducing to a minimum the number of chambers to undergo more time consuming test.

VII. REFERENCES

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Parallel Session A2

Readout, commissioning and integration

Integration and Installation of the CMS Electronics system

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Abstract

The electronics systems used to control, trigger, and acquire data from the four experiments at LHC are, for the field of High Energy Physics, of unprecedented level of complexity and sophistication.

In the case of CMS, the users are gaining access to the underground counting room (USC55) at a late stage with respect to the official LHC start-up date.

Measures taken to reduce the time required between when the access is granted for installation and the experiment is ready for physics are presented along with the current status and plans.

I. Introduction

When it became obvious that the CMS cavern was going to be delivered to the collaboration at a very late stage, measures were taken to cope with the situation. In fact, neither the underground counting room USC55, nor the underground experimental cavern UXC55, is fully available for electronics installation to date.

In order to allow pre-integration of subsystems prior to installation in USC55 an Electronics Integration Centre (EIC) has been put in place.
All subsystems have also means to make internal tests between on-detector electronics and the part of the electronics system to be installed in USC55. As an example, the integration centre of the silicon tracker in building 186 has a quarter of the readout electronics installed in order to fully test the detector before it is transported to the experimental cavern for final installation and commissioning.

II. The Electronics integration centre

An Electronics Integration Centre (EIC, in building 904, CERN), used by all electronics subsystems across CMS, was created in order to allow system integration to take place during the year before any electronics could be installed in the underground counting room. The goal is to use, as far as practical, the same technology and the same techniques in the EIC as will be used in the underground counting room.

The electronics integration centre is currently being intensively used by practically all subsystems, including the Detector Security System (DSS) which is, as in USC55, responsible for the safety in the racks where the electronics modules under test are located.

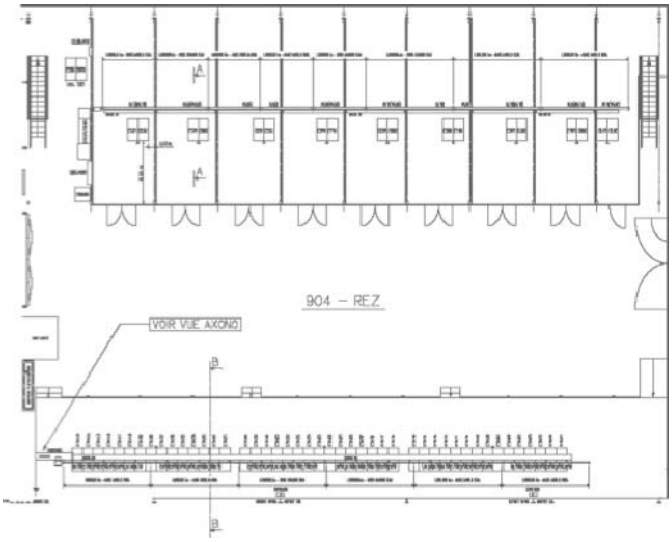

Figure 1: Drawing of the EIC: The “private” labs on top and the integration area on the bottom

Every subsystem has a “private” room allocated in which two standard racks, a cupboard, and a workbench is available. The “private” room is intended for test and development of the electronic modules used in the subsystem.

The integration centre provides also three rows of 15 standard LHC racks with water cooled heat exchangers. One row is used for system integration, one for sub-system burn-in, and the last row for burn-in of low voltage power supplies.



Figure 2: The integration area in the CMS Electronics Integration Centre; the first 15 racks are for system integration, the second 15 are for burn-in, and the last 15 racks are being used for burn-in of the low voltage power supplies.

III. The cosmic challenge during the CMS magnet test

As an additional test, most subsystems contribute to an integration test attached in time to the CMS magnet test with the goal to detect, trigger, and read out events originating from cosmic particles. The event goes under the name Magnet Test Cosmic Challenge (MTCC).

Fractions of the sub-detectors have been mounted in the final positions inside and outside the large solenoid which contributes with the S in CMS. A complete slice of the electronics for the control, trigger, and readout systems is deployed, providing the opportunity to test and verify the interoperability of the sub-detector electronics systems with the level 1 trigger and the DAQ system before the experiment is lowered and installed in the and the CMS electronics system is finally installed for commissioning in the underground control room.

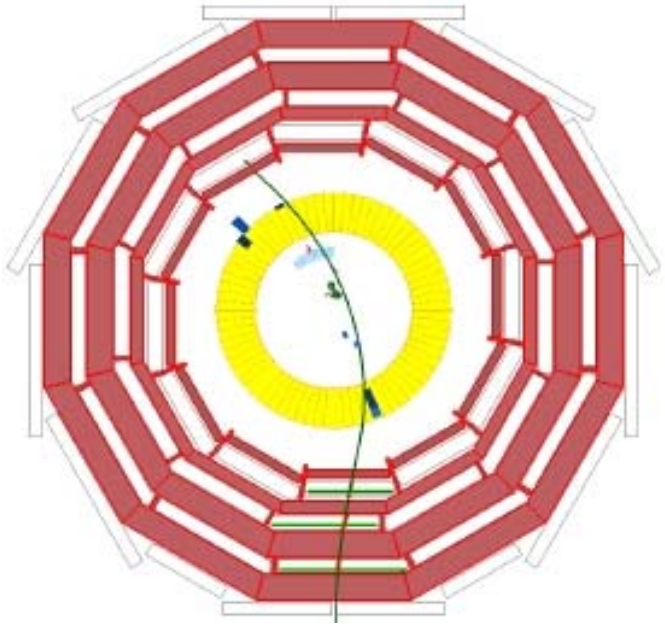

Figure 3: MTCC event display showing a cosmic muon making a trace through the HCAL, the ECAL, and the tracker, and out through the barrel muon detector (DT) on the bottom, actually proving that these sub-systems perform together in a magnetic field of 3.8T.

IV. Installation of electronics subsystems in USC55

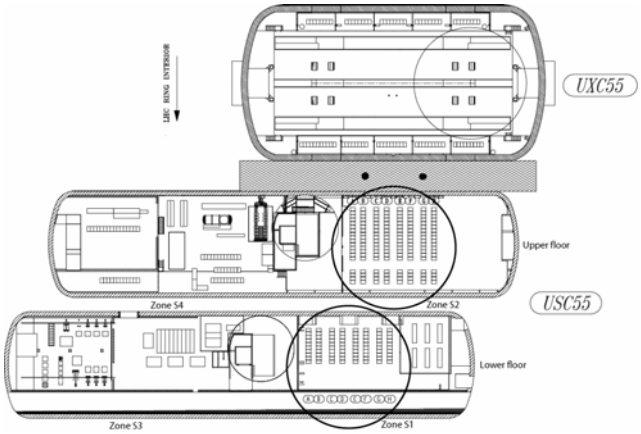

Figure 4: Point 5 Underground Area; The experimental cavern UXC55 with the adjacent, albeit a 7 meter thick concrete wall, underground counting room USC55, consisting of two floors.

A. *Installation readiness*

After a successful integration in the EIC, every subsystem has to go through an installation readiness review where every system having a direct interface has to agree that no visible problem exist. This review is estimated to be a useful preparation for installation, leaving only the new interconnects to verify during and after installation. Obviously, if a sub-detector has successfully participated in MTCC, the sub-system is considered as being ready to be installed.

B. *The overall plan*

The overall plan for installation of support infrastructure at point 5 is vast and very difficult to overlook. It integrates the day to day work of external subcontractors performing a large variety of tasks, including installation of cables, cooling and gas pipes, security systems, etc. The responsibility for the overall plan and the coordination of the work is with the CERN group TS-LEA.

C. *The Electronics installation plan*

The plan for the electronics installation in USC55 has initially been developed together with TS-LEA. As the site becomes ready, the actual plan for the electronics installation is detached.

Currently, the only resource considered in the plan for the electronics installation is space. It has been assumed that, on average, the time needed to install one rack of electronics in USC55 is one week. During this time, the access to the front and to the rear of the row of racks is prohibited to other groups. The outcome of the planning exercise is that the whole counting room should be possible to install and test in three months, including internal testing with local DAQ.

The result is a detailed day to day program. It is to be understood that the planning only provides an indication about the priority between the subsystems. In fact, almost half of the S1 level of USC55 is housing the readout and control system for the tracker, one quarter the global and muon triggers and the TTC (Trigger, Timing and Control), and the last quarter the readout of pixels, barrel muon drift tubes (DT), and end-cap muon chambers (CSC). The S2 level has

mainly ECAL readout and high voltage, HCAL readout and high voltage, and the regional calorimeter trigger (RCT).

As can be noticed in figure 4 and figure 5 the S2 floor is more advanced than S1. There are several reasons. First of all, before any useful tests can be done involving readout electronics the PC area, located in S2, has to be ready and powered. This is actually possible only since one week. The real reason, however, is a problem with failing cooling manifolds. When the bad quality of the manifolds was discovered during a final reception test in June 2006 it was decided that the S2 floor had to be dealt with first since any leaking water could damage equipment installed in S1.

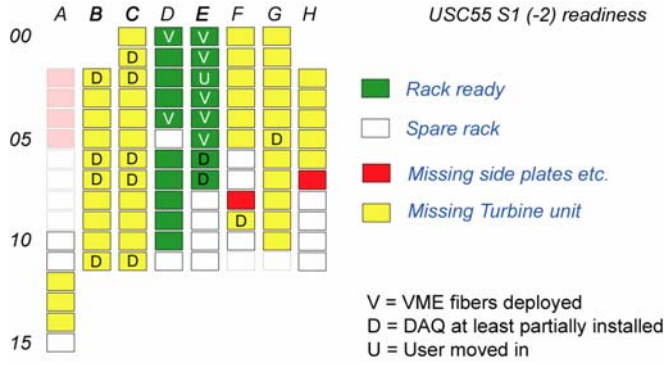

Figure 5: Electronics installation readiness of the USC55 S1 floor

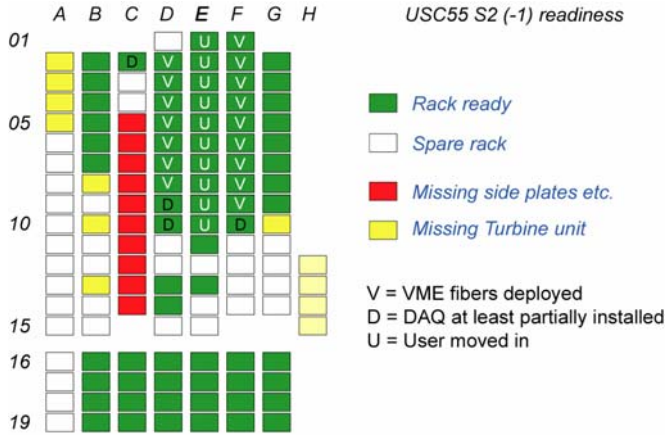

Figure 6: Electronics installation readiness of the USC55 S2 floor

Considering that that point 5 is a construction site only partially in the hands of the users, the installation of each subsystem has to follow the program with great precision, i.e. start and finish on time. Failing to do so, the user might see the access to the underground control room refused the next morning due to some scheduled event.

V. Installation Status

Considering the Electronics installation readiness of the underground control room it is easy to understand that not much electronics has been installed to date in USC55. The electronics subsystem are, however, practically all ready for installation, several in their entirety. The approximate production and integration status for different subsystems can be found in table 1.

Table 1: Subsystem production and integration status

Subsystem	Production Status	Integration Status
Pixel	Preseries	No
Tracker	100%	MTCC OK
ECAL readout	75%	MTCC OK
Preshower	Prototype	No
HCAL	100%	MTCC OK
DT readout	75%	MTCC OK
DT Track Finder	75%	MTCC OK
RPC trigger	In production	MTCC OK
CSC readout	100%	MTCC OK
CSC Track finder	100%	MTCC OK
RCT	100%	MTCC II
GCT	Prototype	No
GT	100%	MTCC II
TTC	100%	MTCC OK
DAQ	100%	MTCC OK

The status of the physical installation in the USC55 can be found in table 2. Please note that so far no electronics integration has been possible due to lack of power in the PC racks.

Table 2: Subsystem physical installation status

Subsystem	items	Integration
HCAL	HTR crate	5%
RCT	Infrastructure	100%
TTC	Infrastructure	25%
DAQ	User interface	75%

The official target dates for different levels of operation can be found in table 3. Considering the installation readiness of the subsystems, these target dates are considered reasonable.

Table 3: Installation target dates

Milestone	Target date
Ready for powered crates	October 2006
Electronics installation	October – December 2006
System commissioning	January to March 2007

VI. Maintenance of Electronics Systems in EIC

After completion of the electronics system commissioning, the EIC facility will continue to serve as a centre for hardware, firmware, and software development. This development may be either for upgrades, or to achieve the design performance of the experiment.

The task to develop new firmware builds, actually solving more problems than they create, is likely to become major. No guarantees can be given that the initial developers, who have the detailed knowledge about how and why the system actually works, are available even one year after the first physics run. Thus one important task may be to educate new experts, capable of understanding the detailed behaviour of the hardware and firmware. The value of having a complete slice of the experiment, at least for the level 1 trigger system, cannot be overestimated.

The plan is to provide such a slice in EIC, after the CMS electronics system has been commissioned, throughout the lifetime of the experiment.

VII. References and Acknowledgements

This paper is based on information obtained through private communication with Jordan Nash (CERN PH/CME), Tim Christiansen (CERN PH/CMM), Jan Troska (CERN PH/MIC), Wesley Smith (University of Wisconsin), and information obtained during numerous meetings and through work at the CMS experimental site (Point 5, Cessy, France).

[2]

Installation and Commissioning of the On-Detector Electronics of the CMS Electromagnetic Calorimeter

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Abstract

The CMS electromagnetic barrel calorimeter is composed of 76,000 $PbWO_4$ scintillating crystals. The scintillating light is captured by photodiodes, amplified and digitized. The conversion is performed inside the detector volume and data are transported through optical fibers to the off-detector electronics. About 25,000 Printed Circuit Boards of 5 different types and 5,500 Gigabit-Optical-Links and fibers should be installed and tested. The integration of electronics, cooling system, mechanical supports, low and high voltage distribution, synchronization and controls are discussed. Each step of the assembly sequence is followed by extensive test and quality control. Installation, commissioning strategy and the achieved system performance results are presented.

I. INTRODUCTION

A very high performance and homogeneous electromagnetic calorimeter [1] is an essential part of the CMS experiment [2]. It is designed to operate in a 4 Tesla magnetic field, in a ~ 2 kGy/year radiation environment and at the LHC bunch crossing rate of 40 MHz. This challenging requests and the energy resolution needed to detect the postulated two photons decay of the Higgs Boson have driven the design of ECAL. Lead tungstate scintillating crystals [3] have been chosen because of fast scintillation, short radiation length and small Moliere radius. The scintillating light from a crystal is detected by two avalanche photo-diodes (APDs). In order to achieve the design energy resolution, the crystal and APD temperature has to be kept constant to a high precision, and the crystal transparency, which varies with irradiation, has to be monitored and corrected. The signal amplification and digitization, including the formation of Trigger Tower sums on each group of 25 crystals, is performed inside the detector volume and transported through high speed links (optical fibers) to the counting room. Lower speed links are used to transport timing and control information to and from the detector. This scheme requires a large quantity of radiation hard electronics installed on the detector. Moreover the electronics must be highly reliable since it will not be accessible during data taking. For these reasons all the chips are manufactured in 0.25µm CMOS technology to guarantee radiation hardness and low power consumption.

A. The ECAL Barrel OnDetector Electronics

The CMS electromagnetic barrel calorimeter is composed of scintillating crystals grouped in 36 independent supermodules of 1,700 crystals each. The basic block of the electronics is a Trigger Tower made of 5x5 crystals [4]. It contains one Motherboard, five Very-Front-End (VFE) boards, one Front-End (FE) board, one Low Voltage Regulator (LVR) board and two Gigabit Optical Hybrids (GOH) (see Figure 1).

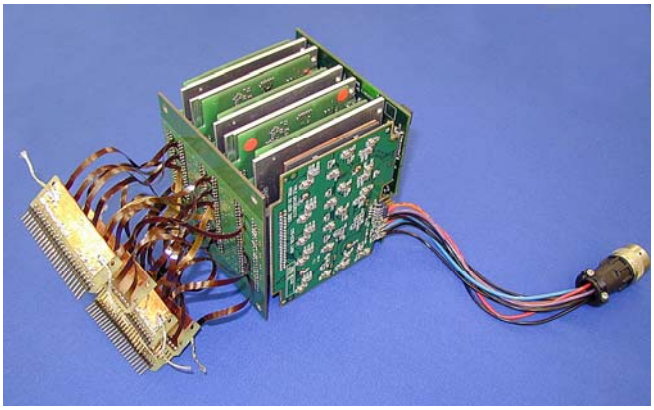

Figure 1: The readout electronics of a trigger tower, the basic electronics serving 25 crystals.

The Motherboard is connected to the avalanche photo-detectors by flexible kapton ribbons and distributes the bias voltage to the APDs and the low voltage from LVR to the VFEs. The LVR stabilizes the low voltage and contains three Detector Control Units (DCU) to monitor input and output voltages and cards temperatures. The VFE consists of five identical readout channels, each one consisting of a multiple gain preamplifier (MGPA) [5] with gains 1, 6 and 12. The three analogue outputs are digitized in parallel by three of the four channels of a 12-bit 40MHz Analog to Digital Converter [6]. The highest, non saturated signal is selected by the ADC integrated logic and stored in a buffer. On the FE board, the data are stored during the 3 µs latency of the trigger Level-1 Accept signal, while the trigger-primitives are calculated and transmitted. For these purpose two GOH boards, one for data and one for trigger, are used. They house a data serializer, a laser driver chip (GOL) and a laser diode with an attached fiber pigtail, 2 m long. Each FE hosts a Clock and Control Unit (CCU) integrated circuit which serves a I^2C interface to control the 68 trigger towers of the supermodule through a system of 8 token rings. A redundancy path guarantees the functionality of a token ring in case of non-operational FEs, provided that they are not consecutive. Each supermodule contains about 600 PCBs (340 VFE, 68 FE, 68 LVR, 68 MB and 8 token-ring link-boards TRLB), 138 Gigabit Optical Links, 17 LV distributors and 12 distributed fiber patch-pan-

els. Each PCB element arrives fully qualified and labelled with bar codes.

For each supermodule a total amount of about 4.6 kW of heat has to be removed by the cooling system in order to keep the crystal temperature within the specified tolerance of ± 0.1° K.

B. The ECAL Barrel Off-Detector Electronics

The off-detector electronics has a modularity of one supermodule served by three 9U, VME64x compliant boards. A Clock and Control System (CCS) board initializes and controls the on-detector electronics. It also receives the LHC clock, the control signals and the trigger L1A and distributes them to the on-detector electronics and the other off-detector boards. A Trigger Concentrator Card (TCC) encodes the trigger primitives, transmit them at 40 MHz to the Regional Calorimeter Trigger (RCT), and stores them awaiting for a L1A signal. Then, upon receipt of a L1A signal, it transmits to a Selective Read-out Process (SRP) a classification of the trigger towers according to their energy deposits. A Data Concentrator Card (DCC) receives the supermodule data at the trigger L1A rate, performs integrity controls, reduces the data size via zero suppression and selective read-out, formats the data including the trigger primitives retrieved from the TCC, and transmits them to the central data acquisition.

C. Installation Sequence

The on-detector electronics is installed and tested at an integration area at CERN, Prevessin site (see Figure 2).



Figure 2: The electronics integration area at CERN. Installation can proceed in parallel on up to four supermodules.

This center is located in a huge assembly hall where trucks can enter and overhead cranes are available to load and unload supermodules. To cope with the construction schedule we have prepared three completely independent assembly stands. Each one consists of: a support stand; a cooling unit; a CAEN HV system powering the 34 channels; a Wiener LV system to power the 17 low voltage channels of one supermodule and 3 additional low voltage channels used to temporarily power trigger towers during tests; a readout system for single trigger towers; a database and shared services as the detector control system and the laser. Some extra stands with partial assembly components are also available. Beside the integration and test zone there are several areas to prepare and test electronics components and mechanical parts and an air-conditioned storage room for up to 20 supermodules.

After a supermodule arrives in the electronics integration area it is installed in a support stand and connected to services. The correct HV settings are retrieved from the database and all connections of the motherboards to the APS's and temperature sensors are tested. Then the integration sequence proceeds in steps, by installing:

- Trigger Tower electronics (first VFEs and LVRs, then FEs).
- Token-rings including TRLB.
- GOHs, optical fibers and fiber patch-panels.
- LV distribution cables and patch panels.
- Commissioning: one week operation and test of the completed supermodule using the standard CMS DAQ and control systems identical to the one that will be used in CMS.

At each step the bar code of installed components and their locations are registered into a dedicated database (CRYSTAL). The program verifies that each card has been previously registered in the database as good for installation and adds the location.

Installation sequence is optimized but still each phase covers the previously installed items so, given the complexity of the system, a full validation of each step is necessary. Extensive testing is part of each installation step to evaluate the full functionality and performance.

VFE cards are prepared by mounting an aluminium front cover, but first we apply a thermally conducting gap filling paste on the components side to ensure a good heat transfer. On the outside of the cover, we put 5 strips of 1mm thick gap pad to provide an efficient thermal contact to the cooling bars. The cover is alodined and connected to the ground plane of the VFE cards. Three captive stainless steel screws are mounted on the front covers to be used later to fix the cards to the cooling bars. The LVRBs are prepared similarly but their front cover is electrically isolated from the cards. FEs are prepared by gluing 3 strips of 1.5 mm thick gap pad in the places where they will touch the cooling bars.

The installation starts with the mounting of the VFE and LVR cards. Five VFEs and one LVRB are inserted on motherboard connectors and then fixed to the cooling bars. The procedure is repeated for all 68 trigger towers. Next the FE is mounted on top of each trigger tower. They have different CCU-IDs soldered so they need to be sorted to match the numbering scheme. In a supermodule the numbers from 1 to 68 are used for the trigger towers.

As a trigger tower is completed, it is connected to a dedicated VME read-out and its full functionality is tested as explained in a dedicated section.

Once all trigger towers are checked completely functional, the token rings are installed. First the four TRLB, each serving two token rings are installed and fixed to the cooling bars. Starting with rings 7 and 8, the token ring cables are installed on the FE cards and the TRLB (see Figure 3). The control fiber ribbon is connected to the PCI PEC in the test stand and all towers in a token ring plus the TRLB are powered. De-

fault and redundancy path are tested to check the functionality of the TRLB and the correct cabling.



Figure 3: A supermodule after Trigger Towers and Token Rings installation.

Then, the GOHs (see Figure 4) for data and trigger links are installed together with the distributed fiber patch panels (DFPP), one each 12 channels of data and one for 12 channels of trigger. The DFPP contains a single fiber to a 12-way ribbon adapter. The extra-length of the GOH pigtail is stored in the DFPP. The routing of these optical fibers should be done rather carefully since they are fragile and a bending radius of ~ 4 cm should be respected. The correct operation of each individual GOH is verified by connecting the single fiber coming out from each box to the in-line patch panel. Every trigger tower is then tested again using the same software but now each tower is using its final links.

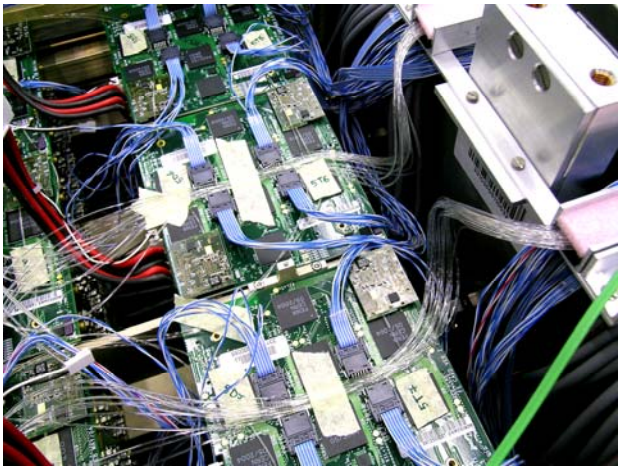

Figure 4: GOHs , optical fibers and Token Rings installation.

At this point the final low voltage distribution [7], made of 17 low voltage bus-bar, is installed together with their support plates, covering completely the on-detector electronics as shown in Figure 5. Each of the bus-bar connects to 4 trigger towers and to the corresponding TRLB. The power inputs connectors are fixed at the supermodule patch panel. A remote sense cable with 17 twisted pairs of wires terminated with a 37-pin connector at the supermodule patch panel is connected to the input of the 17 LVDs. Three inhibit cables terminated with 50-pin connectors are installed at the supermodule patch panel to control the LVDB. The voltages and correct assignment of the inhibit channels is verified.

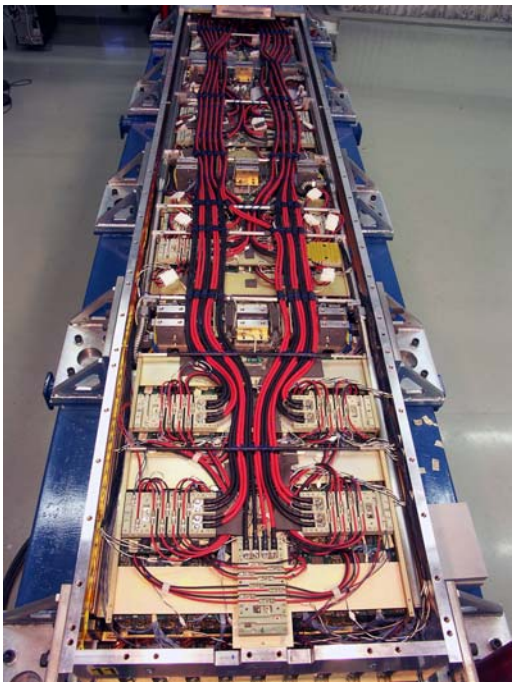

Figure 5: Overview of a completed supermodule. The low voltage distribution layer on top, is visible.

D. Single Trigger Tower Testing

The testing of individual trigger towers explores the full functionality of the corresponding channels and assesses their performance. It uses a dedicated VME read-out and a graphic data analysis interface.

The test sequence is the following:

- The communication of the CCU of the TT is verified by reading the CCU-ID on the FE, which should match the trigger tower location number in the supermodule.
- All devices connected to the 16 I^2C interfaces of the CCU are checked by scanning their addresses.
- The registers of FE and of the MGPA of the 5 connected VFEs are initialized, read back and their correctness is verified. For the FE case this insures the accessibility of all important registers. It includes setting the enabled channels, the power of GOHs, the transmission mode of optical links, the pipeline delay, the number of samples per trigger, the peak finding status, the filter parameters for the trigger and loading the pedestal values. In the MGPA case the registers are read for each individual channel. These registers are the calibration pulse enable, the pedestal DAC value for each gain and the test pulse amplitude, for each gain.
- A pedestal DAC values scan followed by a line fit is performed for each channel and each gain. Values are set to give pedestal mean values (200 ± 15) ADC counts A

typical distribution of pedestal averages is shown in Figure 6.

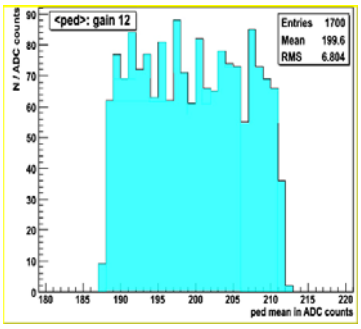

Figure 6: Pedestals mean value distribution for gain=12, all channels.

Using the obtained pedestal DAC settings the pedestals are measured. A total of 100 events, 10 samples each, are collected. The total noise is calculated as the r.m.s. value of all 1,000 samples. A low frequency contribution is estimated from the r.m.s. of averages per event. These measurements establish the performance of the readout and at the same time verify the correct operation of the full readout chain. A typical distribution of pedestal r.m.s. is shown in Figure 7.

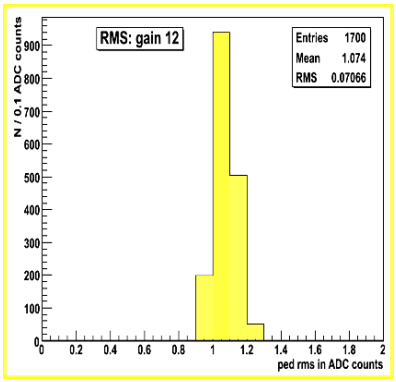

Figure 7: Pedestals noise distribution for gain=12, all channels.

The measure is repeated with HV on and off to check the correct connection and biasing of the APD, since the noise (r.m.s. of the pedestal) depends on the capacitance connected to the MGPA.

- For each channel and gain, mean amplitudes and r.m.s. of 10 test-pulses, injected using the generator internal to MGPAs, are measured and compared with the expectations (as shown in Figure 8). The same is done for the trigger channel. This test pulses are used to calibrate the electronics.

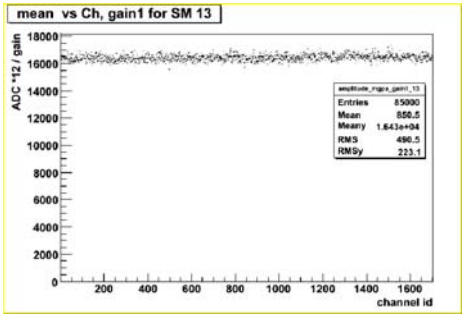

Figure 8: Test pulse amplitude distribution for gain=1, all channels

- Finally, using the DCU chips installed on the LVRB and VFEs, the low voltages and temperatures of the electronic cards , the APD leakage currents and their temperatures are measured.

A pulsed laser is available to test the full chain from crystal to optical fibers outputs (Figure 9). The same trigger tower test system is also used to read the signals of laser light injected into the front face of the crystals. This allows a validation of the full readout chain including crystals and APDs.

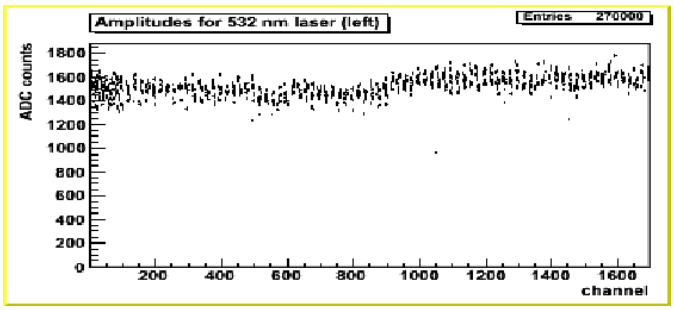

Figure 9: Laser signal amplitude distribution, for half a supermodule.

E. Commissioning of a Supermodule

Once a supermodule is completed it is operated at the electronic integration center for at least seven days. All problems discovered during this period are corrected, if possible. The standard CMS off-detector electronics system is used and it is controlled by the latest stable version available of the CMS-ECAL data acquisition software. Four different types of running mode are used in the data taking sequence:

PEDESTAL SCAN - to determine the DAC setting for pedestals mean values ~ 200 ADC counts.

PEDESTAL RUN - to measure with the above setting pedestal mean values, r.m.s. for all channels and all gains.

TEST PULSE RUN - to measure the amplitudes, for all channels and all gains, of the pulses injected by MGPAs at the input of the amplification chain.

LASER RUN - to measure the amplitudes of laser pulses injected in each channel.

At the end of each run a monitoring program is launched automatically to execute a series of control tasks, including a check of data integrity, pedestals and r.m.s., laser and test pulse amplitudes. Summary plots and reports containing detailed information are stored into web pages. They are easily accessible through browser application and provide immediate feedback for possible intervention.

The CMS Detector Control System (DCS) and ECAL Safety System (ESS) are used to monitor at all times low and high voltage, temperature and cooling system, allowing safe and unattended operation of the supermodule.

F. Results

23 supermodules have been assembled until now. As estimated it takes about 4-5 weeks to complete a supermodule achieving a very good quality and excellent performance.

For the first 19 supermodules assembled, corresponding to 32,300 channels, 278 problems were found and interventions

done corresponding to 8.6 per-mills of the channels. 63% of the interventions were done during the installation of electronics components, 36% during the commissioning. Several types of typical problems (noisy channels, one or more gains not functioning, bit 11 problem, HV capacitor problem) have been classified and are found and solved systematically. In 78% of the cases the problem was solved by changing a component. Problems still remain in 62 channels corresponding to ~ 0.2%. Of these 32 channels are not working and 30 channels expose problems, i.e. showed a lower response to the laser pulse that seems related rather to bad optical connection of the laser fiber. The response can be verified with cosmic muons or with the test beam data.

G. *Status and Plans*

The integration and commissioning of the supermodules of ECAL barrel is proceeding well despite a slow down during the summer months due to MB problems related to some deliveries of bad quality kapton (bubbles and badly controlled etching). Figure 10 shows the commissioned supermodules and the planned schedule.

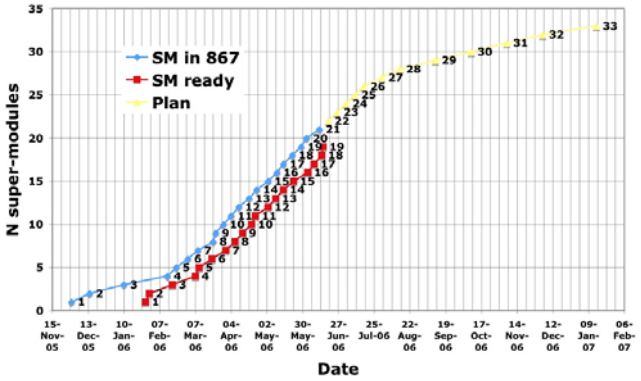

Figure 10: The integration progress in time showing the number of supermodule arrived so far to the integration center, the number completed and the schedule for the future months.

Until now 23 supermodules are completely commissioned, 20 have gone through cosmic data taking and 4 have been calibrated with an electron beam (see next paragraph).

The installation and commissioning of the 37 (36 + 1 spare) barrel supermodules shall be completed by early spring 2007.

H. *Cosmic Ray, Calibration on a Test Beam and Other Data Taking*

After the week of commissioning in the electronic integration center the supermodule is transported to a cosmic calibration stand. Ten days of cosmic ray data are collected. The supermodule is operated in stable environmental condition for 24 hours a day with no shifters, supervised by the already mentioned DCS and ESS. Besides the normal cosmic ray data taking, a sequence of pedestal, test pulse and laser runs is recorded regularly. Each run is analyzed automatically by the monitoring program immediately after completion of a run and re-analyzed later to extract crystal inter-calibration constants. The main goal is to achieve a further calibration of the crystals [8] in addition to laboratory and test-beam calibrations. But an important added value is the addition of a period of continuous running.

In this months different supermodule operations are ongoing at CERN. A subset of commissioned supermodules is calibrated with an electron beam at the H4 beam line in the North Area. Up to now four supermodules have been calibrated. Another supermodule is taking part in a combined hadronic and electromagnetic calorimeter test beam at the H2 beam line. At the CMS surface global integration area, two other supermodules together with sectors of the CMS detector are participating in the CMS magnet test and cosmic challenge (see Figure 11).



Figure 11: Two supermodules installed in CMS and the proud installation team.

I. *Conclusions*

The on-detector electronics installation sequence, test strategy and procedure are described and results of the system performance achieved are presented. The procedure for integration is well established and has improved with the accumulated experience. The commissioning of CMS ECAL barrel is proceeding steadily in compliance with the CMS installation schedule. The standard CMS-ECAL off-detector electronics, acquisition software and detector control and safety system are continuously used during commissioning, cosmic ray calibration, test beam calibration and CMS magnet test facility. The supermodules functionality and performance is tested both in standalone and in concert with other CMS subdetectors. A very good quality standard has been achieved with a level of channel failure down to a few per mills.

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Performance of the CMS ECAL Very Front End Electronics

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Abstract

We report the results of tests of 12880 Very Front End (VFE) readout cards for the barrel of the CMS electromagnetic calorimeter. A thorough test sequence was applied to each card including power-on test, burn-in and final calibration.

Cards failing the tests were at the few per mille level. The results prove the very high quality of the VFE cards.

I. Introduction

The CMS [1] electromagnetic calorimeter (ECAL) is divided into the Barrel (EB) and two end-caps (EE) made of 61200 and 14648 crystals, respectively. The EB is split up into 36 supermodules with 1700 crystals each [2]. The EE is made of 4 DEE's with 3662 crystals each.

The scintillation light of the crystals is converted into an electrical signal by two Avalanche Photo-Diodes (APD) for the EB. The Very Front End (VFE) card is used to amplify, shape and digitize the signals coming from the Avalanche Photo-Diodes. The VFE comprises five identical read-out channels, serving five crystals.

Each channel has a Multi Gain Pre-Amplifier (MGPA) [3] and a four channel ADC followed by LVDS to CMOS level-converters (LVDS_RX). The signals are pre-amplified and shaped and then amplified by three amplifiers with nominal gains of 1, 6, and 12, covering a dynamic range of 60 pC. The shaping is done by a CR-RC filter with a shaping time of 40 ns. The output pulse non-linearity of the MGPA is less than 1%. Its noise, in the Barrel case, is about 8000 electrons for gain 6 and 12, and about 28000 electrons for gain 1. The MGPA contains three programmable 8-bit DACs to adjust the output signal levels to the ADC inputs. An integrated test pulse generator with amplitude which is adjustable through an 8-bit DAC allows a test of the read-out electronics over the full dynamic range.

The 3 analog output signals of the MGPA are digitized in parallel by a 4-fold 40 MHz 12-bit ADC (AD41240) [4]. It has an effective number of bits of 10.9. Digital logic internal to the ADC selects the highest not saturated pulse for output. A Detector Control Unit (DCU) measures the leakage currents of the five Avalanche Photo Diodes. In addition it measures the resistance of thermistors which are attached to every 10th crystal hence monitoring the temperatures.

Each VFE is identified by a barcode (figure 1). This allows its unique identification and registration into a data base.

All active components are application specific integrated circuits (ASICs) implemented in 0.25 μm technology.

The electronics production for the ECAL Barrel and the tests of all 12880 VFE cards, which corresponds to 340 cards per supermodule and spares, is completed. The electronics production for the ECAL end-caps is on going.

The test sequence included:

- Automatic Optical Inspection (AOI) done by the manufacturer.
- Power-on test: It is the first electrical test of the VFE cards. It measures the voltages, the currents and performs a functional test of the card.
- Burn-in [5] test for 72 hours at 60 ºC.

Calibration of the characteristics of each individual channel by measuring the gain in units of ADC counts per pC, the pedestal, the noise, the linearity including a complete functional test.

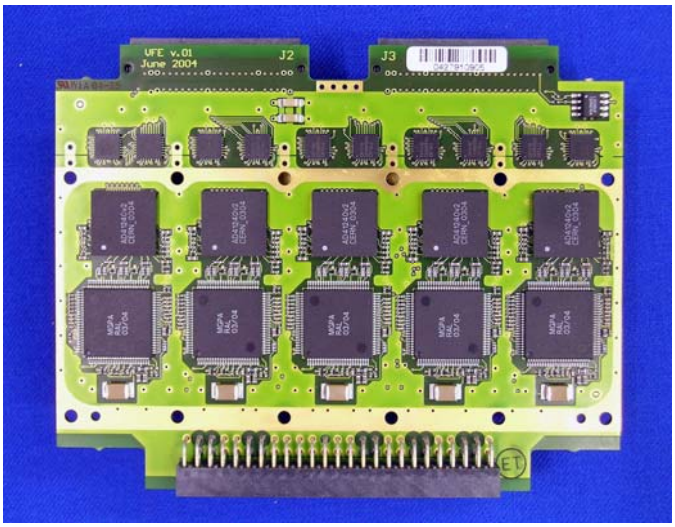

Figure 1: Very Front End card

II. POWER ON TEST

The power-on test [6] is a quick (~30s) electrical test of the VFE card [7]. All VFE cards are tested twice, once by the manufacturer (ASCOM Schweiz AG) before delivery and after reception in the ECAL electronics integration centre at CERN. Three copies of the test system have been built: one system is at CERN and two are at the manufacturer.

The test system is composed of a programmable power supply, a barcode reader, a dedicated electronics board which includes a Xilinx FPGA, and one NI DAQ card. A Labview program interfaces the test system via RS232 bus.

The VFE needs three separate supply voltages of 2.5V: one for the MGPA and the analog part of the ADC, one for the digital part of the ADC and a third one for the LVDS to single ended CMOS buffers (LVDS-RX converter). The output voltage of the power supply and the 3 input voltages of the VFE card are measured with a NI DAQ PCI-6013 card. The corresponding currents are determined by measuring the voltage drops over calibrated shunt resistances with nominal value of 0.033Ω.

A functional test of the VFE is performed using the Xilinx FPGA to acquire the data digitized at 40 MHz:

It records and analyzes the data generated by the MGPA's internal test pulse system.

It selects the ADC gain modes.

It reads simulated APD leakage currents and crystal temperatures from the DCU.

The FPGA triggers and reads one pulse per channel and verifies the correct shape of the signals. It collects 64 equidistant samples and determines the pedestal, the noise and the amplitude of the three output pulses and calculates the real gain of every channel. Pulse heights and pedestal are compared within defined limits. The pulse shapes are plotted and the calculated numbers are printed on the front page of the test program (see fig.2).

The system also measures the leakage current from the DCU and the temperature. The results of the power-on test are stored in two different text files, one for voltage and current and another for the functional test.

The distribution of the analog, digital and buffer voltages measured by the power-on test are Gaussians with mean values of (2.489, 2.499 and 2.45) V and RMS errors of (0.001, 0.001 and 0.03) V.

The distribution of the currents are Gaussian with mean values of (1.482, 0.529) A and with RMS errors of (0.008, 0.01) A, respectively for the analog and the digital part; the buffer current is included into the digital measurement.

Of the 12880 VFE cards produced, 109 cards were rejected during the power-on test.

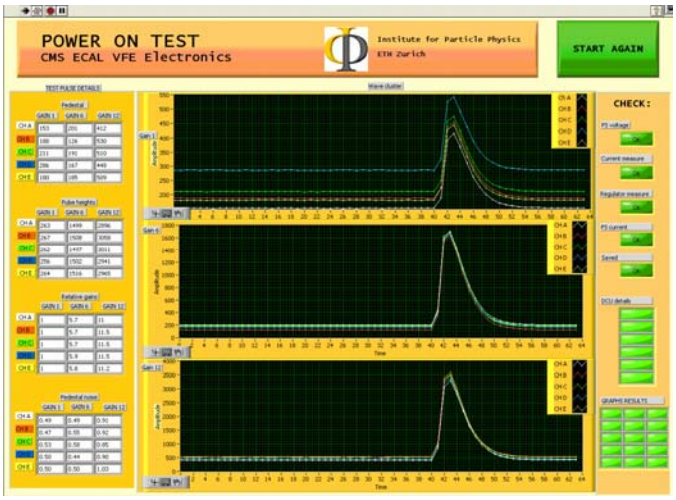

Figure 2: POT front page: on the left pulse height, pedestal, noise and relative gains are given. On the right the plots show the pulse shape of the 3 gains.

III. BURN IN

All the ECAL Barrel VFEs that have passed the power-on test are burned-in.

The burn-in [8] [9] is carried out to find infant mortality failures and freak failures and to guarantee the device's reliability. Typical problems that can be observed during burn-in are for example broken chips, bad soldering or nearly open bonds. They usually occur in the first 20 hours of the card's operation.

Freak failures result from defects in the component's structure leading to a hot spot. The lifetime of freak failures is usually higher than infant mortality failures.

The tests are performed at higher temperature since the failure rate depends exponentially on the temperature; according to the Arrhenius model the reaction rate varies as $e^{-Ea/kT}$ with an estimated activation energy of E_a = 1 eV. Thus the aging of the device is 100 times faster if its operating temperature is increased from 25°C to 65°C. Therefore a burn-in period of 3 days at an elevated temperature of 60°C has been chosen. Up to 300 cards are tested in one go. All cards are powered at their nominal voltage of 2.5 V during the test. The 40 MHz clock is distributed to the cards using a special mother board. A PC workstation monitors the clock and the total current of each of the 300 VFE cards.

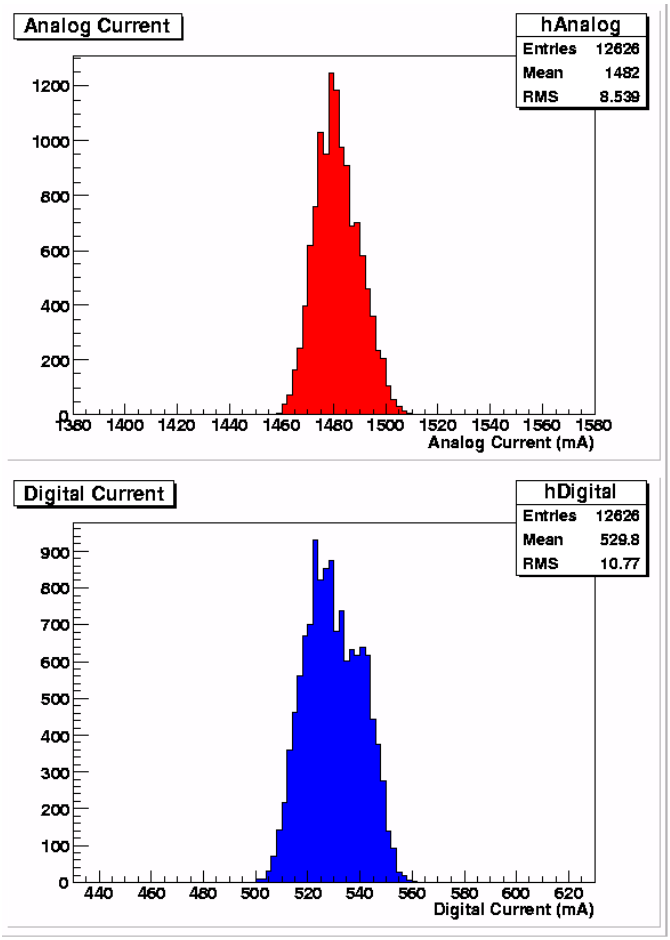

Figure 3: analog and digital current distribution for the whole production of VFE for the ECAL BARREL

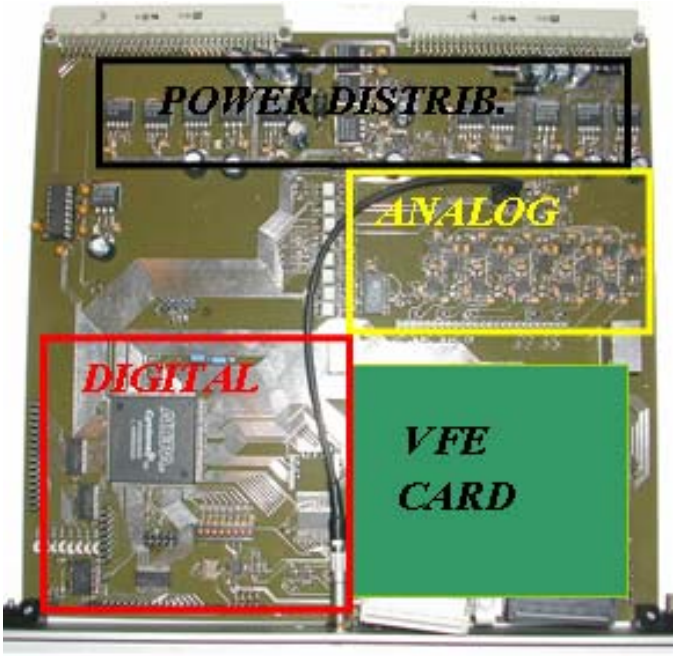

Figure 4: the calibration board

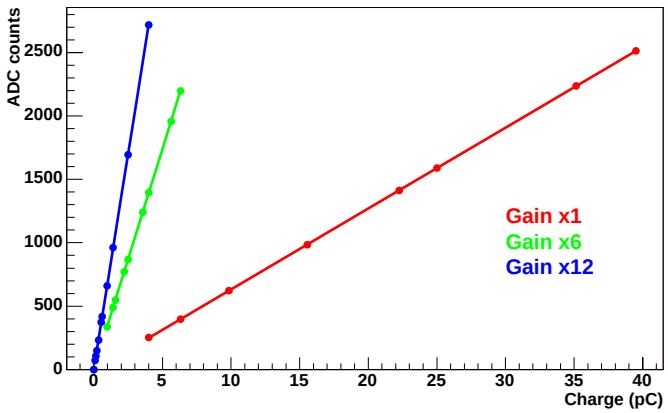

Figure 5: typical set of calibration curves for the 3 gains of a single channel of a VFE card.

IV. CALIBRATION TEST

The calibration test [6] [8] determines the characteristics of each channel by measuring the pedestal, noise and the linearity for the three different gains.

The calibration set up comprises:

- Six calibration boards (fig. 4).
- an Agilent 33250A waveform generator
- programmable CAMAC attenuator
- a PC running LabWindows
- a CAMAC fan out
- a bar code reader

The whole setup is housed in a 6U crate with a custom designed backplane. The backplane provides the power for the digital and analog part of the six calibration boards. It also controls the communication between the different calibration boards and the PC via a RS232 interface.

A. The calibration sequence

Each VFE is inserted into a calibration board using a dedicated mechanical support. An ALTERA FPGA (see fig. 4) present in each calibration board sets the pedestal values for each channel and gain to roughly 160 ADC counts.

The linearity of the MGPA is measured by injecting 21 different charges (see table 1). The charges are generated by applying different voltages onto calibrated capacitors (10.0±.01) pF. These voltages are obtained from a constant voltage source using a programmable attenuator. Plotting the known charges versus the ADC response yields a curve whose slope corresponds to the gain measured in ADC counts per pC (see fig.5). In this way the full dynamic range of the 3 gains is covered. Cross calibration of the 3 gains is achieved by taking advantage of overlapping gain curves (cf. table 1).

The input charge of 3.9 pC is the only value that can be measured in all three gains.

Charge in Gain 1	Charge in Gain 6	Charge in Gain 12
3.9	1.0	0.09
6.3	1.4	0.16
10	1.6	0.22
15.8	2.2	0.35
22.3	2.5	0.56
25.0	3.5	0.62
35.4	3.9	1.0
39.7	5.6	1.4
	6.3	2.5
		3.9

Table 1: Input charges for the three nominal gains. Values measured in more than one gain range are indicated in red.

	Gain 1	Gain 6	Gain 12
Slope (ADC counts/pC)	64.6±0.8	350.3±3.8	683.2±7.9
Offset (ADC counts)	-6.2±0.9	2.4±1.1	1.7±0.9

Table 2: Gains and offsets extracted from the calibration data of the 12625 VFE cards having passed all criteria.

B. Analysis and results

During the calibration test a program performs an on-line linearity check of each channel for all the three gains. The charge pulses are fitted and the peak position are determined (see fig.7). The three gains are obtained by plotting the extracted peak positions versus the corresponding input charges and by applying a linear least square fit to the data points (see fig.5). Slopes, offsets of the fitted lines are given in table 2. Only channels with coefficient of determination $r^2 > 0.9999$ are accepted.

A similar test is done using the internal test pulse of the MGPA. In this case 12 charges are injected instead of 21.

The accuracy of the APD leakage current measurement is tested using a current source to simulate a leakage current between 0 and 200 nA on the input of the VFE card. The data are collected by the DCU chip on the VFE and are sent to the data acquisition system via the RS232. The test board uses a digital potentiometer instead of a thermistor to test the temperature read out. The resistance of the potentiometer is varied in 15 steps from100 to 160 kΩ. All measured values are saved, and later stored in the REDACLE database [10] together with all other results.

Since the calibration set-up did not allow to measure precisely the RMS error of the pedestal,

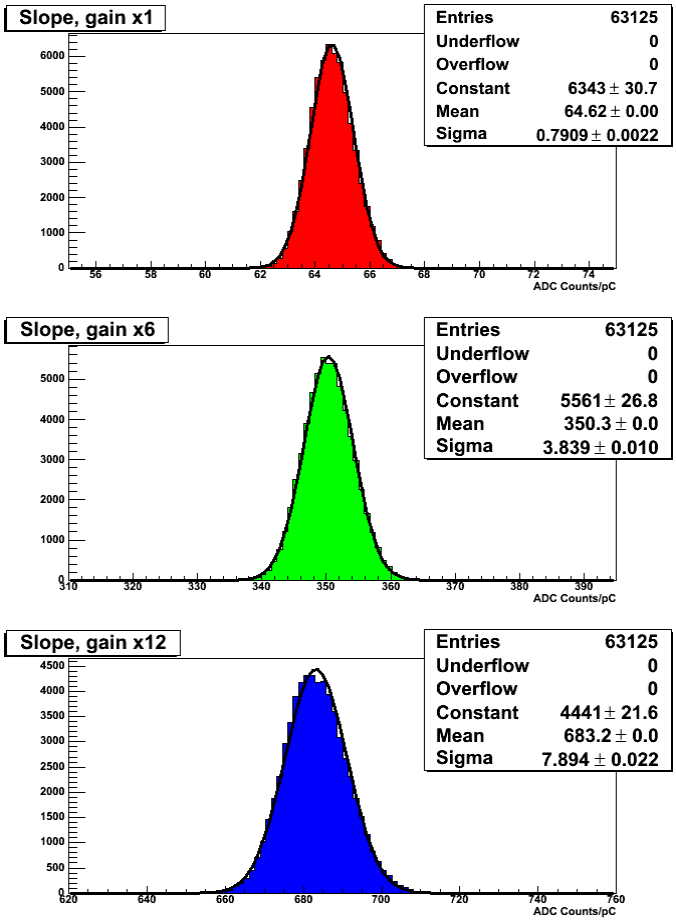

Figure 6: distribution of the slope in the gains 1, 6, 12

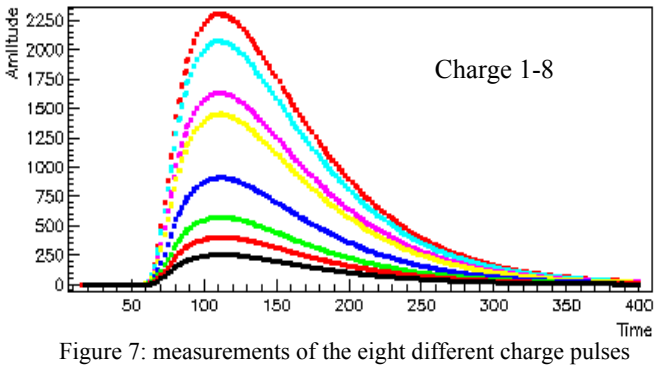

Figure 7: measurements of the eight different charge pulses injected in gain 1

the noise figure reported here stems from measurement of VFE cards already integrated in supermodules. Of the 36 supermodules 23 have been fully assembled and have shown a uniform and extremely stable noise distribution (see fig.8). The noise obtained is typically 1.1, 0.75 and 0.6 ADC counts for gain 12, 6 and 1, respectively; the relative gains (see fig.9) are 5.42 and 10.57 with RMS values of 0.047 and 0.11 compared to the design values of 6 and 12, respectively.

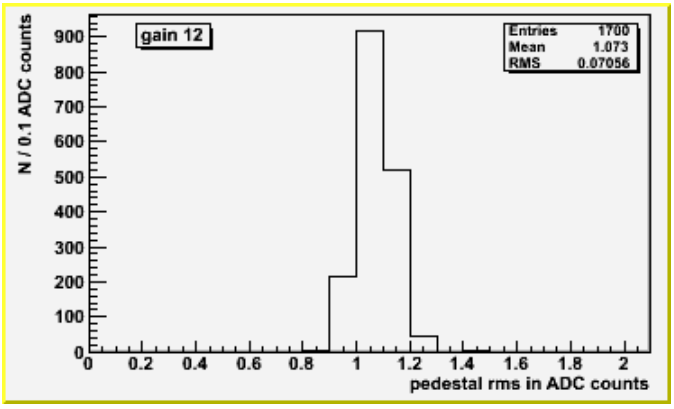

Figure 8: typical noise distribution of gain 12 in a supermodule.

V. Conclusions

The production of the VFE cards for the ECAL Barrel is finished and all cards are tested and calibrated. Roughly 66% of all supermodules of the Barrel calorimeter are fully assembled.

Given the quality achieved the tests and actions chosen were adequate and the overall test strategy was a success.

Of 12880 cards produced, 2% failed the tests: 149 were rejected during calibration and burn-in, 106 were rejected during power-on. 12625 cards passed all tests.

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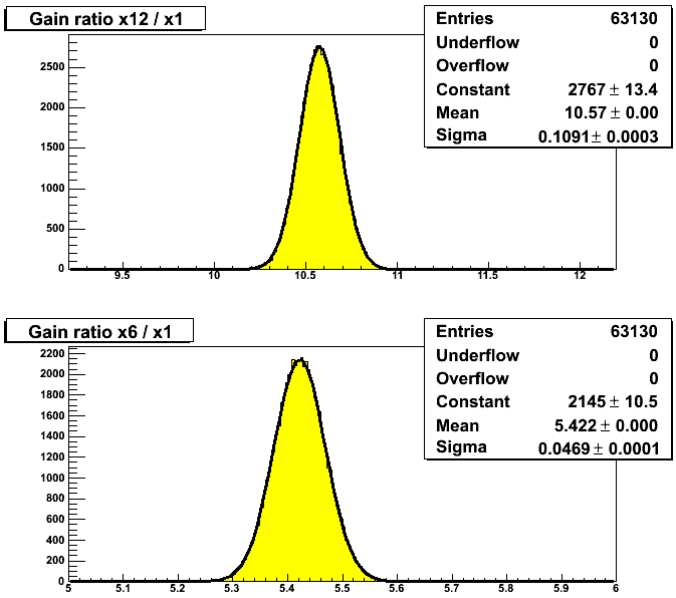

Figure 9: final distribution of the gain ratio.

FEC-CCS: A common Front-End Controller card for the CMS detector electronics.

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Abstract

The FEC-CCS is a custom made 9U VME64x card for the CMS Off-Detector electronics. The FEC-CCS card is responsible for distributing the fast timing signals and the slow control data, through optical links, to the Front-End system. Special effort has been invested in the design of the card in order to make it compatible with the operational requirements of multiple CMS detectors namely the Tracker, ECAL, Preshower, PIXELs, RPCs and TOTEM. This paper describes the design architecture of the FEC-CCS card focusing on the special design features that enable the common utilization by most of the CMS detectors. Results from the integration tests with the detector electronics sub-systems and performance measurements will be reported. The design of a custom made testbench for the production testing of the 150 cards produced will be presented and the attained yield will be reported.

I. Introduction

The CMS Tracker control system [1] which was initially developed for the needs of the CMS Tracker detector is now adopted by the majority of the CMS detectors as a front-end electronics control system. The flexibility of the design architecture, the availability of the Front-End (FE) ASIC chipset in a radiation tolerant technology as well as the availability of the optical link components were the main reasons that established this system as a "*common*" FE control system for the CMS detectors. The CMS detectors that are using this "*common*" control system are ECAL, Preshower, PIXELs, RPCs and TOTEM.

The design architecture of the control system is illustrated in Fig. 1. The system uses a ring topology configured in a local area network, allowing for a variable number of network nodes to be added in the ring depending on the FE electronics system topology of each CMS detector sub-system. This flexibility of the design architecture is further augmented by the availability of a radiation tolerant ASIC chipset (CCU, PLL, QPLL, DCU) that permits the customization of the FE control functionality depending on the requirements of each CMS detector sub-system.

The connectivity of the control system for the on-detector part is realized with copper links while for the long distance connection with the off-detector electronics controller is realized with a 4 way optical fiber link. The physical layer of the link (electrical or optical) is capable to simultaneously transport to the front-end ASICs the 40MHz LHC clock along with a set of four Trigger Commands and to establish a 40Mbps bi-directional Data Link for control information transactions. The Trigger Commands are clock synchronous and are used for signaling to the front end system the LV1A Trigger, the Resynchronization cycles, the Bunch Crossing tick marks, and the Calibration cycles.

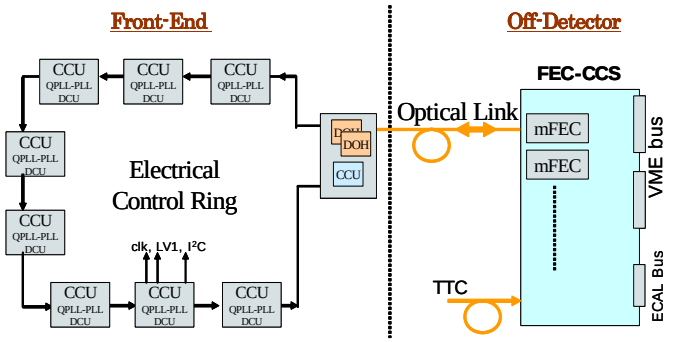

Fig. 1: Front-End electronics Control System

The Front-End Controller card (abbreviated as FEC in the Tracker subsystem) is located in the counting room and serves as the master node of the control rings. In the ECAL detector electronics subsystem this card serves a more central role acting as a local controller for the synchronization of the readout links and the triggers links and is denoted as Clock and Control System card (abbreviated as CCS). Special design considerations were taken in the design of the card in order to address the functionality requirements of both subsystems, thus leading to a "*common*" hardware design, a card named FEC-CCS.

II. FEC-CCS Architecture

The FEC-CCS card is a 9U VME64x compliant card following the design rules for custom VME hardware in CMS. The FEC-CCS card functions as a VME carrier for the mezzanine Front End Controller modules (mFECs) that host the functionality of the master controller node for the control rings. Up to 8 mFEC modules can be populated on a FEC-CCS card allowing flexibility in the configuration of the card to tailor for the different needs of the detector subsystems.

As shown in the block diagram in Fig. 2, the FEC-CCS card features a Local Bus that interconnects all the mFEC modules with an FPGA circuit (VME FPGA) that creates a bridge connection with the VME bus. This establishes a "slow

control path" that relays slow control transactions from the VME to the mFEC modules.

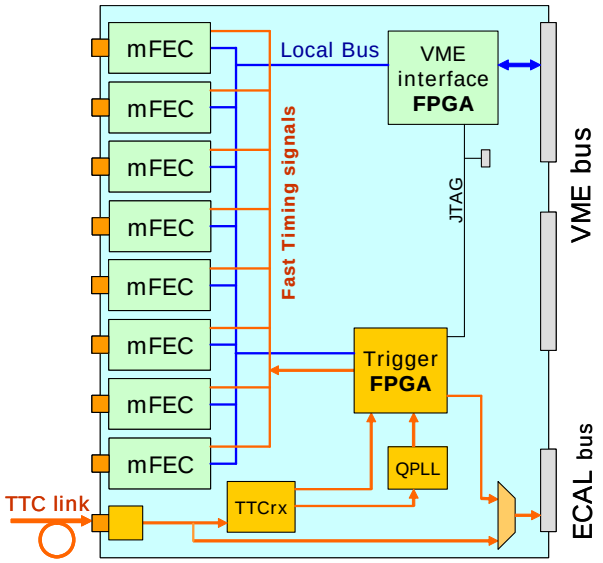

Fig. 2: Block Diagram of the FEC-CCS card.

The FEC-CCS card features also a "fast timing path" that relays fast timing information from the experiment TTC network to the mFEC modules. The fast timing signals arrive from the TTC link and are decoded by an on board TTCrx ASIC. The TTCrx provides the 40.08MHz system clock and decodes the two channels of the TTC signal: Channel A providing the LV1 accept and channel B providing fast control commands. The fast timing signals are distributed to the mFEC modules though the Trigger FPGA circuit that implements the sub-detector specific Trigger Command handling. A QPLL ASIC is inserted in the timing path between the TTCrx and the Trigger FPGA to reduce the jitter of the system clock and to operate as local clock generator in the absence of the TTC signal.

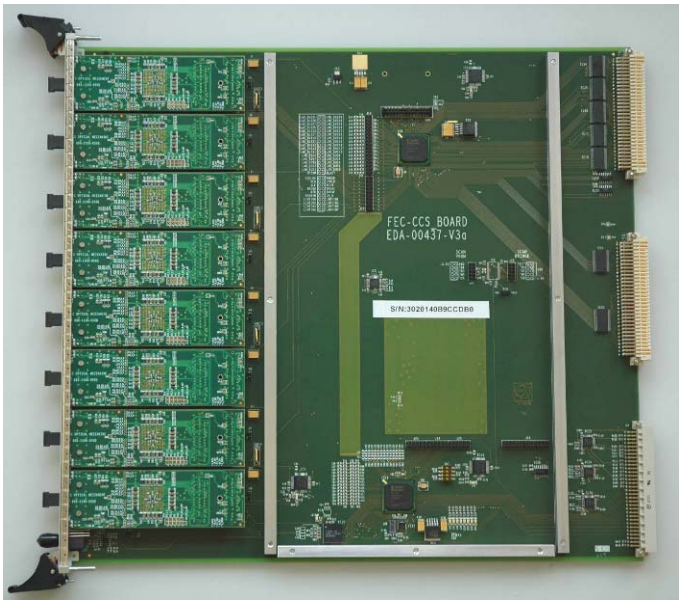

Fig. 3: Photo of the FEC-CCS card

For the ECAL, Preshower and TOTEM subsystems the FEC-CCS card delivers some extended functionalities like the fanout of the TTC signal and the merging of the TTS (Trigger Throttling Signals) signals via a special backplane connector that connects to a relatively short length "ECAL bus".

The photo in Fig. 3 shows the final production version of the FEC-CCS card. The performance of the card has been tested successfully in a VME64x crate and all the functionalities have been verified. The measured trigger latency of the FEC-CCS cards was found to be 5 BX (bunch crossings). The power dissipation of a fully configured card (8 mFECs) is ~30W drawing 7A @ 3.3V and 1A @ 5.0V.

A. The mezzanine FEC(mFEC)module

The mFEC is the Front-End Control module for the control link. It is implemented as a mezzanine module that can be plugged into different types of carrier boards. For most test applications a PCI carrier board is most suitable, for installation in the experiments the 9U VME FEC-CCS card will be used. The mFEC consists of a transmit FIFO for data to be sent out of them FEC onto the token ring and a receive FIFO for data coming back from the ring. The two FIFOs are accessible through a Local Bus interface. The mFEC is handling the insertion and circulation of the token on the ring. It generates the data packets that are encoded using the 4b5b encoding scheme. The mFEC also generates the CRC for the transmitted data and checks the CRC for the received data packets. More information about the operation of the mFEC can be found in [2].

B. The VME FPGA

The VME FPGA implements a VME64x compliant slave interface offering D32, A32, VME bus transfers. The block diagram of the VME FPGA is depicted in Fig. 4. The design makes use of the Plug & Play feature available in VME64x implementing a Configuration ROM (CR) and a Command and Status Register (CSR) containing the necessary information for automatic enumeration of the card during the VME system initialization.

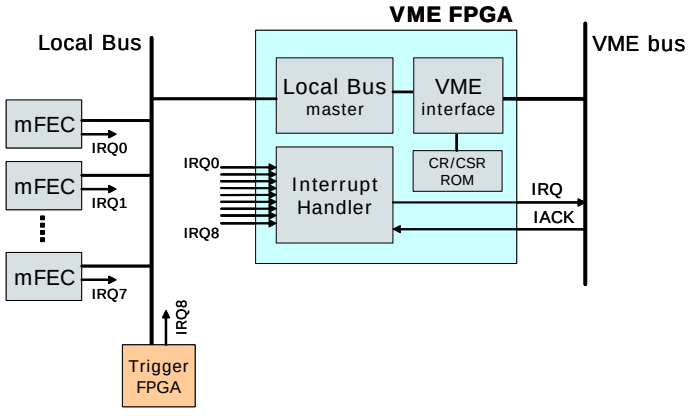

Fig. 4: Block Diagram of the VME interface FPGA.

To communicate with the 8 mFEC modules the VME FPGA implements a Local Bus master node logic. The operation standard for this bus was chosen to be compliant with the Local Bus protocol used by the PCI 9054 PCI Bus Master I/O accelerator chip from PLX technologies [3]. The VME to Local Bus bridge supports VME Block Transfers.

The VME FPGA implements a VME Interrupter logic that can be connected to anyone of the seven VME bus interrupt lines. The Interrupter logic prioritizes the interrupt signals received by the 8mFEC and the Trigger FPGA and modifies their priority order every time an interrupt request is acknowledged sending at the bottom of the priority list the most recently serviced interrupt signal. The mFEC modules generate interrupts every time a packet containing control information from the front-ends return to the mFEC receive FIFO. The user software can exploit this functionality to implement interrupt driven data transfers to/from the front-end electronics.

C. *The Trigger FPGA*

The Trigger FPGA is the central component in the fast timing path implementing all the Trigger Command encoding functions as well as all the subsystem depended custom logic. As depicted in the block diagram of Fig. 5, the Trigger FPGA implements a Control Ring Clock Encoder that encodes four "*Control Ring Trigger Commands*" on the 40MHz clock signal with a simple encoding scheme, just by selectively removing a number of pulses over three consecutive clock cycles from the clock stream. Possible transmission patterns are: 100, 101, 110 and 111.

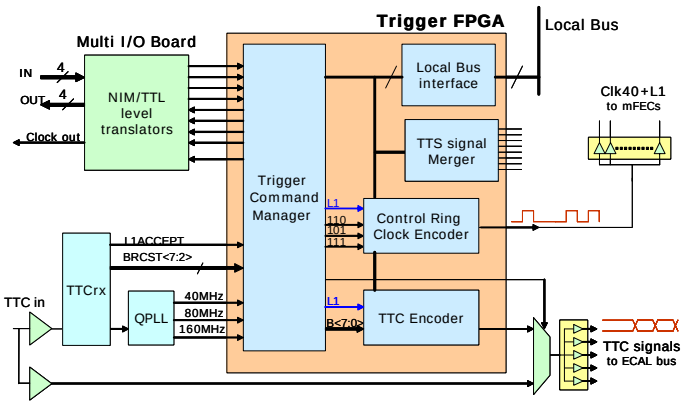

Fig. 5: Block Diagram of the Trigger FPGA.

The Trigger FPGA receives the LV1 accept signal and the B channel broadcast commands from the TTCrx ASIC and assigns them to the four Control Ring Trigger Commands. The LV1 accept signal is always assigned to the '100' Control Ring Trigger Command. The B channel TTC commands are mapped on the remaining three Control Ring Trigger Commands ('101', '110', '111'). Unfortunately these Control Ring Trigger Command assignments are not common among the CMS detector FE electronics. To accommodate for these differences a LUT with five pages, one for each subsystem, is implemented. The pages are user selectable through the Sub-System Identification (SSID) configuration register.

The Trigger FPGA has two distict modes of operation: the "*Remote*" mode which is activated when the TTC signal is detected at the optical input of the card and the "*Local*" mode which is activated on its absence. In the "Remore" mode, the received TTC signal is propagated to the ECAL bus. In the Local mode a TTC encoder circuit in the Trigger FPGA generates the required TTC signal carrying the locally generate Trigger commands as described in the following section of this paper.

To support the ECAL bus functions a Trigger Throttling System (TTS) signal merging logic, combines five TTS signal sources from adjacent VME cards using the priority encoding scheme which is defined by the CMS DAQ group. The combined TTS signal is propagated to the DAQ Fast Merging Modules (FMMs).

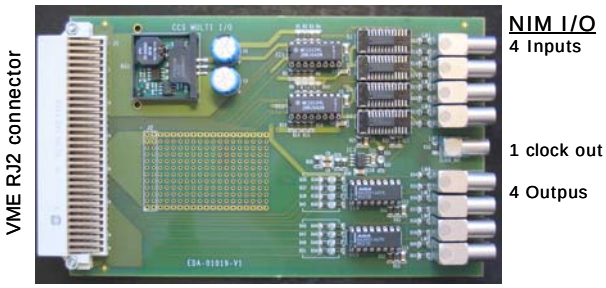

Fig. 6: Photo of the Multi I/O Card.

The Trigger FPGA has a set of four input and four output signals to interface with external equipment. This functionality proved to be extremely useful for system operation in standalone test setups where external trigger sources could connect directly to the FEC-CCS card, without the necessity of a TTC crate, and where the firing of laser pulses for calibration purposes could be command by the FEC-CCS card. Since most of the equipment use NIM signalling levels a level translator card (Multi I/O) has been built and is shown in Fig. 6. The card is 3U rear VME transition card that connects the RJ2 rear VME backplane connector.

D. *Local Trigger Command Generation*

The Local Trigger Command generation logic is based on a flexible user programmable logic that can be configured according to the functionality required by the target system setup. A set of eight identical "*Command Channels*" bearing elementary logic circuitry are the sources of the locally generated commands. As depicted in the block diagram in Fig. 7 there are four "Trigger Command Channels" that correspond to the four available Control Ring Trigger Commands ('100', '101', '110', '111') and four "Auxiliary Trigger Command Channels" that can be used to signal commands to external equipment.

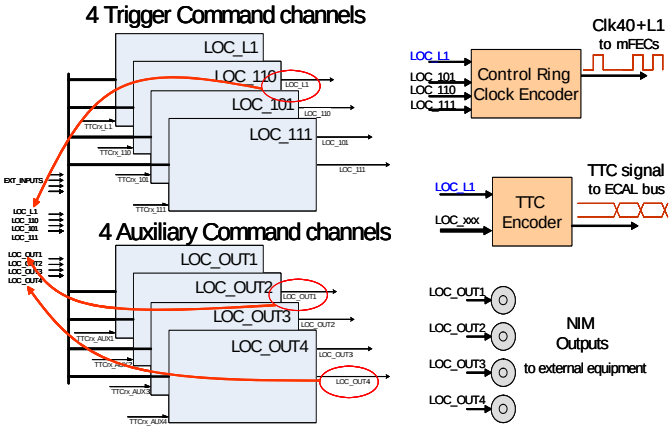

Fig. 7: The Command Channels

The trigger output signals of the command channels are retrofitted to their inputs thus allowing to trigger one another enabling the user to create sequences of multiple trigger commands. With the use of a programmable frequency generator in the Trigger FPGA circuitry, periodic sequences of commands are also possible to produce.

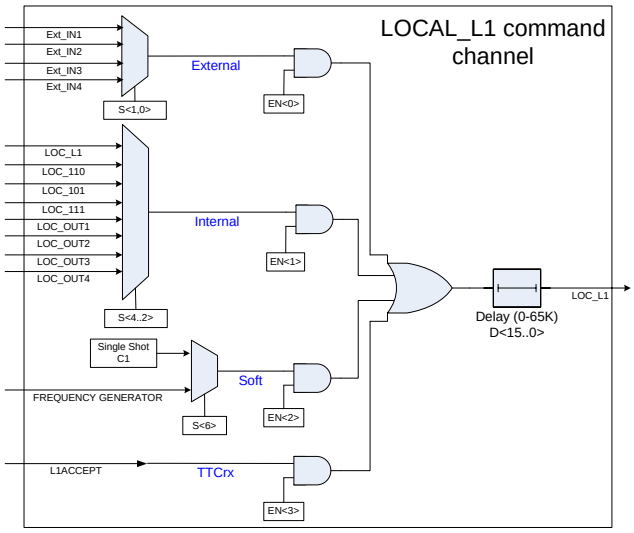

Fig. 8: Block Diagram of a Command Channel.

Each command channel has four different trigger sources that that can be individually selected or mixed. The block diagram of a command channel is depicted in Fig. 8. The trigger sources are four input signals from external equipment, internal signals from the other command channels, software controlled, single shot or periodic trigger signals or signals that can be assigned to TTCrx B channels commands. All external input signal are routed though a special circuitry that allows “debouncing” and synchronisation of the signal with the 40MHz system clock as well as the possibility for programmable prescaling of the received trigger events. A programmable delay in the command channel logic facilitates the proper timing of the locally generated trigger commands with respect to external signals or other trigger commands to match the timing requirements of the target test setup.

III. Integration with Detector Sub-Systems

A. *The CMS Tracker Case*

A schematic diagram of the CMS Tracker readout and control system [4, 5] is shown in Fig. 9. In this system there is a clear distinction and separation of the readout system and the control system. There are separate VME crates hosting the Front End Driver (FED) cards and the FEC cards. There is no direct communication between the two crates. The FED and the FEC crates receive the trigger commands via identical TTC signals from a Tracker TTC crate equipped with a set of cards that generate and fanout the TTC signal and also establish the two Trigger Throttling feedback loops. The first Trigger Throttling feedback loop is relized by the APVE (APV emulator) card while the second by the TTS signals from the FEDs and the FMM and LTC cards.

The successful operation of the FEC-CCS card in the Tracker readout and control system has been demonstrated in multiple setups, namely the Tracker electronics integration centre, the Tracker Integration Facility (TIF) and the CMS Magnet Test and Cosmic Challenge (MTCC) test setup that took place during the summer of 2006.

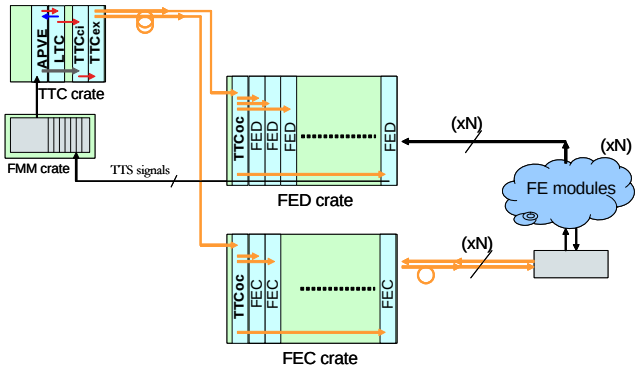

Fig. 9: The CMS Tracker Readout & Control System.

A number of FEC-CCS cards have also been distributed to external institutes to equip the facilities of the tracker integration test setups.

B. *The CMS ECAL Case*

A schematic diagram of the CMS ECAL readout and control system [6] is shown in Fig. 10. In this system the readout, the trigger and the control systems coexist in the same crate. The FEC-CCS card plays a more central role here distributing the clock and the trigger commands to the DCC (Data Concentrator Card) and the TCCs (Trigger Concentrator Cards) through the special ECAL backplane bus and merging the TTS signals generated by these modules. This set of DCC, FEC-CCS and TCC modules forms an “entity” of off-detecor electronic modules capable to readout and control one ECAL supermodule structure.

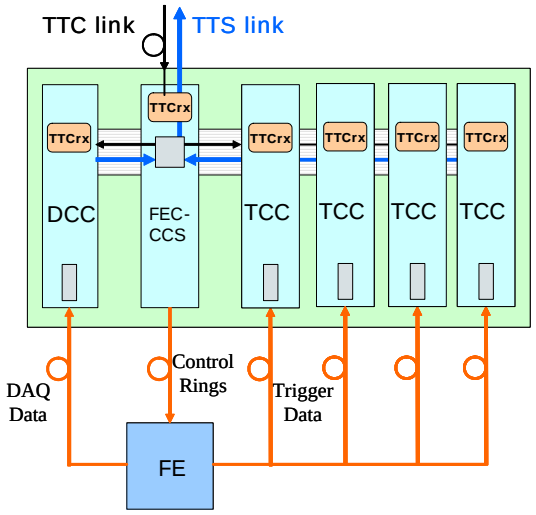

Fig. 10: The CMS ECAL Readout & Control System.

The successful operation of the FEC-CCS card in the ECAL readout and control system has been demonstrated in five different test setups. The Local Trigger generation logic proved to be very flexible and versatile, permitting to adapt to the requirements of each test setup namely the supermodule integration hall in building 867, the H4 cosmics calibration

stand, the H4 test beam stand and the H2 ECAL+HCAL test beam stand. The successful operation of the ECAL readout and control system using an external TTC signal source was demonstrated during the summer 2006 CMS MTCC run.

The Preshower [7] and the TOTEM [9] detectors will be using a variant of the ECAL backplane bus while the Pixels [8] detector will follow the Tracker detector system approach.

IV. Production & Testing

For the production testing of the 900 mFEC modules and the 150 VME FEC-CCS cards a common custom made test bench has been prepared and operated at CERN. The production testing was performed in two stages. In the first stage all the 900 mFECs were tested using one selected FEC-CCS card as carrier. In the second stage the 150 FEC-CCS cards were tested while being populated with the previously tested mFEC modules.

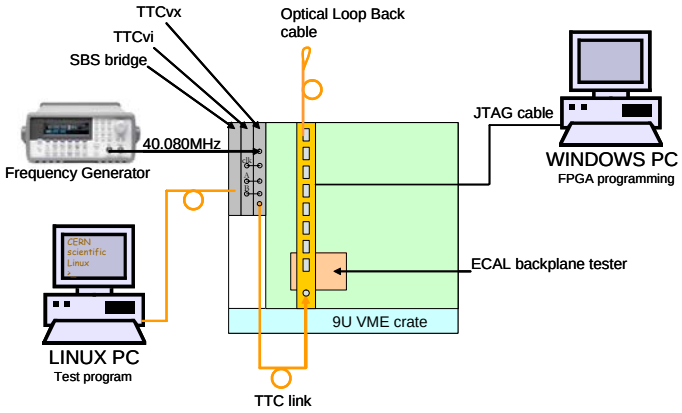

Fig. 11: The FEC-CCS Production Testing Setup.

As can be seen in Fig. 11, the production test bench is assembled around a 9U VME crate hosting a FEC-CCS card. The crate is equipped with a TTCvi and a TTCvx card to generate a TTC signal with properly encoded trigger and B channel commands. A frequency generator tuned at 40.080MHz serves as the LHC clock reference generator. A set of optical loop back cables have been specially prepared to connect at the mFEC optical ports creating virtual control rings allowing the transmission of control packets. A PC running WINDOWS OS and a firmware programming tool is used for the card firmware uploading via the JTAG bus. A second PC running LINUX OS, acts as a VME crate controller and executes the specially developed test software. The production testing procedures involve the transmission of control packets of variable length on the rings, the decoding of trigger commands, the locking of the QPLL on the LHC clock frequency and the functionalities of the ECAL backplane.

From the 900 mFECs that were tested 35 modules were found to be defected. A post production of 50 more modules was executed to compensate for the rejected modules. The production testing of the 150 FEC-CCS card is currently in progress. The cards show very high production yield. Nearly 60 prototype FEC-CCS cards have been already delivered to the CMS sub-systems to participate in various detector test benches and test beam data taking systems.

V. Conclusions

The FEC-CCS card has been developed as a common Front End Controller card for the CMS detectors. Adopting a modular hardware design, using the mFEC modules, and a flexible, user programmable timing logic we have succeeded in developing a card that merges the requirements of different CMS detectors.

The operation of the card has been successfully demonstrated in numerous system setups. The production testing is near to its completion and cards are currently being delivered to equip the CMS electronics subsystems.

Having a common hardware module minimized the development effort and the associated cost and will certainly facilitate the maintenance during the operation period of the CMS experiment. To enable the seamless utilization of the FEC-CCS modules across the different CMS subsystems a high level of programmability has been introduced in the firmware design so that not only a common hardware module but also a unique firmware version could be deployed to all the cards for all the sub-systems thus minimizing the effort for system maintenance and support for the years to come.

VI. References

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Parallel Session A3

Readout, commissioning and integration

Recent Results on the Performance of the CMS Tracker Readout System

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Abstract

The CMS Silicon Tracker comprises a complicated set of hardware and software components that have been thoroughly tested at CERN before final integration of the Tracker. A vertical slice of the full readout chain has been operated under near-final conditions. In the absence of the tracker front-end modules, simulated events have been created within the FED (Front End Driver) and used to test the readout reliability and efficiency of the final DAQ (Data Acquisition). The data are sent over the S-Link 64 bit links to the FRL(Fast Readout Link) modules at rates in excess of 200 MBytes/s per FED depending on setup and conditions. The current tracker DAQ is fully based on the CMS communication and acquisition tool XDAQ. This paper discusses setup and results of a vertical slice of the full Tracker final readout system comprising 2 full crates of FEDs, 30 in total, read out through 1 full crate of final FRL modules. This test is to complement previous tests done at Imperial College[3] taking them to the next level in order to prove that a complete crate of FRLs using the final DAQ system, including all subcomponents of the final system both software and hardware with the exception of the detector modules themselves, is capable of sustained readout at the desired rates and occupancy of the CMS Tracker. Simulated data are created with varying hit occupancy (1-10%) and Poisson distributed trigger rates (<200KHz) and the resulting behaviour of the system is recorded. Data illustrating the performance of the system and data readout are presented.

I. INTRODUCTION

The CMS Silicon Tracker will produce large amounts of data, which must be read out by the Front End Drivers (FEDs) [3][4], which are 9U 400mm VME64x cards that process the raw data from a subset of 192 APV25[2] silicon readout ASICs, equivalent to 0.2% of the tracker. After multiplexing and streaming, the data from the tracker are routed via analogue optical links to the FEDs. 96 optical channels are then digitised to 10bit precision at 40MHz and processed in large FPGAs, before being collated into events and sent to the CMS DAQ via either VME or the SLINK-64 protocol.

Under final running conditions the SLINK-64 protocol must be used to enable a data throughput of up to, and in some cases where only one FED is connected per FRL exceeding, 200 Mbytes/s per FED. It is clear therefore that such a system must be well tested before final assembly at Point 5 on the LHC ring thus ensuring that the final operation of the system is certified. However, during the testing and assembly stages in 2006 there are not enough Tracker front-end modules available in order to drive a large enough number of FEDS to make a true vertical slice test. Nominally a vertical slice would consist of 1 whole crate of FRLs, which corresponds to two whole crates of FEDs ~ 30 in total. Therefore another method of testing the readout system without the need for the detector modules is required. This is achieved by creating Pseudo-Random fake events within the front-end FPGAs of the FED, which are injected directly into the FED exactly where the optical data samples would arrive from the final system.

In order to qualify the hardware readout system and operation of the DAQ, the system was set up in building 904 on the CERN Prevessin site in France. The system is capable of creating variable event occupancies in the front end of the FED without the need for the actual detector modules to create the event frames from the APV25 front-end readout chips. The “fake events” which are created in the FED have the capability to be set to operate at any occupancy between 0 and 100% and also include a pseudo random adjustment to the pedestals of the fake APV frames, in order to simulate the random nature of the hits in the front-end silicon detector modules.

The main purpose of this test is to qualify the functionality of the entire trigger and readout chain from the LTC, TTCci, TTCex, TTCoc, APVE, FMM, FRL, FED, Transition Card, Slink Sender Card and DAQ software. Operating the system under various conditions by varying the strip hit occupancy and therefore data throughput. In doing so one can investigate the limiting factors of the system to gain a better understanding of how the final tracker will perform.

II. TRACKER FED FAKE EVENTS

By exploiting some of the remaining block memory within the delay FPGAs on the front end of the FED, it has been possible to set aside enough space to program individually each optical channel with a unique multiplexed APV25 frame. The fake events that are produced within the FED are exact replicas of the data frames that would normally arrive over the optical analogue links. The frames are programmed into a block RAM within the delay FPGAs

using the same method over VME as is utilized to program all other configurable registers within the FED.

In order to accurately simulate more realistic final conditions, a pseudo random number generator has been implemented to augment the values set within the stored data frame. The magnitude of this random augmentation of frame samples is programmatically adjustable to have a range of between 0-1 up to 0-256 ADC counts. This factor can also be applied on a channel-by-channel basis. The value produced by the random number generator is then summed with the value stored in the block ram for the sample being input into the front end FPGA on that clock cycle. Between each sample the random number generator is cycled and a new number produced to be summed with the next sample in the APV data frame and so on, thus a sample by sample noise is introduced over the whole APV frame.

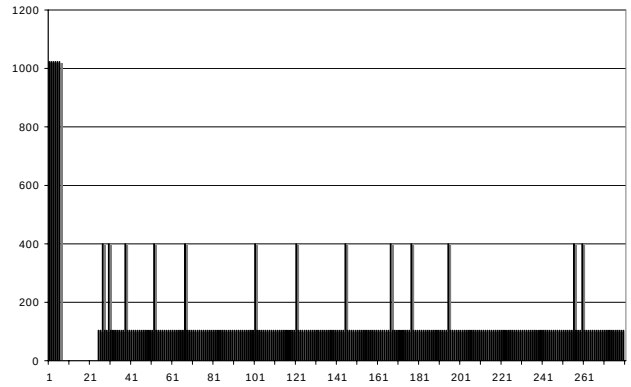

Figure 1: APV Fake Data Frame With 5% Occupancy

In this test the range of the noise was set to between 0 and 25 ADC counts. The strip hit values were set to 400 ADC counts. The hit threshold was set to 25 ADC counts. In order to fully test the functionality of the FED all frames were created with a base offset pedestal of 104. The same value was then set as the pedestal for subtraction in the FED and the FEDs were run in Zero Suppression mode. Figure 1 shows an example APV fake data frame with a strip-hit occupancy of 5% corresponding to 13 hits out of the 256 strips. It just so happens that an occupancy of 5% corresponds to a condition in the system where there is a fine balance between the buffer occupancy within the APV25 front end chips and that of the FEDs. At this occupancy with the trigger set to 100kHz one clearly sees backpressure being exerted by both buffers. This is merely a point of interest and not one for further discussion.

III. TEST SETUP

The test setup comprises a complete vertical slice of the full final CMS Tracker trigger and DAQ system excluding the detector silicon strip modules, analogue optical link and the back end readout link of the FRL for the final DAQ. For the purpose of this test the data were read out over the SLink, the CRC value was calculated for each event and each FED, checked with the CRC stored within the data and the result was logged. Data were assumed to be ok given the corroboration of CRC checksums. Note that it is possible that limitations on the speed of this final section of the DAQ could reduce the achievable rates measured in this test.

Figure 2 is a schematic representation of the final test setup. For more detail on this system see reference [5]. The basic configuration of the system and interconnections can be seen in simplified form. Three VME crates are used in this system all of which are controlled by rack mounted PCs, running the Linux operating system, via the CAEN PCI to VME bus controller[7]. The software installed on all machines contains the full installation of XDAQ[1] and the Tracker specific software packages [6][8] for online Tracker commissioning and data analysis tasks. The DAQ PC controls a compact PCI crate and runs the specialised software developed to control and readout the FRLs[10]. The trigger is controlled by the final CMS system comprising LTC, TTCci, TTCex, TTCco and the Tracker Specific APVE.

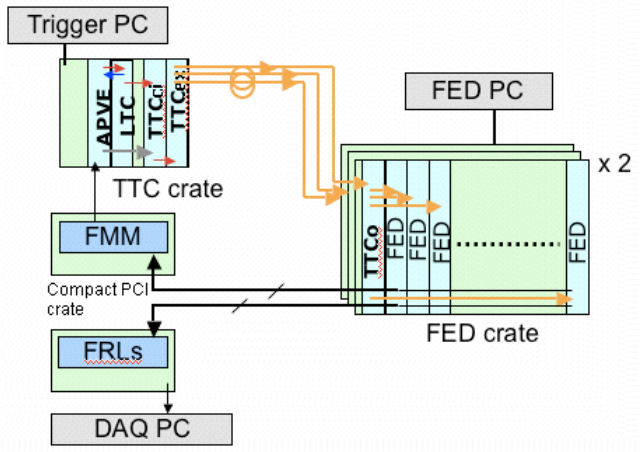

Figure 2: Test Setup

Back-pressure for this system is achieved using the final FFM feedback loop that is in place to prevent overflowing of buffers on the FED and also to communicate run time statuses of the FEDs in the system. The statuses can be logged by the FMM modules thus it is possible to record the history of state changes on the individual FMM channels. The complete set of statuses from all the FEDs are then combined in a logical OR to produce a single signal that is fed into the APVE module where this status is then combined in a further logical OR with the status of the APV emulator. The result of these merged signals is a global signal that is then fed to the LTC trigger card where upon receipt of a status other than READY, either WARN or BUSY, the trigger controller will then interrupt the flow of triggers in order to reduce the occupancy of buffers in the system to a safe level at which point the FEDs and/or APV emulator will then de-assert BUSY or WARN thus allowing triggers to resume.

All of the 30 FEDs are configured and controlled by the CMS Tracker DAQ online software with the use of the

Fed9USoftware[9] package developed by Imperial College London. Each FED is programmed with the same fake event of a specific representative detector occupancy and on receipt of a trigger the FEDs process the fake APV frame and output the Zero Suppressed data buffer containing the hit information for the APV frame.

IV. RESULTS

Results were taken over a full week of running and in total more than 30 billion events were read out from 30 FEDs. The system was run with pseudo random Poisson generated triggers with a mean rate of 140kHz. Note that this frequency drops when the backpressure system must assert BUSY and thus veto the trigger. Figure 3 shows an example distribution of triggers produced by the Poisson generator of the LTC when running with mean rate of 140 kHz. These data were taken directly from the trigger analyzer on the APVE card during one run with hit occupancy of 1%, thus resulting in no rate reduction due to backpressure.

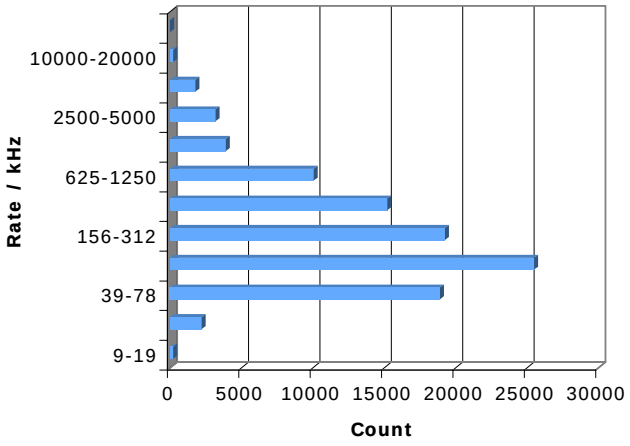

Figure 3: Trigger distribution for 140kHz mean rate

In an attempt to demonstrate what the results represent when considering the final CMS Tracker readout expectations the data are displayed in terms of percentage data loss calculated from the ratio of measured trigger rate to 100kHz, the published desired mean trigger rate of CMS. No data is actually lost, data from all triggers were received and no corruption or loss data was seen.

The FEDs were setup to run in Zero Suppression mode with pedestal subtraction and common mode subtraction all activated. The pedestals were set to 104 ADC counts as described in section III. Two sets of data were taken for two different modes of operation of the FED. Figure 4 shows the percentage data loss for full debug header mode, which is a verbose mode of operation giving more information about the status of each event.

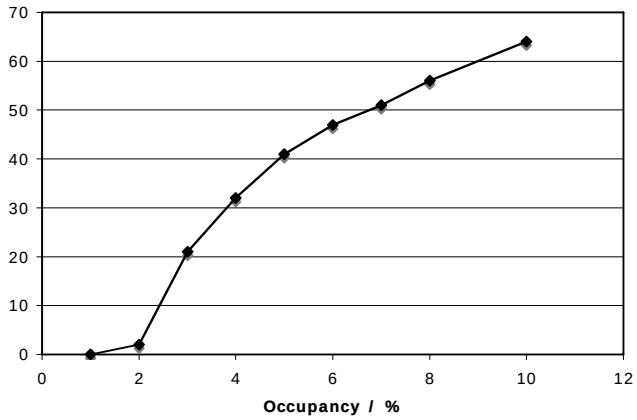

Figure 4: % Data Loss for Full Debug Data Frame at 100kHz

This plot shows that for low occupancy of 1-2% the system ran with practically no reduction in trigger rate. It is important to note that a large majority of the CMS Tracker will run under such conditions in the LHC. As we reach the limit of buffer occupancy in the FED and APV at 3% occupancy we find that the data loss has a sharp increase up to 20%. At a higher occupancy of 10% there was a 64% reduction in trigger rate therefore it is clear that this system is extremely sensitive to the hit occupancy within the silicon strips.

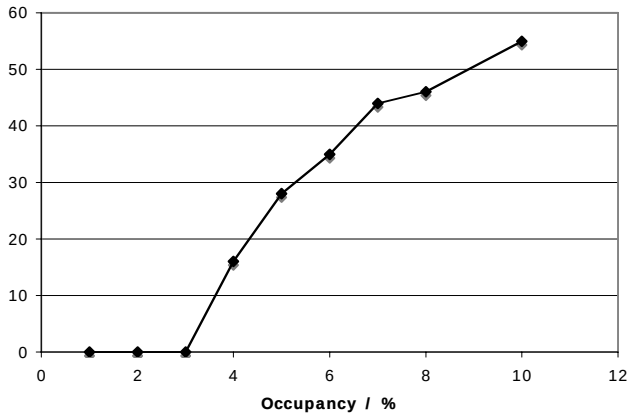

Figure 5: % Data Loss for Compressed Data Frame at 100kHz

For those innermost areas of the Tracker where the occupancy is expected to be the highest it is still encouraging to look at the results from Figure 5 where the data format is now set to compressed mode. With the reduction in header information and overall data packet size for this mode, one is able to readout data with hit occupancy of 3% with no reduction in trigger rate. Again there is a sharp rise in the data loss at 4% occupancy up to 17%. It is clear that this reduced data packet size will be essential when reading out the innermost layers of the Tracker in order to keep the sustainable trigger rates as high as possible.

V. CONCLUSIONS

The results of this test have shown that the system is stable for periods of time over many hours when running at 150KHz Poisson distributed triggers, the back pressure from the APVE and FED, via the FMM, works perfectly to throttle the trigger rate down to a sustained rate of 72Khz when operating the FED at 5% occupancy. At lower occupancies, 1-3%, more representative of nominal data taking conditions in the final Tracker, the system runs without interruption at trigger rates around 100 KHz sustained. Note that these measurements were conducted without final shipping of the data for processing and analysis, it is likely that some delay may be introduced into the readout of the data from FRLs due to slower final shipment of the data. However, this is Software and PC processor power dependent and therefore not without the possibility for future improvements. The results in this paper are the best possible achievable readout rates without further reduction due to data processing.

VI. REFERENCES

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Readout Electronics Tests and Integration of the ATLAS Semiconductor Tracker

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Abstract

The SemiConductor Tracker (SCT) together with the Pixel detector and the Transition Radiation Tracker (TRT) form the central tracking system of the ATLAS experiment at the LHC. It consists of single-sided microstrip silicon sensors, which are read out via binary ASICs based on the DMILL technology, and the data are transmitted via radiation-hard optical fibres. After an overview of the SCT detector layout and readout system, the final-stage assembly of large-scale structures and the integration with the TRT is presented. The focus is on the electrical performance of the overall SCT detector system through the different integration stages, including the detector control and data acquisition system.

I. Introduction

The ATLAS detector [1], one of the two general-purpose experiments of the Large Hadron Collider (LHC), has entered into the final stages of installation at CERN. The LHC, a proton-proton collider with a 14-TeV centre-of-mass energy and a design luminosity of 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$, is expected to deliver the first proton beam by the end of 2007. The ATLAS central tracker (Inner Detector, ID) [2] combines the silicon detector technology (pixels and micro-strips) in the innermost part with a straw drift detector with transition radiation detection capabilities (Transition Radiation Tracker, TRT) in the outside, operating in a 2-T superconducting solenoid.

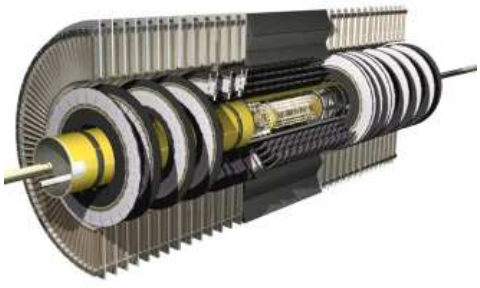

Figure 1: Layout of the ATLAS Inner Detector: it comprises the Transition Radiation Detector, the Semiconductor Tracker and the Pixel system from the outer to the inner radii, respectively.

The microstrip detector (Semiconductor Tracker, SCT), as shown in Fig. 1, forms the middle layer of the ID between the Pixel detector and the TRT. The SCT system [2, 3] comprises a barrel made of four nested cylinders and two end-caps of nine disks each. The barrel layers carry 2112 detector units *(modules)* altogether, while a total of 1976 end-cap modules are mounted on the disks. The whole SCT occupies a cylinder of 5.6 m in length and 56 cm in radius with the innermost layer at a radius of 27 cm.

The silicon modules [4, 5] consist of one or two pairs of single-sided p-*in*-n microstrip sensors glued back-to-back at a 40-mrad stereo angle to provide two-dimensional track reconstruction. The 285-$\mu\mathrm{m}$ thick sensors [6] have 768 AC-coupled strips with an 80 $\mu\mathrm{m}$ pitch for the barrel and a $57-94$ $\mu\mathrm{m}$ pitch for the end-cap modules. Between the sensor pairs there is a highly thermally conductive baseboard. Barrel modules follow one common design, while for the forward ones four different types exist according to their position in the detector.

II. The SCT readout system

The readout of the module is based on 12 ABCD3TA ASICs manufactured in the radiation-hard DMILL process mounted on a copper/kapton hybrid [7]. The ABCD3TA chip [8] features a 128-channel analog front end consisting of amplifiers and comparators and a digital readout circuit operating at a frequency of 40.08 MHz. This ASIC utilises the binary scheme where the signals from the silicon detector are amplified, compared to a threshold and only the result of the comparison enters the input register and a 132-cell deep pipeline, awaiting a level-1 trigger accept signal. It implements a redundancy mechanism that redirects the output and the control signals, so that a failing chip can be bypassed. To reduce the channel-to-channel threshold variation, in particular after irradiation, the ABCD3TA features an individual threshold correction in each channel with a 4-bit digital-to-analog converter *(TrimDAC)* with four selectable ranges. In addition, a calibration circuitry is implemented in the chip providing an injection charge in the range $0.5 - 10$ fC. By injecting various known charges and performing threshold scans, the analogue properties of each channel can be determined, such as the gain, the offset and the noise.

The clock and command signals as well as the data are transmitted from and to the off-detector electronics through optical links [9]. On the detector side, the DORIC[1] and VDC[2] are utilised for receiving the optical clock and control signal (one link) and for data transmission (two links), respectively. Therefore, three optical fibres are connected to each module, terminated by an opto-package consisting of Si *p-i-n* diodes and VCSELs mounted on the Back-Of-Crate (BOC) card. The latter serves as an interface between the optical signals and the off-detector electronics in the Read-Out Driver (ROD). Each ROD

[1] Digital Optical Receiver Integrated Circuit.
[2] VCSEL (Vertical Cavity Surface Emitting Laser) Driver Chip.

controls and monitors 48 SCT modules.

The LHC operating conditions demand challenging electrical performance specifications for the SCT modules and the limitations mainly concern acceptable noise occupancy level, tracking efficiency, timing and power consumption. These requirements reflect on the design of the readout system, as well as on the quality assurance/control strategy followed throughout the detector construction. To this respect, a series of electrical tests were performed during the various stages of the detector assembly; from module production [10], to macro-assembly [11], at reception at CERN [12], and eventually after the final integration with TRT. These repetitive tests are necessary to ensure that the module/system performance does not change after each stage, to finalise the corresponding data acquisition software, and to learn how to recover potential errors/problems. The final stages of the SCT assembly and testing at CERN were carried out in the ATLAS SR1 clean-room, equipped with a system capable of characterising up to one million readout channels simultaneously. Electronics tests results such as electrical connections checks, noise and gain measurements, as well as temperature and leakage current measurements were given particular attention. The outcome of these electronics tests, essential also for the validation of the grounding, shielding and cooling system, are discussed in the following sections.

III. SCT ASSEMBLY AND INTEGRATION

After the module production, being distributed over several sites in Australia, Europe, Japan and the USA, the macro-assembly[3] took place in three laboratories, in the UK and the Netherlands. The four barrel layers were assembled at the University of Oxford employing two specially designed robots for the mounting of modules onto cylindrical support structures. A detail of a barrel layer showing the overlapping modules is given in Fig. 2 (left). The on-detector services, being fitted during macro-assembly, include thin-wall Cu-Ni pipes and module cooling blocks, which remove heat through an evaporative C_3F_8 cooling system. The modules are individually supplied with LV and HV power through Al- or Cu-*on*-Kapton low mass tapes.

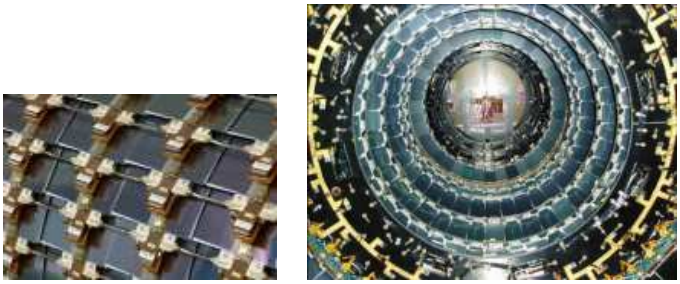

Figure 2: Left: detail from a barrel outer surface; silicon sensors and hybrids are visible. Right: beam's eye view of end-cap C.

The electrical performance of whole barrels was duly tested in Oxford for barrels 3, 4 and 6[4] and at CERN for barrels 3 and 5. All digital and analog functions were examined by following standard measuring procedures [10]. The tests showed stable operation for a simultaneous readout of up to one million channels in terms of thermal operation, data acquisition and detector control. More than 99.7% of all barrel channels are fully operational as evident from Table 1, where detailed information for dead and noisy channels for each barrel is given. These figures are in agreement with the ones obtained during module production. The average module noise was stable at 4.5×10^{-5}, well below the design specification of 5×10^{-4}. Concerning the detector bias, the leakage current drawn by the sensors at $\sim 15^{\circ}$C was much lower than 1 μA at the nominal bias value of 150 V, *i.e.* within the specifications.

Table 1: Channel defects breakdown for the barrel SCT as measured after macro-assembly, in Oxford and at CERN.

Barrel	Total nr. channels	Dead	Noisy	Other	Total defects
B3	589 824	357	460	666	1483 (0.25%)
B4	737 280	245	242	354	841 (0.11%)
B5	884 736	770	492	556	1818 (0.21%)
B6	1 032 192	2513	1936	1271	5720 (0.55%)
Total	3 244 032	3885	3130	2847	9862 (0.30%)

After completing the individual testing of the barrels at CERN SR1 room, the four layers were eventually integrated into one barrel. This operation, completed within a period of three months, was carried out step-by-step with one layer being inserted into the structure each time from the largest down to the smallest one. During this operation, the SCT services of the *inner* layer were transferred onto a horizontal service support structure, whereas the ones of the *outer* layer were unfolded radially at the ends.

The two end-caps, on the other hand, were brought together at the University of Liverpool (End-Cap C, *EC-C*) and at NIKHEF (End-Cap A, *EC-A*). The modules were manually mounted onto disks, fully characterised in a test-box and finally the disks were installed inside carbon fibre cylinders. A photograph of the fully assembled EC-C as seen from inside is shown in Fig. 2 (right); all disks are clearly visible. Both end-caps have been transferred to CERN —first EC-C and then EC-A— and they have passed successfully the reception tests, which include visual inspection, disk alignment measurements, examination of the cooling circuits and comprehensive electronics tests. The EC-A was tested while cooled down to the nominal temperature of -7°C in contrast to EC-C which was tested warm. The measured ENC[5] noise for each module of EC-A is shown in Fig. 3. These values are comparable to the ones measured during module assembly [10] and after macro-assembly at NIKHEF. The fraction of dead channels was also found to be at the same level as previously measured and around 0.2%.

Many of the activities performed on the SCT large structures was devoted to connection and manipulation of services, *i.e.* the connection of the evaporative cooling plants, the final power supplies and readout electronics. A prototype of the final Data Acquisition (DAQ) system, consisted of RODs and BOCs, and

[3]Mounting of modules onto disks (end-cap) or cylinders (barrel) and installation of the respective services.

[4]The four SCT barrels are numbered from 3 to 6 starting from the innermost one, *i.e.* B3–B6, whereas B0–B2 denote the pixel layers.

[5]Equivalent Noise Charge defined as the input charge giving signal equal to effective output noise (expressed in electrons).

the Detector Control System (DCS) was engaged. The DCS provides high and low voltage for the sensors and ABCD3TA chips, voltage for the DORIC and VDC ASICs and monitors the temperature on the modules. Besides monitoring and controlling various parameters of these power supplies, the DCS includes a hard-wired interlock system which automatically switches off the power supply to certain groups of modules in the event of an over-temperature. In addition, the DCS monitors humidity and temperature sensors mounted on the outlets of each cooling loop and records the corresponding data.

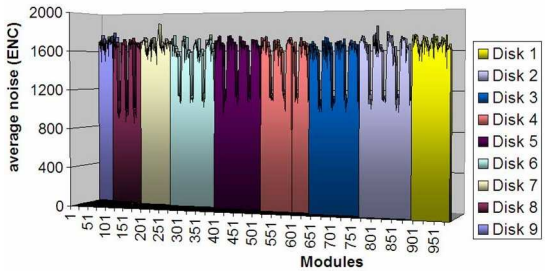

Figure 3: ENC noise per module for all disks of end-cap A as measured at CERN. The modulation observed in the plot is due to the different noise levels of the four types of end-cap modules [5]; $\sim 1450 - 1550\ \mathrm{e}^-$ for the outer and long middle modules and $\sim 900 - 1100\ \mathrm{e}^-$ for the inner and short middle ones.

Each of the three SCT blocks, the barrel and the end-caps, are enfolded in cylindrical structures, the Outer and the Inner Thermal Enclosures (OTE and ITE, respectively). These foam-based layers, covered by aluminised Kapton (OTE) or carbon-fibre-reinforced-plastic (ITE), provide gas tightness,[6] thermal isolation and Faraday shielding. The gas envelopes are complemented by flat panels fitted on the ends. A quite large fraction of testing time was given to gas tightness measurements, identification and sealing of leaks. After several iterations, the leak rate was reduced to an acceptable level for the barrel and EC-C (EC-A OTE has not been fitted yet).

IV. Barrel SCT-TRT integration

The integration and commissioning of the barrel SCT with the respective TRT [14] is almost complete. It started in February 2006 with the insertion of one detector into the other, shown in Fig. 4, using a rail system and a cantilever stand. During this operation, the SCT services were transferred onto the Insertion Service Support Structure (ISSS), fixed onto the SCT cradle extensions. The TRT, installed in the inner detector trolley, was finally slid over the SCT.

A series of combined tests followed the integration of the barrel ID, covering a wide spectrum of operational and detector performance related aspects [15]. During these tests in SR1, one eighth of the TRT and one quarter of the SCT were equipped with the complete readout chain, in a top-bottom layout as shown in the left-hand side of Fig. 5. As far as the SCT is concerned, 468 out of the 2112 modules were read out using 12 RODs and one TIM.[7] In the TRT, on the other hand, about 10 000 channels were examined with nine RODs and three TTCs. Three scintillator counters were also installed (see Fig. 5, left) to provide an external trigger from cosmic rays to both detector systems. A typical cosmic-ray track is shown on the right-hand side of Fig. 5 as reconstructed by a combined SCT & TRT tracking algorithm. The measurement results that follow were obtained with this *cosmic* setup.



Figure 4: Insertion of barrel SCT into barrel TRT; the OTE is visible surrounding the barrel SCT, as well as the services on the ISSS (foreground).

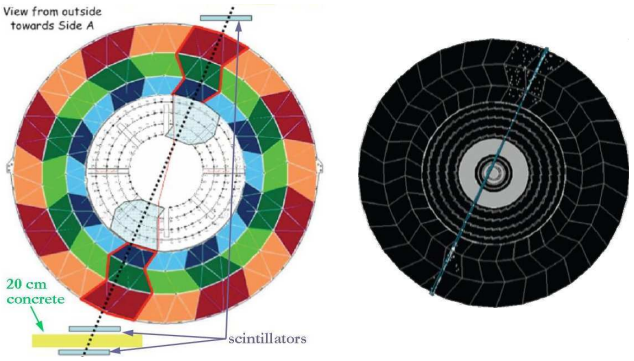

Figure 5: Left: Transverse schematic view of the setup for the cosmic run. The actually read out parts are highlighted (half of the bottom TRT section was not read out). Three scintillator counters were used for trigger. Right: reconstructed cosmic track in the SCT and the TRT.

A typical electrical testing sequence begins by establishing communication between the modules and the off-detector electronics system and by optimising the optical links settings. After the digital tests, *i.e.* checking the redundancy links, the chip by-pass functionality and the pipeline circuit, the analogue measurements follow. These include measurements of the gain, the offset and the noise for each channel and evaluation of the module noise occupancy. The noise is measured by performing a threshold scan in the absence of charge injection. The slope of the logarithm of the occupancy versus the square of the threshold is approximately proportional to the ENC noise. Furthermore, the noise occupancy at the 1-fC threshold level is obtained, with the exact 1-fC point for each channel already been defined by the trimming. Several distinct configurations were tried in order to assess the potential dependence of the noise on those.

The noise stability was monitored throughout the measurements and only a slight increase was observed for single barrels in comparison with the macro-assembly values, as well as between the whole barrel and the individual barrel layers. No pick-up noise was detected in the presence of external heaters

[6] The SCT will be operated in a N_2 environment at $-7°$C, whereas the TRT will be embedded in CO_2 at a temperature of $\sim 20°$C.
[7] TTC (Timing, Trigger & Control) Interface Module.

on the SCT thermal enclosure. After applying temperature corrections, the ENC noise was found to be $\sim 40 - 50$ e$^-$ higher for the barrel than after macro-assembly.

For the noise occupancy measurements, the TrimDAC thresholds for each channel were initially set to the value obtained during module production, leading however to a wide threshold variation. To remedy this problem the so-called *new Response Curve (RC)* configuration was introduced, which included a $\sim 10\%$ wafer-by-wafer correction to account for variations in the ABCD3TA calibration capacitor. The latter configuration is compared with the *old trim target* uncorrected one in Fig. 6 with respect to the measured noise occupancy. With the new configuration, the noise occupancy values are clearly less scattered, returning an r.m.s. value of 3.7×10^{-5}, whereas the old one gives an r.m.s. of 5.5×10^{-5}. The observed decrease in the mean value with the RC threshold, on the other hand, is due to the long period of detector bias preceding these measurements, rather than the threshold configuration. This behaviour had previously been observed in single barrel tests and is evident in calibration as well as physics-mode runs. The RC configuration was used throughout the cosmic run.

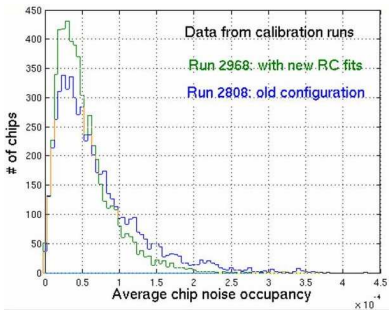

Figure 6: Average noise occupancy for each chip for the cosmic test setup and for two different threshold configurations: the'old trim target' (blue), rendering a mean (r.m.s.) value of 6.8×10^{-5} (5.5×10^{-5}), and the 'new RC' (green), returning 5.1×10^{-5} (3.7×10^{-5}), respectively. The measurements with RC configuration were taken after a few days with detector bias.

The effect of high trigger frequency was studied by varying the pulser rate in physics mode. For a trigger rate ranging from 5 Hz up to 50 kHz, no evidence of increase in noise occupancy was found.

The grounding scheme may be a potential factor contributing to noise level. Therefore the effect of a change in the grounding was studied, by measuring the noise occupancy with the power supply DC shorting cards *in* and *out* when noth SCT and TRT are triggered from a pulser at 50 Hz. No significant change in the noise occupancy was observed, however the grounding scheme in SR1 is not the final one, which will not be available before the detector is installed in its final position.

Noise can be evaluated by two methods: online with calibration scans and triggers provided by the ROD and TIM and offline with physics mode runs triggered by a pulser by applying the offline analysis. With either approach practically the same results were obtained in terms of noise occupancy.

In Fig. 7, a comparison between the ENC noise recorded when the SCT only is read out (left panel) and when the TRT is also operated simultaneously (right panel). The ENC noise in both cases remains the same and equal to ~ 1750 e$^-$, thus no electrical pick-up noise is induced between the two detectors. A similar result is acquired when a different data compression logic[8] than the previously applied *test mode* (XXX, excluding 000) is selected; for the *level mode* (X1X), the ENC noise is 1611 electrons for the SCT only and 1610 electrons for SCT & TRT together. Similar conclusions are drawn for the TRT in the absence/presence of the SCT readout.

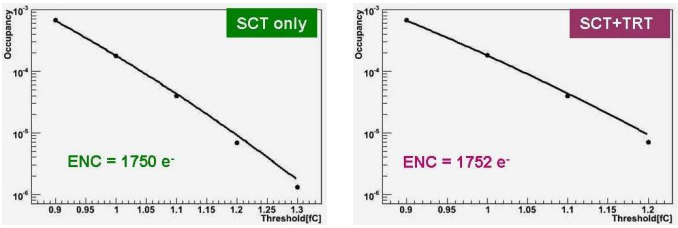

Figure 7: Noise occupancy as a function of the threshold for SCT only (left panel) and for SCT and TRT simultaneous readout (right panel) when the *test mode* (XXX, excluding 000) is selected for the data compression. The points represent measurements taken with threshold scans and the curves are analytically (through a complementary error function) derived from the ENC value indicated.

As far as common-mode noise is concerned, no evidence of such was found. There was no increase in noise occupancy observed when using synchronous triggers. No correlations have been observed neither between noise hits within chips, nor between hits on different modules.

The ID barrel was transported from SR1 building and installed in the ATLAS detector in August 2006. After being lowered into the ATLAS cavern with only a few millimeters of clearance, the detector was successfully inserted in the liquid argon calorimeter cryostat (see Fig. 8). The final stage of the barrel ID commissioning is under way, involving the connection of cables and services, the verification of full connectivity to the power supplies, readout and DAQ systems, and the on-detector functionality checks of all detector modules for SCT and TRT. This intervention will be carried out by implementing the final grounding and shielding scheme for all ~ 2000 SCT modules and the complete TRT. It should validate the detector for autonomous operation for ten years without further access.



Figure 8: The barrel ID installed in its final position inside the electromagnetic calorimeter cryostat bore.

[8] In view of the foreseen 1% strip occupancy on any event, data compression is employed, in order to reduce the number of bits of data read out of the chip for each event. This logic examines the three bits of data, representing three beam crossings centred on the level-1 trigger time, making up the hit pattern for each channel. The state 'X' denotes any bit value; 0 or 1.

V. End-cap SCT-TRT integration

The integration of the forward parts of the ID started in September 2006 with the insertion of the SCT EC-C into the TRT EC-C, shown in Fig. 9. Before this operation, the functionality of an octant of the EC-C was successfully tested inside the thermal enclosures. The readout and power cables are currently being connected in preparation for the two-month long combined tests in the SR1 clean-room. During those, one quadrant of the SCT, *i.e.* 247 modules, will be read out together with an adjacent sector of the TRT corresponding to 1/16 of the total end-cap (7680 straws/channels).



Figure 9: Insertion of the SCT EC-C into the TRT EC-C.

The ID EC-A, on the other hand, is going to follow more or less the same integration and installation steps as EC-C. However, this process is expected to proceed faster taking advantage of the experience gained during the EC-C integration. The ID EC-A is expected to be integrated by November. Both end-caps are scheduled to be ready for installation in the ATLAS cavern by January – February 2007.

VI. Conclusions

ATLAS SCT is progressing well towards integration with the other parts of the ID, installation in ATLAS and commissioning. Repeated tests in various stages have demonstrated operational stability and good electrical performance. The fraction of dead channels has been kept below 0.2%. Particular attention was given to the electronics tests such as electrical connections checks, noise and gain measurements, as well as temperature and leakage current measurements. The outcome of these tests validated the grounding, shielding and cooling system. As far as noise is concerned, no remarkable change with respect to measurements during module production and macro-assembly has been observed and no pick-up noise has been detected while TRT is read out. Combined tests with cosmic rays allowed to gain experience with the overall operational and running conditions (DAQ, DCS, monitoring, *etc*). The barrel ID (SCT & TRT) has been successfully installed in the ATLAS cavern inside the electromagnetic calorimeter cryostat and the SCT end-caps integration with the TRT has already started and is well under way. The innermost layer of the ID, the Pixel detector, will be installed independently in 2007.

Acknowledgments

The progress reported in this paper represents work performed across the ATLAS SCT collaboration. I would like to thank all my colleagues whose work is presented here and, in particular, Pepe Bernabeu for his useful comments and suggestions.

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A Read-out Driver for Silicon Detectors in ATLAS

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Abstract

I present an overview of a read-out driver (ROD) for silicon detectors in the ATLAS experiment at the Large Hadron Collider (LHC). Two silicon-based ATLAS tracking systems, referred to as the Pixel Detector and the Semiconductor Tracker (SCT), are controlled and read-out using a common 9U VME board. A hybrid design of Field Programmable Gate Arrays (FPGAs) and Digital Signal Processors (DSPs) has allowed the silicon ROD to meet the challenges of format error-counting and event trapping without interfering in the construction and transmission of event fragments to the next level in the read-out system. Performance of the ROD during detector assembly, calibrations and cosmic-ray data-taking are also discussed.

I. Introduction

The ATLAS experiment [1] is a general-purpose detector centered around one of the LHC pp collision points. Two major ATLAS detector subsystems [2] lie closest to the interaction point–the Pixel Detector [3], comprised of more than 8.0×10^7 channels, surrounded by the SCT [4], itself containing more than 6.2×10^6 channels; both are essential for providing the tracking information in the pseudo-rapidity region $0 \leq |\eta| < 2.5$ and are used to tag secondary vertexes from B-hadron decays. The ROD is a 9U VME board common between both of these detector systems and designed to meet the formidable challenge of module configuration and read-out, trigger distribution and event fragment construction.

A. The ATLAS Pixel Detector

The ATLAS Pixel Detector is the tracking subsystem that lies closest to the interaction point. It is comprised of 1456 Pixel modules [5] in three Barrels and 144 modules in each of two Endcaps.

Each Pixel module has 16 Front-end ICs, with 2880 channels per IC for a total of 46080 channels. There are 18 columns and 160 rows of 50×400 μm pixels on each silicon sensor and the ICs are bump-bonded to the sensor. A Module Controller Chip (MCC) [6] is employed on the module for the purpose of collecting data from the 16 FE chips as well as translating commands into chip signals. Groups of seven modules are connected to a single optoBoard, enabling the transmission and reception of optical signals. The read-out rate for the inner-most Barrel layer, known as the "B-Layer," is 160 Mbit/s. Both Pixel Endcaps and Layer-1 (the middle Barrel layer) are read-out at a rate of 80 Mbit/s. The outer-most Barrel layer, Layer-2, is read out at a rate of 40 Mbit/s.

B. The ATLAS Semiconductor Tracker (SCT)

The SCT lies just outside of the Pixel Detector and contains 2112 modules [7] in four Barrels and 988 modules in each of two Endcaps.

An SCT module has two sides with one Hamamatsu silicon sensor on each; the top and bottom sensors are offset from one another by a 40 mrad angle. Each sensor contains 768 instrumented strips at an 80 μm pitch. Each side of the module contains an array of six binary read-out chips, known as the ABCD3TA ASIC [8], that read-out 128 channels each and contain a discriminator, pipeline, data compression logic as well as a read-out buffer. A harness connected to the module includes and opto package to send data off-detector optically; the read-out rate for all SCT Barrels and Endcaps is 40 Mbit/s.

II. The Silicon Read-out Driver (ROD)

The silicon Read-out Driver (ROD) [9] is central to the data acquisition chain (DAQ). The primary purpose of the silicon ROD is module configuration, trigger propagation and data formatting. The secondary purpose of the ROD is detector calibration and monitoring. Control commands are sent from the ROD to the modules as serial data streams. These commands can be Level-1 triggers, bunch-crossing resets, event counter resets, calibration commands or module register data. Each ROD board is responsible for the configuration and read-out of up to 48 SCT or 32 Pixel modules. After formatting the data collected from the modules the ROD transmits these fragments to the ATLAS read-out subsystem (ROS) via S-Link.

Up to 16 RODs can reside inside of a single VME crate. Each VME crate contains one single-board computer (SBC) that is used for communication between the DAQ host computer and the RODs. A single TIming Module (TIM) [10] in the crate receives timing, trigger and control information from ATLAS and passes this information on to the RODs. There is one Back-of-Crate (BOC) [11] card for each ROD and, as the name suggests, the BOC resides in the back of the VME crate just behind the ROD with the backplane forming a partition between them. The BOC is capable of converting electrical commands from the ROD (e.g., triggers) into optical signals and passing them on to the detector modules via optical fibers. Conversely, the BOC can receive optical signals from the modules (e.g., event data) and convert these into electrical signals before passing them on to the ROD. The BOC also hosts the S-Link, which is exploited by the ROD to send formatted event data to the ROS.

The hardware on the ROD itself (Figure 1) is common between the Pixel and the SCT subsystems, however it should be noted that differences in firmware do exist. A hybrid architec-

ture of FPGAs and DSPs allow the ROD maximum versatility during physics-running and calibrations. The FPGAs are dedicated to performing time-critical operations such as ROD setup, module configuration and the formatting, building or routing of events. A single "Master" and four "Slave" DSPs reside on the board and are utilized for the control and coordination of on-ROD operations, as well as performing high-level tasks such as data monitoring and module calibration. Once configured, the ROD FPGAs handle the event data-path to ATLAS Level-2 without further assistance from the DSPs.

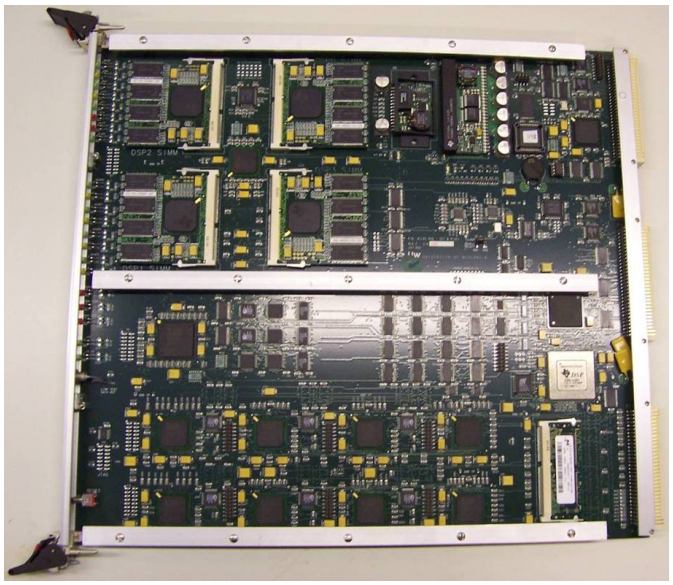

Figure 1: The ATLAS silicon Read-out Driver (ROD).

ROD reset and the VME interface are handled by an FPGA referred to as the Program Reset Manager (PRM). At power-up, the PRM activates the host-to-ROD VME interface and resets the Master DSP (MDSP). Once the MDSP has booted, configuration information is transmitted for the Controller FPGA as well as the data-path FPGAs–known as the Formatter, the Event Fragment Builder and the Router (Figure 2). The farm of Slave DSPs (SDSPs) are loaded with boot code from the host via the MDSP.

The ROD supports two main modes of operation: physics data-taking and calibrations. During physics data-taking triggers issued from ATLAS are relayed to the ROD via the TIM. When running calibrations the MDSP serial ports can be used to issue triggers to the modules. In both modes of operation, the data-path through the Formatter and the Event Fragment Builder remain the same. In calibration mode the Router sends events to the farm of SDSPs for histogramming, whereas in data-taking mode they are routed to the ROS via the S-Link.

In the event that the S-Link is receiving data from the ROD faster than it can be transfered to the ROS during physics data-taking, the S-Link will apply back-pressure to the ROD thereby halting the output of events from the ROD EFB. If back-pressure continues to be applied and the EFB memories become full, back-pressure is propagated to the Formatter FPGAs stopping the transmission of event data from the Formatters. If a critical limit in the Formatter memories is reached, a ROD Busy signal will be sent to the TIM halting triggers from ATLAS. The likelihood of this occurring even with 2.5 times the projected occupancy at the highest luminosity is exceptionally low.

A. ROD Controller FPGA and Master DSP

The main function of the ROD Controller FPGA and Master DSP is to setup the ROD data-path, to execute BOC and silicon module configuration and to process as well as propagate triggers.

The MDSP is a Texas Instruments 6201 integer DSP running at 160 MHz with two internal 64 kB blocks of memory and an additional 32 MB of (slower) external memory. The MDSP has ROD and BOC registers connected to one of its External Memory InterFaces (EMIFs) thereby allowing any ROD or BOC registers to be set from the host via the MDSP. The MDSP runs software to perform system functions while the FPGA performs real-time functions. Module configuration is performed by the MDSP using its multi-channel buffered serial ports (SP0 and SP1); configuration data is passed to the MDSP from the host. In calibration mode the MDSP serial ports are also used to send triggers.

During normal ATLAS running the trigger and event description information (Level-1 ID, bunch-count ID and trigger-type) is supplied to the ROD by the TIM. The TIM trigger is detected inside of the Controller and expanded into the trigger codes required by the Pixel and SCT modules. The trigger code is then sent out a 48-wide mask gate and propagated on to the modules.

B. Formatter FPGAs

The Pixel MCC and the SCT ABCD3TA each return a bit stream. The BOC splits these into individual 40 MHz streams. The ROD input links receive the data streams from the BOC. For the inner-most layers of the silicon tracker, the data comes in over several links at multiples of this 40 MHz.

Eight identical ROD Formatter FPGAs serve the purpose of serial-to-parallel conversion of the event data coming from the modules and to de-randomize event fragments. The Formatters are also used to detect module packet errors and inform the Controller FPGA when link trailers have been received.

The FPGA firmware is subsystem specific. The version for the Pixel Detector contains four links per Formatter and the version supporting the SCT allows for 12 links per Formatter. A single ROD SCT Formatter gathers the data from up to six modules (there are two read-out links per module). For the Pixel Detector the number of modules read out by a single Formatter depends on the rate used. The 40 Mbit/s, 80 Mbit/s and 160 Mbit/s modes support the read-out of four, two and one module(s) per Formatter, respectively.

C. Event Fragment Builder FPGA

The purpose of the ROD Event Fragment Builder (EFB) is to collect the Formatter output, check the L1 and BC IDs, count errors and generate the event header and trailer.

The EFB contains two engines to collect the Formatter output. Information from the ROD Controller FPGA regarding Event Data and trigger type as well as L1 and BCIDs are accepted by the EFB Header and Trailer Generator and compared with the data collected by each of the two EFB engines. The EFB flags event errors by using dedicated bits inside of the event header and trailer.

Once the event data from the two engines are ready, as well as the header and trailer, the EFB passes this information onto the ROD Router FPGA.

D. Router FPGA and Slave DSP Farm

The purpose of the Router FPGA is to route formatted data to ATLAS Level-2 and/or the Slave DSPs. The four SDSPs are used for error counting as well as event capture and histogramming. The slave DSPs are Texas Instruments 6713 floating-point DSPs running at 220 MHz with 256 kB of internal memory, 256 MB of (slower) external memory, and are used for monitoring in addition to calibration histogramming. One EMIF of each SDSP is connected to a separate pipeline in the Router FPGA, thus allowing events to be transferred to any SDSP independently. The full memory range of the four SDSPs are available to the MDSP through registers attached the the SDSP host port interfaces. SDSP external memory is used to store event histograms.

III. ROD Communication

A system of communication registers, primitives, tasks and text-buffers are used for host-to-ROD and MDSP-to-SDSP communication and control.

A. Communication Registers

A series of communication registers, blocks of 32-bit words at the start of the DSP's internal memory, are regularly checked by the MDSP while inside of the main (infinite) loop of the software running on the processor. The MDSP polls these registers, watching for requests from the host (user). Similarly, these registers are used to indicate the status of the DSPs to the host.

There are quite a few different types of Communication Registers on the ROD. General Status Registers keep a tally of the number of tasks currently running, note if the event trapping is engaged, etc. Dedicated Histogramming Registers are used to report calibration scans statistics. Registers specific to inter-DSP communication (i.e., MDSP-to-SDSP) also exist.

B. Primitives

The ROD FPGA registers are mapped in the MDSP memory space. A system using software entities known as primitives allows the MDSP to remain in control of its memory while receiving commands from the host. It is through the use of primitives that reading and writing to ROD registers is possible; the ROD and BOC are configured and initialized using this system of primitives. In general, primitives are executed once by the DSP.

Primitives exist for reading and writing FPGA registers, reading and writing regions of MDSP memory, loading or modifying silicon module configurations, and starting the SDSPs. The MDSP can send primitive lists to the SDSPs to start calibration histogramming, for example. The DSP software is versatile enough to handle new primitives written by the user; these are simple and easy to compose.

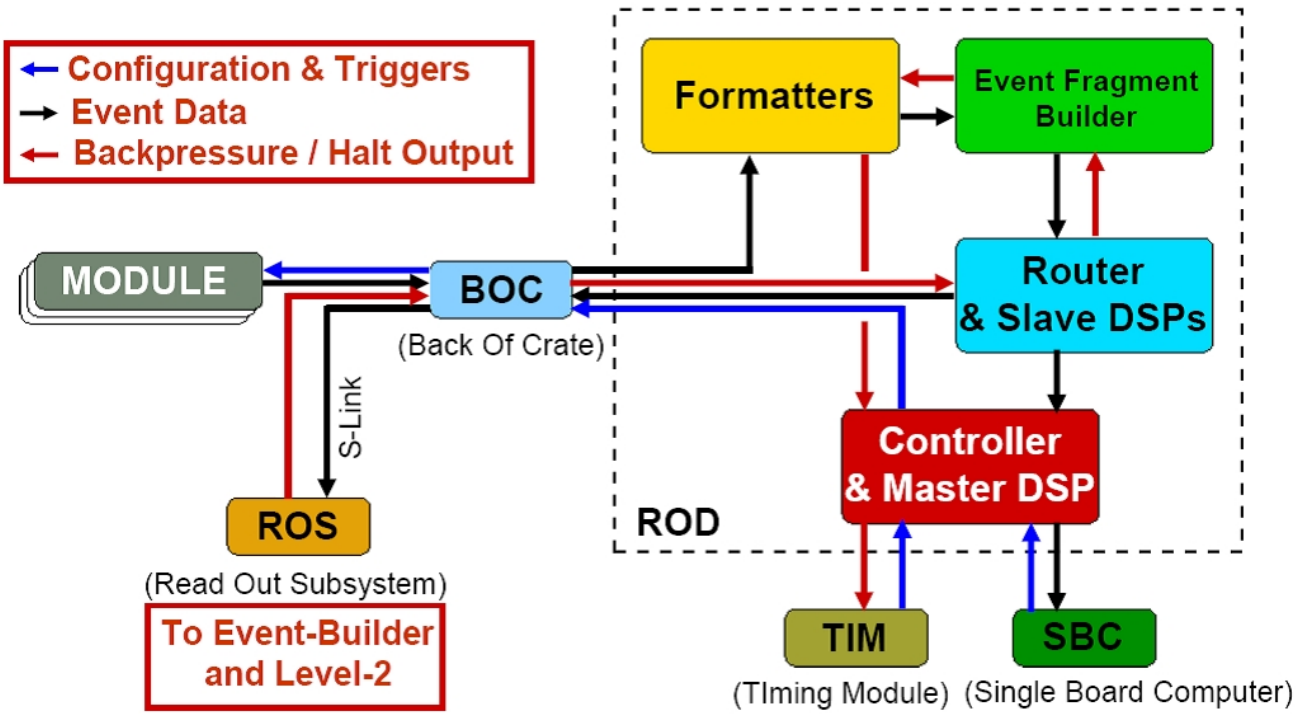

Figure 2: The path of command and event data through the ATLAS silicon ROD.

C. Tasks

Primitives are typically executed once whereas tasks execute ROD functions over an extended period of time. These operate independent of the Primitive Lists, however the ROD can still process Primitive Lists while various tasks are running. Tasks start and stop by the host (or MDSP) sending primitives and they run until they complete or are halted manually. The Event Trapping and Histogramming Tasks are just a couple of examples. The former runs on the SDSPs to handle event trapping while the latter manages the issuance of triggers along with the processing and binning of event data.

IV. Operating Modes

Both physics data-taking and calibration modes are supported by the silicon ROD.

A. Physics Data-taking

Once the data-path on the ROD has been setup, it is completely handled by the FPGAs and does not require any intervention from the DSPs. During physics data-taking the Router FPGA possesses the capability of capturing events on a user-defined pre-scale (i.e., every nth event) and sending them to the farm of SDSPs on a non-interfering basis. One could conceive of collecting such events, binning them, and comparing with a set of reference histograms thereby providing detector experts with information on channels with unusually high or low occupancies.

B. Calibration

In calibration mode the transmission of data through the S-Link is inhibited. Instead, frames of data (256 32-bit word chunks) are passed from the Router FPGA to the SDSPs using Direct Memory Access (DMA) transfer. Tasks running on the SDSPs flag these transfered events for processing and subsequent histogramming. A monitoring task can be run on the SDSPs that is capable of parsing the event errors flagged by the FPGAs and reporting these errors back to the host.

Two of the most common Pixel calibration scans focus on the determination of thresholds and noise. During the Threshold Scan, on-chip charge injection is carried out for each individual pixel. The number of hits for each injected charge is scanned to obtain the discriminator threshold (Figure 3). A Noise Scan is simply a Threshold Scan without any charge injection and is used to measure the noise occupancy.

SCT calibration scans include tests of basic communication such as the Rx Threshold Test (optimize the Rx threshold value in the BOC data-receiver chip), as well as a suite of digital and analog tests like the N-Mask Test (demonstrate that the chip mask register functions properly; Figure 4) and the Noise Occupancy Test.

V. ROD Performance

Production RODs have been used extensively during silicon detector assembly, runs with test beam, and most recently during a period of cosmic-ray data-taking.

A. ROD use during Detector Assembly

Calibration scans have been used routinely during module production [12] to verify module functionality before and after being mounted or transported. Such scans also help to rank production modules by the number of defects so that only the very best may be mounted on the detector and installed in ATLAS.

The detector assembly phase has given essential feedback to the ROD hardware, firmware and software developers. Several DSP software and FPGA firmware problems have been uncovered during the production and assembly tests thus giving the programmers critical feedback before physics running with complete detectors in the ATLAS Collision Hall.

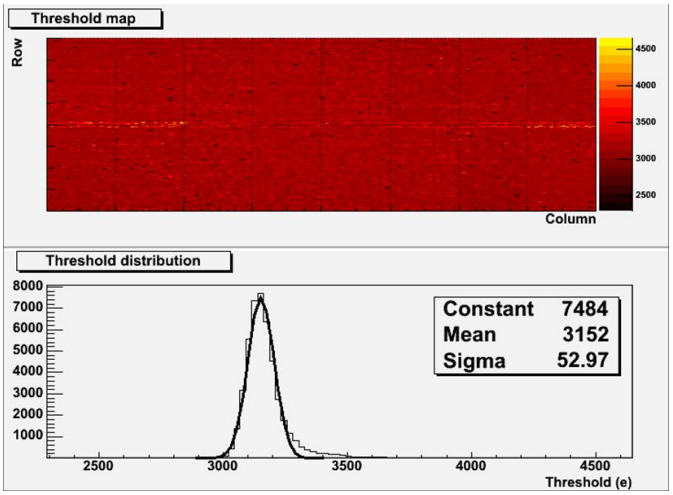

Figure 3: The results of a Pixel Threshold calibration scan.

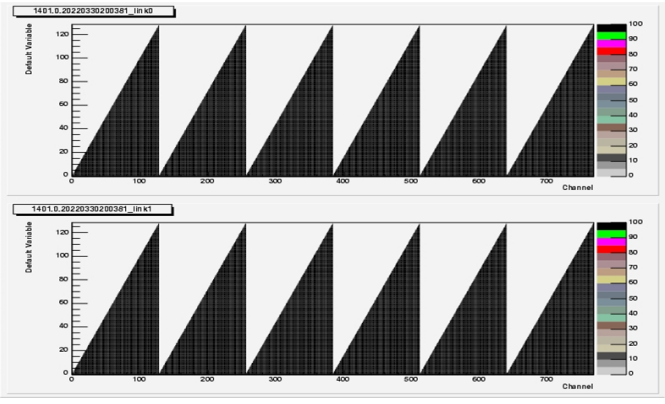

Figure 4: The results of an SCT N-Mask calibration scan.

B. ROD use during Cosmics Running

The production ROD as well as some of the very latest FPGA firmware and DSP software were tested extensively during a period of combined cosmics running using the ATLAS Transition Radiation Tracker (TRT) and SCT Barrels in May 2006. The ROD performed well during this very successful run

in which more than 400k events were collected. This large-scale test involved ∼500 SCT modules (∼10 RODs) and served as a useful DAQ and detector shake-down in addition to providing data for detector efficiency and alignment studies.

VI. Conclusions

Approximately 260 production ROD boards have been assembled and tested. Roughly 160 of these are dedicated to the Pixel Detector while the remaining fraction are assigned for use by the SCT Barrels and Endcaps. Many of these boards are now installed in the ATLAS USA-15 counting-room crates; their location for ATLAS physics data-taking.

The final production version of the ROD has already been used extensively during module production and detector assembly at various sites around the world, as well as during test-beam runs at CERN [13] and the combined cosmic-ray data-taking run.

We are looking forward to larger-scale multi-crate tests and with the SCT Barrels now lowered into the ATLAS Collision Hall that opportunity is rapidly approaching. Additional testing during the upcoming cosmics data-taking run using one of the Pixel Endcaps is another opportunity to gain additional experience reading-out large numbers of modules.

Future work will focus on speeding up the DSP software to shorten the time taken for both module configuration and calibration scans. Any implementation of on-ROD data-quality and detector monitoring during physics data-taking as well as an automated response for module recovery and re-configuration (in conjunction with the DAQ and Detector Control System) would certainly prove to be very beneficial.

VII. Acknowlegements

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The Vertex detector of the LHCb Experiment: The VeLo

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Abstract

The LHCb experiment is the dedicated b physics experiment of the LHC that will study CP violation and rare b decays. Its vertex detector called *VeLo* (Vertex Locator) has been designed to achieve an impact parameter resolution of 14μm + 35μm/p$_T$ and a propertime resolution of 40fs^{-1}. The main components of the detector and module are introduced focusing on the radiation hard front end Beetle chip, the radiation tolerant silicon sensors and the readout system of the detector. In preliminary testbeam results a resolution of 8μm and 4μm for tracks of angle 0.16rad has been measured. Construction, assembly and commissioning are currently on going. The latest commissioning showing the successful performance of the VeLo alignment algorithm.

I. Introduction

The $LHCb$ experiment[1] (see figure 1) is the only dedicated b physics experiment located in the Large Hadron Collider(LHC) ring. It is a one arm forward spectrometer whose design has been optimised for the measurement of the $b\bar{b}$ pairs to study CP violation and rare b decays. These include excellent particle identification and vertexing. The vertexing and finding their location are the main tasks of the most forward tracking detector in LHCb called the Vertex Locator(VeLo) which is the main focus of this note.

II. The VeLo

The geometry of the vertex detector has been designed to measure the displaced vertices that are part of the topology of a $b\bar{b}$ event. It is called the Vertex Locator (VeLo) but it is not a vertex detector in the classical sense because it also has tracking capabilities which on average contributes around 13 hits to the global tracking. For LHCb to be sensitive to the expected oscillations in the B_s system the detector has been designed with the following goals in mind. A primary vertex resolution of 8μm for the x and y axis and 44μm in the z direction. The impact resolution of 14μm + 35μm/p$_T$ which results in a propertime resolution of 40fs^{-1}. This has been achieved by placing the detector in vacuum and as close as possible to the LHC beam with the edge of the sensors being only 8mm from the centre of the beam.

Another task the VeLo has been designed for is to contribute to the High Level Trigger(HLT) [3]. This is an offline trigger which first uses the Rz information of tracks to find B-decays and if promising the Phi coordinates. Once fitted the information is fed to the next stages of the HLT.

Physically the VeLo detector is approximately 1m long and is composed of two halves. Each half possess 21 modules whose instrumented face is perpendicular to the beam. The two halves are operated in vacuum and can be moved towards or away from the beam. The beam vacuum is separated from the detector vacuum by a 250μm thick aluminium $RFfoil$ on each side. The detector uses evaporative cooling with CO_2 gas and the electrical connection to the module is achieved by flat kapton cables through a 50 pin feedthrough. A detailed description of the VeLo can be found here [2].

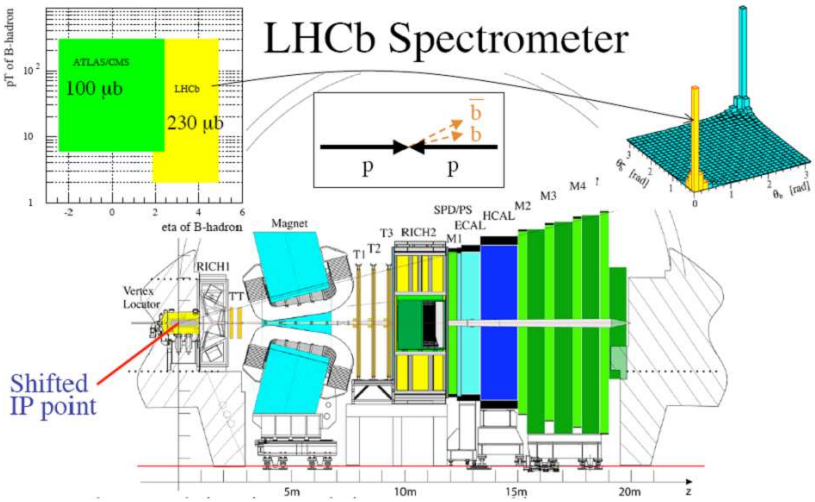

Figure 1: The LHCb spectrometer featuring the VeLo detector at the front.

The are a number of constraints that has influence the design of the VeLo module. The major constraints are:

1 The instrumented region to be placed as closed as possible to the beam to minimise the distance between the primary vertex and first point of measurement.
2 To be able to withstand the high radiation dosage expected at the LHC.
3 The position of the clusters to be measured in cylindrical coordinates.
4 Minimise the scattering from the supporting structures.

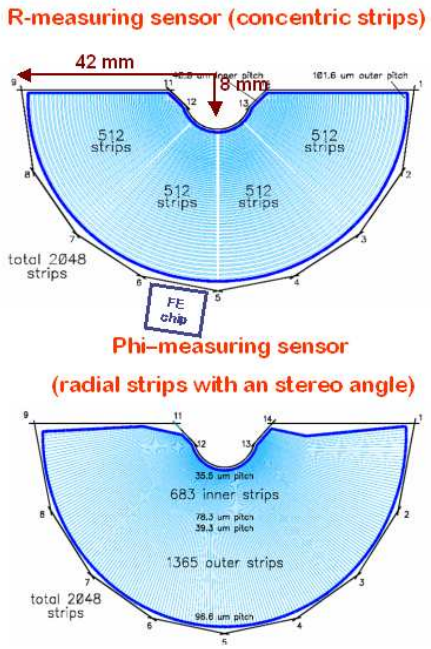

Figure 2: The Phi and the R measuring sensors that are part of each VeLo module.

The first constraint was addressed by having sensors with a semi circle shape as shown in figure 2 with the inner radius being 8mm and the outer radius 42mm. The cylindrical coordinates system is achieved by instrumenting each sensor with either concentric or radial strips. Each sensor has a total of 2048 strips whose pitch increases with respect to radius (40-100μm) keeping the occupancy of each channel uniform and allowing the complete surface to be instrumented.

The sensor is a single sided 300μm thick n-on-n oxygenated silicon fabricated by Micron. It has been designed to deplete from the back and after type inversion to deplete from the strips. This technology has been developed to allow sensors to withstand the high radiation environment that the VeLo will operate in, 1.3×10^{14} neq/cm^2/year at a radius of 8mm and 5×10^{12} neq/cm^2/year at the edge of the sensor (r = 42mm)[4].

The module (See figure 3) has two sensors of each type that are glued back to back on opposite surfaces of the hybrid. A double sided kapton circuit is also glued to its surface. The heat generated is efficiently removed due to the construction of the hybrid, a TPG plane in between a number of carbon fibre rectangles.

Another important features of the module is the paddle to which the hybrid is glued to. The purpose of the paddle was to move the supporting plate away from the beam in accordance to the last constraint previously listed. Physically the paddle is a carbon fibre shell with a height of 16cm whose surface has been treated to minimise outgassing during vacuum operation.



Figure 3: A VeLo module. The main components shown are the paddle, the hybrid, the front end chips and the sensor.

III. The Beetle chip and its selection

The front end readout chip that is employed by the VeLo module is the Beetle v1.5. The chip is radiation hard by virtue of the process technology (0.25μm standard CMOS with a thin gate oxide, $t_{ox} \approx \mathring{A}$) used for its fabrication and the consistent used of enclosed NMOS transistors. The latter reduces the shift in the transistor threshold voltage and eliminates leakage current paths. The design has incorporated triple redundant logic to minimise Single Event Upsets (SEU) and has been tested up to a radiation dose of 130MRads. A complete description can be found here [5].

The Beetle chip has 128 readout channels which can operate in analogue or binary mode. Each channel has an analogue front-end which consists of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. For VeLo operation the comparator that discriminates the acquired pulse is not enabled, only the shaper output is sampled and stored into the analogue pipeline.

A complete VeLo will require a total of 1344 chips. Ideally these chips will be identical in their characteristic and performance, making it easier to understand the capabilities and degradation of the VeLo during its operation at the LHC. In reality the performance tend to vary from chip to chip hence the need to test each single one and select a batch whose characteristics are within defined limits. The testing referred to as wafer probing[6] focused on the Beetle's power consumption, digital performance, characterisation of the analogue front ends and DACs used to bias the different circuits on the chip.

The power consumption focused on measuring the current drawn by an individual chip after power on and during normal operation. The digital performance mainly involved exercising the chip's communication on the I2C bus and the transfer of data. The characterisation of analogue front end was performed on each channel of the chip for a number of bias settings. From each pulse obtained parameters were extracted as shown for a typical pulse in figure 4. Finally all the DACs relevant to the operation of the chip were exercised allowing their gradient and correct operation of each bit to be measured and asserted.

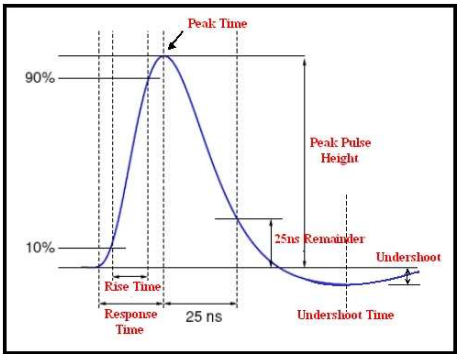

Figure 4: The typical pulse shape from a Beetle channel.

The analysis of all the measurements and tests, developed in Glasgow [7], resulted in 69 variables being defined that characterised the performance of a Beetle chip. For each variable distributions were created which included the values of the same type of chip from 18 wafers. A total of 4299 chips composed each distribution. The selection criteria was implemented as cuts about the mean of the distributions. The value of the cut was calculated by multiplying the RMS of the distribution by a factor. This factor has direct influence on the uniformity of the batch and thus the yield of the selection criteria.

A problem that was encountered during the analysis was related to the non correlation of the different distributions. For example chips with average currents would have a dac gradient which was outside the limits. The actual gradient would have little effect on the performance of the chip but a one factor policy would see chips like this being rejected even though important parameters such as the currents were within limits. To overcome this problem and maximise the yield, the variables were classify into two groups. The first group contained all the variables whose value was deemed important towards the performance and operation of the chip. A very stringent cut would be placed on their distributions. The second group would contained the rest of the variables and cuts were placed mainly to guarantee functionality.

The first group was composed of 18 variables such as currents, all the digital performance and some pulse shape parameters such as $PulseRiseTime$ and the ratio of $Remainder/PulseHeight$. The second group was composed of the remaining 51 variables. The value of the two factors were obtained from a yield map (factor$_1$ vs factor$_2$). It was reasoned that a batch of 2000 chips (a yield of ≈50%) would provide a generous margin over the required number and the corresponding factors (2.2 and 3.5) result in chips whose uniformity is adequate for VeLo operations. The resulting current distribution of the selected chips is shown in figure 5 and typical analogue parameters for a Beetle 1.5 in table 1.

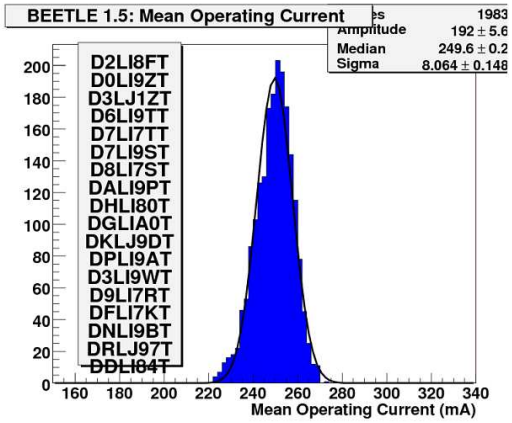

Figure 5: The operating current distribution of the selected Beetle chips.

Variable	Mean	RMS
Pulse Response Time (t90)ns	40.78	0.80
Pulse Rise Time t(90-10)ns	15.41	0.67
Undershoot - Peak Time ns	62.79	1.70
Peak Pulse Height (ADC)	71.64	2.92
Undershoot/Peak Height	-0.113	0.00646
25ns Remainder/Peak Height	0.135	0.032

Table 1: The mean obtained from the distribution featuring ≈ 2000 chips and its RMS for the analogue parameters obtained during the wafer probing. The chips were exercised using the VeLo settings (ITP=24,VFS=56 and VFP=20).

IV. The VeLo DAQ

The VeLo DAQ is composed by a number of systems that performs all the necessary operations to control the front ends, provide clock and triggers and read the digitised data. The implementation of the DAQ has physical components distributed in the counting room (60m from the beam), the balcony (20m from the beam) and outside the VeLo tank. The last two positions require boards to be tolerant to radiation levels of 500Rads and 100kRads respectively.

The control board is located in the balcony and receives the Timing and Fast Control (TFC) signals such as the trigger and the clock and together with the I2C signals to operate the front ends. These are routed to five outputs with each output connected to an individual hybrid through the Repeater board attached to the outside of the VeLo tank.

The repeater board performs a number of functions which are implemented in the mezzanine cards that it carries. The two main ones are: the $Low\ Voltage$ card and the $Driver$ card. The $Low\ Voltage$ card powers the front ends and mezzanines through 8 radhard voltage regulators. The $Driver$ card amplifies the analogue signals from the front ends before they are transmitted at 40MHz through a 60m cable to the receiver card

located in the counting room. The output of the module consists of four analogue links with each link connected to a driver card.

The receiver card is part of the TELL1[8] board which digitises the incoming analogue signal. The TELL1 is an FPGA based signal processing board on which a number of algorithms have been implemented such as zero suppression, clustering and Finite Impulse Response filters with which to process the incoming signal. If a trigger is received the data is sent to the readout network which is implemented as gigabit ethernet and internet protocol (IPV4) with the final destination being the computing farm.

V. Performance of a VeLo module

There has been a number of testbeam conducted by the VeLo group to understand and measure the performance of the VeLo module design. The results presented in this note are from the 2004 testbeam that was carried out at the North Area Facility at CERN. The main results obtained from a module with a 300μm thick Phi sensor are shown in figures 6, 7 and 8. The first graph shows the resolution as a function of strip pitch measured during the testbeam at 250V(middle line). For comparison the corresponding binary resolution and the resolution obtained from a previous Hammatsu prototype at 180V are also shown. The binary resolution is the upper line while the results from the prototype provide the lower limit. The higher resolution of the prototype sensor is attributed to diffusion of the charge which at lower voltages plays a significant role thus allowing the charge to be shared more effectively.

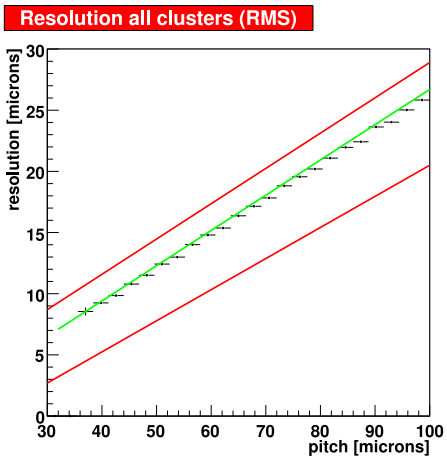

Figure 6: The measured resolution of the Phi module at 250V versus the pitch. The measurement is the middle line while the simulation are represented by dots. This is compared to the resolution obtained with a binary readout scheme(top red line) and the results of an earlier prototype at 180V(bottom red line).

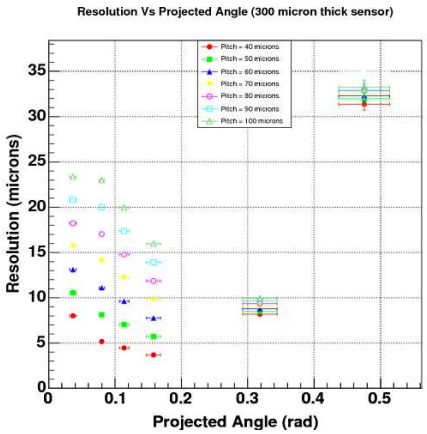

Figure 7: The resolution of clusters for different strip pitch as a function of track angle measured for the 300μm thick Phi module. The average track expected by the VeLo is 0.12rad almost coinciding with the best resolution measured.

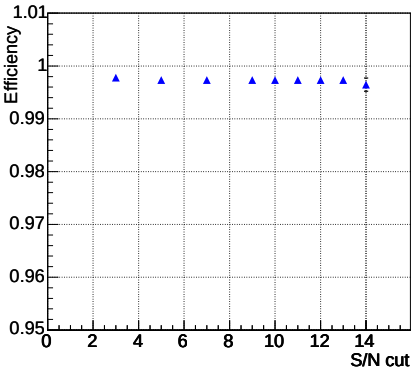

Figure 8: The efficiency of the PHI 300μm thick sensor module as a function of the cut placed on the signal to noise ratio.

The second graph shows the resolution of different strip pitch with respect to angle track. The change is mainly due to the change in geometry that the incident particle experiences. As the angle increases the charge deposited by the track is distributed over a greater number of channels increasing the sensitivity when determining the centre of the cluster. The same effect occurs throughout the sensor as tracks incident on the different strip pitches follow the same trend. The encouraging news is that the average angle of the tracks expected to traverse the VeLo is 0.12rad[4] roughly coincides with the optimal resolution.

The third graph features the efficiency of the module with respect to signal to noise cut. The efficiency is constant throughout much of the range of the cut with a value ≈99.8%. It is only when the cut is greater than 13 that efficiency slightly deteriorates. This together with the two previous graphs shows that the current module design is expected to deliver the design goals for the VeLo.

VI. COMMISSIONING

The current focus of the VeLo group is on the construction, assembly and commissioning of the complete detector. The modules are being constructed at Liverpool and the burn-in performed at CERN before they are assembled into the final mechanics. Once assembled, the detector will be taken to into the pit (IP8) where the complete detector will be commissioned. To ensure the performance is satisfactory, a number of smaller commissions are conducted prior to this one. As production versions of the components become available the complexity and thoroughness of the commission increases. The exercise incorporates everything that is related to the VeLo, software and hardware and they are fondly referred to as ACDCs (Alignment Challenge and Detector Commissioning).

The first ACDC, conducted in July 2006, was an online DAQ exercise. The second, performed in August 2006, included three production grade modules that were powered using production Repeater boards and their data read using the production chain together with cables. On the software side employing the alignment algorithm developed for the VeLo[9] was a great achievement. For the third ACDC, scheduled for November 2006, the final right half mechanics will be installed in the testbeam area containing 10 production modules. This will be the dress rehearsal for the final commissioning since at least 6 modules will be read and controlled simultaneously.

Preliminary results from ACDC2 results are shown in figure 9. Four graphs are shown featuring residuals of only straight tracks from a tested module. The distributions are separated into x and y axis (left and right) together with before and after alignment (top and bottom). The success of the alignment algorithm is evident in the decrease of the sigma of the fitted gaussians to the distributions (50μm to 16μm and 22μm to 19μm for the x and y axis respectively) and their centring around zero. The favourable results of the alignment resulted in the testing of other software components such as the tracking and simulation.

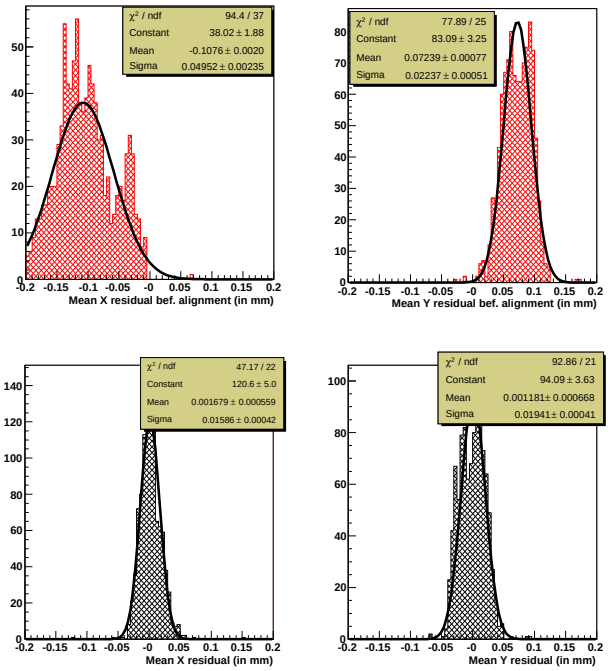

Figure 9: The preliminary residual distributions obtained for straight tracks. A decrease in the sigma of the fitted gaussian and a mean zero are evidence of the alignment performed favourable.

VII. CONCLUSION

The VeLo is a key detector required by the LHCb experiment to achieve its physics program. Its unusual shape is due to the need to maximise its performance with respect to impact parameter resolution, propertime resolution and incorporate acquired data into the second level trigger. The module has been designed to operate in vacuum and in the harsh LHC radiation environment. Radiation tolerant oxygenated n-on-n silicon sensors and the Beetle readout chip, tested upto 130MRads are the key elements of the module.

The selection criteria of the Beetle presented was developed to maximise the performance uniformity of the modules. The yield was $\approx 50\%$ but the resulting number provided a generous margin to complete the VeLo detector. The performance of the module during 2004 testbeam is summarised as having a resolution of 8μm and 4μm for tracks of angle 0.16rad for the smallest strip pitch. This is within the necessary values to achieve the design goals. Currently the group is focussing its efforts on the construction, assembly and final commissioning of the complete detector. Preliminary work with the data taken with ACDC2 allowed modules to be aligned using straight tracks by applying the VeLo alignment algorithm.

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Design and test of the final ALICE SDD CARLOS end ladder board

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Abstract

The paper presents the design and test of the final prototype of the CARLOS (Compression And Run Length Encoding Subsystem) end ladder board that is going to be used in the ALICE experiment at CERN. This board is able to compress data coming from one Silicon Drift Detector (SDD) front-end electronics and to send them towards the data concentrator card CARLOSrx in counting room via a 800 Mb/s optical link. The board design faces several constraints, mainly size (54x49 mm) and radiation tolerance: for this reason the board contains several CERN developed ASICs. A test setup has been realized for selecting the good devices among the 500 cards already produced.

I. Introduction

The Inner Tracking System (ITS) [1] of the ALICE experiment contains six coaxial cylindrical layers. Layers 3 contains 14 ladders each one hosting 6 SDDs, while layer 4 contains 22 ladders each one hosting 8 SDDs. The CARLOS end ladder board is placed on both sides of each ladder with the purpose of acquiring and compressing data coming from each SDD before sending them towards the data concentrator card CARLOSrx in counting room through optical fibers. The board contains the compression chip CARLOS [2] that performs a bi-dimensional compression of the data coming from the SDD front-end electronics. CARLOS 16-bit output bus is encoded with 8B/10B Ethernet protocol and sent to a single mode optical fiber using a 1310 nm optical laser with a total data throughput of 800 Mb/s.

II. Final CARLOS End Ladder Board

Figure 1a and Figure 1b show the layout of the components' positions on the final CARLOS end ladder card. Looking at Figure 1a from the top-right corner the 1310 nm edge-emitting laser diode is shown. This component transmits the compressed and packed dataset to the CARLOSrx board, at a rate of 800 Mb/s. Below the laser, two pin-diodes (FT1 and FT2) receive the clock and the serial signals. The latter signal provides the system configuration at start-up and may stop the acquisition in event of channel congestion. The 2 pin-diodes and the laser are single-mode 1310 nm (wavelength) pig-tailed modules. These modules are interfaced with the commercial transceivers (Optoway SPS-7110) on the CARLOSrx card via optical adaptors. In more detail, the

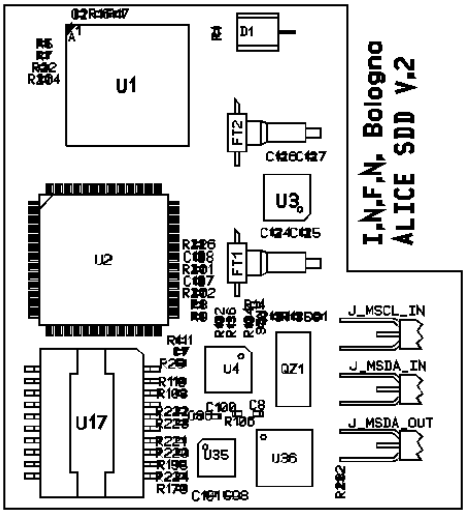

Figure 1a: CARLOS end ladder card layout top view.

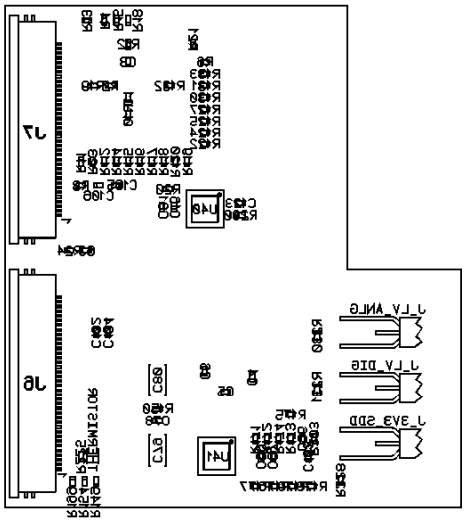

Figure 1b: CARLOS end ladder card layout bottom view.

signals received on the pin-diode interface with the other components through the 2-channel receiver chip RX40.

Let us now describe the system data-flow. The dataset that originates from the Front End Electronics (FEE) enters the

card through the Molex connectors and is read by the CARLOS chip. This performs basically a bi-dimensional compression [3], [4] during the normal DAQ mode and works as a system JTAG switch during the FEE configuration. CARLOS reduces and packs the dataset and its outputs are serialized via the Gigabit Optical Link (GOL) serializer chip that interfaces, by means of an 800Mb/s link [5], with the laser diode. Finally, the GOL chip serializes the dataset that is reconstructed within the Counting Room Emulator by a mirroring de-serializer device that outputs the data to the state analyzer instruments. As the GOL chip requires a low-jitter clock signal, as low as 50 ps peak-to-peak, the QPLL clock filter chip has been applied. This locks the 40.08 MHz clock signal, derived from one of the two pin-diodes, on a very-low-jitter 160.3 MHz crystal (QZ1). Then this frequency is divided by 4 and passed to the GOL and CARLOS chips. The low-right corner of the Figure 1a shows the layout for the 3 twisted pairs of the I2C bus that it is used for monitoring some embedded parameters, such as supply voltage, temperature and current on the front-end and CARLOS end ladder boards. The bus is remotely controlled by the Detector Control System (DCS) card that interfaces the DILBERT and DCU chips on the CARLOS end ladder board. This control bus (I2C) allows to reset the DCU, to inhibit the power-supply for FEE and to power-cycle the GOL chip. The power-cycle feature is achieved by using the CRT4T [6] [7], a CMOS power switching chip developed by the CERN Microelectronics Group.

Three twisted pairs (in the bottom side of the card, see Figure 1b) are used for implementing the fine voltage regulation for the FEE and CARLOS end ladder. The chips are powered with a 2.5 V low voltage regulator (LHC4913) that is configured for an overall current of 1 A. All the components embedded into the final CARLOS end ladder board are Application Specific Integrated Circuits (ASICs) designed to be radiation-tolerant to the total ionizing dose that is estimated (nearly 30 krads) for a 10-years of data-taking within the ALICE ITS environment

III. CARLOS End Ladder System Test

The CARLOS end ladder board as a whole is qualified using two different test setups. The first setup is used to verify the behaviour of the CARLOS end ladder board together with the electronics developed for the ALICE-SDD experiments.

The second is a Bit Error Rate Test (BERT) system, which is used to measure an upper limit on the BER, when the CARLOS end ladder board is operated under ideal laboratory conditions.

A. Experimental Results

The card was tested using the test setup shown in Figure 2. The SDD module contains the FEE that generate the 16 bit data streams at 40 MHz to be fed to the CARLOS end ladder board.

The data are processed by the card and sent via optical link to the receiver board that interfaces the ALICE Detector Data Link (DDL) [8]. In this way it is possible to

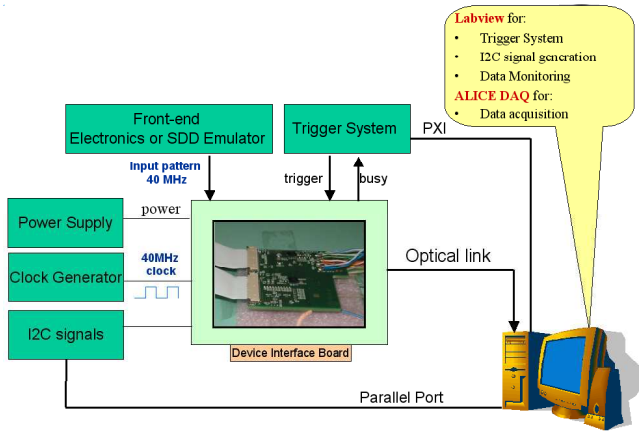

Figure 2: Test setup for CARLOS end ladder board.

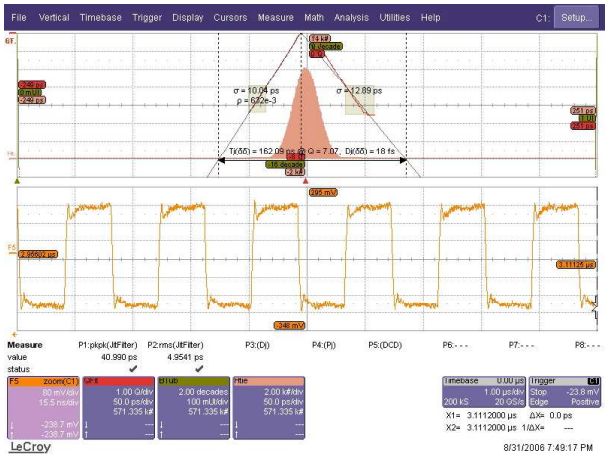

Figure 3: QPLL jitter filtering results.

store and monitor the data processed by the CARLOS end ladder card looking for errors in the structure of the data. A Labview program controls the instrumentation used to generate the trigger and I2C signals that are used to start the acquisition and monitoring of the control parameters (i.e. temperature, voltage and current) and digital lines (i.e. power to GOL) for the CARLOS end ladder board and the FEE. This setup has confirmed the validity of the architecture implemented in the CARLOS end ladder board.

Figure 3 shows the measurements for the CARLOS end ladder board hosting the QPLL circuit. Since the output clock jitter is less than 50 ps peak-to-peak and is less than 10 ps RMS when the input jitter less than 120 ps RMS, this confirms the achievements of the design goals.

The CARLOS end ladder board delivers a clean eye diagram when driven with a bias current of 16 mA at 800 Mb/s, as shown in Figure 4. At this current, the optical power output from the MU connector is approximately –5 dBm.

Figure 5 shows the bathtub plot for the transmission of data via optical link, the horizontal axis is the unit interval (UI) of 1.25 ns and the logarithmic vertical axis is BER. The estimated BER from the signal-to-noise ratio of the eye diagram is less 10^{-16} with a 70% open eye. This diagram

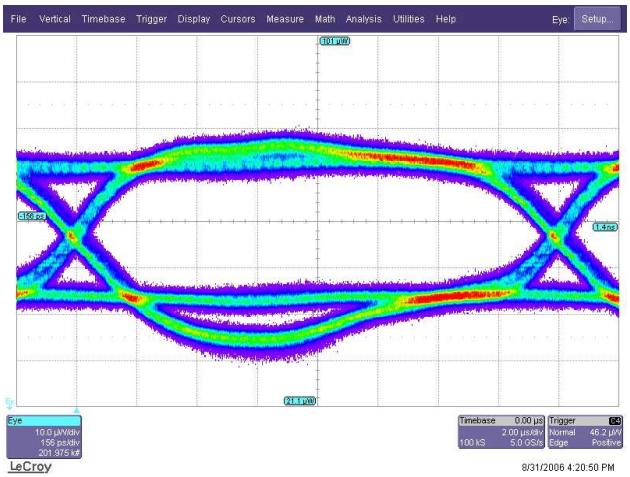

Figure 4: Eye diagram at 800 Mbits/s.

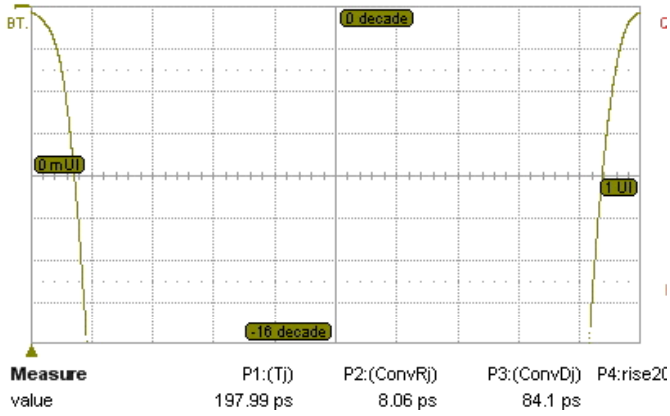

Figure 5: Bathtub curve.

shows the quality of the optical link and the quality of the filtered clock.

B. BERT System

The BERT is a custom-built system based on a SDD emulator FPGA board, CARLOS end ladder board and BERT card. It is illustrated in Figure 6. The SDD emulator is a special card developed by Bologna group that emulates the signals coming from the FEE, with the difference that it is possible to send a specific data pattern to the CARLOS end ladder board. Xilinx FPGA's on the SDD emulator (XC2V1000) and BERT (XC2VP7) cards generate data input to the CARLOS end ladder board and read output form the deserializer (TLK1501), respectively.

The firmware implemented in the BERT card compares bit-by-bit the expected data with the acquired data and if a mismatch is found the firmware increases the error count and the position in the pattern for future analysis. In this way the BERT card compares the bits at the same speed of the acquisition (640 Mb/s).

Using the BERT system the bit error rate has been measured to be less than 10^{-14}, comparable to the estimated BER from the signal-to-noise ratio of the eye diagram.

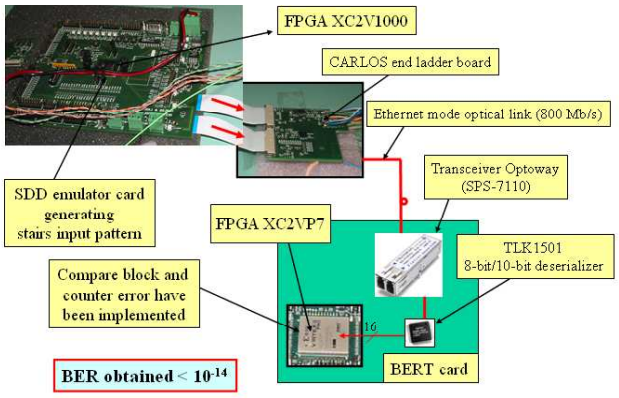

Figure 6: Bit Error Rate Test (BERT) system setup.

IV. Integration With The FEE

The CARLOS end ladder board has been tested and assembled in the ladder structure with the final FEE, readout and power supply electronics. In Figure 7 the CARLOS end ladder boards placed on the end side of the ladder are shown. No errors were attributed to the CARLOS end ladder board during these tests.

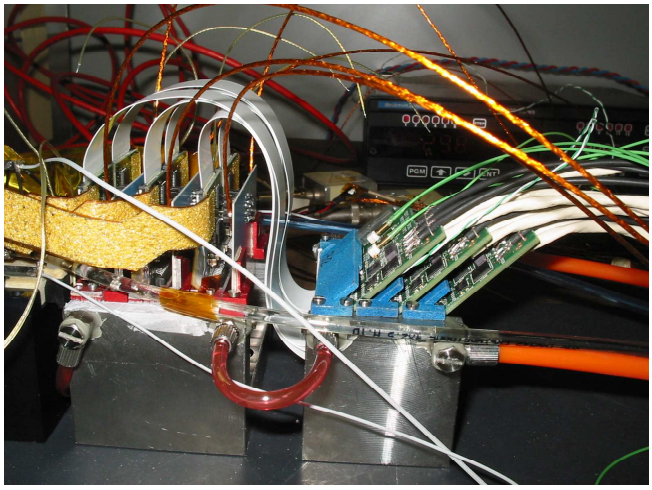

Figure 7: CARLOS end ladder boards assembled in the ladder structure.

V. Conclusions

The CARLOS end ladder board fulfils the requirements on space (54x49 mm with a maximum thickness of 16 mm) and on construction materials for its final use in the ALICE experiment. The board has been tested using the complete setup from the front-end electronics to the data concentrator card CARLOSrx: the test of the board was successful both for what concerns data transmission and DCS features. Beside that an FPGA based board has been developed as an emulator of the front-end boards with the purpose of generating known patterns after receiving a trigger signal: this allowed us to obtain the measure of the optical link Bit Error Rate (BER) lower than 10^{-14}. It has clean eye diagram, low bit error rate

and low clock jitter. Up to now 500 boards have been produced and the test of the production is being carried out.

Beside that, the installation of 260 CARLOS end ladder board has started.

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Parallel Session A4

Optical links

Potential Upgrade of the CMS Tracker Analog Readout Optical Links Using Bandwidth Efficient Digital Modulation

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Abstract

The potential application of advanced digital communication schemes in a future upgrade of the CMS Tracker readout optical links is currently being investigated at CERN. We show experimentally that multi-Gbit/s data rates are possible over the current 40 MSamples/s analog optical links by employing techniques similar to those used in ADSL. The concept involves using one or more digitally-modulated sinusoidal carriers in order to make efficient use of the available bandwidth.

I. Introduction

The current CMS Tracker optical links employ analog Pulse Amplitude Modulation (PAM) at 40MS/s. The Signal to Noise Ratio (SNR) of the system is specified so that the link has an equivalent digital resolution of at least 8 bits. Hence, the analog modulation scheme is akin to digital baseband PAM using 256 distinct levels (8 bits) at 40MHz. The equivalent data rate is 320Mbits/s (=8×40MHz).

The next iteration of the CMS Tracker will be operated in the Super LHC (SLHC) environment, and will have to cope with significantly increased data rates due to the tenfold increase in luminosity that is foreseen. In contrast to the telecoms industry where the optical fiber and its installation drive the cost of a transmission system, it is the cost of the optoelectronic components that represents a large fraction of the CMS Tracker electronics budget. The high cost of development of new components able to match the physical and environmental constraints of a high energy physics experiment provides the motivation behind re-using the current link components.

It is proposed to convert these links to a digital system in order to achieve higher data rates using the current analog link components. Additional components on either side of the existing links would be required to perform the necessary digitization, digital transmission and reception. The development can be treated as that of a generic digital communication system, where the medium (or *channel*) over which digitally modulated signals are to be sent is the current CMS Tracker optical link (Figure 1). The main constraints are the bandwidth of the link and available signal power, limited by the transmitter (the Analog OptoHybrid or AOH) [1] and the 12-channel Analog Optoelectronic Receiver (ARx12) [2]. Therefore a bandwidth efficient digital modulation scheme −such as one based on Quadrature Amplitude Modulation (QAM)− is required to achieve transmission at Gbit/s rates. The feasibility of such a conversion must be explored in terms of performance that can be achieved and implementation complexity.

The analytical method to calculating the achievable data rate using QAM in the current Tracker optical links has been detailed in [3]. The previous work was based on simplified assumptions regarding the noise in the optical link, which was presumed to be additive white Gaussian (AWGN) with power spectral density (PSD) derived from the specifications of the readout system. At a bit error rate of 10^{-9}, the achievable data rate was estimated at ~2.3-2.7Gbit/s [3].

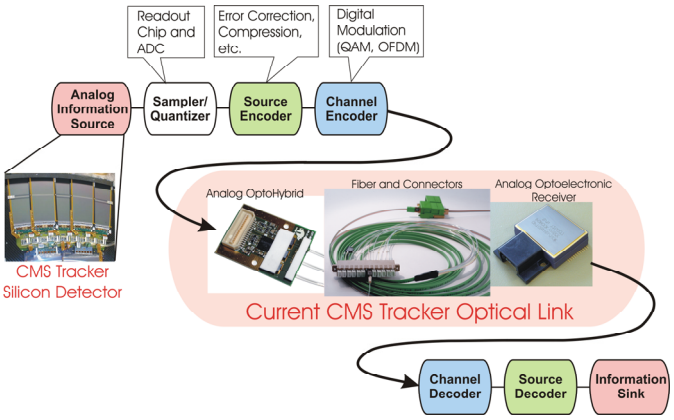

Figure 1: Basic components of a digital communication system based on the current optical link components. The analog channel is the current CMS Tracker optical link. This paper deals only with the Channel Encoder/Decoder blocks.

A future system based on QAM modulation could be implemented using a single carrier, or with multiple carriers as in Orthogonal Frequency Division Multiplexing (OFDM) and Discrete MultiTone (DMT) [4]. While there are practical limitations that will govern this decision, for analytical purposes the two systems can be considered to be equivalent in terms of data rate[1].

Experimental tests are needed, not only to test the validity of the assumptions made previously, but also to demonstrate whether or not the concept is viable and worth pursuing. Given the time constraints and complexity issues, the implementation of a custom-built prototype QAM-based digital communication system is not a realistic option at this early stage of development. Commercial QAM-based modems with such a high throughput do not exist. In order to

[1] This ignores the limitations due to Peak to Average Power Ratio (PAPR) which is normally an order of magnitude higher in a typical OFDM implementation, compared to a single-carrier QAM system. More details on PAPR can be found in [4].

experimentally assess whether such a system is feasible and determine the maximum theoretical data rate, a different approach is necessary.

We consider a multi-carrier (OFDM) system with hundreds of low-symbol rate (1MS/s) QAM carriers covering the entire frequency range of the channel (~500-700MHz). The concept involves a test-setup based on commercial instruments (a signal generator and a spectrum analyzer) capable of QAM modulation/demodulation which can send and receive a single, 1MS/s QAM-modulated carrier through the optical link. If the carrier frequency is swept through the entire frequency range, each carrier of the OFDM system is effectively tested independently (Figure 2). In order to reach useful conclusions, the available transmission power needs to be appropriately allocated to each carrier, taking into account the total power constraint of the channel. Hence a multi-carrier implementation is assessed by the aggregate performance of all single-carrier tests.

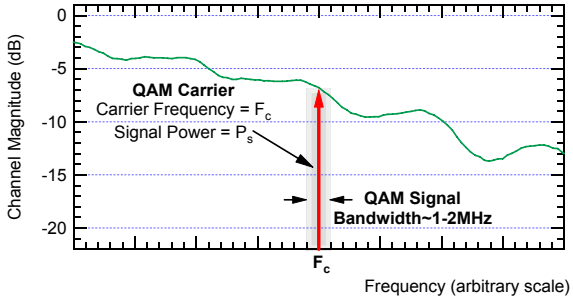

Figure 2: Illustrating a 1MS/s QAM carrier transmitted through a channel with an arbitrary frequency response. The carrier frequency, F_c, can be varied across the entire frequency of the channel.

II. Testing Digital Communication Systems

A. QAM Signal Generation

Combined amplitude and phase modulation is achieved by simultaneously impressing two separate *k*-bit symbols on two quadrature sinusoidal carriers (Figure 3). Each branch in Figure 3 is essentially the amplitude modulation (PAM) of the corresponding carrier.

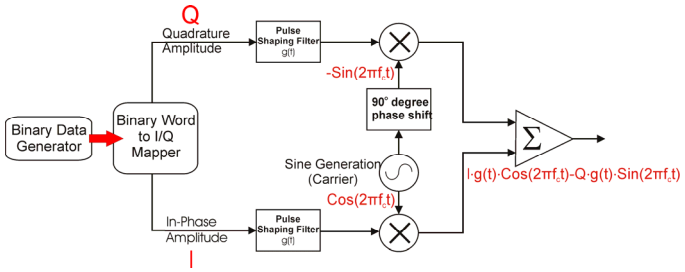

Figure 3: Illustrating QAM signal generation.

A symbol consisting of 2*k* binary bits is clocked in to the I/Q mapper at the required symbol rate. Half of the bits are translated to a quadrature amplitude, *Q*, and half to an in-phase amplitude, *I*. After pulse shaping, these are modulated on the sin and cos carriers respectively, and summed at the output. The resulting signal waveforms are:

$$s(t) = \mathrm{Re}\left[(I + jQ)g(t)e^{j2\pi f_c t}\right] \quad for\ 0 \le t \le T$$
$$= I \cdot g(t)\cos(2\pi f_c t) - Q \cdot g(t)\sin(2\pi f_c t) \qquad (4)$$

g(t) is the signal pulse and I and Q are the information-bearing signal amplitudes of the quadrature carriers.

B. Assessing System Performance

A basic explanation of the underlying concepts behind the experimental tests is required to aid understanding of the subsequent sections. The aim of the laboratory tests is to determine the number of bits/symbol that can be allocated to each QAM carrier [3] in a hypothetical multi-carrier system, for a given target error rate and transmission power.

While a direct BER test is the best way of evaluating a system's performance, it requires fairly complex hardware and can be very time-consuming when the target BER is low. As a guideline, for a target BER of 10^{-9}, $3 \cdot 10^9$ bits need to be transmitted through the link with no errors for a 95% confidence level in the result. The tests to be carried out will involve individual, low symbol rate carriers. For example, a 1MS/s carrier with 5bits/symbol transmits 5Mbits/s, requiring 10 minutes to complete the test for an error rate of 10^{-9}. This is unacceptably slow, given that the tests will involve sweeping the carrier frequency, input power and bit assignment, hence requiring hundreds of individual BER tests. A more practical approach is described next.

C. Error Vector Magnitude

Error Vector Magnitude (EVM) is a modulation quality metric widely used in digital RF communications [5]. It is sensitive to any impairments that affect the amplitude or phase of a demodulated signal. The error vector is defined as the vector difference between the reference signal (i.e. the ideal constellation points) and the measured (demodulated) signal in the IQ plane[2] (Figure 4). EVM is the root mean square (rms) error vector over time, and is usually normalized, to the *average* symbol magnitude of the respective QAM constellation. By convention, it is expressed as a percentage:

$$\mathrm{EVM} = \frac{\text{Error Vector (rms)}}{\text{Average QAM Signal Amplitude}} \cdot 100\% \qquad (1)$$

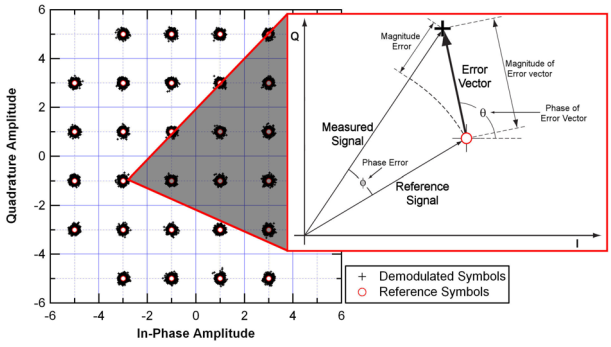

Figure 4: Error vector and related quantities. The IQ plot shows 40 000 demodulated symbols belonging to a 32-QAM constellation. The EVM is ~3.9% in this case, corresponding to an SNR of 28.2dB.

[2] An IQ plot is a useful way of representing demodulated QAM signals. The in-phase Vs quadrature amplitudes of the QAM signal are plotted. More details on this can be found in [3, 4].

EVM can be related to the digital Signal to Noise Ratio (SNR) by:

$$\mathrm{EVM} = \frac{1}{\sqrt{\mathrm{SNR}}} \qquad (2)$$

D. *Symbol Error Rate from EVM*

It has been shown how the SNR in a QAM digital communication system can be derived from an EVM measurement. The significance of this is that SNR can be used to relate EVM to the error rate. For a system corrupted by Additive White Gaussian Noise (AWGN) the symbol error rate[3] (SER) in QAM is given by [6]:

$$SER \approx 2erfc\left(\sqrt{\frac{3 \cdot SNR}{2 \cdot (2^b - 1)}}\right) \qquad (3)$$

Where erfc is the complementary error function and b the number of bits per symbol (e.g. 4 for 16-QAM).

Equation (3) is graphically depicted in Figure 5 for various modulation schemes, where the probability of error is plotted against SNR. Figure 6 shows the corresponding relationship with EVM.

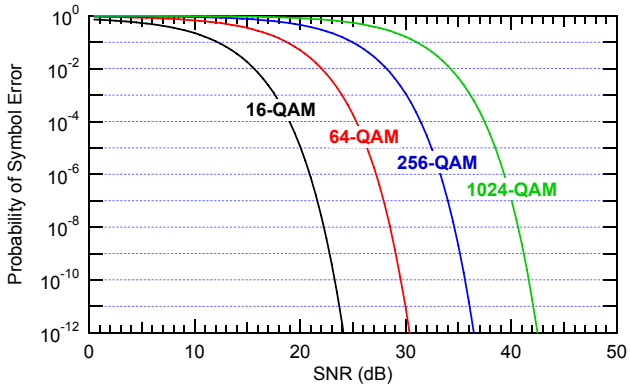

Figure 5: Probability of symbol error in QAM as a function of SNR.

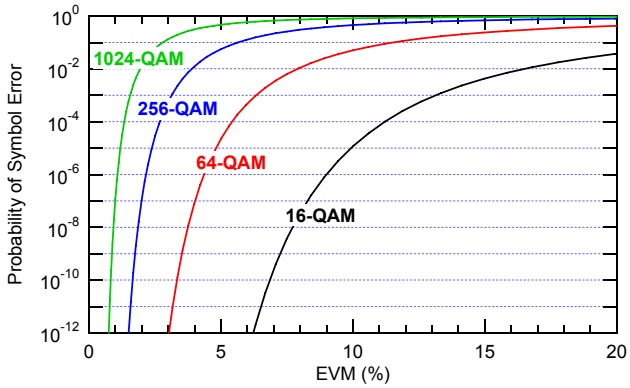

Figure 6: Probability of symbol error in QAM as a function of EVM.

[3] The relationship between bit error rate (BER) and SER depends on the bit-mapping and the QAM constellation. The BER is upper bounded by the SER multiplied by the number of bits/symbol, *b*. For rectangular Gray-encoded QAM constellations where the SER>>1, $\mathrm{BER} \approx \mathrm{SER}/b$. This discussion is beyond the scope of this paper, and we will limit ourselves to using the SER.

The advantages of using EVM measurements to estimate the error rate, rather than a direct BER test, are that of speed and lower complexity. There is no need to decode the demodulated symbols. EVM can be accurately estimated using only a few thousand symbols, in contrast to a BER test that requires sending and receiving a large number of bits to allow an accurate calculation.

III. Laboratory Tests

A. *Objectives*

The aim of the tests described in this paper is to determine, experimentally, the data rate achievable using bandwidth efficient digital modulation in a link based on the current optical link components. To achieve this, it is necessary to determine the number of bits/symbol that can be allocated to each of the QAM carriers across the entire frequency range of the link, given the total available transmission power and the target error rate. Since it is the SNR of a QAM carrier that determines the number of bits/symbol that can be allocated to it (for a given target error rate), it follows that the SNR as a function of carrier frequency and transmission power is all the information needed to calculate the data rate.

B. *Test Setup*

An Agilent ESG E4438C vector signal generator [7] was used as a modulator, while an Agilent PSA 4440A spectrum analyzer [8] demodulated the received QAM signals. The optical link consisted of production versions of the AOH and ARx12. One AOH channel's fiber pigtail was mated to one of the connectors on a 12-channel MU/MPO12 patch cord, with the MPO connector mated to the ARx12. The AOH requires a differential input, while the signal generator has a 50Ω single-ended RF output. An interface based on the high-bandwidth AD8351 differential driver was therefore employed. On the receiving end, the spectrum analyzer was operated in ac-coupled input mode, receiving the single-ended output from the ARx12 directly. 50Ω coaxial cables with type-N and BNC connectors were used for the electrical connections between the instruments and components. A Mac computer running Labview and equipped with GPIB provided control for the AOH and ARx12, with an Agilent 34970A switch used to select the appropriate settings on the optical receiver. Finally, a GPIB-equipped PC was used for communication with the signal generator and spectrum analyzer. The test setup is shown schematically in Figure 7.

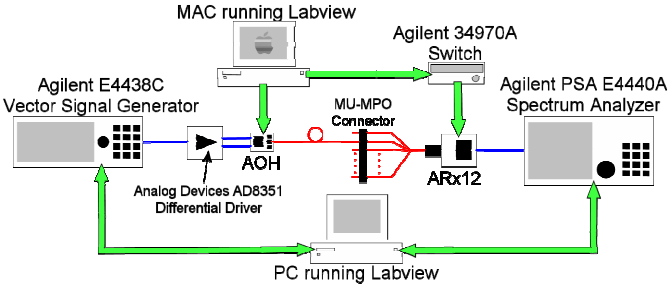

Figure 7: Showing the test setup used. Control and data acquisition (indicated by the arrows) was performed using GPIB-equipped computers.

C. Method

Five different modulation schemes were used in the tests: 4, 16, 32, 64 and 256-QAM. The modulated carrier was swept in frequency (20MHz to 1000MHz, in 20MHz steps) and input power[4] (0dBm to ~ -50dBm), for each modulation scheme (Figure 8). The symbol rate was kept at a constant 1MS/s, and root Nyquist pulse shaping with a filter alpha of 1 was used at the transmitter and the receiver. The internal baseband generator of the vector signal generator was set to produce a pseudo-random bit pattern which was then used to modulate the carrier. For every point in frequency and power, the average EVM and SNR was calculated over 2 000 received symbols.

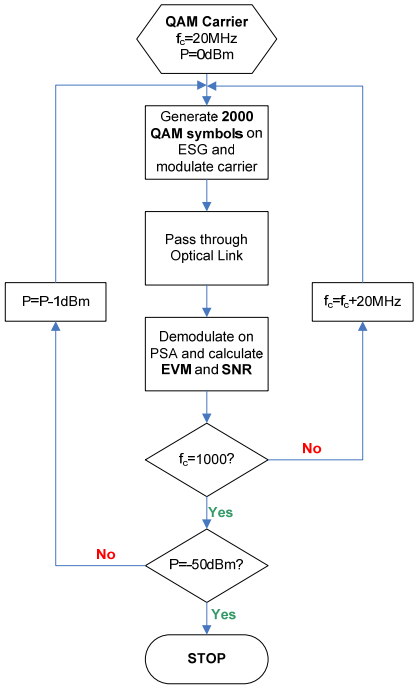

Figure 8: QAM test flowchart, showing the procedure followed for each modulation scheme (4-QAM, 16-QAM, 32-QAM, 64-QAM, 256-QAM).

D. Results

1) Noise

If the SNR and error rate of a given QAM carrier are to be calculated from the EVM, it is important to determine whether or not the noise in the test system is indeed Gaussian (since equations (2) and (3) are only valid for AWGN channels). Several IQ plots were taken at various frequencies and input powers. The results obtained were similar for every case where there was no amplifier saturation in the link. A typical case is presented in this section.

A 32-QAM signal with a symbol rate of 1MS/s and a carrier frequency of 40MHz was passed through the link (see Figure 4 for the noisy, received constellation). 40 000 symbols were retrieved by the spectrum analyzer. In order to obtain maximum statistics on the noise, the received IQ points were amplitude normalized relative to their ideal symbol points and merged into one. Moreover, in the subsequent tests, the EVM calculated is an average over all received symbols, not one particular constellation point. Hence, studying the noise in this way is consistent with the test method.

A 2-dimensional histogram of the received (noisy) points is shown in Figure 9. The projections of the in-phase and quadrature components of the histogram are clearly Gaussian, and hence the EVM can be used to obtain the SNR (and error rate) in a QAM system, with a high degree of accuracy.

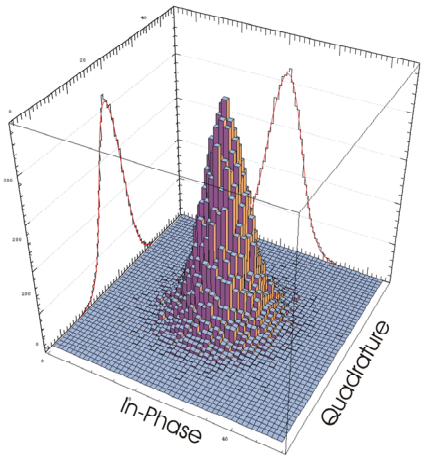

Figure 9: 3-D representation of the 2-D histogram of the 40 000 received IQ points. Projections of the 1-D in-phase and quadrature histograms are also shown.

2) SNR Vs Carrier Frequency

The same test procedure (Figure 8) was followed for all modulation schemes (4, 16, 32, 64 and 256-QAM). Hence, for a range of input powers, plots of SNR Vs carrier frequency were obtained. The results were combined into one graph by averaging the SNRs obtained at each frequency and for each modulation scheme (Figure 10). By sweeping the frequency and input power, the parameter space of the two quantities which are needed for the link's capacity calculation have been fully explored. The error bars in Figure 10 denote the standard deviation of the SNR values. The results were quite consistent across all modulation schemes, giving confidence in the test method [9].

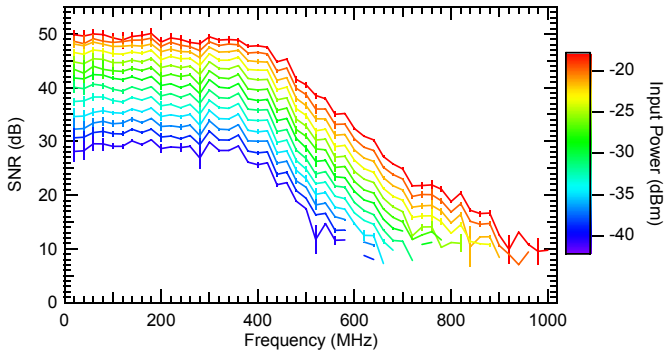

Figure 10: SNR Vs frequency for a carrier of symbol rate 1MS/s, for several input powers. The plots were obtained by averaging the results from all tests (4, 16, 32, 64, 256-QAM).

[4] The input power stated in this paper is that reported by the signal generator, and is not necessarily equal to the electrical transmission power injected at the input of the optical link. The two quantities are, however, proportional.

IV. Achievable Data Rate

In the previous section, the SNR Vs center frequency of a QAM carrier was calculated for a range input powers. This gives all the information required to calculate the data rate of a QAM-based system over the optical link. The analytical method described in [3, 9] is used for the calculation. It should be noted that the amount of transmission power available for such a system is implementation-specific. Therefore, the data rate is calculated as a function of normalized transmission power[5], for various target error rates, and is shown in Figure 11. The shaded area indicates the likely operating range of a future QAM system (whether single or multi-carrier), leading to predicted data rates of 3.5-4.0 Gbit/s for a target symbol error rate of 10^{-9}.

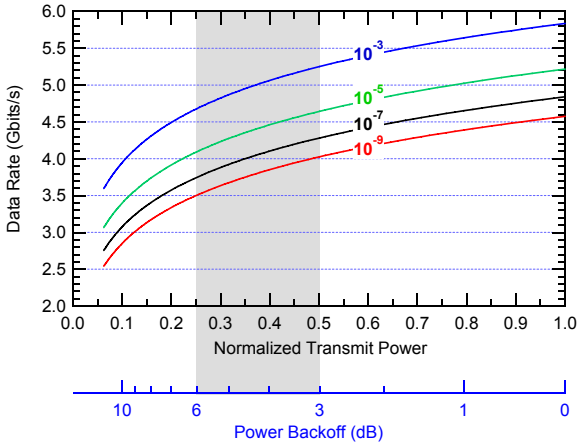

Figure 11: Data rate as a function of transmission power, for various target error rates.

V. Conclusions

It has been demonstrated experimentally that ~3.5-4.0Gbit/s at an error rate of 10^{-9} can be achieved using uncoded QAM-based digital modulation over the CMS Tracker analog optical links. Compared to the data rate of 2.3-2.7Gbit/s calculated in the analytical approach followed in [3], the results are much more optimistic. The main reason for this is that the assumptions made previously turned out to be highly conservative. The noise specification of the link was used in the calculation, and assumed to be additive white. Furthermore, the system was assumed to be a frequency selective channel with a constant noise source at the output. This is clearly an over-simplified approach, which greatly affected the SNR calculation. Finally, due to the better than expected SNR, the available channel bandwidth was larger by about 150-200MHz, with a corresponding increase in overall data rate.

Whether the estimated data rate will be enough for a future CMS Tracker operating in the SLHC environment remains to be seen. Factors such as implementation complexity, power consumption, and detector data volume will all drive any future decision.

A QAM-based system with such performance would be unprecedented in commercial applications, meaning a future implementation would consist of proprietary hardware. This represents a departure from the conventional approach for high energy physics (HEP) applications, where industrial trends drive component and system design choices. Consequently, more effort is required for research and development, and the component costs will certainly be higher than less complex, commercially available optical systems are capable of over 10Gbit/s, and may present a more cost-effective solution.

A QAM modulator would require high speed digital signal processing and digital to analog conversion in the front-end. The power consumption of such devices may be prohibitively large for the context of a HEP experiment.

Despite the drawbacks, the proposed scheme would have the advantage of re-using an existing system, hence preserving the investment in components as well as in non-material costs (e.g. research and development, quality assurance, production testing, installation, etc.).

VI. Acknowledgements

The authors are grateful to Jean-Jacques Gratier and Agilent Technologies for kindly lending us the instruments needed to complete these tests, and for their technical support. We also thank Christophe Sigaud for his help with the interfacing required in the test setup.

VII. References

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[5] Or equivalently, this can be expressed as power 'backoff' from the maximum signal power allowed by the linearity of the optical link.

Integration of CMS Tracker Optical Links

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Abstract

The world's largest point-to-point optical link system is being developed at CERN for readout and control of the CMS Tracker. The optical links are currently being integrated into the Tracker sub-detector systems and preparations are underway for final cabling and connection of the Tracker in CMS at LHC Point 5. Development was recently completed on the dense, in-line optical patch-panel in addition to the back-end patch-panel. Quality assurance and quality control procedures related to cabling and connections, acceptance tests, and tests of final system performance have been defined and practiced. The recent experience during sub-detector integration and the CMS Magnet Test Cosmic Challenge is described.

I. Introduction

The installation of the largest and densest fibre optic system in any of the LHC applications is now underway. 41000 analogue optical links and 3000 digital optical links will be used for readout and control of the CMS Silicon Strip Tracker system[1,2]. These two systems are illustrated together schematically in Fig. 1.

Both sets of optical links are based on commercial off-the-shelf parts including 1310nm edge-emitting lasers, InGaAs photodiodes and single-mode fibre-optic cables with standard connectors in custom in-line and back-end patch-panels. The active components are integrated onto compact optohybrids at the front-end and into VME (FED and FEC)[1] cards at the back-end. The cabling includes single-fibre, 12-way ribbon and 8x12 multi-ribbon cables going from the front-end to the back-end respectively. All parts inside CMS have been qualified for reliability and radiation hardness[2]. Each optical link is typically 65m long, spanning between the Tracker in the CMS experimental cavern (UXC55) and the counting room in the adjacent cavern (USC55) at LHC Point 5, as in Fig. 2. There are three patch-panels for the fibre connections: one at the front-end, close to the optohybrids, a second very dense, in-line patch-panel just within the CMS magnet coil, and the final connection point at the back-end racks.

Production of all of the optical link parts is now complete[3], including 5-10% spares across the whole system. Many parts have been already distributed and integration of the front-end parts in particular is nearing completion. The remaining work involves mainly the installation of in-line and back-end patch-panels, then cabling and connections and commissioning of the full system. In the following sections we will describe the experience gained so far during subdetector integration, the CMS Magnet Test/Cosmic Challenge (MTCC), and future plans for the final integration of optical links in CMS at Point 5.

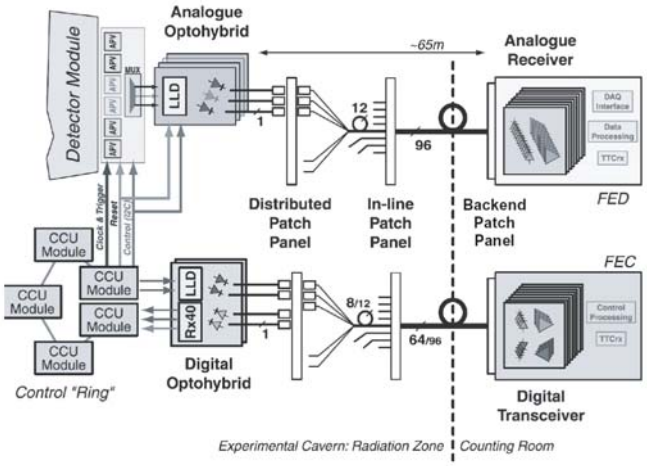

Figure 1: Analogue (uppermost) and digital (lowermost) optical link systems for readout and control of the CMS Tracker.

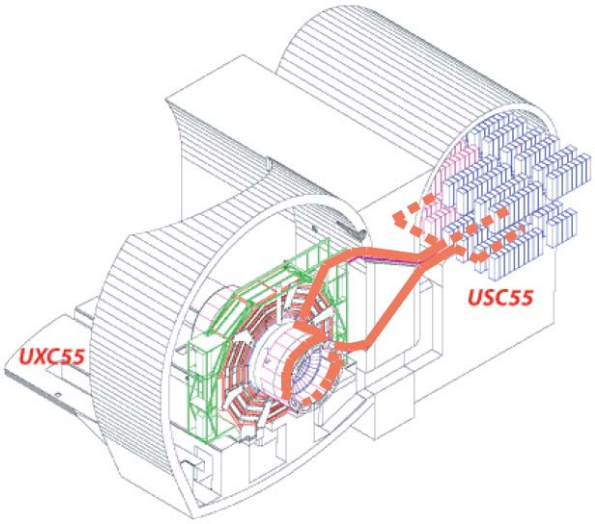

Figure 2: Examples of Tracker optical link cable paths between PP1 sectors on the CMS central barrel wheel (YB0) in the experimental cavern (UXC55) and the back-end racks in the service cavern (USC55) at LHC Point 5.

II. Sub-detector integration activity

Analogue and digital optohybrids have been installed in the sub-detectors very close to the silicon detector modules. i.e. the 'strings' in the Inner Barrel/Inner Disks (TIB/TID), 'rods' in the Outer Barrel (TOB), and 'petals' in the Endcap (TEC). The fibres have then been routed carefully to the edge of the given support-structure (e.g. barrel layer or disk) where the distributed patch-panel is located. The optohybrids have

been manufactured with a spectrum of fibre lengths to match the intended routing in cases where the path lengths were calculable in advance, e.g. in TOB and TEC there are 35-120cm fibre pigtails. TIB/TID fibre route lengths were, in contrast, not calculated in advance and all TIB/TID optohybrids were made with 2m long fibre pigtails. The slack management has since presented a difficult and lengthy challenge for TIB/TID subdetector integration, requiring very careful routing of the slack fibre on the mechanical structures.

Tests have been made in all subdetectors to check that the installed optohybrids function correctly. A commissioning procedure was prepared for the optical links that uses the output, in particular the synchronization pulses (known as 'ticks'), from the front-end microstrip detector APV[1] readout chips to drive a known-size signal into a given optical link. The optical output is then collected using a fibre ribbon cable, or multi-ribbon cable, connected to either a purpose-built DAQ system or a small slice of the final CMS Tracker DAQ. Fig. 3 shows an example of an analysis of analogue optohybrid performance, in terms of measured APV tick-size for different laser driver gain settings. These data were from burn-in tests of the TIB. The data matches very well the expected gain distribution of the optical link[4], also illustrated in Fig. 3. This was also the case in integration tests in the other Tracker sub-systems. Optohybrid channels with gain outside the expected ranges[4] were identified and investigated. This occurred typically in ~1% of channels, always with lower than expected gain. In these cases, the optical connections were re-cleaned and the gains re-measured. Re-cleaning the connectors resulted in proper functionality in almost all cases, except where a fibre had been broken during installation.

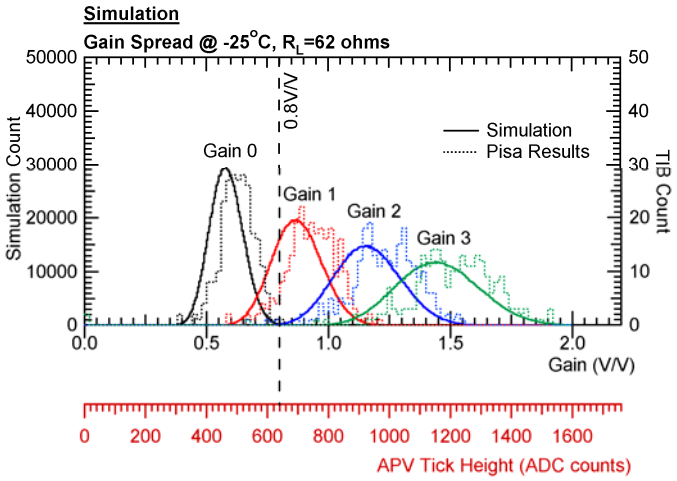

Figure 3: Optical link output for analogue optohybrids having different laser driver gain settings. Data is from TIB/Pisa burn-in tests. Also shown is the simulated link performance based on production test data for the various optical link sub-components[4].

Tests have also been made, for example during TIB/TID integration, to check the optical ribbon fanout continuity after installation (but before connection). This was done usually by illuminating the 12-channel MFS connector with a multiple red-LED light source (that makes no physical contact with the optical fibres) and checking for emergent red-light at the distributed patch-panel. The sMU-MU connection there between ribbon fanout and optohybrid was then made after the MU-connectors were all cleaned with a reel cleaner. The sMU connectors however were only cleaned if the ribbon had been used previously or if it was suspected that the connection was dirty or faulty, based on the results of a measurement. Following connection of the fanout/ribbon to the optohybrids, the performance of the optical link was checked again, usually with a slice of the DAQ system, as with the tests done earlier for the optohybrids only.

The ribbon installers also check that the installed cable will indeed reach PP1. This is done by checking the position of a mark made on the cable jacket at the position that represents the minimum length outside the TIB/TID structure required to reach PP1. Then the ribbons are grouped into bundles which match the prescribed connection at PP1, where groups of up to 8 ribbons are mated with the 96 channel (8x12) multi-ribbon cables. Spare ribbons have also been foreseen, either as reserve stock to use to replace those broken during installation, or ribbons to be installed as 'dark-fibre' alongside the nominally used ribbons, for use only if needed later to re-route a damaged channel where the ribbon cannot be physically removed and replaced.

The integration of the front-end parts has taken more time than expected in the sub-detector community. This was mainly due to the fragile nature of the parts, the number and density of channels, and the number of tests made to prove that all channels were working before moving to the next integration step. There have been very few accidents and breakages. Only 70 optohybrids out of almost 17000 installed optohybrids and 50 out of 3000 ribbon-fanouts have been damaged during installation. Damage and breakages occurred mainly due to mishandling during the early phases of installation. The integration centres were visited one or more times by the optical link team to discuss installation procedures and minimize the risk of damage. So far, all damaged optohybrids have been replaced with spares. The same applies to broken ribbons/fanouts except for some in the TOB and TEC which could not be easily removed and replaced. In this case the ribbons were repaired by cutting off the damaged end and fusion splicing a new ribbon pigtail.

III. CABLING AND CONNECTIONS AT P5

A. *PP1 development*

There has been significant effort recently on the final definition of the CMS Tracker PP1 patch-panels in the 2x16 phi-sectors around the inner edge of the CMS magnet cryostat. For the optical links, PP1 houses the in-line patch-panel, where the connections are made between the ribbon fanouts coming from the Tracker and the multi-ribbon cables coming from the service cavern USC55. In each sector the in-line patch-panel consists of a box of volume 600x90x150 (length x width x height, all in mm) containing 4 partially removable cassettes.

A prototype cassette is shown in Fig. 4 in the 'open' position, with the full complement of 5 multi-ribbon cables and 40 ribbons attached. The 4 cassettes can therefore manage up to 20 multi-ribbon cables per sector, i.e. 160 ribbons, or 1920 fibre channels.

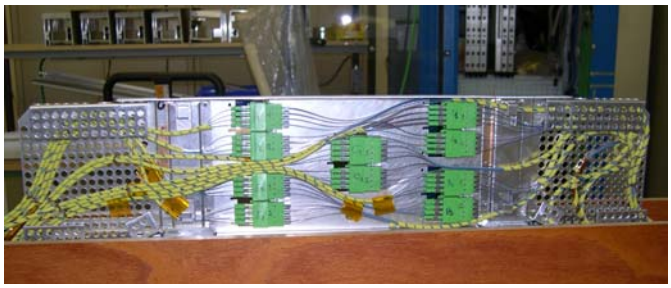

Figure 4: Prototype PP1 in-line patch-panel cassette (in 'open' position) complete with full complement of 40 ribbons (from the left) and 5 multi-ribbon cables (from the right) connected at 5 MFS connector blocks mounted in the centre of the cassettes.

The optical connector at PP1 is a variant of the MFS 12-way ribbon connector from Diamond, who also supply the in-line patch-panel, following developments in partnership with CMS. It is worth noting that the density of optical fibre is so high in the cassettes that the ends of the optical ribbons cannot protected by cable sheath (over 80cm in the case of the ribbon cables, and 60cm for the multi-ribbon cables).

The overall PP1 housing beyond the in-line patch-panel cassette volume also includes some storage space for excess lengths of ribbon-cable at either end of the cassettes as well as strain relief elements for the multiribbon cables, about 10cm away from the cassettes.

Several in-line patch-panel prototypes have been produced by Diamond and tested at CERN. One was used successfully in the CMS MTCC. Delivery of all the final cassettes will be in October 2006.

B. Trunk-cabling (pre-cabling of YB0)

Preparations are under way for the optical cabling in CMS at Point 5, which will occur over several months after the CMS central barrel wheel YB0 has been lowered into UXC55 in 2007. The final trunk cabling involves laying and fixing of approximately 560 multi-ribbon cables on YB0 from the in-line patch panel (PP1) to the racks in the service cavern (USC55). A detailed cabling procedure, outlined below, has been developed and practiced in the MTCC.

The trunk cable connections between frontend (PP1) and backend patch-panels (at FED or FEC crates) follow a pre-defined map and route, which was proposed already in some detail several years ago, and was recently frozen. This map, in combination with work of CMS Integration group on routing the cables, allowed the lengths of cable to be defined so that the appropriate spectrum of cable lengths could be manufactured pre-terminated. As with the optohybrid pigtails and ribbon/fanouts it was considered impractical to connectorize so many multi-ribbon cables on-site. This choice therefore required careful planning of the spectrum of lengths to be produced, which ranges between 45 and 65m in 5m bins. At least 5m of slack is planned for each cable path and there are in addition ~10% spare cables available.

The optical trunk cables for the Tracker will be probably installed last during the pre-cabling phase of the YB0. The precise cabling order has not yet been decided but it is expected to be done one sector at a time with two teams, one cabling YB0+ and the other YB0-.

For a given PP1 sector, the appropriate selection of cables will be made from the inventory according to the number and lengths of cables prescribed in the cabling map for that sector. The cables will have protection elements attached, covering the naked optical ribbon sections at each end, allowing safe handling by the cabling crew. It is expected that each cable will be associated to a specific final path and have a CMS (INB) label attached just before installation. The cable 2-D barcode (QR code) will be scanned and then associated with the CMS/INB code in our cable map and inventory.

The actual installation of optical cables will probably be made one-cable at a time, starting from the balcony nearest the passage between USC55 and UXC55 (recall Fig. 2). The end with MFS termination will be threaded along the intended path to PP1 where it will be fixed in a strain relief at the appropriate position. The cable will then be fixed in the correct position in cable trays all the way back to the balcony. The other end of the cable, with MPO termination can then be pulled through the passage to USC55, where it will be routed towards the intended destination rack along pre-defined cable tray routes in USC55. All of the remaining cable length will be pulled through from UXC55 to USC55 with the slack being taken up, in most cases, in the 1.8m tall false floor beneath the rack, wound on a special figure-8 shaped support. This winding technique allows the ribbon stack inside the trunk cable sheath to relax, avoiding the stress and strain that would occur if the ribbons were wound on a simple circular spool. The position of some racks, e.g. those over a void in the false floor, precludes this slack storage solution beneath the rack and it is expected that the slack on these cables will be stored instead either nearby the rack in the false floor, or on the cavern wall in UXC55.

The time to lay a cable from PP1 to back-end patch-panel is expected to be 1 hour, so the total time required is approximately 600 hours divided by the number of teams working in parallel, e.g. cabling both sides of YB0. In addition to a 4-5 man CMS cabling crew that lays/pulls/fixes the cables (which is likely to be the same team that laid the electrical cables), a large team of trained people from the Tracker is required: 2 people to prepare, label and handover the cables to the cabling team and 2 people at each PP1 and then 2 people at the back-end patch-panels ready to receive the cable-ends, i.e. up to 8 Tracker personnel per shift.

At PP1, the tracker personnel remove the protection on the naked ribbon end of the cable and then mount the MFS connector block in the correct PP1 cassette and slot. This operation normally requires only a few minutes per cable, so it should be possible to carry out this task before the next cable arrives. It is intended that the cables are laid in an order that reflects the most efficient manner of stacking and attaching the cables at PP1. The order of trunk cabling should fill one cassette at a time, in an order, e.g. slot 1 through 5 in the cassette, which will allow the fastest and easiest installation of the naked ribbon cables and management of the naked ribbon slack length inside each cassette. This step has been practiced in the lab and the routing of slack ribbons in a cassette can be seen in Fig. 4 (where multi-ribbon cables enter on the right hand side as viewed).

C. *Tracker cabling at Point 5*

After the pre-cabling of YB0 is completed, the Tracker can be lowered and installed inside CMS at Point 5. Before transport to Point 5, the ribbon pigtails and connectors from the Tracker will have been stored on the 'nose-cones', which are substantial mechanical frames at each end of the Tracker support tube that are used for Tracker insertion.

One immediate aim, after the Tracker is lowered and inserted into CMS, will be to clear the nose-cones quickly of both optical and electrical cables, in order that the beam-pipe can be installed without undue delay. The optical ribbons will be laid in cable channels in each sector from the Tracker periphery up to the PP1 patch-panels. Once the ribbons arrive at PP1, the optical connections will be made to the multi-ribbon cables. Note that after pre-cabling of YB0, when the in-line patch-panels are installed and filled with MFS blocks from the multi-ribbon cables, there will be no other space available to store temporarily Tracker ribbons during beam-pipe installation, so the final optical connections have to be made.

Before connection at PP1 every ribbon connector in the bundle will be cleaned with an appropriate fibre-cleaning tool, and checked using a special inspection microscope if time permits. There will be human-readable labels on the MFS adapters that the fanouts are attached to, and the barcode on at least one ribbon in a given bundle (up to 8 ribbons) will be scanned in order to lookup and validate the optical connection. The final list of connections made will be uploaded later to CMS Tracker and CMS databases.

There exists a potentially difficult issue of slack management at the in-line patch-panel. A large amount of slack can be absorbed easily in the cassettes, e.g. up to 50cm is stored already for the trunk cables as shown in Fig. 4, but this slack has to be common to the whole ribbon bundle. A problem arises with the ribbons coming from the Tracker, where there could be a variation of up to 10cm between individual ribbons in the same 8-ribbon bundle. This mismatch of slack length cannot be accommodated inside the in-line patch-panel cassettes. The solution has therefore been to leave some space available between the end of the Tracker cable channel and the in-line patch-panel cassettes, approximately 170mm long x 150mm deep x 90mm wide. The mismatch in ribbon slack can be stored here and the remaining pigtail lengths equalized before the ribbon bundles enter the cassettes. Arranging that the mismatch in slack lengths is confined to this space will be a very delicate operation, however it should become easier with accumulated experience.

These final stages of Tracker cabling and connections were all practiced on a small scale (33 ribbons in one cable channel) in the MTCC. It is foreseen to practice in the Tracker PP1/cable-channel mock-up in Q4 2006, using a maximally occupied channel having 140 optical ribbons.

A first estimate of manpower for Tracker ribbon cabling and connection has been made, based on our experience in the MTCC. It is expected that a trained 4 person team is needed per PP1 sector, 2 people to lay the fibre bundles into the cable channel and 2 to make the routing, connection and slack management at PP1. Connecting 40 ribbons to a single in-line patch-panel cassette requires approximately 2 hours if the ribbon bundles have been well prepared. This suggests that 1 sector (out of 32 in total) can be cabled per 8-hour shift per team. Given the likely time-pressure, very careful preparation work at the Tracker Integration Facility (TIF) will be required to ensure that the ribbons for a given sector are already divided into appropriately labelled bundles, making their installation into the cable channels and subsequent connection at PP1 as easy and as fast as possible. It is expected that this preparatory work in the TIF will also require the effort of several people for a period of several weeks. The precise arrangement of the fibres on the nose-cones is currently being discussed and will be decided after practicing with the Tracker PP1/cable-channel mock-up at CERN.

IV. TESTS OF CABLING AND CONNECTIONS

Extensive QC (acceptance) tests of the final cabling and connections are foreseen. These include visual inspection of the cabling, connections, cable/connector barcode validation, plus measurement of the optical link performance in terms of light-loss in the cables and connectors.

Again, time-pressure is expected and these tests of the cables and connectors will have to be done in parallel with the installation. As the cables require a lot of time to install it is expected that the additional time required for acceptance tests might not be significant, and it should fall conveniently into the shadow of the installation work, as long as sufficient manpower is available.

If a break in a cable is suspected during installation, it can be checked with either a simple light-source/camera inspection tool (for a basic test of the trunk cables only) or using a specialized instrument such as an optical time domain reflectometer (OTDR). As well as detecting broken optical fibre channels or poorly mated optical connections, an OTDR also provides a very precise measurement of the cable lengths in the system, which is needed later for the synchronization of the Tracker[5].

It is planned that a high resolution OTDR will be used for final acceptance of the pre-cabling of YB0 and then again later for testing the full optical link system, in particular the connections made at PP1. These will remain accessible for some time before LHC start-up and suspect connections can be cleaned and re-mated if necessary. The measurement setup is illustrated in Fig. 6, which shows how a full link will be measured, 12 channels (1 ribbon) at a time, using the OTDR and a customized optical splitter. The splitter has staggered lengths on the different outputs which allow the reflected signals on the 12 fibre channels to be separated while being measured simulataneously.

If the cable is unbroken and correctly connected at PP1 a trace such as that shown in Fig. 6 is expected. Here there are strong peaks in the trace resulting from reflections at the ends of the fibres just in front of the laser diodes. The lengths of the different optical links can be calculated based on these signals and the known lengths of the launch cables and the different splitter arms. The precision is around 10cm, i.e. sub-nanosecond uncertainty when feeding these data later into the Tracker synchronization procedure[5].

However, if there are additional peaks in the OTDR trace, for example at the expected PP1 position, or at a point within the ribbon fanout length, and in particular if the peaks normally associated with the laser are missing, these will indicate problems either at the PP1 connection or in the front-end section of fibre. In case of difficulty or uncertainty in interpretation the OTDR traces, the 12-channels in question can be flagged and re-measured using a similar setup, but with an optical switch instead of the splitter, so that the ribbon is measured one fibre channel at a time.

In case of problems, there are a variety of solutions available. If there is a broken ribbon or multi-ribbon cable between PP1 and USC55, the optical links can be re-routed through a spare cable, as there will be one spare multi-ribbon cable available per sector, plus some of the other multi-ribbon cables also contain unused ribbons that could be exploited. Suspect connections at PP1 can be re-inspected, re-cleaned, re-mated and re-tested until either fixed or confirmed as being faulty. Breaks in ribbons in the cable channels between PP1 and the Tracker might also still be repairable depending upon time/access available for a spliced repair. In contrast problems suspected to be close to or inside the Tracker volume will be irreparable and these will only be flagged for reference, to be re-checked once the Tracker sector in question is powered.

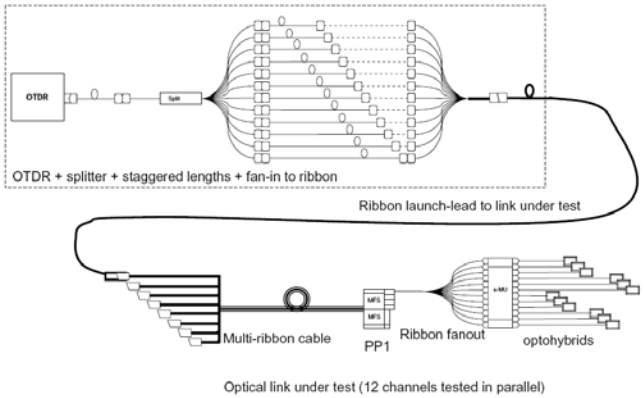

Figure 5: OTDR setup with splitter and optical link under test. The splitter allows measurement of 12 channels (sharing the same ribbon) at once and the staggered lengths allow differentiation between the separate fibre channels.

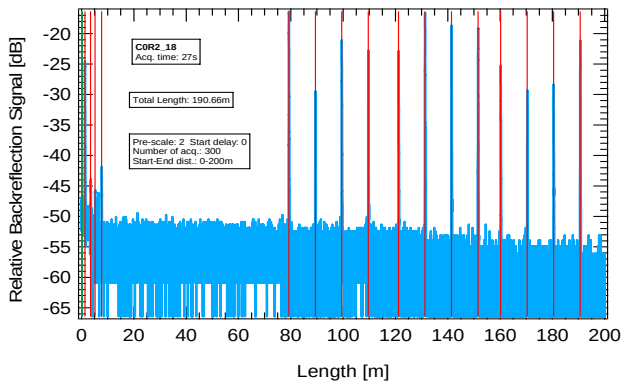

Figure 6: Typical OTDR trace for 12-channels of fully connected optical link measured with the setup shown in Fig 5. The vertical lines on the right hand side indicate peaks from reflections at the 12 lasers. Lines/peaks at the left hand side are from launch connections.

V. Conclusion

There has been excellent progress so far in integrating the optical links into the CMS Tracker. The various subdetectors are close to completion, very few problems have occurred in the optical cabling and connections and the links function very well. A significant effort is now underway to install a large quantity of optical links (~12000 fibre channels) in the TIF at CERN for the remaining tests on the Tracker before it is ready for transport to Point 5.

For the final optical link integration steps of pre-cabling of YB0 and then cabling and connection of the Tracker after insertion into CMS, all the preparations are also well underway. A cabling procedure has been written and practiced in the CMS MTCC for YB0 pre-cabling of the multi-ribbon cables, and for cabling and connection of the Tracker optical ribbons. The resources required have been estimated for cabling/connection activities at Point 5. Finally, an extensive array of test tools and procedures is now in place, including a sophisticated OTDR cable/connection tester.

Acknowledgements

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The HELEN Latin-American exchange programme is acknowledged for providing support to Pedro Pedesta and Isabel Pedraza.

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Bandwidths of Micro Twisted-Pair Cables and Fusion Spliced SIMM-GRIN Fiber and Radiation Hardness of PIN/VCSEL Arrays

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Abstract

We study the feasibility of fabricating an optical link for the SLHC ATLAS silicon tracker based on the current pixel optical link architecture. The electrical signals between the current pixel modules and the optical modules are transmitted via micro-twisted cables. The optical signals between the optical modules and the data acquisition system are transmitted via rad-hard SIMM fibers spliced to rad-tolerant GRIN fibers. The link has several nice features. We have measured the bandwidths of the transmission lines and the results indicate that the micro twisted-pair cables can transmit signals up to ~ 1 Gb/s and the fusion spliced fiber ribbon can transmit signals up to ~ 2 Gb/s. We have irradiated PIN and VCSEL arrays with 24 GeV protons and find at least one candidate PIN and one VCSEL array that can survive to the SLHC dosage.

I. Introduction

The SLHC is designed to increase the luminosity of the LHC by a factor of ten to 10^{35} $cm^{-2}s^{-1}$. Accordingly, the radiation level at the detector is expected to increase by a similar factor. The increased data rate and radiation level will pose new challenges for a tracker situated close to the interaction region. The present optical link [1] of the ATLAS pixel detector [2] is mounted on a patch panel instead of directly on a pixel module. This separation greatly reduces the radiation level at the optical modules (opto-boards) and simplifies the design and production of both the pixel modules and opto-boards. Data communication between the separated modules is achieved by transmitting electrical signals using ~ 1 m of micro twisted-pair cables. The optical signals between each opto-board and the off-detector optical electronics are then transmitted via 8 m of rad-hard/low bandwidth SIMM fiber ribbon fusion spliced to 70 m of rad-tolerant/medium bandwidth GRIN fiber ribbon. The optical signals are generated and sent using the PIN and VCSEL arrays, respectively. We currently transmit optical signals at 80 Mb/s and expect to transmit signals at 1 Gb/s for the SLHC. If the present architecture can transmit signals at the higher speed, the constraint of requiring no extra service space is automatically satisfied.

We have started an R&D program to study the feasibility of an upgrade based on the optical link architecture of the current pixel detector while taking advantage of the several years of R&D effort and production experience. In this paper, we present results on the bandwidth measurement of micro twisted-pair cables and a fusion spliced SIMM/GRIN fiber ribbon and the radiation hardness of PIN and VCSEL arrays.

II. Bandwidth of Micro Twisted-Pair Cables

Commercial copper cables [3] can transmit several Gb/s over tens of meters. However, the diameters of these cables are too large for the pixel detector. The present pixel optical link uses a micro twisted-pair of wires for transmission of low voltage differential signals (LVDS) between a pixel module and the driver and receiver chips on an opto-board. Each pair of wires is twisted 5 turns per inch (TPI) which corresponds to 2 turns per cm. For barrel pixel detectors, each wire is aluminium with a diameter of 100 μm (38 AWG) plus 25 μm of insulation, for an outer diameter of 150 μm. The length of the twisted pairs varies from 81 to 142 cm. The wires for the endcap pixel detector are finer, 60 μm with 12 μm of insulation. The length of these copper twisted pairs is ~80 cm. The impedance of the twisted pairs is ~ 75 Ω.

We have measured the bandwidths of micro twisted-pairs of various lengths, diameters, and numbers of turns per inch. The cables tested include [4]:

- 38 AWG (100 μm core plus 25 μm of insulation): 5 TPI with 75 Ω termination.
- 36 AWG (127 μm core plus 9 μm of insulation): 5 TPI with 75 Ω termination and 10 TPI with 100 Ω termination.

For the bandwidth study, we transmitted LVDS pseudo-random data in the selected cable and measured the signal characteristics at the termination with a LeCroy WaveMASTER 8600A (6 GHz) oscilloscope and differential probe (7.5 GHz). The rise and fall times of the cables are shown in Figs. 1 and 2. The current barrel cable has the fastest rise and fall times.

The eye diagrams produced by transmitting pseudo-random data of 650 Mb/s and 1 Gb/s in the current barrel cable are shown in Fig. 3. The masks shown are adapted from Fig. 39-5 and Table 39-4 of the Gigabit Ethernet Specification (IEEE Standard 802.3) with the mask voltage levels modified to match the LVDS receiver chip used. From these figures, it is evident that the micro-twisted cable is adequate for transmitting signals at 640 Mb/s and that transmission at 1 Gb/s might be acceptable.

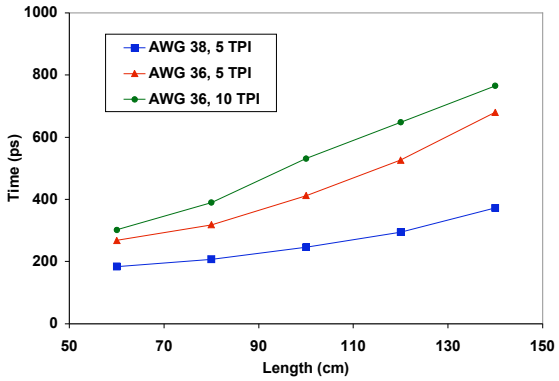

Figure 1: The rise times (20-80%) of the micro twisted-pairs vs. wire length for wires of various diameters and TPI.

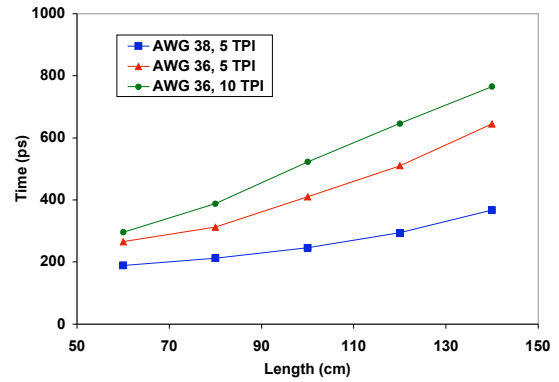

Figure 2: The fall times (20-80%) of the micro twisted-pairs vs. wire length for wires of various diameters and TPI.

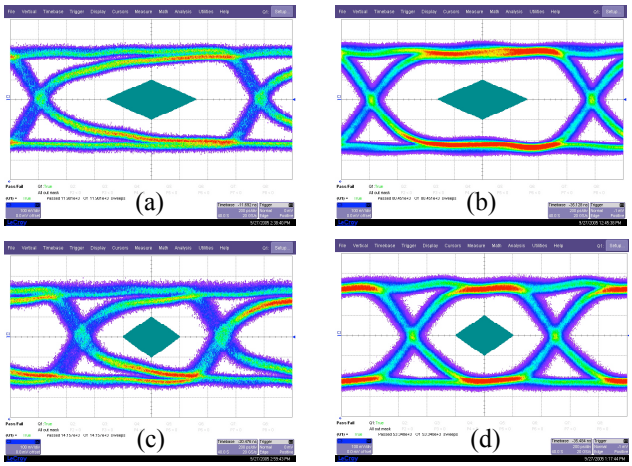

Figure 3: Eye diagrams for signals of (a) 650 Mb/s and (c) 1 Gb/s in a barrel cable of 1.4 m. (b,d) show the corresponding signals for a cable of 0.8 m.

III. Bandwidth of Fusion Spliced SIMM/GRIN Fiber

There are three kinds of commercial fibers available with each having different bandwidths. Single mode fiber has a core diameter of less than 10 μm, no modal dispersion, and hence the highest bandwidth. The other two fibers, GRIN and SIMM, are multi-mode fibers with core diameters of 50 or 62.5 μm. The former has medium bandwidth and is radiation tolerant. The latter has lower bandwidth with a radiation-hard pure silica core. Each pixel optical link of the present pixel detector has 8 m of 50 μm SIMM fiber ribbon fusion spliced to 70 m of 62.5 μm GRIN fiber ribbon.

We have measured the bandwidth of 8 m of 50 μm SIMM fiber fusion spliced to 80 m of 62.5 μm GRIN fiber. The optical signal was generated with an 850 nm VCSEL, contained within a Finisar FTRJ-8519-1-2.5 fiber optic transceiver, and measured using the above oscilloscope with a 4.5 GHz optical to electrical converter. Resultant eye diagrams for pseudo-random signals of 650 Mb/s and 1 Gb/s are shown in Fig. 4. The mask shown is adapted from Fig. 38-2 of the Gigabit Ethernet Specification (IEEE Standard 802.3) and in accordance with the specification, a fourth-order Bessel-Thomson software filter is used to view the signals. To represent the waveform more accurately we choose a higher bandwidth than recommended for the filter: 1.5 Gb/s instead of 487.5 (750) Mb/s for the 650 Mb/s (1 Gb/s) transmission. It is evident from these results that the fiber can adequately transmit signals up to at least 1 Gb/s and hence the transmission bandwidth of the wire link will be the limiting factor in the present pixel detector transmission lines.

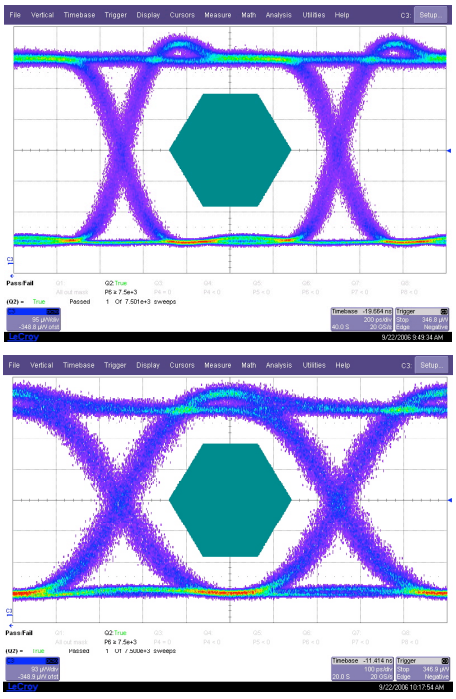

Figure 4: Eye diagrams for optical signals of (a) 1 and (b) 2 Gb/s in a fusion spliced SIMM/GRIN fiber.

IV. Radiation Hardness of PIN and VCSEL Arrays

We use the Non Ionizing Energy Loss (NIEL) scaling hypothesis to estimate the SLHC fluences [5-7] at the present pixel optical link location (PP0). The estimate is based on the assumption that the main radiation effect is bulk damage in the VCSEL and PIN with the displacement of atoms. After five years of operation at the SLHC, we expect the silicon

component (PIN) to be exposed to a maximum total fluence of 2.5 x 10^{15} 1-MeV n_{eq}/cm^2 [8]. The corresponding fluence for a GaAs component (VCSEL) is 1.4 x 10^{16} 1-MeV n_{eq}/cm^2. We study the response of the optical link to a high dose of 24 GeV protons. The expected equivalent fluences at LHC are 4.3 and 2.7 x 10^{15} p/cm^2, respectively. For simplicity, we present the results from the irradiations with dosage expressed in Mrad using the conversion factor, 1 Mrad = 3.75 x 10^{13} p/cm^2. The expected dosages are therefore 114 and 71 Mrad, respectively.

We irradiated four opto-boards with PIN and VCSEL arrays from various vendors using 24 GeV protons at CERN. Each board was instrumented with one silicon PIN array and a pair of GaAs VCSEL arrays. The PIN arrays were all fabricated by one vendor, Truelight, and the VCSEL arrays were fabricated by three vendors, Optowell, Advanced Optical Components (AOC), and ULM Photonics (two varieties, 5 and 10 Gb/s). On the opto-boards, each of the PIN and VCSEL arrays coupled to radiation-hard ASICs produced for the current pixel optical link, the DORIC (Digital Opto Receiver Integrated Circuit) and VDC (VCSEL Driver Chip). Furthermore, the opto-boards were mounted on a shuttle system which enabled us to easily move in and out of the beam for annealing of the VCSEL arrays.

We characterized the arrays before the irradiation. Figure 5 shows the LIV (Light-Current-Voltage) curves of the VCSEL arrays. All arrays produced large optical power, in excess of 1 mW for the VCSEL current of 7 mA, the rated maximum current of the ULM 10 Gb/s array. This latter array also required higher voltage, ~ 2.3 V, to produce this current. The 5 Gb/s array required somewhat lower voltage to produce this current and the arrays from the AOC and Optowell, required significantly lower voltage. The latter arrays are therefore more suitable for operation at the SLHC because we expect to fabricate the driver and receiver chips using the 0.13 μm process with a thick oxide option which has a maximum operating voltage of 2.5 V. Given that it requires ~ 0.2 V to operate the transistors in the driver chip, the maximum drive current in the ULM arrays is therefore ~ 7 mA. This implies a lower optical power and less efficient annealing of arrays with radiation damage.

The test system monitored various parameters of the opto-boards throughout the irradiation. Of particular interest was the optical power of the VCSEL arrays vs. dosage as shown in Fig. 5. The power decreased during the irradiation as expected. We annealed the arrays by moving the opto-boards out of the beam and passing the maximum allowable current (up to 20 mA per channel) through the arrays for several hours each day. The optical power increased during the annealing. However, there was insufficient time for a complete annealing. Consequently both the A.O.C. and ULM 5 Gb/s arrays had no optical power at ~50 Mrad. The ULM 10 Gb/s arrays continued to have optical power of more than 100 μW up to 65 Mrad and the Optowell arrays survived up to at least 70 Mrad, the SLHC dosage. We believe that more arrays would have survived if we had more time for annealing.

The silicon PIN arrays survived the irradiation quite well. After the full SLHC dosage, the responsivities decreased to ~35% of the pre-irradiation level as shown in Fig. 6.

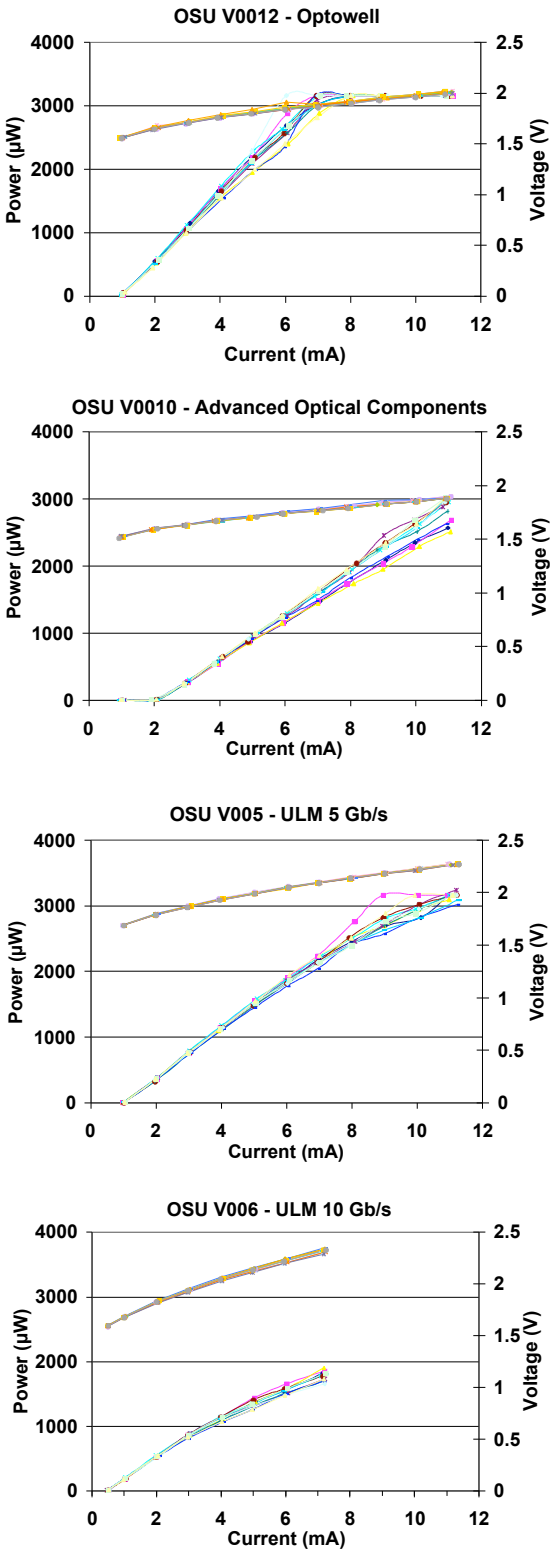

Figure 5: LIV curves of the four VCSEL arrays before irradiation.

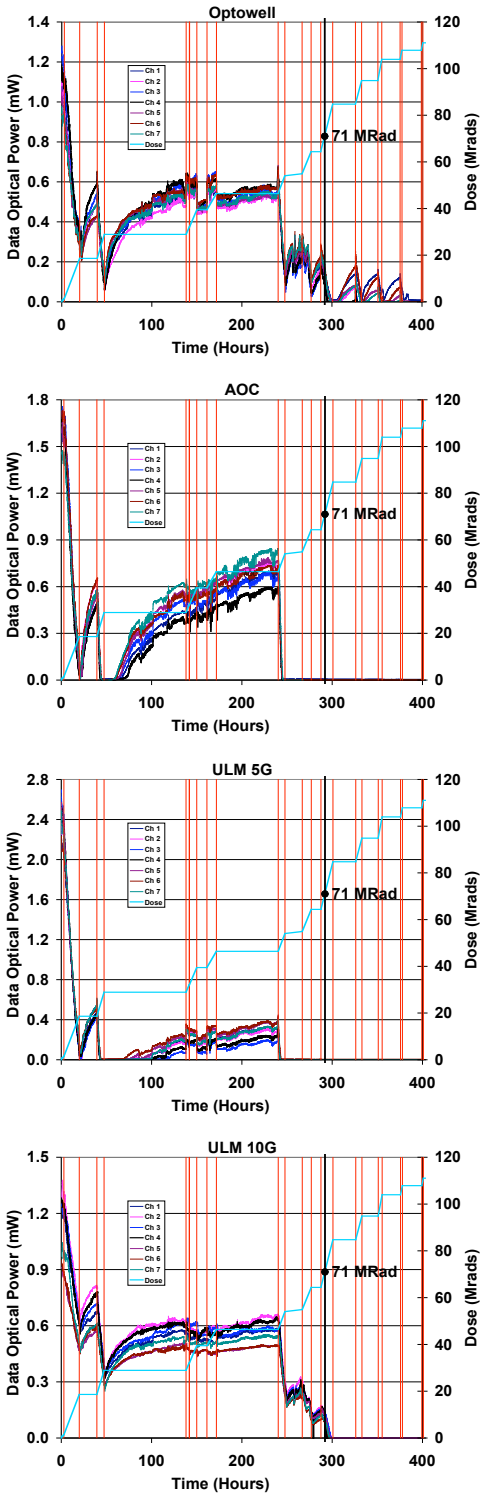

Figure 6: Optical power as a function of time (dosage) for the four VCSEL arrays that transmitted data to the control room. The power decreased during the irradiation but increased during the annealing as expected.

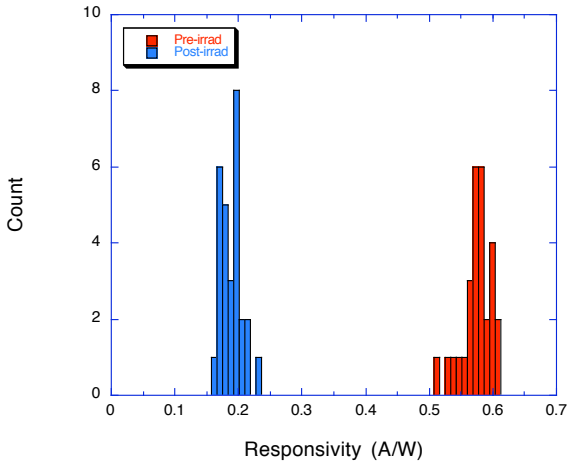

Figure 7: Responsivities of the four PIN arrays before (blue) and after (red) irradiation.

V. Summary

We have studied the bandwidth of the electrical and optical transmission lines of the current optical link of the ATLAS pixel detector. The results indicate that the micro twisted-pair cables can transmit signals up to 1 Gb/s and the fusion spliced fiber ribbon can transmit signals up to 2 Gb/s. A silicon PIN and GaAs VCSEL array candidate have been identified to have radiation hardness suitable for the SLHC operation. The current infrastructure can therefore be used for the SLHC as a possible upgrade scenario.

VI. Acknowledgement

This work was supported in part by the U.S. Department of Energy under contract No. DE-FG-02-91ER-40690.

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Parallel Session A5

DAQ and Optical technology

A multi-channel optical plug-in module for gigabit data reception

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Abstract

A plug-in module has been built for reception of optically transmitted data by gigabit applications. The optical receiving module is based on a 12-channel optical receiver and an FPGA with embedded high-speed deserializers. It is compatible with the serializer ASIC used by many LHC systems. Due to its compact design, several of these modules could be plugged into VME readout systems. This module will be the principle element for both the CMS Preshower data concentrator card and the TOTEM front-end driver.

I. Introduction

The CMS Preshower [1] sub-detector comprises 4288 silicon sensors, each containing 32 strips. The data transport from the on-detector system is achieved by 1208 optical links running at 800Mbps. This enormous resulting data flow of ~1Tbps necessitates the reduction of the data volume. Indeed, given the expected maximum average strip occupancy of ~2%, a significant data reduction is feasible.

For the readout of the Preshower, a VME-based system able to acquire on-detector data from a number of optical fibres, perform the appropriate on-line data reduction algorithms and pass the concentrated data to the CMS event builder is required.

Recent studies [2] have shown that the requirements of the Preshower for on-line data reduction cannot be met by existing readout hardware designed for use by other CMS sub-detectors.

Hence, the need for the development of a CMS Preshower data concentrator card coincided with a need for a readout system (but with different requirements) for the TOTEM experiment [3]. This gave birth to the idea of a modular VME-based readout system, common to both systems allowing selection of which constituent modules are to be used, depending on the requirements of each system.

The 12-channel optical plug-in module for gigabit data reception (OptoRx-12) presented in this manuscript is the principle element for both readout systems.

II. Implementation

The optical receiving module is based on a 12-channel optical receiver and an FPGA with embedded gigabit deserializers. Figure 1 shows a photograph of the module.

The 12-channel digital optical receiver (NGK's POR10M12SFP [4]) used is the one specified for the CMS ECAL optical links and it is qualified for data rates up to 1.25Gbps. The 1310nm optical receiver uses a "Multi-fiber Push On" (MPO) connector for the interconnection of the 12-fibre ribbon.



Figure 1: Photograph of the OptoRx-12.

The FPGA used belongs to the Altera's Stratix GX family [5] that incorporates embedded hardware deserializers with data rate up to ~3.2Gbps. The FPGA deserializers provide built-in functions compatible with the Gigabit Ethernet (8b/10b encoding) [6] protocol. This feature of the FPGA is very important since this encoding scheme is used by the GOL [7] serializer ASIC that drives the optical links of both the Preshower and TOTEM front-end systems. It is worth mentioning that tests have shown[1] that the deserializers can be configured to be also compatible with the other transmission protocol (G-Link [8]) supported by the GOL ASIC, used by other LHC systems.

The module is compatible with two FPGA devices (1SGX25FF1020 & 1SGX40GF1020) from the Stratix GX family, allowing the selection of the appropriate device depending on the logic resources required for each application. Table 1 summarizes the features of the two compatible FPGA devices. One of the most important features of these FPGA devices is the way the dedicated memory resources are fragmented, allowing the instantiation of a large number of individual memory blocks. This feature plays an essential role for on-line multi-channel data processing applications and it was the decisive factor for selecting this FPGA family [9]. For this decision, important role also played the previous experience with FPGA devices from the same family, where a testbench [10] was based on.

[1] Extensive tests have been carried out for the possible use of the module as a part of the Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector. Although the module has been configured successfully as a 12-channel G-Link receiver, it cannot be used for this project since its deserialization latency is greater than the trigger system can tolerate [11].

Table 1: FPGA comparison

FEATURES	1SGX25FF1020	1SGX40GF1020
Logic Elements	25,660	41,250
512bit RAM blocks	224	384
4Kbit RAM blocks	138	183
512Kbit RAM blocks	2	4
Total RAM bits	1,944,576	3,423,744
9x9 multipliers	80	112

The module incorporates an electrical interface with 280 single-ended lines connected to the FPGA's I/O pins via 5 PMC connectors. The 64 pins are reserved for controlling the module through a local bus. The remaining pins could even cover the possible requirement of providing all the deserialized data in parallel[2]. Although the total number of interconnections is large, its size was kept relatively small[3], allowing several of these modules to be plugged onto a VME64 board [12]. A JTAG connector for the configuration of the module is also available.

The optical receiving module also provides an optional connector on the bottom side[4], for attaching an S-Link64 [13] transmitter mezzanine card, if required (i.e. for the TOTEM front-end driver). Figure 2 shows a photograph of the module with an S-Link64 transmitter mezzanine card attached to it. In this case, the stacking height of this combination of mezzanine cards exceeds the specified limits for VME cards. Therefore, the VME systems based on this configuration (i.e. the TOTEM front-end driver) will have to occupy two consecutive slots of the VME rack.

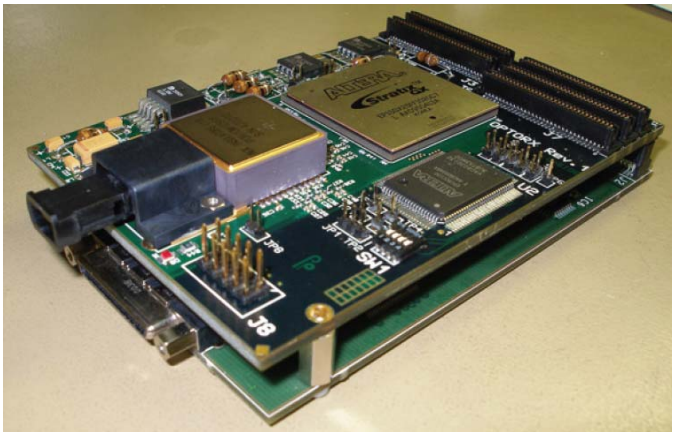

Figure 2: Photograph of the OptoRx-12 with an S-Link64 Transmitther attached to it.

III. EVALUATION

The evaluation of the performance for that kind of equipment is a complicated and time-consuming process, since the most important issue is to examine how frequently an error in the data reception can occur. The required setup for the evaluation of the module incorporates the following:

- A pattern generator able to provide 12 optical serial output streams. The device used is a programmable 12-GOL driver [14] developed by TOTEM. The device incorporates an FPGA that drives independently 12 GOL serializer ASICs. For the purpose of these tests, the device was programmed to generate continuously 12 different sequences of pseudo-random numbers based on linear feedback shift registers (LFSRs) [15]. This device is illustrated in Figure 3.

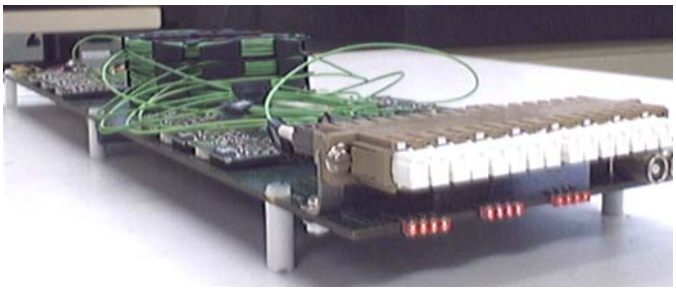

Figure 3: Photograph of the 12-GOH driver used as a pattern generator for the evaluation of the OptoRx-12.

- A variable optical attenuator. The attenuator is introduced in between the 12-GOL driver and the OptoRx-12.
- The plug-in module itself programmed with a special firmware that generates pseudo-random numbers (based on identical algorithms as implemented in the 12-GOL driver) and compares them with the words received from its twelve serial inputs.
- A host board where the module is plugged-in that provides power, clock as well as a USB interface to a personal computer to retrieve the error measurement results from the OptoRx-12. This device is illustrated in Figure 4.
- A PC and associated software.

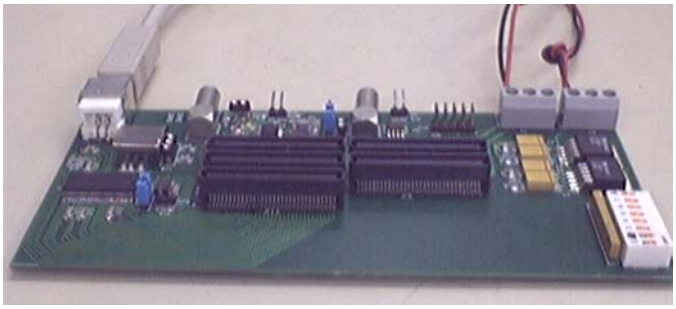

Figure 4: Photograph of the support board that provides power, clock, JTAG and USB interface to the OptoRx-12, used for evaluation purposes.

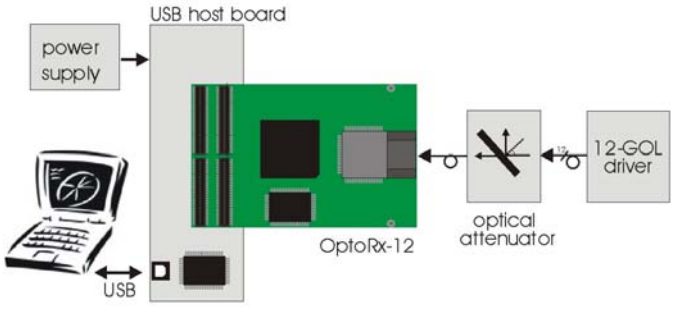

Figure 5: The evaluation setup.

[2] (16bit data + 2bit control) x 12 = 216bit.
[3] Length: 115mm, width: 75mm, height: 14mm (10mm PMC connector stacking height + 2mm PCB thickness + 2mm height of the mechanical components on the bottom side i.e. screws etc).
[4] Top side, when the module is plugged.

A block diagram of the evaluation setup is shown in Figure 5. Error rate measurements were taken using this setup where the optical signal was attenuated gradually. Figure 6 shows a graph with the word error rate vs the optical power, for one of the channels.

The outcome of the measurements (that have lasted about a month) is that the sensitivity of the overall system coincides with that of the digital optical receiver (-19dBm) [4]. Therefore, the additional (to the digital optical receiver) components do not affect the overall performance of the optical receiving module. It is worth mentioning that during the CMS experiment, the operating optical power in the Preshower data concentrator card is expected to be more than two orders of magnitude higher (>-12dBm). Therefore, no errors are expected in this operating range.

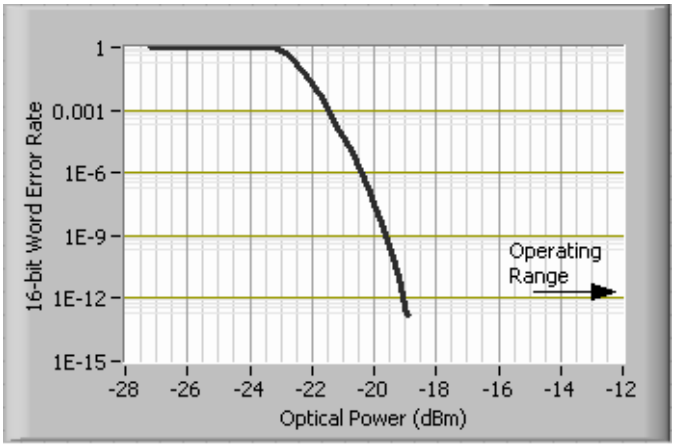

Figure 6: Error Rate vs absolute optical power for one of the input channels of the module. The sensitivity of the overall system coincides with that of the digital optical receiver (-19dBm).

IV. Summary & Conclusions

A plug-in module built for reception of optically transmitted data by gigabit applications has been developed. The optical receiving module incorporates a 12-channel optical receiver and an FPGA with embedded high-speed deserializers.

The module is fully compatible with the serializer ASIC used for high-speed data transmission by many LHC systems. Its compact size allows its use as a mezzanine card plugged into VME-based readout systems.

The performance of the module was extensively tested and its behavior been deemed satisfactory. The fact that the sensitivity of the overall system coincides with that of the digital optical receiver has proven that the additional components of the optical receiving module do not affect the overall performance.

This module will be the principle element for both the CMS Preshower data concentrator card and the TOTEM front-end driver.

Besides forming the basis of the CMS Preshower data concentrator card and the TOTEM front-end driver, it is envisaged that this compact plug-in module will also be useful for the readout of other detector electronics systems, for LHC and beyond.

V. Acknowledgements

The authors would like to thank Georgios Sidiropoulos (from the University of Ioannina, Greece) for his idea of building modular (and thus easily upgradable) readout systems, based on plug-in modules like the one presented in this manuscript.

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PCI Express Over Optical Links for Data Acquisition and Control

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Abstract

PCI Express is a new I/O technology for desktop, mobile, server and communications platforms designed to allow increasing levels of computer system performance. The serial nature of its links and the packet based protocols allows an easy geographical decoupling of a peripheral device. We have investigated the possibility of using an optical physical layer for the PCI Express, and we have built a bus adapter which can bridge remote busses (> 100m) to a single host computer without even the need of a specialized driver, given the legacy PCI compatibility of the PCI Express hardware. This adapter has been made tolerant to harsh environmental conditions, like strong magnetic fields or radiation fluxes, as the data acquisition needs of high energy physics experiments often require.

I. Introduction

The electronics developed for LHC detectors is expected to operate in a intense radiation field. This aspect has to be taken into account also when designing a board that will be located in the periphery of a detector. Concerning the CMS experiment, our practical need is to link the counting room with the VME creates placed on the balcony of the five barrel wheels. The radiation dose absorbed after ten years of operation in this environment is less than 0.2 Gy and the expected neutron fluence is not high enough to generate a relevant bulk damage (less than $2.5 \cdot 10^{10}$ n/cm^2) [1]. Nevertheless the detector electronics could still be fooled or even damaged because of Single Event Effects (SEE).



Figure 1: Block diagram of the hardware setup.

To cover the long distance (about 100 m) between the control room and the detector electronics we chose to manufacture an adapter that translates PCI express signals to/from the optical physical layer (Fig. 1) and which, using commercial bridges, could be fitted into legacy bus standards (PCI, CompactPci, VME). PCI Express is a new local bus generation using existing PCI programming concepts: it represents a radical move from traditional I/O architectures in that it replaces parallel multi-drop busses with serial switched point-to-point links. The link bandwidth is committed to the number of lane (individual serial pairs). Every lane utilizes two LVDS signals at 2.5 Gbit/s per direction so the capacity of the channel after 8b/10b encoding is fixed at 250 MByte/s times the number of lanes [2].

PCI Express adopts a "communication centric" approach: the load-store operations between two nodes are performed exchanging framed packets in accordance to a suite of stacked protocol layers taking care of the physical, link and transaction issues of the channel. In case of PCI Express all these activities are carried out at the hardware level, with no software intervention. Clearly this load-store model logically matches the model of field bus control in which a host and a networked peer node exchange software arranged packets to access memory and registers of the field bus for I/O operation. As the PCI Express base specifications version 1.0a make no assumption about the nature of the interconnection medium, to investigate the PCI Express I/O bus used like a distance communication protocol running on an optical fiber link we addressed a number of research activities in the context of the project LINCO (INFN Gr. V).

II. The New Physical Medium

The first goal of LINCO project is a feasibility study of an optical layer for the PCI Express protocol. The problems raised by the adoption of fiber as physical medium are mainly two: the jitter that, being specified both at the transmitter and the receiver implicitly constrains the in-between medium, and the reference clock distribution.

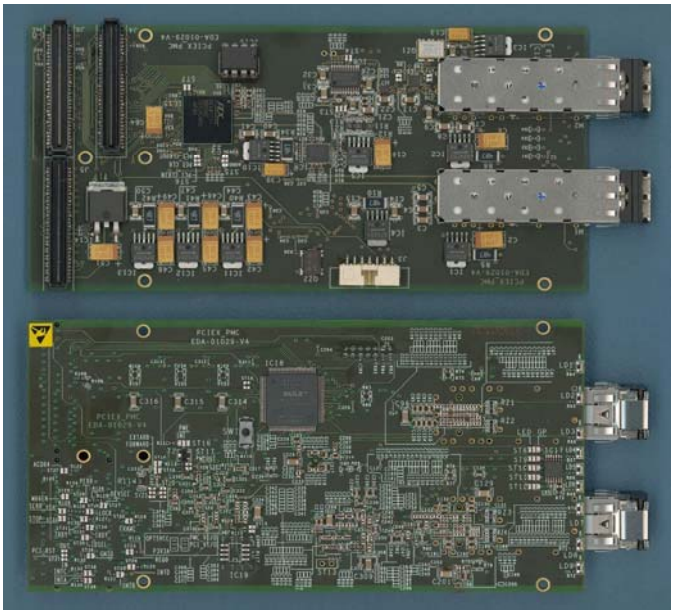

Figure 2: Picture of the board.

The figure of total jitter reserved for the interconnection, as fixed by the specifications, is a maximum of 0.3 Unit

Intervals (UI), e.g. 120 ps of total (random plus deterministic) jitter at a Bit Error Ratio (BER) level of 10^{-12} [3]. This figure refers to the jitter introduced by the chain of transmission side connector, electrical-to-optical conversion, fiber, optical-to-electrical conversion and receiver side connector. To this regard, important design parameters are related to the choice of the transceivers because their contribution to the overall jitter is in the critical path. For this reason we qualified for our application two types of transceivers: an Intel transceiver Infiniband compliant (2.5 Gbit/s) in a multimode fiber and a JDS Uniphase multirate (up to 2.7 Gbit/s) transceiver for OC-48 operation on a 1310 nm single mode fiber.

The other issue to face was designing the reference clock distribution. In fact the PCI Express reference clock (100 MHz) is usually supplied by the host board to the add-in cards but the specifications do not mandate its presence [4]: in principle a local supplied 100 MHZ ± 300 ppm clock should suffice to properly reconstruct the incoming stream. In practice, our tests revealed the need of bridging also the reference clock signal. A frequency offset in the clock generator of the PC host board we used showed that it may be impossible to lock the data signal. For these reasons we deserved a separate optical transmitter and fiber to broadcast the host reference clock.

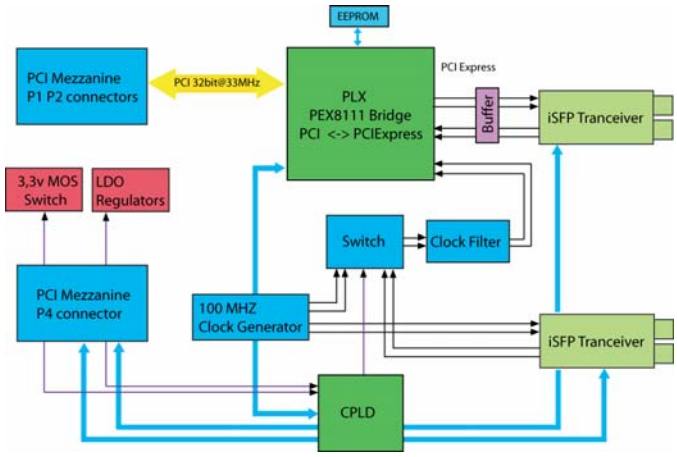

Figure 3: Block diagram of the mezzanine board.

III. Board Description

We chose the Pci Mezzanine Card (PMC) form factor (Fig. 2) in order to meet the two different bus standards the board will be inserted (CompactPCI and VME crate). A key component of the board is a PLX Technologies bridge (PEX 8111) that allows transparent bridging between a PCI bus and a PCI Express x1 lane (Fig 3). This kind of bridge can be configured as a device that can tunnel configuration cycles from the PCI side to the PCI Express channel (in our application when it sits in the control PC) or vice versa (when it is used in the remote VME field bus). Also the clock path is dependent on configuration indeed a Micrel SY58023U high speed switch is used to broadcast either the local generated clean 100MHz clock or the received one, both to the PEX8111 bridge and to the optical transmitter. A PLL with a small loop bandwidth is used to filter the jitter of the reference clock and to provide the proper differential and common mode voltages as per the PCI Express specifications. The presence of the optical transceiver in the data transmission path force us to use a Pericom PI2EQX4401 buffer to comply with the PCI Express receiver detect mechanism. An Altera programmable logic device is connected to the general purpose I/O bus of the PEX8111 and to the gate of a high power MOS switch; the use of this device will be illustrated in the CMS application section.

IV. Board Test

A direct measure of the voltage and timing margins at the entrance and exit of the electrical-optical-electrical chain, taken with an Agilent 54855A 6GHz real-time scope, shows that the contribution of the medium to total jitter is respectively of 4.88 ± 0.21 ps (Fig. 4). In order to measure the eye opening at a 10^{-12} we used the tail fit method [5]. We extracted the jitter's Probability Density Function (PDF) from the histogram of the data Time Interval Error (TIE) i.e. the time difference between the recovered clock (from the data stream) and the data signal. Since the deterministic jitter PDF is bounded below a certain jitter range, all the PDF comprises just random jitter processes. Through a Gaussian fit on these tail regions we extrapolated the PDF analytic function concerning rare events. Fig. 5 gives an illustration on the relationship between jitter PDF and BER that can be considered as the cumulative distribution function, essentially the integral of the PDF function.

From the so-called "bathtub" curve of the BER (showed in Fig. 5), we deduced the real eye opening as the time difference between its branches corresponding to a 10^{-12} BER level. From this extrapolation it turns out that both transceivers are compliant with the minimum eye opening fixed by specifications (183 ps), with the Intel transceiver outperforming the competitor with a measure of 243.69 ± 0.14 ps.

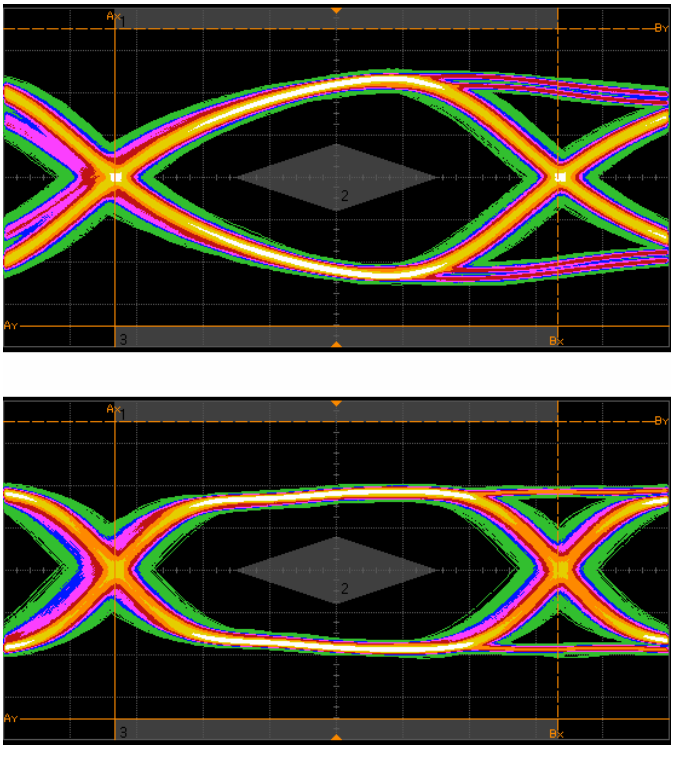

Figure 4: Contribution of the optical medium to signal jitter.

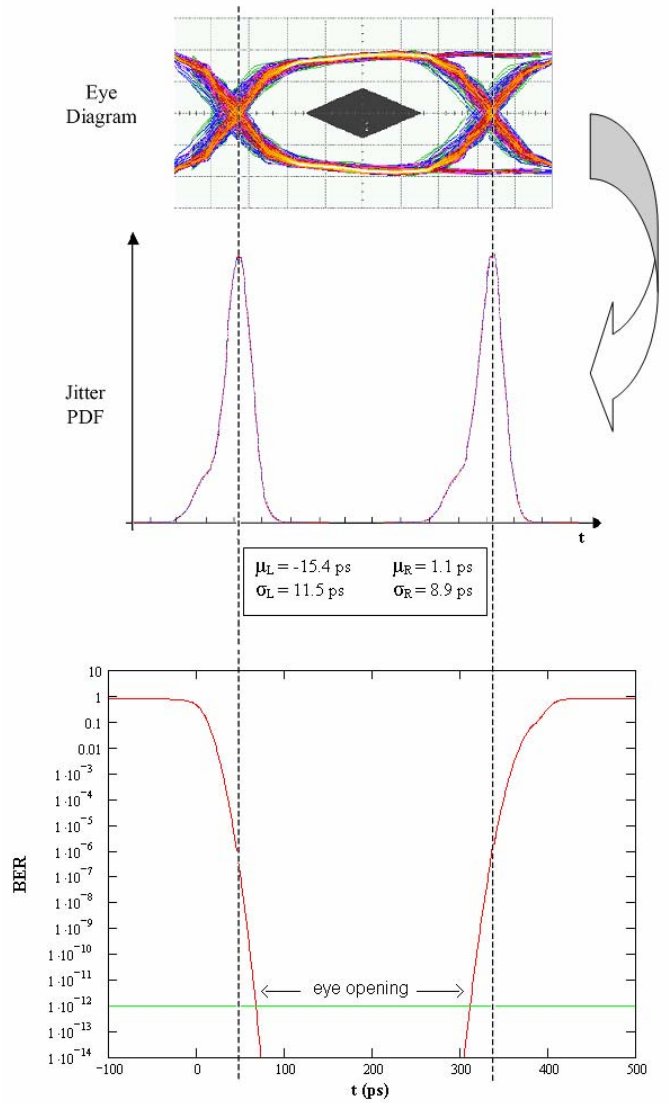

Figure 5: Modeling of Probability Density Function of jitter from measured data.

With the aim of understanding this difference, further tests were done on the data signals [6]. We used a real time individual jitter component separation technique, based on the examination of the TIE trend and its Fourier transform. For the estimation of the two jitter components probability density functions we assumed a dual Dirac delta model [7] that relies on two basic assumptions:

- Random jitter PDF follows a Gaussian distribution (hence fully described by its width σ),
- Deterministic jitter PDF follows a finite distribution formed by two Dirac delta functions separated by the entire amount of deterministic jitter.

The dual Dirac model is a simplistic model for jitter distribution. In fact it fits a real world jitter distribution only in presence of pure duty cycle distortion. In our case we obtained a better representation of the deterministic jitter PDF by deconvolving the PDF of the random jitter from the measured probability density function of total jitter. This method yields a more realistic evaluation of the deterministic jitter with respect to the dual Dirac. The only disparity between transceivers turned out to be the amount of deterministic jitter: the JDS device adds more than 30 ps p-p to this parameter with respect to the Intel one. The reason of this addition has to be charged to increased crosstalk levels due to the faster rise time of the JDS device.

We configured two prototypes: one for local and the other for remote operation. The first has been fit into a host PC, with passive adapter, while the second has been tested in a CompactPCI crate. The two boards were linked by a 100m multimode fiber with Intel transceivers. The BIOS could take control of the remote PCI bus without any driver and we could transfer data at the full legacy PCI throughput. Besides the jitter in the reference clock path has been measured holding a safe 85 ps (Fig. 6). Another test was done using a remote VME crate with an active adapter hosting a Tundra UniverseII PCI to VME bridge. In this case transfers were achieved on a VME target with a 3 to 4μs single access latency.

The only disparity between the PCI Express data signal reshaped at the end of the optical chain and the local one is the loss of the de-emphasis (e.g. a feature that affects a transmitter driving a trace with more then one bit of the same polarity; by lowering the voltage level of 3.5 dB with respect to the first bit it avoids an excessive charge of the parasitic capacitances of the transmission line). The limiting amplifier, which is in the optical chain, nullifies the de-emphasis making the optical interconnection not fully PCI Express compliant.

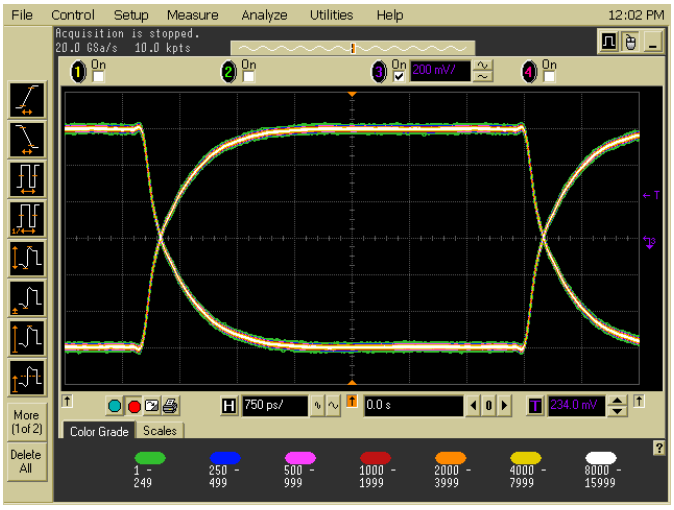

Figure 6: Remote reference clock.

V. CMS Environment

As reported above the operational environment of our PMC board presents harmful conditions. Due to the strong magnetic field (about 1 Tesla at the periphery of the detector [1]) we have been forced to avoid the use of core inductors. Usual LC filters in the power supplies have been replaced with lossy RC filters and the voltage drop associated with them has forced a careful design of the power distribution to the different devices of the board. For these reasons a proper decoupling strategy has been extensively analyzed with a full-wave electromagnetic field simulation software (Ansoft SiWave). The S-parameters of the high speed traces have been extracted from simulations and used in a Hspice program

to predict timing and voltage margins of the PCI Express signal at the input of the optical transceiver.

To qualify our design to Single Event Effects (SEE) we have setup a radiation test at the Paul Scherrer Institute in Zurich with protons of 60 MeV energy. The fluence measured on the board was $5 \cdot 10^{10}$ p/cm^2 and the board has been exposed for 8 hours, corresponding to a total ionizing dose of more than 6 Krad (ten years of LHC operation). In the picture (Fig. 7) you can see our board hosted by a commercial Tundra VME bridge. During the test, these boards were active and a certain number of VME registers were continuously written with random patterns, read back and compared for Single Event Upset checking and logging. Furthermore we checked the absorbed total current in order to verify the occurrence of Single Event Latch-up (SEL) events.

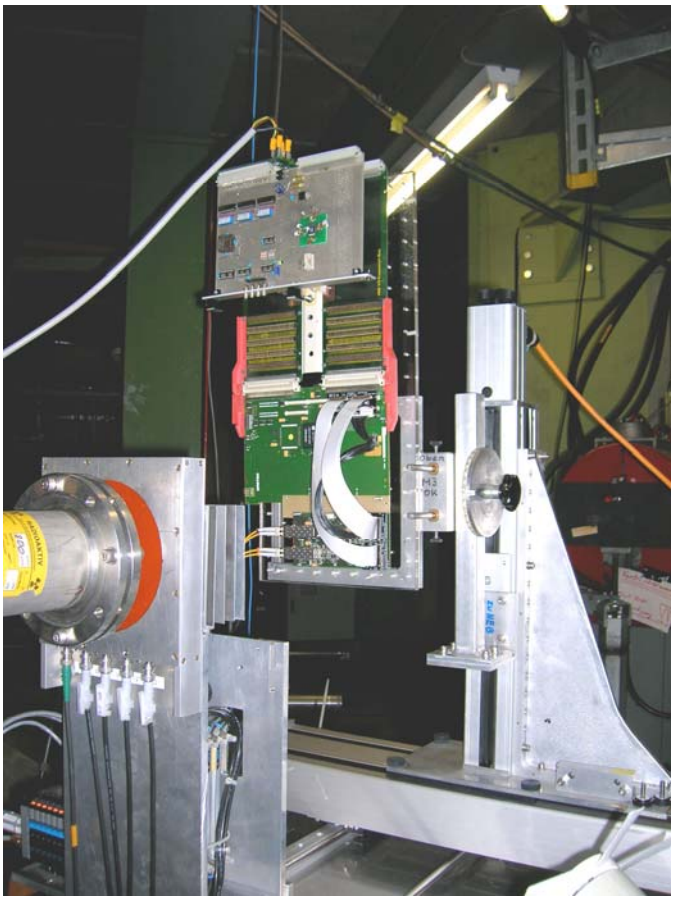

Figure 7: Radiation test setup at PSI.

We didn't observe any SEU, the only relevant effect being the maximum radiation dose absorbed by the Intel transceivers before latching-up. To ease operation at LHC, a watchdog-type mechanism for automatic reset has been put in place using the Altera programmable logic device on the board. The watchdog drives the gate of the high current MOS switch in series with the main power supply of the board and it is continuously reset through the GPIO bus of the PLX bridge. The GPIO bus is in turn periodically toggled by the remote host through the optical link; when a single event functional interrupt (SEFI) occurs on the remote board that stops the communication with the host, the watchdog doesn't get toggled any more and this results in a power off/on cycle, e.g. a cold reset that restores the PCI Express link functionality. Furthermore we continuously monitor the transceivers life parameters, like laser bias current, temperature and optical transmitted and received power, through I^{2}C protocol on GPIO bus.

VI. Conclusions

The implementation of a PMC board has been used both as a proof of concept and a test-bed for measurements of PCI Express compliance. In particular our tests show that the optical transport medium is very effective from the point of view of functionality and a modest jitter difference was found between the signals before and after the optoelectronic chain. Finally the application in the LHC harsh environmental condition doesn't seem to be an issue for our board.

VII. References

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Status of the TTC upgrade

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Abstract

The TTC (Timing, Trigger and Control) system [1] broadcasts the timing signals (Bunch Clocks and Orbits) from the LHC machine to the experiments. Once at the detector level, it integrates the trigger information and local synchronous commands with these signals, for transmission to several thousands of destinations. The equipment for this second part of the system is fully produced, but the main network between the machine and the experiments required to be upgraded to ensure its easy maintenance. The design work began at the end of 2005 and the new modules will be tested during the summer 2006 and the structured test beam in September 2006. A status of this design work is given, including the description of the upgrade principle, the main modules, the results of the tests done on the prototypes and the plans for production and support of this system.

I. Upgrade Principle

As it was before 2005, the system was difficult to maintain for various reasons. The main ones were the following: obsolete components with really few spares (only 2 receiver crates per experiment), no documentation to reproduce the modules (no schematics, no manufacturing files), and no way to remotely monitor, in case of troubles, the status of the transmitter crate to be installed in the CCR (CERN Control Room).
Moreover, the quantity of required signals increased between the time the TTC system was specified and now. Three Bunch Clocks (BCring1, BCring2, BCreference) and two Orbits (Orb1 and Orb2, one per ring) are now required, instead of one pair of Bunch Clock and Orbit signals previously.
Finally, the last argument justifying a redesign of the TTC backbone was that no piquet service was foreseen for a 24 hours a day, 7/7 days on-call support of such a vital system. Such a piquet service is really rare and only the AB/RF team was willing to do it, provided that we use equipment they already support.

A. Criteria

A study was thus made [2] to allow a reasonable upgrade of the system, with the following criteria as a basis:

- Full compatibility with the experiment trigger systems, which use the outputs of the previous TTCmi receiver crate,
- Equal or better jitter performances than the previous system,
- Up-to-date components with a stock of spares and a fully documented design,
- Possibilities to remotely monitor the status of the transmitters and receivers, as well as to adjust phases, length and sources of the received signals (LHC Bunch Clocks and Orbits),
- Use the AB/RF standard transmitters and receivers, so as the AB/RF piquet service accepts to maintain and support the TTC backbone as it supports its own system.

B. System Overview

An agreement [3] between the experiments, the PH/ESS group in charge of the TTC support and maintenance, and the AB/RF group, was signed in November 2005. The specifications began at the same time and the system design in January. A design review happened in May [4], followed by the production of PCBs during the spring and summer 2006.

This agreement was based on a simple statement: the AB/RF group was already responsible for the transmission of the timing signals from SR4 (Echenevex Site, where the LHC RF is generated) to the CCR using their own equipment. The natural proposal was then to simply extend the transmission links provided by the AB/RF group up to the experiments, removing all the active components from the CCR.

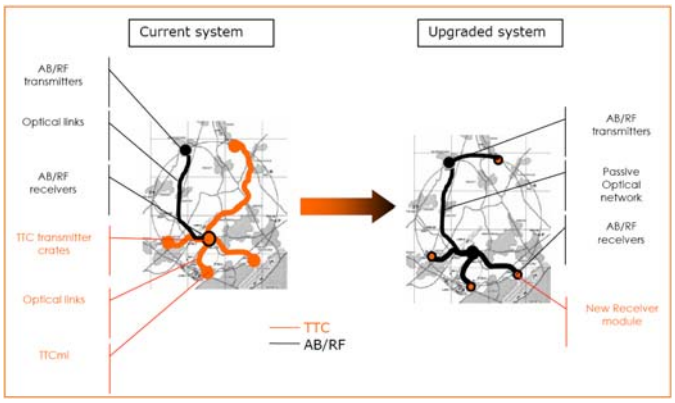

Figure 1: Principle of the TTC upgrade

The TTC transmitter crate will be removed from the CCR, and replaced by simple passive optical splitters. The transmission will be ensured from the SR4 by a 6U VME crate provided by the AB/RF group, equipped with their crate controller and their transmission modules (see figure2). Instead of being encoded following the TTC protocol at the CCR, Bunch Clocks and Orbits will thus be transmitted over parallel optical fibers from the SR4 down to the experiments.

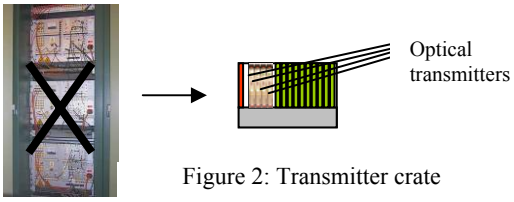

Figure 2: Transmitter crate

In the experiments, the TTCmi (old receiver crate) will be replaced by a 6U VME 64x standard crate, equipped with one crate controller, two or three AB/RF receiver modules, and with one RF2TTC interface module, allowing selection and adjustments of the signal sources before being transmitted to the experiments.

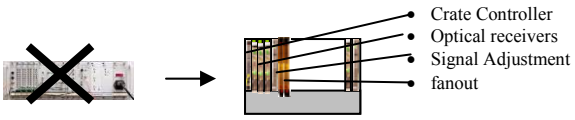

Figure 3: Receiver Crate

The AB/RF optical components to be used in the transmitter and receiver crates were already specified and selected at the end of 2005, but the modules housing them were not designed yet. As these lasers were initially supposed to transmit the 400 MHz Radio Frequency signal of the LHC (as a 0dBm continuous sinewave), they had to be as clean as possible in term of phase noise.
After a complete evaluation of the components made in collaboration between AB/RF and PH/ESS groups [5], the PH/ESS group designed the VME Analogue Optical transmitter and receiver boards according to the AB/RF specification. This set of Analogue modules will be detailed in the following section.

Nevertheless, as the TTC signals (40.078 MHz Bunch Clocks and 11 kHz orbit pulses) - as well as some other signals being used by the AB/RF group for their other applications - were digital, the use of such analogue modules to transmit them would have been an overkill.
PH/ESS, thus, proposed to AB/RF a second set of links, digital, based on SDH/SONET transmitters. After a first evaluation of these digital links made with AB/RF [6], PH/ESS designed one transmitter and one receiver boards, which could replace the analogue set where the signal to be transmitted is not analogue but digital. This set of Digital modules is currently being validated by the AB/RF before being fully standardized. It will be also detailed in the following section.

II. Module Description

The modules composing the receiver crates are here described. This includes the crate controller, the optical receiver modules (analogue and digital), the module in charge of the signal adjustments (RF2TTC) and a fanout module.

A. Crate Controllers

As each experiment standardised a different crate controller for its VME crates, different controller types will be used. The VP110 and the VP317 from Concurrent Technologies for ATLAS and ALICE respectively, the CAEN A2818 and V2718 for CMS, and finally the CAEN V1718 for LHCb.

B. Transmission Links

Two or three receiver boards will be installed in the receiver crate. The corresponding transmitters will be installed in the SR4 transmitter crate. As two types of transmission links (analogue and digital) were designed, both options are here presented.

1) Analogue Link

The lasers and receivers composing these modules were initially selected to transmit the 400MHz Radio Frequency signal, as a continuous sinewave.
It is composed of two modules [8] [9], one transmitter and one receiver, both of them equipped with 2 optical components. The selected link is the LBL 3GHz from MITEQ, designed to transmit analogue 0dBm signals with a very low phase noise (between 0.5 and 3 picoseconds according to the transmitted frequency). The components are uncooled, so a special heatsink has been designed to keep them at a temperature close to 35 degreC. The electrical interfaces of the lasers and receivers are direct SMA connectors fixed on the front panel, to isolate the analogue signals from the digital side of the modules dedicated to control and monitoring.

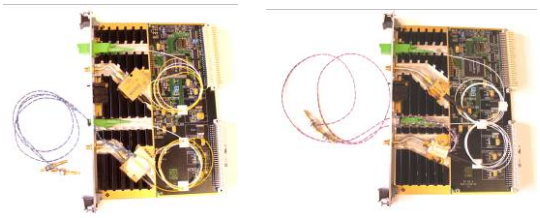

Figure 4: Analogue RF_Tx and RF_Rx modules

The VME interface was designed following the AB/RF standards (type of components, schematics, and firmware). The J2 connector of these modules is not used, as this part of the backplane used in AB/RF VME crates is custom.
These modules are monitored by the VME interface, by reading the VME registers storing the optical power level of the transmission link, both at the laser and at the receiver level.

These modules were fully satisfactory during evaluation [5]. The phase noise measured with 400 MHz sinewave 0dBm signal was less than 0.5ps (see also section III). However, their very high price (7 kCHF per transmitted signal), justified by their very good performances, required to find a cheaper solution for all the signals which did not need such a quality.

A study for a digital link was thus made.

2) Digital Link

These modules were developed by PH-ESS to substitute the analogue ones [10] [11]. Their mandate is to be used instead of the analogue links everywhere the signal does not need to be sinusoidal, but can be transmitted as digital clocks or pulses.

A study was made to identify the components able to transmit and receive various clock frequencies, as well as pulses of various width and periods.
The transmitters selected were the OCP-STX03 and OCP-STX-24, pin compatible, which have respectively 300MHz and 1.5GHz of bandwidth.
On the receiver side, the OCP-SRX-03 and OCP-SRX-24, AC coupled, were selected for clock reception, whereas the

Truelight TRR-1B43-00 was selected for pulses. Indeed, the cut-off frequency of the TRR's AGC (Amplitude Gain Controller) is low enough (below 3kHz) to transmit the 11kHz pulses used for the Orbit signals. Moreover, this component is used everywhere in the TTC system inside the experiments. It is really cheap (7$ piece) and still in production.
Each VME transmitter module can house three pigtailed lasers, which can be OCP-STX-03 or OCP-STX-24 without any hardware changes. To match with various kinds of amplitude and signal types, the electrical input signal is latched at the input of the board using a comparator, the threshold of which can be adjusted via VME registers.

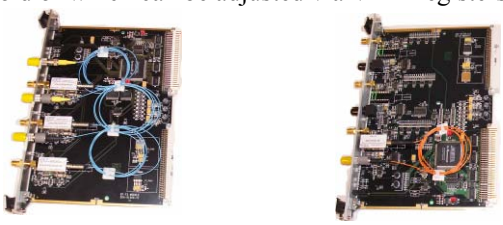

Figure 5: Digital RF_Tx and RF_Rx

Each receiver VME module can house three receiver modules. The design was done to allow various receivers to be used, requiring a minor hardware modification. For 400 MHz or 200MHz clocks, the OCP-SRX-24 can be plugged in. For 40 MHz, the OCP-SRX-03 or the TRR-1B43-00 are recommended. And for pulse (or not DC-balanced signals) reception, the TRR-1B43-00 will be plugged in. On Figure 5, the receiver module is equipped with two Truelight components and one OCP-SRX-03.
Once the conversion from optical to electrical is done (by an OCP or a Truelight component), the signal is converted to standard ECL using a comparator common to OCP and Truelight receivers. A threshold is applied to this comparator, which is adjustable via a VME register. The signal is then fanned out. One copy goes to the FPGA for frequency and signal detection (status accessible via a VME register) and one copy is transmitted to an ECL 50 Ohm coaxial cable driver to make the signal available on the front panel. This full signal path, from optical input to ECL output, is reproduced three times on the VME module.

The price of these modules is much more reasonable than the analogue ones (about 1.2 kCHF per transmitted signal, which is one sixth of the price of an analogue link).
These digital modules are being evaluated by the AB/RF group in charge of their maintenance and support, and by PH/ESS.

The signals delivered by the receiver modules are then transmitted to the RF2TTC module, in charge of their timing adjustment and multiplexing.

C. *RF2TTC Module*

The RF2TTC converts the three 40.078MHz Bunch Clocks (BC1, BC2 and BCref) and the two orbit signals (Orb1 and Orb2) from the optical receivers to ECL signals, and performs various adjustments on each signal before making them available for the in-detector TTC electronics.
The full functionalities are gathered in a specification document [4] [12].

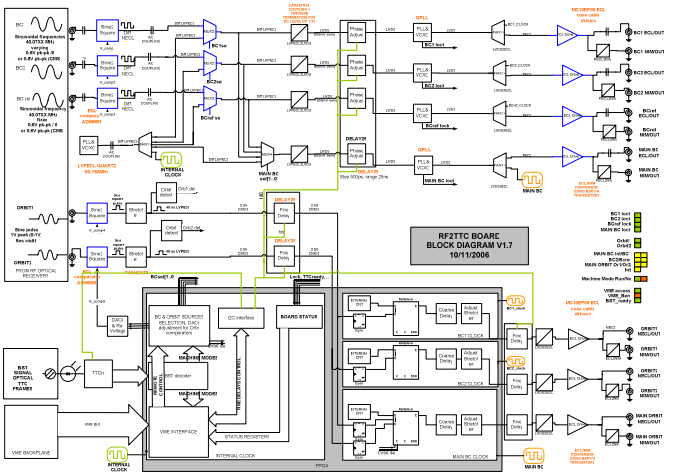

Figure 6: RF2TTC module diagram

The three Bunch Clocks (represented on the top part of the above diagram) are all treated in the following way:
A comparator with an adjustable threshold first converts the input signal into a PECL signal, before being multiplexed with an internal 40.078MHz clock in case of absence of the Bunch Clock on the front panel. The signal is then shifted by an adjustable delay with 0.5ns precision, before being cleaned by a QPLL and transmitted on the front panel via an ECL 50 Ohm coaxial cable driver with an AC-coupled output.
A global multiplexer allows selection between the three Bunch Clocks and the internal clock to generate a fourth Bunch Clock output, called Main BC, which can also be delayed.



Figure 7: RF2TTC module

The two orbit signals (middle and bottom right parts of the diagram) are first converted using the same adjustable comparator stage as for the Bunch Clocks. They are then lengthened to more than 25ns, finely delayed with 0.5ns steps, before going into an FPGA (grey block of the diagram), where they are synchronized to their corresponding clock, multiplexed with an internal orbit, and coarse delayed. Their length and polarity can be adjusted, and they are then again finely delayed before being transmitted by the ECL drivers.
A global multiplexer also allows selection between the two orbits and an internal one, synchronized to the Main Bunch Clock. This orbit signal is called Main Orbit and can as well be finely delayed before being transmitted.

The BST (Beam Synchronous Timing) optical signal (on the bottom left part of the diagram) is received, decoded and analyzed to recover the machine mode. This mode is useful to know when the timing signals are stable and can be used. In deed, neither the Bunch Clocks nor the Orbit signals are fully guaranteed out of the physics modes (flat top of the LHC energy curve). It is thus advised to use internal signals when the machine mode indicates that there is no beam.

All the adjustments are done using VME registers. Many status registers are available, as well as special configurations, for stand-alone or debugging work.

The prototype arrived at CERN at the beginning of October 2006 and is currently being tested.

D. *Fanout Module*

The TTC Fanout module is a 6U VME module designed by the PH/MIC group [13]. It is split in two identical parts. Each of them fans out one ECL input into 18 identical ECL outputs. The delay between the outputs is below 100ps. In addition to these eighteen ECL outputs, four NIM outputs are available for monitoring.
It is possible to daisy chain the two parts, giving a total of 35 ECL outputs and 8 NIM outputs for one ECL input.



Figure 8: TTC Fanout module

The second version of the prototype will be available in October 2006.

III. PERFORMANCES

A. *Optical Components*

The optical components were fully validated in term of phase noise and jitter, before the design of the boards themselves. The results of these measurements are gathered in two documents [5] and [6].
The test setup for the phase noise measurement is the following:

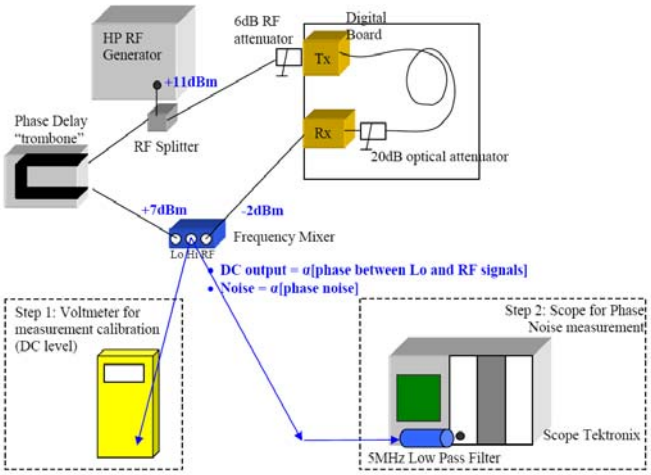

Figure 9: Setup for the Phase Noise measurement

This setup uses a frequency mixer, delivering a sinusoidal signal, function of the difference of the two input frequencies. As the two frequencies are the same (they come from a unique source), the output signal of the frequency mixer is a DC level, plus a function of the phase noise. Shifting the phase of one of the signals, to reduce this DC level as close as possible to 0, allows us to approximate this DC level (V) as a linear function of the phase noise (P): $V=\alpha.P$. Two measurements with slightly different phases give the α coefficient, and we can deduce the phase noise from the signal monitored on the oscilloscope (see fig. 10).

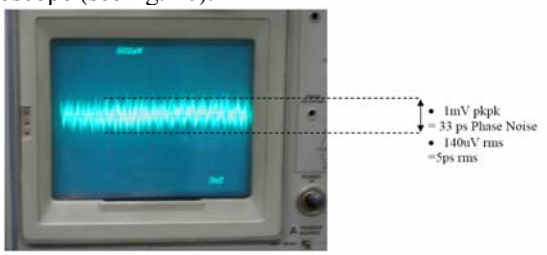

Figure 10: Phase noise measurement

The results measured for the Analog system are gathered on the table below:

Table 1: Phase Noise measurements

Freq (MHz)	Analog System Phase Noise (pkpk)	Digital System Phase Noise (pkpk)
10	20 ps	44 ps
40	5 ps	33 ps
400/160	0.4 ps (400 MHz)	6 ps (160 MHz)

B. *Preliminary System tests*

1) *Bunch Clock Transmission*

Some jitter tests of the complete modules were made in September 2006, using the 40.078 MHz and the 24 kHz signals of the SPS RF, generated close to the CERN Control Room in Prevessin. Digital clock and orbit were transmitted over the previous RD12 TTC, the analogue and the digital transmission systems. The recovered clocks were connected in the TTC laboratory in Meyrin site, to a 1GHz oscilloscope and their relative jitter was analysed.

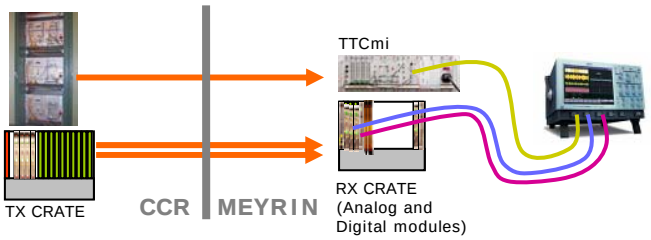

Figure 11: setup for jitter measurements of the three transmission schemes

The recovered signals are displayed on the figure 12, and the jitter results are presented on the table 2.



Figure 12: recovered clocks from the three transmission schemes

Two types of jitter were measured: the Cycle-to-cycle jitter (comparing two consecutive periods of the same signal), and the skew jitter (comparing the phase of one signal to the TTC RD12 recovered clock).

Table 2: jitter measurements

Jitter type	TTC RD12	Analog System	Digital System
Cy2Cy	29 ps rms	18 ps rms	27 ps rms
Skew	-	35 ps rms	36 ps rms

2) 25ns Structured Test beam

The three systems were also compared in the 25ns structured test beam occurring in September. The oscilloscope was triggered by a scintillator's output, and the delays between the trigger pulse and the three clock edges were analysed by the oscilloscope and gathered on one histogram.

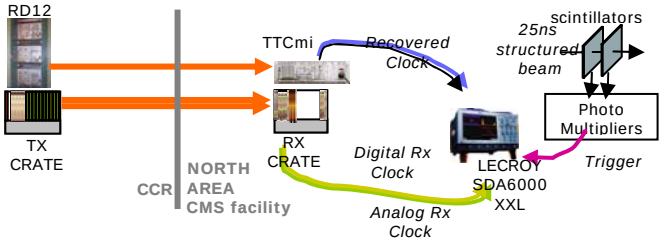

Figure 13: setup using the 25ns structured test beam

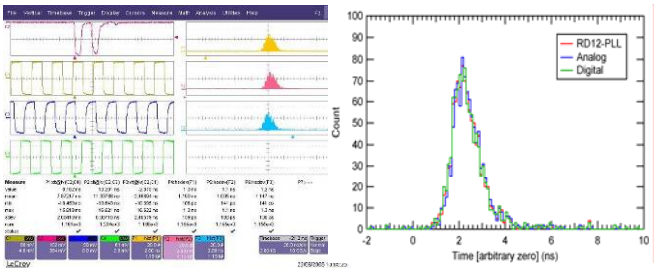

Figure 14: histograms of the jitter measurement between the particle triggers and the three recovered clocks

The three histograms were really identical, as the limiting factor in term of quality was more the jitter of the bunches (of the order of 2ns rms), than the jitter of the systems themselves.

IV. Status

The development of the new system is well advanced. The crates and crate controllers are available for the experiments. Five prototypes of each transmission and reception modules are available. They are currently being tested by the AB/RF and the PH/ESS groups. The RF2TTC prototype arrived at CERN at the beginning of October and is being tested now, together with its VME library. A second version of the TTC fanout is being produced and should be available end of October.

The fibres have been requested from the SR4 point (were the 40.078 MHz and the 11kHz orbit will be generated), down to the experiments control rooms. The installation campaign already began, and the path between SR4 and the CERN Control Room will be cabled by the end of November.

A library to control the full receiver crate, as well as an Application Program Interface (API), is being developed by PH/ESS for the experiments and will be delivered to them in November.

A Production Readiness Review (PRR) will occur at the end of 2006, once AB/RF has validated the transmission and reception modules, and once the experiments have had the opportunity to use the system and to give their feedback.

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On the development of the final optical multiplexer board prototype for the TileCal experiment

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Abstract

This paper describes the architecture of the final optical multiplexer board for the TileCal experiment. The results of the first VME 6U prototype have led to the definition of the final block diagram and functionality of this prototype. Functional description of constituent blocks and the state of the work currently undergoing at the Department of Electronic Engineering, in collaboration with IFIC-Valencia, is presented. As no board is yet produced, no experimental results are presented but, nevertheless, design issues that have been taking into account as component placement and signal integrity issues will be detailed.

I. Introduction

TileCal [1] is the hadronic calorimeter of the ATLAS [2] detector at LHC [3]. Speaking in term of electronic systems, it consists of roughly 10000 channels which are read at the LHC bunch crossing rate (25 ns).

ATLAS trigger system is built around a multilevel concept which reduces the data acquired from the detector from 50 TB/s to 10-100 MB/s thanks to the low effective production cross section of the particles searched. Figure 1 shows the block diagram of the trigger system. Level 1 is detector dependent because it has to adjust to their particularities while level 2 and 3 are common to all subdetectors in ATLAS.

In the interface between levels one and two, data gathering according to physical phenomena takes places and, depending on the detector, also data preprocessing can be performed. This functionality, among others is part of ROD (Read Out Driver) systems [4].

For the Tilecal ROD system, channels are gathered, at this level, following the trigger towers and data is preprocessed calculating, in real time, the energy, timing and $\chi 2$ values using digital signal processing algorithms. These values for all the channels are sent to second level processors for further decision. The ROD system will be built with 32 custom VME boards which will treat around 2 Gbytes/s of data (300 channels per board). The basic schema used is based on the ROD crate concept in which ROD modules are grouped into VME crates jointly with a Trigger and Busy Module (TBM) [5] and possibly other custom cards when needed. This ROD crate interfaces with the TileCal Run Control and the ATLAS DAQ Run control.

TileCal FrontEnd electronics is placed inside the detector. This makes the system sensitive to radiation produced by the particle collisions. In this sense, ATLAS specifications require the electronics to work properly for a period of 10 years.

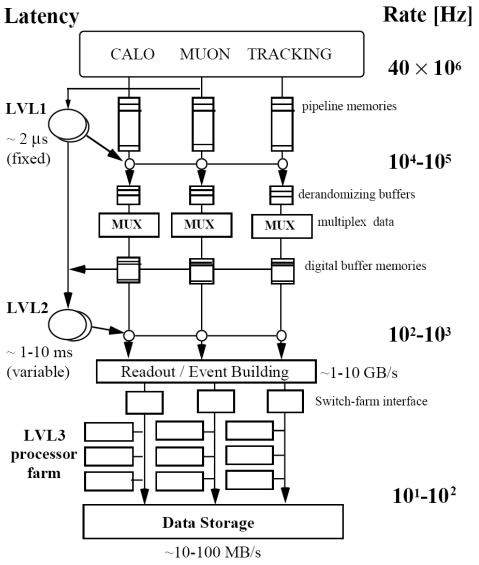

Figure 1: The ATLAS three levels trigger system.

TileCal electronics will receive about 2 Gy/year (0.2 Krad/year) of radiation for a total dose of 20 Gy in the experiment lifetime [6]. To measure radiation hardness of TileCal FrontEnd electronics, tests were conducted with proton beams in different areas and with different beam sizes. Thanks to these tests, three non-destructive kinds of errors were found:

- Transient error in the data flow out to the ROD.
- Permanent errors in the data flow requiring reset.
- Latch-up error with an increment in current consumption of 60 mA.

To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. At ROD system level, data redundancy is used to discard the fibre with errors due to radiation. The checking is based on rightness of the Cyclic Redundancy Codes (CRC) of the data packets on both fibres. This is also necessary as the ROD motherboard is expecting just one fibre per channel. For this purpose a new module, called PreROD or Optical Multiplexer Board (OMB) was conceived.

In this way, the Tilecal ROD System is subdivided into two subsystems:

- The ROD motherboard [7]
- The Optical Multiplexer Board [8]

The ROD motherboard contains the full processing capability for the estimation of energy and time on data coming from the FrontEnd while the OMB will perform data checking looking for transmission errors due to radiation.

II. Optical Multiplexer Board 6U Prototype

The OMB 6U Prototype was conceived as a first experience with the implementation of the functionality of this system. Besides, in the course of the work, a Data Injection Mode was added as a way of testing the ROD module in production phases or whenever there is no FrontEnd available. It has been designed as a VME64x slave module architecture including four optical inputs connectors (two input channels) and two optical outputs connectors integrated in the PCB. The input channels are capable to read up to 4x16 bits at 40 MHz. The output also runs at 40 MHz with a data width of 16 bits.

The error check is based on the real time calculation of the CRC value of the data received on both input fibres. Once calculated, this value is compared to the one included within the data. If the values differ, then the fibre is carrying defective data. Decision logic then selects which fibre will provide the data to the ROD motherboard taking into account the results of the CRC checking. In Data Injection Mode, data can be preconfigured or dynamically loaded using VME bus and injected with an internal or external trigger signal.

There are four input G-Link chips (Agilent HDMP-1034) [9] on the board, two output G-Link chips (Agilent HDMP-1032) [9], two FPGAs for CRC calculations (CRC FPGAs) and one FPGA for VME interface (VME FPGA). These lasts are implemented in ALTERA devices. Furthermore, for the Data Injector Mode, the OMB has two additional copper input cables for trigger and busy signals coming from the ROD motherboard. These external signals are included in this prototype to send correctly internal data in order to test the ROD functionality.

The block diagram of the board is shown in Figure 2. A short description of the main functions of the G-link and FPGA chips in the OMB board is given in Table 1.

Table 1: OMB main components

Components	Main Function	Chip
6 G-Link Chips	Serialize/deserialize the outcoming/incoming data.	HDMP-1034 HDMP-1032
2 CRC FPGAs	Send correct data to ROD. ROD Injector Data.	CYCLONE EP1C12
1 VME FPGA	VME Interface. OMB control.	ACEX EP1K100

1) Input/output hardware

Infineon optical transceivers [10] are used for input and output optical links. There are four optical fibres coming in from the FrontEnd Boards (FEB) and two optical fibres going out to the ROD. G-link chips (HDMP-1034 and HDMP-1032) are used in the input and output stages. The HDMP-1034 deserializes the input bit stream and output it as a 40 MHz 16 bit word data flow to the CRC FPGAs (one per input channel, i.e. two input fibres). The output data of each CRC FPGAs is a 16 bit word stream at 40 MHz sent to the HDMP-1032 chips where it is serialized and sent to the ROD motherboard.

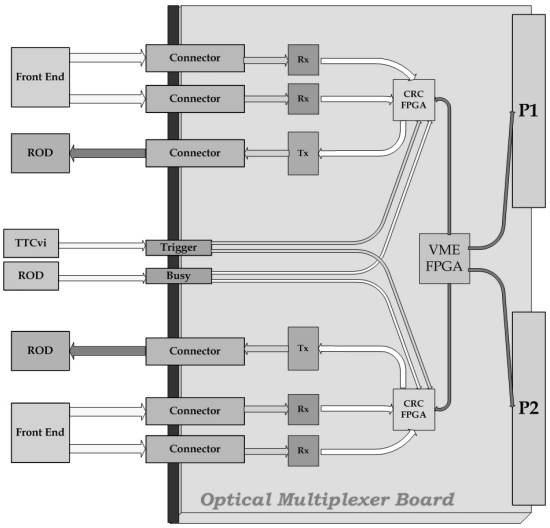

Figure 2: Optical Multiplexer Board Block Diagram.

2) FPGA Description

Two CYCLONE EP1C12 FPGAs [11] are used in the OMB board for CRC checking and link control. The incoming data from each pair of different G-link receiver chips is routed to one of these FPGA. Data is then analyzed, in parallel both input links, and the decision is made on which data link is the correct one. Each CRC FPGA routes the correct data to its G-link transmitter chip.

If the OMB is working in Injection Mode then only the output fibres (and the corresponding serializers) are used. In this mode the data to send is preconfigured in the CRC FPGA firmware or stored in an event memory using VME bus transactions. The user can choose how to trigger these data: either externally (using NIM level signals) or internally thanks to a trigger generator programmed inside the VME FGPA. Once triggered, data is sent either to one or both of the CRC FGPA which sends them to ROD motherboard. The data injection can be stopped externally, if programmed in this way, by means of a Busy signal.

VME interface is controlled by an ACEX EP1K100 [12] FPGA chip present in the OMB. The OMB module is considered as a VME slave module and all actions and commands are controlled by the crate CPU following the VME64 standard.

VME map includes registers holding the number of CRC errors detected in the optical fibres, control registers to select CRC checking or injection mode and an event memory to load the data for injection. The addressing mode is A32D32. A 16-bit bidirectional bus connects the VME FPGA with the two CRC FPGAs.

All the FPGA firmware in the OMB was developed with Altera Quartus II software [13].

3) OMB implementation

The OMB was built using a 12 layer PCB. The layer stackup was designed to minimize crosstalk between layers by routing the adjacent ones orthogonally. Each two internal layers are between power or ground planes for this same reason. Optical transceivers and serializers/deserializers chip signal are preferably routed on the top layer for faster signal transmission. Buses are routed in parallel with equal trace length for minimization of skew. Figure 3 shows a photograph of the OMB finally implemented.

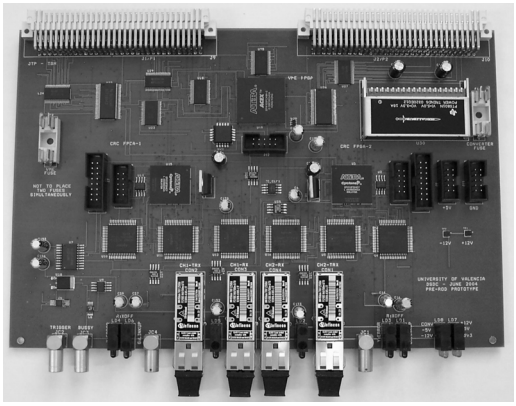

Figure 3: The Optical Multiplexer Board prototype.

III. OMB 9U FINAL PROTOTYPE

The good results achieved with the 6U experience are being now used to define the final OMB prototype. This prototype is conceived in a 1 to 1 ratio with respect to RODs. This means that each final prototype will have 8 input channels (16 fibres) and 8 output channels (8 fibres). Due to this modification a 9U format has been chosen for this new implementation.

With respect to functionality there are some minor modifications among of which, the inclusion of the TTC receiver chip is the main one. This would lead to the possibility of having trigger directly from the TTC system, something which is not possible now.

In view of future upgrades and functionality the design includes four PMC connectors for mezzanine boards connected to CRC FPGAs and is being designed for 80 MHz operating frequency instead of the nominal 40 MHz of LHC.

This last issue poses some problems related to signal integrity and component placement aspects. Among them, the use of a single JTAG chain for the programming of all the FPGA chips in the board, the bus connecting the VME controller and the CRC controllers and the clock distribution are the main concerns. Simulations of these connections as well as firmware modification in the FPGA used are part of the work currently going on.

A. Board Description

Figure 4 shows the block diagram of the final 9U prototype including the modifications mentioned above.

Stratos Ltd. dual optical receiver (M2R-25-4-1-TL) and transmitter (M2T-25-4-1-L) [14] have been chosen to optimize the space in the board.

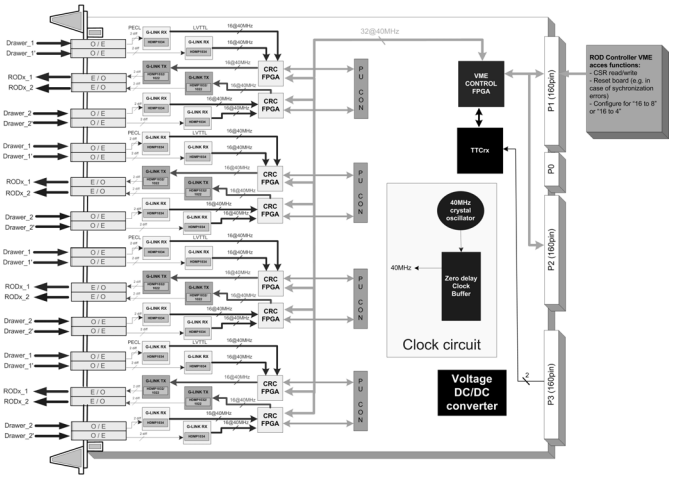

Figure 4: OMB 9U prototype block diagram.

For the CRC FPGAs we use the CYCLONE EP1C12 used in the previous 6U prototype. However, the VME FPGA has been changed from the ACEX FPGA to a CYCLONE EP1C20 FPGA. The reason for this change is that the final prototype includes a TTCrx [15] receiver chip. For this chip, special control firmware must be present in the board. In order to keep the number of components to a minimum we have decided to put this firmware inside the VME FPGA. In order to not compromise the occupancy of the FPGA we have chosen an FPGA with even more logical components than the CRC FPGA.

Figure 4 also shows the four PMC connectors placed in the board which connect to each two CRC FPGAs. The idea behind this decision is twofold: we have plenty board space and, if needed, daughter boards might be plugged in to do some processing tasks on data sent by the CRC FPGAs.

For what respects to functionality, the final prototype keeps the presently available in the 6U prototype except for the possibility of receiving TTC signals. This means that the OMB will be able to inject data on the basis of an external trigger signal or VME command, including real trigger information.

B. PCB description

The OMB final prototype layout is a 10 layers PCB which optimize cross-section to minimize signal integrity problems. Figure 5 shows the arrangement of layers. We tried to keep every signal layer between two power planes or, when it was not possible, routing the two adjacent layers orthogonally. Layers TOP, INT1, INT2, INT3, INT4, BOTTOM are signal layers while PWR1, GND1, GND2, PWR2 are power layers.

Power distribution is also a concern in this board as we need several different supply voltages. For all the FPGAs we need 3.3 V for the I/O while internal operation needs 1.5V. The NIM to TTL conversion for the external trigger signals need a 12V supply voltage while other logic circuitry needs 5 V. The 12V and 5V power supplies are taken from VME bus or, when not available or for testing, from special pins on the board. Generation of the lower voltages (3.3 V and 1.5 V) is

accomplish by voltage regulation from the 5 V main power supply.

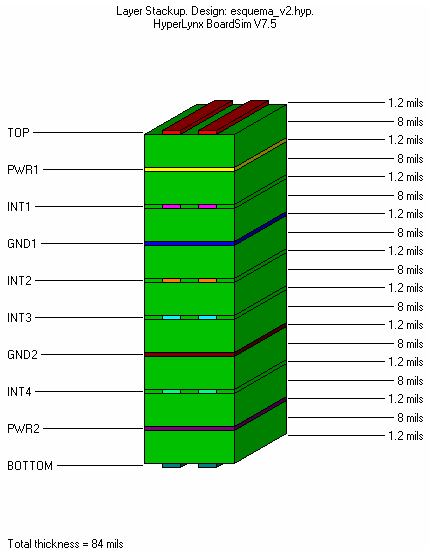

Figure 5: OMB 9U Prototype layer stackup.

With this configuration, we chose to assign PWR1 plane to 3.3 V while PWR2 is a split plane with a main 5V area and a 1.5V island (figure 6).

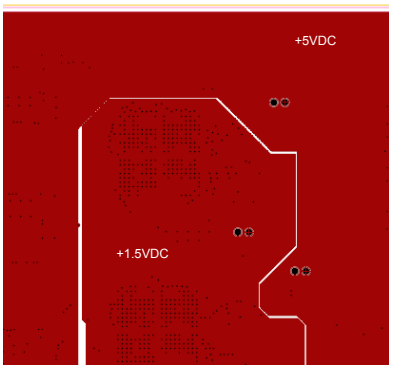

Figure 6: PWR2 split power layer detail.

C. *Signal integrity analysis*

As it was previously mentioned, signal integrity analysis is one of our main concern in the design of this prototype. In this sense, the three main signal distributions to be aware of are the JTAG chain, the clock distribution and the serial bus. Differential lines connecting the optoelectronic connectors and the GLINK chips are also of great importance. However, close placement of chip to connectors and parallel manual routing of the lines assure signal quality.

Because our work is still under development only the analysis of the serial bus will be presented here. This bus has a CLK signal and 3 data lines. In principle, we would only use one of the data lines. The other 2 data lines will be used if an increase of bandwidth is needed.

The key point is this analysis is how to route and terminated properly this bus. We test three different routing and termination schemes and analyzed them with Cadence PCB Studio and SigExpert tools [16].

The first attempt was to route the bus from the VME FPGA to a point between the first and second CRC FPGA. All these FPGA will be place in a column along the board width. Figure 7 shows this configuration.

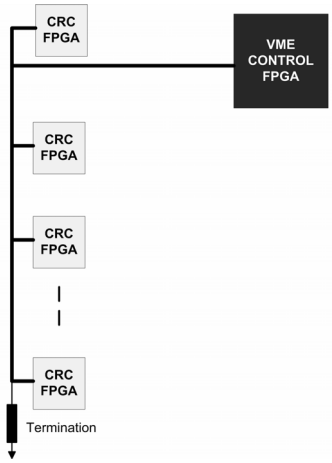

Figure 7: First routing scheme from VME to CRC FPGAs.

After topology extraction, simulation of the bus signals was carried out. The results are displayed in figure 8.

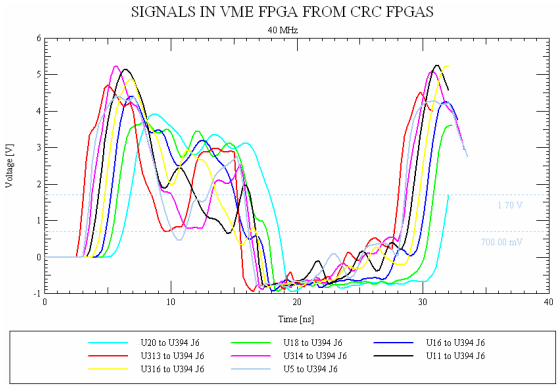

Figure 8: Simulation results of the first configuration

It is clear that the results are everything but satisfactory as several signal cross the logic thresholds even more than once. The reason for this behaviour is the “T” junction that appears when the lines coming from the VME FPGA get to the ones connecting all the CRC FGPA. This junction creates reflections which travel all along the line. Also reflections at the top FPGA travel down the bus creating interferences.

A better, but not too much, behaviour is accomplish is the routing is designed so signals travel along all the CRC FPGA from top to bottom, as figure 9 shows.

Simulation results of this configuration are shown if figure 10. We may observe a little improvement in signal quality but these results are far from optimum.

From this point we analyzed the termination scheme. In the literature bidirectional buses like this one are generally terminated using serial resistors at the output of all the devices attached. However this generates an staircase waveform in the middle of the bus. In our case, data go from an to the VME FPGA but not among the CRC FPGA so, strictly speaking this bus is not full bidirectional.

Analysis of this special case with SigExpert showed that the best results are achieved when one termination resistor is

placed at each end of the bus, i.e. one at the VME FPGA output and one at the bottom CRC FPGA (figure 11). The value of this resistor is 50 Ω.

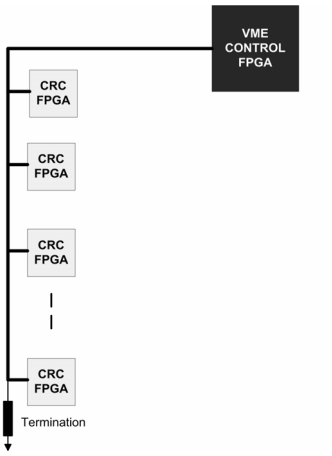

Figure 9: Second routing scheme from VME to CRC FPGAs.

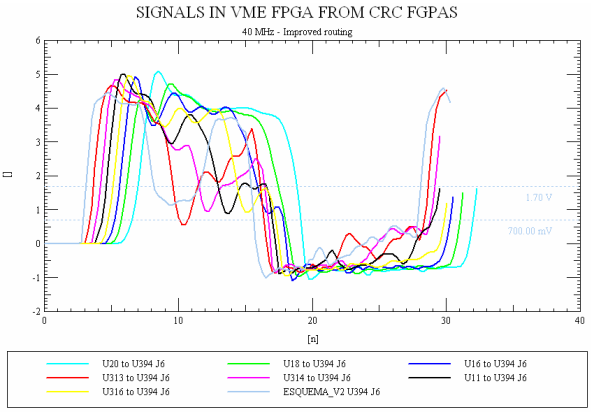

Figure 10: Simulation results from the second configuration.

With this termination setup results are greatly improved as it is shown in figure 12. This means that the correct routing will be from top to bottom CRC FPGA with two resistors placed at both ends of the bus.

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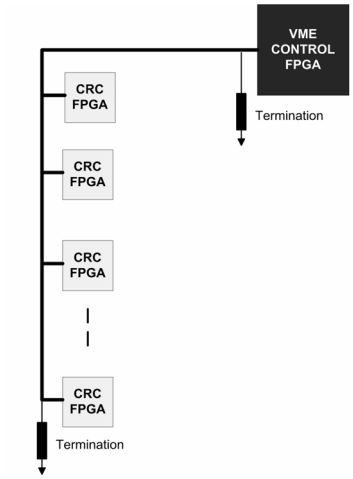

Figure 11: Final routing scheme of the serial bus.

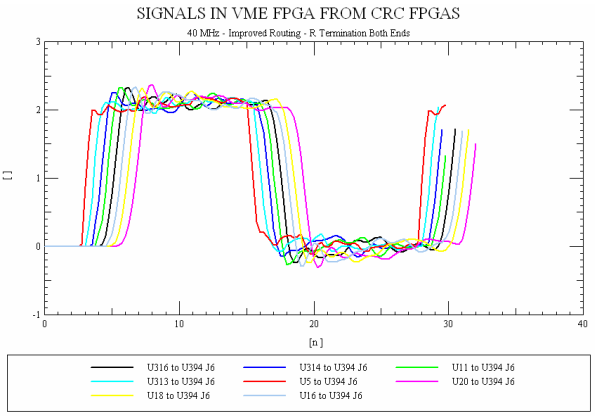

Figure 12: Simulation results of the final configuration.

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V. Acknowledgments

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Parallel Session A7

ASIC developments

Front-end Electronics for Silicon Trackers readout in Deep Sub-Micron CMOS Technology The case of Silicon strips at the ILC.

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Abstract

For the years to come, Silicon strips detectors will be read using the smallest available integrated technologies for room, transparency, and power considerations. CMOS, Bipolar-CMOS and Silicon-Germanium are presently offered in deep-submicron (250 down to 90nm) at affordable cost through worldwide integrated circuits multiproject centers. As an example, a 180nm CMOS readout prototype chip has been designed and tested, and gave satisfactory results in terms of noise and power. Beam tests are under work, and prospectives in 130nm will be presented.

I. Context of the Silicon Strips at the ILC

A few millions of 10 to 60 cm long Silicon strips are foreseen for a large Silicon tracker at the ILC. Their thickness will be between 200 and 500µm, with a strip pitch between 50 and 200 µm. They will be single sided. DC versus AC coupling is presently being evaluated in terms of costs, and overall complexity.

A. Detector and Readout Parameters

Such Silicon strips exhibit a dominating interstrip capacitance of the order of 1 pF/cm and strip to substrate capacitance of 0.1 pF/cm. The occupancy at the ILC defined as the percentage of channels hit per beam crossing will be less than 1 % in the barrel layers, of the order of a few per cents in the end caps layers. The ILC machine will produce trains of 3000 or 6000 bunches spaced by 150 or 300 ns for 1ms, followed by an idle stage of 100 ms. During trains, data will be recorded in analogue pipe-lines, then digitised and processed during the idle stage.

B. Detector data

Both pulse height and time will be recorded. A resolution transverse to the strip of a few micrometers can be achieved using centroids, and two shaping times will be implemented, one from 500ns to 1 µs on all layers, depending mainly on strip length for beam crossing tagging, and 10-30 ns for some nanosecond timing layers intended to provide a crude measurement of the impact along the strip with a resolution of a few centimeters.

C. Coordinate along the strip

Pulse propagation evaluation along the strip using a Spice based linear model and laser diode stimulation measurement show that a current pulse induced in a strips at a given length propagates a voltage step along the strip as in a RLC transmission line with a velocity $1/\sqrt{LC}$ of the order of c / 3.7 (~ 8cm/ns), where L and C are the inductance and capacitance of the strip per unit length. The Spice model includes both strip to substrate and the interstrip capacitances as shown on Figures 1 and 2. Figure 3 shows the measured propagation when strips are illuminated with a laser diode light moved along the detector.

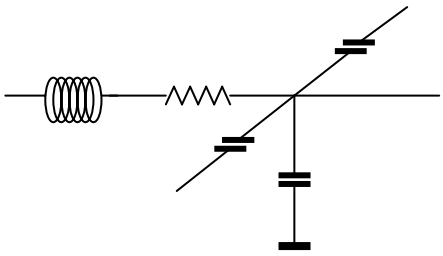

Figure 1. Strip linear model

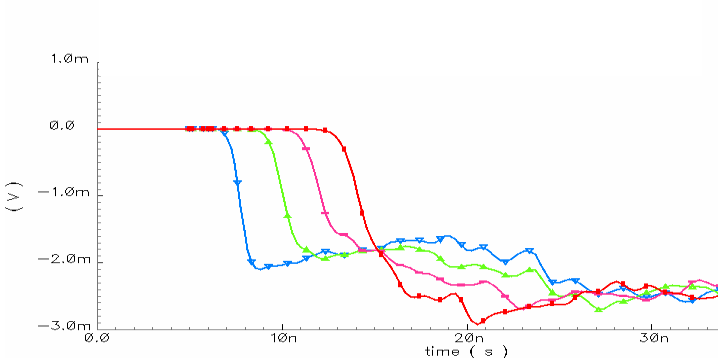

Figure 2. Spice simulation of a propagating voltage pulse along a microstrip detector.

Work in the framework of the SiLC R&D (Silicon for the Linear Collider) collaboration and the EUDET I3-FP6 European project

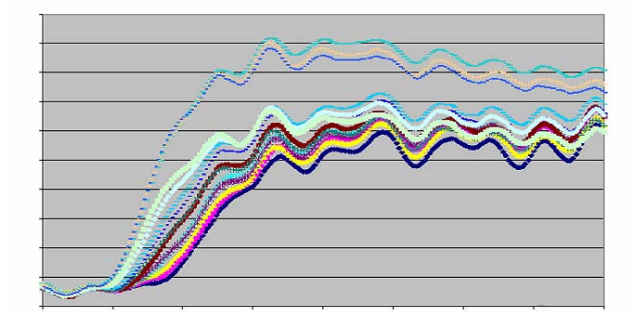

Figure 3. Measured relative response moving a laser light source by 0 to 24 cm along the strip (horizontal scale 50 ns).

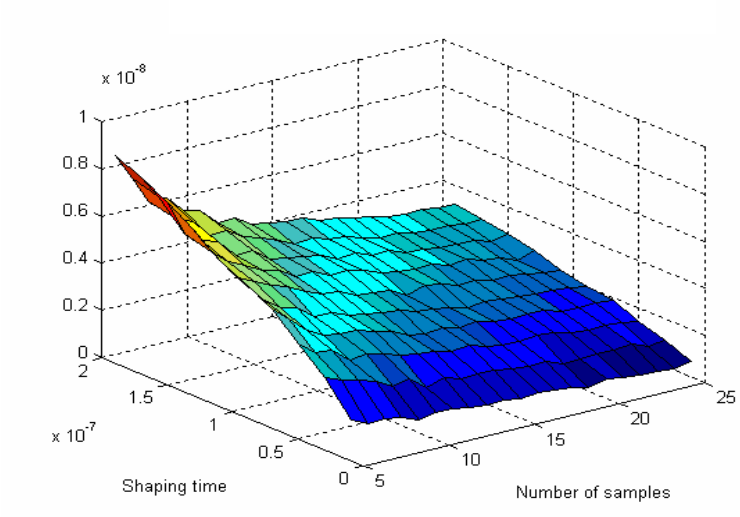

Figure 4. Simulated time resolution as a function of the shaping time, and the number of samples. Signal to noise is set to 25. Least square time estimation using the Cleland and Stern algorithm Ref[1].

II. TECHNOLOGIES

The Silicon detector and VLSI technologies allow today to improve both detector and front-end integration. Front-end chips implemented in deep sub-micron CMOS technologies down to 90nm allow to integrate hundreds if not thousands of channels at a reduced power budget, thanks to the reduction of all wiring capacitors. Silicon-Germanium exhibits less 1/f noise for a bandwidth improved by one order of magnitude, chip thinning, bump bonding and even 3D integration Ref[2]. will allow smaller pitch detectors and consequently better position and time resolution, for less on-detector material.

III. INTEGRATED FRONT-END ELECTRONICS

The data sketched above can be obtained from the detector with pulse sampling allowing to get accurate amplitude and timing. Sparsification is to be performed in the front-end, using thresholds on analogue sums of adjacent channels. Calibration can also be integrated in the front-end chips using Digital to Analogue Converter and Metal Insulator Metal capacitors of known values as charge reference, together with switches networks.

During data taking, activity exceeding the threshold on a given channel will be stored in a 16-deep analogue pipe-line including pedestal, and digitised after the train in parallel for all channels with a 10-bit Wilkinson Analogue to Digital Converter. In case a strip is hit several times during a train, an event buffer can record 16 sets of samples. The analogue pipe-line has therefore two dimensions, along time and events.

Digital signal processing in the front-end can perform some low level tasks such as centroids, least squares amplitude and time fits, lossless data compression, error correcting codes.

Power will be carefully optimised, taking into account the duty cycle of the ILC machine allowing to save at more a factor of 100. On the ILC detector, the voltages supplies will be ramped in a round robin scheme to avoid high current spikes on single spots in the detector.

The foreseen front-end chip architecture is depicted on Figure 5.

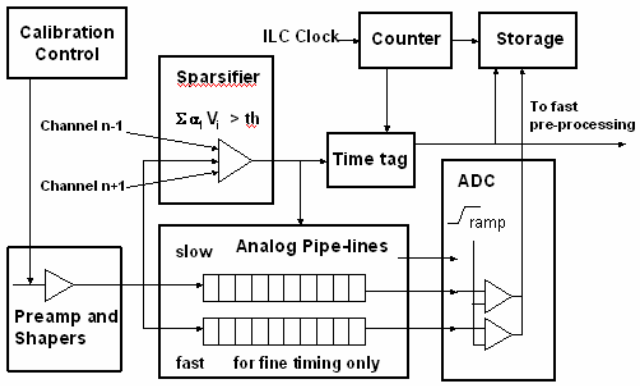

Figure 5. Foreseen front-end chip architecture

To summarize, the goal as seen today is to integrate 512 to 1024 channels in 90nm CMOS including amplifiers with a 20-30mV/MIP voltage gain over 20-40 MIPs, two pulse shaping options: 500ns-1µs, and 20-50ns for fine timing, zero suppression, pulse sampling, event buffering, AD conversion, digital pre-processing, calibration and power switching.

A. 180nm Chip

A chip has been submitted in 180nm CMOS technology, and tested in 2005. Each channel comprises a preamplifier-shaper, a sample and hold, and a comparator. The 180 nm CMOS technology and tools from United Microelectronics Corporation, Taiwan, were accessed through Europractice at IMEC (Leuven Belgium). The process allows six metal layers, various threshold voltages transistor options with thin oxide C_{ox} at 4.9 mF/m^2, 3.3V transistors, Metal Insulator Metal planar capacitors at 1 fF/µm^2.

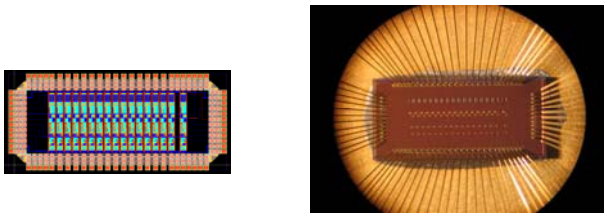

Figure 6. 180nm chip layout and picture.

The preamplifier is a buffered folded cascode structure providing a gain of 8 mV/ MIP, the shaper is an active CR-RC filter using an optimised version of the preamplifier. Power is 210 mW for the preamplifier and shaper. The chip has been extensively tested, process spreads within a wafer have been measured of the order of 3 % (Figure 7)

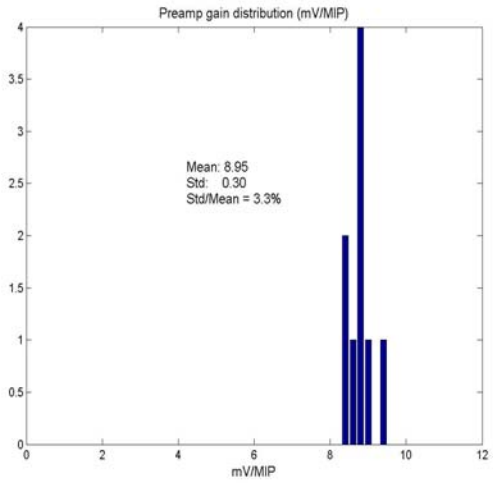

Figure 7. Process spreads (preamplifier gain) across a 180 nm CMOS wafer from UMC.

The shaper output noise is shown Figure 8. A total noise of 375 electrons + 10.4 be-/pF is found against 275 + 8.9 predicted by simulations, explained by a small instability of the shaper understood and fixed in the 130nm next version.

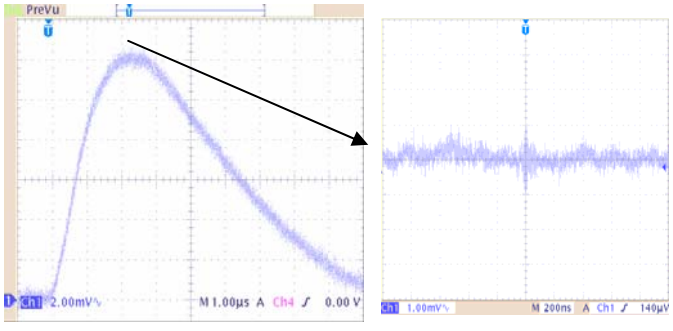

Figure 8. Shaper output. 375 electrons rms noise

As a conclusion, this process appeared to be stable and mature, models being accurate, only one failure found over twelve chips measured. As the 130 nm CMOS process from UMC was available beginning 2005, it was decided to switch the next design to this technology.

B. 130nm Chip

The motivations to go to thinner process were the following: chips are smaller, faster, more radiation tolerant, dissipate less power. In addition, support will be given in the next years to this technology that will be dominant in the industry.

However, some features make designs more constraining such as a reduced voltage swing (to keep the same electric field in the devices), leaks appear under the threshold voltage, as well as tunnel currents across the gates. Models are more complex, somewhat inaccurate in some cases as found later on.

Table 1 compares 180 and 130nm technologies.

Table 1.

	180nm	**130nm**
3.3V transistors	yes	yes
Logic power supply	1.8V	1.2V
Metal layers	6 Aluminum	8 Copper
MIM capacitors	1fF/µm^2	1.5fF/µm^2
Transistors	Three Vt options	+ Low leakage option

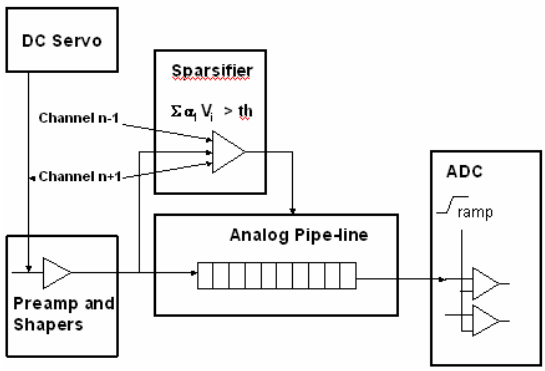

Figure 9. 130nm prototype chips architecture

The chip submitted in May 2005 was received in August and is being tested at the time of this workshop. Figure 10 shows a simulation of the analogue pipe-line signals and controls. Figure 11 shows layout and picture as well as analog sections in 180 and 130nm at the same scale.

A second chip in 130nm has been sent recently including the DC servo as shown in Figure 9, and an improved version of the sampler.

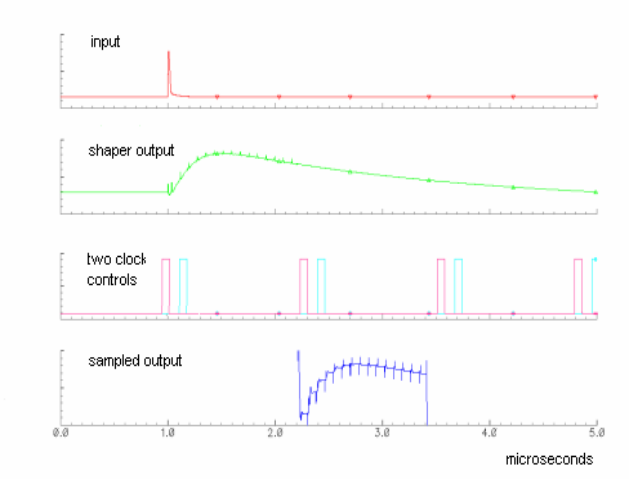

Figure 10 . Simulation of the analogue pipe-line signals and controls.

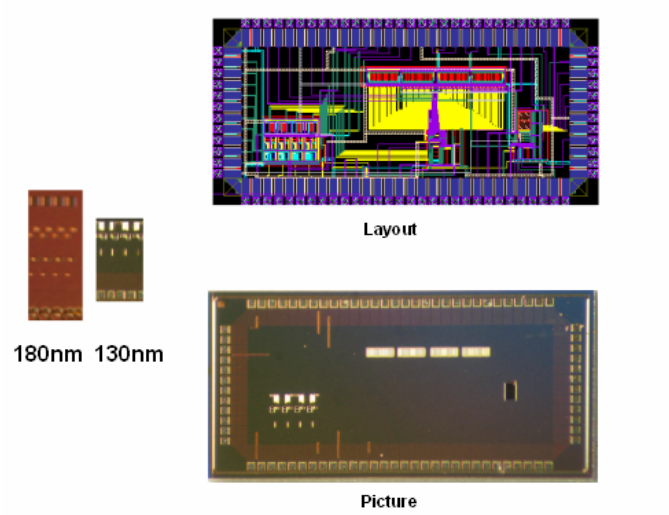

Figure 11. 130nm Silicon. Layout and picture.

During the design of these chips, NMOS noise was found much higher in simulations compared to the 180 nm process under the same sizes and transconductance conditions, and low Vt transistors somewhat leaky, as the low leakage option was not used. These features will be measured when the chips will be delivered. Verifications were done using Mentor rather than Cadence .

IV. Future Plans

If these 130 nm chips give the expected results and noise is within acceptable levels, next versions will include the fast shapers and samplers, as well as calibration and power cycling. A 128 channels chip able to read a Silicon detector is envisaged. Digital has to include chip control, buffer memory, processing for calibrations, amplitude and time estimations, raw data lossless compression. Digital library are available at Virtual Silicon Technologies, synthesis, place and route tools from Cadence together with the design kits provided by Europractice. Some IPs (PLLs, SRAM) are even available.

V. Conclusion

At the time this workshop takes place, a 180nm chip has been successfully designed and tested. This technology allows clearly to design the low noise mixed designs required by Silicon strips detectors. Two 130nm CMOS prototypes have been submitted including a full readout chain up to the AD conversion. Depending on the results, this work will be carried on with multi channel versions, the goal being to provide in 2007 chips able to read a full Silicon detector, including calibration and power cycling.

Acknowledgments

The authors are indebted to Erwin Deumens and Paul Malisse at IMEC for the efficient help provided along the chip designs, in particular at the verifications stage. Interface with UMC (Taiwan) was also extremely positive, thanks to their efforts.

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Prototype of the Front-end Circuit for the GOSSIP (Gas On Slimmed Silicon Pixel) Chip in 0.13 µm CMOS Technology.

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Abstract.

The new GOSSIP detector, capable to detect single electrons in gas, has certain advantages with respect silicon (pixel) detectors. It does not require a Si sensor; it has a very low detector parasitic capacitance and a zero bias current at the pixel input. These are attractive features to design a compact, low-noise and low-power integrated input circuit.

A prototype of the integrated circuit has been developed in 0.13 µm CMOS technology. It includes a few channels equipped with preamplifier, discriminator and the digital circuit to study the feasibility of the TDC-per-pixel concept.

The design demonstrates very low input referred noise (60e^- RMS) in combination with a fast peaking time (40 ns) and an analog power dissipation as low as 2 µW per channel. Switching activity on the clock bus (up to 100 MHz) in the close vicinity of the pixel input pads does not cause noticeable extra noise.

I. Introduction

The GOSSIP (Gas On Slimmed Silicon Pixel) detector [1], depicted in Fig.1, consists of a CMOS pixel array with a grid foil, placed parallel at a distance of 50 µm. Recently the grid has been realised by means of wafer post-processing technology (Integrated Grid or InGrid) [2]. One mm above this grid a cathode foil is built. The cathode foil and the grid are put at -800V and -400V, respectively, and the pixel array surface is at ground potential. The volume between the cathode foil and the pixel array is filled with a suitable gas mixture.

When a fast charged particle crosses the drift gap, a track of electron-ion pairs will be created. Driven by the electric field the electrons will drift into the holes in the grid. In the gap between the grid and the (pixel) anode, an electron avalanche occurs with sufficient charge to activate an on-pixel integrated circuit [3]. The activated pixels will show the projection, on the array surface, of the track. From drift time measurements the polar angle of the track and its distance to the anode could be obtained [1].

The GOSSIP detector has advantages with respect to the now widely used Si vertex detectors. Instead of a silicon sensor it has a 1 mm layer of gas, reducing the material budget, and the radiation damage in the depletion layer of the silicon sensor is eliminated (the on-pixel circuit will be sufficiently radiation hard due to the intrinsic properties of the up-to-date deep-submicron CMOS technology).

The value of the parasitic capacitance at the input of the front-end circuit is determined by the area of the pixel pad and consequently could be as low as 5 - 30 fF. This feature enables us to design a low-noise (60 – 80 e^- (RMS)) and at the same time very low power circuit (2 µW per pixel).

The low power aspect is of primary importance since cooling systems add material to the detector. We expect the GOSSIP chip to dissipate 100 mW/cm^2. In this work we have developed a prototype of the front-end circuit in 0.13 µm CMOS technology.

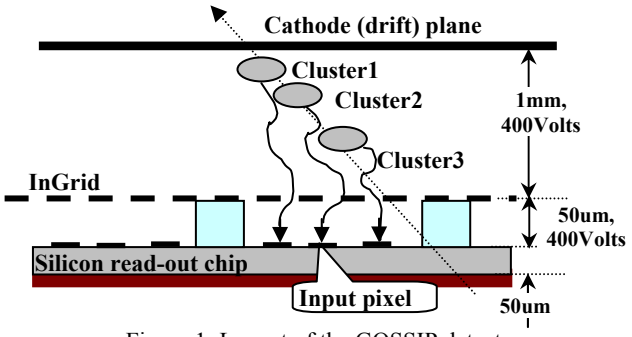

Figure 1: Layout of the GOSSIP detector.

II. Inputs and requirements for the design of the readout circuit

A. Single electron efficiency

Simulations show that 90 % efficiency of detecting single electrons can be reached at a gas gain of 4000 and a threshold of 400 electrons (see Fig.2). This sets a limit to the input-referred ENC.

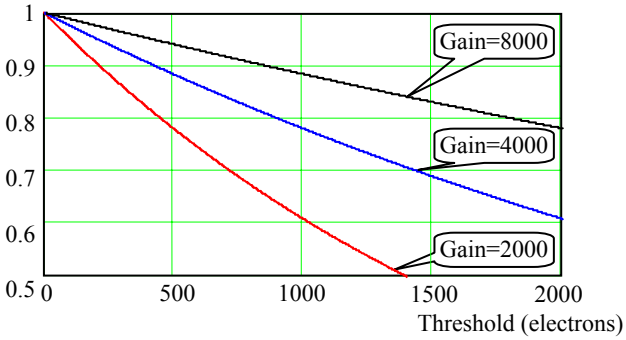

Figure 2: Single electron efficiency as a function of operating threshold.

B. *Shape of the detector current signal*

The detector current has an electron and an ion component. The drifting electrons cause a short current pulse, while the ion component is determined by the drifting ions crossing the gap between the anode and the grid (see Fig.3).

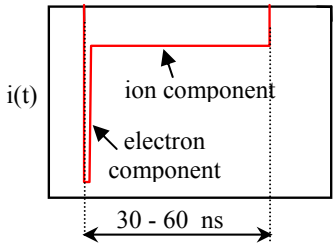

Figure 3: Schematic shape of the detector current [3].

C. *Single electron drift time measurements.*

Simulations have shown that a time resolution of 2 ns (RMS), corresponding to spatial resolution of 100 μm (RMS), seems feasible (see Fig.4).

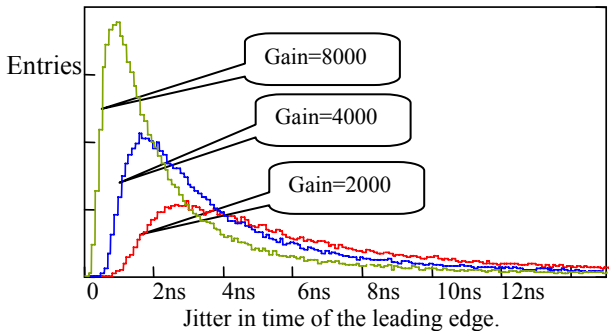

Figure 4: Simulations of the single electron drift time resolution at various gas gain factors.

In order to measure the drift time of each of the electrons on the track, each pixel must be equipped with an individual time-to-digital (TDC) converter.

D. *Analog-digital crosstalk.*

Data taking and readout will occur simultaneously and constantly. The high sensitive analog front-end circuit will operate in the close vicinity of the high speed switching gates. This requires to make every effort to keep the front-end away from the switching noise.

E. *Power consumption.*

A low power dissipation reduces the amount of material for a cooling system. We intend to limit the power dissipation to 2 μW per pixel (~ 100 mW per cm^2).

III. The prototype of the front-end circuit.

A. *Parasitic capacitance at the input of the front-end circuit.*

The detector source capacitance is an important input parameter for the front-end circuit design. It determines the optimum set of parameter values for speed, noise and power consumption. In the GOSSIP detector, the source capacitance consists of three components. These are the pad-to-InGrid capacitance ($C_{p\text{-}grid}$), the pad-to-pad capacitance ($C_{p\text{-}p}$) and the pad-to-substrate capacitance ($C_{p\text{-}sub}$) (see Fig.5).

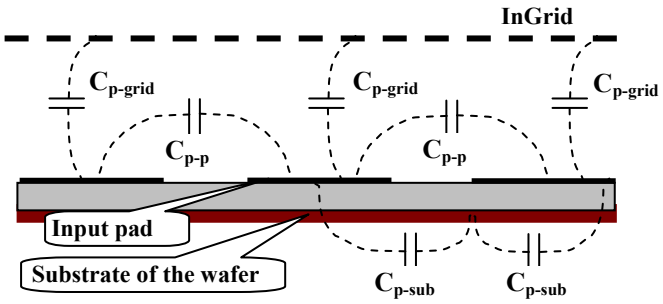

Figure 5: Parasitic capacitances associated with the input pad

The pad-to-substrate capacitance is dominant: it depends on the pad size and is large due to the very thin dielectric layer in the body of the chip. With no need for a (bump-bonded) silicon sensor, a very small size of the input pad is possible. As a result, a very low value of the source capacitance of around 10 fF can be reached (see Fig.6).

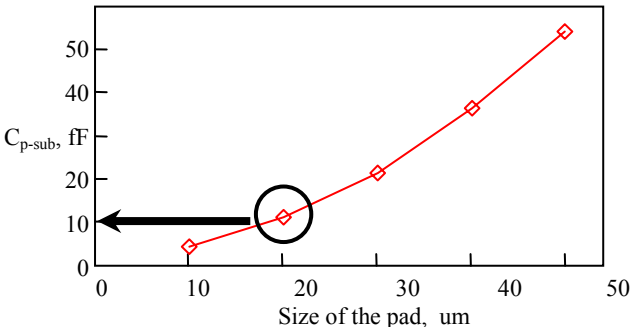

Figure 6: The pad-to-substrate capacitance as a function of the size of the pixel.

B. *Gain in the charge-sensitive preamplifier.*

Charge-to-voltage gain of the charge-sensitive preamplifier (see Fig.7) is inversely related to the feedback capacitance.

$$\text{Charge-to-voltage gain} \approx C_{fb}^{-1} \qquad (1)$$

To get the highest gain we should decrease the feedback capacitance. However, its value must be larger than the parasitic capacitance value divided by the open loop gain factor as follows:

$$C_{fb} >> C_{par} / A \qquad (2)$$

Since C_{par} is 10fF and A is around 100, we can consider a feedback capacitor with a value as low as 1fF.

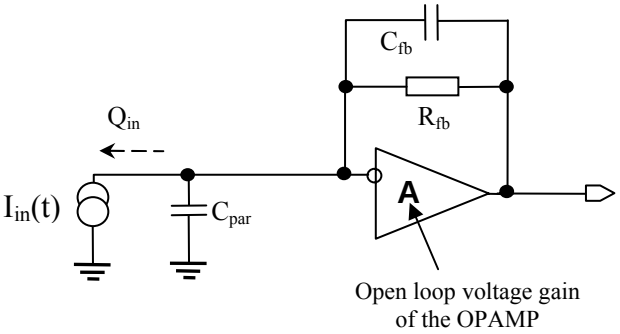

Figure 7: The charge-sensitive preamplifier.

In order to optimize the parasitic capacitance, a coaxial-like structure has been applied (see Fig.8). In this structure the feedback capacitance is formed by vertical plate capacitance. High precision in the capacitance is guaranteed due to accuracy of lithography and thickness of the metal layer. In addition, in this layout the high sensitive input is shielded and isolated.

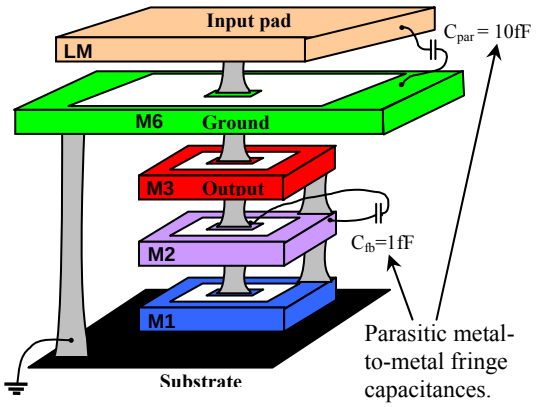

Figure 8: Layout of the input interconnection.

C. *Schematic of the preamplifier.*

The scheme proposed by Krummenacher [4] is a common way to implement a preamplifier for hybrid pixel detectors. The circuit compensates for the leakage current of the silicon sensor. It will, however, become unstable if the parasitic capacitance at the input is very low.

The GOSSIP detector has no leakage current. Krummenacher's scheme has been modified to improve the stability (see Fig.9). The current in the load of the differential pair M1-M2 has been kept fixed. As a result, the circuit has an intrinsically safe phase margin, even when the input parasitic capacitance approaches 10 fF.

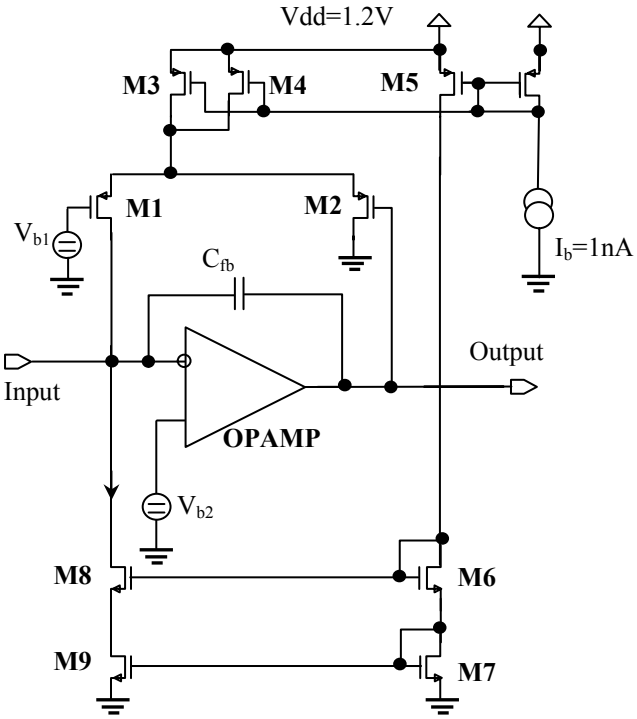

Figure 9: Schematic of the charge sensitive preamplifier.

DC feedback in the circuit allows for discharging of the feedback capacitor. The virtual resistor is a sum of inverse transconductances of transistors M1 and M2 and equals 80 MΩ. It also biases the input of the circuit so as to keep the voltage at the output equal to the reference voltage (V_{b1}). Because of use of differential stages and floating current sources the biasing is highly insensitive to temperature drift and power supply voltage instability. Statistical spread of the offset at the output is 20mV (RMS) corresponding to the input referred signal of 170 electrons.

The operational amplifier (see Fig.9) is formed by a cascode differential pair, loaded with a current mirror (see Fig.10). A voltage follower provides a low output impedance of the amplifier. The input-to-output small signal transfer function has a pole with time constant of 14 ns, and the opamp has a DC gain of 130. The circuit draws about 1.2 μA current from the 1.2 V power supply. The overall power consumption is 1.5 μW.

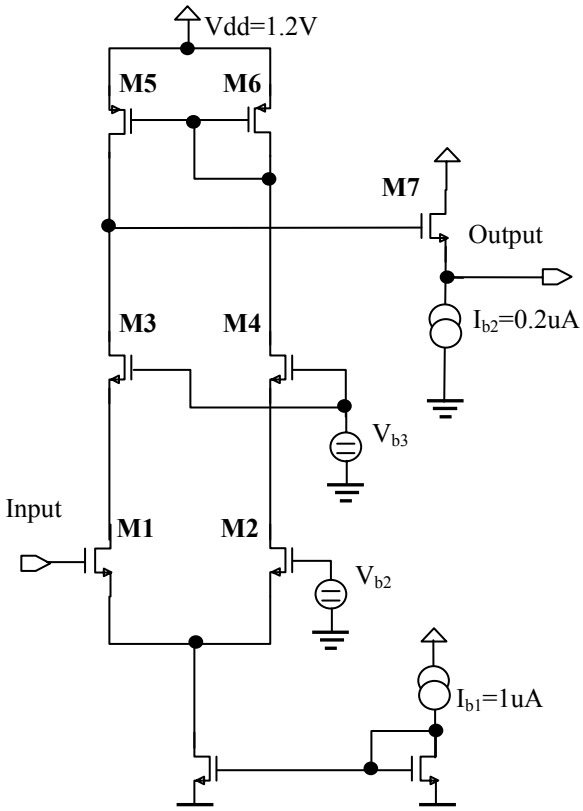

Figure 10: Schematic of the operational amplifier.

D. Objectives of the prototype.

In prototype, submitted on December 12, 2005, we intended to measure the most important characteristics of the front-end circuit such as stability, pulse response, noise and channel-to-channel spread. For this purpose a bare preamplifier with a voltage follower has been designed. We also built a complete front-end circuit including a CMOS comparator and a counter. With this, cross-talk between the sensitive analog inputs and the high speed switching CMOS blocks can be observed. A general view of the physical layout of the prototype is given in Figure 11.

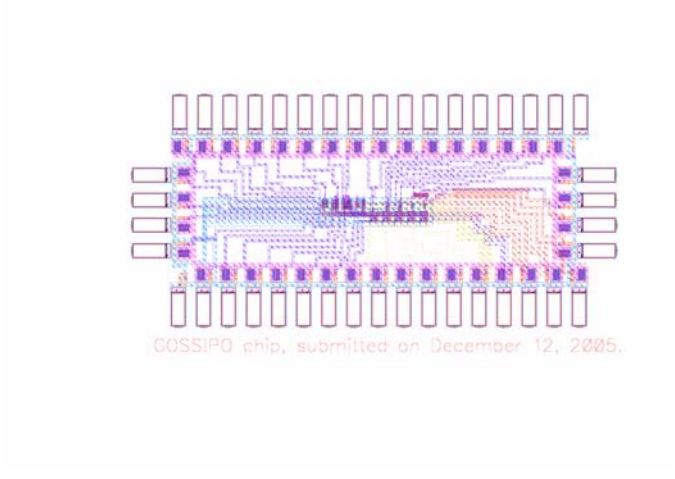

Fig.11. The prototype of the GOSSIP chip, submitted on December 12, 2005.

Substrate noise is likely to be the most significant cause of the analog-digital crosstalk. The local substrate potential fluctuates due to current flow, originated by the switching of the digital gates. The substrate fluctuations will affect the characteristics of the analog circuits. A very nice feature in the used 0.13 µm CMOS technology is the option to make a floating p-well separated from the substrate. In the p-well we can place analog N-type transistors and keep them away from the substrate noise (see Fig.12). Using this, the analog-digital crosstalk has been essentially eliminated.

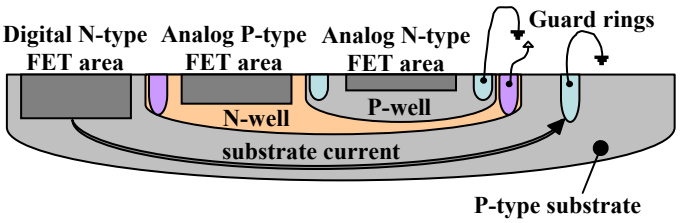

Figure 12: Triple well layout in the 0.13 µm CMOS technology.

E. Measurements & results

The measurements demonstrate that the preamplifier has a sufficient stability margin and an expected shape of the pulse response (see Fig.13). The equivalent input noise charge is 60 electrons (RMS), in agreement with simulations.

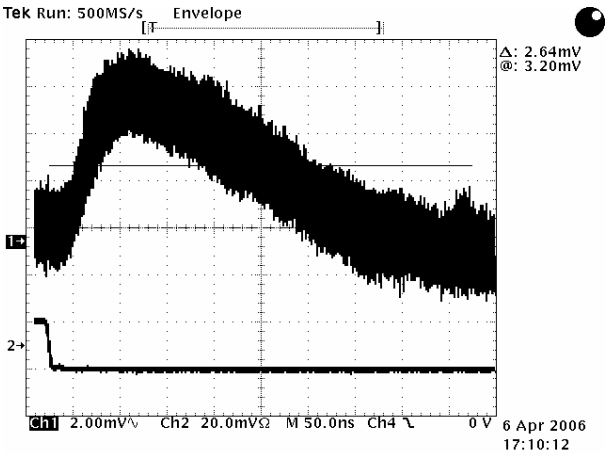

Figure 13: Delta-pulse response of the preamplifier. The input signal is 410 electrons.

The output response of the CMOS comparator of a delta-pulse at the input is given in Figure 14. No indication of after-pulsing or oscillation supports our expectation that the parasitic output-input crosstalk is very low.

The channel-to-channel spread of the threshold is 160 electrons (RMS). Also this result is consistent with simulation.

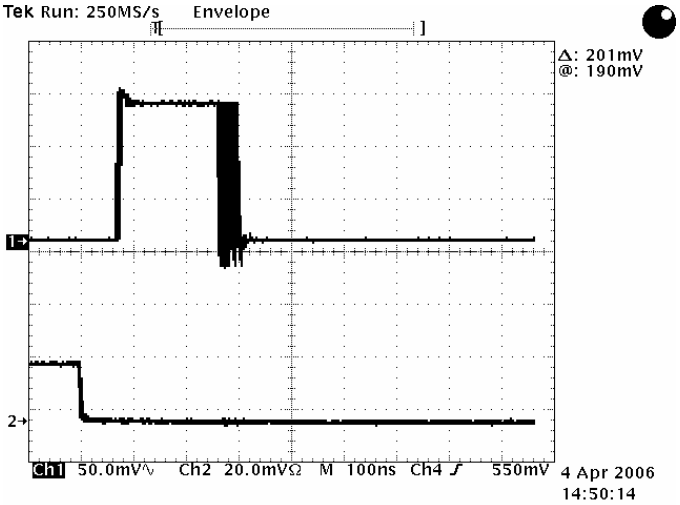

Figure 14: Delta-pulse response of the output of the CMOS comparator. Input signal is 410 electrons. Threshold is 300 electrons.

We also studied the analog-digital crosstalk by asserting a 100 MHz clock signal to the CMOS counter which is in the close vicinity of the high sensitive front-end. Even at very low threshold, no significant crosstalk to the input has been observed at the output of the comparator (see Fig.15).

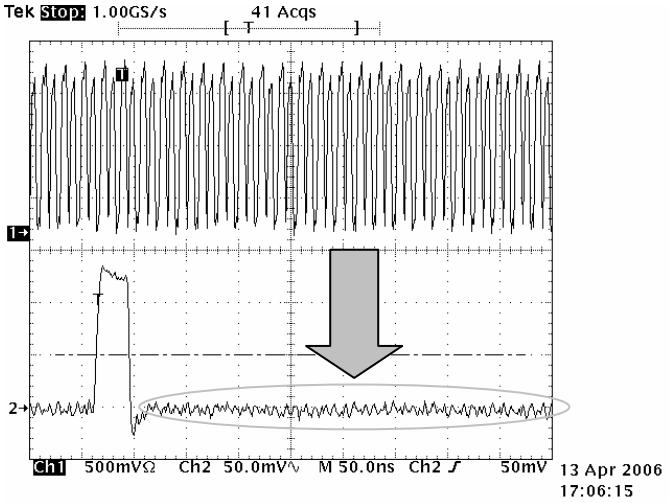

Figure 15 Output of the CMOS comparator along with the clock signal running at 100 MHz.

IV. Conclusions and plans.

The front-end readout circuit of the GOSSIP chip benefits from the low detector parasitic capacitance and the absence of any leakage current.

This first prototype demonstrates that a fast (40 ns peaking time), low-noise (ENC = 60e^- (RMS)) and low-power (2 μW per channel) front-end circuit can be implemented in a 0.13 μm CMOS technology.

Owing to the triple well layout used in the prototype, the sensitive analog inputs are effectively isolated from the high speed switching gates.

A new prototype featuring a TDC-per-pixel concept will be submitted at the end of 2006.

V. Acknowledgements.

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An Error-Correcting Line Code for a HEP Rad-Hard Multi-GigaBit Optical Link

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Abstract

This paper presents a line encoding scheme designed for the GBT ASIC, a transceiver under development for a multi-gigabit optical link upgrade of the TTC system. A general overview of issues related to optical links placed in radiation environments is given, and the required properties of the line code discussed. A scheme that preserves the DC-balance of the line and allows forward error correction is proposed. It is implemented through the concatenation of scrambling, a Reed-Solomon error-correction scheme and the addition of an error-tolerant DC-balanced header. The properties of the code are verified for two different interleaving options, which achieve different error correction capability at different implementation costs. One of the two options was implemented in a fully digital ASIC fabricated in a 0.13 μm CMOS technology, and ASIC implementation details and test results are reported.

I. INTRODUCTION

The Timing, Trigger and Control (TTC, [1]) system is responsible for timing distribution from the RF generators down to the experiments at the LHC. At the experiments, together with the LHC clock, level-1 trigger and control information are broadcast from a master transmitter to many receivers placed inside the detectors. In the framework of future luminosity improvements of the LHC, an upgrade of TTC system is under development. In the new proposed version the optical link becomes bidirectional and the transceiver ASIC is named GigaBit Transceiver (GBT). This new link profits from a new technology for the ASIC implementation which allows an important speed improvement. While in the present TTC 2 bits per 25 ns are delivered, corresponding to one bit reserved for level-1 trigger and one for control information, more than 60 bits are available in the new version. This allows the transmission of complex trigger information as opposed to the present 1-bit value, the protection of the whole packet through error-correcting (EC) schemes, the transmission of a whole control command every bunch crossing (whereas in the present system it takes many).

A line code is required to provide a relatively high number of transitions on the serial bit stream in order to facilitate clock and data recovery (CDR) and in particular for low jitter. Moreover, the data stream has to be constituted of roughly the same number of zeros and ones in order to allow for ac-coupling in the receiver. As in our application Single Event Upsets (SEUs) on the photodiode (PD) are likely to be the main source of errors, the line code proposed here includes an EC scheme particularly targeted to this issue.

We propose a line code that uses the concatenation of a scrambler, a Reed-Solomon (RS) EC encoder/decoder and the addition of an error-tolerant header used for frame synchronization. The scheme is proposed in two options which achieve slightly different EC capabilities. Details about each line code building block and the differences between the two options are explained in the third section of this paper, simulation results are given in the fourth section.

A demonstrator ASIC for the first option was implemented in a 0.13μm CMOS technology, its details are described in the fifth section of the paper along with test results.

II. OPTICAL LINKS FOR HEP EXPERIMENTS

A. Requirements for general purpose links

The scheme of a general purpose optical link is shown in Fig. 1 and summarizes what the fundamental components of the system are.

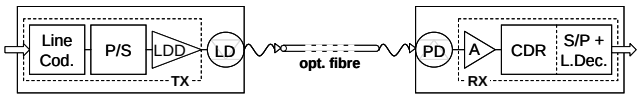

Figure 1: General scheme of an optical link. In the ASIC transmitter (TX), among other functions, line encoding and parallel-to-serial (P/S) conversion are performed. LDD is the laser driver and LD the laser diode. In the ASIC receiver (RX) amplification (A), CDR, serial-to-parallel conversion (S/P) and line decoding are performed.

The transmission of abundant timing information eases clock recovery circuitry design and operation, and allows the reconstruction of a low jitter clock. In a system based on non-return-to-zero data transmission, the timing information is contained in the level transitions between 1-bit values and 0-bit values. The abundance of these transitions is quantified by average and maximum run-length, that is the average and maximum length of strings constituted by identical values (zeros or ones). Additionally, the sequence of transmitted bits should not be periodic in order to keep pattern dependent jitter low. These requirements apply in particular to a system like the GBT on which the experiments rely for the precise delivery of the LHC clock and where the target jitter is as low as 20 ps rms.

The amplifying stages between the PD and the receiver have a high-pass response eliminating the low frequency content of the signal spectrum. For this not to distort the transmission, the data stream is required to have small low frequency content (i.e. DC-balanced data). This is equivalent to saying that the data should contain on average an equal number of zeros and ones on a time window with length proportional to the inverse of the low cutoff frequency.

B. *Additional requirements for HEP applications*

Optical links used in HEP applications have to be radiation resistant in order to be able to operate reliably in harsh radiation environments. The radiation hardness of the system is ensured through two approaches, one concerning the optical components and the other concerning the ASICs. When exposed to radiation, semiconductor laser diodes suffer a threshold shift, optical fibres "darken" (i.e. the attenuation increases) and PD responsivity decreases [2]. The optical components go through a thorough qualification process and an additional margin is built-in in the optical power budget. Concerning the electronic components, the effects can be classified into total dose effects and Single Event Effects (SEEs). The former effects can be minimized by adopting particular layout techniques (e.g. enclosed layout transistors, [3]). Concerning the latter effects, examples are single event latch-up and SEUs. Testing carried out on the technology to be used indicate that single event latch-up does not occur for the technology in use and the radiation levels expected at the LHC. SEUs are a concern for this technology, but ASICs can be made "SEU-tolerant" mainly by architectural and circuit techniques, e.g. by triple modular redundancy (majority voting) logic circuits [4].

Photodiodes are also sensitive to SEUs. Their function in the link is to detect light coming from the laser transmitter through the optical fibre. By means of the same physical principles, they also detect ionizing radiation. As no light detection translates into a 0-bit value, while light detection translates into a 1-bit value, ionizing radiation can in fact transform a logical 0 sent by the transmitter into a logical 1 detected by the receiver. Data transmission can be protected against such "fake signals" by implementing error correcting schemes in which the encoding is performed at the transmitter and the decoding at the receiver, i.e. after the PD. As SEE errors on the other components of the link can be easily dealt with, the proposed line encoding scheme addresses in particular the issue of SEUs on the PD.

Error cross-section studies for optical links components to be used in HEP or satellite environments were reported [5, 6, 7]. It is established that the major error cause is PD SEUs. The error probability decreases with an increase on the level of incident optical power, it increases with data rate and has a maximum when the angle of incidence between the particles and the PD is 0 degrees (i.e. grazing angle). Considering fluxes easily exceeding 10^6 particles s^{-1} cm^{-2} in the inner parts of the detectors at the LHC [8] and average reported error cross-sections of $10^{-6}cm^2$ [6, 7], a bit error rate of 10^{-10} can be estimated for the link under development. According to this bit error rate value, the probability of two error events falling in the same frame is 10^{-17} (Bernoulli trials, [9]).

Even though system performance depends highly on the launched optical power and the PD has not been chosen yet, the estimated bit error rate is not acceptable as it is (1 error/s per link), and thus EC capability has to be implemented in the system for reliable operation. At least single error event correction has to be included in the link in order to shift from the initial bit error rate value of 10^{-10} to 10^{-17} for double events (corresponding to 1 error per hour on 10000 links).

Low latency is fundamental in the GBT link as one of its functions is to deliver level-1 trigger information shortly after a collision event. This is a limiting factor in the choice of the EC scheme as many of the EC algorithms proposed in literature and utilized in commercial links are more computationally intensive.

III. LINE CODE ARCHITECTURE

The line code is designed to provide the data with the following properties: 1) a high number of transitions; 2) DC-balance; 3) non-periodicity; 4) frame synchronization capability; 5) high efficiency; 6) EC protection; 7) low latency (as only a time latency equivalent to few LHC clocks can be spent for line coding).

While the last two points are specified in particular for the GBT optical link, the previous ones are more general and of concern for many commercial links. For this reason, commercially adopted schemes were evaluated for our application, even though none of them is found fully compliant with our needs. The 8b/10b scheme [10] for example is difficult to combine with error-correcting codes while maintaining a good efficiency: single errors on the line are converted into bursts, which then require a strong error-correcting scheme, and consequently lead to a less efficient use of bandwidth. The 64b/66b scheme, used in 10G Ethernet physical layer (IEEE 802.3ae standard) could satisfy most of our needs apart from SEU tolerance.

The proposed line code utilizes a concatenation of three operations in order to get to a line data stream that complies with all the requirements stated before. As can be seen in Fig. 2, the data is first scrambled, then encoded through a RS EC scheme and finally a header is added for frame recognition. Inverting the order of scrambling and EC would result in error multiplication due to the scrambler, and this would consequently impose the need for a stronger EC scheme.

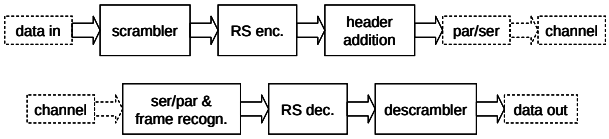

Figure 2: Block diagram of the proposed line encoding scheme: encoder diagram (top) and decoder diagram (bottom).

A. *Scrambling*

Scrambling [11] is a method of randomizing the statistics of a data stream. Some data patterns, as long strings of 1's or 0's, are commonly transmitted but problematic with regard to DC-balance and run-length issues. Through scrambling, these sequences are mapped to others which resemble closely real random data. This statistically guarantees DC-balance and a low average run-length on the scrambled bits.

A scrambler is typically implemented through an n-bit linear feedback shift register. Its output sequence is "pseudorandom", and for a constant input, the output has a period of 2^n-1. Thus higher n produces longer sequences.

In order to avoid the need for a synchronization code the scrambler is implemented as self-synchronizing. In this way, at the beginning of the transmission and in case of

synchronization loss there is no need to send a special synchronization code. As the TTC is currently implemented in a broadcast topology, self-synchronization is particularly effective since it allows a single receiver to reacquire synchronization without interfering with the operation of the other receivers. The implementation of a self-synchronizing scrambler and descrambler of length 63 is shown in Fig. 3.

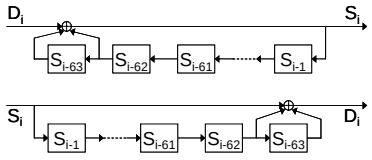

Figure 3: 63-bit scrambler (top) and descrambler (bottom). D_x is the user data and S_x is the scrambled data. The square blocks are memory elements; the sum is an exclusive-or operation.

B. Reed-Solomon error correction

RS codes [12] are linear cyclic block codes which treat groups of m bits, referred to as "symbols", as single entities. The correction of one symbol corresponds to the correction of all the m-bits that belong to it, making the codes very well suited for burst errors. Moreover, encoding and decoding are naturally implemented in parallel structures, allowing operation at a frequency that is m-times slower than line speed. The code construction is very flexible and they can be built to correct multiple errors. RS codes are also proven to be very efficient [12].

The chosen RS encoding scheme is systematic, i.e. the redundancy bits are appended without actually modifying the data word, so that the resulting RS encoded word after scrambling is still DC-balanced. Additionally, the pseudorandom characteristics of the data word are acquired also by the redundancy bits.

Once the width m of the symbol is chosen, the maximum number of symbols that belong to the same block is fixed ($N_{s,max} = 2^m-1$, or, in bits: $N_{b,max} = m\cdot(2^m-1)$), being the block the unit on which the error correction operation is performed. In the case of a 60-bit block, 15 4-bit symbols can be used. Also a shorter block length can be used if part of the available data space is considered filled by zeros. These in fact are not transmitted, but the feature is known at both ends of the link and used in the encoding and decoding algorithms, additionally allowing extra error detection. In the case above, if only 40 bits, that is 10 symbols, are needed out of 60, then 5 of 15 symbols can be zero-padded. If a number t_s of symbols needs to be corrected, then up to $(N_{s,max} - 2t_s)$ symbols in the block can be used for data information.

The encoding procedure is performed via a division operation which is implemented through a feedback shift register. The decoding operation is more complicated and is divided in steps: 1) detection of errors; 2) identification of the corrupted symbol and 3) identification of the corrupted bits within a symbol. The case of single error correction (i.e. $t_s = 1$) uses a simple and fast algorithm. Due to the latency requirements of the link under study, $t_s = 1$ is chosen. Decoding is then implemented through a feedback shift-register followed by multiplication and look-up operation.

In order to accommodate for the cases in which the SEU error event extends over 2 bits that might belong to different symbols, and in order to extend the error correction capability, interleaved blocks are used.

C. Frame delimitation

The addition of a header block is imposed by the need of synchronizing the data stream at the frame level. Repeated recognition of a valid header in a fixed position in the frame allows for frame-locking. Repeated non-valid header recognition causes loss of frame lock.

At the same time, different headers are required to distinguish different packet types, i.e. user data, trigger data or idle pattern. The patterns used for the headers are 6 or 8-bit long (depending on the interleaving option) and are chosen to be DC-balanced and redundant so that they are still recognizable even if corrupted by an SEU event.

D. Coding options

Our scheme proposes two interleaving options: one is based on 4-bit RS symbols and interleaving of two RS blocks, while the other one is based on 3-bit RS symbols and four-block interleaving. The first interleaving option is shown in Fig. 4 and the second in Fig. 5.

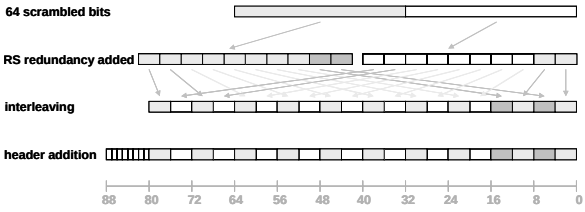

Figure 4: Modification of the data word through the line encoding building blocks, first option.

In the first option 64 user bits are first scrambled. Then two blocks of 32 bits each are RS encoded: 2 redundancy symbols (8 bits in total) are added to each of the two blocks, which are then interleaved. Last, an 8-bit header is appended, leading to a total frame length of 88 bits, a total link speed of $f_{bit} = 88\cdot40$ MHz = 3.52 GHz and an overall line code efficiency of 72.7%. The overall encoding process takes one $T_{FRAME} = 88\cdot T_{bit}$, while the decoding process takes 2 T_{FRAME}.

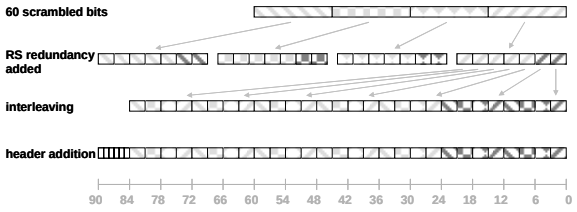

Figure 5: Modification of the data word for the second option.

The main differences between the two options are the number of interleaved blocks and the block widths. In the second option (see Fig. 5) first 60-bit data are scrambled, then four 15-bit blocks are RS encoded (24 redundancy bits are added) and interleaved. A 6-bit header is then added, for a total 90-bit frame, a link speed of $f_{bit} = 90\cdot40$MHz = 3.60 GHz and an efficiency of 66.7%. The overall encoding process

takes one $T_{FRAME} = 90 \cdot T_{bit}$, while the decoding process takes $2\ T_{FRAME}$.

The summary of the parameters for the two options is given in Table 1. In the table, m is the RS symbol width, L is the number of interleaved blocks, N_s is the number of symbols per RS block, out of which K_s are information symbols. N_b is the total number of bits after RS encoding, K_b of which are information bits. H is the header bit length and N_{tot} is the total frame bit length. The efficiency R is the ratio between the number of information bits and total frame length.

Table 1: Line code characteristics for the two presented options.

code characteristic	first option	second option
scrambler order n	63	60
m	4	3
L	2	4
N_s	10	7
$N_b = N_s L m$	80	84
K_s	8	5
$K_b = K_s L m$	64	60
H	8	6
$N_{tot} = N_b + H$	88	90
$R = K_b / N_{tot}$	72.7%	66.7%
$f_{bit} = 1 / T_{bit}$ (GHz)	3.52	3.6

IV. PROPERTIES OF THE PROPOSED CODING SCHEME

A. *Error-correction capability*

The proposed scheme allows correcting any single upsetting event per frame, even if the event extends over two consecutive bit periods.

Due to interleaving, additional error correction capability is obtained, so that independent double errors per frame can sometimes be corrected depending on the position in which they fall in the frame. The two errors can be tolerated if one falls on the header and one on the RS segment. In case the two errors fall on the RS segment, then two cases must be distinguished. If they fall in different RS blocks, they can be corrected. If they fall in the same RS block, but not in the same symbol, then they cannot be corrected and the packet is corrupted. Due to the choice of implementing the scrambler as self-synchronizing, this last case causes the frame that follows the corrupted one to be incorrect as well. Statistical calculations have been carried out to explore all different possibilities for two events falling in the same frame: the first interleaving option can correct 62% of them, while the second option can correct 81%. The first option though allows for additional error detection due to the use of zero-padding.

The line code error correction capability improves the link performance from an uncoded transmission BER α to a coded Frame Error Rate $FER = 3 \cdot 10^3 \cdot \alpha^2$ for the first option and $1.5 \cdot 10^3 \cdot \alpha^2$ for the second one. This corresponds to an improvement from $\alpha = 10^{-10}$ to FER = 3.8 errors/hour on 10k links for the first option or 1.9 err./h. for the second option.

B. *Implementation complexity*

A Verilog model for the two interleaving options schemes was written, simulated and synthesized using a commercial standard cell library. A comparison of the two options in terms of implementation complexity is carried out based on synthesis. In Table 2 the number of cells and power consumption of encoder and decoder blocks for the two options is reported. The results are based only on the blocks that perform scrambling, RS encoding/decoding and control logic. It can be concluded that the second option halves the error probability at the price of increased power consumption and decreased efficiency.

Table 2: RS code complexity for the two line code options. The power consumption is normalized to the value obtained for the encoder for the first interleaving option.

Module	Cell count	Power cons. (a.u.)
enc.1st option	1066	1
enc. 2nd option	1098	1.23
dec. 1st option	2794	2.04
dec. 2nd option	2402	2.56

C. *DC-wander simulation results*

Excessive DC-wander impacts on system performance by effectively closing the eye diagram. In order to verify the amount of DC-wander generated by this scheme, the high level model and the synthesized netlist were extensively simulated. The baseline wander behaviour is studied through a finite time step simulation of high-pass filtering the line data stream (at f_{bit}) with a 100 KHz cutoff frequency. Histograms of the obtained wander probability on 5 Mb data streams are plotted in Fig. 6 (top) for the first option and (bottom) for the second one. Different user data (random data, constant 0's and 1's, idle frames) show qualitatively the same wander, with means of the order of 0.01% of signal amplitude, and maximum sigma of 0.47%. These values for the DC-wander impact on the system by generating a BER well below 10^{-22}, consequently negligible with regard to other noise sources.

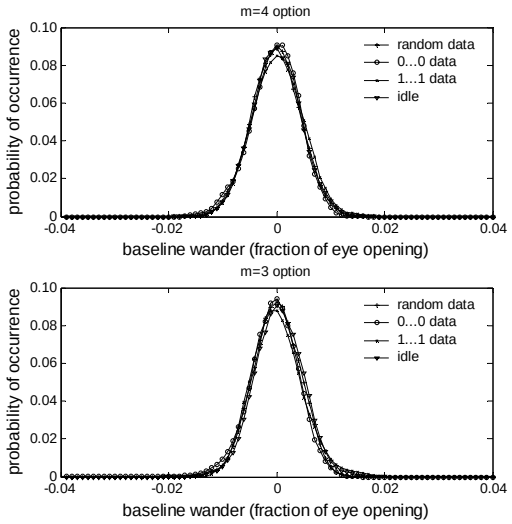

Figure 6: Baseline wander probability of occurrence.

Simulation results show that for both options of the proposed encoding scheme the average run-length is less than 2 bits as consequence of data scrambling, while the maximum run-length is strictly limited by the presence of the header to 80 bits for the first option and 84 bits for the second one.

V. DEMONSTRATOR ASIC IMPLEMENTATION

A. Functionality

A test chip for the first option of the encoding scheme was fabricated in a commercial 0.13 μm CMOS technology. Encoder and decoder are implemented according to the block diagrams show in Fig. 7. The 64 user bits enter the encoder bytewise due to pad number limitations. The data packet is then scrambled, the RS redundancy bits and the header are added and finally the 88-bit word is serialized and driven out of the chip. In the decoder the inverse process is implemented. First a frame synchronization block identifies the frame boundaries, then the word is checked for errors through the RS decoder, finally descrambled and multiplexed out in 8-bit groups. Data or idles can be sent, and scrambling or RS encoding can be bypassed for testability.

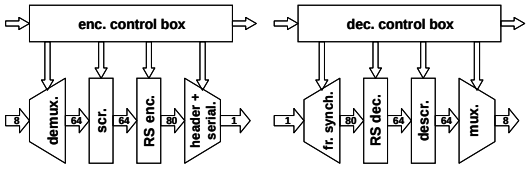

Figure 7: Block diagram of the encoder (left) and decoder (right) implemented in the ASIC. Details about control signals cannot be discussed due to space limitations.

B. Implementation details and test results

The whole encoder block utilizes 1700 cells for a power consumption of 25 mW/GHz, while the decoder block counts 5000 cells for a power consumption of 50 mW/GHz. The total area of the die is (1.3 x 1) mm^2, while the active areas are (0.15 x 0.35) mm^2 for the encoder and (0.35 x 0.35) mm^2 for the decoder. An image of the die is shown in Fig. 8.

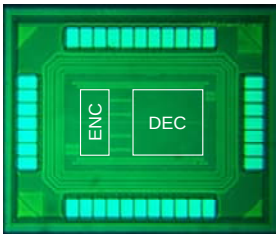

Figure 8: Picture of the die. The 36 bondpads and the power rings are visible around the encoder and decoder active areas.

Through a digital tester, test vectors can be applied to the inputs of the die via a board and socket interface. The die signal outputs are checked against vectors obtained from simulation and the correct operation of the ASIC can thus be verified. Test input vectors were applied to the encoder and decoder for verifying data or idle transmission while applying different control settings. In the decoder case, also data corrupted by errors were used to verify the operation of the error correcting circuitry. The encoder and decoder were additionally tested in back-to-back mode. The tests were carried out at frequencies below 50 MHz due to limitations imposed by the test board. All tests were successful. The power consumption measurement is in agreement with the simulated values. The ASIC implementation does not take into account radiation resistance of the ASIC itself, characteristic which will be dealt with in future work.

VI. CONCLUSIONS

We reported the study for a line code to be used in the GBT ASIC transceiver. The line code performs error correction while guaranteeing a DC-balance well below 1% of signal amplitude and average run-length of 2 bits. The code is based on the concatenation of scrambling, a Reed-Solomon error-correcting scheme and the addition of a DC-balanced error-tolerant header. Two different coding options are explored which correct all single upsetting events and different fractions of double events per frame, at different implementation costs. One of the two options was implemented in a fully digital 0.13 μm CMOS technology demonstrator ASIC for which implementation details and test results are given.

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Development of a CMOS SOI Pixel Detector

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Abstract

We have developed a monolithic radiation pixel detector using silicon on insulator (SOI) with a commercial 0.15 μm fully-depleted-SOI technology and a Czochralski high resistivity silicon substrate in place of a handle wafer. The SOI TEG (Test Element Group) chips with a size of 2.5×2.5 mm^2 consisting of 20×20 μm^2 pixels have been designed and manufactured. Performance tests with a laser light illumination and a β ray radioactive source indicate successful operation of the detector. We also briefly discuss the back gate effect as well as the simulation study.

I. Introduction

A monolithic radiation pixel detector with the SOI technology is one of the position sensitive detectors that are able to overcome the difficulties in decreasing the pixel size and thickness, and the bump bonding employed by a hybrid pixel detector. The SOI pixel detector consists of a monolithic Silicon layer (handle wafer) covered with a insulating SiO_2 layer (Buried Oxide, BOX), and a thin Silicon film (device layer) over the BOX, in which a readout LSI is formed. The handle wafer is used for a radiation sensor with a matrix of depleted diodes directly connected to the LSI through a hole in the BOX. The SOI structure enables us to use two different types of silicon, i.e., the high resistivity silicon handle wafer for the radiation detection and the low resistivity silicon film for the readout electronics utilizing CMOS transistors.

Transistors formed on the SOI wafer can operate with higher speed and lower power consumption compared with the conventional bulk CMOS processes because of less parasitic capacitance [1]. Moreover, the SOI transistors are free from the latch-ups since individual transistors are completely separated by the BOX layer and have no PNPN parasitic structure. The thin device layer is insensitive to Single Event Upsets and Transients [2] due to its small energy deposit by ionizing radiations. Those SOI characteristics can satisfy the requirements of further improvement of the spatial resolution and radiation hardness imposed by future particle physics, astrophysics and medicine.

We have developed the SOI pixel detector in collaboration with OKI Electric Industry Co. Ltd. [3]. The basic technology of OKI's fully-depleted 0.15 μm CMOS SOI process [4] is employed. Additional processing steps for the implants to the handle wafer and contacts to it have also been developed. Figure 1 shows a cross-section of the SOI pixel detector.

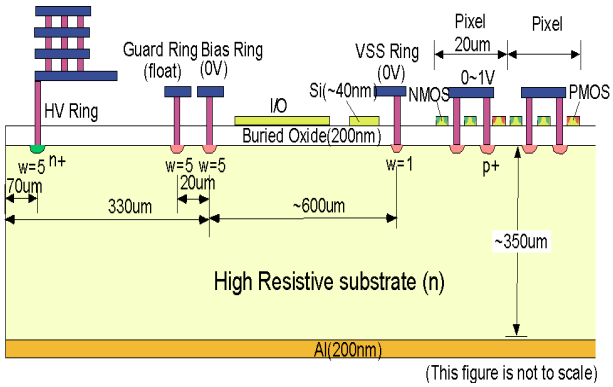

Figure 1: Cross-section of the SOI pixel detector.

II. The SOI process

The SOI wafer is provided by SOITEC which employs the smart-cut procedure for the production. The wafer consists of a high resistive Cz silicon handle wafer ($>$ 1 kΩ·m), a BOX layer with a thickness of 200 nm on the substrate and a p-type 50 nm thin Cz silicon film on the top in which transistors are formed. Since there is no original type assignment of the handle wafer and a possibility that the type could change during processing due to the thermal donor generation [5], we fabricated two kinds of TEG chips for p-type and n-type handle wafers.

The implantation of p+ and n+ to the handle wafer and the formation of transistor drain and source implantation on the silicon film are performed simultaneously with the carrier density of about 10^{20} cm^{-3} after opening holes in the BOX. This procedure can decrease the number of masks and process steps, and therefore costs. The implantation in the handle wafer is connected to a metal contact through the hole in the BOX. Three to five metal layers are formed on the silicon film for the circuit formation. Three different types of transistors are fabricated in the SOI process: high voltage transistors for I/O buffers, high threshold transistors utilized for normal logic and low threshold transistors used for high speed circuit. The pixel readout circuit employs the high threshold transistors with body ties.

The handle wafer having an original thickness of 650 μm is thinned to 350 μm, and its backside is plated with a 200 nm aluminum film. The detector bias can be applied from either the aluminum backside or pads on the top, both are connected to an n+ implant HV ring.

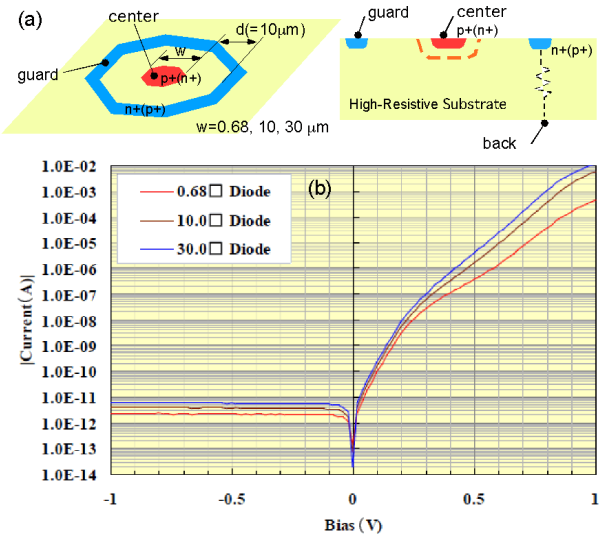

Figure 3: Measured I-V curve between p+ implant and the backside.

III. Diode TEG

To determine the handle wafer type prior to process pixel TEG chip, we fabricated diode TEG chips having p+ and n+ implant in the handle wafer. Figure 2 shows a TEM picture of the cross section of the p+ implanted diode TEG and metal contacts to the first metal layer. The measured sheet resistance of p+ (n+) implant is 136 (33) Ω/squre. The 0.16×0.16 μm^2 contact resistance is measured to be 218 (87) for p+ (n+) implant. We perform the I-V measurements for both p+ and n- implanted diode TEG. Figure 3 shows the curves of the diode TEG between p+ implant and the backside, indicating the diode characteristic and therefore the 'n' type handle wafer. We also measure the handle wafer resistivity with a four point probe to be 700 Ω·m, corresponding to the carrier density about 6×10^{12} cm^{-3}.

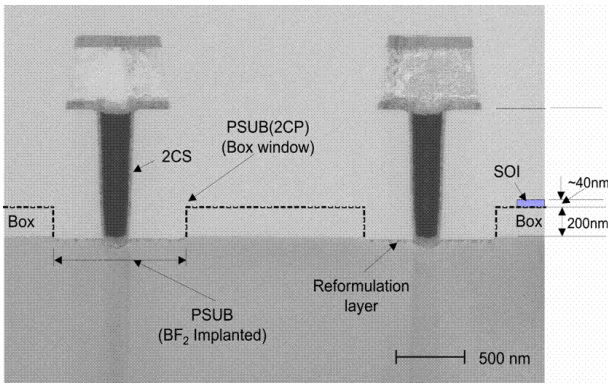

Figure 2: TEM picture of the cross section of the p+ implanted diode TEG and metal contacts to the first metal layer.

IV. Pixel TEG

The 2.5×2.5 mm^2 pixel TEG chip consists of a 32×32 matrix of pixels with a size of 20×20 μm^2. Figure 4 shows a picture of one pixel cell, which is composed of four 5.4×5.4 μm^2 octagonal p+ implants and a storage capacitor of 100 fF. The pixel center is opened for a light illumination test. The accumulated charge is read out using correlated double sampling.

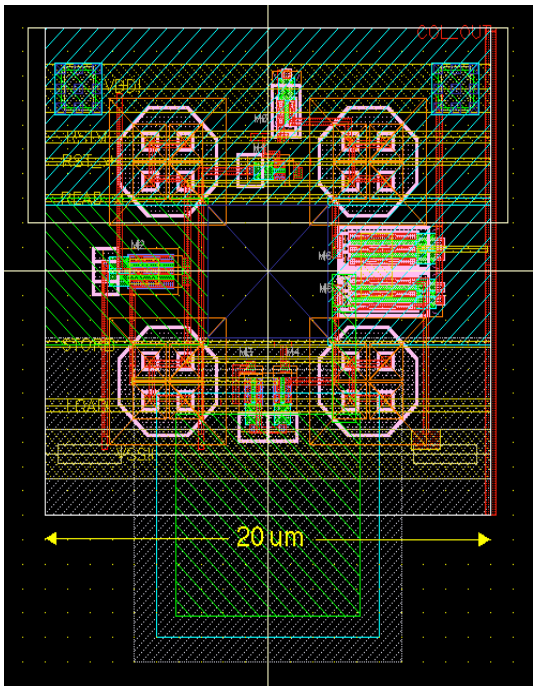

Figure 4: Picture of one pixel cell which is composed of four 5.4×5.4 μm^2 octagonal p+ implants and a storage capacitor of 100 fF. The pixel center is opened for a light illumination test.

Figure 5 shows a I-V measured curve of the pixel TEG, where the bias voltage is applied from the backside Aluminum cover. The same curve is obtained by applying the bias to the HV ring pad. The breakdown happens when more than 98 V is applied, where the depletion thickness is about 140 μm. Using an infrared camera we find that the breakdown is caused by a hot spot around the corner of the bias ring. This can be cured by smoothing the corner and moving the ring inward. However, there is a much lower bias voltage limit for the proper operation of the pixel TEG readout due to the back gate effect described in the next section.

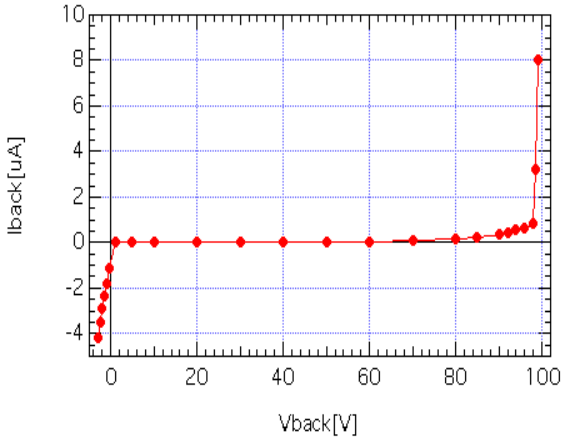

Figure 5: I-V measured curve of the pixel TEG.

We take a picture by illuminating red laser light (670 nm wavelength) with a plastic mask placed in front of the pixel TEG. We apply the detector bias of 10 V and expose it for 7 μs. Figure 6 shows an image obtained. From the size of the pixel window and the laser light intensity, we estimate the number of photons detected in the white part of the image to be 2×10^4; we expect 400 mV output signal height with 8 fF pixel capacitance. The measured signal amplitude is consistent with the expectation.

We also irradiate β rays using a ^{90}Sr source. Figure 7 shows an oscilloscope image of the pixel TEG output. The step in the picture indicates the β ray signal. The size is measured to be 70 mV, which is consistent with the estimated collected charge of 0.6 fC (3500e) with the depletion thickness of 44 μm and the pixel capacitance of 8 fF.

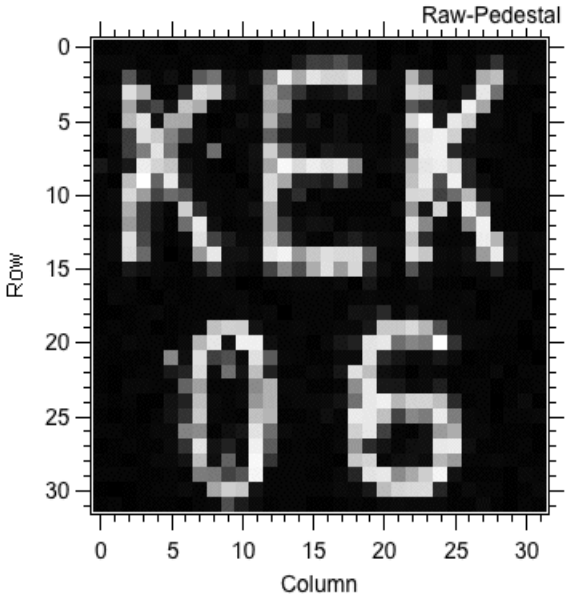

Figure 6: Picture taken using the pixel TEG with a red laser.

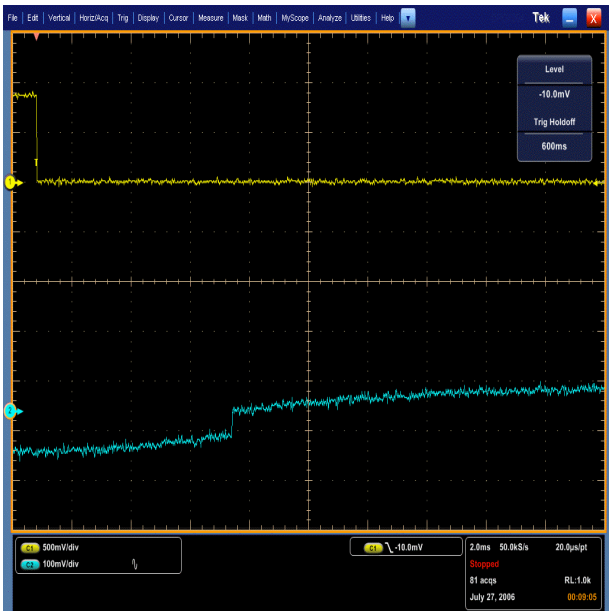

Figure 7: β ray signal in the oscilloscope image of the pixel TEG output.

V. Back Gate Effect

The transistors on the top Si film is affected by the potential level in the handle wafer, i.e. the transistor threshold voltage depends on the bias voltage applied to the handle wafer. Figure 8 shows measured threshold voltages of the three different types of transistors as a function of the bias voltage. The dependence is clearly seen, and the readout circuit is expected to stop its function with bias voltage more than 10 V. We confirm

this by observing the signal output of the I/O buffer. Figure 9 shows an oscilloscope image of the input and output signals of the I/O buffer. The output signal shape starts deviating when the bias voltage exceeds 15V. This behavior is also confirmed with a SPICE simulation.

Using a 3D TCAD simulation [6], we find that the back gate effect of an NMOS transistor can be reduced by implanting p+ in the handle wafer near the transistor position. We are optimizing the design and layout of the implant using the simulation.

VI. Summary

We have started development of the SOI pixel detector using a commercial OKI 0.15 μm SOI process and SOITEC wafer. We identify the handle wafer type as 'n' and find that its resistivity is satisfactory for the radiation detection. The pixel TEG has been fabricated and tested. Photo images are successfully taken and β ray signals are clearly detected. We find that the back gate effect can be removed by placing implantation near the transistors. The distance and shape of the implant is being optimized using the TCAD simulation.

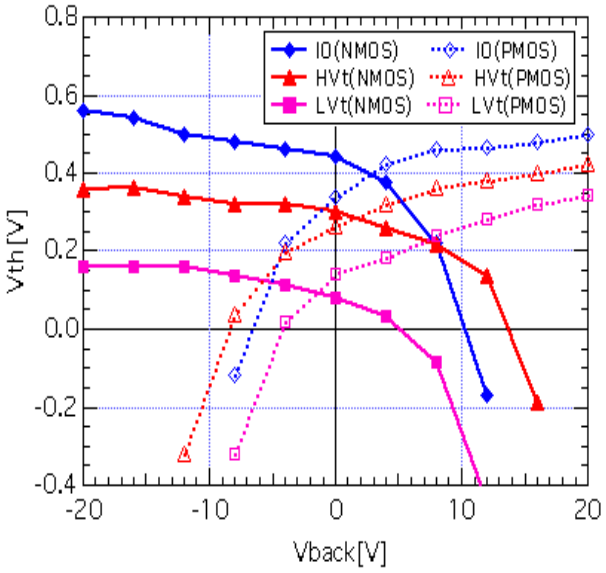

Figure 8: Measured threshold voltage (Vth) as a function of the bias voltage applied to the backside (Vback) for NMOS and PMOS transistors of three different types.

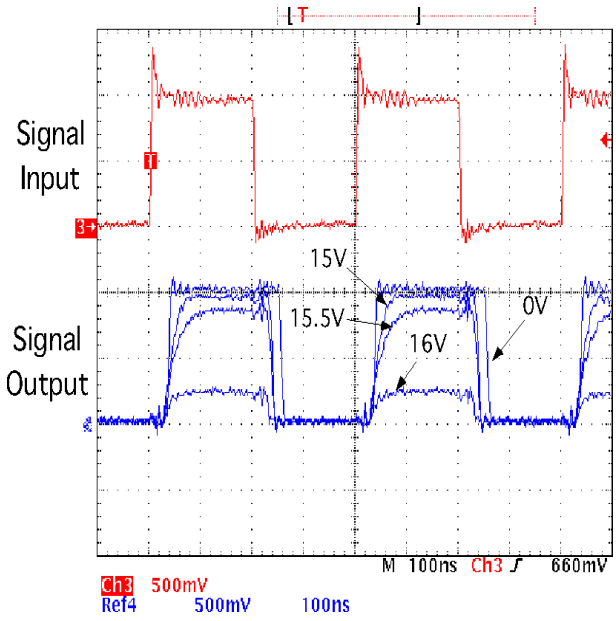

Figure 9: Oscilloscope image of the input and output signal of the I/O buffer. The output signal deviation becomes large as the bias voltage increases.

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Parallel Session B1

Trigger session 1

Integration of the CMS Regional Calorimeter Trigger Hardware into the CMS Level-1 Trigger

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Abstract

The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid Experiment (CMS) have been produced and tested. The RCT hardware consists of 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8-bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger (GCT) after processing.

Before installation, integration tests were performed. Data was successfully received from the TPG electronics and read out with a RCT Jet Capture Card. These tests, other tests involving more trigger subsystems, their results, and the RCT installation will be described.

I. Introduction

The Compact Muon Solenoid (CMS) is a general-purpose detector that will operate at the Large Hadron Collider (LHC). Its construction is currently underway at the European Laboratory for Particle Physics (CERN) near Geneva, Switzerland. This large detector will be sensitive to a wide range of new physics at the high proton-proton center of mass energy $\sqrt{s}$ =14 TeV [1].

At the LHC design luminosity of 10^{34} cm^{-2} s^{-1}, a beam crossing every 25 ns contains on average 17.3 events. These 10^9 interactions per second must be reduced by a factor of 10^7 to 100 Hz, the maximum rate that can be archived by the on-line computer farm. This will be done in two steps. The level-1 trigger first reduces the rate to 75 kHz, and then a High Level Trigger (HLT), using an on-line computer farm, handles the remaining rate reduction.

The CMS level-1 electron/photon, τ-lepton, jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [2]. The RCT plays an integral role in the reduction of the proton-proton interaction rate (10^9 Hz) to the High Level Trigger input rate (10^5 Hz) while separating physics signals from background with high efficiency. The RCT receives input from the brass and scintillator CMS hadron calorimeter (HCAL) and $PbWO_4$ crystal electromagnetic calorimeter (ECAL), that extend to $|\eta|=3$ (pseudorapidity η is $-\ln(\tan(\theta/2))$ where the x-y plane is perpendicular to the beam line defined by z). An additional hadron calorimeter in the very forward region (HF) extends coverage to $|\eta|=5$. A calorimeter trigger tower is defined as 5x5 crystals in the ECAL of dimensions 0.087x0.087 ($\Delta\phi x\Delta\eta$), which corresponds 1:1 to the physical tower size of the HCAL.

II. RCT Hardware

A. Primary RCT Cards

The RCT electronics comprises 18 crates for the barrel, endcap, and forward calorimeters, and another crate for clock distribution. These will be housed in the CMS underground counting room adjacent to and shielded from the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, two energy characterization bits, a LHC bunch crossing bit, and 5 bits of error detection code will be sent from the ECAL, HCAL, and HF calorimeter electronics to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on mezzanine cards, located on each of 7 Receiver Cards and the single Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the one mezzanine card located on the Jet/Summary Card is for receiving the HF data. The V7216-1 converts serial data to 120 MHz TTL parallel data, which is then deskewed, linearized, and summed before transmission on a 160 MHz ECL custom backplane to 7 Electron Isolation Cards and one Jet/Summary Card. The Jet/Summary Card receives the HF data and sends the regional E_T sums and the electron candidates to the Global Calorimeter Trigger (GCT). The GCT implements the jet algorithms and forwards the 12 jets to the Global Trigger (GT).

The Receiver Card (shown in Figure 1), in addition to receiving calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Synchronization of all data is done with the local clock and the Phase ASIC (Application-Specific Integrated Circuit--described below). The Phase ASIC also checks for data transmission errors. Lookup tables are used to translate the incoming E_T values onto several scales and set bits for electron identification. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

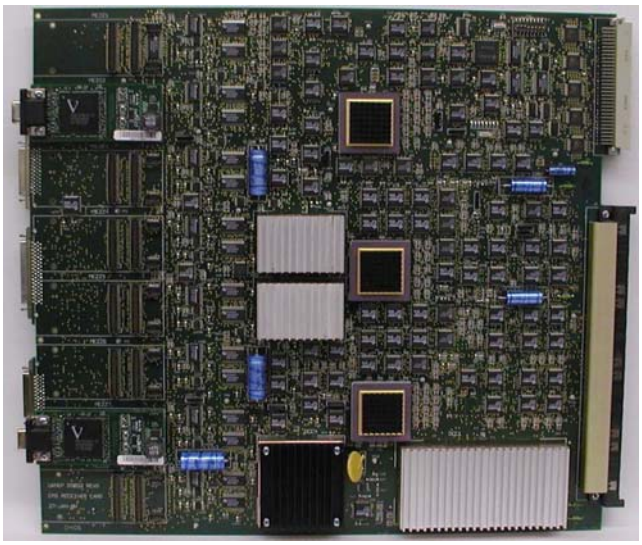

Figure 1: Front of a Receiver Card showing two Receiver Mezzanine Cards in place and Adder ASICs.

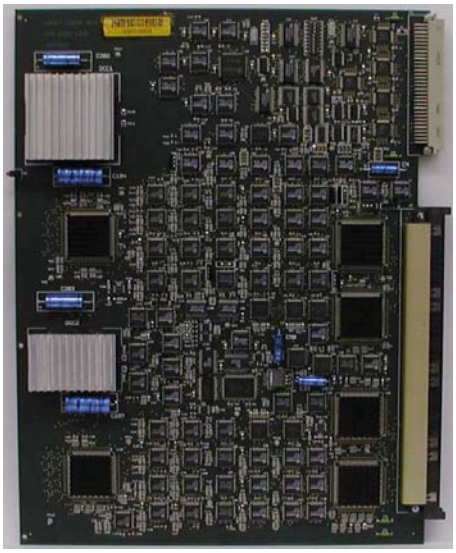

Figure 2: Electron Identification Card showing Sort ASICs and EISO ASICs.

The Electron Isolation Card (shown in Figure 2) receives data for 32 central towers and 28 neighboring towers via the backplane. The electron isolation algorithm is implemented in the Electron Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the Jet/Summary (J/S) Card. The electrons are sorted in a Sort ASIC on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing. The J/S Card also receives E_T sums via the backplane, and forwards them and two types of muon identification bits (minimum ionizing and quiet bits – described later) to the GCT. A block diagram of this dataflow is shown in Fig. 3.

To implement the algorithms described above, five high-speed custom Vitesse ASICs were designed and manufactured, a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an Electron Isolation ASIC [3]. They were produced in Vitesse FX™ and GLX™ gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the Receiver Card align and synchronize the data received on four channels of parallel data from the Vitesse 7216. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25 ns, while providing bits for overflows. The Boundary Scan ASIC handles board level boundary scan functions and drivers for data sharing. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the Electron Isolation Card. Sort ASICs are located on the Electron Isolation Card, where they are used as receivers, and are located on the J/S Cards for sorting the e/γ. All these ASICs have been successfully tested on the boards described below, and procured on in the full quantities needed for the system. The boards described have been produced using these ASICs and sufficient quantity has been obtained to fill 18 crates and create a stock of spares.

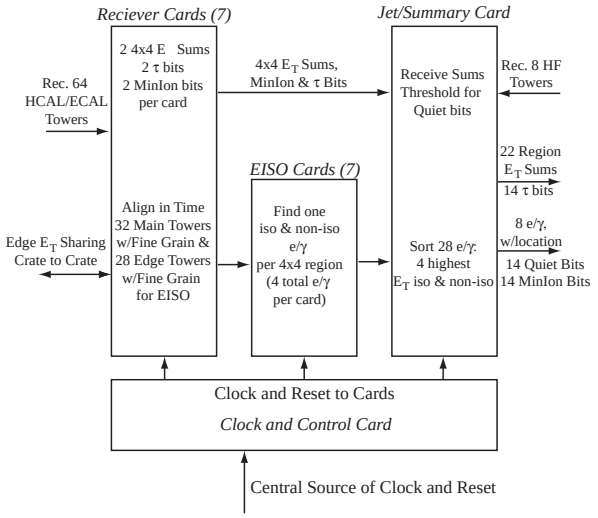

Figure 3: Dataflow diagram for the crate, showing data received and transferred between cards on the 160 MHz differential ECL backplane. Brief explanations of the card functionality are shown. For more details see the text or reference [2].

Currently in production is the Master Clock and Control Crate and cards. This crate will be centrally located among the 18 RCT crates and provide clock and control signal distribution. It includes a Clock Input Card (CIC), to receive the LHC clock, Bunch Crossing Zero (BC0), and CMS local control signals via an optical fiber to a LHC TTCrm mezzanine board [4], and to set the global alignment of the signals. This CIC will feed fan-out cards that will distribute the signals to the individual crates via low-skew cable. Delays on these cards will allow fine-tuning of the signals to the individual crates.

B. RCT Test Cards

For validation and production testing, two special test boards were developed to verify the input and output of the RCT. Versatility was built into the cards so that they may be used by other groups and in other situations at CMS.

The Serial Test Card (STC) was the first of these cards to be produced. It can be used in two ways. It can transmit data that mimics the input from the calorimeter Trigger Primitive Generators (TPGs). In this configuration they were used to validate the RCT Receiver Card links. Several cards were daisy chained together to produce 4 inputs to a RC. With this setup, all of the RC links and routes that could not be validated without active links were tested in a reasonable amount of time.

The STC can also be configured to receive data from an active link. A pair of cards, a transmitting card and a receiving card, was used to validate all the Receiver Mezzanine Cards. Additionally, the receive mode was used to validate the link board for the TPGs, the Serial Link Board (SLB), in another test stand.

The second test card, the Jet Capture Card (JCC) was developed to capture the output of the JSC in a variety of modes and if needed, generate an external trigger. It sits in the spare VME slot of an RCT crate, receives clocks and control signals from the CCC on two low-skew cables and data on six 68-pin cables from the JSC. Using the ability of the RCT to repeatedly cycle through its LUTs, it was possible to validate the data paths of a full RCT crate with changing patterns for an extended period of time. The capture feature was also used in integration tests described later in and the trigger feature will be exploited in the CMS Magnet Test and Cosmic Challenge (see below) [5].

III. Integration

A. Trigger Primitive Generators

The HCAL Trigger Readout (HTR) Boards and the ECAL Trigger Concentrator Cards (TCCs) provide the input to the RCT using a Serial Link Board (SLB), a mezzanine with the V2716-1 mounted on each type of card. The SLB is configurable, with two Altera Cyclone® FPGAs for data synchronization at the V2716-1, Hamming code calculation, FIFOs, and histogramming. The clocking for the SLB is separate from the HTR and TCC primary clocking to ensure alignment at the RCT. The HTR can have up to 6 SLBs and receives data from the front end on fibers into its front panel. The TCC has up to 9 SLBs and also receives front-end data via a fiber to its front panel.

B. Early Integration Tests

Before a CMS electronics integration facility was ready for use at CERN, integration had already begun at UW and at CERN. A single input cable was used, and the output and errors monitored with an oscilloscope for short runs to verify the designs and firmware of the HCAL Trigger Readout (HTR) boards, SLBs, and the RCT Receiver Card. These tests also evaluated a couple of new types of cable for the links, one of which proved to be the final choice for the system (Kerpen MegaLine® 8 [6]).

C. CMS Electronics Integration Facility

While the underground counting room was being readied, there was a pressing need for laboratory space to perform integration of electronics subsystems. For this an aboveground facility was built in an existing space at CERN. This facility has separate lab spaces with cable trays in-between and a row of racks outside of the labs identical to what exists underground at CMS, so ample space is available to integrate multiple trigger subsystems at the same time. The Regional Calorimeter Trigger was one of the first residents.

1) ECAL and HCAL TPGs

Initial tests with the HCAL HTR and ECAL TCC (Trigger Concentrator Card) were performed separately in the integration facility. Only a few cables were needed for initial tests of the input to the RCT so tests were done between the labs in the facility. Simple pattern data was sent from the HTR and TCC and the Jet Capture Card was used to verify transmission and alignment through the RCT. The RCT received all of this data on its HCAL input links, and used the functionality of the LookUp Tables (LUTs) and Adder ASICs on the Receiver Cards as a transparent way of reading out the results using the JCC attached to the JSC. The values of these regional sums were read out and the alignment of the data checked. Common clocking was done via a TTCvi (Trigger Timing and Control VME interface module) [4] located in the HCAL crate. Alignment of up to 6 links simultaneously was obtained and monitored for hours at a time.

After these successful tests, integration was moved to the integration row of the facility (See Figure 4 and Figure 5). This allowed ECAL and HCAL to send data simultaneously to the RCT, and use a clocking system with the same hardware as the CMS clocking system, the LTC (Local Trigger Control) [7] and 3 TTCci modules (CMS Trigger Timing and Control module) [7], one for each subsystem, the ECAL, HCAL, and RCT/SLB.



Figure 4: Front of the HCAL (right), ECAL (center), and RCT (left) racks at the integration facility. The top crate of the HCAL has the 19 cables attached to SLBs mounted on HTR cards. The ECAL rack has the TCC with SLBs and cables. The RCT has 6 cables (black) from the JSC to the JCC, and two cables (beige) from the CCC to the JCC.

One crate of HCAL HTRs sent data on 19 cables, and one ECAL TCC sent data on 9 additional cables (Figure 5). In this way, the links were run for extended periods of time and debugging of intermittent problems became possible. After long-term stability tests proved successful, this setup

was also used for firmware evaluation, software development, and continuing integration work.

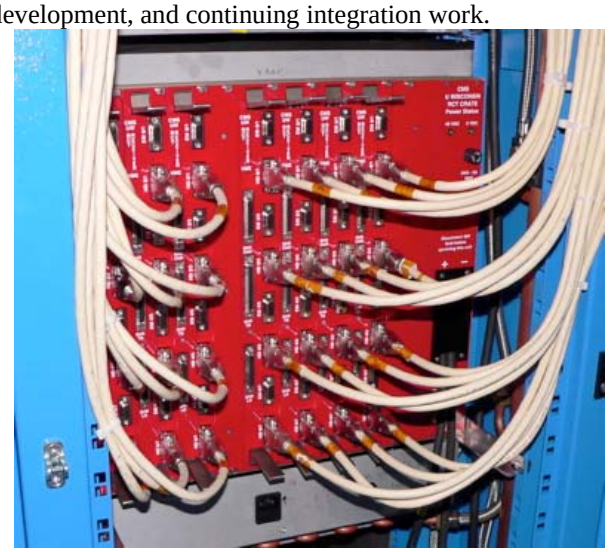

Figure 5: Rear of the RCT rack showing the 28 cables as input to 7 Receiver Cards. Half of the links were used.

2) Global Calorimeter Trigger

On its own, the RCT is able to generate the equivalent of 64 LHC bunch crossings of pattern data by cycling addresses of its Receiver Card LUTs. This functionality was used to test the interface with the Global Calorimeter Trigger (GCT), the Source Card. In its final form, the GCT will receive the differential ECL output of the 18 RCT JSCs. In total 66 Source Cards will receive 108 68-pin cables with regional sums, e/γ candidates, muon and τ bits and use this data to find jets, calculate global quantities, and find the four highest energy e/γ candidates of each type, isolated and non-isolated.

Long-term tests were performed successfully using two RCT crates synchronized with each other. The synchronization was achieved using a prototype RCT Master Clock Crate and Clock Input Card and a single TTCci with optical fan-out as the clock source for both the RCT and the GCT.

3) Preparations for the Magnet Test and Cosmic Challenge

In summer and autumn 2006 the CMS barrel rings and endcap disks, along with parts of the muon system, ECAL, HCAL, and tracker were used to understand the magnetic field and perform a "slice test" of the CMS DAQ system. The Magnet Test and Cosmic Challenge (MTCC) included the trigger systems. In order for the RCT to be used as part of the trigger in the second phase (autumn) of the MTCC, it was necessary to use the Jet Capture Card's capability of sending a trigger out. This required testing with two different systems.

One, the Global Trigger, would receive two trigger signals at its Pipeline Synchronization Board (PSB) and perform logic on the board using its FPGAs. For this, synchronization with orbit structure of the LHC was required. Therefore, the RCT used the pattern generation capability of the ECAL TCC to send predictable data via its links, which was used to create up to 2048 four-bit JCC trigger patterns for every LHC orbit. The patterns were provided to the Global Trigger, and they were able to verify that the data was coming over the link.

The other, the LTC, part of the CMS TTC system, can receive LVDS inputs and record them as part of its readout. Again, the ECAL was used as input and a JCC trigger signal out was sent to the LTC once per orbit. The rate, determined by the LTC software, was matched to BC0 rate, and was identical, so the test was determined a success.

4) Future Tests at the Integration Facility

Currently in the planning stage is a long-term test to study the software trigger emulators and test the algorithms of the RCT. The RCT LUTs can be programmed to duplicate incoming data. This will be set up and the RCT trigger emulator will be used to predict the outputs of the RCT. The HTR emulator will also be tested, and all of this will be done using a CMS software package for trigger control, the Trigger Supervisor [8]. This test will be done using two RCT crates and two JCCs and take place in October.

D. HCAL TPG to RCT in MTCC

As part of the second phase of CMS Magnet Test and Cosmic Challenge, the RCT has installed a crate and all support in the counting house for the MTCC. Data comes from the HCAL barrel HTRs (Figure 7) and 56 links are connected at the rear of the RCT crate (Figure 8). The desired trigger is a coincidence between the HCAL top barrel and HCAL bottom barrel. In order to separate these paths, the cables from the HCAL top goes to the HCAL inputs of the RCT, and the HCAL bottom cables go to the ECAL input of the RCT. A special LUT configuration allows the paths to remain separate, and produces two separate ORs performed by the RCT with its JCC. These two signals come out of the JCC and either go to the LTC via small logic board to perform an AND of the two signals, or directly to the GCT PSB, where the AND is performed internally.

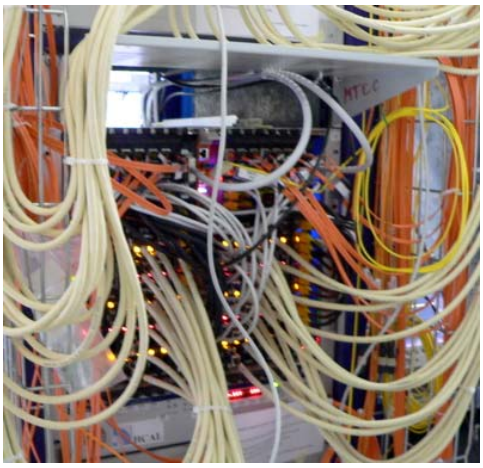

Figure 6: Cables to the RCT (beige) from the crate with HCAL HTRs for the bottom of the detector.



Figure 7: Cables into the RCT in the MTCC counting house.

The crate is ready and the links have been checked. The MTCC will restart in early October.

E. Integration Underground at CMS

Many of these tests will be expanded when trigger subsystems move to the underground counting room. As part of the commissioning process, it will be necessary to verify if all of the 1026 links to the RCT are attached, their (correct) location, and their long-term stability. In addition, after any board swaps or repairs, software tools are needed to recheck the connections. It is also expected that between LHC fills, tests will be run to help diagnose and find any problems that developed during running.

IV. Commissioning

A. Commissioning Underground at CMS

Installation has begun underground at CMS. The RCT has been allocated 10 racks that will hold a total of 21 RCT crates, 6 Global Calorimeter Crates, and a Clock crate for the HCAL. Nineteen of the RCT crates will be used as part of the final system. This includes a Master Clock Crate and eighteen of the 20 standard RCT crates. Two of the RCT crates will be used for local testing and powered storage.

1) Rack Infrastructure Installation

In late July, as soon as the underground counting room was deemed "ready for crates" a team from Wisconsin arrived to install the rack infrastructure and crates without cards. This included the installation of a custom rack monitoring system. This system, at the heart of which is a Rack Monitor Card, monitors the status of the power supplies, fans and crate temperatures. A serial port on the card is attached to a serial-to-ethernet connection. PVSS [9], an object-oriented process visualization and control system, is being used for the software interface to the Rack Monitor Card. This will enable remote monitoring and control of the racks and crates.

2) Card Installation

In October the RCT cards will be installed. Cards are shipped as pre-tested sets (16 different cards to a crate). Before installation in the crates, the cards will be checked out at the electronics integration facility, using the JCC and a crate self-test. This is repeated again in the underground counting room. To expand the scope of these self-tests, a program of sharing tests using the Master Clock Crate, data-sharing cables, and JCC is in development. This will check all of the inter-crate paths over cables and ensure clock distribution to the crates has been done correctly. In addition, the cables from the HTR and TCC SLBs will be installed and the links validated with expanded versions of previous tests above ground.

V. Conclusions

The integration and testing of the Regional Calorimeter trigger has expanded our understanding of the hardware and the subsystems that we connect to, the HCAL HTR, the ECAL TCC, and the GCT. It has led to improvements in the hardware and the firmware of the subsystems. As integration continues in the MTCC, and during installation underground, lessons learned will help provide a robust RCT for the turn-on of the LHC in 2007.



Figure 8: RCT Racks underground with crates and infrastructure. No boards have been installed yet.

VI. References

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The CMS Global Calorimeter Trigger Hardware Design

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Abstract

An alternative design for the CMS Global Calorimeter Trigger (GCT) is being implemented. The new design adheres to all the CMS specifications regarding interfaces and functional requirements of the trigger systems. The design is modular, compact, and utilizes proven components. Functionality has been partitioned to allow commissioning in stages corresponding to the different capabilities being made operational. The functional breakdown and hardware platform is presented and discussed. A related paper discusses the firmware required to implement the GCT functionality.

I. Overview

The CMS Global Calorimeter Trigger (GCT) is an integral portion of the CMS trigger system [1]. Its function is to receive and process data from all 18 Regional Calorimeter Trigger (RCT) crates and send the highest ranking electron and jet triggers to the Global Trigger, where they are used for generating the First Level Trigger Accept (L1A) decision. This system has been designed to be modular in design as well as commissioning. Due to a compressed development schedule, it borrows heavily from existing designs.

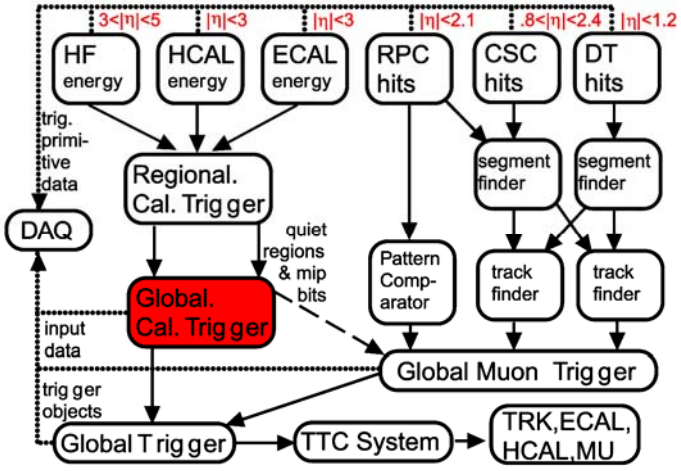


Figure 1: GCT's position in the CMS Trigger system

The GCT is composed of four module types, the Source, Leaf, Wheel, and Concentrator cards.

Source cards receive input directly from the RCT crates, and transmit the data via multi-Gigabit optical links to the GCT crate. They are located in the same racks as the RCT, and provide differential ECL to high speed serial conversion. In addition, they provide a means of data capture and readout for the RCT.

The Leaf cards are configured to receive either electron or jet trigger data on high speed optical fibers. Each electron leaf card processes the electron data from 9 RCT crates, selecting the four highest energy candidates for further processing. Similarly, the jet leaf cards process data from 3 RCT crates, and forward the 4 highest energy jets to the Wheel cards. However, the jet finding algorithm implements a sliding window – which requires data from adjacent RCT crates (corresponding to adjacent physical areas on the detector). Jet leaf cards are linked to their neighbours in a corresponding fashion to facilitate this algorithm.

The Wheel cards are only used for processing jet data, and combine the output of 3 Leaf cards. These 3 Leaf cards process the data from 9 RCT crates, or ½ of CMS. The Wheel cards sort the jets generated by the Leafs, and forward the 4 with the highest energy to the Concentrator.

The Concentrator card accepts data from 2 electron Leaf cards and 2 Wheel cards. It performs the final sorting of both electron and jet events, and sends the 4 highest energy candidates of each type to the Global Trigger. In addition, it provides a VME interface (slow control interface), and S-link data acquisition interface for the entire system.

II. Requirements

The primary requirements of the GCT are to sort electron triggers, and generate and sort jet triggers. The design has been optimized for these tasks. Secondary requirements include jet trigger counters, total jet transverse energy trigger, total transverse and missing transverse energy trigger, luminosity monitoring, and RCT readout. An in-depth discussion of all the GCT requirements is far beyond the scope of this paper, and are covered in detail in the CMS Trigger TDR [1] and several subsequent CMS internal notes [2,3]. The focus here will be on the primary requirements which have driven the hardware architecture.

A. Jet Trigger

The primary driver of the GCT hardware design is the need to find and sort jet triggers in the RCT data. The GCT jet finder uses a 3x3 sliding window (12x12 trigger towers) to search for patterns of energy deposition consistent with jets. This sliding window requires a contiguous data space, crossing the data boundaries of RCT crates. This implies a data sharing scheme within the GCT that matches the physical configuration of the detector. The detector data is processed by the RCT in 18 longitudinal sections, each ½ the length of the barrel and spanning 40degrees in phi. Since the data space spanning the center of the detector (eta 0) must be contiguous

as well, a similar sharing scheme needs to be implemented between the center sections of each ½ barrel. Once identified, jet objects need to be sorted by Et. The 4 highest energy candidates are forwarded to the GT.

B. Electron trigger

In comparison to the jet trigger, the electron trigger is straightforward. The RCT implements a sliding window algorithm similar to the jet algorithm described above and forwards 4 candidates (highest Et) of both isolated and non-isolated electrons. The electron trigger candidates simply need to be sorted and the 4 highest energy candidates sent to the GT.

C. Latency

The GCT has a limited amount of time to accomplish its task of jet identification as well as jet and electron sorting. This is driven by the limited storage in the front end electronics, which can store data from 128 events (which corresponds to 128 40 MHz clocks). The entire trigger process needs to complete in this time period, and the GCTs allocation has been defined as 24 40 MHz clocks.

III. High Level design

The GCT is a large data processing system, which needs to interface directly to 18 high power ECL crates spanning an entire row of racks located on a different floor or the CMS equipment area. RCT output data needs to be collected and concentrated for efficient transport and processing. The processing of the data needs to highly parallelized and as efficient as possible. In addition, the design is subject to extreme schedule pressure, and needs to be modularized to both reduce risk and allow efficient parallel efforts in both the hardware and software teams. Lastly, the compressed schedule demanded that the design be based as much as possible on existing modules.

A. Basic design Methodology

Due to the compressed schedule, it is critical to reduce risk by designing conservatively. In the GCT this has taken the form of data transfer rates that are well within the capability of the chosen technologies and minimizing the number of FPGAs in the processing chain. While the reasoning for conservative data transfer rates is obvious, reducing the number of FPGAs may not be. It is well known that the cost of FPGAs is not linearly related to their capacity – so it is almost always less expensive to design with multiple smaller devices than one large one. However, such designs usually have a much higher firmware risk. This is due to difficulty of accurate simulation, poor partitioning efficiency by synthesis tools, and the additional delays introduced when moving data between chips. This additional firmware risk can be substantial, and easily offsets the lower hardware cost in low production or one of a kind systems.

B. Data Transport and Concentration

Interfacing to the RCT system involves several challenges. Electrically, its output is differential ECL, and the data format is not DC balanced. This implies maintaining an accurate ground reference to 18 ECL crates, which are consuming over 10KW of power. In addition, the data is presented on a total of 108, 68 pin cables. Simply providing panel space for these connectors can be a problem. To provide both electrical isolation and concentration it was decided to build a data transport card, utilizing multi-Gigabit serial optical links to transport the data from the RCT racks to the GCT. Each 68 pin cable is replaced by two fibers, allowing a very high data density input to the GCT. This data transport and concentration card is known as the source card, and was derived from the IDAQ data acquisition module designed by Imperial College (UK).

C. Processing

The RCT produces a massive amount of data corresponding to over 233 Gbps. To process this amount of data, a hardware based signal processing system is required. In addition, much of this data needs to be shared (locally) within the system, so concentrating as much data as possible in individual processing elements is highly desirable.

A processing module was design to meet this requirement, based on the largest and fastest Xilinx FPGA with embedded Multi-Gigabit serial links available. While these devices are quite expensive, they provide a high level of integration and unmatched data density. This reduces risk in both the hardware design and firmware development. Two of these devices (Xilinx Virtex2Pro70s), which support 16 serial links each, were designed into a module with multi channel fiber receivers to support a total of 32 links on a double PMC. This processing module is known as the Leaf card, and was derived from a satellite processor prototype designed by Los Alamos Laboratory (US).

The most elegant design for the GCT would consist of a chain of these processing modules, each processing and sending serialized reduced data to a following layer. Unfortunately, there is a latency cost involved in serializing and deserializing data, and the integrated deserializers in FPGAs are particularly inefficient. In the case of the GCT, only one level of data concentration by serialization can be tolerated if the latency budget of 24 clocks is to be maintained. The remainder of the processing, which consists almost entirely of sorting, is accomplished by large (9U VME) carriers with wide parallel interface busses.

Two types of carriers have been designed, corresponding to primary jet trigger sorting, and electron and final jet trigger sorting. These are new designs developed by the GCT team at CERN, and have been designed to be compatible with the existing ECAL backplane design.

The primary jet trigger sorting carrier is known as the wheel card, and it supports the unique requirements of the jet finder algorithm. The data from 9 RCT crates that cover ½ the detector barrel is processed by 3 Leaf cards arranged in a ring topology. Each Leaf card shares data with its neighbours, providing the contiguous data space required by the jet finder algorithm. A second set of three Leaf cards is required for the remaining ½ barrel. To provide the required overlap between the two barrel halves, data from the first 2 regions in eta for each ½ barrel (the central region of the detector) is duplicated

and sent to the opposite side for processing. Each wheel carrier supports 3 Leaf cards, and processes jets from ½ of the detector. The wheel receives the jet objects from 3 Leaf cards and sorts them by energy. The resulting data is sent to the concentrator over 3, 80 pair differential cables.

The last stage of the GCT processing chain is the Concentrator card, which directly supports the two Leaf cards required for electron sorting, and receives data from two wheel cards for final jet sorting. In addition, the Concentrator provides interfaces to the GT, the data acquisition system, and slow control (VME). While algorithmically simple, the Concentrator is a complex design involving multiple system interfaces.

D. Overall System

The overall GCT system consists of the four types of modules discussed. There are 54 Source cards, 8 Leaf cards, 2 Wheel cards and one Concentrator card in the final system. A high level block diagram of ½ the GCT (which is symmetric), is shown in figure 1.

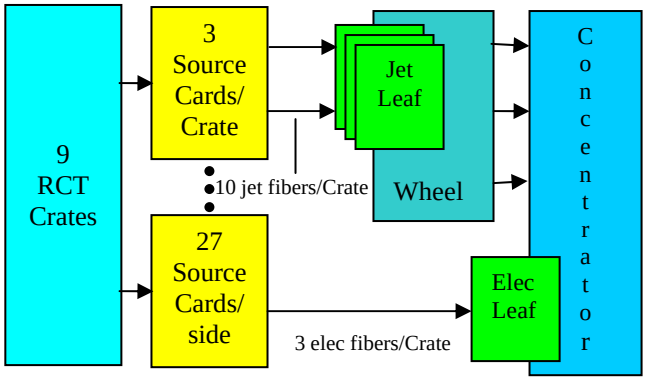


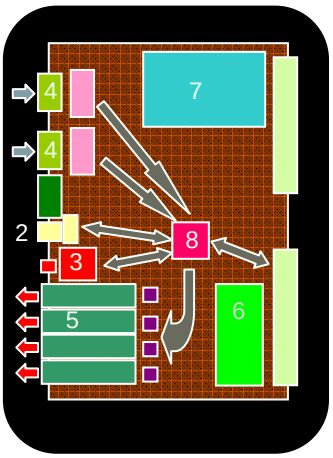
Figure 2: ½ GCT

IV. Source Card

The Source card is responsible for receiving data from the RCT, and transmitting it to the Leaf cards for processing. In addition to this primary function, it is also used to capture RCT data for diagnostic purposes. Each Source card interfaces to two RCT input cables, and 4 optical fiber outputs. A CMS standard TTCrx is used to reclock the RCT data and check synchronization. The Source card is implemented in a 6U VME format, and multiple sets of Source cards are housed in VME chassis installed in the RCT racks.

The IDAQ data acquisition card developed by Imperial College was the original choice for the source card function. However, due to the number of cards required in the final system, a simplified design derived from the original IDAQ with only the required functionality was implemented. This retained most of the support software and related firmware, as well as many components and general design elements.

The Source card logic is implemented in a single Xilinx Spartan 3 FPGA (3S1000), which performs all the data routing and readback functions. Data serialization is accomplished by 4 TI TLK2501 SERDES devices, which also handle the 8B/10B encoding to insure a DC balanced data stream. Optical outputs are provided by 4 standard SFP modules, in this case Agilent HFBR-5720AL devices. The Source card prototypes have successfully completed testing and are waiting on Leaf card availability for final link tests.



1. 10-layer 6U VME form factor
2. USB 2.0 (Cypress SX2)
3. TTCrx & QPLL
4. 2xVHDCI SCSI for RCT input
5. Optical SFP output & SERDES
   - TLK2501
   -Agilent HFBR-5720AL
6-7. Power supplies
8. XC3S1000-5FG676C

Figure 3: Source Card Block Diagram

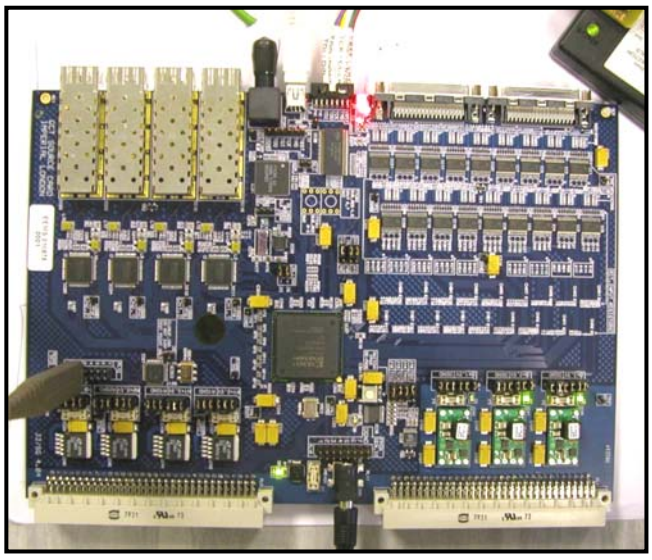


Figure 4: GCT Source card

V. Leaf Card

The Leaf card is the main processing module in the GCT, and is used for both jet and electron triggers. It can also be used for data snapshots of individual RCT fiber inputs, and to generate test data for Wheel and Concentrator verification.

The processing capabilities of the Leaf card are driven by the requirements of the jet finder algorithm. This algorithm, described in a related paper [4], requires that the data from an entire RCT crate, plus a portion of its neighbours, be available to search for patterns of energy deposition consistent with jets. The logic footprint of the search operation, which is highly parallelized, is more than 3 million gates. In addition, the jet data from a single RCT requires 8 optical links at 1.6 Gbps to transport. The most efficient implementation of this algorithm is to tightly couple adjacent jet finders, preferably in the same chip. The Leaf card design is an attempt to balance the maximum density of multi gigabit optical inputs

and available hardware processing power required to perform this task.

Practical matters of design and schedule risk heavily influenced the choice of processing components and form factor of the module. Early on it was recognized that it would be optimal for the processing FPGAs to have integral high speed serial links, as opposed to external deserializers. The internal devices are far more power efficient, and the intimate connection to the processing fabric of the FPGA gives considerably more design flexibility. Xilinx V2P70 devices were chosen as the best fit for density of high speed serial interfaces and logic capacity. Devices of this size require a reasonable amount of support on the PC board in the form of multiple high current regulators, filtering networks, and precision clock networks. Designing such systems capable of supporting the FPGA near the limit of its performance is a non trivial effort. Fortunately such a design existed in double PMC, a satellite processor prototype (a digital channelizer) designed at Los Alamos Laboratory. This device hosted two of the largest Virtex2 FPGAs and external serializers, and had been verified under high load conditions. A lesson learned from this previous design was that the designs power density (~60W) on a double PMC could not be easily pushed higher. Achieving the required density of fiber optic inputs was not possible with standard SFP modules. Moving to another industry standard, SNAP-12 MFP, provided a good match between serial ports available on the V2P70 and available front panel space.

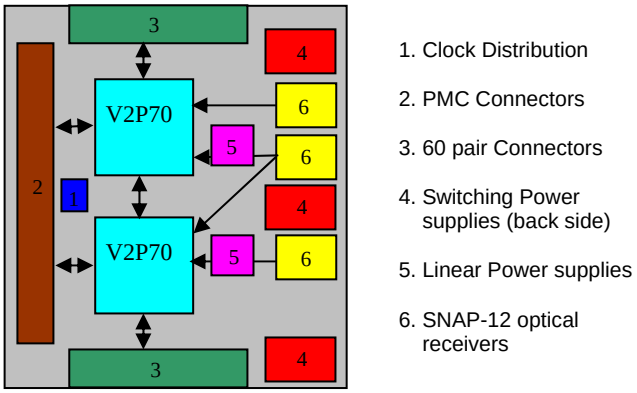


Figure 5: Leaf Card Block diagram

The Leaf card is implemented with 2 Xilinx V2P70 devices, and 3 SNAP-12 MFP optical receiver modules on a modified double PMC form factor. In order to facilitate sharing of data between adjacent jet Leafs, each card supports a 60 pair LVDS connection on the top and bottom edge of the card. The differential clock tree includes a high stability local 80MHz reference as well as multiple inputs from both PMC and micro coaxial connectors. The power supply system includes both phase controlled switchers for FPGA logic and linear regulators for the high speed serial links. The Leaf also includes two flash PROMs to configure the FPGAs, which are configured in a single JTAG chain which is jumper selectable between a header and the PMC connectors.



Figure 6: Leaf card

VI. Wheel Card

The Wheel card carrier is used to support three Leaf cards for jet processing and each Wheel processes the data from ½ the detector barrel. The Wheel card is functionally straightforward, sorting the jet objects found by the Leafs, and forwarding them to the Concentrator for the final sort. It also supports the slow control, synchronous trigger, and JTAG interfaces to the Leaf cards. The main design challenge on the Wheel was to manage to large number of parallel busses required to transport the jet object data to the sorting FPGAs, where pin limitations drove the selection of large Xilinx V4LX100 devices. In this case, the desire to be conservative in bus speed complicated the hardware design, since the design point of 40 MHz DDR directly relates to the number of I/O pins required. Experience with the Leaf has shown that 100 MHz can be safely transferred through the PMC connectors, so it is likely that the system is considerably over designed.

The Wheel card is implemented as a double wide 9U VME PMC carrier, with a total of 3 double PMC sites (two on the front and one on the back). The Wheel card is compatible with the existing custom 9U backplane used for CMS ECAL. The jet object sorting is handled by one Xilinx V4LX100, and energy summation and control by a second V4LX100. Communication to the Leaf cards is via the PMC connectors, which are fully connected to the FPGAs. A fully differential clock distribution system is implemented, which provides local 40 and 80 MHz clocks (generated by a QPLL), and external clock inputs from the Concentrator. The Wheel communicates with the Concentrator via 3, 80 pair differential cable assemblies. Once again, the design is perhaps over constrained here. The data rate is defined as 40 MHz DDR, but the cables, connectors and electronics are rated for over 4 times this. The JTAG chain, which can include all Leaf cards as well as the local FPGA and associated PROMs, is controlled by a dedicated CPLD, with manual front panel configuration. This allows each Leaf and Local FPGA to be independently added to the chain, and also selects either a front panel header input or a link to the Concentrator.

VII. Concentrator Card

The Concentrator Card is the heart of the system, and where all final sorting of jet objects and electrons is done. It carries the electron sorting Leafs directly on two double PMC sites, and interfaces to two Wheel cards via 3, 80 pair differential cable assemblies each. Output to the GT is provided on a double PMC site which houses a multi channel serializer compatible with the receivers on the GT. The Concentrator also provides the system VME, Slink DAQ, and synchronous timing (TTC) system interfaces. As on the Wheel card, the main design challenge is managing all the large parallel busses required to pass the electron and jet object data at 40 MHz DDR. Once again, the desire to be conservative in data rate complicated the hardware design significantly.

The Concentrator is implemented as a double wide 9U VME PMC carrier with three double PMC sites, two on the front and one on the back. It is also compatible with the CMS ECAL backplane. Electron and jet object sorting is handled by two Xilinx V4LX100 FPGAs. The VME and DAQ interface is provided by a Xilinx 2V3000 FPGA. The selection of large vitrex 4 devices was driven by pinout requirements of the data busses, and these devices are only lightly used to implement the sorting function. A fully differential clock tree is provided which includes a QPLL driven by a TTCrx, which is intended to be the timing reference for the entire GCT system. Both 40 and 80 MHz clocks are fanned out differentially to each Wheel and all PMC sites. The JTAG chain is controlled in a similar manner as the Wheel, with a CPLD controlling a segmented chain. The JTAG chain is also accessible by software, allowing the entire GCT to be configured under software control. In order to prevent JTAG errors from disrupting the VME interface, the VME interface FPGA is on a dedicated chain not accessible by software.

VIII. Current System Status

Development of the GCT hardware has been proceeding in parallel, and first articles have started to arrive over the last few months. The two designs based on existing work, the Source and Leaf cards, are in hand now and under test. Of the two new designs, the Concentrator is in manufacture (due in mid October), and the Wheel is in final layout.

The Source card has been tested extensively, and has met its performance requirements. It is awaiting integration with the Leaf before entering production.



Figure 7: Source card under test at Imperial College

The Leaf card has just started integration tests, and is behaving as expected at this point. The test fixtures and software is in place to start the high speed serial testing, and this critical phase of testing will begin shortly.



Figure 8: Leaf card under test at CERN

The firmware modules for the GCT have been in continuous development and test (both simulation and hardware) for six months. The firmware for several revisions of the Leaf jet finder algorithm has been simulated and successfully tested in hardware on the Los Alamos satellite board. A larger simulation of the Concentrator card and electron Leaf firmware is in progress. The slow control interface has been simulated and proven in initial Leaf card testing.

IX. Conclusion

The CMS GCT effort is well under way, with nearly all required hardware in hand or in production. The schedule is optimistic, with 7 Source cards, 2 Leafs and the Concentrator scheduled for installation in the first months of 2007. Integration and testing will be continuing toward this goal.

X. References

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[2] CMS-IN 04-009, Updated Interface Specification for the CMS Level-1 Regional Calorimeter Trigger to Calorimeter Global Trigger.

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The Drift Tube Track Finder Trigger at the CMS Experiment

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Abstract

The Compact Muon Solenoid (CMS) is a general purpose experiment designed to study proton-proton collisions at the Large Hadron Collider (LHC). The CMS L1 Trigger must select interesting collisions at a rate smaller than 100 kHz. The CMS Drift Tube Track Finder (DTTF) Trigger performs a full muon tracking analysis in real time for the CMS L1 Trigger. The DTTF trigger motivation, electronic implementation, and expected performance are presented.

I. Introduction

At the Large Hadron Collider (LHC) muons of large transverse momenta are expected to play a crucial role in the physics under study. The Compact Muon Solenoid (CMS) is a general purpose experiment designed to study proton-proton collisions at the LHC. There, proton beams will cross each other at a rate of 40 MHz, producing in average 20 p-p interactions. The CMS L1 Trigger must select interesting collisions at a rate smaller than 100 kHz. In this report we describe the Drift Tube Track Finder (DTTF) Muon Trigger. More information about the CMS L1 Trigger in general, and the other trigger subsystems in particular, can be found in [1].

CMS will combine three different technologies for precise muon detection and efficient triggering [2]: drift tube (DT) chambers in the barrel region ($|\eta| < 1.2$), cathode strip chambers (CSC) in the forward region ($0.8 < |\eta| < 2.4$), and resistive plate chambers (RPC) in both regions ($|\eta| < 2.1$). Fig. 1 shows a longitudinal view of the CMS muon detectors. The DT muon chambers are located in the gaps of the barrel iron yoke. The yoke is organized in five wheels along the detector axis. Each wheel is divided in twelve 30° wedges in azimuth, and four concentric stations in the radial direction: MB1, MB2, MB3, MB4. In every station in a wedge, one DT muon chamber contains twelve layers of drift cells organized in two $r-\phi$ superlayers and one $r-z$ superlayer (except the MB4 chambers that do not contain $r-z$ superlayer).

The information delivered by the DT muon chambers is processed by the DT L1 Muon Trigger, which is divided into a DT Local Trigger and a DT Regional Trigger. Hits in the DT muon chambers are first organized in segments and assigned a beam crossing (BX) by the DT Local Trigger (BTI, Traco and Trigger Server subsystems). The Sector Collector gathers the segments in the four stations of a sector, synchronizes them, and sends them, via optical links, to the DTTF crates in the Counting Room. The performance of the DT Local Trigger was measured at the 2003 and 2004 Beam Tests [3, 4]. Beam test results relevant for the present report are the measured DT Local Trigger efficiency of 99% for DT fiducial muons and the Traco position resolution of about 0.5 mm.

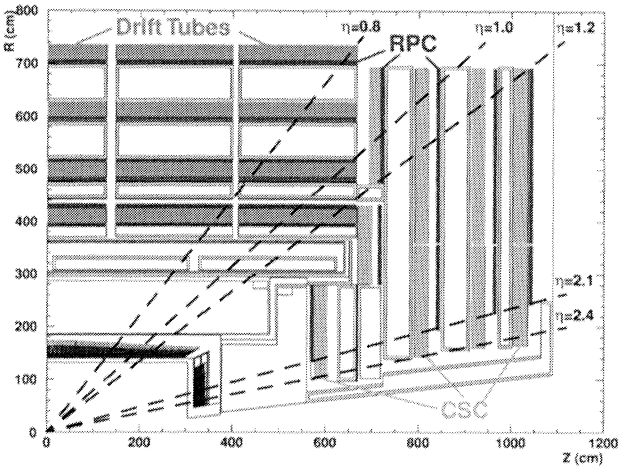

Figure 1: *Longitudinal view of the CMS muon system.*

The DTTF system implements the DT Regional Trigger. Taking advantage of the large (order 2 T) CMS return magnetic field, it is possible to go beyond the conventional coincidence analysis. The DTTF performs a full muon tracking analysis in real time for the CMS L1 Trigger.

II. The Drift Tube Track Finder Trigger

The task of the Drift Tube Track Finder Trigger is to reconstruct tracks consistent with the trajectory of a muon, to assign them physical parameters, to select the best four muons in the barrel detector, and to output them to the Global Muon Trigger for further processing [1].

The DTTF Trigger is physically realized using a sophisticated electronic system. Its segmentation replicates the CMS barrel detector geometrical structure (Fig. 2). The system is organized in twelve modules stored in six 9U crates. Each module processes the information that originated in a 30° wedge of the barrel detector. One module is formed by eight boards : six Phi Track Finder (PHTF) sector processors (one PHTF for wheels ± 1 and ± 2, and two PHTF boards for wheel 0), one Eta Track Finder (ETTF), and one Wedge Sorter (WS). Two modules share the same crate and the same VME Controller, Timing, and Data Link Interface (DLI) boards. In addition, a seventh crate contains the Barrel Sorter (BS), Data Concentrator Card (DCC), VME Controller, and Timing boards.

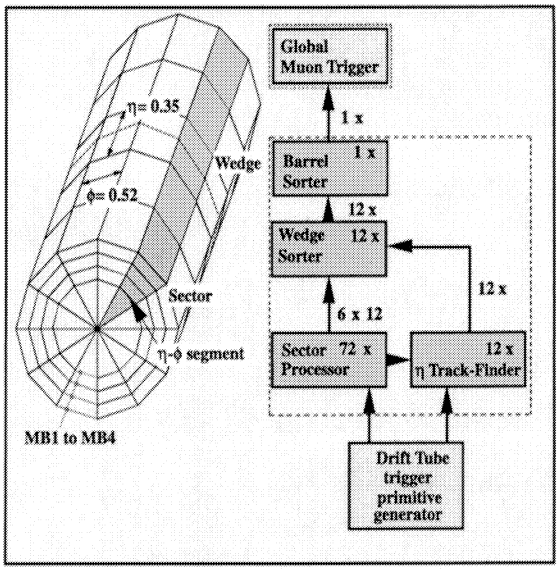

Figure 2: *Logical segmentation and block diagram of the DTTF Trigger.*

A. The Phi Track Finder

The Phi Track Finder (PHTF) processors reconstruct muon tracks in the $r-\phi$ plane. The PHTF track finding algorithm is implemented in three logical steps (Fig. 3):

- **Extrapolation:** In the first step the sector processor tries to match pairs of track segments (delivered by the DT Local Trigger) according to an extrapolation principle, i.e. the correlation between the change in the azimuthal coordinate ($\Delta\phi$) and the bending angle (ϕ_B). Using the spatial position, ϕ, and the angular measurement, ϕ_B, of a track segment in a Muon Barrel (MB) station, the extrapolated coordinate in an outer MB station can be calculated. Attending to this principle, an extrapolation is considered successful when the spatial position in the target MB is found to be inside a 99%-efficient extrapolation window. Windows are downloaded to the hardware in the form of Look-Up-Tables (LUTs).

- **Track Assembling:** The results of the extrapolation process are used in the track assembling step, where all consistent extrapolations are assembled together to form tracks. Depending on how many track segments and from which MB they come from, the PHTF will assign them a quality code.

- **Parameter Assignment:** Finally, the two reconstructed tracks with best quality codes are assigned muon physical parameters: 5 bits of transverse momentum (p_T), 8 bits of ϕ position, 1 bit of electric charge, and 3 bits of quality.

  The two inner muon stations with a valid extrapolation are used as a magnetic spectrometer for transverse momentum assignment: the value of p_T is estimated from the measured value of $\Delta\phi$ using a relation stored in hardware LUTs.

The muon azimuthal coordinate (ϕ) is assigned attending to the local ϕ value measured at MB2. If no actual track segment was found at MB2, extrapolation from MB1 or MB4 is used to predict the ϕ position of the muon track at MB2. Again, this is implemented using LUTs which are downloaded into the hardware.

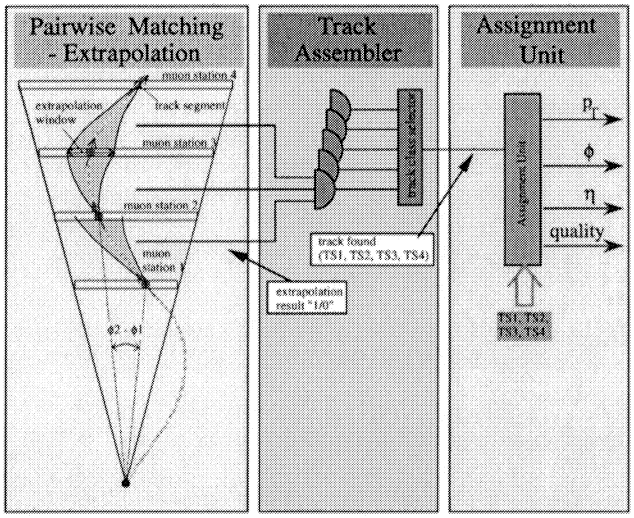

Figure 3: *Schematic representation of the PHTF three-step algorithm.*

The PHTF processors are 9U VME boards (Fig. 4). The complete implementation is based on synthesizable behavioral VHDL code. In the final design, one big Altera Stratix EP1S40 FPGA (1020 pins) mounted on a mezzanine board, accommodates the full track-finding algorithm and LUTs. This solution is referred to as System-on-Chip (SOC). For practical reasons, only the Input Receiver block is implemented in a different Altera Stratix EP1S10 FPGA (780 pins). Every PHTF finds up to two transverse tracks after 475 ns.

The number of PHTF inputs/outputs is considerable. One PHTF receives 506 bits/BX: 110 bits/BX via optical inputs from the Sector Collector, and the rest from PHTF interconnections. In addition, the outer wheel PHTF boards interchange segment information with the CSC. The outputs are 48 bits/BX to the WS, and 10 bits/BX for PHTF-ETTF interconnections.

The PHTF (and ETTF) boards contain a programmed Spy system, implemented as a synchronous, triggerable 512 BX-long ring memory accessible via a 2nd JTAG chain. At the board level, the Spy Master Trigger can be programmed with all possible situations at every step of the track-finding process. At the DTTF level, all Spies can be triggered simultaneously by an external L1 Accept condition. The Spy system allows to follow all the internal data flow in the board and, especially, to validate the trigger decision. The DTTF Local DAQ software system has been developed on top of the Spy hardware: Spy-DAQ. The DTTF Local software has been organized in maintenance, set-up, operation, monitoring and emulation modules. Spy-DAQ has been used intensively at the prototyping, test, quality control, and commissioning phases of DTTF development.

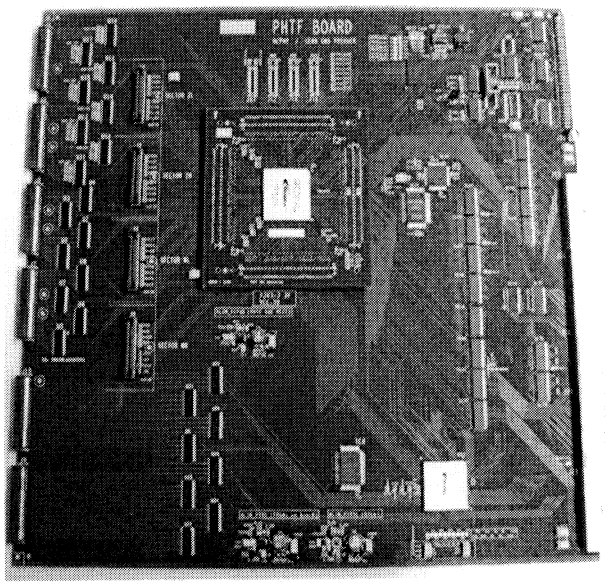

Figure 4: *Phi Track Finder production board.*

Production and quality control of the 72 PHTF boards needed for the final system, and 8 spare boards, finished in March 2006.

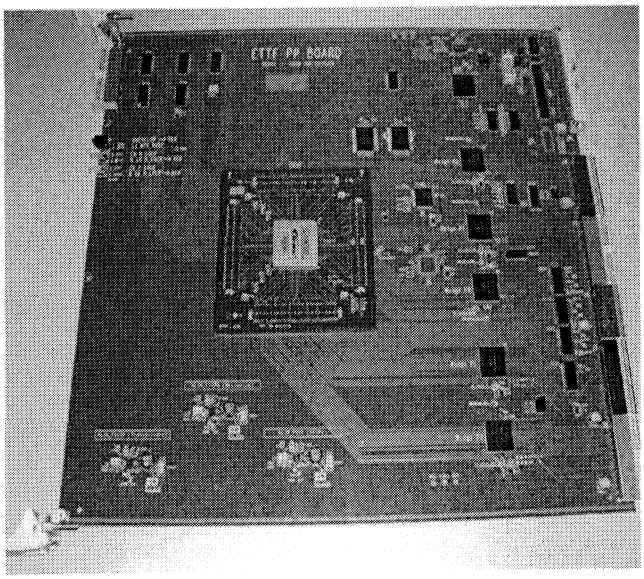

Figure 5: *Eta Track Finder production board.*

B. The Eta Track Finder

The Eta Track Finder (ETTF) processor task is to promote PHTF transverse tracks into full DTTF 3D muon candidates. In every wedge, the ETTF reconstructs the muon trajectory in the $r-z$ projection using data from the $r-z$ superlayers in the five MB1, MB2 and MB3 chambers.

The ETTF implements a pattern-matching algorithm, divided in three logical steps. First, patterns of $r-z$ segments are recognized among a predefined set (η-patterns). Second, η-patterns are matched to PHTF tracks. Finally, if the pattern matching step was successful, the PHTF track is assigned a fine value of the η coordinate. If no η-pattern could be matched, the ETTF can still assign a rough η value according to the place where the PHTF track crossed wheel boundaries.

The final ETTF 9U VME design (Fig. 5) adopted the SOC solution (Altera Stratix EP1S25, 1020 pins) for the pattern-matching algorithm. Five Altera Cyclone EP1C4 (324 pins), with independent timing, accommodate the five Wheel Input Receivers.

One ETTF receives 235 bits/BX from the DT Local Trigger, and 60 bits/BX from the PHTF processors in the same wedge. The outputs are 84 bits/BX to the WS.

Successful production and quality control of the 12 ETTF final boards, and 5 spare boards, was accomplished by April 2006.

C. The Drift Tube Sorters

The DT Sorters [5] select the four highest rank DTTF muons in the barrel detector, after a clean-up procedure (removal of PHTF duplicate tracks below the expected dimuon trigger rate), and forward them to the Global Muon Trigger. The highest rank muons are those with highest quality and highest transverse momentum. The sorting process is implemented in two steps:

- **Wedge Sorter:** In every wedge, one Wedge Sorter (WS) receives the addresses and muon physical parameter information from the six Phi Track Finder and Eta Track Finder processors. Using this information, it selects the two best muon tracks out of (at most) twelve candidates.

  Fig. 6 shows a WS 9U VME production board. See [5] for more information.

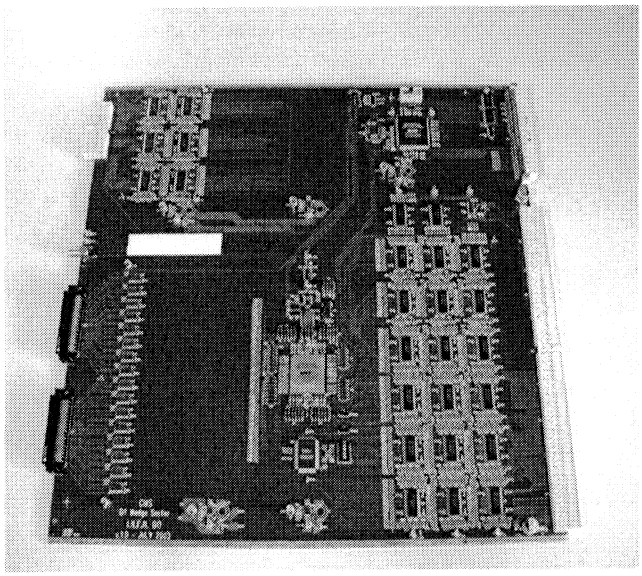

Figure 6: *Wedge Sorter production board.*

- **Barrel Sorter:** There is one DT Barrel Sorter (BS) for all

the DTTF Trigger system. It selects the four highest rank muons among the (at most) 24 delivered by the 12 Wedge Sorters and forwards them to the Global Muon Trigger.

The BS hardware implementation (Fig. 7) accommodates all the logic in a big Altera Stratix EP2S130 FPGA (1508 pins) mounted on a mezzanine card. The rest of the 9U VME board is essentially used for the 24 input (744 bits/BX) and 4 output (128 bits/BX) LVDS connectors.

All final 12(1) WS(BS) boards, and 6(2) spare boards, have been produced and tested.

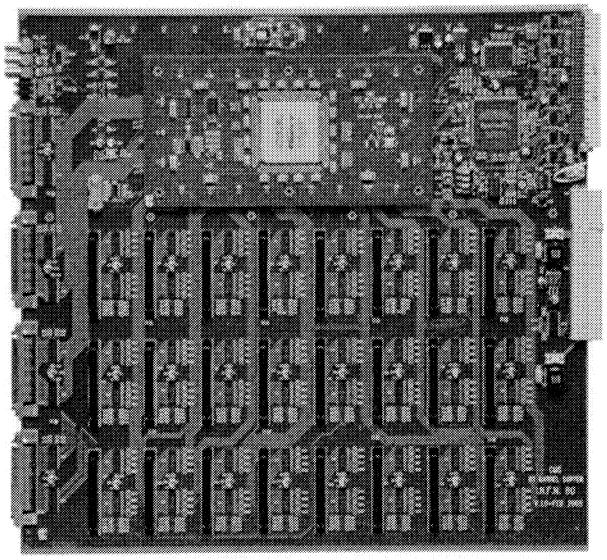

Figure 7: *Barrel Sorter production board.*

In addition, the Barrel Sorter can generate a trigger signal under programmable conditions. The BS input (i.e. the WS output) and output trigger data can then be validated using the 128 BX-long Spy memories. The BS trigger signal has been used at the MT/CC 2006 (see next Section), and will be the base of the DTTF Local Monitoring system at CMS.

D. DTTF Readout

The DTTF, as any other CMS subdetector, sends data to the CMS Central DAQ system at L1 Accept condition. The DTTF data record contains all the input and and output signals from the triggered BX, the previous one, and the next one. The total event size is 53.2 kbit, corresponding to a data rate of 635 MB/s at a maximal L1 trigger rate of 100 kHz. To comply with the maximal allowed average bandwidth of 200 MB/s, a zero-suppression algorithm has been worked out.

The hardware implementation starts with DAQ blocks in the PHTF and ETTF processors. The PHTF and ETTF boards in one crate send bit streams at L1 Accept to the DLI board. Information from the six DLIs is gathered by the DCC board at the seventh crate, and transmitted to the CMS DAQ using the CERN Slink-64 protocol.

III. DTTF Trigger Performance

In this section, the DTTF Trigger performance highlights are presented.

In October 2004 the real DTTF Trigger behavior was studied using data at the CERN test beam [4, 6]. At this beam test all PHTF features, except Track Assembling, were validated.

In 2006, the DT Trigger (including the DTTF) has provided a 3-Sector Cosmic Trigger for CMS at the Magnet Test / Cosmic Challenge (MT/CC). The DTTF hardware setup included three PHTFs, one WS, and one BS. The software setup included SpyDAQ, online monitoring, and a C++ bit level emulator program. In August, a total of 25 million DT events at 0 and 4 T, with the ECAL and Tracker in the readout, have been offered to the Collaboration. Just from the DTTF point of view, the MT/CC has been the first opportunity to validate triggers coming from long tracks, especially tracks changing wheels and/or sectors. Analysis of the data is underway.

In addition, the expected DTTF performance at LHC has been computed using simulated events [6]:

- **Efficiency:** The combined effects of efficiency and transverse momentum resolution are summarized in the 'turn-on' curves in Fig. 8, where the DTTF single muon trigger efficiency is represented as a function of the muon transverse momentum, for different transverse momentum thresholds. The plateau efficiency is 95%, only limited by the DT detector geometrical acceptance.

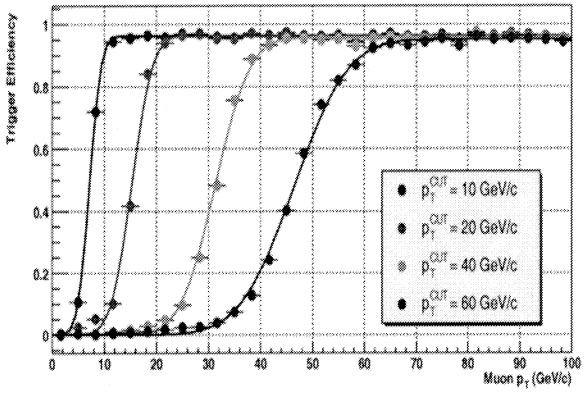

Figure 8: *The DTTF trigger efficiency as a function of the muon transverse momentum, for different p_T thresholds.*

- **Momentum resolution:** From the turn-on curves an overall transverse momentum resolution of 14% is obtained, dominated by dead material effects in the barrel iron yoke.
- **Position resolution in ϕ:** Resolution in phi is dominated by the PHTF output bin size (0.02 rad). The dimuon resolving power is limited by the DT Local Trigger segment position resolution.
- **Position resolution in η:** Resolution in the η coordinate is 0.03 (0.08) for fine (rough) assignment.

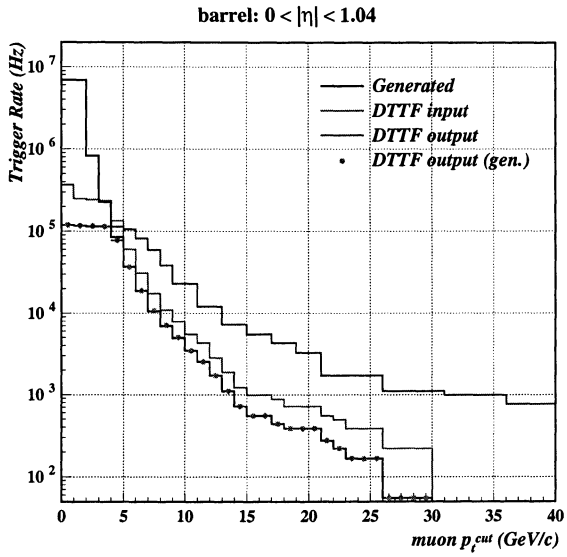

Figure 9: *Integrated inclusive muon DTTF trigger rates at nominal LHC luminosity, as a function of the muon p_T threshold.*

- **Trigger rate:** The accumulated inclusive muon DTTF trigger rate at nominal LHC luminosity, as a function of the transverse momentum threshold, is shown in Fig. 9. Output transverse momenta are assigned for 90% cut efficiency. At low-, intermediate-, and high-p_T the rate is dominated by real muons (decays-in-flight, heavy quarks, and vector bosons, respectively). For a transverse momentum threshold of 15(25) GeV the expected rate is about 6(2) kHz.

IV. Conclusions

In summary, the Drift Tube Track Finder Trigger has been presented. Its rationale, modus operandi, hardware implementation and software tools have been described. Finally, the system performance has been summarized; actual at beam tests and at the MT/CC, and expected at the LHC.

Production of the full DTTF system electronics is complete. Installation at the CMS underground Counting Room and integration with the rest of the CMS L1 Trigger will follow, to be ready for the 2007 LHC Pilot Run.

V. Acknowledgments

The results presented in this report are the result of the ingeniousness and diligent work of all the members of the CMS DTTF Collaboration.

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An RPC-Based Technical Trigger for the CMS Experiment

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Abstract

In the CMS experiment, sub-detectors may send special trigger signals, called "Technical Triggers", for purposes like test and calibration. The Resistive Plate Chambers are part of the Muon Trigger System of the experiment, but might also produce a cosmic muon trigger to be used during the commissioning of the detectors, the CMS Magnet Test-Cosmic Challenge and the later running of CMS. The proposed implementation is based on the development of a new board, the *RPC Balcony Collector* (RBC); the test results on prototypes and their performance during the recent CMS Cosmic Challenge are presented.

I. Introduction

The Resistive Plate Chambers (RPC) are gaseous parallel plate detectors that will be used in the CMS experiment for the muon trigger system [1]. The task of the RPC muon trigger is to identify muons, measure their transverse momentum, determine the bunch crossing from which they originate and select the best track candidates. In the CMS Barrel, a total of six layers of RPCs will be embedded in the iron yoke while in the Forward region up to four layers of RPCs will be instrumented, to cover the region up to $\eta = 2.1$.

The block diagram of the RPC Trigger electronics full chain is shown in Figure 1. The signals induced on the readout strips are amplified and discriminated by the Front End Boards [2] and sent unsynchronized to the Link Boards, placed on the detector periphery. The Link Boards synchronize the signals with the 40 MHz LHC clock and, after a data compression (LMUX), send them to the Splitter Boards and then to the Trigger Boards located in the CMS Counting Room over 90 m optical link at 1.6 GHz. Each TB receives signals from up to 6 layers of RPC and implements the trigger algorithm based on pattern recognition, performed by FPGA devices called Pattern Comparator (PAC). After some steps of sorting and ghost-busting, the RPC Trigger system provides the 8 highest momentum muon candidates to the Global Muon Trigger [3].

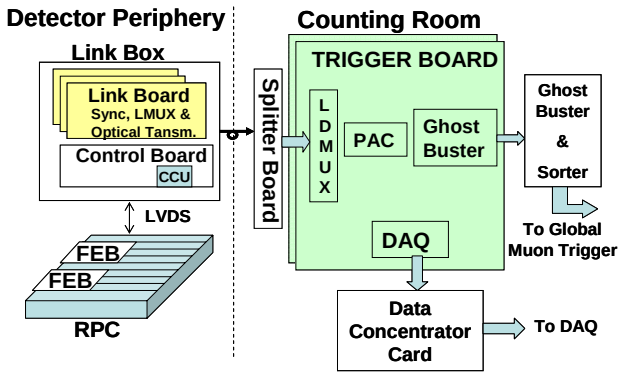

Figure 1: RPC Trigger Electronics Full Chain

II. The RPC-Based Technical Trigger

A. Requirements

During the phase of commissioning, the installed RPCs are carefully tested in all their components: gas system, HV, LV and Front End electronics. A crucial aspect for the analysis of the proper functioning of the detection chain is the generation of a trigger signal independent from other detectors and designed to select cosmic muons. Moreover, the CMS experiment itself foresees the possibility that sub-detectors could send special triggers, called Technical Triggers, for test, calibration and other purposes. An RPC-

based cosmic trigger can be designed to cover all these aspects.

The simplest way to implement an RPC-based cosmic trigger is apparently to use the RPC Trigger System itself, just loading the cosmic patterns into the Pattern Comparators. But the RPC Trigger System was built to identify muon tracks starting from the interaction point. This means that all the interconnections among Link Boards and Trigger Boards are optimized to fulfil the vertex geometry, which is not adequate to a cosmic trigger. This goal might be achieved adding some Splitter Boards and Trigger Boards, but another useful feature of the cosmic trigger in the proposed architecture is to be redundant, in order to have a powerful debugging tool independent from the Trigger Electronics.

The demand for an RPC-based cosmic trigger raised up when the design of electronics and cabling in the experimental hall were frozen; therefore, another constraint of this new system is to use, as much as possible, the existing functionalities and infrastructures and don't introduce major modifications to the existing electronics. Then, this technical trigger must be capable to generate a trigger signal both *locally* and *globally*. The local trigger involves the chambers of one Barrel sector and can be used during the Commissioning of the RPCs to check the efficiency of the installed chambers. The global trigger, used as CMS Technical Trigger, involves the whole barrel and requires infrastructures in the counting room.

B. Implementation

In the proposed scheme, the RPC-based Technical Trigger is implemented by two types of electronic boards: the *RPC Balcony Collector* (RBC) housed in the cavern and the *Technical Trigger Unit* (TTU) located in the Counting Room, as shown in Figure 2.

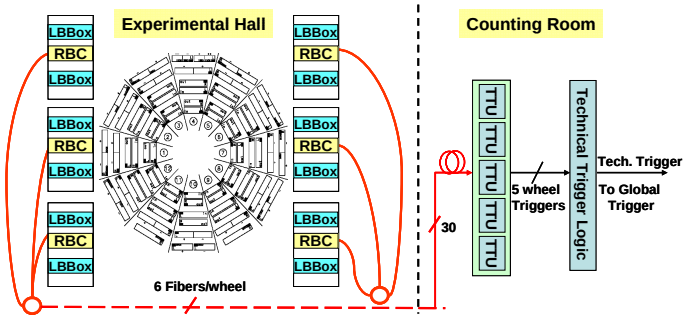

Figure 2: Technical Trigger principles of operation

As described in the previous paragraph, the RPC signal cables are connected to the Link Boards (LB) for synchronization, data compression and optical conversion. Each LB reads 96 strips of one η partition (1 roll = half RPC) and produces an OR signal that can be used for our goal. On the front panel of the LBs there is the *CSC connector*, used only in the forward RPCs to send some synchronization signals from the RPCs to the Cathode Strip Chambers. This connector is not used in the barrel and represents the easiest way to send signals from LBs to RBC without modifying the layout of LBs, already frozen and under production. So, considering also that the cosmic rate at the forward region is expected to be very low and not adequate to perform quick calibration runs, it was finally decided that the RPC Technical Trigger should involve only the barrel chambers.

The 13 or 15 Link Boards corresponding to the chambers of the same barrel sector are housed in the same crate, called LBBox (LBB). The LBBs are housed, in groups of 2, in the 30 racks around the detector. In order to keep the overall cost low, it was decided that one RBC should serve two sectors, for a total of 30 RBCs to equip the whole barrel. The most convenient position for the RBC is inside one of the two LBBs of each rack: in fact from the LBB backplane the RBC can receive the power supplies and the slow control signals provided by the Control Boards, while the input ORs can be easily collected from the CSC Connectors of the LBs by means of simple front-planes circuits. In order to improve the manageability of these front-planes, they are divided into two parts, as shown in Figure 3: the FP1 collects the 7 or 9 ORs from the left part of the crate while the FP2 collects the 6 ORs from the right part, beyond the LHC clock and the reconfiguration signal RCO (this last described in the next paragraph) from the LB housed in the slot # 14. The connection between FP1 and FP2 is made by means of a short flat cable. The same Front-Planes will be used also in the LBB non hosting the RBC: in this case, instead of RBC, a special connector called RBC_FAKE will collect and reroute in the proper way the signals to be sent to the RBC of the same rack by means of a shielded twisted pair cable.

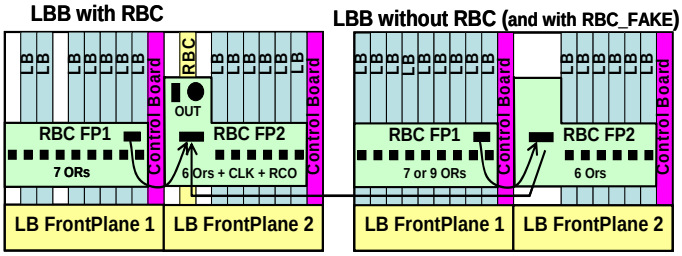

Figure 3: RBC integration in LBBoxes

So each RBC collects 26 or 28 ORs from two sectors, produces two independent sector-based cosmic trigger as "local" triggers and transmit optically the ORs to the Technical Trigger Unit boards in the Counting Room, where a wheel-level cosmic trigger will be produced and sent as technical trigger to the Global Trigger of the experiment.

III. The RBC Board

As shown in Figure 4, the main features of RBC are:

- mask the dead or noisy input ORs;
- produce a sector-level cosmic trigger based on pattern recognition, using pre-loaded pattern and according to selectable majority level;
- force one or more input ORs to be in the pattern, in order to increase the trigger selectivity;
- transmit electrically the OR on the front panel, for eventual data acquisition during the Commissioning;
- introduce selectable latency, at steps of 25 ns, to synchronize the RBC trigger with other detectors;

- remotely controlled using I^2C bus;
- transmit optically the ORs to the Counting room.

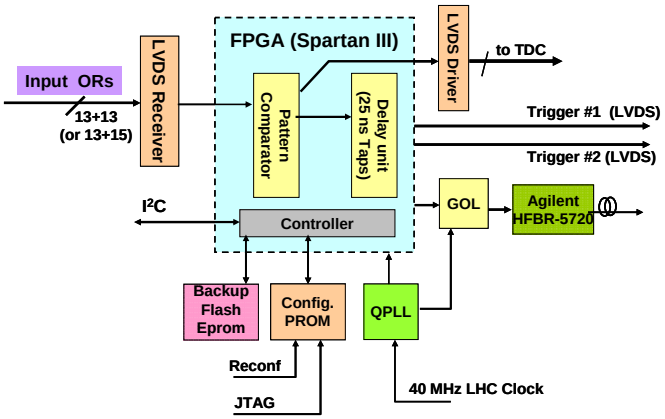

Figure 4: RBC Block Diagram

The RBC has been designed using the Xilinx Spartan-3 FPGA, in order to have high flexibility and the possibility to upgrade the firmware. Since the RBC is out of the slow control CCU chain, the FPGA can be configured only in situ using the JTAG Bus. Therefore, eventual firmware upgrades will be done only during the opening phases of the detector. In any case, this aspect does not represents a major limitation since all RBC parameters can be modified remotely using the I^2C bus and moreover, during the experiment, all the signals will be available in the Counting Room, where the TTU board will have a higher flexibility and possibility to be upgraded also remotely.

A. *RBC Prototypes*

Three prototypes have been produced and successfully tested. The circuit is a 10 layer 14x14 cm^2 PCB, to be housed on a mother board fitting the LBBox dimensions. All the I/O are accessible on the front-plane FP2 through a ZPACK connector, with the exception of the power supplies and the I^2C bus that are received from the backplane. A picture of the board is shown in Figure 5. The prototypes have been tested both on the Bari test bench and in the Bld. 904 at CERN, where they have been installed in the LBBs (Figure 6) and all the interconnections were checked.

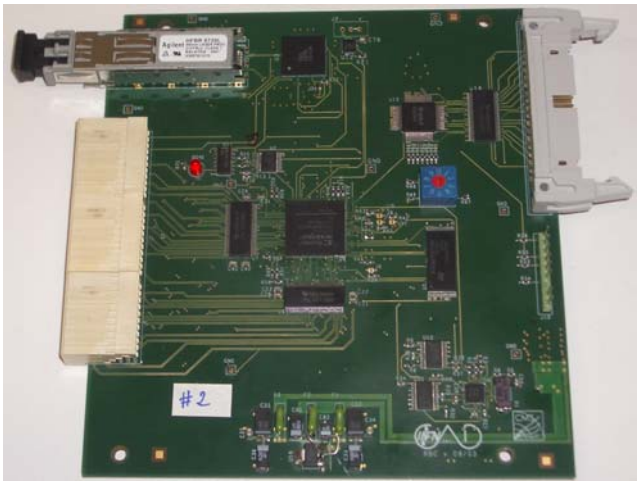

Figure 5: RBC Prototype

Moreover, since during the MTCC the RBC will be located 120 m far from the receiver end (the Local Trigger Controller LTC or the PSB board of the Global Trigger), the LVDS Trigger signal was sent on a 150 m long cable, to check the quality after such a long distance. The LVDS signals, having a pulse width of 75 ns, showed a jitter of ~ 10 ns, while transmitting them in LVPECL and opto-coupled with the receivers, the jitter decreased down to 5 ns and the signals were properly received by both receiving boards in proper synchronization.

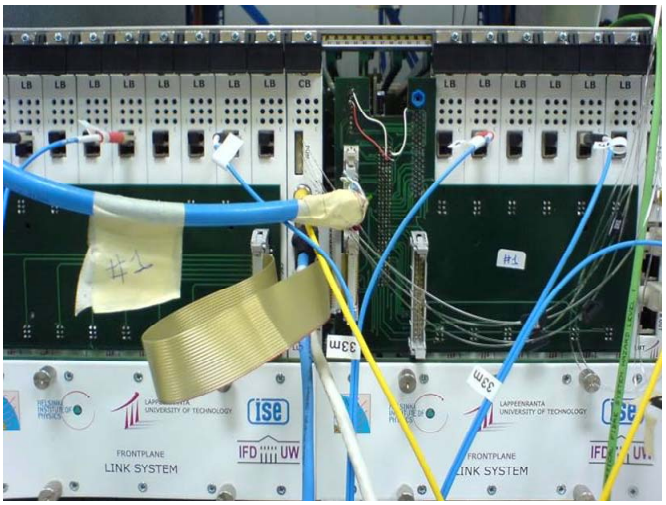

Figure 6: RBC system in LBBox

B. *RBC SEU strategy*

On the detector periphery, the environment is not critical. In fact, the expected total dose is less than 1 krad, the neutron flux for neutrons with energy more than 20 MeV is expected to be less than 100 $cm^{-2}s^{-1}$, giving a neutron fluence less than 10^{10} cm^{-2}. The most sensitive device is the SRAM-FPGA, where Single Event Upset might corrupt the configuration memory. Tests performed at Los Alamos Neutron Science Center by Fabula et al. [4] has shown that, for the chosen device, the expected SEU cross section is $\sigma_{bit} \sim 3.0 \times 10^{-14}$ cm^2/bit, corresponding to $\sigma \sim 2.9 \times 10^{-8}$ cm^2, while the expected Time to Configuration upset = $1/(\sigma * Flux) \sim 95$ hours/device.

In order to mitigate the risk, since the RBC is embedded into the LB system, it comes natural to adopt the same strategy as the Link Boards (also based on Spartan III FPGAs), that is to reload periodically (every 5 minutes) the configuration SRAM from Flash EPROM, that are extremely robust against our level of irradiation: upon the arrival of the RCO signal from LB, the required time to load the bit stream is about 200 ms.

Concerning the serializer, the rad-tolerant GOL chip developed at CERN is used [5], while the chosen optical transceiver is the AGILENT HFBR-5720L, that was successfully tested by Alice group with neutron fluence 10^{11}n/cm^2 at different energies: 10 MeV, 150 MeV and 180 MeV [6].

C. MTCC

Two RBC prototypes have been installed and used during the CMS Magnet Test-Cosmic Challenge (MTCC phase I), started in June 2006 to complete the commissioning of the magnet before the lowering in the cavern and, at the same time, to demonstrate the operations of the various sub-detectors with cosmic trigger, the cosmic ray reconstruction across CMS and test the Muon Alignment systems.

Concerning the barrel RPCs, 3 sectors have been involved in the MTCC: the sector 10 of the Wheel YB+1, readout by the RBC1 and the sectors 10 and 11 of the Wheel YB+2, readout by the RBC2, though till the end of September 2006 the sector 11 of YB+2 was not fully equipped with LBs and is expected to be fully operational only for the MTCC phase II, starting at the end of September.

In the MTCC phase I the RBC was connected to a simple L1 trigger system using the LTC as Trigger Controller, while in the MTCC phase II the LTC will be replaced by the Global Trigger and the RBC trigger will be sent to the Pipelined Synchronized Buffer board of GT, that in CMS will be the board receiving the technical triggers.

Beyond the two sector-based RBC triggers (RBC1 and RBC2), the RPC Trigger Board was also used to look for muons pointing to the tracker (RPCT Trigger).

The RBCs were well synchronized with the RPCT Trigger, as well as with the other muon detector (DT and CSC) Triggers.

The RBC Trigger working point has been studied through variations of the RPC High voltage. As an example, the RBC trigger rate as a function of the inner RPC HV of Sect.10-YB+1 is shown in Figure 7.

For both sectors, the trigger rate is about 30 Hz/sector for majority level of 5/6, while working with majority 6/6 the trigger rate is around 13 Hz/sector.

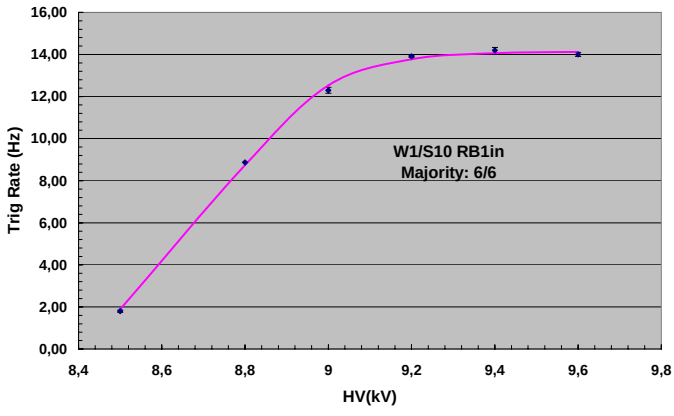

Figure 7: RBC trigger rate vs. inner RPC High Voltage

During the MTCC the RBC has been demonstrated to be a very useful scientific tool to study the performance not only of RPC, but also of DT. In Figure 8, an Iguana event display of a cosmic muon triggered by RBC and crossing RPC and DT is displayed.

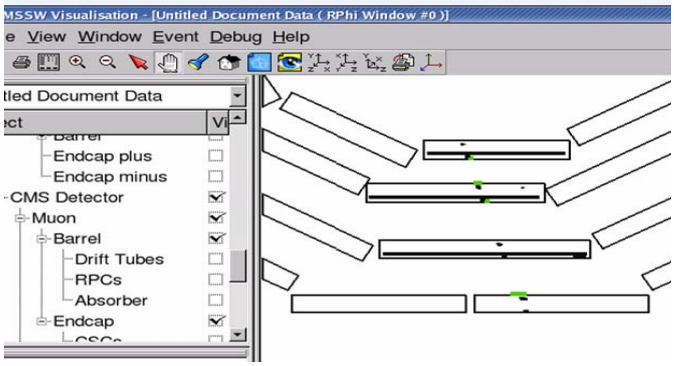

Figure 8: Iguana event display

IV. TECHNICAL TRIGGER UNIT

The Technical Trigger Unit (TTU) boards will be housed in the counting room to receive the produced wheel-based cosmic trigger to be sent to the Global Trigger as Technical Trigger.

The TTU system will receive 30 RBC fibers each carrying 26 or 28 bit at 40 MHz. The signals must be synchronized with the local LHC clock and then the pattern recognition algorithm must be implemented.

All these functionalities are already implemented by the RPC Trigger Board [7] (Figure 9), developed by the Warsaw RPC Trigger Group. In fact, each TB can receive up to 18 fibers and the pattern comparators are implemented into fully programmable FPGAs with large amount of logic cells, enough to implement cosmic pattern recognition based on the OR of strips. Since each of the 6 the Opto-Synch FPGAs can receive at most 72 signals, only 12 links per TB can be used for TTU implementation, hence 3 TBs are needed to equip the full Barrel.

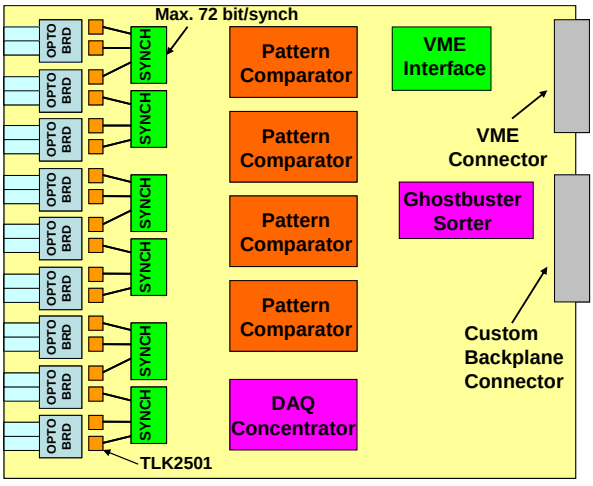

Figure 9: Trigger Board as Technical Trigger Unit

The huge advantage to use TB for this goal is to save time and money to produce new boards and, at the same time, to profit of all other infrastructures needed, such as the hardware and software tools developed by the Warsaw Group to load and control the board remotely. Beyond the development of the new firmware to be uploaded into the PACs, it will be only necessary to design a custom backplane, where mounting the TTC_{rx} chip to receive the timing and

control signals and the simple electronics to properly combine the wheel-level cosmic trigger and produce the final technical trigger.

The TB-TTUs will be placed in the RPC Sorter Crate in the Counting Room.

V. CONCLUSIONS

The architecture of the RPC-based technical Trigger has been shown. A new board, called RPC Balcony Collector, has been designed to produce Sector-Based Cosmic Trigger and the prototypes have been successfully tested and used during the CMS Magnet Test Cosmic Challenge. The RBC will be fully produced before the end of 2006 and in the next weeks the firmware for the TB-TTU and the TTU backplanes will be designed to complete the full chain of RPC-based Technical Trigger.

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Design and Test of the Off-Detector Electronics for the CMS Barrel Muon Trigger

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Abstract

Drift Tubes chambers are used in the CMS barrel for tagging the passage of high Pt muons generated in a LHC event and for triggering the CMS data read out. The *Sector Collector* (SC) system synchronizes the track segments built by trigger modules on the chambers and deliver them to reconstruction processors (*Track Finder*, TF) that assemble full muon tracks. Then, the *Muon Sorter* (MS) has to select the best four candidates in the barrel and to filter fake muons generated by the TF system redundancy. The hardware implementations of the Sector Collector and Muon Sorter systems satisfy radiation, I/O and fast timing constraints using several FPGA technologies. The hardware was tested with custom facilities, integrated with other trigger subsystems, and operated in a beam test. A test beam on a 40 MHz bunched beam validated the local trigger electronics and off-detector prototype cards and the synchronization tools. The CMS Magnet Test and Cosmic challenge in 2006 proved stable and reliable operation of the Drift Tubes trigger and its integration with other trigger systems and with the readout system. Constraints, design, test and operation of the modules are presented.

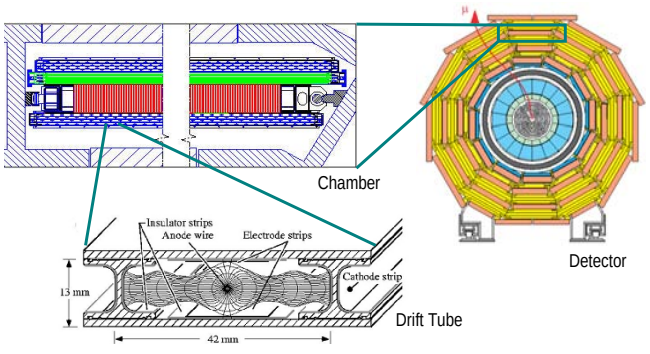

Figure 1: Schematic view of the DT detector

I. The Drift Tubes Muon Trigger

The aim of the muon system [1] is to provide a robust trigger, with bunch crossing assignment, identification and momentum estimation of the muons produced in the p-p collision in a wide Pt range. The system is embedded in the return yoke of the magnet, and the bending given by the magnetic field inside it is used to provide a Pt assignment for muon tracks. Drift Tubes (DT) detectors are used in the barrel region.

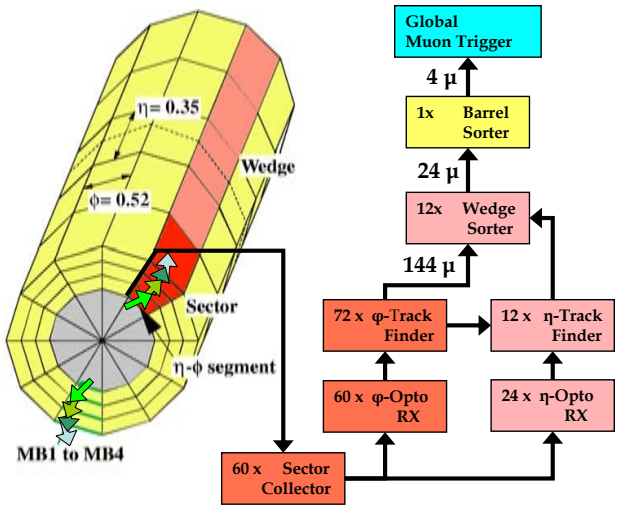

Figure 2: Left: sketch of the DT detector as it is partitioned for the off-detector electronics. Right: block scheme of the Sector Collector and regional trigger system.

The DT system is segmented in 5 *wheels* along the z direction, each about 2.5 m wide and divided into 12 azimuthal *sectors*, covering $\sim$30° each. A cross section of a wheel is shown in Fig. 1: DT chambers are arranged in 4 concentric cylinders - called *stations* - within each wheel, at different distance from the interaction point, and interleaved with the iron of the yoke. Each DT chamber is instrumented with staggered layers of drift tubes in the transverse (r, ϕ) plane and in the longitudinal (θ, z) plane and it is equipped with trigger electronics consisting of several modules. This *local trigger* electronics [2] is able to identify tracks crossing the station, assigning collision from which the particles originated [3] and the impact postion, together with the angle of the tracks with respect to the radial direction, providing a measument of the bending of the muon. As it is sketched in Fig. 2, local trigger data are sector-wise collected on the towers near to the detector by Sector Collector cards where the timing from different channels is adjusted to account for time of flight and cable lengths. One sector is linked by one SC card, thus 60 SC boards are needed. Segments are sent to the underground counting room using optical links and delivered to the *regional trigger* where Track Finder cards run an extrapolation and matching algorithm in order to build full muon tracks and to measure their transverse momentum [4]. In the right part of Fig. 2 a block scheme of the regional trigger is shown: the numbers of modules are shown inside each block, while near to the connecting arrows the maximum number of muons that are

processed at each step is shown. The colors help understanding how the system is partitioned: each Track Finder module operates on one sector of the DT detectors and the large number of muon tracks (up to 144) that can be potentially found is analyzed wedge- and barrel-wise by the Muon Sorter cards, that run a ghost suppression algorithm and finally sort up to four muon candidates from the whole barrel.

In the following sections, details about implementation, test and integration of the Sector Collector and Muon Sorter systems will be given.

II. The Sector Collector

The Sector Collector (SC) is a VME 9U board installed on tower crates, near to the CMS detector itself [6]. Its main task is to collect from one sector of the DT detector the local trigger data, received in high-speed (480 Mb/s) LVDS [5], and trasmit them on optical fibers to the counting room.

A. Receiver cards

The SC design has been split in several sub-units. In Fig. 3 a picture of a receiver mezzanine is shown. This mezzanine can receive the trigger data from one chamber, performing the deserialization and some data processing and monitoring. On the right side, the FTP cables are connected. The numbers help identifying the main components: cable equalizers (1), deserializers (2) and a flash-based FPGA ProAsicPlus from Actel (3). A flash-based FPGA was chosen due to its intrinsic radiation hardness (with respect to a SRAM-based FPGA), since the SC boards will be installed in the undergroun experimental room, where low-energy neutrons may flip SRAM configuration bits leading to functionality interrupts [7]. Flash configuration memory is more robust to low energy ionization events in the silicon, ensuring an interruption-free operation [8, 9].

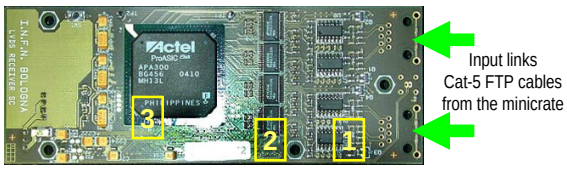

Figure 3: The LVDS receiver mezzanine. The main components are labelled with numbers (see text).

The FPGA on the receiver mezzanine has several tasks: it checks the data integrity, through deserializers status monitoring and data parity calculation; it sorts the highest quality ϕ segment if more than one is received at the same bunch crossing; it handles test features that are useful to synchronize the system and to test the connections with the main board.

B. Optical transmission card

The data from each receiver mezzanine are fan-out to the host motherboard (Fig. 6), where an optical transmission mezzanine is plugged. A picture of the optical transmission card is shown in Fig. 4. The main components are a clock filtering and fanout circuit based on a QPLL [10], and six GOL chips serializing data at 1.6 Gb/s using the Gigabit Ethernet protocol [11]. The serialized data are sent to the undeground counting room over multimodal fibers ($\sim$ 70 m) at 850 nm using VCSELs from Honeywell. Fig. 5 the *eye pattern* seen on the receiver board after electrical conversion, together with measurements of the eye opening that allow the bit error rate from the signal shape to be estimated less than 3×10^{-14}.

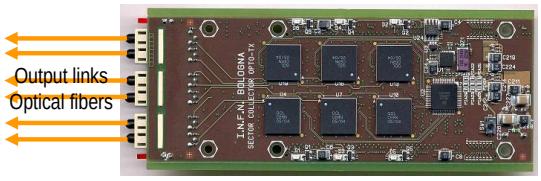

Figure 4: The optical transmission mezzanine.

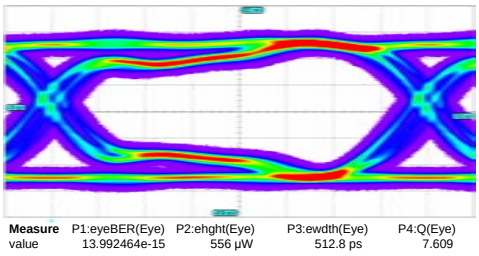

Figure 5: The eye pattern seen on 1.6 Gb/s serialized data.

C. SC Motherboard

In Fig. 6 the SC motherboard is shown. Only receivers mezzanines for the MB1 and MB2 chambers and the optical transmission mezzanine are plugged in this picture. The device indentified by (6) is a further ProAsicPlus device, called controller chip, that implement the VME interface of the board and several bridges to other interfaces. A JTAG chain [13] connects the receiver mezzanines FPGAs, while a I2C interface allows the GOL chips to be monitored and configured, as well as current limiters, temperature sensors and laser monitoring to be accessed. The synchronization of the system is monitored accessing parity error counters and controlling clock phases using independent delay lines (8, 9). A spy system is implemented on the controller chip. Each receiver mezzanine sends to the controller chip a subset of the trigger data flow that is written on FIFO buffers. The spy data allows the timing of the triggers from the (r, ϕ) and (θ, z) planes of the DT chamber to be monitored, together with the quality of the local track segments. The FIFO write process can be controlled by central triggers (level-1 accept) or by a self-generated trigger, expressed as a logic function of single chamber triggers. The spy data can be sent to the DT readout electronics [12] through a dedicated inteface

(10) or accessed locally through VME.

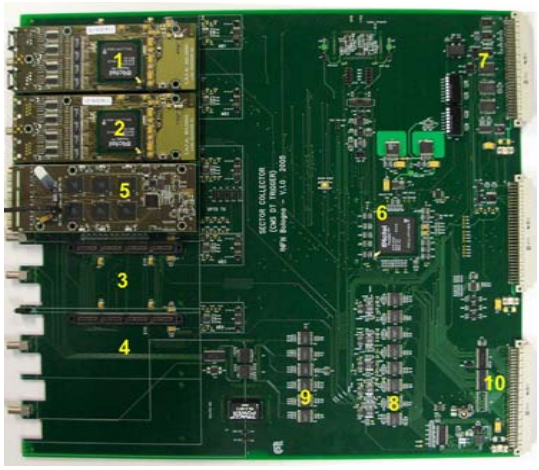

Figure 6: The motherboard, only LVDS receiver mezzanines for MB1 and MB2 and opto transmission mezzanine are plugged.

D. Optical receiver card

In Fig. 7 a picture of the optical receiver board is shown. The main components are labelled by numbers: PIN diodes and amplifiers converting the optical power into electrical signals (1); a FPGA (Altera StratixGX) hosting embedded deserializers, which also checks the data integrity (2); and output buffers, delivering parallel data to the corresponding $\phi(\eta)$-Track Finder [14] board (3). In The main FPGA is designed with a custom JTAG interface, driven by the corresponding Track Finder board, to access internal status information about the data integrity and to drive test modes. The same boards are used for the $/phi$ and the η parts of data, with the main FPGA firmware built in two versions.

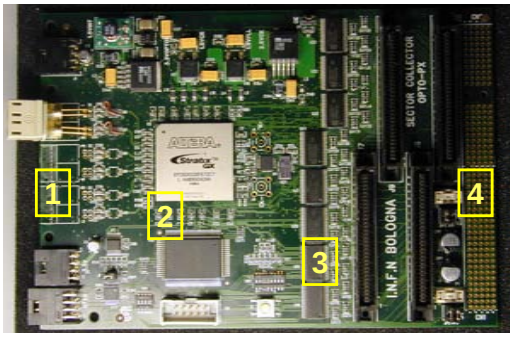

Figure 7: The opto receiver board. The main components are labelled with numbers (see text).

III. The Muon Sorter system

As it is shown in Fig. 2 the Muon Sorter is split in two consecutive processing steps, performed by the Wedge Sorter modules and by a single Barrel Sorter board. All boards are VME 9U, where the interfaces and the main processing units have been designed using S-RAM FPGAs [6].

A. The Wedge Sorter

Each Wedge Sorter receives up to 12 muon candidates from the Track Finder modules operating on the five sectors of a wedge, and selects the two "best" candidates, with an overall I/O of about 450 parallel signals at 40 MHz. A picture of the board is shown in Fig. 8. Two FPGAs from Altera are used to implement the VME interface of the board (Acex1k FPGA, 2) and the main computational part (Apex20k FPGA, 1).

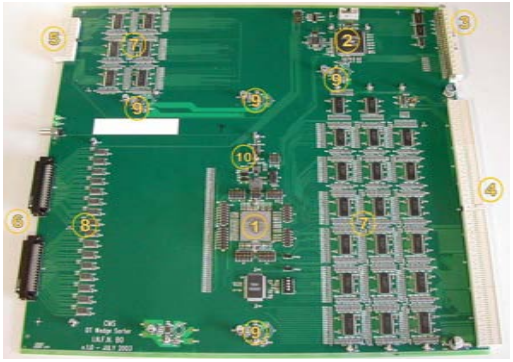

Figure 8: The Wedge Sorter board.

On the latter, a ghost busting algorithm is able to identify if consecutive track finder modules delivered two copies of the same physical track, to reduce the rate of these "false dimuon" events. An example of false dimuon reconstruction is shown in Fig. 9, where a longitudinal section of the muon system is shown: the two muons cross consecutive sectors, and both are reconstructed twice by independent Track Finder processors [15]. Using information about the segments used to build the tracks, the ghost busting algorithm identifies common segments and cancels the worst quality (i.e., built with less and outer segments) track of each pair [16]. The sorting algorithm is fully parallel, and can sort the two "best" tracks (highest reconstrucion quality, highest transverse momentum) out of twelve input tracks in less than 50 ns.

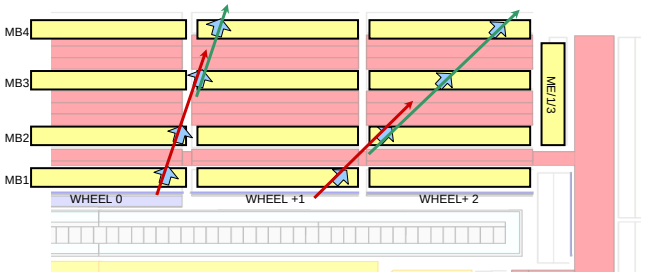

Figure 9: Example of fake track generation by the partitioning of the Track Finder system. A longitudinal section of the the muon detectors is shown.

B. The Barrel Sorter

Outputs from 12 Wedge Sorter are sent in parallel LVDS on twisted pair cables to the Barrel Sorter board, which is shown in Fig. 10.

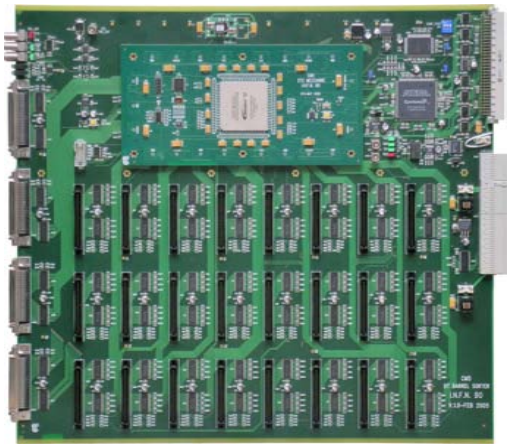

Figure 10: The Barrel Sorter board.

This board performs the final ghost busting and selection over the full sample of 24 muon candidates from the previous stage, with an impressive parallel I/O of about 900 bit at 40 MHz (∼36 Gb/s). Also in this board, two FPGAs are present: a VME interface, implemented on an Altera Cyclone, with a full VME speed parallel bridge to the main FPGA, an Altera StratixII in a 1508 pin BGA package, mounted on a mezzanine board. The main processing unit performs the ghost busting and sorting within 75 ns. To satisfy this latency requirement a mixed parallel/serial approach was chosen for the sorting algorithm, with an internal pipeline running at twice the I/O frequency (i.e., at 80 MHz). Moreover the main FPGA contains FIFOs with VME access to spy the full I/O of the trigger data. The device can also drive an external trigger, based on programmable conditions, like thresholds on track qualities.

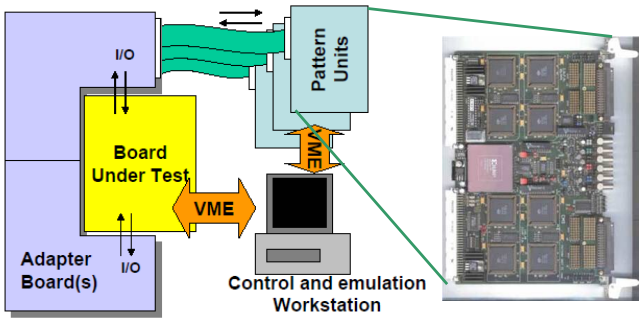

Figure 11: Sketch of a generic test bench: a workstation controls a VME system with Pattern Units, that are itnerfaced to the device under test by adapter boards. On the right, the picture of a Pattern Unit.

IV. Test of the Electronics

The produced electronics, both at the prototyping and at the final production stages, undergo severe tests to verify the functionalities. The tests are both stand-alone, to qualify the single card, and integrated, to check a more complex chain of several modules.

A. Stand-alone tests

In the left side Fig. 11, the sketch of a stand alone test bench is shown. The approach shown in the picture has been followed in all the test benches that validated prototype and production boards. The key component of this test bench is the *Pattern Unit* (PU), shown in the right side of the figure. This is a custom VME 6U I/O board, based on FIFO memories and provided with a VME interface, able to receive/drive up to 128 I/Os at up to 100 MHz [17]. These cards can be run in parallel, allowing to run workstation-controlled tests of devices at their full speed injecting millions of random or specific patterns. For this purpose, adapter boards are built, in order to match the form-factor or the electrical standard of the device under test. On the workstation an emulator is run, in order to verify bit by bit the response.

B. Integration tests

Stand-alone test benches can then be mixed both in hardware setup and in software emulation in order to perform integration tests, i.e. to test a complete Sector Collector system or to test the WS to BS connection. The spy tools embedded in the designed FPGAs are useful in integration tests and in real life operation. In Fig. 12 the integration of Track Finder and Muon Sorter test setup is shown. On the left side, a block diagram shows the data flow. VME Test Boards inject data in the Track Finder boards, and the data flow thorughout the system is spied at several levels up to the last module.

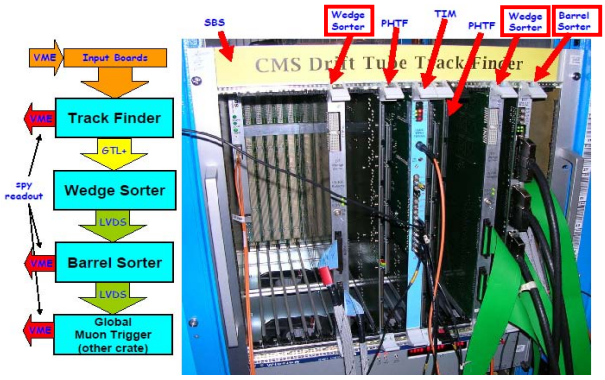

Figure 12: DTTF-WS-BS integration test.

V. CMS Cosmic Challenge

The CMS detector, currently being assembled at surface, was intensively tested with cosmic muons during the first magnet test runs. This "Magnet Test and Cosmic Challenge" (MTCC) setup is shown by the event display reported in Fig. 13.

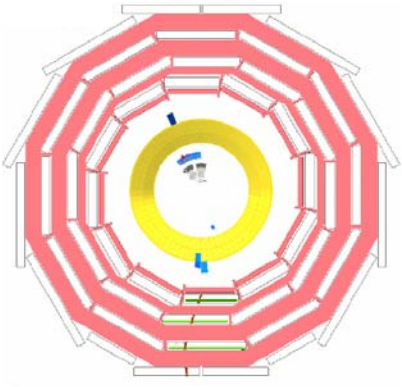

Figure 13: MTCC event

A full "slice" of the CMS experiment was integrated: three sectors of DT detectors were synchronized and triggered cosmic muons, with the readout system including calorimeters and the trackers. The DT trigger was generated by the Barrel Sorter board, on which a quality threshold was applied to tracks built by the Track Finder. In the event shown, a muon (bended by the magnetic field inside the superconducting solenoid and in the yoke iron) was triggered by the DT detectors, in the lower part of the detector; the track can be backward followed to see that also HCAL, ECAL and the Trackers had hits. The DT trigger chain was based on three sectors of the detector, using the three inner chambers on each sector. In Fig. 14 some plots from the Sector Collector spy system are shown. Each plot shows the number of track segments found versus the segment bunch crossing number. On each column, the plots from the three chambers of one sector (i.e., one Sector Collector board) are shown. This kind of data allows the relative synchronization of the different detector partitions to be checked quickly and reliably.

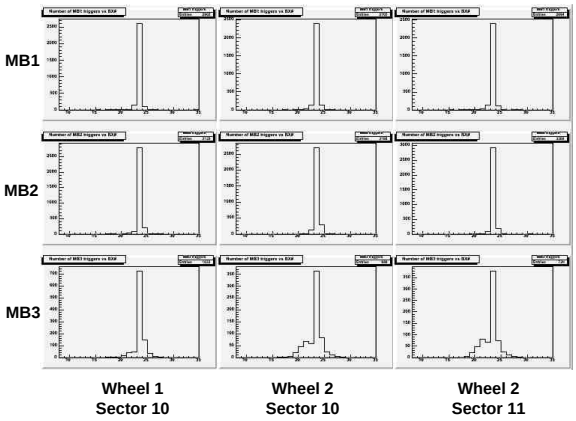

Figure 14: 3 sectors x 3 chambers synchronization plots from MTCC (SC SPY).

VI. Summary and conclusions

A general overview of the CMS DT muon detectors and trigger system was given. The main tasks and design features of several off-detector components of the trigger electronics were described with some implementation details. The electronics is based on custom FPGA designs, implementing the trigger algorithms and useful test and data spy features. The modules were tested in their working conditions using setups based on custom I/O units. Integration tests and the CMS Magnet Test and Cosmic Challenge were the final integration test bench that proved the correct and reliable operation of the DT trigger system.

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Parallel Session B2

Trigger session 2

Level 0 trigger decision unit for the LHCb experiment

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Abstract

The Level-0 Decision Unit (L0DU) is the central part of the first trigger level of the LHCb detector. The L0DU receives information from the Calorimeter, Muon and Pile-Up sub-triggers, with fixed latencies, at 40 MHz via 24 high speed optical fiber links running at 1.6 Gb/s. The L0DU performs simple physics algorithm to compute the decision in order to reduce the data flow down to 1 MHz for the next trigger level and a L0Block is constructed. The processing is implemented in FPGA using a 40 MHz synchronous pipelined architecture. The algorithm can be easily configured with the Experiment Control System (ECS) without FPGA reprogramming. The L0DU is a 16 layer custom board.

I. The Unit

The purpose of the Level-0 Decision Unit (L0DU) [1] is to compute the L0 trigger decision by using the information from the L0 sub-triggers in order to reduce the data flow from 40 MHz down to 1 MHz for the next trigger level [2] (see Figure 1).

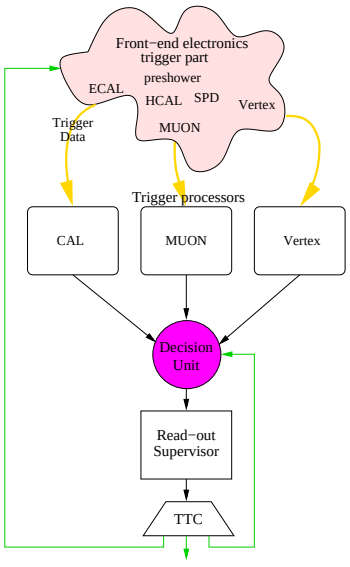

Figure 1: Simplified L0 trigger system

For that purpose, the L0 Decision Unit receives an event summary from the L0 calorimeter selection board [3], the L0 Muon trigger processor [4] and the L0 Pileup system, each with its own latency, at 40 MHz (see Figure 1). Then, a physics algorithm is applied to select events and delivers the L0DU trigger decision to the Readout Supervisor (ODIN) [5] which takes the ultimate decision to accept or not the event. The L0DU trigger decision is encoded in a 16 bit explanation word (RSDA) [6]. At each event, a ”L0-Block data” is constructed and sent to the High Level Trigger (HLT) when the L0DU has received a L0Accept signal coming from ODIN via the Timing and Trigger Control system (TTC) [7].

The L0DU architecture is designed to be flexible in order to have the possibility to configure different algorithms through the Experiment Control System (ECS) [8] with the same programmed architecture. Special triggers can be implemented with specific arithmetic and logical computations. Downscaling (accepted rate of a trigger channel) of the L0 trigger decisions and changing conditions of the decision (algorithm, threshold, downscaling factors, ...) are possible. Monitoring of performance and statistic analyses will be done by the hardware and the software. The motive of the decision is coded in an explanation word (L0DUrpt) in the L0Block data and is sent to the Data Acquisition (DAQ).

Special care of the good running and debugging of this unit is taken. Thus, in addition to an internal test bench based on RAM, a dedicated test bench has been developped [9]. It is based on an optical pattern generator board able to send test pattern during 18 LHC cycles.

Table 1: L0DU port summary

External system	I/O	# bits
CALO	I	224@40MHz
MUON	I	256@40MHz
PILE-UP	I	64@40MHz
Spare	I	224@40MHz
RSDA	O	16@40MHz
HLT	O	1024@1MHz
ECS	IO	-
PC Interface via USB	IO	-

A. Input and output data

The input data [10] are made up of several ”candidates” that correspond to the few highest transverse energy or momentum (Et, Pt) detected particles. Thus, the calorimeter sends one electron, one photon, one neutral pion, one global neutral pion and the highest hadron as candidates. The muon detector sends the two highest muons for each quarter of the detector, while the vertex detector transmit the global condition in order to make a veto (no trigger allowed in case of multiple collision) calculation. In addition, the total energy deposited in the calorimeter

and the SPD detector occupancy are also received by the L0DU. The data are sent on 32 bits words including a bunch identification number allowing to time align the incoming data since each has its own latency.

A total of 864 bits (Table 1) at a frequency of 40 MHz is expected at input of the L0DU. The total latency of the L0 trigger is 4 μs and the L0DU latency budget is 500 ns counted from the late arriving sub-trigger data.

The L0DU transmits the decision within a 16 bits word at 40 MHz to trigger distribution system ODIN. This word contains the decision, a bunch crossing identification number. An additional bit is used to ask for forced trigger for debugging and slow control purpose. Another bit allows timing tuning functions of the trigger distribution system. It is set when a given pattern of decision is detected over 5 events (the current event and the two events before and after): isolated decision or collision. The last bit is used as a status bit, and indicates to ODIN that the L0DU decision could be erroneous.

B. Architecture

For each data source, a "Partial Data Processing" (PDP) system performs a specific part of the algorithm. It re-phases the data with the system clock, does the data time alignment and prepares the algorithm data. In this first step, the pipeline architecture is optimized for each L0 sub-trigger data and implements pre-processing like searching the three highest Pt muon. Then, a "Trigger Definition Unit" (TDU) processes the information to form a set of trigger conditions which are combined to compute the L0DU decision (see Figure 2).

Every trigger conditions are ORed to obtain the L0DU decision after indivudal downscaling if needed.

Then, the decision word (16 bits) is sent to ODIN.

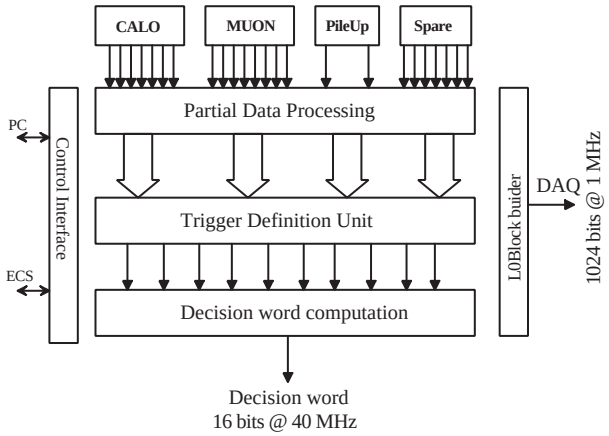

Figure 2: L0DU logical architecture

The L0Block builder part constructs the L0Block. The L0Block contains up to 32 words of 32 bits of data concerning an event (header, raw input data, processing algorithm partial results, etc. . .). It is sent to the DAQ system only when the experiment L0 trigger is received on the decision unit. For that, the L0Block is built for each event and stored into memories waiting for the L0 trigger and finally put into a FIFO when validated. Each validated L0Block is sent word by word at a 40 MHz.
The control interface exploits signals delivered by the ECS to manage the algorithm parameters, the data processing algorithm behaviour, reset scenarios, slow control, on line debugging and monitoring and many other tasks like FPGA programming.

C. I/O format

All the L0 sub-triggers transmit their data via high speed optical links running at 1.6 Gb/s, 17 single optical fibers are expected from the L0 sub-triggers and 7 spare optical links have been added. This 17 single optical fibers are connected to 2 patch panels. Each patch panel converts the 12 single optical channels into a MPO fiber ribbon which is connected to the L0DU.

The L0DU implements two optical transceiver HFBR-782BE from Agilent, each connected to a ribbon. Then, 24 TLK2501 from Texas Instrument are used to deserialize the data. A data word is seen as two words of 16-bits at 80 MHz on the reception side.

The decision word is sent to ODIN over a point-to-point 16-bit LVDS link using a 3M pack connector (34-pins) and a twisted pair ribbon cable with 17 pairs.

D. L0DU setup

The L0DU decision unit is implemented as a plug-in module on a standard LHCb DAQ board (TELL1) [11], (see Figure 3). The main data flow does not use the TELL1 board which consists in sending at 40 MHz the decision word to ODIN. The L0DU uses the TELL1 board for DAQ interface, for the ECS access through the CC-PC of the TELL1, for the power supply and the JTAG chain access through the CC-PC.

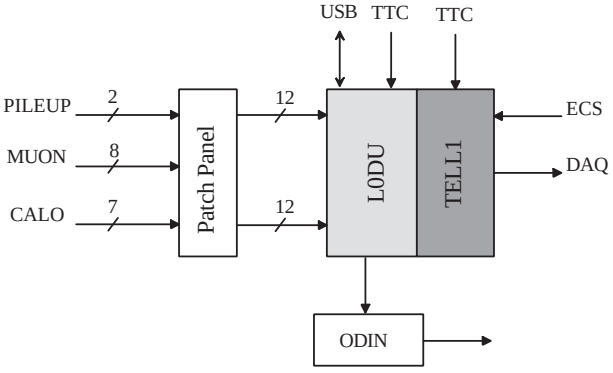

Figure 3: L0DU implementation

E. Flexibility

For the design, an emphasis is put on flexibility. The use of FPGA makes this point easy to implement. As the data processing algorithm remains quite simple, most of the probably needed functionalities can be implemented and then selected by the way of configuration register, without the need of a dedicated complex configuration software.

The L0DU architecture is flexible (see Figure 4), and allows to compute and to realize the most current types of algorithms. The structure of the flexible architecture is composed by a first step which is dedicated to the selection of all the inputs of the algorithm coming from the Partial Data Processing (PDP). This function is equivalent to an interconnexion switch. In a second step, the elementary conditions are elaborated by using arithmetic and logical operators. Then, a Programmable Logic Device (PLD) architecture is used to make combinaison, compose the triggers channels and take the decision.

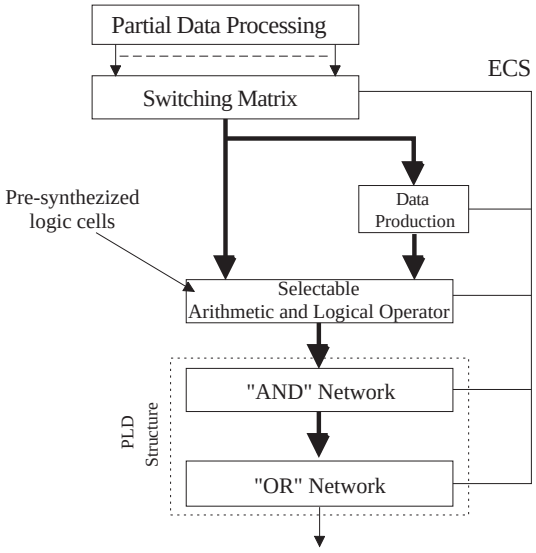

Figure 4: Flexible architecture

The interconnexion matrix is composed by multiplexors which allow to affect each output by a trigger data coming from the PDP. The elementary condition block is composed by macro-cells and allows to select the logical operators. The PLD structure allows to combine the elemenary conditions in a configurable way.

The architecture is not specific to a particular algorithm and is fully configurable without re-programming the FPGA. The structure and the way to compose step by step the algorithm introduce flexibility: new trigger channels can be added easily. Evolution are possible because unforeseen functionnalities can be added with no modification of the global architecture but will need a re-programmation of the FPGA.

The limits are imposed by the amount of pre-synthezized macro-cells, the size of the interconnexion switch, the size of the PLD and the amount of logic elements available in the FPGA.

II. Functionnalities

The L0DU is based on very simple algorithms combining some cuts on energy or impulsion of the candidates. Of course the type of selected physic events is conditionned by the applied algorithm. As an example, calorimeter candidates is selected by applying threshold on Et can be used to select b events while total Et can allow to reject multiple interactions.

Some more complex tasks are implemented: data synchronisation, time alignment, search for the 3 highest muons over the 8 candidates, sum of the two highest Pt muon, production of new data or combinaition between simple conditions to produce fine triggers.

Others functionnalities are implemented which do not concern directly the decision algorithm. The L0DU implements monitoring for on-line analysis like error counter, time alignment checking, counter associated to the trigger channel and the L0DU decision.

The L0DU implements specific module for the commissioning of the L0DU unit and the interface to the L0 sub-triggers, ODIN, the DAQ through TELL1 and check the behavior of the L0DU in a stand alone test mode.

III. L0DU Test Bench

The test of the L0DU and the test bench are more complex than the unit itself. A Specific pattern injection (GPL) has been developed to be able to emulate the L0 sub-triggers and to characterize the links used. This board allows to emulate physics run and failure like loss of synchronisation of the optical link or erroneous data.

A. GPL functional description

The GPL board allows to send test pattern on 24 optical fiber running at 1.6 GB/s. The pattern could be either a fixed pattern, a counter or a RAM content. The board is also able to acquire the L0 decision word sending at 40 MHz. The GPL registers and GPL RAM can be accessed with an USB interface or an ECS access through the L0DU plugged on the TELL1 board.

The GPL is compatible with TTC for synchronisation and with the standard LHCb crate and can be installed in the pit.

B. GPL board design

The GPL board (see Figure 5) relies on three Stratix FPGA, two are used for the processing and one is used for the control of the board. The GPL implements 12 external memories able to strore test pattern during 18 LHC cycle, a clock network and two optical channels. The GPL board has an emulated ODIN input and an USB interface for the control of the board. Special

cares have been taken concerning the clock network, the jitter filtering and the board place and route.

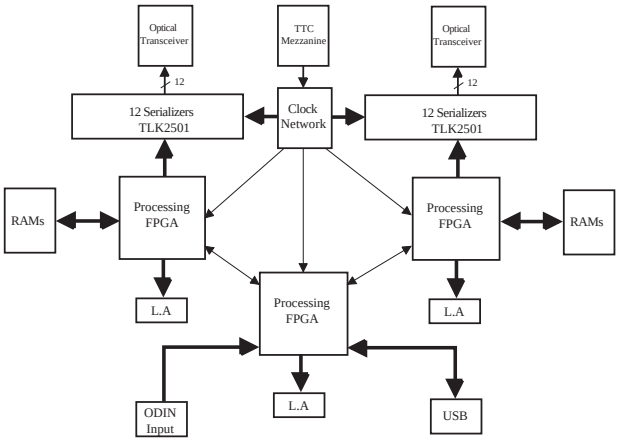

Figure 5: GPL board design

two procesing FPGA centralizes the information coming from the L0 sub-triggers and it is that FPGA which implements the definition of the L0DU algorithm. A dedicated FPGA is implemented on the L0DU to control de board. This control FPGA is connected to the TTC mezzanine, the ECS of the CC-PC of the TELL1, a USB interface and the processing FPGA in order to deliver the signals and the ECS.

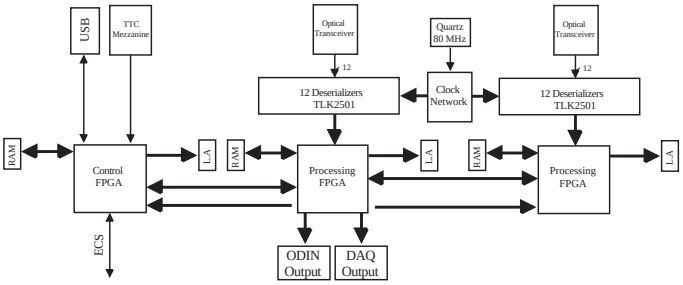

Figure 6: L0DU board design

C. Embedded test bench

A simplified version of this external test bench is implemented on the L0DU. It allows to test the behaviour of the L0DU architecture after installation by injecting known patterns with internal memories (Depth:256, Width:32). The processing results are stored and compared to the expected results. The comparison can be done either by the hardware either by the L0DU software. The internal test bench is composed by 24 RAM to store the test pattern, 2 RAM (Depth:256, Width:16) to store the results and the expected results. Nevertheless, the full debugging and the maintenance will be performed with the external test bench at laboratory.

IV. L0DU BOARD

A first prototype [1] has been assembled and tested at the begining of the year 2002. It was a simplified version that had neither ECS nor Timing Trigger Control connection and had a reduced number of inputs and outputs. The inputs and outputs were in LVDS format at 40 MHz via Ethernet CAT 5+ cables and RJ45 connectors.

Due the number of interconnexion between the L0 sub-triggers and the L0DU, it has been decided to use optical links. Furthermore, it has been decided to implement the L0DU as a TELL1 mezzanine in order to benefit of the ECS and DAQ paths. A new prototype has been designed, and all the functionnalities required for the L0DU are now implemented [12].

A. Design

The processing of the L0DU is done by two Stratix FPGA in BGA package due the hight number of interconnexion between the optical design part of the L0DU. Each, FPGA receives the data output bus of 12 TLK2501 deserializers. One of the

The FPGA used for the processing are Stratix EP1S25-F1025-C7 in BGA package, and the control FPGA is a Stratix EP1S10-F780-C7 in BGA package.

B. L0DU processing

The first part of the internal design of the processing FPGA is composed by an optical module that allows to re-synchronise the data to the local system clock and converts for each optical link the input data flow 16 bits at 80 MHz into 32 bits at 40 MHz. This function implements errors synchronisation detection and the demultiplexing data.

Then, a specific step is dedicated to the latency compensation and time alignment between the different sub-trigger data. Data production, data formating and internal patch panel are introduced to prepare and to select the data that will be used in the Trigger Definition Unit.

Thresholds are applied on data to constitute the elementary condition that will be used in algorithm. Each elementary condition are combined, by a AND network, to form the trigger channel that are after downscaled. The decision of the L0DU is taken by apllying a OR network between the downscaled trigger chanel.

C. ECS and Software

The actual prototype allows to access to the L0DU through the I^2C bus of the CC-PC [8] of the TELL1 board. A software control system for L0DU is being designed to be integrated in the LHCb software environment. According to the LHCb rules, the software interface in based on the PVSS [13] and use the JCOP [14] control framework for the integration of the hardware.

D. Test and results

All the interface and the functionnalities of the L0DU have been tested and validated: DAQ interface, ECS and JTAG access, ODIN link and all the optical links. The Bit Error Rate (BER) of each optical link has been qualify and is below $10^{-}12$ as required for the LHCb experiment [15]. The ODIN link has been qualified with a BER below $10^{-}12$.

Various types of algorithm have been implemented and tested on the board with realistic data generated from a sample of simulated physics event. This prototype is closed to the final version and allows to evaluate the ressources and the limation of the board.

E. Final version of the L0DU

The limation of the actual design is due to the logical ressources of the FPGA. The upgrade for the final version is to implement FPGA with more logic ressources with the same package, to add interconnexion between the two processing FPGA and add spare connexion with the TELL1 board.

V. Conclusion

The figure 7 shows the second prototype of the L0 Decision Unit plugged on the TELL1 board. The L0DU board is complex due to the high density of signals and the high frequency of signals. Many Specctra Quest simulations must have been done before manufacturing and allowed to make a such design without hardware failure. This prototype will be used during the LHCb detector commissioning phase.

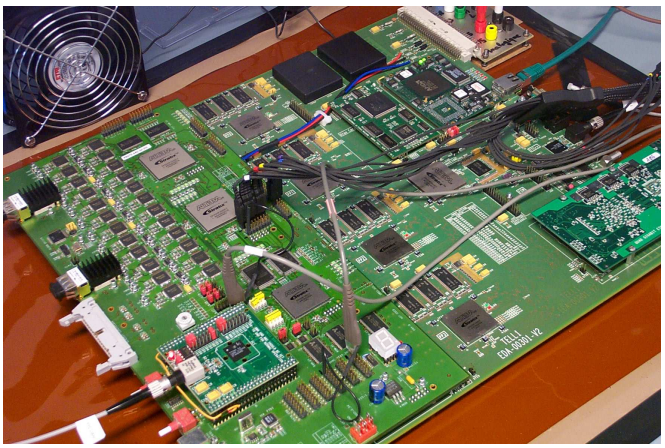

Figure 7: L0DU board plugged on a TELL1

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The Level-0 Muon Trigger for the LHCb Experiment

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Abstract

The Level-0 Muon Trigger looks for straight tracks crossing the five muon stations of the LHCb muon detector and measures their transverse momentum. The tracking uses a road algorithm relying on the projectivity of the muon detector. The architecture of the Level-0 muon trigger is pipeline and massively parallel. Receiving 130 GBytes/s of input data, it reconstructs muon candidates for each bunch crossing (25 ns) in less than 1.2 µs. It relies on an intensive use of high speed multigigabit serial links where high speed serializers/deserializers are embedded in Field Programmable Gate Arrays (FPGAs).

I. OVERVIEW

The muon system has been designed to look for muons with a high transverse momentum, a typical signature of a b-hadron decay. It is composed of the muon detector and the level-0 muon trigger.

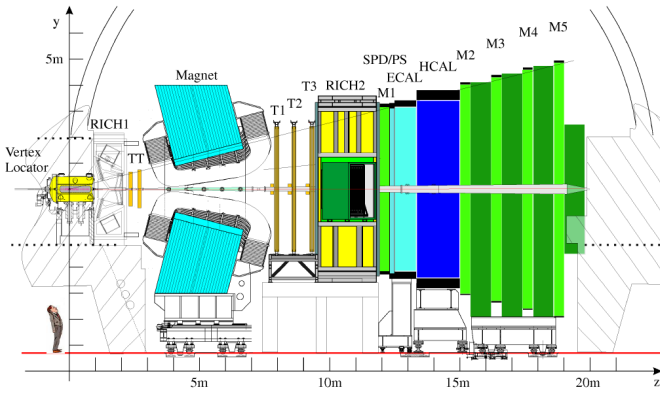

Figure 2: The layout of the LHCb spectrometer [1] showing the electromagnetic (ECAL) and hadronic (HCAL) calorimeters as well as the five muon stations M1-M5 interleaved with iron filters.

A. Muon detector

The muon detector [2], shown in Figure 1 consists of five muon stations interleaved with muon filters. The filter is composed of the electromagnetic and hadronic calorimeters and three iron absorbers. Stations M2-M3 are devoted to the muon track finding while stations M4-M5 confirm the muon identification. The first station M1 is placed in front of the calorimeter and plays an important role for the transverse momentum of the muon track.

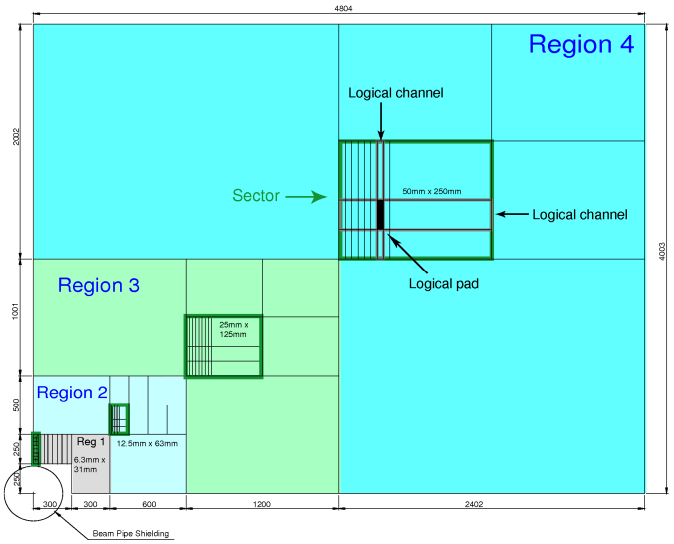

Figure 1: Front view of one quadrant of muon station M2 showing the dimension of regions.

Each station has two detector layers with independent readout. A detector layer contains two gaps in stations M2-M5. To achieve the high detection efficiency of 99% per station and to ensure redundancy, the signal of corresponding physical channels in the two gaps and two layers are logically OR-ed in the chamber to form a logical channel. The total number of physical channels in the system is about 120,000 while the number of logical channels is 25,920.

Each station is subdivided into four regions with different logical pad dimensions as shown in Figure 2. Region and pad sizes scale by a factor two from one region to the next. The logical layout in the five muon station is projective in *y* to the interaction point. It is also projective in *x* when the bending in the horizontal introduced by the magnetic field is ignored.

Pads are obtained by the crossing of horizontal and vertical strips whenever possible. Strips are employed in stations M2-M5 while station M1 and region 1 of station M4-M5 are equipped with pads.

Strips allow a reduction in the number of logical channels to be transferred to the muon trigger. The processor receives 25,920 bits every 25 ns forming 55,296 logical pads by crossing strips.

Each station is subdivided into *trigger sectors* as shown in Figure 2. They are defined by the size of the horizontal and

vertical strips and match the dimension of underlying chambers.

B. Level-0 Muon Trigger

The Level-0 muon trigger looks for muon tracks with a large transverse momentum, p_T. The track finding is performed on the logical pad layout. It searches for hits defining a straight line through the five muon stations towards the interaction point as shown in Figure 3. The position of the track in the first two stations allows the determination of its p_T.

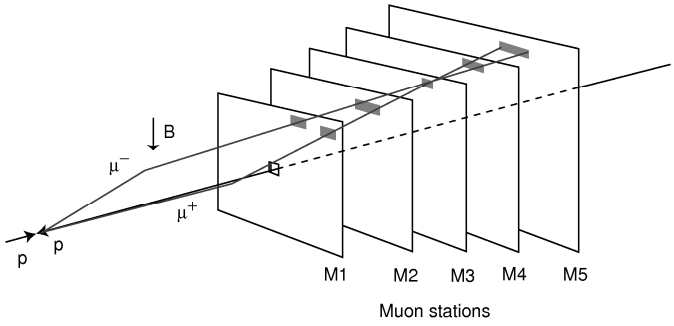

Figure 4: Track finding by the Level-0 muon trigger.

To simplify the processing and to hide the complex layout of stations, we subdivided the muon detector in 192 towers pointing toward the interaction point as shown in Figure 5. A tower contains logical pads with the same layout: 48 pads from M1, 2 × 96 pads from M2 and M3, 2 × 24 pads from M4 and M5. Therefore the same algorithm can be executed in each tower. Each tower is connected to a processing element, the key element of the trigger processor.

The architecture of the Level-0 muon trigger is pipeline and massively parallel. Receiving 130 Gbytes/s of input data, it reconstructs muon candidates for each bunch crossing (25 ns) in less than 1.2 µs.

C. Track Finding Algorithm

The track finding algorithm is illustrated in Figure 4.
For each logical-pad hit in M3 (track seed), an extrapolated position is set in M2, M4 and M5 along a straight line passing through the hit and the interaction point. Hits are looked for in these stations in search windows termed Field Of Interest (FOI), approximately centred on the extrapolated positions. FOIs are open along the *x*-axis for all stations and along the *y*-axis only for stations M4 and M5. The size of a FOI depends on the station considered, the level of background and the minimum-bias retention required. When at least one hit is found inside the FOI for each station M2, M4 and M5, a muon track is flagged and the pad hit in M2 closest to the extrapolation from M3 is selected for a subsequent use.

The track position in station M1 is determined by making a straight-line extrapolation from M3 and M2, and identifying in the M1 FOI the pad hit closest to the extrapolation point.

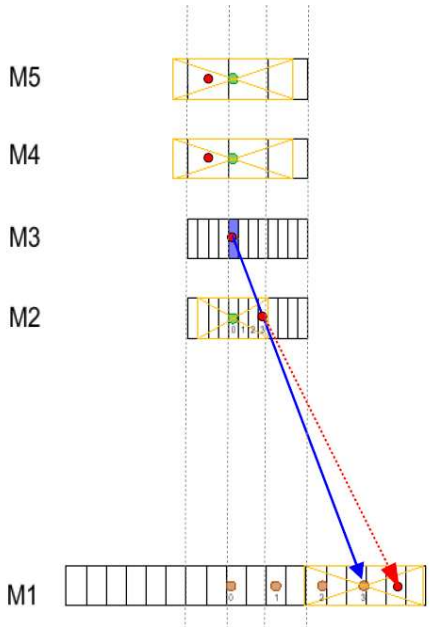

Figure 3: The track finding algorithm.

Since the logical layout is projective, there is one-to-one mapping from pads in M3 to pads in M2, M4 and M5. There is also a one-to one mapping from pairs of pads in M2 and M3 to pads in M1. This allows the track finding algorithm to be implemented using only logical operations.

D. A complex system

The implementation of the track finding algorithm is complex: huge number of logical channels distributed in a large volume; mixture of pads and strips; granularity of logical channels varying between regions and stations. Moreover, there is one-to-one correspondence between towers and trigger sectors except for station M2-M3 region R1 and R2. In region R1, a trigger sector is shared by two towers while in region R2 a tower maps two sectors, as shown in Figure 2.

Finally, processing elements have to exchange a huge number of logical channels to avoid inefficiency on the border of a tower. The topology of data exchange depends strongly on the granularity and on location of the tower.

II. Architecture

An overview of the Level-0 muon architecture is given in Figure 5. Each quadrant of the muon detector is connected to a level-0 muon processor via 312 optical links grouped in 36 ribbons containing 12 optical fibres each. An optical fibre transmits serialized data at 1.6 Gbits/s on a distance of approximately 100 meters.

To collect data coming from a tower spread over five stations and to send them to a unique processing element we use a switch panel located close to the muon processor.

The processing elements run in parallel 96 tracking algorithms on logical channels coming from a tower. It is

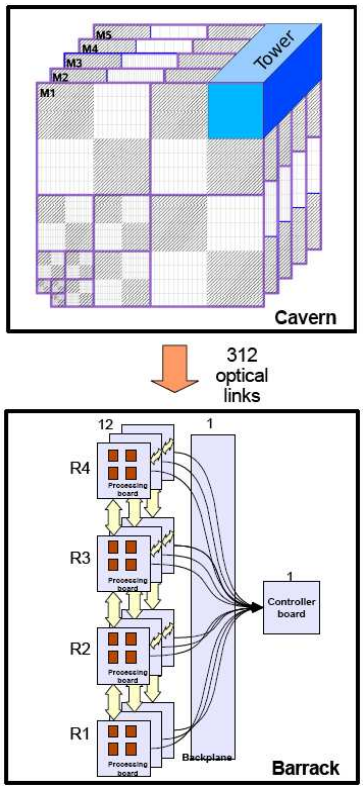

Figure 5: Overview of the Level-0 muon architecture for a quadrant of the muon detector.

implemented in a FPGA named processing unit (PU).

A processing board contains 4 PUs and an additional FPGA to select the two muons with the highest transverse momentum within the board, named BCSU (Best Candidate Selection Unit).

A muon processor houses 12 processing boards, a custom backplane and a controller board. The custom backplane is mandatory to exchange logical channels between PUs located on different processing boards.

A. Generic design

A single generic processing board was designed. The size of each connection between PUs has been maximized to accommodate all configurations. We use 40 MHz and 80 MHz parallel links as well as 1.6 GHz serial links. The resulting topology of the data exchange is shown in Figure 6. In such a framework, firmwares loaded in FPGAs differs according to the area covered by the board. We handle 48 configurations, one per tower of a quadrant.

B. Data flow within a processor

Logical channels are received over 312 optical links. The trigger aligns them in time. Neighbouring information is exchanged between PUs. Tracking algorithms are launched in parallel for the 96 seeds of a PU, which makes 4608 tracking algorithms on each quarter of detector. Each PU delivers a maximum of two candidates to the BCSU. There is one BCSU per processing board. Each BCSU receives eight candidates and selects the two candidates with the highest p_T. At this stage only 24 candidates remain in a processor. The BCSUs send their candidates to the *control unit* (CU) and to the *slave unit* (SU) located on the controller board. The CU and the SU select the two candidates with the highest p_T and send them through two high speed serial links to the L0 Decision Unit.

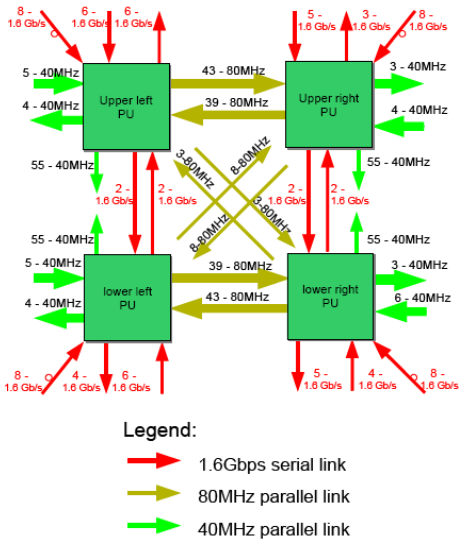

Figure 6: Interconnections between processing units.

III. IMPLEMENTATION

Our implementation relies on the massive use of multigigabit serial links deserialized inside FPGAs. Processors are interfaced to the outside world via optical links while processing elements are interconnect with high speed coper serial links.

The number of pins available on standard high density connectors is not sufficient to transfer at 40 MHz the huge amount of logical channels required to run the track finding algorithm. Multiplexing the data at 80 MHz divides the number of connections by a factor two, but the routing density is very high and therefore sensitive to cross talk. For this reason we decided to mainly use 1.6 Gbits/s serial links for the interconnection between FPGAs.

A. Massive use of multigigabit serial links

By serializing most of the data exchanges at 1.6 Gbits/s we divide the number of connections by a factor 16. Sensitivity to cross-talk and to noise is decreased by a large factor since links are routed on differential lines. However, routing requires a lot of care since the geometry of the tracks must be totally controlled to guaranty a good impedance matching and to minimize electromagnetic emissions to the environment as well as sensitivity to electromagnetic perturbations from the environment.

A processing board embeds 92 high speed serial links while the backplane assuring the connectivity between the processing elements uses mixed technologies: 288 single-

ended links at 40 MHz and 110 differential serial links at 1.6 Gbits/s.

B. Processing board

The synoptic of the processing board is shown in Figure 7. It contains five FPGAs from the Stratix GX family [3]: four PUs and one BCSU. High speed serialiazer/deserializer are embedded in FPGAs. The board sends data to the data acquisition system though a classical L0-buffer/L0-derandomizer mechanism [4]. The processing board is remotely controlled via Ethernet by an embedded PC [5] running Linux.

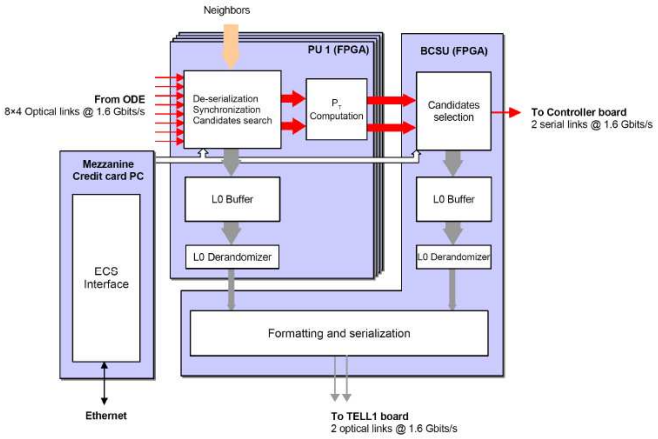

Figure 7: Synoptic of the processing board.

The board shown in Figure 8 is implemented in a 366.7 × 220 mm format. The printed circuit board is composed of 18 layers where 1512 components are mounted. The power consumption is lower than 60 W.

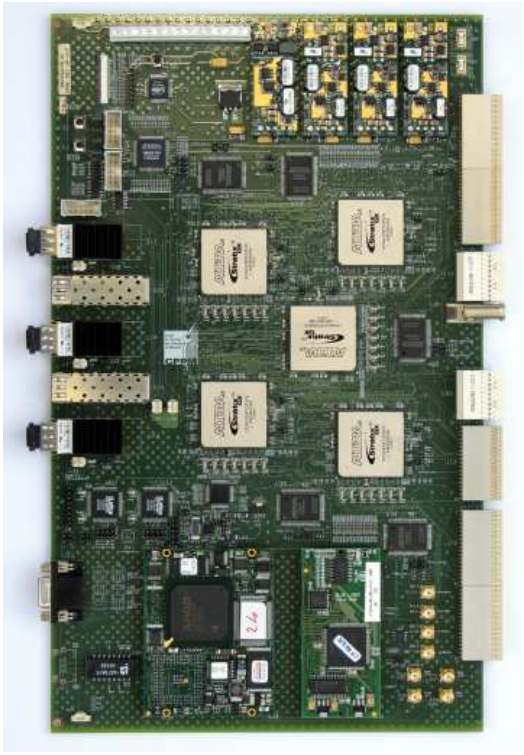

Figure 8: Top view of a processing board.

C. Controller board

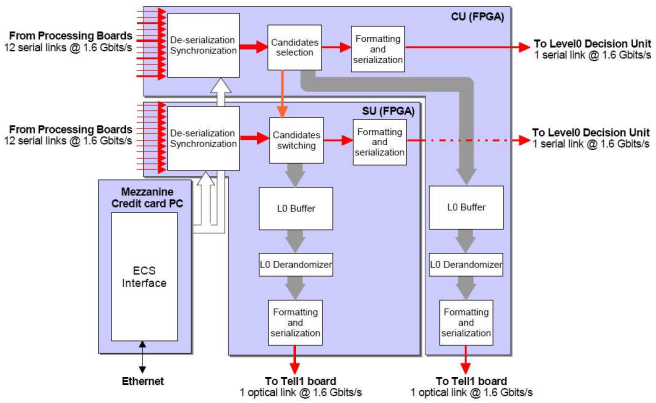

Figure 9: Synoptic of the controller board.

The synoptic of the controller board is shown in Figure 9. It contains two FPGAs from the Stratix GX family: one CU and one SU. High speed serializer/deserializer are embedded in FPGAs. The board shares a lot of common functionalities with the processing board: same embedded PC, same L0-buffer/L0-derandomizer mechanism. The role of the board is (i) to broadcast all the control, clock and reset signals received from the TTCrx [6], (ii) to collect the best candidates coming from the processing boards, and (iii) to select the two with the highest p_T and to send them to the L0 Decision Unit.

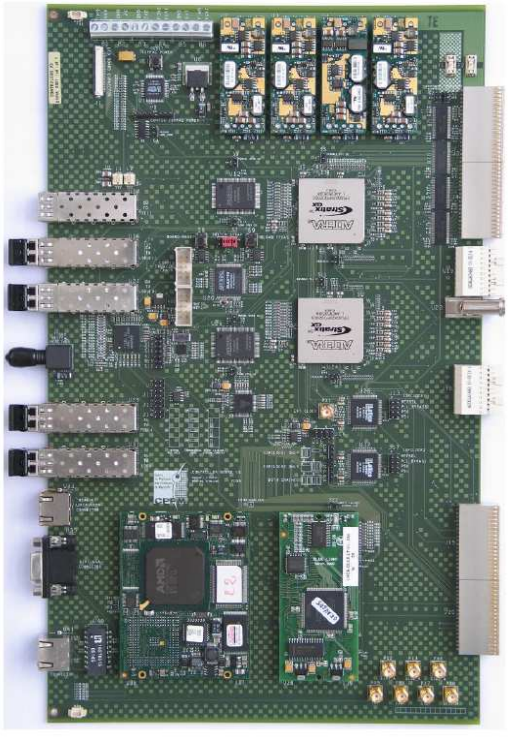

Figure 10: Top view of the controller board.

The board shown in Figure 10 is implemented in a 366.7 × 220 mm format. Its printed circuit board is composed of 14 layers where 948 components are mounted. The power consumption is lower than 50 W.

D. Backplane

The backplane contains 15 slots: 12 for the processing boards, one for the controller board and two for test. The latter allow to check a processing board by looping its outputs on its inputs.

The backplane shown in Figure 11 is implemented in a 395.4 × 426.72 mm format. Its printed circuit board is composed of 18 layers.

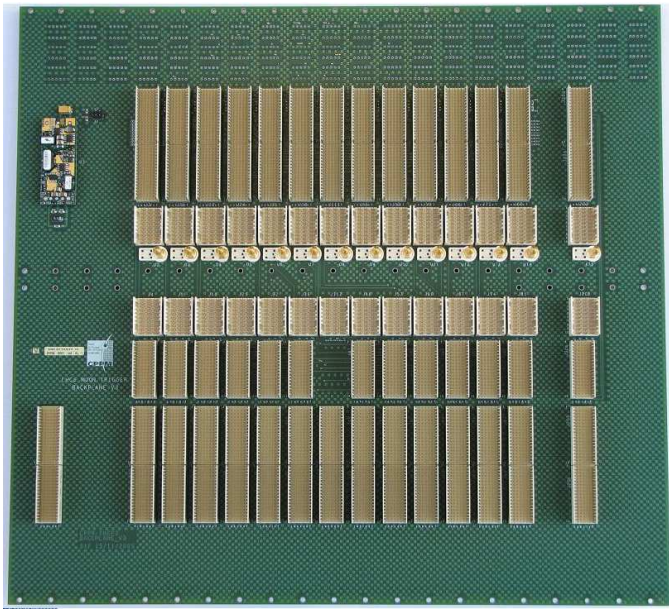

Figure 11: Top view of the backplane.

IV. Debugging and Verification Tools

Each board embeds a PC running Linux which is interfaced to FPGAs by a custom 16 bits bus. Therefore, we can control the operation of any FPGA of the system and monitor its status through error detection mechanisms, error counters, spy and snooping mechanisms.

A. Testability

To test a complete processor in a stand alone mode, we implement data injection buffer which can be substituted to the input data. Results of the processing can be read back by the embedded PC at the output of the L0-derandomizer buffer as shown in Figure 12.

B. Verification

The level-0 muon trigger is a very complicated system. Any malfunction can therefore be difficult to understand and interpret. At each stage we log the input and results of the processing. A PU produces 512 bits per bunch crossing resulting to 2,300 bits for a board and to 30,000 bits for a processor. To handle such a quantity of information, we have developed a software emulator reproducing the behaviour of the hardware on a bit to bit basis. By comparing hardware reports with outputs of the emulator run on the same input data, we can point out any faulty components.

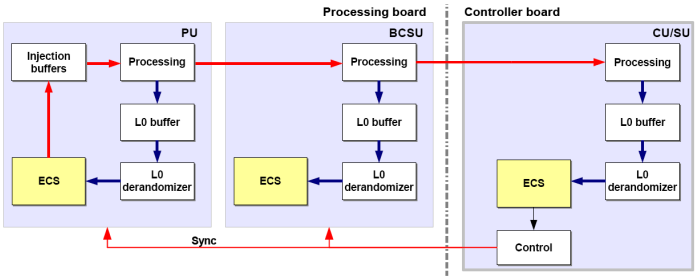

Figure 12: Data injection buffer and read back system.

V. Conclusion

The level-0 muon trigger is a very complex system. We have developed a very challenging architecture based on 248 large FPGAs exchanging data on 2272 high speed links at 1.6 Gbits/s among which 920 component-to-component or board-to-board copper links. 18432 tracking algorithms are permanently running in the system and deliver a result every 25 ns.

All tests demonstrate that the hardware is functional. We have checked, exhaustively, data path integrity by programming FPGAs in a mode where every possible output is toggled at maximum rate. The large number of multigigabit serial links proves to be very reliable.

A very good visibility on each internal node of such a complex system is mandatory. We have developed powerful hardware/software test mechanisms. Their purpose is to help us to understand and to validate the trigger behaviour during the debug and commissioning phases.

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Installation and Test of the ATLAS Muon Endcap Trigger Chamber Electronics

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Abstract

For the detector commissioning planned in 2007, a sector assembly of the ATLAS muon endcap trigger chambers is being progressed in CERN. Final technical test of the electronics mounted on a sector must be made at this stage. For systematic test of the electronics (sector test), we have developed a DAQ system on top of the ATLAS online software framework. The system is not dedicated only for this test, but can be used also for the front-end detector part of the overall ATLAS DAQ system. In the presentation, the procedure, meaning and results of the sector test are discussed after brief introduction of the TGC electronics and the sector structure as a construction unit. We introduce plans of further detailed and elaborated tests for the whole system using cosmic ray and single halo muons when all the TGC sub-detector part is completed as concluding remark.

I. INTRODUCTION

Sector assembly and installation of the ATLAS muon-endcap chambers is being progressed in CERN for the detector commissioning in 2007. The thin gap chamber (TGC) is used for the muon-endcap trigger system [1]. The muon endcap system covers the both endcaps of the detector ($1.05 < |\eta| < 2.4$) to detect isolated muons and give the level-1 (LVL1) muon trigger signal with two ranges of the transverse momentum (pt) of low-p_T > 6 GeV and high-p_T> 20 GeV [2].

As at least three measurement points per track is necessary to identify a muon with even such coarse momentum estimation, there are three TGC stations per endcap (one (M1) has triplet chambers to measure three track points for a muon, and the other two stations (M2 and M3) have two measurement points for a muon each with doublet chambers). Every station has commonly twelve sectors to form a wheel. This 1/12 sector is an installation unit for the trigger muon endcap system for both the chambers and electronics. The sector is also the unit for the trigger and readout system.

A. Overview of TGC electronics system

Fig. 2 summarizes a structure of the TGC electronics system [3]. Electronics components are divided into two parts; on-detector and off-detector ones. The on-detector part is further separated into two parts, one is called Patch-panel and Slave board that is installed just behind the chamber (we call this unit as PS-board) and the other one is Hi-p_T and Star

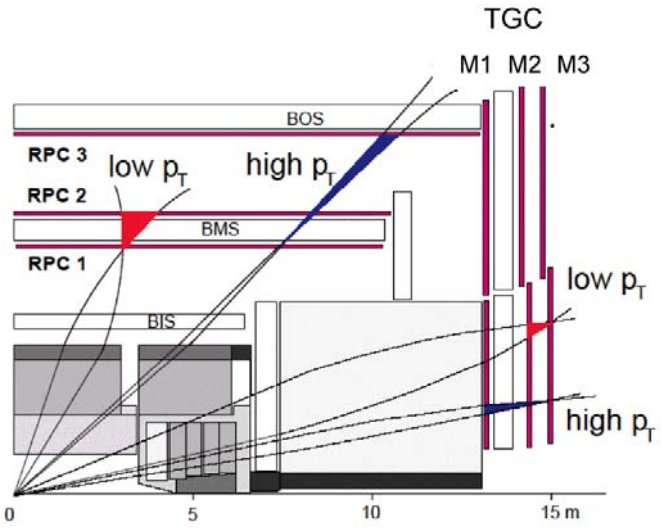

Figure 1: TGC Chamber layout in RZ plane of ATLAS endcap

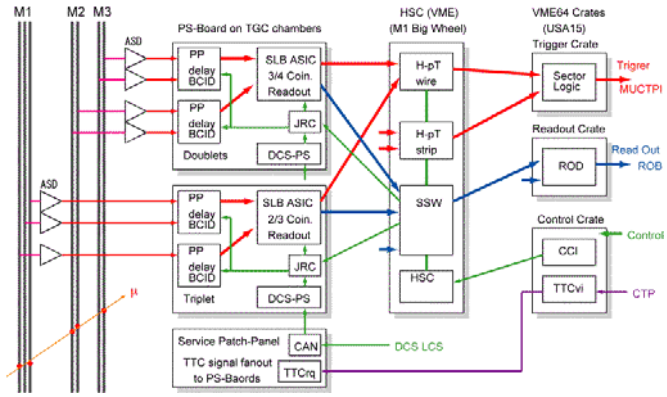

Figure 2: TGC Electronics Overview: The system is divided into three parts, two on-detector parts and one off-detector part.

Switch Control (HSC) crate that is installed at the outer rim of M1. A PS-board and an HSC crate are prepared for each 1/12 sector.

Digitized chamber-signals from Amplifier- Shaper-Discriminator (ASD) boards [4] attached directly to TGC are inputted to Slave Board ASICs (SLB IC) after synchronized and bunch crossing identified in Patch-panel (PP) ASICs (PP IC). SLB performs local coincidence to identify muon tracks

coming from the interaction point with $p_T \geq 6$ GeV, and output information of r, ϕ and Δr, $\Delta\phi$ for every muon candidate (low p_T coincidence with 2-out-of-3 logic using M1 or 3-out-of-4 logic using M2 and M3). The PP and SLB ICs are mounted together on a PS board. The PS board mounts also electronics for the detector control system (DCS) [5]. The output signals of SLB are fed into a Hi-p_T board, which is installed in an HSC crate and is approximately 15m away from the corresponding PS board. The Hi-p_T board contains Hi-p_T ASICs (HpT IC). An HpT IC combines information from two (for doublet) to three (for triplet) SLB ICs to make a global coincidence to find muon tracks with $p_T \geq 20$ GeV (hi p_T coincidence). HpT IC also makes data compression to send its output over a distance of about 90m with serial data transmission to the counting hut where the off-detector electronics are installed.

Signals for r (wire hit information of TGC) and ones for ϕ (strip) are separately processed in the independent streams up to hi-p_T coincidence operation, and the sector logic (SL) installed in the off-detector part combines these two streams and makes a coincidence in r-ϕ to identify muon signals in two dimensional space. At maximum two highest p_T muon candidates per trigger sector (72 trigger sectors/side) are selected after successful r-ϕ coincidence, and the information is sent to the MUCTPI (ATLAS level-1 MUon Central Trigger Processor Interface) [6]. Functionalities and design concept of the three main ASICs (PP, SLB and HpT) have been discussed in detail in [7].

So far we have discussed the on-detector parts of the electronics system. Since the electronics components used in the on-detector parts will suffer the total ionization dose for ten years of about 150 to 210Gy (15 to 21krad), and about 2 hadrons/10cm^2. The both values contain some safety factors. The ionizing dose will degrade gradually the functionality of the electronics and hadrons will damage them as single event upsets. We have, thus, checked the radiation tolerance of the components used in the system by irradiating them with γ-ray and proton beam for the same values as dose and number of hadrons estimated for ten years. We have used only the components, which clear conditions of the radiation tolerance tests. The details of this discussion will be found in [8].

Since hit information for both coordinates will be used not only for the trigger decision logic but also for the second coordinate information for the ATLAS muon reconstruction in offline analyses, a readout system must be implemented. Readout data are processed also in SLB ICs, each of which implements pipeline buffers during the LVL1 processing time and FIFO for selected events (de-randomizer). At every LVL1 accept (L1A) signal, data are serialized in SLB ICs and sent to a data distributor/concentrator, which is so called Star Switch (SSW). One SSW has 18 SLB IC inputs and one output. A sequential process of receiving data from SLB, storing in FIFO, format analysis and output to Readout Driver (ROD) will be done for all used channels in turn under the VME control. Basic concepts and functionalities of SSW will be found in [9].

ROD receives data from total several SSWs, the nuer depends on the configuration. Data received are stored in FIFO, which is prepared for every input channel. All the data stored in FIFOs are merged if these data have an identical L1A identification number. ROD sends data to the ATLAS central DAQ facility in the end.

The functionality, validity of the trigger logic and timing margin of the chain from the front-end ASD (actually using TGC) through both the trigger and readout lines up to central online data acquisition system has been confirmed in two test-beam experiments in 2003 and 2004 done at CERN SPS H8 muon beam dump facility [10].

B. 1/12 Sector as a unit of construction

In Fig.3 a photograph of one 1/12 sector is shown. From this photograph, one can find all the on-detector components of the TGC electronics system; the PS boards are mounted on the chamber surface while the HSC crate is put at the outer edge of the sector. This HSC crate handles signals of all the three corresponding sectors (of M1, M2 and M3), and mounted only on the M1 station.

Once the sector is installed in the whole ATLAS detector system in the cavern, one cannot access easily its electronics as well as cables. We have to test the electronics system after completion of the sector assembly and fix or repair quickly if we find incomplete connection of cables or damage of electronics components. Furthermore since the system involves the LVL1 trigger generation logic, confirmation of functionality of timing adjustment of the delay logic at this assembly stage is also the key issue from the signal synchronization point of view.

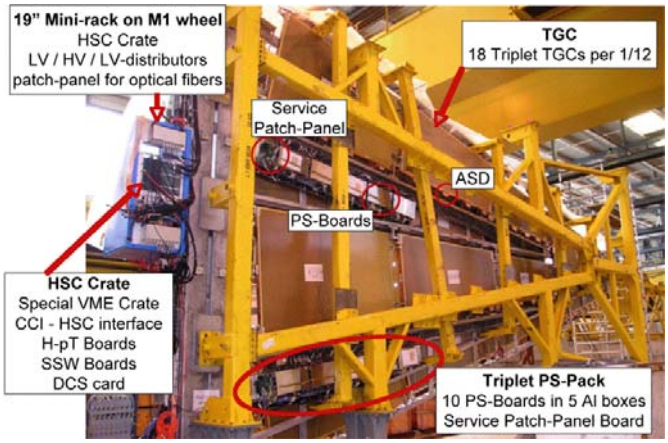

Figure 3: Setup of the on-detector components (M1)

In order to check all the functionalities and adjust timing of the electronics system, it is necessary to do almost full DAQ operation to the sector. We have made a lot of DAQ systems so far for the standalone electronics consistency check or the integrated beam tests with TGCs using the high energy muon beam. These DAQ systems constructed have been dedicated for specific purposes, but none of them can be used in the actual ATLAS online system, although various software codes in particular for individual module controls are re-

usable with minor modification. For the present electronics test of the sector assembly, we have reformed the DAQ system once more. We made it with being fully complied with the ATLAS online software framework [11].

In the following section we describe the installation and mass-test procedure of electronics using this DAQ system in detail and some experience to fix problems encountered actually in the sector assembly. We would like to discuss the timing adjustment procedure in detail. If the adjustment in the sector level is done well, then the timing signals in larger parts (whole M1, M2 or M3 station, each endcap-side or overall muon endcap) will be smoothly synchronized.

II. Construction and Test of Sectors

As discussed in the previous section, every station (M1, M2 and M3) of one endcap-side is divided commonly into twelve sectors. This sector is a unit of the TGC construction as well as the electronics segmentation. Although the chambers have been constructed in different countries of the collaboration, the sector assembly is being done in a building of CERN west area. Once one sector is assembled and passed an electronics connection test (we call this as sector test), the sector is carried to the ATLAS pit for the installation. After the installation of the M1 station is completed, then M2 and M3 stations will be followed for one side. Then the same procedure will be repeated for the other side.

Since it may be difficult and complicated to repair electronics as well as cables in the sector if it is installed in the detector in the ATLAS cavern, a careful and cautious check for hardware of the sector must be done at this stage, and the test should concern to check full facility and connectivity of electronics and cables for a sector. Functionality of all the readout chains is thus checked with this test using and signals readout by the off-detector test-ROD. The outputs of the test-ROD are checked in order to

- find and correct any wrong or loose cable connection,
- find and repair damaged hardware components, and
- confirm several basic functionalities of PP and SLB ICs (adjustability of delay timing and/or mask patterns) .

The delay timing adjustment is a key-issue for the test since all the channels in the sector must be synchronized at this stage.

The signal flow diagram of the electronics setup for the sector test is shown in Fig. 4. We inject a few hundreds of test pulses generated by TTC system [12] to all the channels concurrently in the test. The results are displayed in histogram style and we will see some mal-forms or malfunctions of the electronics from histograms. Each station has several layers (three layers for triplet and two for doublet). The test is done separately for each layer. From histograms shown in Fig. 5, for example, we can see a hole at the last channel in the top histogram but any other histograms. A channel hole means one missing channel that may come from insufficient connection of a cable, damaged cable, defective electronics, or dead channel in the chamber, though we cannot focus the exact point where the problem occurs actually from the histograms. After several inspections of various parts by hand, we can identify the problem.

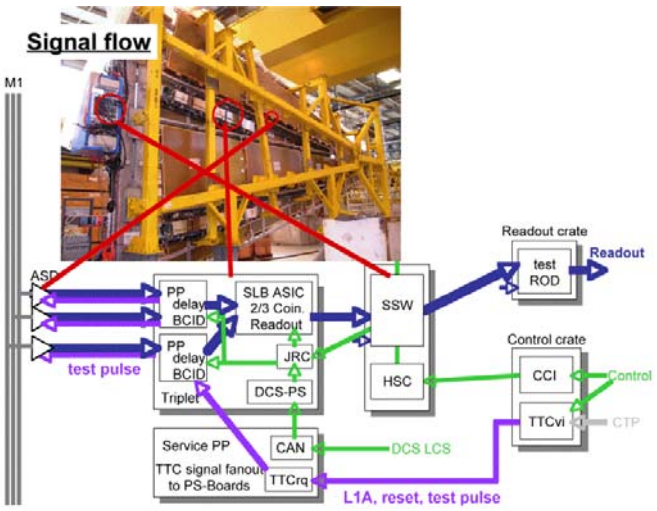

Figure 4: Diagram of the electrical signal flow for the sector test

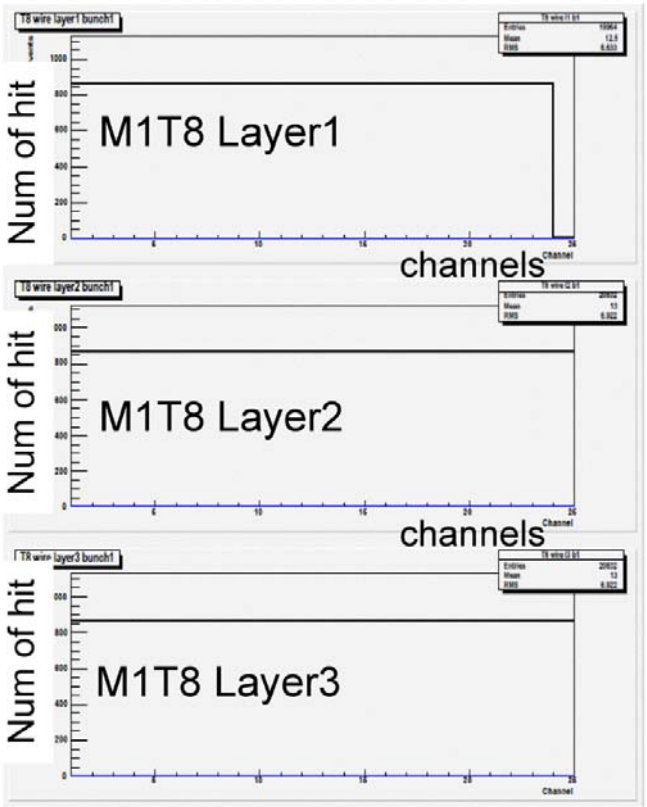

Figure 5: An example of signal detection problems found in the sector test The example are results of a sector test for M1 (triplet)

Changing the delay value to be set in the individual fine-delay adjuster facilitated in a PP IC, we can obtain delay curves. The fine delay for a channel can be set in precision of 25ns/32bit (~0.78ps step) where 25ns is a bunch-crossing interval of LHC. In each fine-delay value, we count how many test-pulses (events) are recognized in an interval of

each of previous, current or next bunch. At the sector test the delay curves for all the channels are accumulated. An example of the delay curves is shown in Fig. 6. From this figure, we can find that test pulses delayed between -50 and -25ns from the nominal delay are all detected in an interval of the previous bunch crossing signal, those between -25ns and 0ns are all detected in the current bunch. We can also find that if we advance the timing signal up to 25ns, then all the pulses are regarded as ones occurred in the next bunch, and no pulses detected rather than this bunch. With this result, we can conclude the timing adjustment unit in a PP IC works fine.

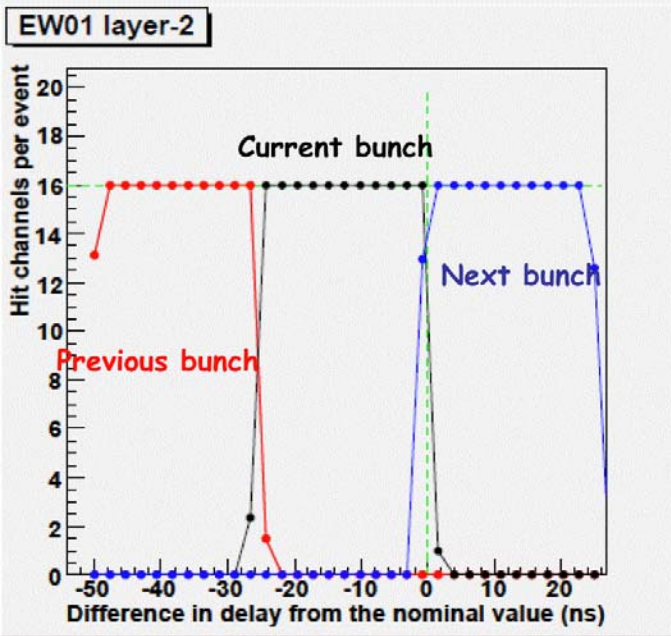

Figure 6: An example of Delay curve obned in a sector test

III. Summary and Outlook

A. *Summary of the Sector Assembly and Test*

In Fig. 7 we have shown the progress rate of the sector assembly. The abscissa is the days we have spent while the ordinate is accumulated number of sectors constructed so far. In the sector assembly site we have two assembly sections (called Jura and Salève in the figure). The assembly is made in parallel at two sections. From the slopes of the lines depicted in the figure, we can find that we need in average one week for one sector assembly including the test whose procedure we have described in the previous section. At the time of writing this document, we have finished the assembly of all the sectors (twelve) for one side of both M1 and M2. Figure 8 shows a picture of the whole M1 station completed in the ALTAS pit. Up to end of 2006, we will finish the whole sector assembly for one endcap unless we have serious problems in the sector assembly stage and/or installation in the pit.

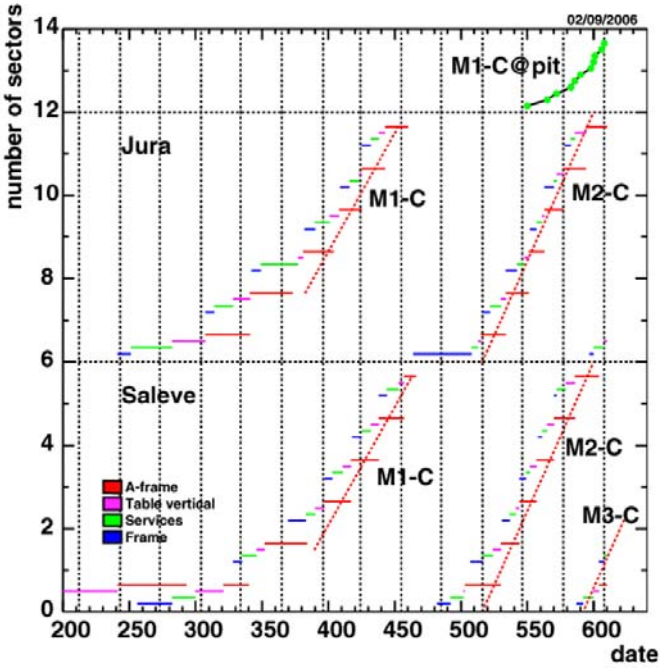

Figure 7: The integrated number of sectors constructed as a function of time (day) for assembly sections (called Jura and Salève). On top of these curves, the rate of the sector installation at the ATLAS pit is also shown in the figure.

B. *Cosmic Ray Test*

As we have discussed, we cannot test in detail the logic chain of the LVL1 endcap muon trigger while we can make debug and adjust the readout chain of our electronics with the sector test. The trigger generation logic must be also debugged and its full functionality must be confirmed in due course. The independent logic chain consists of the coincidence matrices of both low-p_T (implemented in SLB IC) and hi-p_T (implemented in HpT IC) and the r-ϕ coincidence logic implemented in the SL module. One interesting idea to confirm the functionality of this trigger path is to generate cosmic muon triggers using the TGC-trigger logic. We may have such a possibility although the original TGC (including electronics) setup for ATLAS endcap muon detection must be slightly modified.

Since the trigger logic assumes that a muon ordinarily comes from the interaction point to TGC with the dip angle between 40 and 90 degrees (the trigger towers (formed with M1, M2 and M3) always head toward the interaction point), the quite low acceptance will be anticipated if we use the coincidence logic with full three stations (a triplet one and two doublet stations). If, however, we relax the condition to recognize a cosmic muon only with one station (using only the inner most triplet M1 or the outer most doublet M3 with supplying faked signals to the other stations), cosmic triggers will be generated with a reasonable rate using the current setup of the coincidence matrices. If the service lines for TGC (gas, high voltage and optical fibre connection) are completed (at around December 2006), we will immediately begin this project.

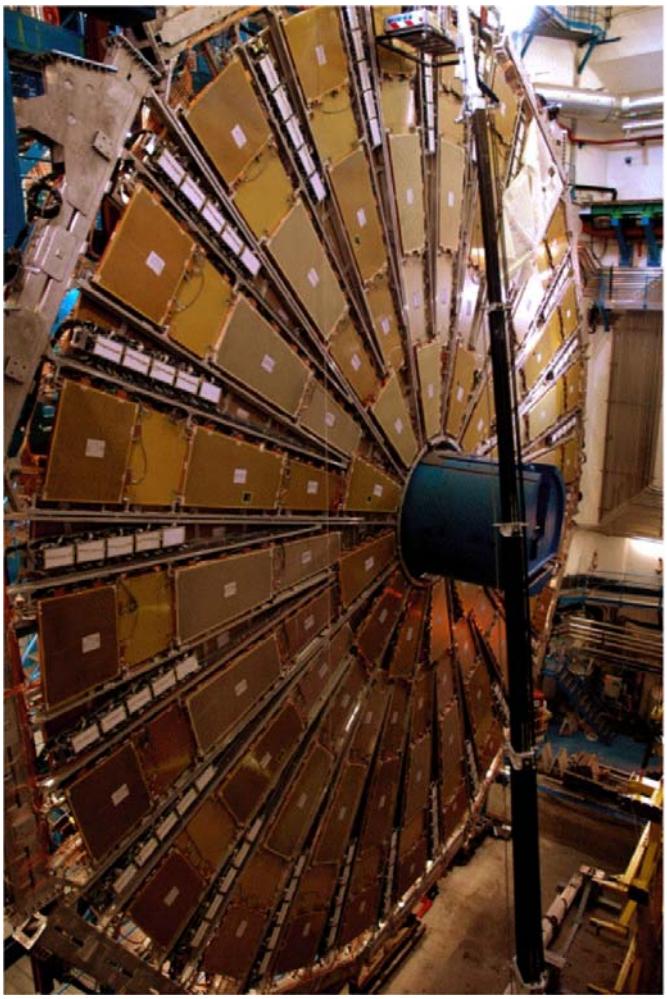

Figure 8: The completed M1 station of TGC in the ATLAS pit (Sept., 2006)

C. *Single Beam Halo Run*

When LHC is running in single beam mode before collision, we can check also our trigger logic using muons that produced in scattering of proton with residual gas in the beam pipe. In the trigger logic the chamber output signal must be synchronized roughly at the input of PP IC (the input of the trigger logic). Although this timing measured from the common bunch-crossing (BC) time is fluctuated among channel by channel due to different time of flight (TOF) of muon from the interaction point and different cable length, rough correction of timing fluctuation can be overcome if we know the distance between a chamber surface point and interaction point as well as the cable length (coarse delay setting). Since a low p_T coincidence matrix is installed in an SLB IC, the signals after PP IC are precisely made synchronized at the input of the SLB IC. This synchronization can be achieved using a fine delay adjuster with sub-nanosecond level implemented in a PP IC as discussed in the previous sections. In principle we can adjust timing up to the input of SLB for all the channels already in the sector test. But this adjustment is done sector by sector independently. We must confirm this synchronization over all the channels using the single beam halo run.

Since the BC timing will be available even in the single beam running mode, and the scattered muon will come into TGC in parallel with the beam, the low-pT, high-pT and r–ϕ coincidence logics will work fine without any modification of the logic configuration for halo muons. If we can have coincidence signals at the very end of the trigger logic, i.e., at the output of the SL (Sector Logic) as the consequence, it then means that the synchronization at the SLB input is well adjusted over sectors and even over stations. There is, however, an issue to do this test because the muon will hit the TGC before the BC timing if the beam and scattered muon come parallel into the detector at the same time, and the TGC is in front of the bunch crossing point. A simple idea to get over this issue is to re-adjust the coarse synchronization at the input of PP IC with TOF = -TOF (just reverse the sign).

Although we are not yet fixed when we do this test because it depends on the LHC running schedule, we foresee to have this test by the end of 2007.

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Parallel Session B3

Trigger session 3

Commissioning of the ATLAS Level-1 Central Trigger

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Abstract

The ATLAS Level-1 Central Trigger consists of the Central Trigger Processor (CTP) and the Muon-to-CTP-Interface (MUCTPI). The CTP receives trigger information from the Level-1 Calorimeter Trigger system directly, and from the Level-1 Muon Trigger systems through the MUCTPI. It also receives timing signals from the LHC machine, and fans them out along with the Level-1 Accept (L1A) signal and other control signals to all sub-detectors. From them, it collects BUSY signals in order to throttle the L1A generation. Upon L1A the Level-1 trigger systems send region-of-interest information to the Level-2 trigger system.

The MUCTPI and CTP crates are already installed in the ATLAS underground counting rooms with final or close-to-final boards. We present their status and discuss first commissioning steps. Particular emphasis is put on the integration of the Central Trigger with the Muon and Calorimeter Trigger systems, the Level-2 trigger, and the readout part of the different sub-detectors.

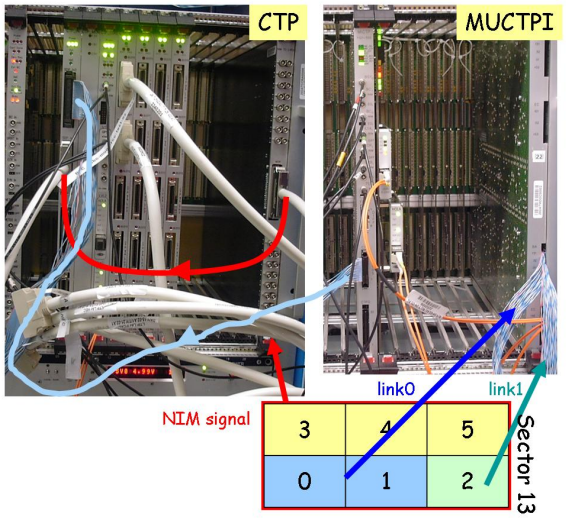

Fig. 1. The CTP and MUCTPI crates installed in the underground counting room. The sketch at the bottom illustrates the connection to the sector 13 barrel muon trigger chambers.

I. Introduction

The ATLAS Level-1 trigger [1] is a system that synchronously processes information from the calorimeter and muon trigger detectors, at the bunch crossing (BC) frequency of 40 MHz. It consists of three parts: the Level-1 Calorimeter Trigger (L1Calo), the Level-1 Muon Trigger (L1Muon), and the Level-1 Central Trigger. The latter consists of the Central Trigger Processor (CTP) [2] and the Muon-to-CTP-Interface (MUCTPI) [3]. The MUCTPI receives muon trigger candidate information at 40 MHz from the barrel muon trigger (RPC) and end-cap muon trigger (TGC) chambers, and subsequently forms muon multiplicities for six different transverse momentum (p_T) thresholds. These data are sent to the CTP as trigger inputs. From L1Calo, the CTP receives electron/photon, tau/hadron and jet candidates as well as global energy information.

From this information the CTP makes the final Level-1 Accept (L1A) trigger decision according to a programmable trigger menu. The L1A is then fanned out to all sub-detectors to initiate readout of the triggered event. In addition, the Level-1 trigger systems send region-of-interest (RoI) information to the Level-2 trigger, and also take part in the combined readout of ATLAS.

In section II we describe the status of the current Central Trigger installation. Section III illustrates the integration tests done with inputs from the L1Calo and L1Muon systems, while section IV is about the commissioning of the Central Trigger system itself. In section V we report on integration tests concerning the distribution of trigger, timing and controls signals to the sub-detectors, the Central Trigger readout and the link to Level-2. Results from cosmic muon data-taking runs with the combined readout of a number of different sub-detectors are discussed in section VI.

II. Status of the Central Trigger Installation

A demonstrator of the MUCTPI and a crate of final CTP modules are already installed in the underground counting room next to the ATLAS experimental cavern. Figure 1 shows the two crates: the CTP crate on the left and the MUCTPI crate on the right. The cabling is explained in section III-B.

The demonstrator version of the MUCTPI provides almost the full functionality of the final system, but misses some flexibility in the handling of overlaps (see [4]). One input board (MIOCT) out of 16 is currently installed, corresponding to one octant in azimuth of one half of the detector. It provides 14 trigger sector inputs (out of 208) to be connected. Currently there are 2 RPC prototype sector logic modules connected (see [5]). In addition to the input boards, the MUCTPI chassis contains the MICTP, MIROD, and MIBAK modules. MIBAK is a custom active backplane used for readout and muon multiplicity summation. The MICTP is responsible for the

timing distribution within the crate and for providing muon multiplicities to the CTP. The readout driver MIROD formats the muon candidate data before transmitting them via S-LINK [6] to Level-2 and the readout system.

The CTP crate is installed with final modules only. It contains one input board (CTPIN), receiving up to four trigger signal cables from the Level-1 calorimeter trigger system and the MUCTPI. Two CTPIN boards are yet to be installed. The CTP crate contains in addition the machine interface (CTPMI), the CTPMON, CTPCORE, and 4 CTPOUT boards, a NIM-to-LVDS converter module, and a custom-made backplane. The CTPMI provides the clock and the orbit signals. The CTPMON monitors trigger input signals per bunch crossing identifier. The CTPCORE is responsible for the Level-1 trigger decision based on a configurable trigger menu. In addition, it formats the CTP data to be sent to the readout system and the Level-2 trigger. Finally, the CTPOUT modules fan out the trigger and timing signals to the sub-detectors.

III. Commissioning of Trigger Inputs

Two tests have been performed so far to ensure that the trigger signals are properly received: one with the L1Calo output board, and one with the barrel muon trigger.

A. Level-1 Calorimeter Trigger

An integration test with L1Calo has been performed in July 2006. A final L1Calo Common Merger Module [7], which provides the L1Calo trigger signals to the CTP over a 12 m long cable, was programmed to send a known pattern at 40 MHz to one of the four inputs of the CTPIN. There, the pattern was captured in a memory and compared to the original pattern. A minor firmware issue was discovered in the treatment of parity, but no data transmission errors were found over a period of 15 minutes.

B. Level-1 Barrel Muon Trigger

In sector 13 of ATLAS, 2 barrel middle and 2 barrel outer chambers were fully equipped with cables and services, providing 6 trigger towers with 3 layers of RPC chambers. Their trigger logic provided trigger signals to two prototype sector logic modules, which were connected to the MUCTPI through 2 links: link0 corresponded to tower $0+1$, and link1 to tower 2. A trigger signal (NIM) formed from all 6 towers was separately fed into the CTP via the NIM-to-LVDS board in the CTP crate. The cabling is indicated in Figure 1.

The phase of the clock in the MUCTPI was adjusted with respect to signals sent through link0 and link1 and the clock edge chosen to sample the input signals correctly. The MUCTPI has then successfully sent muon multiplicities to one of the inputs of the CTP.

The NIM trigger signal from the whole of sector 13 was converted into LVDS by the NIM-to-LVDS board in the rightmost slot of the CTP crate (see 1), and then passed to one of the inputs of the CTPIN board. In the CTPIN, the phase with respect to the clock of both the muon multiplicities from the MUCTPI and the NIM trigger signal was measured and the clock edge chosen accordingly. Since the NIM trigger signal did not pass through the MUCTPI, it arrived at the CTP 6 BC earlier, corresponding to the latency of the MUCTPI. It had therefore to be delayed by 6 BC in the CTPIN to be in phase with the muon multiplicities coming from the MUCTPI.

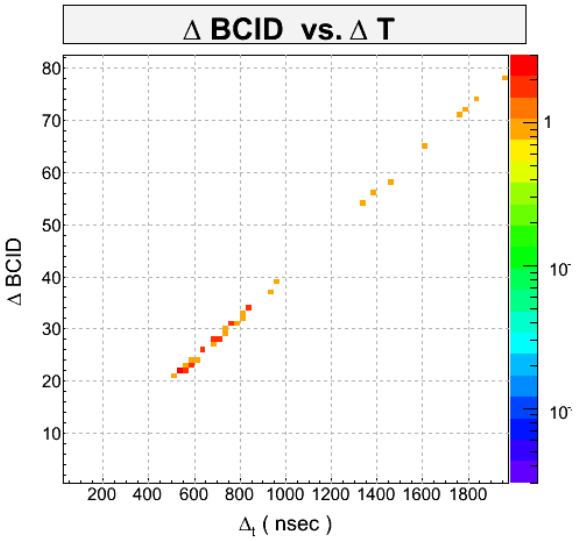

Fig. 2. Correlation of the difference in bunch crossing identifier and time-stamp in the CTP for consecutive events.

IV. Commissioning of the Central Trigger

The Central Trigger hardware is integrated with the ATLAS Run Control online software [8], a state machine which configures the system through a predefined sequence, in which the system is booted, configured from a configuration database, and brought into the running state. The Central Trigger can already be configured from the trigger database [9], and a simple trigger menu has been chosen for the integration with the muon detectors in sector 13: it consists of the logic OR of:

- at least one muon candidate from the MUCTPI for any p_T threshold
- the sector 13 NIM trigger signal.

The mechanism of assigning a GPS-timestamp to each event accepted by Level-1 was tested as well as the simple deadtime algorithm, which asserts a constant, configurable amount of dead-time after each L1A. Figure 2 shows the correlation between the difference in bunch crossing identifier and time-stamp of two consecutive events. The correlation is perfect, and there are no events with differences smaller than 20 BC (500 ns), which is in accordance with the deadtime settings for this particular run.

Basic monitoring software tools were used to display online the global dead-time and its various contributions, the number of L1As in the CTP and MUCTPI, and the muon multiplicities in the MUCTPI.

V. Commissioning of Trigger Outputs

This section describes the commissioning exercises performed with the trigger outputs, which are of three different types:

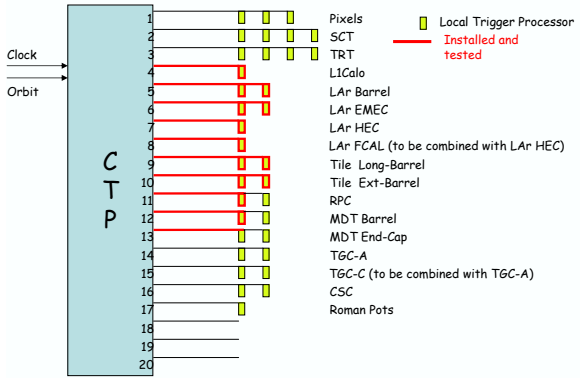

Fig. 3. CTP links to sub-system partitions.

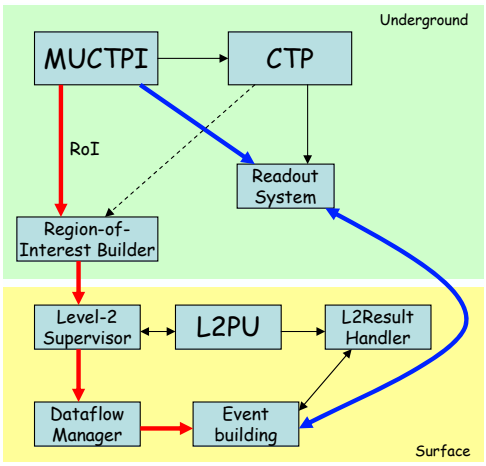

Fig. 4. Setup of the integration tests with the Level-2 trigger.

- trigger, timing and control signals being sent to all sub-detectors,
- readout links, and
- RoI information sent to the Level-2 trigger.

A. Sub-detector trigger, timing and control signals

The CTP supplies all sub-detectors centrally with a common bunch clock and orbit signal, as well as the L1A and other control signals. The bunch clock and orbit signals can either be received from the LHC machine [10], or generated in the CTP for running without beam. The sub-detectors taking part in the combined readout can put back-pressure on the CTP in order to throttle the generation of L1As. This is done via a BUSY signal sent back to the CTP.

The CTP can be connected to 20 sub-systems via differential links with a length typically between 10-30 m. The Local Trigger Processor (LTP) [11] is an interface module used by all sub-detectors to receive the signals from the CTP. In addition, it has the capability of using the signals from local sources such that it can act as a local trigger master, mimicking the CTP. ATLAS is organised in several timing, trigger and control partitions, each corresponding to one LTP and serving a part of a sub-system. Several LTPs can be daisy-chained in order to reduce the number of links to the CTP to below 20. Figure 3 shows the current view on how the CTP will be linked to the various sub-system partitions. Each little box corresponds to an LTP, and the thick lines indicate that the corresponding LTP and cable have already been installed and tested in the underground counting room. This is the case for about half of the links.

The distribution of timing, trigger and control signals to the CTP is done internally in the CTP crate through the backplane. For the MUCTPI, which is located in the neighbouring rack, the signals are distributed directly via LEMO cables.

B. Readout links and readout System

The CTP and MUCTPI send their data through S-LINK mezzanine cards and optical fibres to readout system (ROS) PCs [12] that buffer the Level-1 accepted events. The final readout links and ROS machines are already installed, and a stand-alone integration test has been performed: the MUCTPI was loaded with test input data, which caused the CTP to produce L1As and initiate readout in the CTP and MUCTPI. A temporary event-building PC was retrieving the data fragments from the two ROS PCs over the network, combining and writing them to a single data file on the local disk. Offline, consistency between the MUCTPI and CTP data was found for each recorded event. The rate was limited by temporary event-building to about 25 kHz, proving that the back-pressure mechanisms of the readout systems were fully functional.

C. Level-2 Trigger

For each L1A the MUCTPI and CTP send RoI information via S-LINK to the Region-of-Interest Builder [13] component of Level-2. An integration test has been performed with Level-2, where the MUCTPI data from two complementary streams were compared after event-building. The first stream is the final readout path via the readout system PC, the other one is via the Level-2 trigger path (see Figure 4). The MUCTPI data coming from both paths were found to be consistent for each event and no errors were found. A rate of 20 kHz was achieved, limited by the back-pressure of the reduced subset of the Level-2 trigger system.

VI. Combined Cosmic Muon Runs

Combined cosmic muon runs with several sub-detectors being read out were taken in August 2006. Temporary gas systems were operational in sector 13 for both the barrel muon trigger chambers and the precision muon chambers (MDT). Trigger signals were received from the RPC sector logic as described in section III-B. The sub-systems that took part in the combined readout were the RPC, MDT, the central hadronic calorimeter and the Central Trigger (CTP, MUCTPI).

The timing-in of the different readout chains was done by estimating the signal propagation delays in the electronics and cables, and cross-checking by inspection of the data. The readout window of the RPC was set to 1825-2000 ns (70-80 BC), being in line with the budget of 2000 ns (excluding a 500 ns safety margin) for the total Level-1 latency (from the bunch crossing to the arrival of the L1A signal in the front-end of the sub-detectors). Figure 5 shows the latency contributions from the Central Trigger: the trigger signals from the RPC need 3 BC through the cable to arrive at the MUCTPI, which

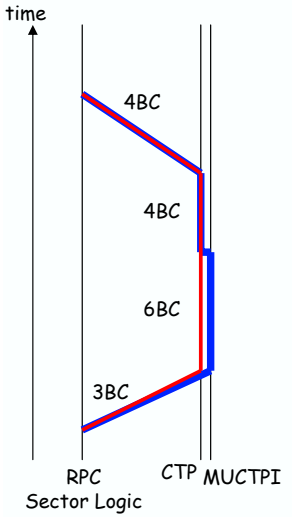

Fig. 5. Space-time diagram of latency contributions by the Central Trigger systems.

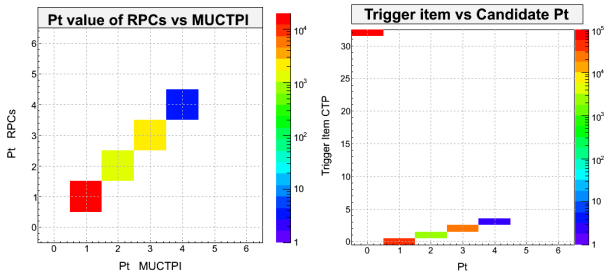

Fig. 6. Left: correlation between the p_T threshold of muon trigger candidates from the MUCTPI and RPC. Right: triggered trigger item number in the CTP versus p_T threshold in the MUCTPI.

takes 6 BC to form muon multiplicities. The multiplicities are further processed by the CTP during 4 clock cycles, before they are sent back to the RPC crate (cable delay of 4 BC). Notice, that the NIM trigger signal arrives directly at the CTP and is therefore delayed by 6 BC (MUCTPI latency) to be in time with the arrival of the multiplicities from the MUCTPI. Both the MUCTPI latency of 6 BC and the CTP latency of 4 BC are within the latency budget required for these systems.

About 500'000 events have been recorded with a rate between 40 and 60 Hz, depending on the configuration of the barrel muon trigger system. Subsequent offline data analysis showed many different correlations between the various sub-detectors: Figure 6 shows, for instance, on the left the p_T of muon candidates as seen in the RPC readout data, correlated with the information as seen in the MUCTPI data. The right picture shows the p_T of muon candidates in the MUCTPI readout data in correlation with the triggered trigger item number in the CTP readout data. As expected, the thresholds 1, 2, 3, and 4 are correlated with trigger items 0, 1, 2, 3, while no candidate (threshold 0) corresponds to trigger item 32. The latter are events where the NIM trigger signal is present, but no muon trigger candidate was found.

VII. Conclusions

The Level-1 central trigger systems CTP and MUCTPI are installed and functional in the ATLAS underground counting room, with mainly final hardware. A complete trigger and readout chain has been successfully operated in the cavern with cosmics, where the CTP triggered on signals from the barrel muon trigger system (sector 13). The RPC, MDT, central hadronic calorimeter, CTP and MUCTPI took part in the subsequent combined readout, whose recorded events were analysed and found consistent. First integration tests with the Level-2 system and the Level-1 calorimeter trigger have been successfully performed.

Acknowledgements

We would like to thank our colleagues from the first-level calorimeter trigger, barrel and end-cap muon trigger, high-level trigger, and data acquisition for their friendly and competent collaboration without which the work presented in this article would not have been possible.

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The Octant Module of the ATLAS Level-1 Muon to Central Trigger Processor Interface

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Abstract

The Muon to Central Trigger Processor Interface (MUCTPI) of the ATLAS Level-1 trigger receives data from the sector logic modules of the muon trigger at every bunch crossing and calculates the total multiplicity of muon candidates, which is then sent to the Central Trigger Processor where the final Level-1 decision is taken. The MUCTPI system consists of a 9U VME crate with a special backplane and 18 custom designed modules. We focus on the design and implementation of the octant module (MIOCT). Each of the 16 MIOCT modules processes the muon candidates from 13 sectors of one half-octant of the detector and forms the local muon candidate multiplicities for the trigger decision. It also resolves the overlaps between chambers in order to avoid double-counting of muon candidates that are detected in more than one sector. The handling of overlapping sectors is based on Look-Up-Tables (LUT) for maximum flexibility. The MIOCT also sends the information on the muon candidates over the custom backplane via the Readout Driver module to the Level-2 trigger and the DAQ systems when a Level-1 Accept is received. The design is based on state-of-the-art FPGA devices and special attention was paid to low-latency in the data transmission and processing.

I. ATLAS First Level Muon Trigger

The ATLAS Level-1 trigger [1] uses multiplicities of e/γ, τ/hadron and jet candidates as well as the global energy information from the calorimeters and multiplicities from tracks found in the dedicated muon trigger detectors to generate the final trigger decision. An overview of the muon trigger system is shown in Figure 1 below.

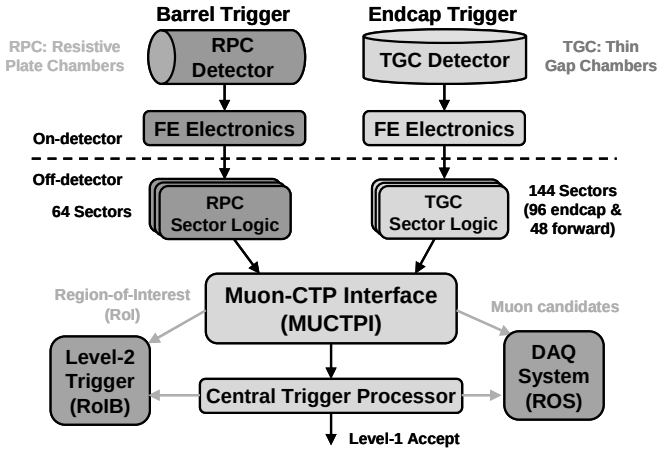

Figure 1: Overview of the ATLAS Level-1 muon trigger

The muon trigger detectors are resistive plate chambers (RPC) in the barrel region and thin-gap chambers (TGC) in the end-cap and forward regions of ATLAS. Coincidences of hits in different detector layers are used to identify muon candidates. The muon trigger electronics also determines the transverse-momentum (p_T) of the muon candidates and classifies them according to six programmable p_T thresholds.

The muon trigger detectors are segmented into sectors, 64 for the barrel, 96 for the end-cap and 48 for the forward region. Each sector can identify up to two muon candidates. At every bunch crossing the detector-specific sector logic sends information about the position and p_T threshold of the muon candidates to the Muon to Central Trigger Processor Interface.

II. Muon to Central Trigger Processor Interface (MUCTPI)

The MUCTPI combines the information from all of the muon trigger sectors and calculates total multiplicity for each of the six p_T thresholds, also resolving possible double counting of muon candidate tracks that traverse more than one detector region, and forwards these multiplicity values to the CTP which takes the final Level-1 decision.

In addition the MUCTPI provides data to the Level-2 trigger and to the DAQ system for events selected at Level-1. The DAQ system receives a formatted copy of the information on candidate muon tracks as well as computed candidate multiplicity. The Level-2 trigger system receives a subset of the candidates, ordered according to decreasing p_T. This information is used to define regions of interest (RoIs) that drive the Level-2 muon-trigger processing.

The MUCTPI has to avoid double counting muons which traverse more than one set of trigger chambers [2], since this would lead to an unacceptably high rate of fake di-muon triggers. This effect is particularly marked for low-p_T muons since their tracks are considerably deflected in the magnetic field of the toroid magnet.

Figure 2 below illustrates the overlap between the barrel and end-cap muon trigger chambers. Tracks for low and high-p_T muons are shown in the barrel and end-cap chambers. In addition an example of a muon track that would be detected in both barrel and end-cap systems is shown. The MUCTPI should detect this case and avoid double-counting this muon candidate in the multiplicity sum.

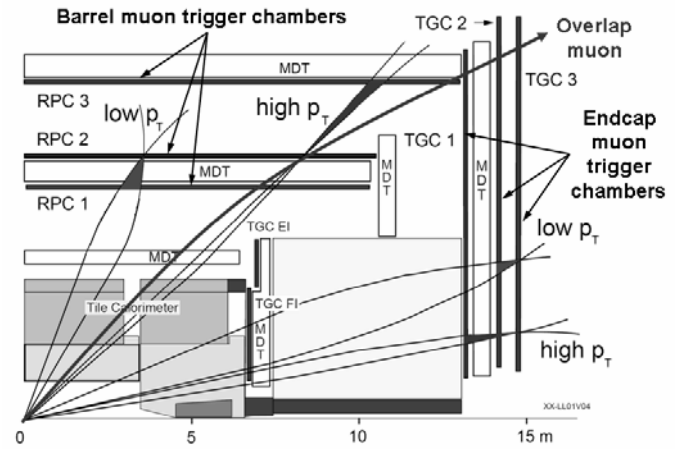

Figure 2: Barrel and end-cap muon trigger chambers

A. MUCTPI Architecture

The MUCTPI system consists of a 9U VME chassis with a special backplane and 18 custom designed modules. 16 MIOCT modules each receive the data from one octant in φ and one half in η of the muon trigger detectors. The MIBAK backplane sums the multiplicities of all MIOCT modules, provides readout data transfer and distributes timing and trigger signals to all modules. The MICTP module receives the timing and trigger signals and forwards the multiplicities to the CTP. The MIROD module collects information from the MICTP and the MIOCT modules and sends the data after formatting to the Level-2 trigger and the DAQ system. Figure 3 shows the architecture of the MUCTPI.

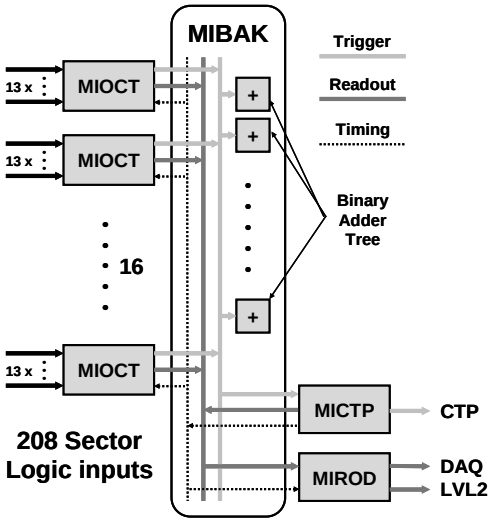

Figure 3: MUCTPI architecture

The different components of the MUCTPI system are introduced in the following sections.

B. MIOCT Module

Each of the 16 MIOCT modules receives the muon candidates from 13 trigger sectors and forms the local muon candidate multiplicities. It also resolves overlaps between the sectors of an octant in order to avoid double-counting of muon candidates. A more detailed description of the design and implementation of the MIOCT module is given in section III below.

C. MIBAK Backplane

The MIBAK is a custom active backplane which receives the muon candidate multiplicities from the 16 MIOCT modules and forms the total multiplicity sums. The multiplicity summing is performed by a binary adder tree implemented using Altera MAX7000 CPLDs for low latency. In addition the backplane implements a bus for the transfer of readout data from the MIOCT modules and the MICTP to the MIROD. This shared readout bus uses a token passing protocol for arbitration and is based on Bus LVDS (BLVDS) [3] signaling. Finally the MIBAK distributes the trigger and timing signals with low-skew to all the modules in the crate. The MIBAK is mounted in the J3 position of the 9U VME crate.

D. MICTP Module

The MICTP module receives the total multiplicity sums for the 6 p_T thresholds from the MIBAK backplane and sends them to the CTP. It also writes the multiplicities into a pipeline for read-out by the MIROD module on reception of a Level-1 Accept from the CTP. In addition the MICTP receives the timing and triggers signals, such as the 40 MHz bunch clock, the Level-1 Accept, the LHC orbit signal and the event counter reset, from the CTP and distributes them through the backplane to the other modules in the MUCTPI crate. The MICTP also provides features for monitoring the multiplicity sums through the VME bus.

E. MIROD Module

The MIROD module is the Read-Out Driver (ROD) of the MUCTPI. For every Level-1 Accept it collects the muon candidates from the 16 MIOCT modules and the multiplicity from the MICTP and sends them after formatting to the data acquisition and Level-2 trigger systems. The standard S-LINK [4] optical link mezzanine cards are used for this purpose. The MIROD also allows reading out the selected muon candidate data via the VME bus for monitoring purposes.

F. MUCTPI Prototype

A working prototype of the MUCTPI exists [5] and a system with one MIOCT has been installed and is being used in the ATLAS underground counting room. Integration tests of the MUCTPI demonstrator with the central trigger processor, the RPC trigger sector logic as well as the DAQ and Level-2 systems have been successful and the system has recently been used in combined cosmic ray data taking runs [6]. Figure 4 below shows a picture of the prototype system with the MIOCT in the rightmost slot and the MICTP and MIROD with the S-LINK mezzanine cards in the center of the crate. The crate also contains a single-board computer (SBC) in the first slot for configuration, control and monitoring.

The existing demonstrator system provides almost all of the functionality and performance required. A redesign of the existing MIOCT prototype was however required, since greater flexibility and programmability is needed for the

overlap handling. In addition only two modules of the original design, which dates back to 2000, were available.

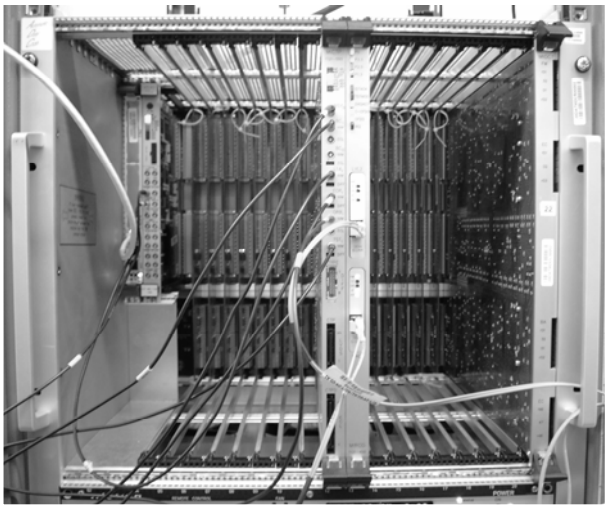

Figure 4: MUCTPI prototype system

III. OCTANT MODULE (MIOCT)

The design and implementation of the revised MIOCT module is presented in the following sections.

A. MIOCT Architecture

The MIOCT is implemented as a 9U x 400 mm VME64x module. The 13 sector logic inputs use 32-bit parallel LVDS signalling at 40 MHz. Serial transmission was excluded because of the latency penalty of ~3 BC due to serialization and de-serialization. Using 2x68-pin high-density dual-stacked VHDCI connectors and low-skew SCSI-3 twisted-pair cable [7], it is possible to fit all 13 sector logic inputs on the front-panel of the module.

Figure 5 below shows the block diagram of the MIOCT module.

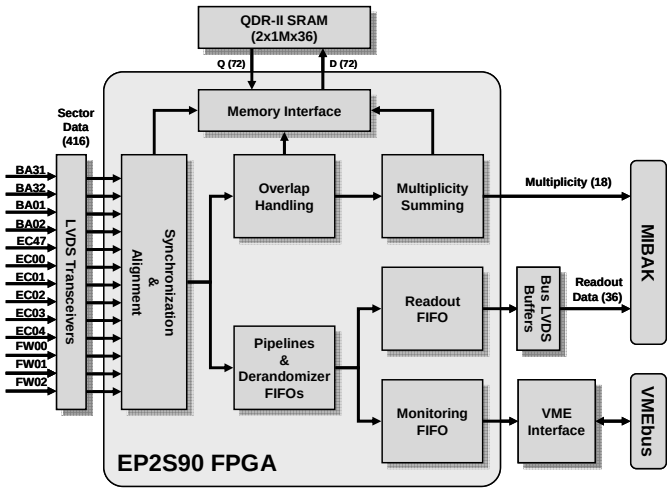

Figure 5: MIOCT block diagram

The main functionality of the MIOCT is implemented in one Altera Stratix II FPGA [8]. This chip features sufficient memory, logic and I/O resources to allow integration of the main MIOCT processing into a single device. There is an additional small FPGA for the VMEbus interface. The implementation is based on the VMEbus interface core [9] which was developed for the modules of the CTP.

Prototypes of the revised MIOCT are currently in production and will be available for testing very soon.

B. Trigger Path

The signals received from the detector sector logic are resynchronized with the system clock received from the MICTP. The incoming sector words are aligned in time to compensate for the different latencies introduced by the RPC and TGC detector specific electronics and the different cable lengths. The MIOCT checks the alignments to be sure that the data word of each sector corresponds to the same bunch crossing.

The multiplicity summing logic counts the number of muon candidates for each of the 6 p_T thresholds, taking into account possible overlaps between sectors. The overlap handling logic suppresses one of the muon candidates if there is a candidate in the corresponding overlap zone of an adjacent sector as well. More details on the overlap handling are given in section D below. The total number of muon candidates is encoded into six 3-bit words and sent to the MIBAK backplane for overall summing.

The internal logic is operated at 4 times the bunch clock (~160 MHz) in order to minimize the latency while maintaining a pipelined architecture. The latency of the trigger path is 3 BC, which is consistent with the existing demonstrator implementation.

C. Readout Path

All the data received from the muon sectors are stored in pipeline memories for the duration of the latency of the Level-1 trigger. In case of a Level-1 Accept, data of all input channels are read out from the pipelines and written into derandomizer FIFOs. The readout window is programmable to ±2 bunch crossings around the trigger. The data in the derandomizer FIFOs are zero-suppressed in order to reduce the data rate on the backplane, formatted and buffered until they are read out via the MIBAK backplane. The data sent by the MIOCT module can also be read out for monitoring purposes using the VME bus.

D. Muon Candidate Overlap Handling

Each MIOCT module receives data from four barrel, six end-cap and three forward sectors of the muon trigger. Figure 6 below illustrates the overlap regions between these sectors, the following types of overlaps between adjacent sectors can be handled by the MIOCT:

- Overlap between barrel sectors
- Overlap between barrel and endcap sectors
- Overlap between endcap sectors
- Overlap between forward sectors

Overlaps of chamber regions within sectors are handled by the detector sector logic. There is no overlap between adjacent octants.

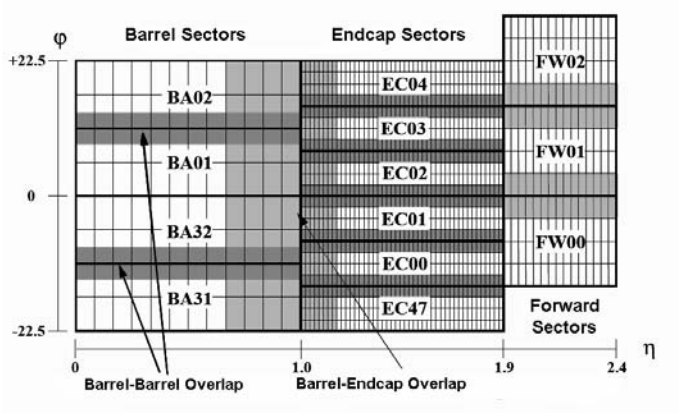

Figure 6: Overlap regions

Figure 7 below shows the block diagram of the implementation of the overlap handling scheme. In the first stage overlaps between muon candidates from different sectors are detected based on their location or sub-sector address and, in the case of the barrel/end-cap overlaps, their p_T threshold and charge sign as well. There is one overlap detection unit for each of the overlap regions listed above. The second stage uses the overlap flags together with a comparison of the p_T values to determine which of the two candidates in overlap should be suppressed. Finally the multiplicity is calculated from the p_T values of the 26 candidates of the octant, ignoring the candidates that are flagged to be suppressed.

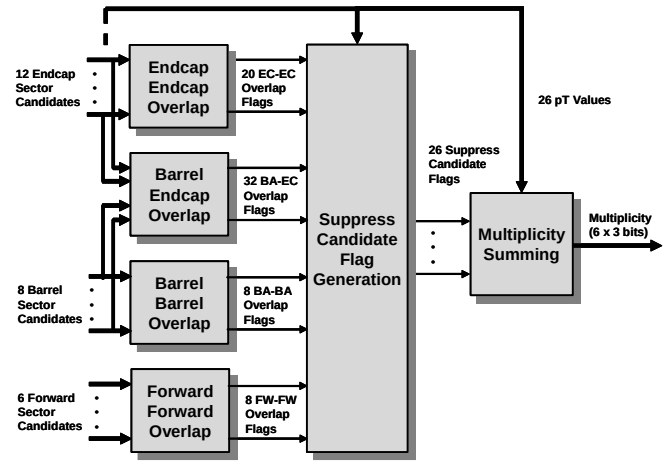

Figure 7: Overlap handling architecture

All the functional blocks of the overlap handling are implemented using programmable look-up tables (LUT). The overlap handling policy can therefore easily be changed by reloading these LUT through the VMEbus interface. The contents of the LUTs will be determined from offline simulations.

E. Snapshot/Test Memory

The MIOCT also features a snapshot and test data memory. The memory can be used to store the data from all 13 input sectors as well as the calculated candidate multiplicity and the candidate suppression flags. This is useful during the timing-in of the system as well as for diagnostics and monitoring purposes. The depth of the snapshot memory is 128K bunch crossings per sector, which corresponds to ~36 LHC turns. For module test purposes, the memory can also be used to replay test data. Since the sector logic LVDS buffers are bi-directional this even allows performing a full functional test of another MIOCT module including the cable connections.

The snapshot/test memory is implemented using two 1M x 36 bit Quad-Data Rate (QDR) SRAM [10] devices. QDR SRAM features independent double data-rate (DDR) read and write ports. The memory devices on the MIOCT are clocked at 160 MHz, resulting in a bandwidth of ~23Gbit/sec for read and write access. The memory interface is implemented using an IP core from Altera. The routing between the FPGA and the QDR SRAM is critical and requires length matching and 50Ω controlled impedance. A signal integrity analysis tool (Cadence SpecctraQuest) was used to validate the termination scheme and the PCB layout.

IV. Conclusions

The MUCTPI interfaces the 208 muon trigger sectors to the CTP. It calculates the muon candidate multiplicities for 6 p_T thresholds and avoids double counting of muons detected in overlapping sectors of an octant. A working prototype system is installed in the ATLAS underground counting room and has been successfully used in combined cosmic data taking runs.

A new MIOCT module has been designed to replace the existing demonstrator. It features a flexible overlap handling architecture and the hardware implementation is highly configurable, being based on look-up tables in a large FPGA device. The new MIOCT will allow a seamless upgrade of the existing MUCTPI system since it is fully compatible with the MIBAK backplane.

V. References

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The ATLAS Barrel Level-1 Muon Trigger Calibration

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Abstract

The ATLAS experiment uses a system of three concentric Resistive Plate Chambers detectors layers for the level-1 muon trigger in the air-core barrel toroid region. The trigger classifies muons within different programmable transverse momentum ranges, and tags the identified tracks with the corresponding bunch crossing number. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut. The on-detector electronics providing the trigger and detector readout functionalities collects input signals coming from the RPC front-end. Because of the different time-of-flights and cables and optical fibres lengths, signals have to be adjusted in time in order to be correctly aligned before being processed. Programmable delay logics are provided in the trigger and readout system to allow for time adjustment, for hit signals as well as for LHC Timing, Trigger and Control signals. The trigger calibration provides the set of numbers used during electronics initialization for correctly aligning signals inside the trigger and readout system. The functionality scheme and the algorithm of the calibration are presented.

I. Introduction

The ATLAS level-1 muon trigger in the barrel region selects and classifies muon candidates with respect of their transverse momentum, and associates their tracks with the correct bunch-crossing number. The muon spectrometer in the barrel region is equipped with a system of Multi Drift Tube detectors for precise particle track measurement, and the Resistive Plate Chamber detectors for the trigger functionality and for the second coordinate measurement. The trigger system processes the full granularity data of about 350.000 trigger chambers channels, reducing the raw rate of 1 GHz proton-proton interactions and 40 MHz beam-beam bunch crossings to 75 kHz, within a maximum total latency inclusive of cable delays of 2 μs.

One RPC detector is composed of two gas gaps, each one being read-out by two orthogonal planes of copper strips, so that each detector has two planes of strips in the bending (eta) view, and two in the non-bending (phi) view. The full barrel system is organised in sixteen radial sectors, each one hosting three RPC detectors, two of them mounted in a middle station inside the air-core toroid, and one in an outer station. Thus a three concentric detectors system is formed, providing six read-out layers per each view (four in the middle station and two in the outer station). Figure 1 shows the position of the RPC detectors on a radial section of the experiment.

The full experiment is divided in two half-parts, side A for positive eta values and side C for negative eta values, so that each ATLAS sector is so divided in two parts, belonging either to positive or negative eta values. One sector side is composed by three planes of RPC detectors (inner, middle-pivot and outer), each plane being formed normally by six or seven adjacent RPC detectors. One ATLAS sector is again longitudinally segmented, from a trigger point of view, in two trigger sectors, so that the global trigger system is structured in sixty-four trigger sectors. A trigger tower is composed by three half RPC detectors (inner, pivot and outer) belonging to the same trigger sector, so that there are six or seven trigger towers per each trigger sector.

The muon trigger algorithm is performed in the bending and non-bending view separately, and is organised in a low-p_T trigger (6 GeV/c transverse momentum cut) and a high-p_T trigger (20 GeV/c). The trigger logic identifies muon candidates coming from the interaction vertex within a p_T range, basing the algorithm on the expected track curvature, and on the hits coincidence within the geometrical roads. The middle RPC detector is used as the pivot plane, while the inner (low-p_T) and outer (high-p_T) RPCs are used as the confirm planes. If a hit is found in the pivot plane, then a confirm hit is searched on the confirm plane, within the desired geometrical road, that is a projection from the pivot layer on to the confirm layers. The road width determines the energy cut. Three different p_T cut per each low and high-p_T trigger can be simultaneously applied. In Figure 2 one quadrant axial section of the experiment is shown, with the trigger scheme illustrated. Figure 3 shows an exemplificative view of the trigger roads, for one trigger sector.

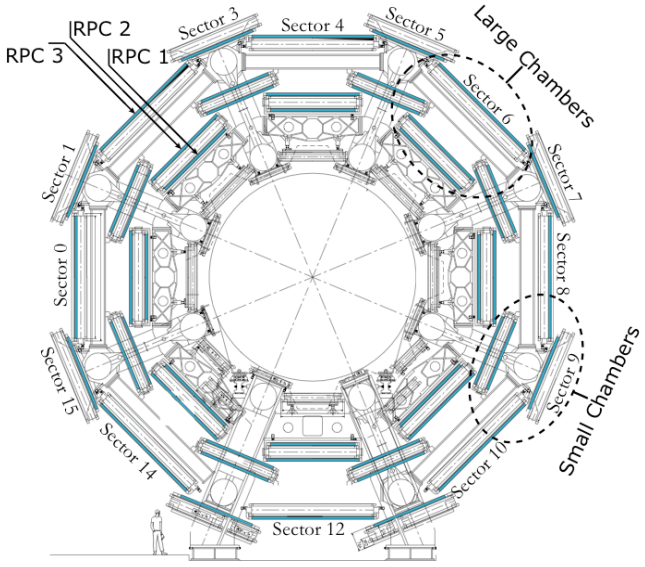

Figure 1: the ATLAS barrel region section, showing the three concentric RPC detectors position into the sixteen-sectors trigger chambers system.

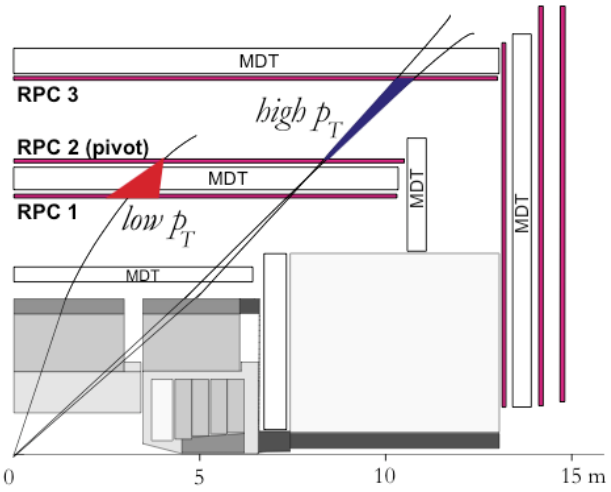

Figure 2: the low-p_T and high-p_T trigger scheme, showing the central pivot detector (RPC2), the inner the low-p_T confirm detector (RPC1) and the outer high-p_T confirm detector (RPC3).

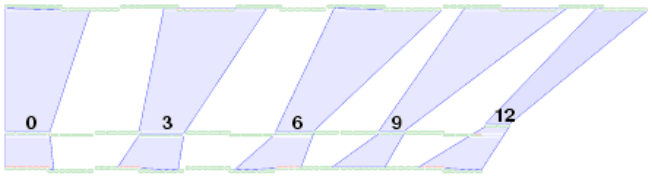

Figure 3: schematic view of the trigger roads projection for some trigger towers. The middle horizontal line represents the pivot plane, for one half barrel, equipped with six RPC detectors. The numbering represents the coincidence windows, two per each RPC.

II. Trigger System Electronics

The barrel level-1 muon trigger system is divided in an on-detector and an off-detector part. The RPC detector front-end electronics resides in the detector itself, and is connected to the on-detector trigger electronics via flat cables. Each RPC has got two sets of 8-channels connectors, one per each strip layer, on both the bending eta and the non-bending phi sides. The on-detector electronics is made of splitter boxes and trigger processors boxes (also called PAD). Because of overlapping coincidence windows in the confirm RPC detector planes, signals coming from the inner and outer RPCs need to be sent to more than one trigger processor box. A splitter box, mounted near each PAD box, is used to split detector signals and to fan-out them to more than one trigger processor box. One PAD box is mounted on top of each half-RPC station (each half-RPC belongs to a distinct trigger sector). A trigger tower is composed by one low-p_T PAD box mounted on top of one middle RPC station, reading-out the inner and the pivot RPC chambers, and one high-p_T PAD box mounted on top of the outer station, reading-out the low-p_T trigger result and the outer RPC chamber signals.

Each PAD box hosts four Coincidence Matrix ASICs, two per each view. One CMA contains both trigger and RPC readout logic, it processes signals coming from up to four detector layers, tags hit information to time bins of 3.125 ns (1/8 of a bunch crossing period), and tags events to the corresponding bunch crossing number. The ASIC has got a pipeline based architecture working at a clock speed of 320 MHz. The CMA trigger algorithm looks for hit coincidences within up to four different RPC detector layers inside the programmed geometrical road. A 1/4, 2/4, 3/4 or 4/4 majority logic can be applied. The trigger logic is replicated three times inside one CMA, so that three different threshold cut can be simultaneously applied. Trigger and readout results coming out from the CMAs are collected together in the local PAD logic (which resides into a FPGA chip), which assembles event data and calculates the RoIs. Low-p_T trigger and readout results are sent via flat cables to the high-p_T trigger box, which applies the high-p_T algorithm and sends results to the off-detector electronics via an optical fibre.

Six or seven optical fibres coming from one trigger sector go to one VME Sector-Logic/RX module, which elaborates the collected trigger and readout data, and sends readout and trigger data respectively to the ROD and to the MUCTPI. A schematic view of the full trigger slice is shown in Figure 4.

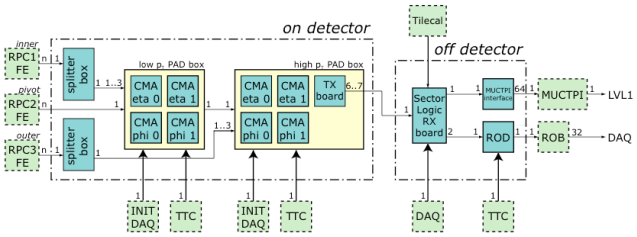

Figure 4: level-1 muon trigger slice, schematic view. The trigger algorithm is performed separately on eta and phi views, and then collected together in the PAD logic. Low-p_T results is elaborated with the high-p_T data in the high-p_T trigger processor, and then sent to the off-detector electronics.

III. Trigger Electronics Configuration

The on-detector electronics can be remotely initialised and controlled via a CANbus based system. Each PAD box hosts one CAN node to be used for receiving configuration commands and DCS commands (on detector board temperature sensors check, voltage control, etc.). Eight rack-mounted linux-based PCs, located in USA-15, run the initialization and DCS software. Each PC has got two PCI CAN interface cards each one with four CAN channels, each channel controlling one trigger sector. The total number of CAN nodes is 804 (one per each PAD).

One trigger processor box has got around 700 configuration parameters that are written/read during initialisation/control phases. The initialisation procedure can be performed either using one CAN write command per each parameter, operating with the user desired values from the PCs, or using a unique CAN command for the fast initialisation procedure, that uses an on-detector board locally-stored set of parameters. In fact the ELMB flash memory can store different sets of configuration parameters to be directly uploaded to the configurable PAD chips. The CAN fast initialisation command accesses the memory address storing the desired set of parameters, and start the local fast configuration procedure.

Table 1 shows the list of the configurable chips inside the trigger processor box. Since the Coincidence Matrix ASIC performs the trigger and readout algorithm, it store a large number of parameters, the most important being: input hit signal timing adjustment, trigger threshold settings, trigger

majority levels, trigger timing, trigger and readout channel masking, readout window settings, trigger and readout input and output dead-time settings, bunch-crossing and level-1 counters presets, etc. The PAD FPGA performs the PAD logic, and its main configuration parameters are: RoI settings, trigger and readout mode settings, test-pulse settings, bunch crossing and level-1 counters presets, testing settings, etc. The other chips that need to be initialised on the PAD boxes are: PRODE (delay/phase adjustment settings for the TTC signals), TTCrx (main control register need to be initialised) and the Optical Link (only on the high-p_T PAD). Finally, the PAD and ELMB flash memories contain respectively the PAD firmware for the PAD logic and the ELMB firmware with the initialisation settings, and they can be both read/written via the CAN bus.

The off-detector Sector-Logic/RX board's configuration parameters (main controls, time adjustments, etc.) are initialised via the VME interface.

Table 1: on-detector trigger processor configuration parameters list.

chip name	*# of chips per PAD*	*# configuration parameter per chip*	*parameters function*
CMA	4	159	configuration registers
PAD FPGA	1	19	configuration registers
PRODE	4	4	channels delay settings
TTCrx	1	5	configuration registers
Optical link	1	1	configuration register
ELMB flash	1	local memory	ELMB firmware configuration files
PAD flash	1	local memory	PAD firmware

The barrel level-1 configuration system stores all the configuration parameters on a central configuration database, used as the reference point for all the online and offline software applications controlling and monitoring the hardware. The TDAQ software runs and controls data taking, and is in due for the hardware configuration (i.e. it handles the PC CAN interfaces and commands). The offline calibration software runs the calibration algorithm based on the detector data coming from the TDAQ and on the configuration used during data acquisition. The simulation and reconstruction software uses the acquired data and the configuration data for its calculations. The TDAQ software, the calibration software, and the simulation and reconstruction software are interfaced with the database using a CORAL C++ based program, which extracts the configuration parameters from the database and passes them in the proper format to the software tools. From the configuration side, a Java based software will interface the database with the configuration procedure, generating a new set of parameters in the database each time a new configuration is created. It also interfaces the database with the program used to create the configuration file to be downloaded in the PADs. The configuration scheme is shown in Figure 5.

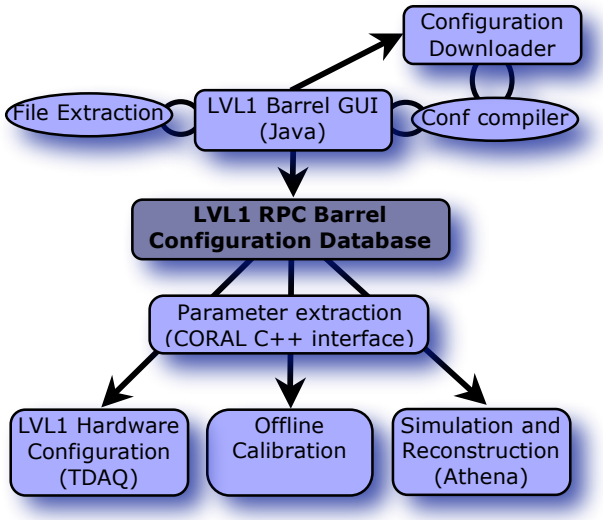

Figure 5: The level-1 barrel muon configuration system.

IV. Electronics Calibration

The barrel level-1 muon trigger calibration procedure is fundamental to assure good trigger efficiency, correct particle track reconstruction and bunch crossing identification. The calibration procedure can be logically separated in the trigger and in the readout part.

A. *Trigger calibration*

From the trigger point of view, the request from the calibration systems is to align in time the hit signals within each trigger tower, between adjacent trigger towers belonging to the same trigger sector, and between different trigger sectors. In order to perform the correct trigger calibration procedure, all trigger system structural characteristics have to be taken into account:

- the difference in length of the cables connecting the RPC detectors front-end electronics to the PAD trigger processors, which causes different timing for the hit signals belonging to the same PAD;
- the length of the cables carrying the low-p_T trigger output pattern signal from the low-p_T PAD to the high-p_T PAD, to be taken into account for the right time coincidence between the low-p_T result and the outer RPC signals;
- the trigger algorithm processing time, which causes a delay for the signals passing through the PADs;
- the time of flight for muons passing from the low-p_T RPC station to the high-p_T RPC station in a trigger tower, to be considered for the proper signal time alignment;
- the different length of optical fibres going from on-detector to off-detector electronics, causing time misalignment between different trigger sectors.

In order to cope with all these different factors, a lot of configuration parameters can be used both for the on-detector

and for the off-detector electronics. The on-detector trigger calibration parameters are the following:

- front-end signals input delay pipelines: signals can be delayed in groups of 16 RPC adjacent strips from 0 to 16 bunch crossing periods (400ns) in steps of 3ns, so that a time alignment can be possible within one trigger tower (within one RPC station and between inner low-p_T and outer high-p_T station);
- all the TTC signals (clock, trigger, resets) inside one PAD can be phase adjusted, in time steps of 1 ns, from 0 to 25 ns.

The off-detector trigger calibration parameters are:

- the sector logic input trigger signals can be shifted and aligned in steps of 1 bunch crossing period. This is used for timing alignment between different trigger towers (same or different trigger sector);
- all 8 inputs to the Sector Logic are aligned in phase with the 40 MHz clock (done on the PAD).

B. *Readout Calibration*

A very similar approach can be used for the calibration readout point of view. The requests for the readout calibration are: a proper trigger calibration, the event of interest selection with respect to the trigger input signal, the bunch crossing identification, event tagging with the correct event and bunch crossing numbers for all trigger towers. To achieve these requests the following it has to be taken into account:

- the level-1 signal latency;
- the length of the cables connecting the low-p_T PAD readout output pattern to high-p_T PAD readout inputs;
- the difference in length for the optical fibres going from on-detector to off-detector;
- the readout algorithm processing time.

The readout calibration on-detector parameters are:

- the readout window position: it can be shifted in time from 0 to 256 bunch crossing periods in steps of 25 ns with respect to the level-1 signal;
- the readout window width: it can be adjusted from 1 BC to 8 BCs;
- the bunch crossing and event counters presets: these internal counters can be preset to the desired value to be loaded when a TTC reset signal arrives;
- TTC signals delay: each TTC signal can be adjusted in time and shifted from 0 to 25 ns in steps of 1 ns.

There are no readout calibration off-detector parameters, since the signals going to the Sector Logic are already aligned in time with the 40 Mhz clock phase.

C. *Calibration Studies*

Studies on the level-1 muon trigger calibration system have been carried out on the following CERN sites:

- muon test-beam (two trigger towers);
- BB5 cosmic ray RPC test stand (one trigger tower);
- ATLAS SX1 surface RPC test pulse system (one RPC station);
- ATLAS sector 13 during the commissioning phase (three trigger towers, two trigger sectors).

These studies have been fundamental to develop the final calibration procedure. The calibration procedure has been developed using a bottom-up approach, following the trigger structure, as shown in Figure 6.

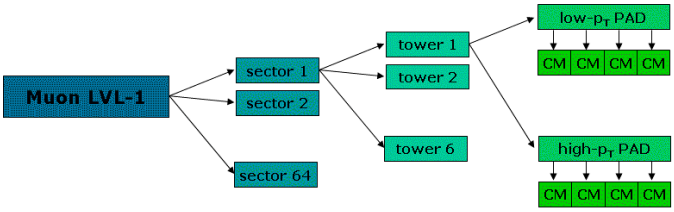

Figure 6: bottom-up level-1 calibration approach scheme.

D. *Calibration Algorithm*

The calibration algorithm first uses data acquired with a known set of parameters values (for example the default one). Timing info is then extracted from the acquired data, calculating the average time distribution for groups of sixteen channels. This calculation gives the information of the time shift between different groups of front-end channels, so that the delay to be applied can be identified. Alignment between CMs is done using the pivot plane as reference distribution, and aligning the others to this reference. The set of delay parameters can so be applied in all the CMAs of one low-p_T PAD, and then on the corresponding high-p_T one, so that the alignment between low and high-p_T PADs can be performed. After the single trigger tower calibration is achieved, the tower-to-tower alignment is calculated, and then the sector-to-sector. Alignment is performed on each view (eta and phi) in steps of 1 bunch crossing period.

Finally a new set of calibration parameters is produced, to be used for system configuration and to be stored in the configuration database. Figure 7 shows the schematic view of the calibration algorithm.

More then 25 thousands of calibration constants are to be calculated and used online, using different calibration parameter sets depending on the physics (cosmics or collisions).

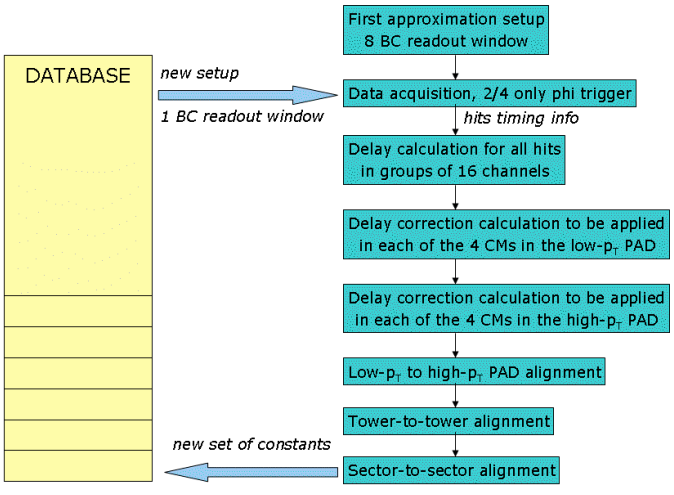

Figure 7: schema of the calibration procedure.

E. Calibration Example

Figure 8 shows the time distribution for cosmics for a group of sixteen channels in one non-pivot plane, before the calibration. Using the latest pivot 16-channels group time as the reference, the time difference between the non-pivot and the pivot group is shown in Figure 9. Repeating this calculation for all groups of channels, we can calculate the delays to be applied to align in time all the groups. Figure 10 shows the misalignment after calibration.

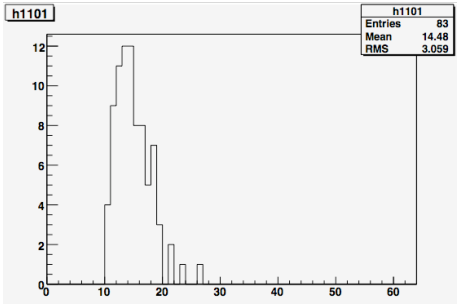

Figure 8: row cosmics time distribution before calibration, time unit in x-axis is 3.125 ns.

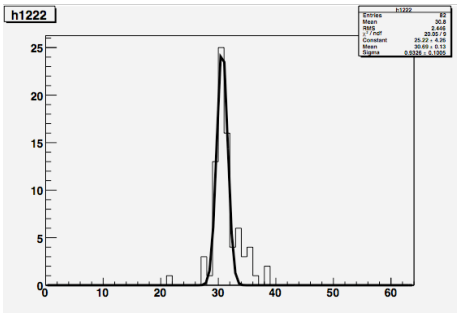

Figure 9: time difference peak finder, time unit in x-axis is 3.125 ns.

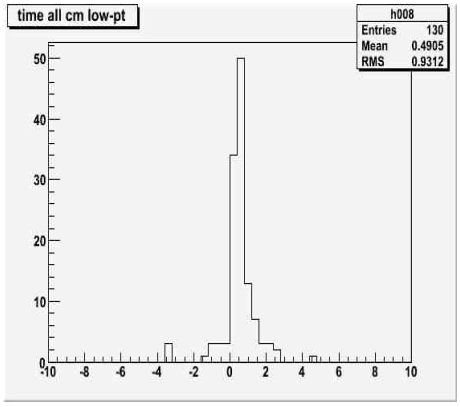

Figure 10: sixteen-channels timing group misalignment after calibration, time unit in x-axis is 3.125 ns.

V. Conclusions

Calibration procedure has been developed so far for in-plane and plane-to-plane alignment, tower-to-tower and sector-to-sector calibration being just started. The ATLAS sector 13 commissioning work allows for extensive studies on detector using standalone RPC or combined RPC-MDT tracking, for studies on chamber efficiency using combined tracking, for the checking of cabling work, for the comparison of the online-offline mapping, and for the studies of eta-phi matching. The level-1 RPC barrel configuration database is being developed (database structure built, now working on the interface with the configuration system and on the GUI). Finally the configuration strategy in case of Single Event Upsets for non-redundant registers (do not affect system functionality) is to be defined.

VI. References

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ATLAS TDAQ RoI Builder and the Level 2 Supervisor system

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Abstract

The ATLAS High Level Trigger (HLT) uses information from the hardware based Level 1 Trigger system to guide the retrieval of information from the readout system. The Level 1 Trigger elements (jet, electromagnetic, muon candidate, etc.) determine Regions of Interest (RoIs) that seed further trigger decisions. This paper describes the device - the RoI Builder (RoIB) - that collects these data from the Level 1 Trigger and the Level 2 Supervisors (L2SV) Farm that makes these data available to the HLT. The status of the system design and the results of the tests and integration into ATLAS TDAQ system are presented.

I. Region of Interest concept and RoIB/L2SV system prototyping

The Level 1 Trigger system (LVL1) identifies a number of RoIs for the HLT - spatially limited areas ('roads') in the detector with candidates for phenomena to be triggered. The information from Level 1 includes the selected trigger type and the details of where in η and φ the trigger objects (e/γ, μ, etc.) that caused the event to be accepted originated. Using this information as guidance, specialized algorithms request a sub-set of the event data from the ROSs to perform the event selection. In this way only a few per cent of the event data need to be transferred initially to the HLT system — thus considerably reducing the network bandwidth required.

The initial ideas and requirements are summarized in [1, 2]. The RoIB and L2SV system have been prototyped a number of times, have undergone a series of design reviews and tests, and have been integrated with individual parts of the Level 1 Trigger system and the HLT.

The Region of Interest Builder (RoIB), located in the underground counting room, takes raw event fragments from various Level 1 Trigger sources, assembles all the fragments of a given event into an RoI record, selects a target Level 2 Supervisor (L2SV) processor in a farm, and then sends the RoI record to this processor. From there the RoI records are distributed to the High Level Trigger (HLT) processors that require them for further event selection and disposition.

The Level 2 Supervisor farm, located in the surface TDAQ computing farm barracks, is comprised of commercial rack mounted PCs. They are connected to the RoIB via ATLAS standard S-LINKs and to the High Level Trigger via Ethernet. Each Level 2 Supervisor processor is thus subjected to a fractiono f the Level 1 accept rate avoiding issues of hight input and output bandwidth.

The overview of the RoIB/L2SV system is shown in Fig.1. The baseline implementation of the RoIB is a VMEbus system which includes a Single Board Computer (SBC) for configuration, control and monitoring. It is composed of two stages: input and assembly. The input stage consists of Input Cards that receive and buffer the RoI fragments. These cards subsequently send the RoI fragments to Builder Cards in the assembly stage where the RoI fragments are assembled into RoI records. Each Builder Card can service up to four supervisor processors. The number of builder cards within the system is not limited and is dictated by the rate that a supervisor processor can sustain.

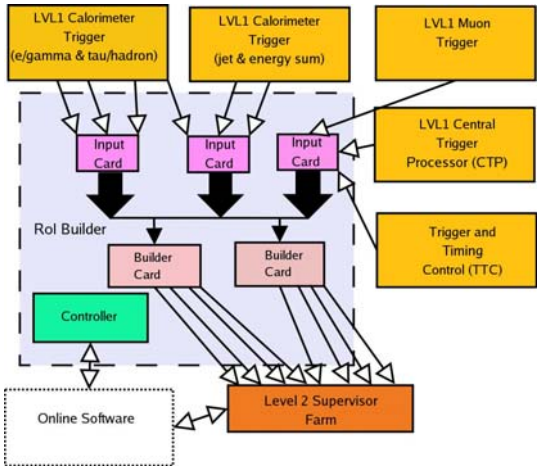

Figure 1: RoIB/L2SV system overview

A prototype of the RoIB was built and tested during the course of 1999. It was based on a pair of 12U VMEbus cards, an Input Card capable of handling six S-LINK inputs, and a pair of Builder Cards able to output to a pair of supervisor processes. This implementation utilized 76 Altera 10K40 FPGAs and 8 10K50 FPGAs. The system and early performance measurements are documented in [3].

Testing has shown that combining RoI fragments from several sources using an FPGAbased device is feasible and that a L2SV consisting of four 300 MHz Pentium II PCs is sufficient to receive the RoIB output rate of 100 kHz. Subsequent tests with prototypes of the muon Central Trigger Processor Interface and the Central Trigger Processor ROD modules of the LVL1 system have made a start on debugging the component interfaces and have further demonstrated that data input to RoIB could be achieved at the required rates [4].

II. RoIB/L2SV System Design

The final implementation of the RoIB cards will be on 9U VMEbus cards. Each of 4 Input Cards accommodates 3 S-LINK input LDC's (Link Destination Card), and can service up to 4 Builder Cards (limited by the custom backplane in the VME crate). Each Builder Card can service up to four supervisor processors sending data via S-LINK output LSC's (Link Source Card), The Single Board Computer (SBC) in the RoIB crate provides the configuration and monitoring information to the Input and Builder Cards.

A. RoIB Input Card

A simplified block diagram of the Input Card is shown in Fig. 2. All transfer of information from the Input Cards to the Builder cards is via J3 high density 250 pin connector and a custom backplane mounted in the rear of the crate.

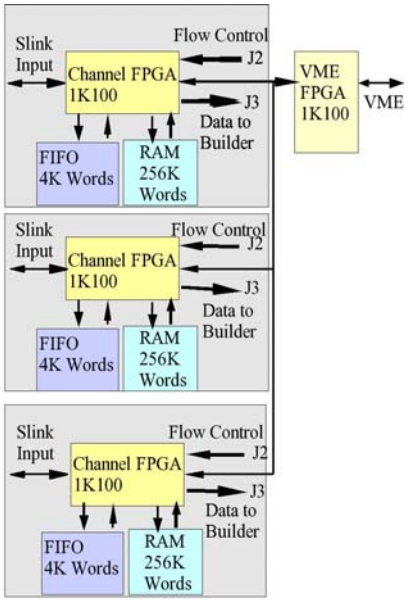

Figure 2: Simplified block diagram of the Input Card

Each Input card also has a diagnostic RAM initialized from VMEbus which allows emulating LVL1 fragments, and enables the operator to verify proper functioning of the RoIB system in a stand alone mode. The Input Cards have several modes of operation:

- Diagnostic Run Mode – the input data streams are provided by the diagnostic RAM's and the contents may be diagnostic data, test vectors from Monte Carlo or simulation results.
- Sniffer Mode – the RAM is written with Fragments from the incoming data stream from LVL1. The contents of the diagnostic RAM can then be accessed in block transfers from VMEbus.
- No Sniffer Data Mode – LVL1 data from an Input Card are transferred through the custom backplane to the Builder Cards with the 3 channels functioning independently of each other.

Each channel has an FPGA to provide the logic required for managing the data. Depending on the Mode that is defined by the status register, there are several paths that data may take. In Sniffer Mode and No Sniffer Data Mode the path of data is from S-LINK through the FPGA into the FIFO. In Sniffer Data Mode the S-LINK words are written to the Diagnostic RAM as they are read from FIFO. In No Sniffer Data Mode, if there are data in the FIFO and there is no Flow Control from the Builder Cards for this channel, data are read from the FIFO one word at a time, parsed and formatted into 20 bit words, and transferred to the Builder Cards. In Diagnostic Run Mode the path of data is from RAM, through the FPGA, into FIFO, from FIFO, through the FPGA, and after being parsed, through J3 to the Builder Cards.

The flow control signals are transferred via User Defined pins on J2. Since each Builder Card deals with input from 12 S-Link channels, it must provide 12 flow control signals. These 12 signal lines are bussed on J2 and are wire-or'ed. The first three of the flow control signals go to the first Input Card, the second three go to the second Input Card, etc.

There is an FPGA to handle the transactions with VME, which include 32 bit non-privileged transfers for reading/writing registers and 64 bit block transfers for reading/writing the diagnostic RAM(S). The VME FPGA also includes a number of registers, such as status, which are relevant to all three channels. A photo of the Input Card is shown below:



Figure 3: RoIB Input Card

B. RoIB Builder Card

Each data fragment contains RoI data collected from a portion of the Level 1 trigger system. The Level 1 information required for the HLT system is the concatenation of all such fragments for an event. This includes both the information about the trigger decision as well as eta and phi data for the subsystems that cause an event trigger. We refer to the collected RoI fragments for a given event as an RoI record, and to the subsystem on the Builder Card that builds the RoI record, as the Assembly Unit (AU, see Fig. 4).

The Input Cards pass RoI fragments to a set of Builder Cards. Each Builder Card communicates RoI records to four

Supervisor processors. The compiled RoI record is transferred to the target Supervisor processors using S-Link. Each of the Builder Cards is responsible for a subset of the events that trigger Level 1.

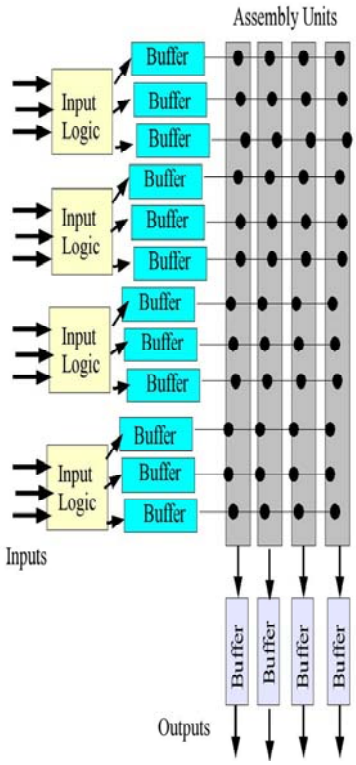

Figure 4: Simplified block diagram of the Builder Card

The RoIB uses basic round robin algorithm to assign Supervisor Processors. The system is expandable in units of four Supervisor processors by adding another Builder Card. The backplane is able to accommodate eight RoIB cards. Each Builder Card has registers which tell it which of the Level 1 channels are active, how many Builder Cards there are, which card it is in the sequence of cards, etc.

Events are allocated to Supervisor processors on a round robin basis, with the hardware automatically adjusting for the number of cards, number of Supervisor processors, etc. The firmware also allows the allocation of events to specific AU's based on criteria other that the Event ID, for example the Event Type.

Flow Control exists at a number of points on the RoIB, and is not treated as one continuous signal. For example, there is a Flow Control between the input FIFO in the Builder Card and the Input Card, Another example of Flow Control on the Builder Card is when the output FIFO goes half full it exerts Flow Control back to the builder logic.

The individual ROI fragments can be as long as 128 S-LINK words including headers and trailers, and are in the S-Link format. It is necessary to accommodate the time skew of arriving fragments, and accordingly a timer is started at the arrival of the first fragment of each event. If all the fragments have been received before the timeout, the compiled record is transferred to the target Supervisor process. If the timeout occurs the system transfers an incomplete record to the target Supervisor process. If a tardy fragment from a previous incompletely built record is received it is discarded.

The timeout and other parameters of the Builder Card are selectable from VMEbus as on the Input Card. The photo of the Builder Card is shown below:

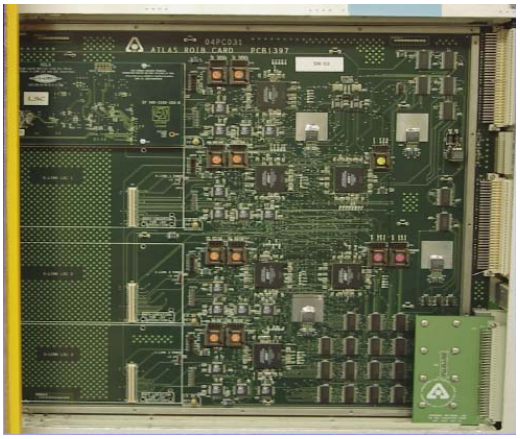

Figure 5: RoIB Builder Card

C. Custom Backplane

Signals are carried from the Input Cards to the Builder Cards via a custom backplane at 3.3 volt logic levels with special care taken to avoid crosstalk. The problem of driving data and clock lines was dealt with by reducing the clock frequency for the input cards to 20 MHz, by paralleling the drivers, and by limiting the number of Builder Cards to 4.

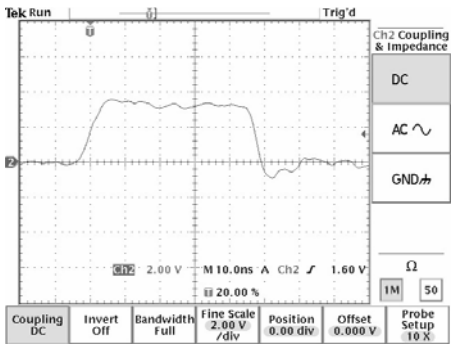

Figure 6: Data bit on the backplane showing rise and fall time

In order to check possible transmission errors, the firmware generates a checksum in the Input Cards on each fragment, transfer it to the Builder Card after each trailer, and compare it with a checksum being generated as the fragment is received. In the event of disagreement the Level1 Event Number is written to a FIFO on the Builder Card. The photo of the custom backplane is shown on Fig. 7.



Figure 7: View of the fully populated RoIB crate

D. SBC and standalone tests

A VME processor VP110/010 from Concurrent Technologies is used as a Controller in the RoIB crate to access the VME registers available for programming and controlling the two types of cards.

It allows two levels of testing of the RoIB – basic single card initial checkout and multi-card integrated checkout (Fig. 8). Single card test for the Input Card includes single S-Link to sniffer RAM test and write/read RAM test, For the Builder Card there are spy FIFO and single S-Link output tests.

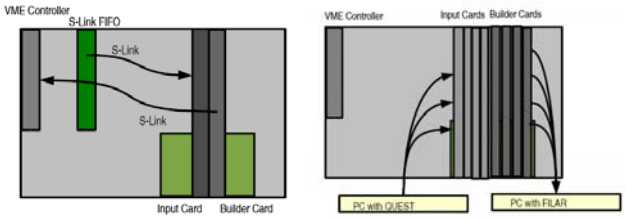

Figure 8: Basic and multi-card test setups

The RoIB test programs for the multi-card integrated checkout use external PCs for data sources/sinks and define 3 levels of complexity - spy FIFO (requires no external sources/sinks), check readout (requires external sink) and check readout with external data source and external sink, sample monitoring data.

The following conclusion about performance of the RoI Builder system was made based on the results of the standalone tests:

- throughput depends weakly on number of inputs due to parallel nature of system,
- throughput depends mainly on length of longest fragment,
- throughput of integrated system (external sources and sinks) was limited by readout rate,
- near 100 kHz is achieved for 3 inputs, 4 outputs.

E. L2SV Farm

The Level 2 Supervisor farm (up to 16 commercial rack mounted PCs) is connected to the RoIB via ATLAS standard SLINKs and to the High Level Trigger – via Ethernet. Each PC is equipped with FILAR card - quad S-LINK LDCs to PCI Interface. Each processor in the farm is responsible for distributing RoI records to the HLT processors farm and effectively managing the processing resources of the HLT farm via a load balancing algorithm. It receives the final decision on an event based on the result of the HLT processor. The decision results are communicated to the Data Flow Manager (DFM) so that accepted events can be further analyzed and rejected events can be flushed from the Readout System.

III. RoIB/L2SV Tests and Commissioning

The RoIB and L2SV system has undergone a number of prototypes, a series of design reviews and several tests, and integration with individual parts of the Level 1 Trigger system and the HLT.

A. H8 Test Beam

Initial test of a small RoIB system was in H8 test beam, it was integrated with Level 1 Trigger outputs from muon and calorimeter triggers. Control software was fully integrated with DAQ system..

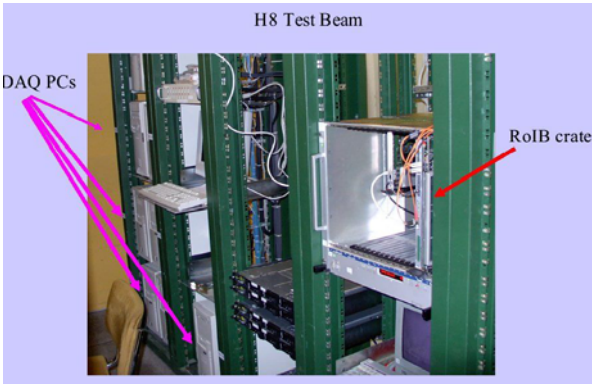

Figure 9: H8 test beam setup

B. RoIB in USA15

The commissioning stage has started with incremental installation of individual RoIB components and connection of the Level 1 Trigger system to a fully populated RoIB crate (see Fig.10).

The RoIB installed recently in the USA15 underground counting room contains 4 Input Cards and 3 Builder cards, however only 3 LVL1 Trigger inputs are connected at present and only 2 L2SV processors are used in the SDX1 counting room. The size of the L2SV farm will be augmented when dictated by increasing event rates during commissioning.



Figure 10: Final setup in USA15

C. TTC LDC

A mezzanine card for bringing TTC information into the RoIB system was developed. This card appears to an Input Card to be an S-Link LDC, but instead receives input from the TTC fibre into a TTCrx. The TTC information is latched on every L1 Accept, is formatted on the mezzanine card to resemble an RoI fragment, and is accepted and processed by the RoIB as if it were an RoI fragment. The data which are latched on a L1 Accept are the 24 bits of the Event Counter, 12 bits of the Bunch Counter, and 8 bits of Trigger Type. Once the data are latched, they are reformatted in the form of an RoI fragment, and written to a FIFO. If there is no flow control imposed, the pseudo fragment is next transferred to the Input Card through the S-Link port. An 8 bit register internally in the FPGA is incremented on Event Resets to provide the top 8 bits of the L1 Event Number.

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Setup, Tests and Results for the ATLAS TileCal Read Out Driver Production

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Abstract

In this paper we describe the performance and test results of the production of the 38 ATLAS TileCal Read Out Drivers (RODs). We first describe the basic hardware specifications and firmware functionality of the modules, the test-bench setup used for production and the test procedure to qualify the boards. We then finally show and discuss the performance results.

I. INTRODUCTION

The back-end hardware for the first level trigger and DAQ of the ATLAS Hadronic Tile Calorimeter (TileCal) consist of four ROD crates. Each ROD crate contains eight RODs and eight Transition Modules (TM) and reads out one out of four partitions in the calorimeter [1]. Therefore, 32 RODs and 32 TMs are needed in order to read out the whole calorimeter. Taking into account the spare units, we have produced and tested a total amount of 38 units of RODs and TMs.

A. The TileCal ROD module

Both the electromagnetic and hadronic calorimeters in ATLAS use a common ROD motherboard (Figure 1) adapted to the specifications required in each case [1]. For this reason, the motherboards were produced together.

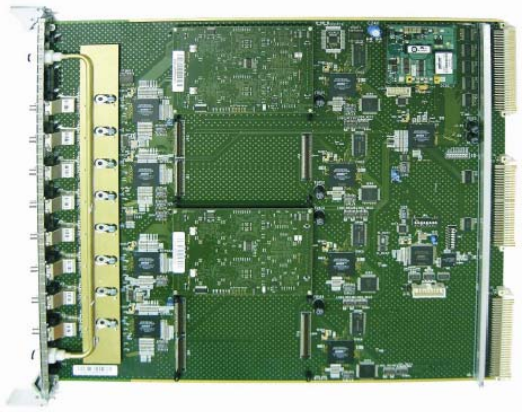

Figure 1: ROD motherboard with 2 Processing Units.

At industry level some general, mechanical checks, JTAG boundary scan and X-ray tests were done for all the RODs. Besides, at the University of Geneva (UniGe) some static tests were done to all the RODs by the Liquid Argon (LAr) group in order to verify the correct functionality of all the components in the board. In addition, several dynamic tests to check the dataflow across the ROD were also done at UniGe [2].

Once the RODs were delivered to the TileCal group, the first task was to adapt the boards to the TileCal requirements before their validation tests. This adaptation consists of some hardware modifications and firmware changes [1]. The hardware modifications customize the ROD to receive the data at the working frequency of the Front End (FE) Interface Cards. Furthermore, the number of Processing Units (PUs) per ROD has to be adapted also, due to the fact that TileCal will use 2 PUs per ROD (called Staging mode), instead of 4 PU/ROD used in the electromagnetic calorimeter of ATLAS (full mode) [1].

Concerning the firmware, specific code for the TileCal ROD in the StagingFPGA, InputFPGA and DSPs is used [1]. As the InputFPGA and DSP code is downloaded at configuration time, only the StagingFPGA code has to be downloaded before the beginning of the tests. Besides, if some code is upgraded for specific or common firmware, it has to be checked and validated prior to be updated in all the boards.

Regarding the TMs, the difference between both calorimeters is the number of High-speed Optical Link for ATLAS (HOLA) mezzanine cards mounted on the boards. LAr ROD system implements four HOLAs per TM, whereas TileCal system uses two HOLAs per TM [1].

II. TEST-BENCH DESCRIPTION

The test-bench mounted in the lab at IFIC-Valencia for the TileCal RODs validation was divided into an injection part, a ROD crate and an acquisition system (Figure 2).

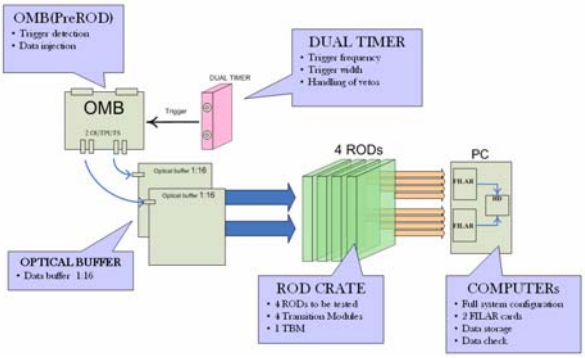

Figure 2: Test-bench diagram.

The FE was emulated by injecting data to the ROD with one Optical Multiplexer Board (OMB) 6U prototype, two Optical Buffers and a dual timer to control the rate of injection.

Up to four RODs in a crate could receive and process data simultaneously and a PC system equipped with 2 FILAR cards gathered, stored and checked all the data coming from the RODs.

Furthermore, one more computer was included in the setup as the main user interface computer responsible for the configuration tasks of all the devices in the test-bench chain.

B. Optical Multiplexer Board prototype

Preliminary studies done on the FE electronics showed that radiation shouldn't be a problem at the beginning of the experiment. Nevertheless, these studies also showed that radiation could cause malfunction, bit errors and durst in the data sent, in particular when the luminosity of the beam will be increased.

In order to avoid these radiation problems, each drawer in the FE will send data to RODs redundantly by two different optical fibers. The final OMB should check the CRC and decide in real time which data is correct and send it to the ROD.

The OMB integrated into the RODs production test-bench was a 6U VME prototype version of the final 9U VME OMB (Figure 3). It has four optical inputs and two optical outputs. Two CRC_FPGAs are mounted and connected, each of them, with two inputs and one output, and they are responsible of CRC check and injection tasks. In addition, a VME_FPGA provides communication between the VME bus and the CRC_FPGAs. The interface with VME is used for configuration tasks and readout CRC error counters [3].

Apart of the CRC check in real time, the OMB was designed to emulate the FE in order to have the possibility to perform ROD calibration and tests while the detector is not working. For these purposes, the OMB can inject events to the ROD in two different modes. These two options were used during the production of the RODs. In the first one, the events have all the words equal, but events are always different between them. In the second mode, the OMB was capable of sending a user defined event, downloaded in advance, even with real data, and it sent the event to the ROD with every trigger signal. Both, the configuration of the injection mode and the event download are done by the VME bus.

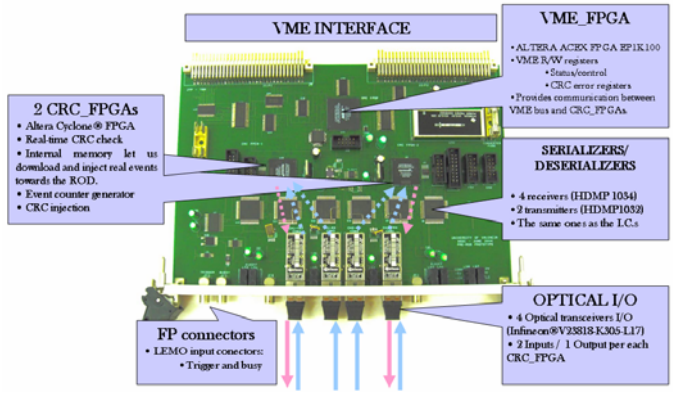

Figure 3: Optical Multiplexer Board 6U prototype.

The counter mode was used in long term runs in order to inject a high quantity of different events at high rate, while memory events, which have to be downloaded before its injection, can not be used at high rate if different events are needed. Nevertheless, this memory mode was used in order to validate the DSP reconstruction code, due to the possibility of inject events with real data.

As part of the raw data format every event sent by the OMB includes in the last word (apart of control words) the CRC calculation of the whole event. This CRC word can be checked after the acquisition chain in order to prove the correct dataflow across the system.

Apart of the injection modes, the trigger has also two modes: external and internal. In the external mode, the trigger signal has to be provided and generated in a dual timer, where the rate of injection and the width of the pulse are configured. On the other hand, if internal mode is selected, the rate of the trigger is configured in the OMB.

C. Optical Buffer 1:16

The Optical Buffer (OB) is a 9U VME board specifically designed for ROD production (Figure 4). As the OMB 6U prototype offers only two optical outputs and the ROD has 8 inputs, the OB was designed in order to increase the number of links injecting data to the RODs. The OB receives one optical input, converts the signal into LVPECL, and repeats it to 16 optical outputs with clock drivers.

With only one OMB 6U prototype and 2 OBs we had 32 links, which is enough to inject data to 4 RODs at the same time. It represents a half partition of the TileCal detector.



Figure 4: Optical Buffer 1:16.

In counter mode, the OMB was programmed to inject different events through each output. The two outputs were repeated with two OBs. Note that to inject only two kinds of events to the RODis not a problem as each DSP process the data coming from two inputs and each DSP works uncorrelated from others.

D. ROD and injection crates

Two crates were used during the ROD production. The first one was utilized as an injection crate, while the second one as a ROD crate. The crates used in the ROD productions tasks were WIENER VME -64x Series 6000 LHC and the Single Board Computer selected as the VME ATLAS ROD Crate Controller (RCC) was the VP 110/01X from Concurrent Technologies. With these crates and RCCs we had VME access to every board inserted in the crates.

The injection crate was composed by a TTCvi for trigger configuration, an OMB 6U as data generator and the OB as a

data repeater. In this case, the RCC was used for the configuration of the TTCvi and the OMB. In addition, a TTCex and a ROD Busy Module were used in order to test the RODs with the whole TileCal data acquisition system

The ROD crate contained the RODs to be tested, the TMs and the Trigger and Busy Module (TBM) to collect the busy signal from all the RODs in the crate and to make the veto to the trigger.

E. Computers and software

Three computers were used during the production for configuration tasks, acquisition and for data checking. The software utilized in the configuration of the tests was the ATLAS Trigger and Data Acquisition official software (TDAQ) adapted to our production tasks [4].

One of the computers was used to run the main partition of the TDAQ software. The TDAQ presents a graphical user interface and it was utilized for the configuration of the tests (Figure 5). A set of user defined applications for the TDAQ handled the CRC error checking during the dynamic tests. The results were displayed in another DAQ panel were the number of errors detected during a run was shown. Other information like number of run, integrated time, number of events processed, etc., was shown in the same display. Besides, when a run was finished another user defined panel stored all this information in the ROD production database (see section J).

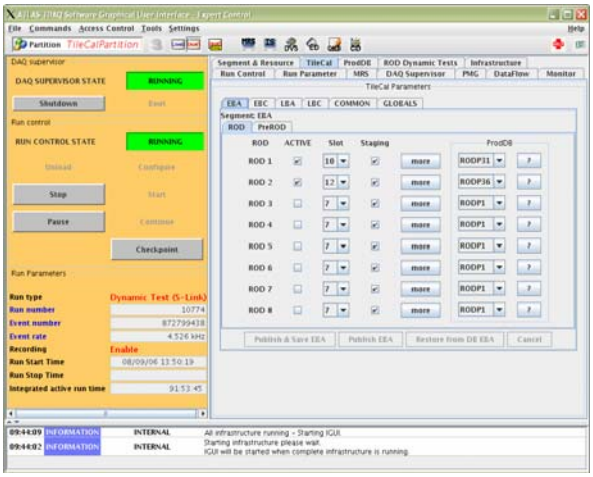

Figure 5: TDAQ software graphic user interface.

Two more computers were used for data acquisition and data checking coming from the ROD system. The first one was a dual CPU with 2 Four Input Links for Atlas Readout (FILAR) cards installed. These 2 FILAR cards read out up to 4 RODs, and store the data in a shared file system. The second computer, with access to this shared file system, checked the data online.

III. PRODUCTION TESTS

The ROD validation was divided into two different phases. In the first one, all the ATLAS calorimeters common RODs have been tested. These tests were made at the industry level and at the University of Geneva. Afterwards, the RODs were adapted to TileCal requirements and finally validated with this configuration.

F. Tests to ATLAS calorimeters common RODs

The ATLAS calorimeters common ROD motherboards were made in TechCI (France), and the components assembly in Seisystem (Italy). The RODs were delivered from industry with some general tests and mechanical checks. With the PUs already installed in the ROD motherboard, some JTAG boundary scan tests were made to the system. Nevertheless, the PUs were checked with X-ray tests previously to its insertion in the ROD motherboard. If all these tests were passed, the RODs were delivered to the UniGe, responsible of the validation of ATLAS calorimeters common RODs [2]. The UniGe group developed several functionality tests in order to check the correct dataflow across the boards. For this purpose, some static tests were made to prove the correct operation of programmable devices. Then, some data path tests proved the correct communication between the StagingFPGA and the OC. Finally, dynamic tests with the ROD Injector as data generator, and the TMs for sending the data out, validated the whole ROD system. These dynamic tests were made at different frequencies of injection and operating in full and staging mode.

G. TileCal adaptation

Once the ATLAS calorimeters common RODs were validated at the UniGe, they were delivered to the TileCal group. Then, the first task was to adapt them to TileCal specifications, including hardware and firmware modifications in the boards [1]. The hardware modifications were made at the electronic laboratory at IFIC-Valencia and they include some changes of clocks and passive components in order to adapt the G-Link frequency of data reception. The number of PUs utilized in TileCal RODs was also adapted as only 2 PUs per ROD are used in TileCal (Staging mode), instead of the 4 used in the Liquid Argon (LAr) subdetector (Full mode) [1].

Once the hardware modifications were done and with the boards already in the ROD crate, the firmware adaptation was realized. The specific firmware for TileCal was downloaded in the StagingFPGA, InputFPGA and in the DSP. Besides, the common firmware was updated as upgrades were available.

H. Validation tests of TileCal RODs

The ROD validation protocol consisted of a four level test chain. Each ROD had to pass all the test levels in order to be validated. The first level, called level 0, was basically a static test composed of three Diagnostic and Verification System (DVS) tests. These DVS tests basically certified the correct access through VME to every register inside all the programmable devices on the ROD motherboard. Besides, the correct communication between the StagingFPGA and the OC was checked sending several events from the internal memory of the StagingFPGA and reading them out with the OC. In order to consider the level 0 approved, each ROD had to pass at least three DVS tests.

Once a ROD has passed the level 0 tests, 3 levels of dynamic tests level 1, 2 and 3 are applied to the module. In these tests the OMB 6U board emulated the FE injecting data to the RODs. The data processed by RODs was stored and checked in the computers. The maximum trigger rate reached

by the online check task was approximately 400 Hz. For higher rates, the software couldn't check all the events in online mode, and only a percentage of the processed events were checked.

Level 1 test was a single ROD dynamic test at low rate. The trigger rate was 200 Hz and all the events passing across the ROD were checked. After more than 4 hours processing data without errors, the level 1 became approved. At that rate, no busy signals appear in the ROD system.

Level 2 test was also a single ROD dynamic test, but increasing the injection rate and number of hours of the run. In that case, the rate of the trigger was 1 KHz and only a 40% of processed events were checked. Besides, some busy signals appeared caused by the storage of data coming from RODs. Thus, the correct busy handling was also checked in that test. The ROD had to process data without errors at least during one hour in order to pass the level 1 test.

Finally, the level 3 test was a multiple ROD burning test at high rate. In this case, four RODs were tested together during at least 72 hours. The trigger rate was selected to be 1 KHz, and only 10% of the processed events were checked.

If no errors were found during the 4 level tests, the ROD became validated and ready to be installed in the ATLAS electronics cavern (USA15) at CERN.

Table 1: Four level tests protocol.

LEVEL	RODs	RATE	MINIMUM TIME
0	1	Three DVS tests	
1	1	200 Hz	4 h.
2	1	1 KHz	8 h.
3	4	1 KHz	72 h.

I. Data checking algorithms

The data processed by the RODs was checked online by two monitoring task algorithms. If the counter mode was selected in the OMB inside an event, all the words were equal and their value one unit higher than in the previous event. Through this check the ROD processing, it was verified the correct functioning of the ROD system.

In addition, as the OMB sent the CRC of each event attached as last word, it could be checked after the acquisition chain. The type of CRC utilized for data checking in ROD production was CRC-CCITT16. This type of CRC is also used in the TileCal experiment in order to check the correct data transmission between the FE and the RODs. The full configuration of the CRC utilized is showed in Table 2.

Table 2: Specifications of the CRC utilized in the RODs production.

Width	16 bit
Poly	1021 This is the divisor polynome
Init	FFFF This is the initial value of the register
Refin	CRC output is not reflected
Refout	CRC output checksum is reflected
Xorout	No XOR is performed to the CRC output
Check	ascii string "123456789" checksum is 29B1

J. Production database

After their adaptation to TileCal requirements the RODs, PUs and TMs were labelled and introduced in a database. Each ROD motherboard had associated two PUs and one TM. The validation of a ROD implied the validation of the entire group, which is labelled with a final ROD (RODF) label. This label can be seen in the front panel of each validated ROD (Figure 6). RODs are installed in the pit according to the component association introduced in the database.

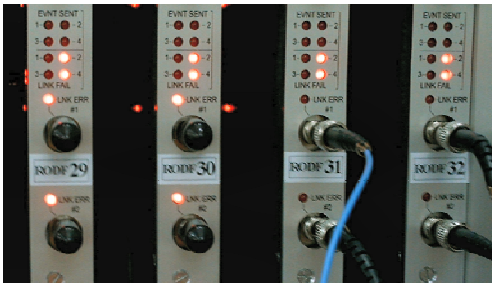

Figure 6: Final label in the ROD front panel.

The production database includes all the information about a ROD group. Besides, with the TDAQ software it was possible to save in the production database all the information related to each run. Thus, apart of the PUs and TM associated to each ROD and the firmware version of each programmable device inside a ROD, the production database includes all the tests done to every ROD.

Finally, the incidences found during the production were also introduced in the production database. Besides, the production database is totally accessible from a web page and as we have seen contains all the information about the ROD production.

IV. TESTS RESULTS

The number of ROD boards produced has been 38. For the read out of the experiment 32 boards are needed, and 6 units have been produced as spares. All the RODs produced have passed all the four level tests previously shown. It implies that each ROD has been processing data during at least 84 hours, has processed more than 264×10^6 events with at least 38×10^6 checked events without errors. Nevertheless, some extra runs were done during the production period in order to validate some firmware upgrades. All the runs were introduced in the production database and all they are counted as processing time by the RODs.

Table 3 summarizes the tests results in terms of time, events processed and events checked in the three different level tests during the RODs production.

Table 3: Summary of tests.

	Level 1	Level 2	Level 3	Extra runs
Time (h)	259	405	2001	560
Processed events	269×10^6	2040×10^6	8112×10^6	2708×10^6
Checked events	269×10^6	395×10^6	781×10^6	280×10^6

Nevertheless, during production tests some functioning problems were found in various RODs. Different kinds of problems were found, but all of them were detected and solved. In order to solve the problems found, one Optical Receiver in RODF24 and one DC/DC converter in RODF30 were replaced. Besides, the RODF25 had a scratch over a data bus and it was repaired. These repaired RODs were revalidated after their reparation.

Considering all the tests done during the production period, the ROD system has been processing data during 3225 hours. A total of $13129x10^6$ events were processed during this time, and $1,7x10^9$ events were checked without errors. The events injected by the OMB 6U and processed by the RODs during the production emulated an actual 9 samples event (176@32bits words). Thus, taking into account the number of bits processed by the ROD system, we obtain a bit error rate (BER) better than 10^{-13}.

Nevertheless, as shown before the number of events processed by the ROD system during the production was approximately $1,7x10^9$, which represents a run of 5 hours of the TileCal experiment at full expected rate (100 KHz).

K. Temperature tests

Apart from validating the correct functioning of each single ROD, we had to validate the cooling system selected for the TileCal ROD crates. As we have seen, RODs were designed in common for all ATLAS calorimeters, LAr and TileCal. In both cases, data are sent from the FE serialized and is deserialized in the ROD through the HDMP-1024 G-Link chip receiver. However due to the much higher channel density of the LAr detector the G-Link chips have to be clocked at 80 MHz in the LAr design, to increase the required bandwidth. This is beyond the nominal specifications of the chip. Nevertheless, the LAr group demonstrated the correct functioning of this device clocked at 80 MHz if the temperature was kept below 35 ºC. For that purpose, a water cooling system was included in the ROD. For the TileCal requirements, the G-Link is clocked at 40 MHz, well within the manufacturer specification, and it was decided not to use the water cooling system in TileCal and to use air cooling instead. In order to verify the correct functioning of the air cooling system some temperature studies were realized in the laboratory and in the pit. For these studies, the final composition of ROD modules per crate to be used at the pit was emulated, i.e., with 8 RODs and 8 OMB 9U boards in a ROD crate. As the OMB 9U are not so far available, we emulated this situation plugging 16 RODs in the same crate. Firstly we proved that the air cooling system worked better in the pit than in the lab. In addition, for the tests done in the pit the temperature of all the G-Links after more than 48 hours processing data was kept below 60 ºC, which is well within the chip specifications (85ºC). Apart of that, from these studies we concluded that the air cooling system doesn't work exactly in the same way in all the slots, and even for all the G-Links in a ROD (Figure 7). Regarding the slot, due to its position related to the fans, slot 18 was the worst cooled. Inside a ROD, the G-Links corresponding to the receiver 2 and 3 were the warmest.

With these results, the StagingFPGA firmware was modified in order to set the temperature threshold for the LED in the front panel of the ROD at 65ºC. At this temperature the ROD should work correctly but we considered that this temperature in any G-Link implies a wrong functioning in the cooling system.

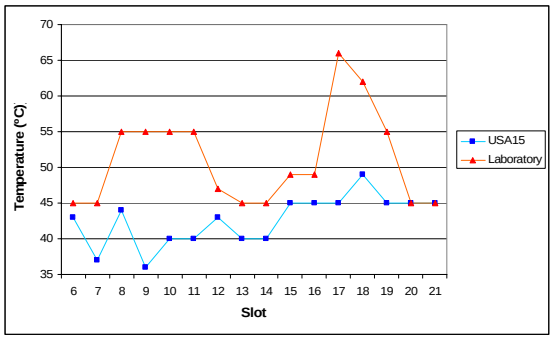

Figure 7: Temperature in G-Link 2 in all the slots of the crate, in the lab and in USA15.

V. Conclusions

The TileCal ROD production has consisted in the fabrication, adaptation to TileCal specifications and validation of 38 RODs. The validation procedure was applied to a complete ROD system composed of a ROD motherboard, two PUs and one TM, which will be installed together in the ATLAS cavern at CERN. A complete test-bench was designed for the ROD production and it continues being utilized on the DSP reconstruction routines tests since it is possible to emulate the front end with real data. Besides, some other firmware upgrades can be developed utilizing the data injection in the test-bench.

During the TileCal RODs adaptation and validation tests some performance errors were found, which were detected and repaired in all the cases. Besides, considering all the burning tests done during the production period, it was concluded that in the ROD system the BER is better than 10^{-13}. This BER is better than the specifications as the G-Link chip manufacturer certifies a BER of 10^{-12}. In addition, the burning tests verified that the air cooling system is enough in TileCal conditions.

All these results are being corroborated during the TileCal commissioning, where the RODs are being integrated in the ATLAS data taking system. Real data from TileCal front end are being processed by the ROD system and successfully analyzed offline.

VI. References

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[3] V.González et al., "Development of the Optical Multiplexer Board Prototype for Data Acquisition in the TileCal system" IEEE TNS, VOL.53, NO.4, August 2006.

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Parallel Session B4

Trigger & DAQ

Recent Developments on the ALICE Central Trigger Processor

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Abstract

The ALI CE Central Trigger Processor has been constructed and tested, and will shortly be installed in the experimental area. In this review, we introduce the new developments in hardware and software, present a measurement of the minimum propagation time, and illustrate various trigger applications.

I. Introduction

The ALICE detector has been designed to operate efficiently under a wide variety of different running conditions. The principal design aim is to allow the study of heavy ion interactions, which are characterized by very high multiplicities. The luminosities are modest compared to those for pp interactions. These two considerations determined the choice of detector technologies for ALICE. In particular, the principal tracking detector is a Time Projection Chamber (TPC), a relatively slow device with a drift time of 88μs that is capable of recording very high track densities. ALICE also contains other detectors which read out more rapidly. However, given a maximum interaction rate not exceeding 200 kHz, it was decided that detectors would not be required to employ pipelining. For this reason, a complex system of dead-time management has been developed to permit these detectors to read out more frequently than the TPC; in addition, the latency of the fastest level of the trigger must be short, to allow its use with track-and-hold electronics.

The study of heavy ions collisions requires collecting considerable statistics in minimum bias events and those selected according only to centrality. At the same time, new trigger signatures have been proposed that have much lower rates, notably those involving high p_T leptons or high p_T jets. Triggers of these types are supposed to run concurrently in ALICE, leading to a very heterogeneous loading of the trigger system. These considerations mean that it is particularly important in ALICE to control the use of resources by different trigger types, allowing sufficient flexibility to weight access to resources according to physics needs, by downscaling and selective disabling of common triggers.

In the past year the construction of the ALICE Central Trigger Processor (CTP) has been completed, with trigger systems in operation at Birmingham and at CERN. In this review, we shall focus on the practical issues related to the commissioning of the trigger system, after a brief overview of the system and its implementation.

II. Overview of the ALICE Central Trigger Processor

The principal features of the ALICE CTP have been described in some detail elsewhere [1,2], and have been discussed at previous workshops [3,4]. A brief description is given here.

The CTP is designed for up to 24 different detectors.. At present there are in practice seventeen detectors in the experiment. These can be grouped into up to six different partitions, referred to as trigger *clusters*. These can each be sent independent trigger signals. Cluster definitions are programmable.

Owing to the low latency for some of the detectors, there are three levels in the ALICE trigger. The fastest level of the trigger, **L0**, has a latency of 1.2 μs (from interaction to the reception of the L0 trigger at the detector). The typical functions of this trigger level are *(i)* to provide a strobe to detectors with fast track-and-hold electronics, and *(ii)* to initiate BUSY for all detectors in an affected cluster. Rate reductions at **L0** are not expected to be high as not all relevant trigger input signals are available at this time. The next trigger level, **L1**, arrives at the detector 6.5 μs after the interaction takes place. At the time of the **L1** decision most of the trigger inputs are available, and therefore major rate reductions can be made. The typical function for this level of trigger would be to store event data in an appropriate multi-event buffer. However, a final decision as to whether to send the data to the data acquisition and High Level Trigger (HLT) system cannot be made at this stage as the final outcome for the past-future protection (see below) is not yet known. The detector with the longest sensitive period in ALICE, the TPC, will register hits up to 88 μs from the time of an interaction. Therefore, the final level of the trigger (**L2**), cannot be given until after this period.

The trigger decisions are made using a total of 60 trigger inputs (24 **L0**; 24 **L1**; 12 **L2**). Owing to the number of inputs at each level, some restrictions are needed on the allowed logic functions. All inputs can be combined in AND. In addition for 6 selected classes the complementary signal can be selected. Finally, for a small subset of inputs (4 **L0** inputs) a look-up table can be used to allow any arbitrary logic function. Four such functions can be defined. Two are used in the past-future protection counters and in the interaction record [1], and two can be added to the list of inputs. In this way, for example it is possible to include an OR of different inputs in the minimum bias interaction definition in low multiplicity pp interactions, in order to improve trigger efficiency.

In order to protect the detector from recording events which have significant levels of overlap from other interactions before or after the one selected by the trigger, a system of past-future protection has been implemented. The details of the circuit have been described in some detail previously [4]. Here we illustrate the functions of the circuit in different conditions.

In heavy ion collisions the rate is such that pile-up has a significant probability in the TPC (>50%), but only a small probability in the other detectors. The overlap of even two full centrality interactions in an event readout would make reconstruction very difficult. In these circumstances, it makes sense to protect the detector over an interval equal to twice the drift time of the TPC, and to reject cases where two interactions having high multiplicity occur inside the protection interval. A different counter is used for low multiplicity events, since here a higher number of superimposed events can be tolerated. Figure 1 shows a schematic diagram of a simple case.

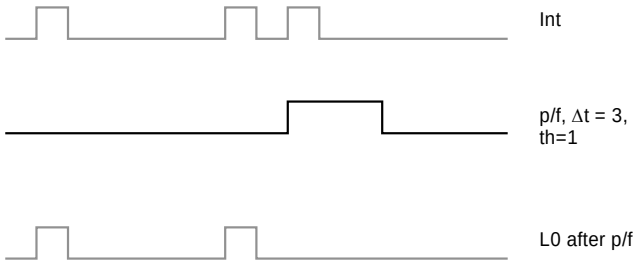

Figure 1: The top trace represents a series of interactions. The middle trace indicates when the past/future protection (with a threshold of 1 and a protection interval $\Delta t = 3$ b.c. is asserted, and the bottom trace shows the final result for an L0 trigger, taking past-future protection into account.

In pp operation, the expected rate is such that pile-up in the TPC is inevitable, but also tolerable owing to the much lower multiplicities. In this case the past-future protection circuit serves to ensure that there is no pile-up in other, faster readout detectors, such as those of the Inner Tracking System (ITS). In this case, using a much smaller time window, it is desirable to check that there is no second interaction accompanying a trigger, with no classification according to multiplicity. It is straightforward to reconfigure the parameters so as to cover both cases.

III. ALICE CTP HARDWARE

Physically, the ALICE CTP is made up of seven different types of 6U board.. There is a board for each of the three levels of trigger (L0, L1 and L2), one for BUSY handling, one to give the interface to the DAQ (INT), some fan-out boards (FO) to transfer trigger signals to the Local Trigger Units, and a board I2C which hosts an I2C multiplexer collecting signals used to monitor voltages on the trigger boards. These are sent on special I^2C lines on the J2 part of the backplane. The signals are transferred to the INT board via the front panel, where they are decoded by an FPGA; the decoded values are accessible via VME.. With the exception of the I2C board, the design for these boards is similar. In each case an ALTERA EPM3512 FPGA provides the VME interface, and also controls the loading of the main logic FPGA. In most cases, the main logic chip is an ALTERA CYCLONE EP1C20 FPGA, and its configuration data are kept in the on-board flash memory (Am29LV081. Additional features include the provision of a 'snapshot memory' (two CY7C-1382 ICs, giving a combined memory of 1 Mwords, 32 bits wide). The snapshot memories, present on every board, are used to record unbiased samples of trigger inputs and decisions for short periods of time (up to about 25 ms i.e. 300 LHC orbits. It is used principally for debugging and development purposes. In addition, a PCF8591T ADC is used to monitor all the supply voltages and the status of fuses on the board. The data are transmitted to the ALICE DCS (slow control system) using the independent I^2C link, as discussed above.

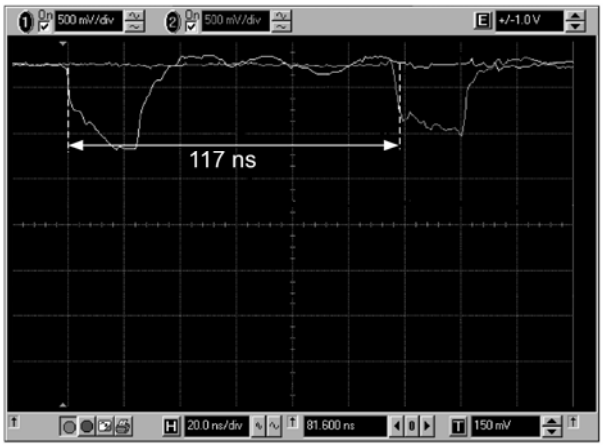

Figure 2: Preliminary measurement of the propagation delay between the arrival of a trigger signal on the L0 board and the production of a trigger on an LTU. (20ns per division)

Figure 2 shows a preliminary measurement of the full propagation delay through the CTP system, from the arrival of a trigger signal at the L0 board to the output of an L0 signal from an LTU board. A minimum latency of 117 ns was found. The contribution of the CTP itself to the trigger latency turns out to be about one bunch crossing less.

Figure 3 shows a recent trigger setup, involving a full set of CTP boards, as used at CERN to transmit trigger signals

to two detector partitions in the DAQ laboratory. This setup is discussed below.

The CTP communicates with each detector independently, since in general detectors may have different triggering patterns. The interface to each detector comes via another VME card, the Local Trigger Unit (LTU). This was described in detail in the 2004 workshop [3]. There is one LTU per detector. The LTU receives signals from the CTP and generates the signals necessary to send to the detectors, via LVDS cables in the case of the L0 signal, and using the RD-12 TTC system for the other signals. It can also be used to emulate the CTP. Extensive facilities exist to emulate different trigger sequences starting in the LTU, including sequences with intentional errors. The LTU can also be used with an external trigger signal for test beam work.



Figure 3: Trigger setup at CERN, showing the full set of CTP boards, together with two sets of TTC interfaces, which transmit to detector emulators about 40m away.

All the VME cards were designed at the University of Birmingham and produced through the Rutherford Appleton Laboratory. 53 LTUs were produced, together with varying numbers of each type of CTP board, so as to allow for an adequate stock of spares. Production is now completed. Many LTUs have been delivered to ALICE detector groups to allow them to test their electronics.

After final tests of the system, three full trigger systems were shipped to CERN in July 2006. Two systems are being used for integrated trigger-DAQ-ECS tests on the CERN Meyrin site, and one is awaiting installation in the ALICE pit. In addition, two complete setups remain in Birmingham, where tests and training sessions are continuing.

The CERN tests use a set of cables and fibres equivalent to those used for connections with detectors in order to connect the trigger and DAQ laboratories. In a first test it was demonstrated that a detector simulator board (a DDG board), connected to the trigger system via a TTC and DDL link, can successfully register trigger words and messages, transferring trigger data correctly to the event headers. The second test is discussed in the next section.

IV. ALICE TRIGGER SOFTWARE

The operation of the ALICE CTP and the LTUs requires the preparation of a large body of software, for example to

- *(i)* configure and load CTP parameters,
- *(ii)* execute, run control functions under the control of the ALICE ECS (Experiment Control System)
- *(iii)* provide monitoring facilities to check for the correct functioning of the trigger, and
- *(iv)* provide debugging facilities for when faults occur.

The software framework for the trigger was decided in 2003. Coding is written mainly in C, and SMI++[5], and either Python/Tk or Tcl/Tk is used for the graphical interface. DIM[6] is used for communication with the DCS and ECS systems. The operating system is LINUX, running on a VME processor (Concurrent Technologies VP315).

Flash memory is used for the configuration of the main FPGA, making it significantly easier to distribute firmware updates to users. (This is important, for example, in the case of LTUs, which are currently being used in ALICE institutes in several different countries.) The user can download the latest firmware versions from the trigger web pages, and load them via VME to the flash memory.

All the CTP boards can be configured and read out with existing software. For example, figure 4 shows a graphical interface used for configuration of trigger classes. Active classes (only) are shown as rows, with the selected trigger inputs and vetos shown according to the column used. This panel combines parameters affecting the three boards L0, L1 and L2. Output clusters are indicated by colours, with a text explanation available by hovering a mouse over the required box. Similar graphical menus exist for all the trigger functions, allowing trigger configurations to be defined and made. Help facilities are also provided. The storage of trigger configurations is being studied; it is expected that a database using MySQL, similar to that being developed by the ALICE ECS group, will be employed.

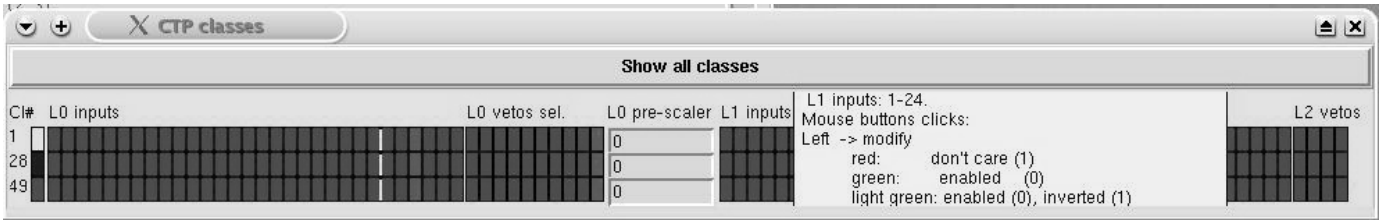

Figure 4: Graphical interface for configuration of trigger classes. In this example three trigger classes (numbers 1, 28 and 49) are in use. Colours are used to indicate the trigger condition; the colours on the far left column of the panel indicate the selected output trigger cluster.

There is a 1 MWord memory on each board, which is used to collect data on a bunch-crossing-by-bunch-crossing basis, creating an unbiased 'snapshot' of the trigger operation. The snapshots are read out through the VME backplane, and are used by online monitoring processors for the CTP; snapshots do not appear in the normal DAQ datastream. They will be heavily used for debugging purposes while the system is being commissioned, as they allow all aspects of the trigger operation to be followed. For many of these, a software simulation of the hardware already exists, allowing detailed checks. They can also be used for timing (alignment) checks, as described by Roman Lietava [7]

As an example of the use of a snapshot, we return to the example of past-future protection, introduced in Section II. Figure 5 shows a snapshot using events on the L0 board. Timings are given in bunch crossing numbers, i.e. in 25 ns increments. The top line shows a randomly occurring trigger input which is included in the interaction definition but does not produce a trigger. The next line shows another interaction contribution which does produce a trigger. The interaction definition used for the past-future protection is the OR of these two contributions. In order to see the action of the past-future protection, two classes are activated, both with the same input conditions. In one case a past-future protection spanning 15 BCs is set; in the other there is no past-future protection requirement. The pulse at bunch crossing 1038 makes a potential trigger in both classes. However, the burst of activity in the random trigger immediately before (BCs 1031-1033) fires the past-future protection, shown in the bottom line in the snapshot. Thus the class with past-future protection (`l0clst1`) gives no trigger, as the trigger is vetoed by the past-future protection, while the class without past-future protection (`l0clst4`) does give a trigger.

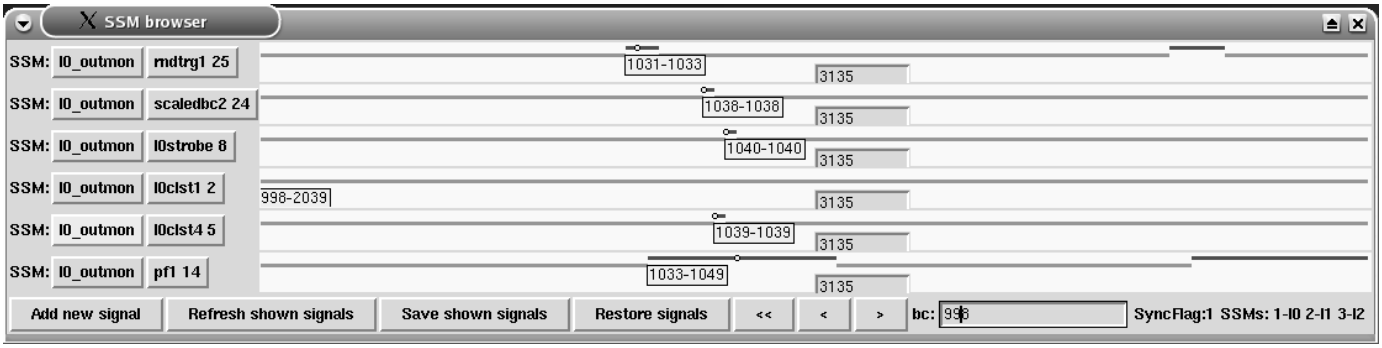

Figure 5: L0 Board snapshot showing the action of past-future protection. The past-future protection circuit is activated by the OR of activity in the signals shown in the first two rows, but only the second row (`scaledbc2`) is used in the trigger. There are two classes with different output clusters. In one (`l0clst1`) there is a past-future protection interval of 15 BC, while in the other (`l0clst4`) there is not. The interval when the past-future protection is asserted is shown in the bottom row (`pf1`), and prevents a trigger from being generated in `l0clst1`.

Software is also needed to provide the interface to the ECS system. This is under development, using the combined trigger-DAQ-ECS system at CERN for tests. The ECS system foresees splitting the ALICE detector into partitions, which are non-overlapping (no detector is allowed to be in more than one partition). Partitions have independent DCS, and can be operated independently as if they were separate sub-experiments. (This will be particularly useful during the commissioning phase.) Trigger clusters have a different logic, as they can be overlapping, so the trigger-ECS interface has had to be written so as to respect the constraints imposed by the ECS partitions. This has been tested. In a separate development, the start-of-run sequence, which is co-ordinated by the ECS, has been implemented. At start-of-run, the ECS ensures the detectors are ready (using the DCS system), the DAQ is ready and the trigger is set. When all is ready, a signal is sent to the CTP to generate a special "start-of-run" event, which is specially treated by the DAQ. A corresponding "end-of-run" event is sent to signal the end of data-taking. At present, runs can be started and stopped in the test system, and partitions of arbitrary nature can be configured, with the corresponding constraints taken into account in the allowed CTP cluster definitions.

V. SUMMARY

Construction and testing of the ALICE CTP has been completed. Five full setups exist, allowing tests and training to proceed in parallel at CERN and Birmingham. The minimum L0 latency of the CTP has been found to be about 90ns, i.e. within the system requirements [8].

Software exists allowing the full configuration of the system, and monitoring tasks are under development. In particular, the use of 'snapshots', illustrated in this report, allows very detailed study of CP operation. The CERN tests are being used for integration of the CTP with the other ALICE control systems, and installation in the ALICE pit is expected to start by the end of October 2006.

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Timing in the ALICE trigger system

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Abstract

In this paper we discuss trigger signals synchronisation and trigger input alignment in the ALICE trigger system.

The *synchronisation* procedure adjusts the phase of the input signals with respect to the local Bunch Crossing (BC) clock and, indirectly, with respect to the LHC bunch crossing instant. The synchronisation delays are within one clock period: 0-25 ns.

The *alignment* assures that the trigger signals originating from the same bunch crossing reach the processor logic in the same clock cycle. It is achieved by delaying signals by an appropriate number of full clock periods.

We propose a procedure which will allow us to find alignment delays during the system configuration, and to monitor them during the data taking.

I. Introduction

The ALICE trigger system [1] is designed to combine and synchronise the information from all the trigger detectors in ALICE, and to send the correct sequence of trigger signals to all detectors in order to make them read out correctly. The trigger inputs are divided into three different levels L0, L1 and L2, which have different associated latencies. The ALICE trigger system consists of three subsystems:

- The Central Trigger Processor (CTP) [2], which receives inputs from trigger detectors and makes trigger decisions,

- the Local Trigger Unit (LTU) [3], which uniforms interface between read-out detectors and the CTP,

- Trigger and Timing Control partition (TTC) which transmits the LHC bunch crossing clock and delivers trigger signals and trigger messages to detectors.

During the installation and commissioning of the ALICE detector, a number of timing operations need to be done, in order to ensure that trigger coincidences are correctly identified, that the correct signals are recorded in the detectors, and that events in each subdetector are correctly labelled with orbit and bunch crossing number.

In the first part of this paper the task of synchronising the signals of different subsystems is briefly discussed.

The second part deals with the procedure of trigger input alignment. We shall present an estimate of the time necessary to measure reliable alignment delays in different circumstances (cosmic trigger, beam gas interaction and beam-beam interaction) and using different implementation of the method in the ALICE environment. A strategy for monitoring the synchronisation and alignment will also be presented.

Finally a procedure for setting the synchronisation parameters and the alignment delays will be proposed.

II. Synchronisation

Synchronisation is necessary at two points of the ALICE trigger system. The phases of trigger inputs relative to the CTP bunch crossing clock and the LTU inputs relative to the LTU bunch crossing clock are to be adjusted. The system provides for an automatic measurement of the phase shift of all trigger inputs relative to the CTP clock and the phase of the LTU inputs relative to the local LTU clock. In both cases, following the measurement, a programmable hardware option is used to adjust the phase of the signals appropriately.

There are up to 60 trigger inputs to the ALICE CTP generated at nearly as many locations and all connected via individual cables. The phase measurement is done using the ADC on the L0, L1 and L2 boards and programmable delay line on the BUSY board. The generation of the ADC inputs is shown in Figure 1. At the time of measurement the trigger detectors are required to generate a pattern of alternating ones and zeros (Figure 1).

The right plot in Figure 1 shows the delay scan of a trigger input when the local BC clock is delayed in steps of 1 ns from 0 to 31 ns. The value of the delay when abrupt changes occur must be avoided in the final settings, since it can introduce an unacceptable time jitter.

After the measurement, synchronisation is achieved by setting the sampling of the input signal using either the rising or the falling edge of the BC clock to guarantee a safe margin outside the setup and hold time.

The CTP - LTU synchronisation is done in very similar way. There is a delay line in the LTU input which allows to perform scan and set the optimal value for the input signal delay. The ADC mechanism is the same as on the L0, L1 and L2 boards.

The procedure allows for automatic monitoring of synchronisation, which will be done outside the physics run.

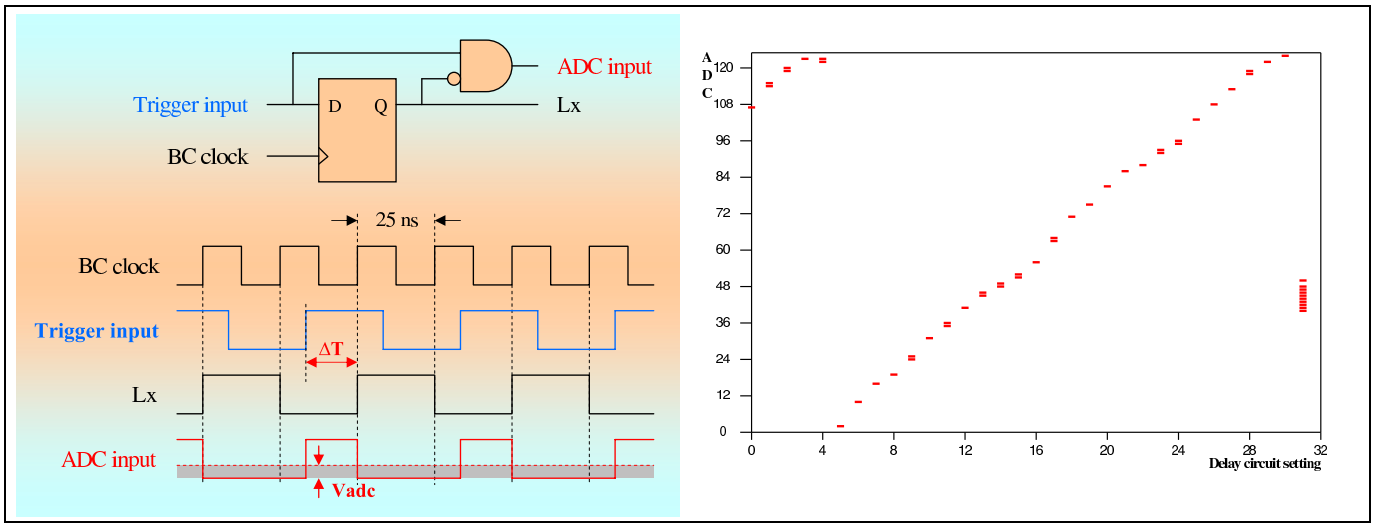

Figure 1: Left panel: measurement of the trigger input phase. The width of the ADC input signal is converted to a DC voltage V_{ADC} with a low pass RC filter (integrator). The ΔT, and the corresponding amplitude V_{ADC} of the DC voltage measured by the ADC, are proportional to delay between the trigger input and its CTP analogue - Lx - clocked by the local BC clock. Right panel: a delay scan of the ADC. The abrupt changes around $\Delta T = 4ns$ and $\Delta T = 30ns$ occur when the transition of the signal coincides with the rising edge of the BC clock.

III. Alignment

Once synchronisation of signals has been achieved, it can still happen that signals produced by the same event are separated by an integer number of bunch crossings. The process of alignment consists of adjusting these signals so as to make them coincide. While it would be straightforward enough to do this with low intensity collisions, it is more difficult to align signals with only one beam or high intensity collisions with background.

The starting point of alignment is to estimate the time intervals between collision and arrival of the trigger input signals to the CTP including the passage of particles through the trigger detectors, front end electronics response and signal propagation over the cable. The CTP hardware provides a 16 BC time window for arrival of the trigger input signals from the different trigger detectors.

We discuss the automatic alignment procedure based on a correlation analysis of different trigger inputs. The method is suitable in the case of high intensity collisions and in the presence of noise. The method is introduced in section A. The feasibility of the method for different beam conditions is discussed in section B. The different scenarios for implementation of the correlation analysis are evaluated in section C.

A. Correlation analysis

First we describe the idea of correlation analysis in the case of a detector with efficiency ϵ and no noise. We try to align two detectors A and B. The detector A produces a time sequence of input signals a_i, where i is the time when signal arrives at CTP. The time i measured in bunch crossings is an integer number. The a_i can have only two different values: $a_i = 0$ (no signal present at time i) and $a_i = 1$ (detector A produces signal at time i). Similarly for detector B we have a time sequence b_i.

We define the correlation function

$$C_N(\delta) = \frac{1}{N}\sum_{i=0}^{N-\delta} a_i b_{i+\delta} \qquad (1)$$

where δ is a delay of signal from detector B with respect to detector A and N is the number of bunch crossing available for analysis. It is obvious that function $C(\delta)$ has a maximum when detectors are aligned:

$$C_N(\delta = d) = r\epsilon_a\epsilon_b$$

where d is correct delay, r is the probability to have interaction in a bunch crossing and ϵ_a (ϵ_b) is the efficiency of detector A (B). The efficiency includes both the geometrical acceptance and the efficiency to produce a signal if a particle passed the detector. In the case when the delay is not equal to the correct value the correlation function is

$$C_N(\delta \neq d) = r^2\epsilon_a\epsilon_b.$$

In both cases the C_N has a binomial distribution (normal for large N) with standard deviation $\sigma^2 = C_N(\delta)/N$.

To estimate the number of events necessary for alignment we define the separation function as the difference of the correlation function in the aligned case and nonaligned case divided by the sum of variances of the aligned correlation function and nonaligned correlation functions:

$$S(r, \epsilon_a, \epsilon_b) = \sqrt{N}\frac{C(\delta = d) - C(\delta \neq d)}{\sqrt{C(\delta = d) + C(\delta \neq d)}} \qquad (2)$$

To get a 3 σ separation with $r = 0.005$ (200 kHz) and efficiencies 0.8 thousand events need to be collected. The situation is less favourable taking into account the noise. Noise is defined as trigger detector signal produced without the collision. The formulae with random noise taken into account are in Ap-

pendix. The correlated noise can be identified by an autocorrelation function analysis

$$A_N(\delta) = \frac{1}{N}\sum_{i=0}^{N-\delta} a_i a_{i+\delta}$$

and taken into account.

Additional information of the beam crossing structure can be used to improve the method.

B. Beam conditions

While the synchronisation is a fully internal procedure of the trigger system, alignment relies on the presence of external physics signals. The feasibility of the method is evaluated in three different cases:

- without a beam (cosmic trigger),
- with one beam (beam gas interaction),
- with both beams.

The cosmic particles are coming mostly in the vertical direction. On the top of the ALICE detector there is an array of scintillators - ACORDE- which will produce efficient cosmic trigger with the rate few Hz/m^2 [8, 7]. The use of this source of particles for other subdetectors is limited by their acceptance. Low intensity cosmic trigger would allow the alignment of trigger detectors with the oscilloscope.

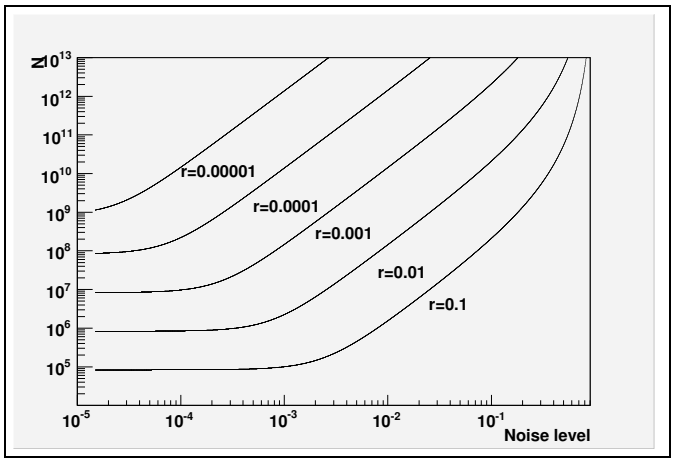

Figure 2: The number of events necessary for 1 σ separation as the function of noise level $\nu = \nu_a = \nu_b$ for different values of probability of interaction in a BC $r = 0.1$, 0.01 and 0.001, 0.0001 and 0.00001. The number of filled bunches $k_b = 43$. The detector efficiencies are $\epsilon = 0.1$ and $\epsilon_b = 0.1$. The formulae from the appendix are used to produce this plot.

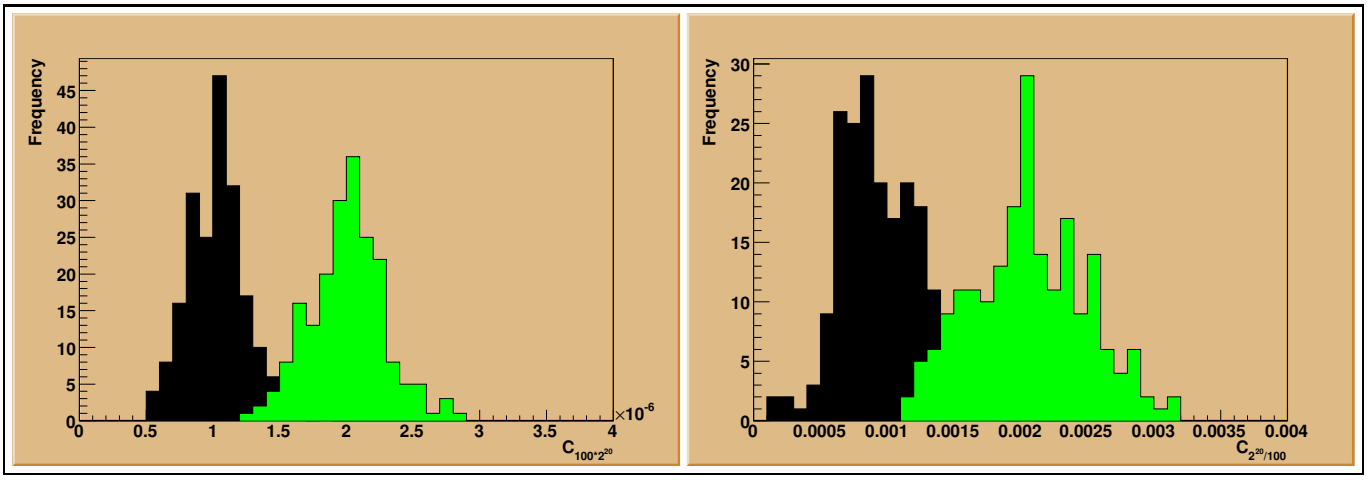

Figure 3: Left panel: The correlation function for the parameters probability of interaction in a BC $r = 0.001$, detector efficiencies $\epsilon_a = 0.8$, $\epsilon_b = 0.1$, and noises equal to $\nu_a = r$, $\nu_b = r$, number of filled bunches $k_b = 43$. The correlation function is sampled for $20 \cdot 2^{20}$ events in order to see the spread of the distribution. Right panel: The correlation function with probability of interaction in a BC $r = 0.15$, ($L = 10^{30}$, $k_b = 43$) detector efficiencies $\epsilon_a = 0.8$, $\epsilon_b = 0.8$ and noises $\nu_a = r/5$, $\nu_b = r/5$. The black (dark) histogram corresponds to correlation function for detectors not aligned. The green (light) histogram corresponds to correlation function for aligned detectors. The correlation function is sampled for 2^{20} events in order to see the spread of the distribution.

The beam gas interactions which would be available during the LHC commissioning with one beam circulating should be used for alignment of trigger detectors. The probability of beam-gas interactions in one BC clock is estimated as

$$r = n\sigma L N_p$$

where n is the residual H_2 equivalent gas concentration in the beam pipe, σ is the p-p inelastic cross section, L is the length of the LHC straight section at interaction point and N_p is the number of protons in a bunch. Taking H_2 equivalent gas density $1.9 \cdot 10^{14} m^{-3}$ [5], p-p inelastic cross section $\sigma = 70$ mbarn, $N_p = 9 \cdot 10^{10}$ protons per bunch [6], and $L = 20m$, the probability of interaction in a single bunch is $r = 0.0024$. This is equivalent to 27 Hz rate per bunch. The spread position of interaction vertex may lead to sizable difference in detector efficiencies, especially in the case of a detector with sensitive volume perpendicular to the beam (V0) with respect to a detector with sensitive volume parallel to the beam (Pixels). The additional

background from beam halo particles would produce a noise. About 10^8 bunch crossings are to be collected in this case, (Figure 2), assuming a large relative noise and low detector efficiencies. On the left panel of Figure 3 the results of the Monte-Carlo simulation are presented in this extreme case.

In the standard situation with two beams the beam gas background would be reduced by a factor of 30 [5] relative to LHC start-up. The well defined position of interaction vertex and left-right symmetry of collisions and detectors would increase detector efficiencies. The probability of an interaction in a bunch crossing is $r = \sigma L / f_{LHC} / k_b$ where σ is p-p inelastic cross section, L is the LHC luminosity, f_{LHC} is the LHC revolution frequency and k_b is the number of filled bunches. About 10^5 bunch crossings are necessary (Figure 2) for alignment. The Monte-Carlo results in this case are shown in Figure 3, right panel.

C. Implementation of the method in ALICE

There are three different ways of implementation of the correlation analysis in the ALICE trigger system:

- trigger input recording in the CTP (snapshot memory),
- trigger class counting,
- data recording through the ALICE data acquisition system (DAQ).

The time needed to complete alignment depends on the number of bunch crossings $N(r, \epsilon, \nu)$ we need to collect for given separation (2), which is a function of interaction rate, detector efficiencies and a noise.

The trigger input recording in the CTP is the most robust of these methods. It enables unbiased collection of the trigger input signals on every trigger level. The case of trigger input recording in the CTP relies on the use of the snapshot memory. Each board contains a memory with a capacity of 1M word which records the trigger inputs (and also other signals for testing and monitoring purposes). The snapshot memory can be read via the VME in about $1.25s$ time. The time necessary to collect N bunch crossings is therefore

$$\frac{N}{2^{20}} \cdot 1.25 sec$$

The scan of the delay δ would be done offline.

In the trigger class counting method the CTP is programmed to provide the trigger classes as coincidences of trigger inputs. The coincidences are actually hardware calculation of the correlation function (1). The delay δ, which needs to be scanned, can be controlled by a hardware delay set on the L0, L1 and L2 boards for L0, L1 and L2 inputs respectively. The number of classes necessary for alignment of n_{inputs} is $n_{inputs} - 1$. Let us assume that the signals are not misaligned by more than δ_{max} (the hardware allows for $\delta_{max} \leq 16$). The time necessary for alignment is in this case

$$N \cdot \delta_{max} \cdot 2.5 \cdot 10^{-8} sec$$

where N is the number of bunch crossings for required separation of the correlation function. The trigger class counting method enables an unbiased calculation of the correlation function on the L0 level, while the bias introduced on the L1 and L2 levels due to the deadtime has to be taken into account.

The last option is the use of the ALICE data acquisition system. The correlation analysis in this case is more complicated since the data are biased even at the L0 level.

The estimates show that the trigger class counting method and the data recorded directly in the CTP require about the same amount of time to collect enough statistics, while the use of DAQ is more time consuming. Note also that the first two methods can collect data and calculate correlation function simultaneously. Figure 2 shows that even in the very extreme case of low detector efficiencies, a large noise and a low interaction rate, 10^{10} BCs would be enough for alignment which corresponds to one and half hour of measurement time.

The methods with trigger input recording and data recording by DAQ also provide a continuous monitoring of alignment without interference with data taking.

IV. Setting procedure

The algorithm which shall find the optimal settings for synchronisation and alignment is formulated.

1. Synchronise trigger inputs with arbitrary setting of BC delay, e.g. the value zero.
2. Align trigger inputs.
3. Find the latest arriving trigger input and set the BC delay to sample it as early as possible, allowing for a sufficient safety margin.
4. Using the measurement taken at 1. recalculate the synchronisation parameters with the adopted setting of the BC delay. Alternatively repeat the synchronisation procedure with that BC delay setting.

The condition that the latest input should be optimally delayed with respect to CTP bunch crossing clock guarantees a minimum delay time for the latest trigger input.

V. Summary

The synchronisation of the ALICE trigger system has been described. An automatic alignment procedure has been proposed. Method provides the alignment in the acceptable timescale (hours in the worst case). It also allows continuous alignment monitoring. Finally a procedure for setting the timing parameters for ALICE trigger system has been formulated.

VI. Appendix: correlation function with random noise

The formulae for the correlation function are presented. The ν_a (ν_b) is the probability to generate a trigger signal in detector A (B) for whatever reason in the absence of collision.

The aligned correlation function for LHC with all bunches filled is:

$$\begin{aligned} C^{alFULL} =& r\epsilon_a\epsilon_b + \\ & r(1-\epsilon_b)\epsilon_a\nu_b + r(1-\epsilon_a)\epsilon_b\nu_a + \\ & (1-r)\nu_a\nu_b + r(1-\epsilon_a)(1-\epsilon_b)\nu_a\nu_b \end{aligned}$$

where the first term is for signal coincidence, the next two terms are for signal and noise coincidence and the last two terms are for noise coincidence in the case of no collision and signal failure due to the detector inefficiency.

The misaligned correlation function in the case of filled LHC is:

$$\begin{aligned} C^{nalFULL} =& r^2\epsilon_a\epsilon_b + \\ & r(1-r\epsilon_b)\epsilon_a\nu_b + r(1-r\epsilon_a)\epsilon_b\nu_a + \\ & (1-r\epsilon_a)(1-r\epsilon_b)\nu_a\nu_b \end{aligned}$$

where the first term is for signal coincidence, the next two terms are for signal - noise coincidences and the last term is for noise-noise coincidence.

The correlation function with some bunch crossing empty depends on the distribution of the bunch crossings in the LHC orbit. The formula for uniformly distributed k_b bunch crossings in the aligned case is

$$C_N(\delta = d) = fC^{alFULL} + (1-f)\nu_a\nu_b$$

where $f = k_b/3564$.

The nonaligned correlation in the case $k_b << 1$ is

$$\begin{aligned} C_N(\delta \neq d) = & f \cdot [r(1-r\epsilon_b)\epsilon_a\nu_b + r(1-r\epsilon_a)\epsilon_b\nu_a] + \\ & (1-2f)\cdot\nu_a\nu_b \end{aligned}$$

In general case the Monte-Carlo provides the correlation function calculation.

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The ALICE silicon pixel detector read-out electronics

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Abstract

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system [1]. The SPD contains 10 million pixels segmented in 120 detector modules (half staves), which are connected to the off-detector electronics with bidirectional optical links. Raw data from the on-detector electronics are sent to 20 FPGA-based processor cards (Routers) each carrying three 2-channel link-receiver daughter-cards. The routers process the data and send them to the ALICE DAQ system via the ALICE detector data link (DDL). The SPD control, configuration and data monitoring is performed via the VME interface of the routers.

This paper describes the detector readout and control via the off-detector electronics.

I. Introduction

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system which contains 10 million pixels organized in 120 detector modules called half-staves. Each half stave consists of a linear array of 10 ALICE pixel chips bump bonded to two silicon sensors and is read out using a multi-chip module (MCM) [2-5]. The ALICE trigger has three stages (L0, L1, L2) whereas the SPD system uses L1 and L2 triggers only. The pixel chips provide binary hit information, which is stored in a delay line during the L1 decision time. In case of a positive L1 decision the hit is stored in one out of four multi-event buffers where the data wait for the L2 decision to be read out or discarded. The ALICE trigger scheme foresees a non-pipelined architecture and allows the detector read-out systems to temporarily reject triggers by sending a busy signal to the central trigger processor. The ALICE SPD off-detector electronics controls, configures and reads out the detector via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) for permanent storage. The SPD control, configuration and data monitoring are performed using the VME interface of the routers. In Table 1 are summarized main system parameters for SPD.

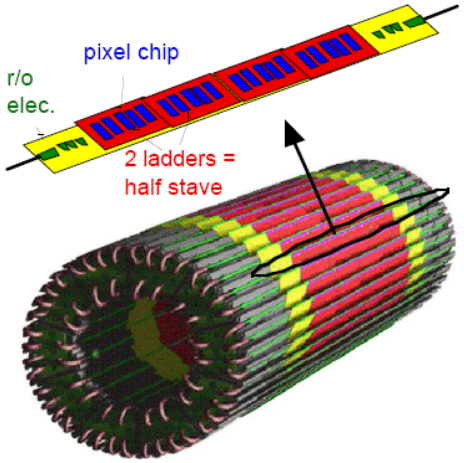

Figure 1: Silicon Pixel Detector

A. *Main system parameters of SPD*

The main system parameters of SPD are in Table 1.

Table 1: Main system parameters

L1 rate	1 kHz
L1 latency	6.5 μs
L2 rate	40–800Hz
L2 latency	100 – 500 μs
Read-out time	256 μs
Multi-event buffers	4
Total Ionizing Dose (inner layer)	2.5 kGy (10 years)
Fluence (1MeV equivalent)	$3x10^{12}cm^{-2}$(10 years)
Material budget per layer	<1% X_0

B. *General readout scheme*

Configuration and trigger data are sent from the VME based electronics (router and link receiver card) in the control room to the on-detector electronics via two optical fibers, one carrying the clock and one carrying serial data. On the detector the PIN diodes in the optical package and the RX40 chip [6] convert the optical signals to electrical signals. The PILOT2003 chip [7,8] initiates the read-out of the pixel chips and controls the ANAPIL chip, which provides analog bias voltages to the pixel chips and measures supply, bias voltages

and the temperature on the detector. Once read-out has been initiated the nonzero-suppressed data are sent from the pixel chips via the PILOT2003 [18] and an 800 Mbit/s G-link compatible optical link driver chip GOL [9,10] and an optical fiber to the control room. The description of row data format is in [16]. There the data are zero-suppressed and formatted in the FPGA-based link receiver mezzanine board. Three such boards, each one serving 2 data channels, are located on one router module. The router performs data multiplexing and establishes the interface to the ALICE trigger and data acquisition. In total 20 router cards read out the 120 half staves. Figure. 2 shows a block diagram of the full SPD read-out chain.

One ALICE standard detector data link DDL [11] per router is used to transmit the data stream to the ALICE DAQ [12,19]. The data are read-out from the link receivers and stored in the FIFO memory inside Router FPGA which is connected to one DDL module. When the DAQ is ready data are immediately sent through the FIFO and DDL module to the DAQ. If the DAQ in not ready data are stored in the FIFO and it waits until the DAQ will be ready.

The Router communicates with the Detector Control System (DCS) through the VME bus. The SPD DCS monitors the read out electronics and the detector services. For monitoring purpose the DCS can read dual-port memory on the Router where samples of data flowing to DAQ are stored. The DCS is responsible for the detector configuration.

In the Router FPGA 6 independent JTAG controllers are implemented. Each controller sends configuration data to the pixel detector. The controllers can run in parallel so that the data are sent to all channels simultaneously.

It is possible to load new code to adapt data processing capabilities to any possible new requirements into FPGAs and EPROMs through remote programming based on JAM player software and the VME access to the Router.

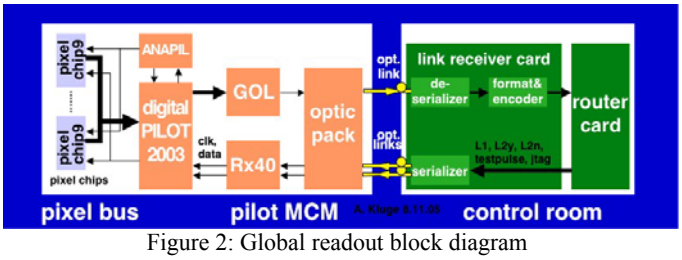

Figure 2: Global readout block diagram

II. LINK RECEIVER

Each of the two link-receiver channels has three optical fibre links; two links for the clock and the serial trigger, control and configuration data and one 800 Mbit/s G-link compatible link to receive data from the detector.

On the link receiver the pixel data stream from the detector is de-serialized, the received data is checked for format errors and the data are stored in a buffer-FIFO before data are zero suppressed, encoded, re-formatted and written to a dual port memory. When all data from one event are stored in the dual port memory on the link receiver, the link receiver asserts event ready flag to be read out by Router processor. The Link receiver also asserts to the Router processor the error flags, that are identified in the data stream coming from detector, like busy violation, idle violation, Glink down error, Glink transmission error, FIFO overflow, memory overflow, Single Event Upset (SEU) error, control error, control detector feedback error and control pixel error. Busy violation is asserted when a 5th L1 trigger signal has been received by the on detector electronics, although all (4) multi event buffers were full and the corresponding busy signal (which has been sent to the trigger) has been active. Idle violation is asserted when a L2 signal (either L2y or L2n) has been received by the on detector electronics although no corresponding L1 signal has been received. Glink down error is asserted when the data link was down during the event read out. The Glink transmission error is asserted when Glink receiver found a error in transmission protocol during the readout of the corresponding event. The FIFO overflow is asserted when at least one of the pixel converter readout FIFOs was full at least once during the data read out. The memory overflow is asserted when at least one of the pixel converter readout memories was full at least once during the data read out. SEU error is asserted when it was detected and was not recovered by the on detector electronics. The control error is asserted when in the control link (from the control room to the detector) a transmission error occurred between the precedent and the actual read out of the corresponding event. All control signals sent to the detector (L1, L2y, L2n, test signal, JTAG signals) are sent back on the fast link for error detection. The control detector feedback error is active if one of the signals sent to the detector was not received back between the precedent and the actual event read out. The control pixel error is asserted when error occurred on the pixel chips. . This error information is sent to the DAQ together with event data in DAQ header.

The G-link receiver deserializes the data stream and recovers the 40 MHz transmission clock using a commercial component (Agilent HDMP1034) [16]. The implementation of the link receiver is also based on a commercial FPGA and dual port memories. Figure 3 shows a block diagram of the link receiver. The expected occupancy of the detector will not exceed 2%. It is therefore efficient to encode the raw data format after zero suppression. In the raw data format the position of a hit within a pixel row is given by the position of logic '1' within a 32-bit word. The encoder transforms the hit position into a 5-bit word giving the position as a binary number for each single hit and attaches chip and row number to the data entry. The output data from the FIFO are encoded and stored in an event memory in a data format complying with the ALICE DAQ format [13].



Figure 3: Block diagram of the link receiver

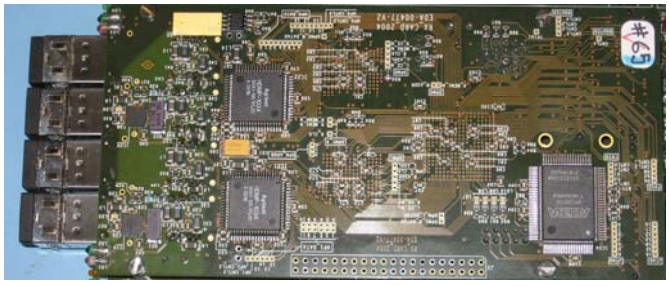

Figure 4: Link receiver (transceiver)

III. ROUTER

The Routers receives the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip [14] and forwards the trigger commands to the pixel detector. Upon reception of the L1 trigger signal the Router sends trigger signals to the detector and the pixel data are copied into multi-event buffers on the pixel chips. After reception of the positive L2 decision, the Router starts to check the event ready flag in the status register of the link receivers. When event ready flag appears the router processor reads the data from the link receiver dual port memory.

Each Router sequentially reads one event from each of the link receiver channels in order to merge data from the 6 channels and labels them with trigger and status information to build one router sub event. The sub events of each of the routers are sent to the ALICE-DAQ system through the ALICE detector data link (DDL). The read out data stream can also be copied into a dual port memory, where it is accessible for data monitoring and analysis via the VME-interface. The Router architecture is shown on Figure 5.

The data access for the SPD control and configuration is performed via the router VME-interface. The router converts the data to JTAG compatible commands which are sent to the detector through the optical links with a maximum data rate of 5 Mbit/s.

The Router is a 10-layers Printed Circuit Board with a 1020 pins chip Altera Stratix EP1S30 component as main processor. The VME interface is inside an Altera APEX EP20K60EQC FPGA with 240 pins.

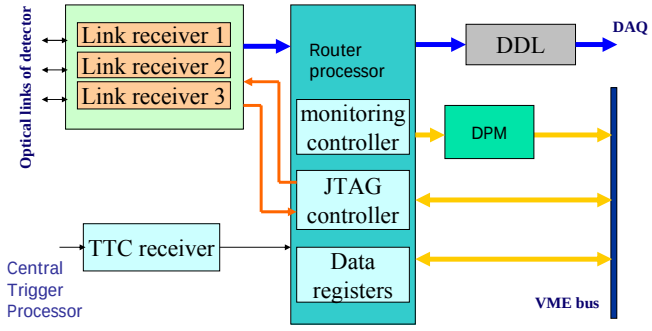

Figure 5: Router architecture

A. *JTAG controller for the configuration of the pixel readout chips*

For the pixel readout chip configuration a specific JTAG controller is used. Each Router has 6 independent JTAG controllers: one each channel serving one half-stave. It works with macro instructions which are stored in the input FIFO memory. Upon receiving the command "execute start" from VME bus, the JTAG controller starts to read data from the input FIFO memory processes the required operations i.e. sends appropriate TCK, TMS, TDI signals to the pixels chips and stores the data received from pixel chips i.e. stores TDO signals to the output FIFO. The data from the output FIFO can be read-out via VME bus. All 6 channels can be programmed with the same data in parallel. The format of the JTAG controller data is described in [15].

B. *Remote programming*

The Router and the link receivers employ ALTERA FPGAs and EPROMs only. This allows to use ALTERA JAM player software for remote programming of these devices. All these devices are in one JTAG chain (Figure 6) and can be programmed remotely using the JAM player software and the JAM player logic inside the VME FPGA. The VME FPGA cannot be programmed because it is used as driver for the JTAG chain.

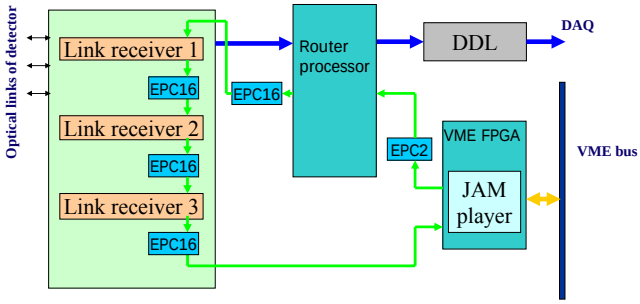

Figure 6: Altera devices on the Router in JTAG chain

C. *Temperature interlock*

The Router receives in the data stream from the pixel detector also temperature information of the pixel sensors and the MCMs. This information is taken from analog-digital converters which are connected to temperature sensors (Pt-1000). The deserialized temperature values are compared in the Router FPGA with the temperature limit. In case the temperature exceeds the temperature limit the Router sends temperature interlock as LVTTL signal to the low voltage power modules. One Router can monitor 6 channels i.e. temperature from 6 half-staves. One low voltage module which has one interlock input provides voltages for 6 half-staves. In case the interlock signal is active, the voltages for all 6 half-staves will be switched off.

D. *TTC interface*

The Router receives the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip [13] and forwards the trigger commands to the pixel detector. In the Router FPGA the L0 signal, L1 signal, L1 message, L2 message are decoded. These trigger signals and the messages are checked, aligned and stored in the trigger FIFO inside Router FPGA. In case of a trigger error the information is sent to the DAQ system in DAQ header [13]. State machines inside the Router FPGA check the number of L1 and L2 triggers and in case that there are 4 L1 triggers and no L2 trigger the Router sends the BUSY signal to ALICE CTP. All information coming from TTCrx chip is written into the dual port FIFO memory for synchronization. It is clocked with an adjusted clock produced by the PLL inside the Router FPGA. This clock is necessary for the proper trigger data registers timing. The other side of the dual port FIFO memory is clocked with the global system clock and trigger data are in this way synchronized with the main FPGA clock.

E. DAQ interface

The data are read-out from the link receivers and are stored in the FIFO memory inside the Router FPGA which is connected to DAQ interface. If the DAQ is ready, then FIFO is immediately enabled for sending data to the DAQ. If the DAQ is busy then the data from the current event are stored into the FIFO memory and they are waiting in the FIFO memory until DAQ is ready. The Router creates also the DAQ header for DAQ system (8 x 32bits) which contains information from trigger messages and front-end electronics. The DAQ header is described in [13].

F. Interface between Router FPGA and link receivers

Upon receiving the L2accept trigger from ALICE CTP the Router starts to check the event ready bit in all 3 link receivers. When the event ready is active in all 3 link receivers, the Router reads 4 registers in each link receiver to get the information about the start address and the length of event stored in the link receivers and the information about errors occurred on the detector. After reading this information the Router starts the data read-out from the dual-port memory of each link receiver and merges the data from 6 channels. If the Router does not find the event ready flag after time necessary for readout in a channel, this channel will have timeout flag asserted in the DAQ header. The Router does not read data from this channel and DAQ is informed about the timeout in this channel. The errors occurred on the detector are also send in the DAQ system in the DAQ header.

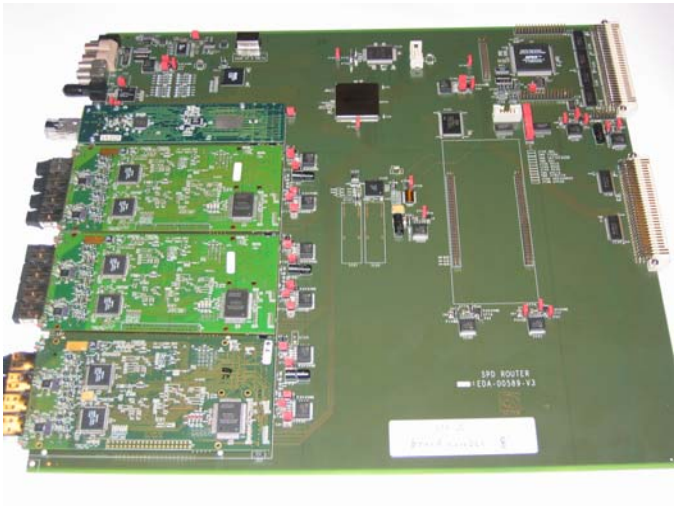

Figure 7: SPD Router

IV. INTEGRATION AND COMMISSIONING

The full SPD read out chain was successfully operated with two half staves during a joint ITS beam test in November 2004, together with a few modules of the other ITS subdetectors (silicon drift (SDD) and silicon strip (SSD)). The functionality and the interface of the off-detector electronics to the ALICE TTC, the DAQ, a simplified version of the DCS system and the on-detector electronics were verified in a combined run with SSD and SDD during 11 hours. Some 5.10^6 events were recorded without errors during this run.

The SPD detector system including the off-detector electronics is currently pre-installed in the CERN Divisional Silicon Facility (DSF) – a clean room where the full detector system is integrated and commissioned before being moved to the underground area. On Fig. 8 is shown one of two VME crate equipped with 10 SPD Routers.



Figure 8: 9U/6U VME crate with 10 final SPD Routers

V. SUMMARY

The integration of the ALICE SPD off-detector electronics with its many challenging technical developments is presented. All the off-detector electronics modules have been produced and tested with final detector elements and have proven to satisfy all specifications. Integration and commissioning of the final system are in progress.

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The ALICE Silicon Pixel Detector Control System and Online Calibration Tools

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Abstract

The ALICE Silicon Pixel Detector (SPD) contains nearly 10^7 hybrid pixel cells. The operation of the SPD requires on-line control and monitoring of some 2000 parameters and $\sim 50000 DACs$. Information for each channel is stored in a configuration database. Timing and data management ($\sim 6GB$ of raw data each calibration) are critical issues. An overview of the SPD electronics read out chain and of the detector control system is given with a detailed description of the front-end controls and the calibration strategy. The status of commissioning and a preliminary evaluation of detector performance are presented.

I. Introduction

The operation of the ALICE Silicon Pixel Detector (SPD) requires the on-line control and monitoring of a large number of parameters. This task is performed by the SPD Detector Control System (DCS). The DCS also has a key role in the calibration of the detector. These combined functions increase the complexity of the system, whose main features are presented and discussed in the following sections.

II. Main features of the electronics system

The SPD (see Fig. 1) constitutes the two innermost layers of the ALICE Inner Tracking System (ITS) at radii of 3.9 cm and 7.6 cm respectively.
The detector consists of 120 half-staves (HS) mounted on 10 carbon fibre support sectors. An HS is an assembly of two ladders glued and wire-bonded to a multi-layer interconnect (the pixel bus) that distributes power and signals. Each ladder consists of 5 pixel chip ASICs [10], 150 μm thick, bump bonded to a 200 μm thick silicon sensor and contains nearly 41k active hybrid pixel cells with dimensions of 50 μm (rϕ) x 425 μm (z). A Multi Chip Module (MCM) [5] on each half-stave distributes the timing signals, provides the required analog references and performs data multiplexing and serialization. The communication between the MCM and the counting room is via optical links with three single-mode fibres. The front-end electronics clock speed is 10 MHz (heavy ion operation). The readout data stream uses a G-link compatible protocol with a 800Mb/s clock. Zero suppression and data encoding are performed in the Link Receiver mezzanine cards (LRx) in the VME based Router readout modules. One Router with three LRx cards [9] serves a half sector (6 half-staves) and has optical links to the experiment DAQ and trigger system.

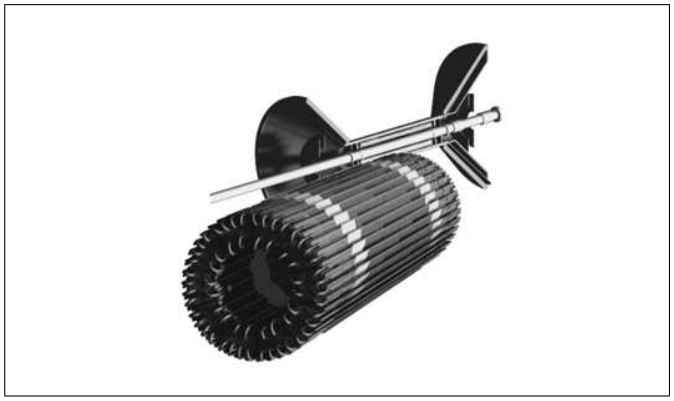

Figure 1: A draw of the full SPD

A unique feature of the SPD is that it can provide a prompt multiplicity trigger within the latency of the L0 trigger (850ns) [8]. The LV power supply requirements for the front-end electronics on each half-stave (HS) are 1.85V ($\sim 6A$) for the pixel bus and 2.6V ($\sim 0.5A$) for the MCM. The LV power supply (PS) system is based on 20 CAEN A3009 LV modules (12 LV channels each), housed in 4 CAEN Easy3000 crates located in the experimental area. Detector bias (50 $\div$ 100 V, $< 7\mu A$) is provided by 10 CAEN A1519 HV modules (12 HV channels each) housed in a CAEN SY1527 mainframe located in the counting room. The SY1527 communicate with the software layer via ethernet (TCP/IP). The SY1527 communication with the LV modules is via CAEN A1676 branch controller.
The FE electronics power dissipation is $\sim 1.3kW$. Cooling is based on an evaporative system with C_4F_{10}. The cooling plant provides one main cooling line for each SPD sector. Each line feeds 6 cooling capillaries, embedded in each sector, to which the staves are thermally coupled by means of thermal grease. The operating temperature of the detector is $\sim 25^oC$. The cool-

ing plant is controlled by a PLC. Communication with the control PC is via ethernet (TCP/IP) using OPC Server-client protocol. Efficient cooling is vital for this very low mass detector. If the cooling were suddenly switched off, the detector temperature would increase at a rate of 1 $^oC/s$. The detector temperature is therefore a critical parameter that must be monitored online and safety interlocks must be activated immediately. On each HS surface are mounted two series of 5 temperature sensors (Pt1000). One group of Pt1000 series (120) are read out via analog modules in a dedicated PLC that generates the corresponding temperature interlocks and sends online via ethernet the detector temperatures readout to the counting room.

III. Detector operation issues

The operation and performance of the SPD require a tight control of many parameters such as timing, the pixel bus power supply voltage Vdd, the reference voltages provided by an analog ASIC on the MCM (Analog Pilot [2]), and the settings of the various DACs in each front-end pixel ASICs. The objective of the SPD calibration is to adjust these parameters in order to obtain the highest efficiency and response uniformity of the pixels matrices. Dead and noisy pixel identification is performed as well during the calibration phase.
Calibration is mainly performed using test pulses (TP) that can be generated in each FE chip. The pulses can be set independently to each single pixel; the amplitude is programmable and is controlled by the Analog Pilot. The detector efficiency and the uniformity of response of the pixels matrices are studied by varying the pulse amplitude at various threshold settings (S-curves)[6].
The list of the noisy and dead channels is important for the offline particle tracks reconstruction.
As previously pointed out, the SPD has the capability to provide a prompt multiplicity trigger. This is the Fast-OR pulse that is generated in each pixel chip when a particle hit is detected. The Fast-OR contributes to the L0 trigger input to the ALICE Central Trigger Processor (CTP). Several calibration procedures are implemented using the TP and eventually the interactions:

a) Uniformity scan: a sequence of TPs is applied to each pixel with an amplitude $>$ 2 Mean Threshold of the chip. The uniformity of the response of the pixel matrix is determined from the efficiency distribution (ratio of hits to pulses).

b) DAC scan: a sequence of triggers is applied to the detector under test, using TPs or a radioactive source, while varying the references generated by the Analog Pilot and/or the DACs in the pixel chip. For each DAC value, the average efficiency of response and the average multiplicity are determined.

c) Mean threshold scan: the uniformity of the pixel matrix is studied by varying the TP amplitude. For each pixel, the efficiency of response is determined as a function of the DAC setting. The TP amplitude that gives an efficiency of 50 % represents the equivalent in voltage of the applied threshold.

d) Noisy and dead pixels identification.

e) Fast-Or characterization: a sequence of TPs is applied to one pixel at a time. The efficiency map of the pixel matrix is determined from the corresponding number of generated Fast-ORs

Automated configuration calibration procedures are implemented in the Detector Control System that is also able to emulate the ALICE DAQ and trigger system.
The calibration raw data from the 1200 FE chips are analyzed online either by the DCS or by the DAQ system. The calibration sequence is iterated until the optimal parameter settings are determined. These settings, including FE chip DACs values, MCM chips configuration and power supplies voltages, are stored in an Oracle based configuration database. The configuration versions are tagged in function of the run (PHYSICS p-p, PHYSICS Pb-Pb, CALIBRATION, BEAM TUNING) for witch they will be applied.

IV. Control System

The system is based on a commercial Supervisory Control And Data Acquisition (SCADA) named PVSS. Five PVSS projects are running independently on different working nodes to control, respectively the cooling system, the Power Supply (PS) system, the interlock and monitor system and the FE electronics; the fifth project links together and monitors the 4 subsystem projects. In the future it is planned to integrate the control of the Pixel Trigger electronics in the SDP DCS as well. A block diagram that represent the HW/SW interconnection is shown in fig.2.

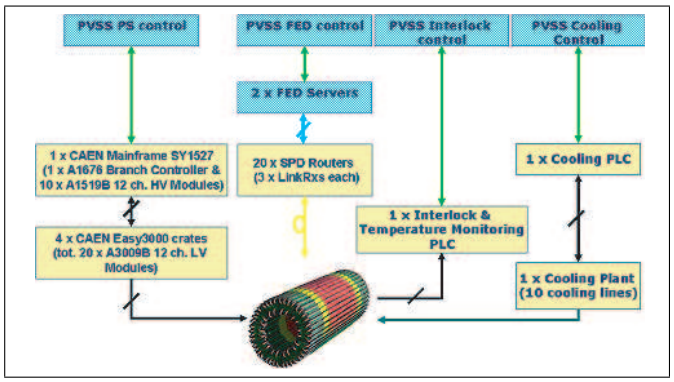

Figure 2: Block diagram that shows the SPD branches of the detector control system

Each main hardware branch is connected directly to an independent PVSS project that bridges the hardware with the logical control of the full system carried out through a Finite State Machine (FSM). The FSM is based on a State Management Interface (SMI++) capable of defining logical domains and links the different SPD sub-systems. The lowest FSM software layer is formed by Device Units (DU) providing the upper layers with an hardware state. The DUs are capable of sending instructions to the PVSS layer connected to them as child. The DU can be connected together either via Logical Units (LU) or via Control Units (CU) that generate states as functions of their children state. The LU and CU are sending commands to the underlying level on the FSM hierarchy. The CU and its children form a domain and can run autonomously on a different computer but the CU has higher RAM requirements (5 MB/DU) than a LU. The SPD FSM hierarchy is shown in fig.3.

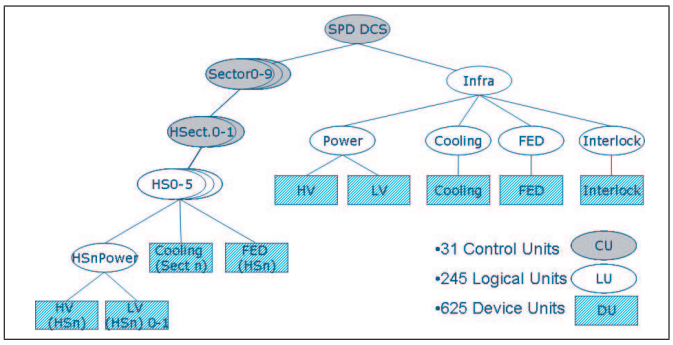

Figure 3: The SPD Finite State Machine hierarchy blocks diagram

The system comprises 31 CUs to place the detector partitioning at the half-sector level. This structure allows to debug a detector subset without interfering with the normal data taking. The SPD FSM contains 245 LUs and 625 DUs. The *SPD* node has 11 branches: one for the infrastructure and one for each sector. The children of the *Infra* LU are the DUs representing the status of the subsystem infrastructures. They are PS mainframe, crates, cooling plant etc. The READY state of the *Infra* is foreseen only when all the subsystem infrastructures are fully operative. If the *Infra* LU is not in ready status the SPD DCS top node sends the switch-off command to all the detector subsystems.
Each sector CU is partitioned in 2 half-sectors CU including 5 HS LUs. The HS LU retrieve information from the cooling system and switch off the power supplies in case of anomalies.
The HV and LV DUs are linked together via a LU (*HSnPower*) that provides the proper HS power-up and power-down sequence.
A set of macroinstructions is provided by the HS LU to the FE control DU that can execute monitoring, control and detector calibration. The SPD is ready for physics or for calibration when the on-detector and off-detector electronics is configured. Different sets of configuration parameters are making the switch between different SPD status such as i.e. calibration and physics.

Each PVSS software layer contains translator scripts capable of converting macroinstructions into the sequence of operations required for the hardware.
Background scripts monitor continuously the status of the hardware and take automatic actions to protect the system in case of abnormal states.
The PVSS layer controlling the PS system allows to upload the prescribed voltage settings in the SY1527 mainframe. The parameters are retrieved from a specific Oracle Configuration Db (CDB). All the voltages and currents are monitored online and archived during all the detector operation phases. An HS power-up and power-down sequence is foreseen to activate or deactivate sequentially MCM, detector bias (HV) and FE chips. The sequence is controlled via the FSM and PVSS background scripts are used for monitoring the status and taking corrective actions if necessary.

The FED DUs control two Front End Device (FED) Servers (C++ based), one for the detector side A and one for side C.

The FED Server is a stand alone application consisting of three software layer. The top one hosts a Distributed Information Management System (DIM - TCP/IP) server that allows the communication with the PVSS layer. The intermediate FED application layer hosts all the logical functions required. It retrieves the commands received by the DIM server, checks the hardware status, pulls or stores, if required, the data from/to the database and communicates with the driver layer to apply the required operations to the hardware. The FED state machine is hosts in this layer. The bottom software layer is the driver for the VME access of the off-detector electronics.

The system structure allows fast remote operator intervention and is highly modular. The communication between the different software applications is via DIM. Most processes are fully automated in order to obtain the required reliability and safety of operation.
The power system (HV and LV) and the cooling systems are controlled directly by PVSS.
The FSM represents also the operator interface to the detector and allows the interconnection with the general ALICE DCS.

V. Calibration Procedures

The system is designed to allow fast and automated calibration procedures. The calibration of the full detector will be carried out during the LHC fill time ($\sim$ 70 mins); the updated configuration settings are calculated automatically.
Two calibration procedures can operate independently: DCS_ONLY and DAQ_ACTIVE. The DCS_ONLY procedure requires the emulation of the alice DAQ and trigger system by the DCS system. It is slower then the DAQ_ACTIVE during the data acquisition but allows the calibration and debug of a detector subset without interfering with the data taking of the other detector partitions.
The block diagram of the DCS_ONLY procedure is displayed in fig.4.

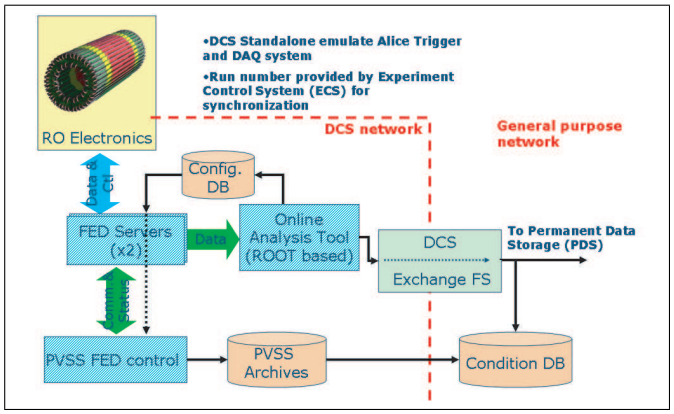

Figure 4: A block diagram of the DCS_ONLY calibration procedure

The routers data spy capability are enabled in this procedure and the main detector data stream is forwarded to an internal router dual port memory accessible via VME bus. The PVSS and the FED servers perform the detector configuration and status monitor. The routers then send triggers and data are

read back via VME by the FED servers acting as software data buffer. The detector data are sent to a ROOT based analysis tool. The tool defines the updated configuration and stores it in the CDB. The analysis results are stored in ROOT format files and forwarded to an Exchange File System (EFS) that allows the communication with the offline network and the Permanent Data Storage (PDS). The analysis tool is controlled and retrieves the configuration parameters needed for the data analysis by PVSS. The communication between the 3 software tools such as PVSS, FED servers and Analysis Tool is performed via DIM. When he calibration is completed the DCS moves automatically the FSM from the calibration state to a standby state. The ECS is the user interface to the detector in operation. The ECS controls the SPD subsystems such as DAQ, DCS and Trigger. In the DCS_ONLY calibration procedure, the ECS sends the calibration start command to the DCS and disables the other two subsystems. A new run can be started only when the DCS leaves its calibration state.

The DAQ_ACTIVE calibration procedure requires the DCS, DAQ and Trigger systems to be all active. A block diagram of this procedure is displayed in fig.5.

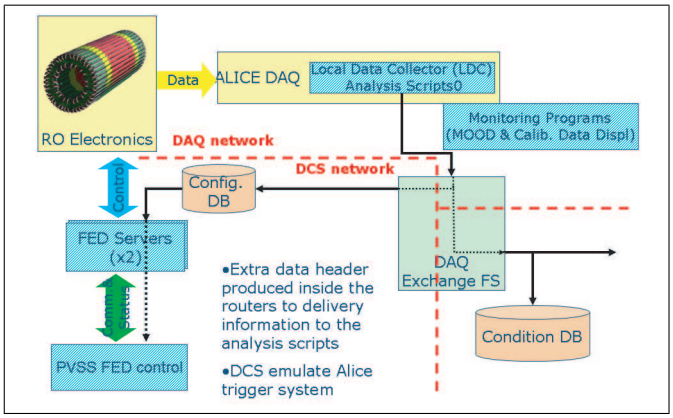

Figure 5: A block diagram of the DCS_ACTIVE calibration procedure

In this configuration the ECS issues the calibration start command to the different subsystem and waits for confirmation of detection configuration execution by the DCS. Depending on the required calibration mode either the Trigger system or the routers generate the readout sequences. The data are recorded in the DAQ Local Data Collectors (LDC). When the calibration procedure is completed, the ECS starts a set of LDC preprocessing scripts. These scripts analyze the raw data and generate ROOT files with the distributions of the hits detected on the pixel matrices (hit-maps). The files are forwarded automatically to a second level of processing that extracts the parameters needed for the reconfiguration of the detector. The processed and pre-processed data files are sent to the EFS that forwards them to the PDS, the CDB and the condition database used for track reconstruction. When this sequence of operations is completed the ECS closes the run and the system is placed in a standby condition.

The calibration procedure start and the SPD subsystems configuration request is performed by the ECS. The two calibration procedures have been implemented in the system test facility at CERN and are used for the SPD sector characterization. The DAQ_ACTIVE procedure allows the fast calibration of the full detector using the parallel data readout functionality.

VI. Safety Interlocks

Efficient cooling is vital for this very low mass detector. In the case of a cooling failure, the detector temperature would increase at a rate of 1 $^oC/s$. The detector temperature is therefore a critical parameter that must be monitored online and requires the immediate activation of a safety interlock if necessary. The maximum temperature allowed for the detector is 40 ^oC and the interlock threshold is set at 35^oC. Four levels of hardware interlocks and two levels of software interlocks are foreseen. In fig.6 is displayed the hardware interlock block diagram.

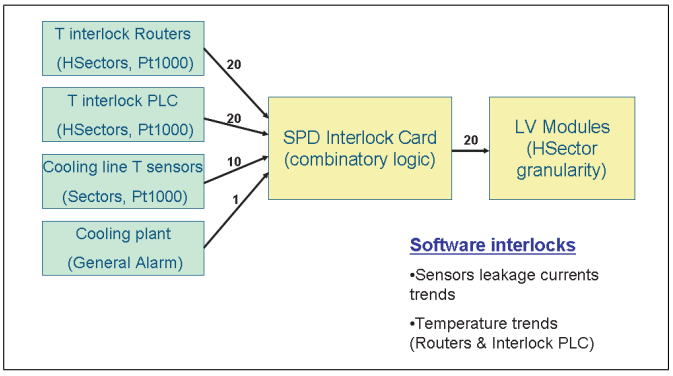

Figure 6: A block diagram of the SPD interlock interconnections

Each HS is equipped with 2 independent series of 5 temperature sensors (Pt1000) each. One of the series is readout by the Analog Pilot on the MCM and the data are encoded in the readout data stream. The Routers read the temperature values and assert the interlocks if needed. The other serie is hardwired out of the detector and read out in a dedicated PLC. The PLC scans the 120 chains in less than 1s. The hardwire interlock lines are processed in a card with SEU mitigation circuitry that provides direct safety interlock lines to the 20 LV power modules (one each half-sector). The temperature readouts are also sent online to the counting room via an ethernet link.
On the ten cooling lines have been placed temperature sensors read back via the temperature monitor PLC. The PLC and the Routers continuously monitor temperature trends and assert preventive interlocks if malfunctions are observed. The detector bias current roughly double each increase of temperature of 8^oC. The PVSS controlling the power supply system monitors constantly the sensor bias currents and in case of dangerous trends it switches off the corresponding HS.
A set of PVSS scripts run in the background to provide the proper overall power-down sequence in case of a part of the system is switched off by an hardware interlock.

VII. SPD INTEGRATION AND COMMISSIONING

The final test, integration and commissioning of the SPD is carried out in a dedicated area inside the Divisional Silicon Facility (DSF) at CERN. The area is equipped with the final cooling plant, power supply system, readout electronics and control system including temperature monitoring and safety interlocks. The DAQ system is a subset of the ALICE general one but with all the functionality. The trigger system is the final SPD partition.
The main objective is to test and commission the full detector with all the final systems and services before installation in the experimental area. Two FED servers are implemented and operational. Three working nodes are used to run the FSM, the DCS data analysis tools and the PLC for temperature monitoring and safety interlock.
The sectors are characterized in DSF and the configuration parameters retrieved using the tools described above are stored in the CDB in order to be used during ALICE startup.
At the time of writing 6 sectors are under test and the mechanical integration of the first half-barrel is starting.

VIII. SUMMARY

The SPD control system has been developed and it is used for the test, integration and commissioning of the sectors and the half-barrels, in conjunction with the final detector readout electronics and services in the dedicated area in the CERN DSF. The integration with the ALICE DCS and DAQ is nearing completion. The detector FSM prototype is operational and it has been integrated in the ECS.
The calibration procedures have been developed and implemented in the system test. Measured performance matches the challenging requirements as reported.

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The Level 0 Pixel Trigger System for the ALICE experiment

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Abstract

The ALICE Silicon Pixel Detector contains 1200 readout chips. Fast-OR signals indicate the presence of at least one hit in the 8192 pixel matrix of each chip. The 1200 bits are transmitted every 100 ns on 120 data readout optical links using the G-Link protocol. The Pixel Trigger System extracts and processes them to deliver an input signal to the Level 0 trigger processor targeting a latency of 800 ns. The system is modular and based on FPGA devices. The architecture allows the user to define and implement various trigger algorithms. The system uses advanced 12-channel parallel optical fiber modules operating at 1310 nm as optical receivers. Multi-channel G-Link receivers were realized in programmable hardware and tested. The design of the system and the progress of the ALICE Pixel Trigger project are described in this paper.

I. Introduction

ALICE is an experiment designed to study the physics of strongly interacting matter and the properties of quark gluon plasma in the collisions between heavy ions nuclei at the Large Hadron Collider (LHC) at CERN [1]. The ALICE apparatus allows particle identification over a broad momentum range, powerful tracking with good resolution from 100 MeV/c to 100 GeV/c and excellent determination of secondary vertices. These features allow important contributions also to the physics of proton-proton interactions. The low material budget and the moderate magnetic field make the apparatus suited for studying low transverse momentum phenomena in proton-proton collisions.

The ALICE Silicon Pixel Detector (SPD) is the innermost detector of the Inner Tracking System of the ALICE apparatus [2]. It is shown in Fig. 1. The SPD is a double layer barrel pixel detector. It is constituted of 120 half staves, 40 in the inner layer and 80 in the outer one. One half stave comprises two 200 μm thick silicon pixel sensors. Each sensor has a matrix of 160×256 pixels of 425×50 μm^2. A sensor is bump bonded to 5 mixed signal readout chips realized in 0.25 μm CMOS technology. The linear array of 10 pixel chips in each half stave is read out via a Multi Chip Module (MCM) [3]. This includes the Analog Pilot chip for biasing, the Digital Pilot Chip for readout and communication, the GOL chip [4], optical PIN receivers and a laser diode transmitter. Timing and commands are received from the control room on two 40 Mb/s serial links. Data are transmitted on an optical link with a wavelength of 1310 nm using the G-Link protocol [5] at a signaling rate of 800 Mb/s. The readout of the data is initiated at the reception of a Level 2 trigger signal. Hit data are stored in the readout chips memory until a positive or negative Level 2 command is received. The readout and control electronics [6] includes 60 Link Receiver boards connected as mezzanine cards on 20 Router boards.

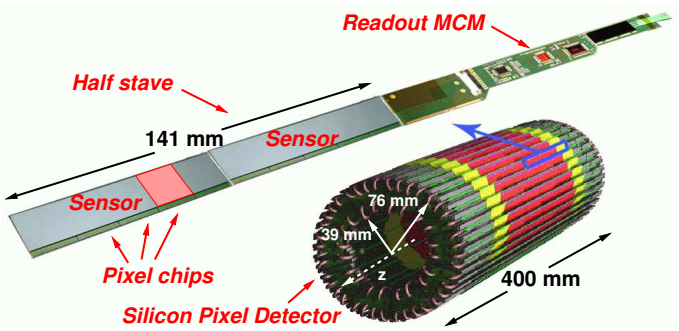

Figure 1: The Silicon Pixel Detector and a detailed view of one of its 120 half staves. The positions on the half stave of the sensors, of the pixel chips and of the readout Multi Chip Module (MCM) are indicated.

The 1200 readout chips of the SPD feature a Fast-OR output signal. This digital output is active whenever at least one of the 8192 channels of the chip records a hit. This information is not stored in the on detector memory. The 10 Fast-OR bits of each half stave are continuously transmitted by the MCM every 100 ns on the output optical link. They are transmitted using the user field of the G-Link control words. The Fast-OR signals allow the SPD to be operated as a low latency and low granularity pad detector, with an equivalent pad size of ∼13×13 mm^2.

The 1200 Fast-OR signals will be used to generate an input signal for the Level 0 trigger decision in the ALICE Central Trigger Processor (CTP). Various trigger algorithms taking into account the Fast-OR data have been investigated [7], including topology based and occupancy based ones. These studies have shown that event selection in heavy ions runs and background rejection in proton-proton interactions can be significantly improved using the Fast-OR data. The different algorithms can be implemented as combinational logic functions of the 1200 Fast-OR signals. This naturally suggests an implementation of the algorithm on a programmable hardware device.

The Pixel Trigger System for the ALICE experiment is required to extract and process the 1200 Fast-OR signals in order to provide a signal input to the Level 0 trigger decision in the CTP. Various user selectable processing algorithms shall be supported by the hardware platform. The overall time latency of the process is required to be less than 800 ns from the interaction to the input to the CTP. This requires the system to be located as close as possible to the detector and the CTP. A limited space of one standard crate could be allocated in the electronic racks next to the CTP.

II. System Architecture

The architecture of the Pixel Trigger System is shown in Fig. 2. The 120 optical fibers outgoing from the detector are connected to the inputs of a commercial passive optical splitter located in the rack next to the CTP. The splitter output fibers forward the data to the readout electronics in the control room at about 110 m from the ALICE apparatus and to the electronic boards of the Pixel Trigger system, located in the same rack of the splitter. The data readout path is not affected by the Pixel Trigger System and remains fully independent from it.

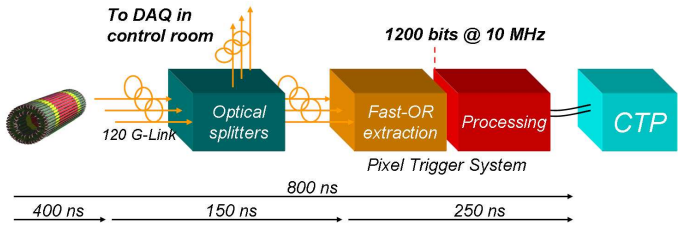

Figure 2: The architecture of the Pixel Trigger system.

The electronic system is subdivided in two subsystems. The first one deserializes the optical data and extracts the 1200 Fast-OR bits from the data flow. It is made up of a set of electronic boards with optical receivers and FPGAs. The second block implements the processing algorithm on the 1200 input bits and generates the output signal for the CTP. It is constituted of one electronic board based on a FPGA with a large number of pins and large logic space. The former architecture is naturally suggested by the need of providing all the 1200 Fast-OR bits as simultaneous inputs to the processing unit.

The overall latency budget of 800 ns can be subdivided among each of the processes along the data flow. The on-detector electronics takes 400 ns from the collision to transmit the Fast-OR bits. The optical fibers path length from the detector to the location of the system is ∼30 m. This implies a signal propagation delay of ∼150 ns. Therefore only 250 ns can be allocated to the deserialization, extraction and processing phases.

The algorithm to process the 1200 Fast-OR bits will be implemented in programmable hardware to allow fast execution, upgrading and reconfiguration by the user. The implementation on a large FPGA of some of the proposed trigger algorithms has been completed. The behavioral simulations showed that even the most complex function could be processed in less than 15 ns in a Xilinx Virtex 4 device. The critical delays in the system are therefore associated with the Fast-OR data deserialization, extraction and transfer between the peripheral FPGAs and the processing unit.

III. Development, Design and Status

Advanced optical receivers were chosen for the optical receiver cards after a qualification procedure. FPGA based solutions for the G-Link deserialization were also investigated. These development activities were motivated by the need of realizing the optical receiver cards as compact as possible. Some outcomes of these investigations are discussed in the following two subsections. The detailed description of the design is given after those.

A. Optical receiver module

Parallel optical fiber modules integrate an array of photodiodes and a receiver chip in a single device. Independent amplifying channels are realized on the chip. These devices allow for a significant reduction of the space required for the optical receivers section in a communication board. However devices operating at 1310 nm are not easily available on the market at the present time. Engineering samples of parallel optical fiber modules operating at 1310 nm were provided to our group by a private company[1]. They are customized versions of commercial devices operating at 850 nm. A photograph of the device is shown in Fig. 3. It features a 12 position MPO/MTP connector on the optical input side. A 100 pin MEG-Array[2] board-to-board connector allows the component to be plugged on the host board.

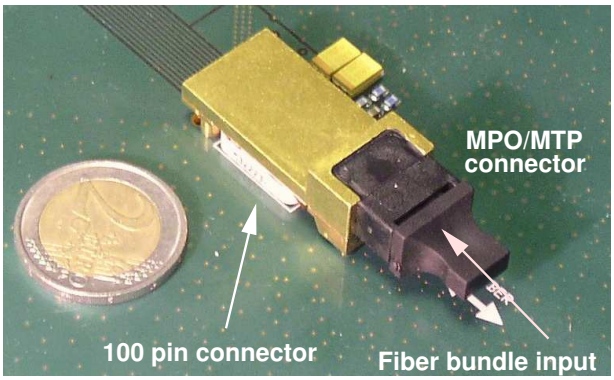

Figure 3: The Zarlink 12-channel Parallel Optical Fiber Module operating at 1310 nm. It features a male MPO/MTP fiber bundle connector on the optical input side and a 100 pin MEG-Array® electrical connector on the host circuit side.

The performance of the two samples was experimentally evaluated with respect to sensitivity, bandwidth, overall jitter and transmission error rate. For these measurements an optical communication setup [8][9] was used. The transmitter side included a pattern generator, the GOL radiation hard serializer and laser driver and a laser diode. The Zarlink optical module was used at the receiver side and its outputs could be connected to an oscilloscope or to a deserializer/receiver ASIC[3].

All the channels of the Zarlink receivers were operational with input optical power as low as -18 dBm. The module specified bandwidth is 2.7 Gb/s. The contribution of the optical module to the overall jitter of the communication chain was measured by the eye diagrams. A value of $\sim$ 25 ps was obtained at -15 dBm. The rate of frame (20 bit word) errors in the transmission was measured at various optical power levels. For

[1]Zarlink Semiconductor, `www.zarlink.com`.
[2]MEG-Array®is a registered trademark by FCI, `www.fciconnect.com`.
[3]Texas Instrument TLK1501.

these measurements the GOL was configured to transmit using the 8B/10B protocol. A Frame Error Rate below 10^{-14} with -18 dBm of input optical modulation amplitude was measured. This figure allowed an estimation of a bit error rate lower than 5×10^{-16} at -18 dBm. The engineering samples satisfied and even exceeded the specifications for the Pixel Trigger receiver cards. The Zarlink parallel optical fiber module was therefore chosen to be used for the Pixel Trigger system.

B. G-Link deserialization

The serial data stream has to be deserialized and frame aligned to allow tapping the Fast-OR bits out of the data flow. The on-detector electronics transmits data formatted according to the G-Link protocol. This protocol is fully supported by the GOL ASIC. However few products supporting the G-Link protocol can be found on the market. Agilent manufactures a single channel G-Link receiver ASIC (HDMP-1034).

Latest generation of FPGAs feature modules for serial communication up to few Gb/s. These modules include serializer/deserializers, comma alignment blocks, protocol decoders and are typically implemented in dedicated circuitry on the FPGA chip[4]. The implementation of a multi-channel G-Link deserializer/receiver on Xilinx and Altera FPGAs with fast serial circuitry was therefore investigated.

A simple parallel 12-channel G-Link receiver was implemented in HDL. It was possible and straightforward to verify by behavioral simulation its implementation both on a Xilinx Virtex 2 with Rocket I/O X and on an Altera Stratix GX. A real working circuit was implemented in hardware using a parallel optical receiver board based on an Altera Stratix GX and developed at CERN [10] by the group of the ECAL (electromagnetic calorimeter) detector of the CMS (Compact Muon Solenoid) experiment. To our knowledge this was the first working implementation of a parallel multi-channel G-Link receiver on programmable hardware.

Device	Latency [ns]		
	Data sheet	Simulated	Measured
Agilent HDMP-1034	88	n.a.	87±7
Altera Stratix GX[1]	n.a.	190	190±5
Altera Stratix GX[2]	n.a.	130	n.a.
Virtex II Rocket IO X[3]	475	475	n.a.
Virtex II Rocket IO X[4]	275	n.a.	n.a.

Table 1: Latencies of alternative solutions investigated for the 800 Mb/s G-Link deserializers/receivers. The Agilent HDMP-1034 is a single channel dedicated ASIC. The remaining four solutions are multi-channel receivers implemented on FPGAs. [1]Fully operational hardware implementation, 20 bit word length, 40 MHz clock. [2]Behavioral simulation, 10 bit word length, 80 MHz clock. [3] Simulation and data sheet, 20 bit word length, 40 MHz clock. [4] Data sheet, 10 bit word length, 80 MHz clock.

The latencies of alternative G-Link receivers were determined and are listed in Table 1. The latencies of the FPGA based circuits were significantly higher than the one offered by the HDMP-1034 ASIC. This was due to the lack of the possibility to bypass several functional blocks of the dedicated modules of the FPGAs, even if they were not actually used. Some examples are the comma alignment module and the 8B/10B decoder. Several clock periods were therefore wasted in the data path of the FPGAs high speed modules. The latency constraint on our application is not compatible with the performances obtainable with the FPGA based circuits. Therefore the HDMP-1034 was chosen for the receiver cards of the Pixel Trigger system.

C. Design and status

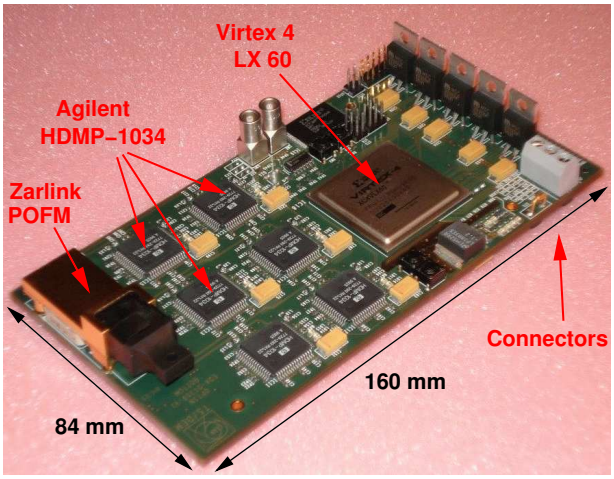

Figure 4: The prototype OPTIN electronic board. The Zarlink Parallel Optical Fiber Module, six Agilent HDMP-1034 chips and the Xilinx Virtex 4 FPGA are shown. Six more HDMP-1034 chips and the Compact PCI connectors are on the other side of the board.

The choice of the optical receiver modules and of the HDMP-1034 ASIC determined the architecture of the optical receiver electronic boards (OPTIN boards). The OPTIN board has been designed and the first prototype produced. It is shown in Fig. 4. It is realized on a 12 layer printed circuit board. It has four connectors compatible with the IEEE 1386 Common Mezzanine Card standard. However, the board is larger than the envelope specified in the standard. Its dimensions are 160×84 mm^2. The assignment of the connector pins are compatible with the Compact PCI specification.

Each OPTIN board acts as a Fast-OR extractor for 12 optical channels incoming from the on detector modules via the splitter. One Zarlink optical module receiver converts and amplifies the signals received on the incoming fiber bundle. Twelve HDMP-1034 deserialize and realign the data streams. A Xilinx Virtex 4 LX60 FPGA receives the parallel outputs of the deserializers and extracts the 120 Fast-OR bits received every 100 ns. They are transmitted on a dedicated parallel output bus. Ten OPTIN boards are needed in total for the full system. They operate, as the rest of the system, at the LHC clock frequency of 40.0786 MHz. The estimated power consumption of the OPTIN board is 12 W. A large fraction of this power, up to 8 W, is needed by the twelve HDMP-1034 chips.

The processing board (BRAIN) is a 9U size (400×360 mm^2) electronic board. It is shown in Fig. 5. Most of the board area is

[4]Both Altera and Xilinx implemented these featured in their latest Stratix and Virtex FPGAs.

reserved to connect the 10 OPTIN boards as mezzanine cards, 5 per each side of the processing board. This interconnection solution is made possible by the compact design of the OPTIN board. A similar approach has already been used for the SPD data readout electronics. The routing of the signals between the boards is thus simplified, avoiding the need of a backplane or wired interconnections.

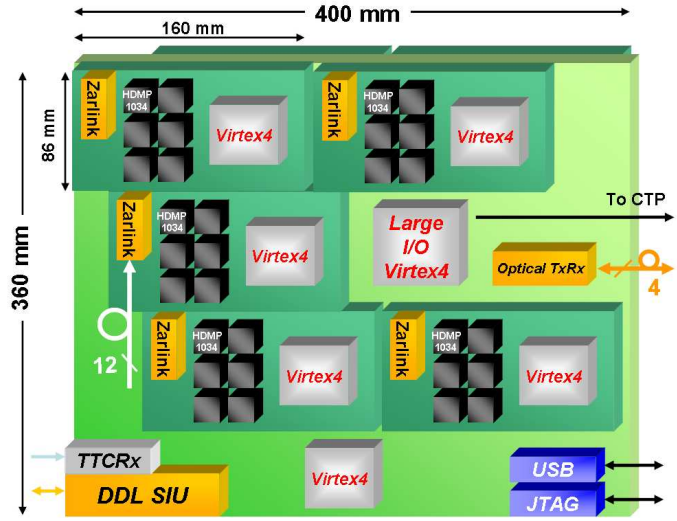

Figure 5: Schematic view of the BRAIN processing board with the OPTIN boards plugged as mezzanine cards. Five OPTIN cards are located on each side of the processing board. The processing and the control FPGAs are in evidence. The diagram also shows the interfaces of the system.

A processing FPGA is the core of the BRAIN board. A large I/O space device, a Xilinx Virtex 4 LX100 with 1513 pins, has been chosen as the processing device because of the large number of parallel lines needed to receive the Fast-OR bits from the OPTIN boards with a minimum latency. The Fast-OR bits are transferred at Double Data Rate (80.16 MHz) on dedicated signal lines. There are 64 Fast-OR dedicated output lines on each OPTIN board. They pass through the OPTIN board connectors and reach dedicated input pins of the processing FPGA. In total 640 input pins of the processing FPGA are used for the Fast-OR parallel bus. This large degree of parallelism is needed to satisfy the constraint on latency. All these lines are routed as controlled impedance striplines. Source impedance matching is implemented using the Digitally Controlled Impedance DCI® feature of the Xilinx Virtex 4.

Several interfaces are available on the processing board. Ten main output lines (LVDS) allow the transmission of the result of the decision algorithm. The ALICE Detector Data Layer (DDL) interface [12] is the main slow control interface. USB and JTAG interfaces are available for *in situ* access and debugging. The TTCrx chip [13] is dedicated to receive the clock and timing information from the experiment Timing Trigger and Control distribution network. Auxiliary high speed serial lines and optical transceivers are available for high bandwidth communication and future upgrades. The design of the BRAIN board is finished. The layout and routing of the board is ongoing. The board shall need 12 routing layers.

The input bandwidth of the system reaches 96 Gb/s (192 Gb/s) with the input links operating at 800 Mb/s (1600 Mb/s). The total power consumption of the BRAIN board and of the 10 OPTIN boards is estimated at about 130 W. The system layout implies that this power is dissipated in a single slot of the electronic rack. The dissipated power density is high and thermal verification of the system design was required. A finite element heat flow simulation of the system was implemented at CERN using dedicated software tools [11]. Detailed thermal models of all the electronic components and of the boards of the system were considered. The geometry of the simulated system was similar to the final one. The boards were located in the partially enclosed volume of an electronic rack, with no other boards in the adjacent slots as it is foreseen for the real case. The simulation considered forced air convection. The results of the calculation are shown in Fig. 6. The hot spots in the system are the voltage regulators on the OPTIN boards. They can reach a temperature of 110 °C. The regulators must operate with a junction temperature $T_j < 125$ °C. The result of the verification was judged acceptable because worst case conditions were assumed at each step in the definition of the thermal model.

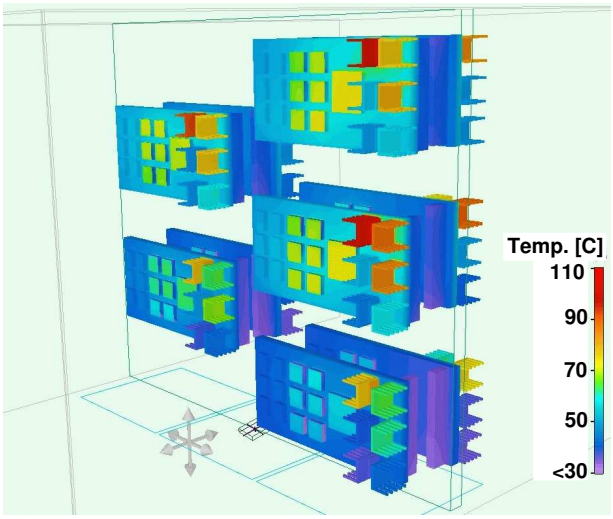

Figure 6: Color map of the temperature of the system calculated by a finite element model. The highest temperature is around 110 °C. Worst case assumptions were made for the dissipated power and the thermal resistances.

The design was checked with respect to signal integrity because of the large number of lines, the length of the interconnections and the large number of loads on shared lines. A simulation study of the critical lines was done. It included IBIS[5] models of the Virtex 4 output drivers as well as models of the signal propagation in the striplines. The signal analysis tools of the Cadence suite were used for this purpose. This study allowed for an optimization of the driving strength and switching speed of the FPGA output buffers. Signal buffering was shown to be required in some cases.

The location of the Pixel Trigger system is a radiation area

[5] I/O Buffer Information Specification, a standard to model the electrical properties of output line drivers.

with an expected neutron fluence [14] of 2.0×10^8 cm^{-2} over 10 years. The iROC report [15] gives a measurement of the number of Single Event Upsets in a similar technology (90 nm) Xilinx Spartan 3 FPGA. That measurement can be used to estimate the number of upset events in the Pixel Trigger FPGAs. This calculation results in 18 Single Event Upsets (including configuration SRAM changes) and 5 Single Event Functional Interrupts (observable at the outputs) during 10 years of operation for each of the system FPGAs.

D. Control and configuration

Full integration of the Pixel Trigger system in the ALICE Detector Control System is necessary. The main control is via the ALICE DDL interface. A second FPGA (Virtex 4 LX 40) on the processing board is dedicated to the slow control, to the system interfaces and to implement the reconfiguration of the main processing FPGA. Status monitoring and control is implemented via status and configuration registers in all the programmable devices of the system, accessed by the control FPGA via a local shared bus. Four JTAG chains are foreseen in the system. Two of them are used for two groups of 5 OPTIN boards, one is dedicated to the processing FPGA and the remaining to the control FPGA itself. JTAG players shall be implemented in the control FPGA to control the OPTIN boards and the processing FPGA chains. The processing FPGA will be reprogrammed remotely. The programming file for a given processing algorithm will be downloaded via the DDL link and the control FPGA to local SRAM memory. The control device shall then transfer the programming file to the Flash PROM connected to the processing FPGA by the JTAG players. Reconfiguration is finally launched via a JTAG command sent to the processing FPGA.

The control software shall be implemented in the ALICE PVSS framework [16]. An intermediate middleware layer (C++ library) will make the basic hardware functionalities available to the upper PVSS layer.

IV. Conclusions

The Pixel Trigger System for the ALICE experiment has been designed and is being constructed. It allows for the 1200 Fast-OR signals from the detector to be used in the Level 0 trigger algorithm in the Central Trigger Processor. The system targets the stringent latency constraint of 800 ns. It is fully independent from the existing data readout electronic chain. It allows for several algorithms to be implemented on the same programmable hardware platform. Remote configuration of the processing FPGA allows the user to change the processing algorithm at choice. The system has a modular design open to future upgrades. The system uses advanced parallel optical fiber modules operating at a wavelength of 1310 nm. Multi-channel G-Link receivers were implemented in FPGAs with dedicated fast serial communication circuitry. They could not be used for the final design because they did not satisfy the latency constraint. The ALICE experiment will be the only experiment at the LHC collider to include the silicon pixel detector in the Level 0 trigger decision from startup.

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Parallel Session B5
Power systems

Quality assurance for CMS Tracker LV and HV Power Supplies

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Abstract

This work describes the quality assurance measurements that have been carried out on about 2000 Power Supply Units produced in CAEN technology for the CMS Silicon Tracker Detector. The automate procedure and the characteristics of the dedicated Test Fixture developed for this activity are described in details. Magnetic field tolerance and radiation hardness of Tracker power supply units is also discussed at length.

I. INTRODUCTION

The CMS Tracker Power system is made out of about 2000 complex units (PSU) able to provide, independently, 2 low voltage lines to the front-end electronics and 2 HV lines for the silicon strip detector bias. A Power Supply Module, commercially labelled CAEN A4601H, is made out of two PSUs and contains then 4 LV and 4 HV channels.

The specific ranges for LV and HV channels are listed in Table 1

Table 1: PSU channels nominal values

PSU Channel	Voltage	Current
LV0	2.5 V	0 – 13 A
LV1	1.25 V	0 - 6 A
HV0	0 – 600 V	0 – 10 mA
HV1	0 – 600 V	0 – 10 mA

They consist of :

- 2.5V and 1.25V regulators:
  - I2.5 max = 13 A ; I1.25 max = 6 A
  - Remote sensing to compensate up to 4V drop on each line:
    V2.5 max= 6.5 V, V1.25 max= 5.25 V
  - noise: Vpp (20 MHz bw) ≤ 10 mVpp
  - Efficiency: ε>70% at 90% of the maximum power.
- 2 independet HV regulators:
  - 0 - 600 V
  - IMAX = 10mA /ch
  - noise: Vpp (20 MHz bw) ≤ 30 mVpp
- Current limiters and trip procedure
- LV comparators: hardware Over Voltage protection
- Isolation: ZCM > 50 Ω at 5 MHz
- external alarms: Interlocks, Reset and mains faults

The A4601Hs will be placed underground close to the detectors, in an area where relevant fluxes of charge and neutral particles and not negligible residual magnetic field are expected.

The radiation levels foreseen in the underground area for the CMS experiment are described in detail in [1] and they strongly depend on the particular location where the device will be placed. At the A4601H's location (R =10m, z=0-6m), we expect to integrate in 10 years, running at nominal LHC luminosity, a neutron flux of 0.3×10^{10} n/cm^2 (E_n>20MeV) Charge particle contribution is lower by 2 orders of magnitude, resulting in an integrated dose of only 0.40 Gy over the same running period..

The magnetic field at the PSU location in the cavern is expected to be around 400 Gauss [2]: to have same safety margin the A4601H have been designed to have less than 10% reduction in efficiency at 1kGauss .

II. TEST FIXTURE FOR CAEN A4601H QUALITY CONTROL

In order to provide an efficient and stable quality control procedure during the production of A4601H and taking into account the large number of boards to be tested, a joint project between INFN Torino and CAEN spa developed a dedicated low noise, electrically floating test fixture module able to check the PSU specifications listed above in an automate way. The goal of the project was to provide a measurement device capable to condition each single channel of the PSU at different working points and measure its performances. Moreover, the device should allow to verify that the PSU channels follow sequences of operations causing

a transition to a defined status like ITrip, Overcurrent, Overvoltage, etc., with a simultaneous cross-check of the slow control system reaction.

The Test Fixture, as shown in Fig.1, has 4 independent channels covering the PSU modularity: 2 channels dedicated to LV lines and 2 channel for HV lines. Each channel has its own microcontroller (ST10F269) with embedded ADC's and high performance 40MHz CPU with DSP function.



Figure 1: The Test Fixture developed by Torino-INFN and CAEN for the quality control on A4601H production

The experimental setup used in the measurement is shown in Figure 2: it consists of an EASY crate capable to host up to 9 A4601H, connected to the Main Controller SY2527.

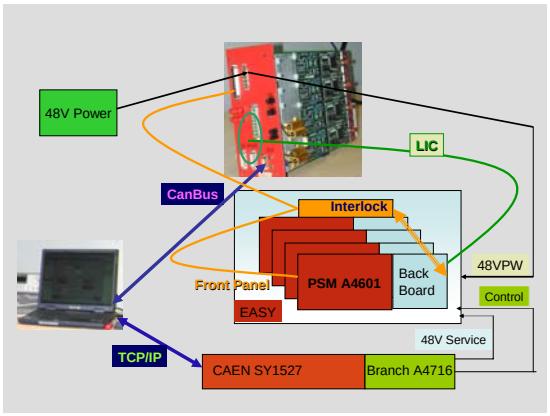


Figure 2: Quality control measuring setup

The SY2527 is a slow control system that allows to monitor PSM's current and voltage values and channel status with a refresh time of 1 s.

The output of the A4601H is connected via the CMS Low Inductance Cable (LIC) [3] to the test fixture loads that simulates the detector.

Two independent 48 V lines are present: the first one is the so called "48 V Power", that provide the power input to the PSMs and is monitored by the test fixture, the second one is the "48 V Service" that is used to maintain communication between the Control System and the Easy Crate in any condition even when the main power is off.

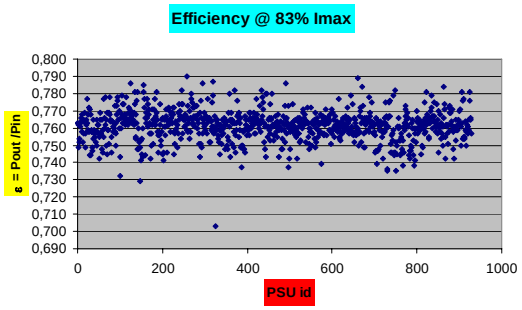
A PC communicates in parallel with the Test Fixture and with the SY2527 controller: this allows to change the PSM working point by terminating it to different resistive loads, to measure the reaction of the power supply with the Test Fixture and to compare it with the SY2527 response.

The development of such Test Fixture started in summer 2004 and was commissioned during spring 2005 using the production pre-series. Three of these experimental setups have been running since may 2005 without breaks both at CAEN directly on the production lines and in Torino for the quality acceptance validation.

III. MEASUREMENTS AND RESULTS

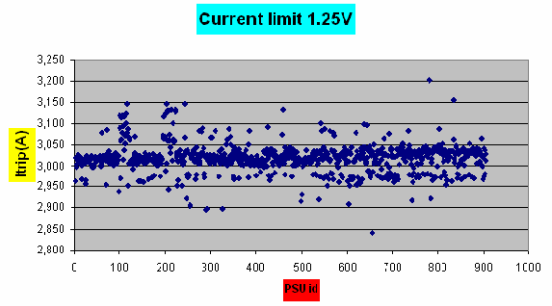
The quality assurance protocol consists of the following steps:

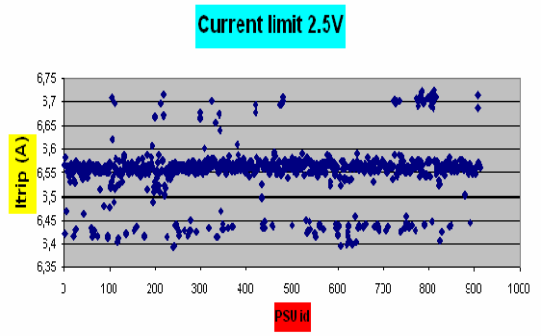
1. Switch on procedure: after a global clear alarm all channels should reach nominal voltage values at 25% of maximum current. Communication between Main Controller and the PSM should run properly.
2. Efficiency: by measuring the 48 V power input the system calculates the ratio ε=Pout/Pin as (Vcon *Imon) / (48Vmon*48Imon) where Vcon is the voltage output at the connector monitored by the SY2527 while Imon is the current measured at the load with the test fixture. A PSM is rejected if ε is less than 0.7 at 83% of maximum deliverable power. As can be seen in the following picture CAEN PSU's efficiency is always above the experimental cut.



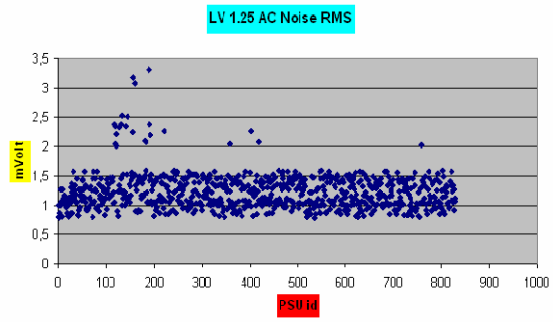
3. Power delivery tolerance: LV and HV channels should deliver nominal voltage values over the full power range with a tolerable variation of 5%. Three points at 5%, 50% and 95% of maximum current are chosen to verify this item for LV channels, while for HV ones two different reference voltages (400 V and 600 V) are tried. This test allows also to implicit check the sense compensation of 4V drop on the cable lines.
4. Current limit: each channel should not stay in a over current status more than set time (500 ms). After that it should turn off following a Trip procedure: a LV Trip switch off the entire PSU while a HV Trip switch off that specific channel only. The implemented test verify this protocol

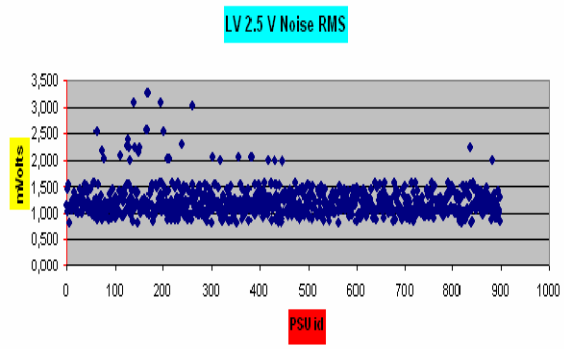
choosing as the working Iset the 50% of maximum current deliverable by the channel under test and also measure the Itrip value to be compatible within ±5% with the Iset value. In the following pictures the Itrip value is shown respectively for the 1.25V channel (Iset= 3 A) and for the 2.5V channel (Iset = 6.5A). The trip intervention is always in the wanted 5% limit.



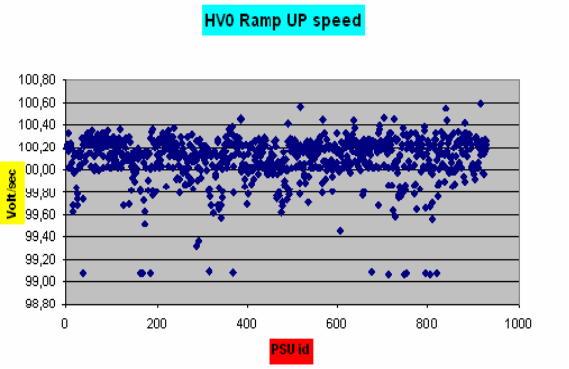


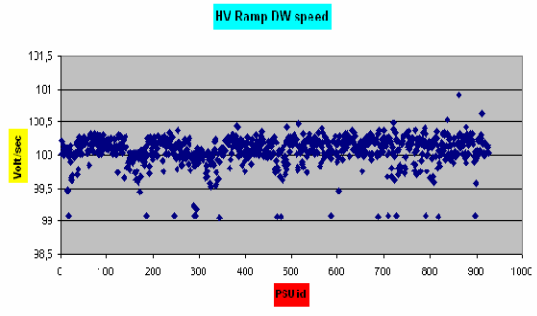
5. Transient load: by simultaneously commuting (10 ns commute time) finite resistive loads on both LV lines, corresponding to a ΔI = ±3A, the system registers and analyzes the under voltage or over voltage reaction at the output. The implemented test verifies that LV channel does not ever switch off and that the recovery time is less than 2 ms (nominal value).
6. AC Noise: for each line the AC noise at the load is measured using a 12 bit ADC acquiring 32000 samples with 20MHz bandwidth. The raw data are analyzed and voltage rms is extracted. The implemented test reject a PSM when 4 *Vrms is greater than 15 mV (LV channels) or 30 mV (HV channels). In the following plots an rms noise of 1 to 3 mV is appreciable.





7. Sense functionality: by forcing each sense line to short circuit to its ground the system checks the proper channel switch off procedure.
8. High Voltage ramp up and ramp down should proceed at 100 V/s. The test system accept a PSM if its HV lines show this feature with a tolerance of ±10%. As can be seen in the following distributions the PSU responses are in the limits.





9. Control Panel: the procedure checks that specific status like Trip, OVC, OVV etc. are measurable at the test points on the PSU front-panel.
10. Interlock: all the PSM in a crate should switch off as soon as an Interlock signal is received by the main CMS safety system. This is simulated by moving the interlock line on the EASY crate bus: channel should then switch off properly and turn back on when the interlock signal is removed.

The mean failure rate we have experienced during the last 2 years production is of the order of 5%, with an evenly distributed source of failure among the 10 different measurements listed above. Details about all the measurement results are retrievable at the page

http://cmstk.to.infn.it/PowerSupply/results.php

All the failed PSMs are sent back to CAEN for repairs and are check back again in Torino before being delivered to the CMS experiment,

IV. HOSTILE ENVIRONMENT TEST

In order to check that the electronic components used to assemble CAEN A4601H are suitable to survive 10 years LHC in the CMS cavern environment several tests have been done to validate CAEN technology during the first phase of the A4601H production, following the experience gained in the prototyping phase [4]. The following sections describe how this has been pursued.

NEUTRON IRRADIATION TEST

The radiation tests discussed in this paper have been carried out using the T2 neutron beam line facility at UCL (Louvain-la-Neuve) (see Figure 3).

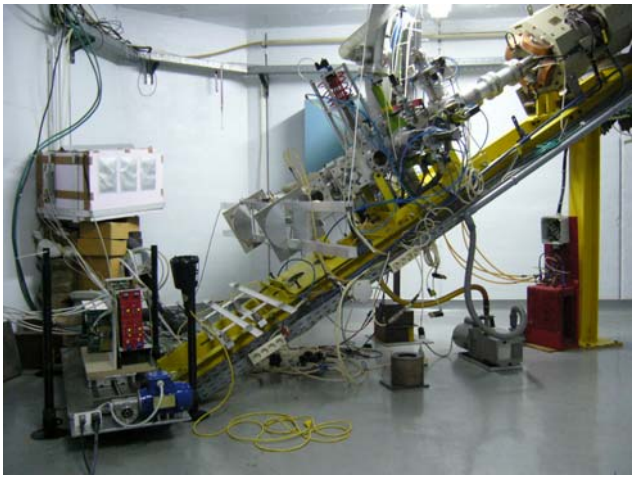


Figure 3: The experimental setup used in Louvain-la Neuve.

Neutrons are obtained converting 50 MeV deuterons on a berillium target. A study [5] has been done on the comparison between the measured Louvain neutron spectrum and the simulated CMS cavern one: 10 years LHC correspond to an integrated "Louvain" flux of 2.17 x 10^10 n/cm2.. The power supply units were mounted transverse to the beam at a distance of about 85 cm from the target..on a movable table. The beam cone radius at the board locations was about 10 cm, with an 85% level of neutron flux homogeneity. By moving the boards back and forth at a speed of about 1cm/s we guarantee homogenous exposure of all the board components. This introduces a correction factor that has been taken into account in the following flux calculations

The irradiation was done in sequential steps having the possibility of tuning the primary deuteron beam current I_b:

Step 1)2.5hours @ I_b =100nA (2.5*10^10 n/cm2)

Step 2)2.5hours a I_b =500nA (1.5 x10^11 n/cm2)

Step 3)0.5 hours a I_b =2500nA (2.7x10^11 n/cm2)

Step 4)0.5 Hours a I_b= 5000nA (0.8 x 10^12 n/cm2)

The first step, corresponding, to 10 years LHC was passed without any problem, and in fact the power supplies survived almost 100 years LHC without failures.

The PSM's output were terminated to resistive loads, placed in a safe room, by using 50 m long LIC cables and communicated as well with a system controller SY2527 that was used to switch on and off the low voltage and high voltage channels and to monitor the outputs with 1 Hz refresh frequency. Moreover it also allowed to check the communication status with the remote branch and to verify the 48 V supply of the remote crate.

The PSU channels were continuously monitored at the loads using a 1MHz digitizer board developed at Torino INFN [6] used in a triggered mode with 50 mV threshold and 2 mV resolution. The idea was that if a Single Event Upset occurred at the PSU level, some instability could appear at the DC output. One example is shown in Figure 4.

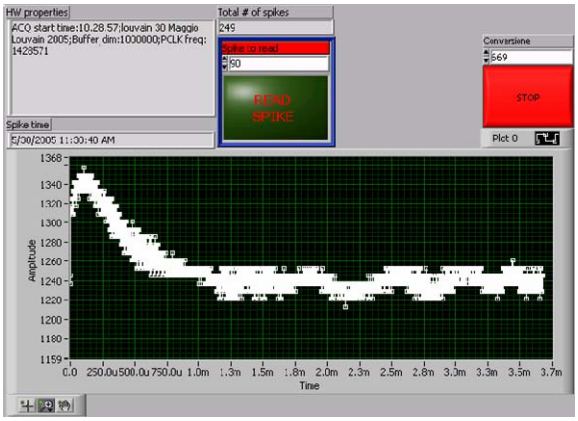


Figure 4: SEU effect on the 1.25V line

Typical amplitude is of the order of 150 mV (see Figure 5) with a recovery time of 0.5 ms (see Figure 4) related to the 2kHz bandwidth of the crowbar circuit used on the CAEN A4601H board to limit voltage instabilities.

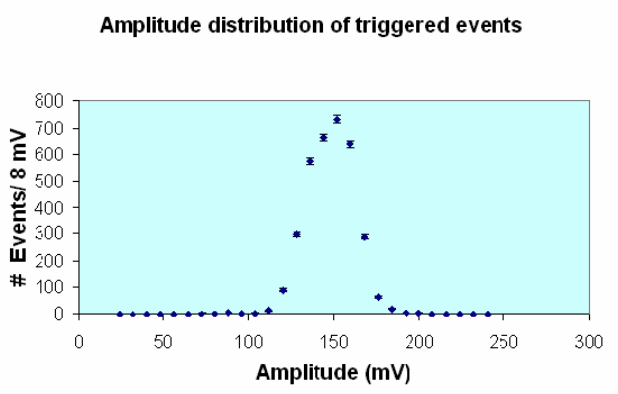


Figure 5: Amplitude distribution of SEU effects as measured at the loads on 4 LV lines using Torino made digitizer. Statistics corresponds to 500 years LHC.

Such instabilities have been proved to be not a problem for the operation of the CMS Tracker front-end electronics. This has been obtained by connecting a real CMS Tracker silicon detector at the PSU output during irradiation and verifying that this kind of oscillations did not affect the detector performances in terms of noise, pedestals and pulse height. The rate of such events was found directly proportional to the beam current and corresponds to 10 events/PSU in 1 year of LHC run at nominal luminosity. Integrating "Louvain" neutron beam current up to 500 years LHC equivalent running period several hundreds of such events have been recorded. However, the PSU's were always able to recover the nominal output values without any external intervention and no switch off was observed.

V. Magnetic field test

The CAEN A4601H underwent a complete magnetic tolerance test at CERN-Prevessin facility.

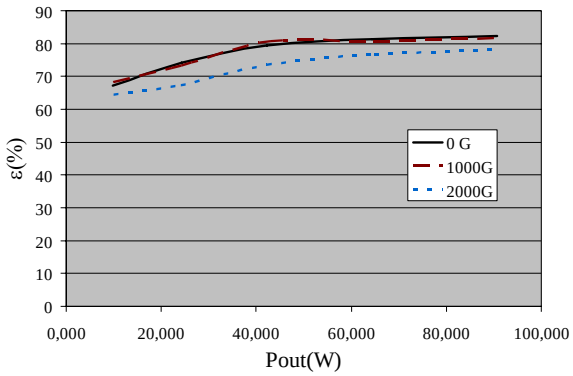


Figure 6: The A4601H board efficiency vs. the output power. Different lines correspond to different values of the magnetic field.

A4601H have been designed to limit the reduction in the efficiency at 1000 Gauss below 10%. For this purpose the range between 0 and 2000 Gauss was explored. The power efficiency of the A4601H board is plotted in Figure 6 as a function of the output power at different B field. The curves correspond to an interpolation of experimental data. Crate auxiliaries and control board dissipate a fix amount of power that have been measured to be 25 W and is not included in these plots. It can be seen that the efficiency is always very good with values of the order of 0.75 and that the external magnetic field has marginal effects on the performance of the power supply. We appreciated a 5% reduction at 2000 G.

VI. Conclusions

The CMS Tracker Power Supply System includes about 2000 complex units, with both LV and HV channels, produced in CAEN technology. A dedicated Test Fixture, developed by INFN-Torino together with CAEN, has been used to validate each PSU during the production. The results of the measurements described in the paper show a very satisfactory quality with a yield greater than 95%.

CAEN technology has proved to be also very robust for what concerns radiation hardness and magnetic field tolerance.

We would like to acknowledge P.Sharp for his encouragement and his advice, F.Faccio and M.Huhtinen for useful discussions on SEU physics , E.Forton for his collaboration at UCL. A special acknowledge goes to Prof. G.Parrini for its support during the definition of the acquisition system and for the interest he has demonstrated in all the phases of the work.

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Evaluation and testing of advanced low-voltage power supplies

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Abstract

A distinguishing feature of the LHC detectors is the enormous number of front end electronics channels in all the sub-detectors. Low voltage power supply systems in the range of multi kilowatts are required to bias such electronics. These power supplies will be located in the cavern close to the detector where stray magnetic field and radiation are present. The main advantage of this topology is the reduction of the length cable needed to carry power to the electronics.

This paper describes results on electrical and environmental tests performed on sample equipment. Descriptions of the objects and methods of tests are given.

I. INTRODUCTION

Several of the sub-detectors in the LHC experiments will have a low voltage distribution for the front-end electronics based on independent multi-channel low voltage power supplies. The overall concept is to distribute DC at high or low voltage to power converters located in the cavern close to the detector, and to transform the DC voltage (400V or 48V) to the required low voltages (between 2V to 8V). This topology reduces the total cross-section of the distribution cables, but the converters have to operate reliably in a hostile environment with significant radiation and stray magnetic fields.

In collaboration with a number of the LHC experiments' sub-detectors, electrical and environmental specifications were established in order to launch a market survey and call for tender by CERN to identify potential suppliers. Eventually W-IE-NE-R Plein & Baus Elektronik - "Wiener" (Germany) and CAEN SpA (Italy) were selected.

To validate the operation of candidate low voltage power supplies, tests were performed on one sample of each item. Verification of the compliance to the electrical specifications, as well as the tolerance to magnetic fields, was made at CERN, whereas radiation tests were performed in several institutes outside CERN.

In this paper the test methodology and results are described, including electrical tests (input and output parameters, efficiency, regulation, ripple and protection etc.), EMC tests (e.g. power factor, harmonic rejection), magnetic field tests, and radiation tests.

II. DESCRIPTION

A. Wiener MARATON

The Wiener MARATON (**MA**gnetism and **RA**diation **TO**lerant **N**ew) is a floating multi-channel high density power supply system consisting of three parts (see Figure 1):

- The AC/DC/PFC which converts the input AC voltage into high DC voltage. The box format is 4U x 14TE x 450mm and can be inserted in a 19''assembly for hosting up to 6 units. It is not tolerant to radiation and magnetic field and must be located in a normal environment. The nominal output power is 3.9kW and the nominal output voltage is 385VDC. The unit also provides active power factor correction.
- The RCM (Remote Control Module) for the control and monitoring is also not tolerant to radiation and magnetic field and has to be located in safe area. It is a 6U VME board form factor, 160mm, 4TE. It can control and monitor up to 12 channels.
- The power box which houses up to 12 DC-DC converter modules supplying the DC output voltage can be located in the hostile environment since it is tolerant to radiation (140Gy over 10 years), and magnetic field (120mT). The format of the box is 3U x 19'' x 325mm.

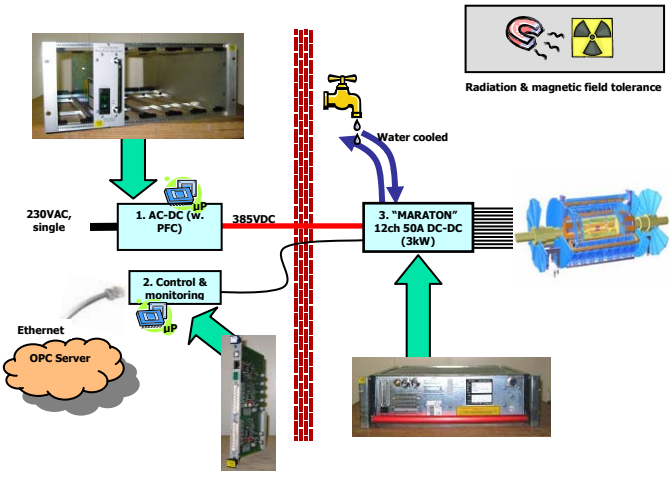

Figure 1: Wiener implementation

B. CAEN EASY

The CAEN EASY (**E**mbedded **A**ssembly **SY**stem) is a low-voltage voltage power supply system designed as an extension to CAEN's existing SY1527 high and low-voltage system, with tolerance to radiation and magnetic fields.

The EASY system consists of four main parts (see Figure 2):

- A radiation and magnetic field tolerant three-phase AC to 48VDC converter providing a 4KW power source for the EASY system.
- An input filter required to reduce harmonic emissions and which acts as a passive power factor corrector. It is not magnetic field tolerant so it must be installed in a safe area.
- Control and monitoring is provided by the SY1527 or SY2527 controller, which also have to be located in a safe environment since they are not tolerant to either magnetic field or radiation.
- A range of radiation and magnetic field tolerant DC-DC converter modules housed in a 6U crate.

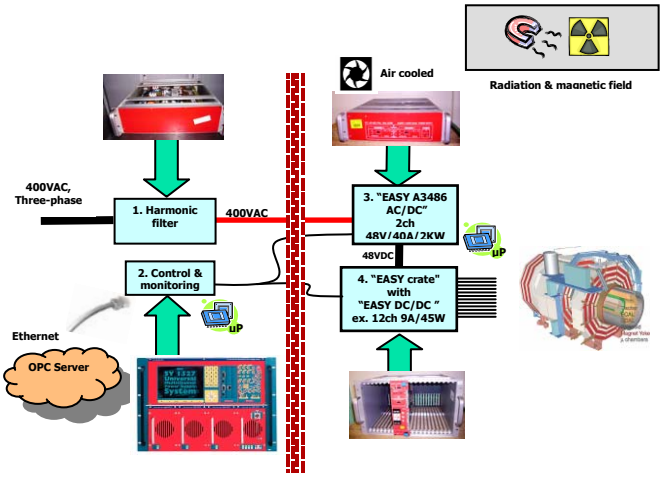

Figure 2: CAEN EASY implementation

III. TESTS AND MEASUREMENTS

A. Electrical tests

These tests consisted of measuring the following electrical parameters for each output channel as well as the overall power supply, functioning in nominal conditions:

- Regulation
  - Static
  - Dynamic
- Efficiency
- Noise and ripple
- Turn ON and OFF characteristics
- Protections
  - Over-current
  - Over-voltage
- Stability
- EMC (Harmonic emissions)

1) Test set-up

The input parameters (i.e. voltage, current and power) are measured by means of an Infratek 603A power analyzer. An electronic load, HP 6050A, was used to sink current from the power supply and to perform current step for dynamic response. The output parameters (i.e. voltage and ripple, etc.) were acquired with a Keithley Digital Voltmeter and a Philips oscilloscope. Figure 3 shows the test-set-up.

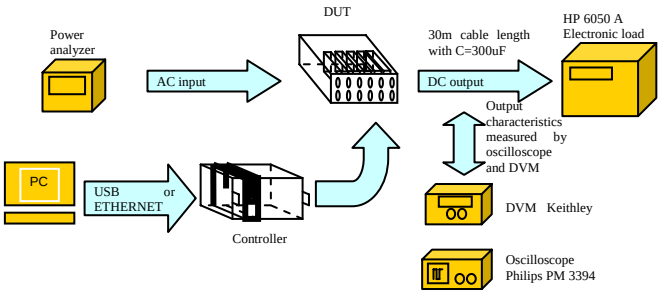

Figure 3: Test set up

2) Test results (Wiener)

The electrical parameters were found to be all within the technical specification with the exception of the ripple which was measured as 15mVpp instead of 10mVpp, but which was considered acceptable (see Table 1).

Table 1:Electrical test results (Wiener MARATON)

Criterions	Specification	Measurement
Static regulation	0.5%	0.034%
Dynamic regulation	10%	8%
Efficiency	70%	75%
Ripple	≤10mVpp	15mVpp
Turn ON	>50ms <100ms	75ms
Turn OFF	<5ms	2.5ms
Current Limit	110%	109.7%
Over-voltage	125%	124%

Table 2:Input AC parameters (Wiener MARATON)

	Phase	Units
Voltage RMS	228.9	V
Current RMS	21.4	A
Active power	4673.2	W
Reactive power	320.8	VAR
Power Factor	0.997	-
Frequency	50.02	Hz
THDi	10^{-5}	-

3) Harmonic emissions(Wiener)

The Wiener MARATON power supply was measured to be compliant to the EMC standard 61000-3-2 from the 1st to the 50th harmonic.

4) Test results (CAEN EASY)

Some functions were found not to be compliant to the technical specification (see Table 3).

Table 3:Electrical test results (CAEN EASY)

Criteria	Specification	Measurement
Static regulation	0.5%	100% in specification
Dynamic regulation	10%	100% in specification
Efficiency	70%	DC/DC: 65% AC/DC: 88% Overall: 57%
Ripple	≤5mVpp	18mVpp
Turn ON	>50ms <100ms	100% in specification
Turn OFF	<5ms	150ms
Current Limit	110%	100% in specification
Over-voltage	125%	No crowbar

5) Harmonic emissions(CAEN without harmonic filter)

The CAEN EASY system, without harmonic filter, was not compliant to the EMC standard for harmonic current emissions 61000-3-2 for harmonic number 5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35. The Power Factor: 0.73 and the THDi: 0.65 were also measured to be out of specification (see Table 4).

Table 4:Input AC parameters (CAEN EASY)

	Phase 1	Phase 2	Phase 3	Units
Voltage RMS	230.1	230.2	230.1	V
Current RMS	7.65	8.02	7.65	A
Active power	1290	1301	1270	W
Reactive power	1200	1250	1200	VAR
Power Factor	0.73	0.73	0.73	-
Frequency	50	50	50	Hz
THDi	0.65	0.66	0.65	-

6) Harmonic emissions (CAEN with harmonic filter)

To improve the AC characteristics, a harmonic filter was required in order for the EASY system to conform to the EMC standard for harmonic current emissions 61000-3-2 from the 1st to the 50th harmonic. The Power Factor of 0.97 and the THDi: 0.17 were brought within specification (see Table 5).

Table 5:Input AC parameters (CAEN EASY)

	Phase 1	Phase 2	Phase 3	Units
Voltage RMS	229.2	230.2	230.1	V
Current RMS	6.18	6.13	5.93	A
Active power	1360	1350	1330	W
Reactive power	2950	2590	2670	VAR
Power Factor	0.98	0.98	0.97	-
Frequency	50	50	50	Hz
THDi	0.18	0.19	0.19	-

B. Environmental tests

Based on the requirements of the LHC experiments, two environmental specifications were established (see Tables 6 and 7).

Table 6: Magnetic field and radiation tolerance for specification A

Category	Mag. field (mT)	TID (Gy) (10 yrs)	N/cm^2 1Mev (10 yrs)	P/cm^2 >20Mev (10 yrs)
Normal environment	<5	<5 10^{-2}	-	-
Low magnetic field, low radiation *ALICE*	<30	<1 10^{-1}	10^{10}	2 10^{9}
Low magnetic field, high radiation *LHCb*	<30	140	10^{12}	2 10^{11}
High magnetic field, high level radiation *ATLAS-TRT*	<120	140	10^{12}	2 10^{11}

Table 7: Magnetic field and radiation tolerance for specification B

Category	Magnetic field (mT)	TID (Gy)	Neutrons N/cm^2 1Mev	Protons P/cm^2 >20Mev
CMS experiment	180[1]	4	10^{11}	10^{10}

1) Magnetic field tolerance tests

These tests consist of measuring the tolerance of the power modules in magnetic field environment working in nominal output power conditions in all axes. They were performed at CERN using magnets with different dimensions.

The PH/ESS magnet was used for component tests, since its aperture is only 15cm. The maximum magnetic field is 1.8kGauss. See Figure 4.

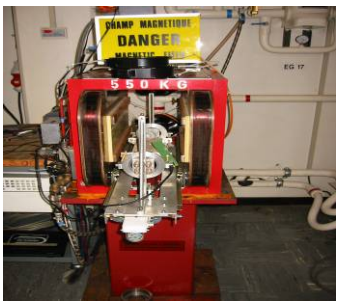

Figure 4: PH/ESS magnet

To test complete systems, a magnet with 50cm aperture was necessary, and the CERN MNP22 magnet was used, see Figures 5 and 6.

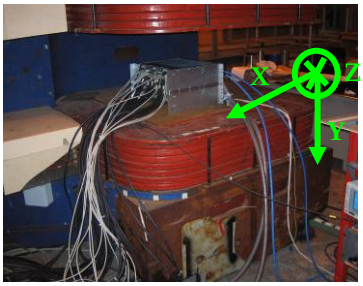

Figure 5: Wiener MARATON system

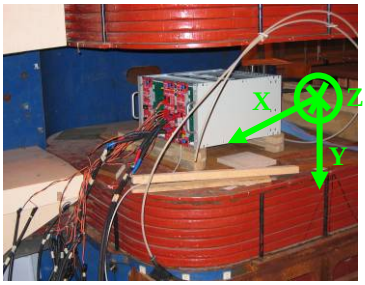

Figure 6: CAEN EASY system

2) Magnetic field tolerance test results

Wiener MARATON

The approach taken by Wiener to magnetic field tolerance was to start with one of their standard low voltage power

[1] The magnetic field tolerance requirement for CMS was relaxed to 120mT after a new simulation of the stray magnetic field.

supply products and to make the minimum modifications necessary to make acceptable for LHC environment. The changes included soft iron screening of the magnetic components, such as transformers and inductors and, following tests, a judicious selection of components for radiation tolerance.

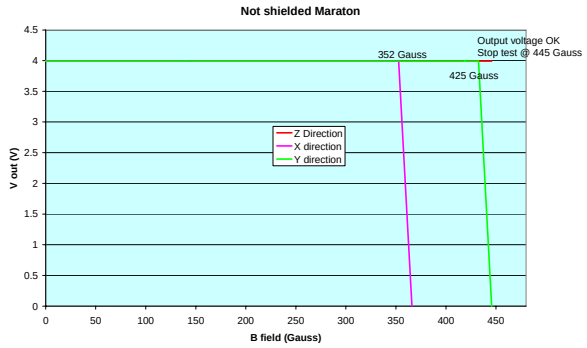

Figure 7: Magnetic field test for non-shielded MARATON

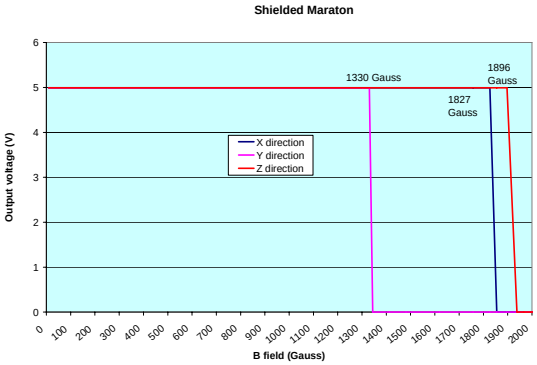

Figure 8: Magnetic field test for shielded MARATON

Both Wiener MARATON power supply topologies, unshielded and shielded, are conformant to the technical specification A in any magnetic field direction: 30mT for the unshielded and 130mT for the shielded.

CAEN EASY

CAEN adopted a novel research strategy using transformers with high permeability able to operate in high external magnetic field

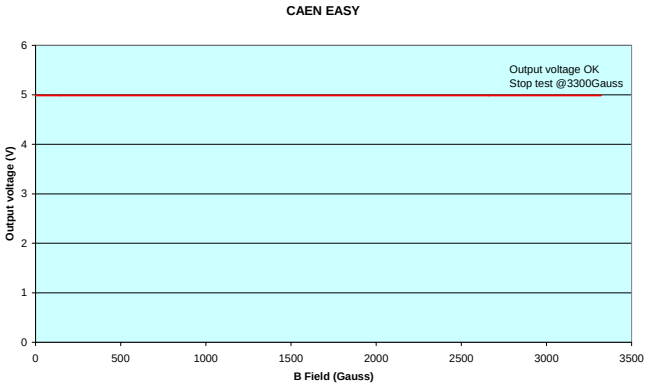

Figure 9: Magnetic field test for CAEN EASY

All the CAEN EASY equipment is compliant to both the A and B technical specifications concerning the magnetic field tolerance. Figure 9 shows the response of one EASY power module (A3009); the results obtained for all the DC-DC converters tested were found to be identical.

3) Radiation tolerance tests

These tests consisted of measuring the tolerance of the power modules to radiation working at nominal output power conditions, and were performed several facilities.

For proton tests, beams in three different locations were used. The PSI (Paul Scherrer Institute), in Switzerland and the UCL at Louvain la Neuve, in Belgium have small diameter beams (8 - 10cm), and were used to test devices at component level.. Complete systems, for which a large beam was necessary; were tested in the TSL proton beam at Uppsala in Sweden which has a diameter of 15 to 20cm (see Figure 10).

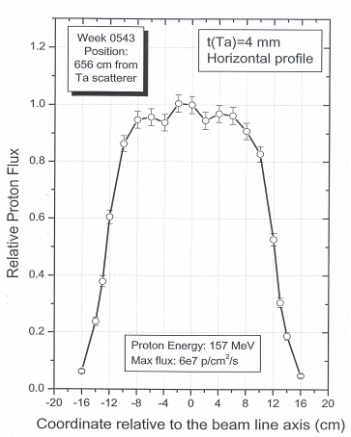

Figure 10: TSL Uppsala beam profile

For NIEL tests, the PROSPERO nuclear reactor at Valduc near Dijon in France which produces neutrons at 1Mev energy was used, and for TID tests a cobalt 60 source in Cassacia in Italy was used.



Figure 11:Uppsala protons beam



Figure 12:PSI proton beam



Figure 13:PROSPERO reactor

4) Radiation tolerance test results

Several irradiation campaigns demonstrated the weakness of various components and corrective actions were required.

In the Wiener topology, opto-couplers had to be changed because of NIEL effects. Also, due to the implementation of a Power Factor Corrector, switching transistors having a greater drain-source voltage were used, necessitating extra radiation tolerance tests.

In the CAEN topology, a low pass filter in the microprocessor reset line had to be implemented, due to the sensitivity to high energy hadrons of the existing opto-couplers. Also, other components such as amplifiers and EPROMs had to be replaced.

After several iterations, over a number of years, the tolerance of the Wiener MARATON to radiation was as shown in Figure 14.

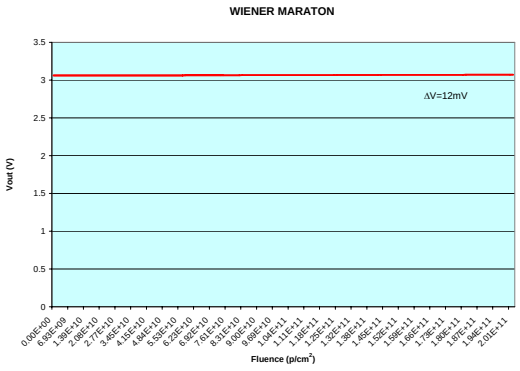

Figure 14:Radiation test for the Wiener MARATON

After modifications made on the CAEN EASY system, it behaved under radiation as shown in Figure 15.

Concerning Wiener, there no event was seen up to $2*10^{11}$ p/cm^2, 14kRad. Previous campaigns for NIEL tests were also successful. Concerning CAEN, there is one event due to the loss of communication between the controller and the EASY module. However this is acceptable since this fluence represents 10 years of operation of the experiments.

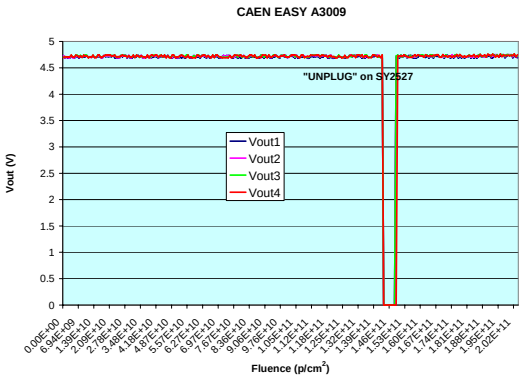

Figure 15:Radiation test for the CAEN EASY

IV. Conclusions

Some of the specified parameters had to be adapted to changes in the requirements of the detectors during the approval process. In addition, compromises were accepted to the specification where the resulting changes had limited impact on the overall performance of the power supplies. Qualified radiation and magnetic field tolerant detector power supplies are now available to the four LHC experiments from two suppliers, CAEN and Wiener.

The qualification of COTS equipment is a very long, costly and painful process. Close collaboration between users, power supply and radiation tolerance specialists at the earliest possible stage is of prime importance to minimize the time required as well as the overall cost.

V. Acknowledgements

Access to the broad proton beam at TSL was possible thanks to the "Transnational Access within the Integrated Infrastructure Initiative" from the European Community.

I would like to that the following for their advice, support and hard work during the long process of qualifying the power supply systems:

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C .Parkman (CERN, PH-ESS)
R. Richter (MPI)
C. Rivetta (SLAC)

In addition many other colleagues from CERN, the LHC experiments and the two manufacturers concerned have made very important contributions...

VI. References

[1] Wiener MARATON user manual. http//www.wiener-d.com/
[2] CAEN EASY user manual. http://www.caen.it/
[3] Test report in preparation

Distributed Low Voltage Power Supply System for Front End Electronics of the TRT Detector in ATLAS Experiment

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Abstract

We present a low voltage power supply system which has to deliver to the front end electronics of the ATLAS TRT detector [1] ca. 23 kW of electrical power over the distance of 55 -106 m (which adds another 24 kW). The system has to operate in magnetic field and under radiation environment of the LHC experimental cavern. The system has ~ 3000 individual channels which are all monitored and controlled (voltage and current measurement). The hardware solutions are described as well as the system control software.

I. INTRODUCTION

A. TRT detector

The TRT (Transition Radiation Tracker) is a part of the Inner Detector tracking system of ATLAS experiment. It covers $|\eta|<2.5$ in pseudo rapidity at radii between 128 and 206 cm, allows for electron-pion separation at 97% level and provides continuous tracking with accuracy ~120 μm/point. The detector has three parts – barrel and two end-caps – which consist of arrays of the thin walled proportional counters – straw tubes. The barrel detector contains 96 parts called modules (3 layers of 32 modules). The end-caps consist of 20 'wheels' each, where wheel is functionally divided into 32 sectors. Each module and sector have its own individual electrical services (HV, LV, timing etc). The straw configuration gives ~36 space measurement points in whole TRT acceptance. The detecting elements act as drift tubes ensuring the tracking function and measure energy deposit in specially chosen active gas allowing for efficient detection of the transition radiation photons thus performing identification function. The detector contains ~350 000 detecting elements - straws.

B. Power requirements

The front end electronics of the TRT is based on two custom designed ASIC's: ASDBLR (amplifier-shaper-discriminator-base-line-restorer) which amplifies, shapes and discriminates the charge signal from straw anode and DTMROC (drift-time-measuring-read-out-chip) which measures the time-of-arrival of the signal with respect to the bunch crossing, encodes the charge value and serves as the read-out controller. Both chips are designed in radiation hard technologies. Total power consumption of individual channel is 40 mW/channel for ASDBLR and 21 mW/channel for DTMROC. From quoted numbers we find that whole front end (F-E) electronics consumes ~23 kW of power. Modern fast electronics requires very low voltage power supplies which results in high supply currents. Then a length of the cables, their cross-section and voltage drops are important factors for the power supply system design.

The F-E electronics of the TRT requires +/-3V (analogue part) and +2.5V (digital part). The auxiliary circuitry requires additional, supply of +5V with relatively low current.

The following table shows the current consumption in different detector parts.

Table 1: Power consumption in TRT detector (per side)

Sub-detector	Per stack/sector/side			Per subdetector/side		
	+3V	-3V	+2.5V	+3V	-3V	+2.5V
Barrel	13A	11A	13.5A	416A	352A	432A
Wheels A	18A	16A	19A	576A	512A	608A
Wheels B	12A	10.5A	12.5A	384A	336A	400A
Total	*43A*	*38A*	*45A*	*1376A*	*1200A*	*1440A*

Estimated power dissipation in the front end electronics is 22.66 kW. This requires careful design of the cooling system having in mind the confined space where electronics is positioned.

II. ARCHITECTURE OF THE SYSTEM

The TRT low voltage system consists of two basic parts - Figure 1:

- ✓ Bulk power supplies delivering power to distributors associated with detector geographically defined zones (in TRT case this are 32 sectors in Phi)
- ✓ Voltage distributors which supply individual loads (multiple in each sector) splitting the lines received from bulk power supplies

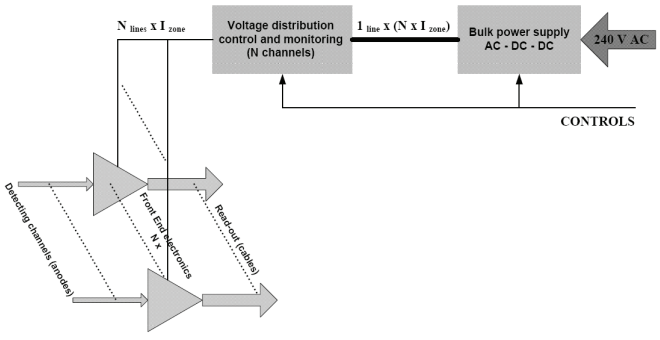

Figure 1: Architecture of the powering system

A. Bulk power supplies

To minimize the need for development, service and maintenance effort we have decided to use commercially available hardware. After market survey the WIENER MARATON [2] power system has been chosen. The system, developed originally for the needs of LHC experiments is able to operate in the moderate magnetic and radiation fields existing in the ATLAS experimental cavern during LHC operation. The principle of the system is shown on Figure 2:

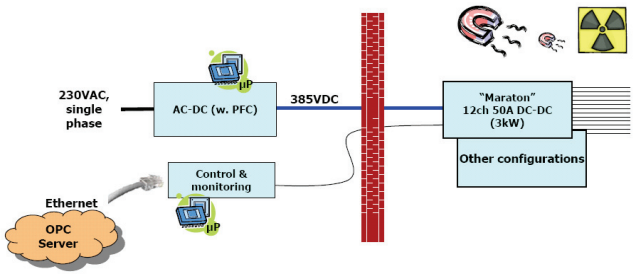

Figure 2: The MARATON power supply system (picture courtesy C.Parkman CERN)

Proper choice of the granularity allows for grouping into 'slices' (or 'wedges') the detector; a 1/32 phi segment of the detector is driven by four MARATON modules (one per each voltage used by the front-end electronics and one for the patch panel) delivering 8 V - 50 A. Control part of the system is placed in the control room. The bulk DC-DC converters are situated in the experimental cavern. Such a configuration allows for reasonably short low voltage cables requiring large cross-section of the Cu conductor and contributing to losses.

B. Voltage distribution

The voltage distribution has been based on the availability of radiation hard voltage regulators [3]. The granularity of the sub-detector front-electronics is such that each 'granule' consumes a current which can be delivered by 1 (or max. 2) voltage regulator i.e. ~ 3 A. The regulators together with control and monitoring electronics has been arranged onto boards which are housed in specially designed liquid cooled simple crates called Patch Panels 2 (PP2). These patch panels boards are placed within the volume of ATLAS at a 12 to 15-meter distance of the front-end electronics.

1) Radiation hard voltage regulators

The LHC(X)913 is a positive/negative voltage regulator family. Housed into power SO-20 slug-up, it is specifically intended for applications in rugged environments, subject to ionizing and neutron radiation. Input voltage ranges from (-)3 to 12(-9) volts. It is characterized by a low voltage drop (0.5 volt@ I_{out}=1A and 1.5V@I_{out}=3A). The over-temperature, and over-current protections guarantee robust operation. Output short circuit monitoring, signalled by TTL output allows for status detection. The regulator can be enabled/disabled by external TTL signal which in our application is going to be used for control of each output.

2) Low Voltage Patch Panels

Groups of regulators supplying geographically close parts of detector front-end electronics have been placed on a printed circuit board together with the control and monitoring electronics. One card of 440x200 mm size houses up to 36 regulators (positive and negative) delivering 6/8 voltage sets : +/- 3 V for analogue electronics and +2.5 V for digital part. Three boards are used to power a 1/32 phi slice of the detector: 1 for the barrel part and two for the end-cap wheels. Due to high power dissipation on the board (60 - 70 W) and to the requirement of being thermally neutral, it is equipped with an aluminium cooling plate which transports heat to the crate body where it is taken away by liquid cooling circuit. Thermal contact between regulators packages and cooling plate is assured by a layer of special thermo conductive rubber. Figure 3: presents the board photo (control side).

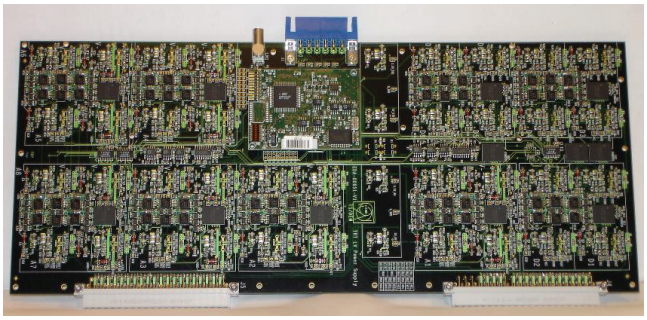

Figure 3: Low voltage 'patch panel' board

The circuits on the board perform the functionalities described in following paragraphs

3) Voltage regulation and setting.

The regulators used are of the adjustable version. Changing the voltage 'adjust' input allows output to be set at the value assuring the proper operation of the f-e electronics during life cycle of the experiment when semiconductor devices could change its characteristics due to radiation. The variable voltage is delivered by radiation hard DAC embedded in the DTMROC chip [8]. The settings of the DAC's are controlled over simple 3-wire serial protocol. The current swing of the DAC output allows for regulators output to be varied by ~0.5V up to 1.2 V, which is fully covering expected change of the voltage supplies of F-E electronics. Figure 4: shows basic schematic of the regulator control [4].

Some F-E parts draw current slightly exceeding the maximum one allowed for the regulators (wheels A). For these channels parallel operation of the regulators has been implemented. Carefully designed biasing network ensures correct sharing of current between the two regulators.

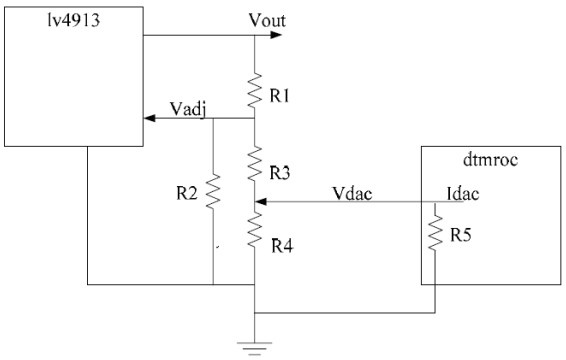

Figure 4: Positive voltage adjustment

4) Voltage and current measurements in each individual output line.

The board contains embedded controller – an ELMB (**E**mbedded **L**ocal **M**onitoring **B**oard), standard control unit designed for ATLAS [5]. All voltage outputs are connected to the ELMB's ADC allowing for output voltage measurements. The same ADC is measuring the output currents, by monitoring the voltage drop on 22 mOhms serial resistors inserted in output lines.

5) Over Current protection

The regulators have an over-current protection which, when current drawn exceeds designed value, operates the regulator in constant current mode. Such a state of regulator is signalled by a level on one of the pins. This signal is latched by board logic and can be read-out by ELMB and if enabled will switch the affected channel off.

6) Enabling and disabling individual output lines (on/off)

The DTMROC has an output which via the proper command can be set 'true' or 'false'. This output is connected to the 'inhibit' input of the pertinent regulator thus providing a mean to switch the regulator output on/off. The same input is as well accepting the signal from over-current-monitor circuitry.

C. Control and monitoring

The TRT power supplies control system has been build upon the commercial SCADA (**S**ystem **C**ontrol **A**nd **D**ata **A**cquisition) software package chosen by CERN as standard for control systems of LHC experiments – PVSSII. Detailed description of the available tools and methods can be looked at elsewhere [6].

1) CAN bus and ELMB

ELMB is a basic hardware unit of ATLAS detector control system which can operate in magnetic field and radiation environment of experimental cavern. It contains 64 channels multiplexed to the ADC input and several I/O digital ports. Its basic functionality and detailed description can be found elsewhere [5]. ELMB commands and monitoring readback values are send over the CAN bus - one of the CERN recommended commercial fieldbuses.

The CAN bus, designed and widely used in automobile industry, is a very robust communication layer and both hardware and software components are available from wide range of manufacturers.

Different autonomous actions can be taken when ELMB error condition was detected: node reboot, microcontroller firmware reload, disconnecting affected node from CAN bus. Merging the NodeID with MessageID codes to COBID (CAN Object ID) field allowed to set very efficient message oriented priority mechanism. A set of broadcast messages allows reducing bus load in complex systems.

2) DTMROC

The DTMROC is the digital front end chip for the TRT detector. This radiation hard chip contains four 8-bit DAC's which are used here to set the output voltage of the regulators.

Writing and reading of the DTMROC registers is performed over a 3-line serial protocol (data-in, data-out, clock) which is driven by the ELMB in this application.

III. SOFTWARE SOLUTIONS

A. Bulk power supplies

The MARATON power supplies are delivered with an OPC server package which serves for the remote control of the unit. The server operates via Ethernet.

1) OPC standard

One of the means to facilitate the equipment integration into complex control system is use of the standard interfacing methods to remove the need of device specific drivers. Industry cooperation with Microsoft has resulted in construction of the OPC (OLE for Process Control) standard. The device driver is hidden under the server software layer which when complying with OPC rules allows for easy integration into any SCADA system. The OPC standard has been adopted by CERN as one of the mandatory specifications for commercial equipment purchased for LHC experiments.

2) CERN FRAMEWORK

The effort needed for design and construction of the control system for LHC experiments in many cases surpasses the possibilities and available manpower of groups involved. This has resulted in wide use of commercial equipment and software tools making the tasks possible to achieve. CERN control group from IT department provides users with the skeleton software solution called FRAMEWORK. The package contains many useful tools serving for construction, integration and configuration of the complex multi-channel systems build of the standard, widely available equipment. The MARATON system has been included into FRAMEWORK which makes its integration very easy. Figure 5: shows typical PVSSII [6] control panel for MARATON system which can be tailored to specific user needs.

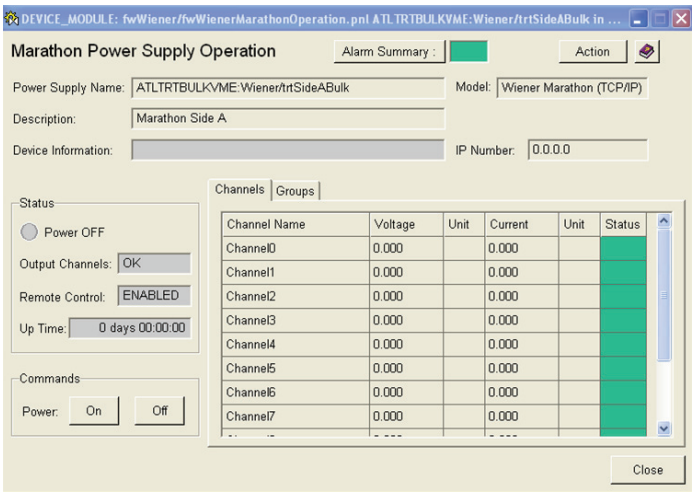

Figure 5: MARATON control panel as provided by CERN FRAMEWORK

The control commands of the MARATON system are limited. Basically the only important action which can be undertaken by user is switching the given output *on* or *off*. Such an action is triggered by clicking *ON* or *OFF* buttons on the panel.

B. LVPP boards

The main development effort spend on the TRT low voltage system has been directed into the design, programming and debugging of the Low Voltage Patch Panel boards (LVPP) containing the voltage regulators and main controlling/monitoring circuitry. As already has been mentioned the heart of the LVPP is an ELMB communicating with the host controller over the CAN bus. The read-out of the analogue values (current and voltage) is typical (and standard) for ELMB use and is based on the CANOpen [9] software layer where the OPC standard for data access has been implemented. The 'analogue' functionality of the ELMB has been included as well into CERN FRAMEWORK package so the integration and control is reasonably easy and straightforward. Fully custom made design was done for the control of the voltage regulators by DTMROC's. Figure 6: shows idea of the control.

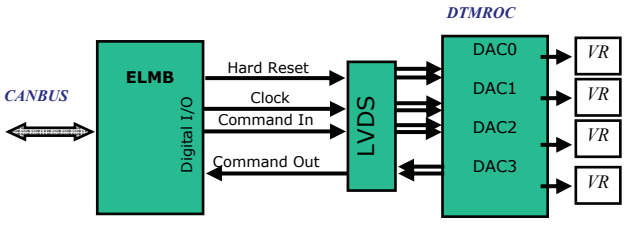

Figure 6: ELMB controls DTMROC

1) Possible solutions

The commands issued by control application to the DTMROC's via ELMB have to follow the mentioned control protocol i.e. ELMB has to send properly formatted data stream accompanied by clock pulses. This is done by proper control of the outputs of the ELMB digital ports. However correct sequence of bits and clock pulses on the output lines can be generated by programming in several places of the software layers. The expected performance is discussed on Figure 7:

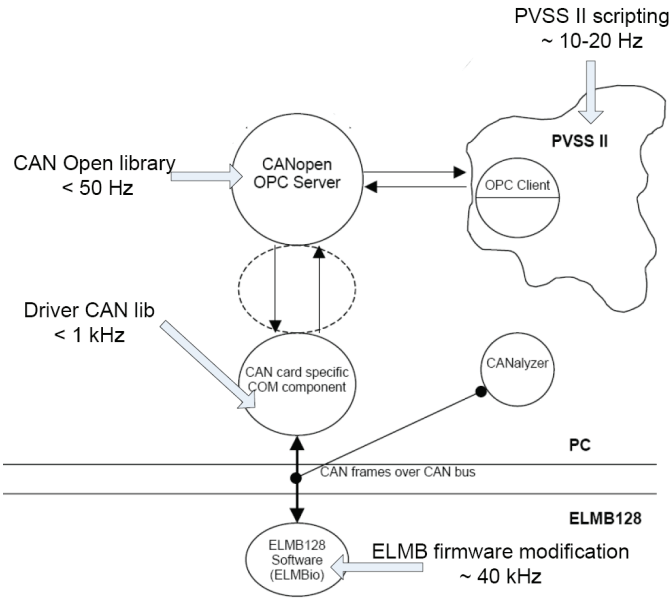

Figure 7: DTMROC control - possible places of the control software embedding

The easiest way would be to implement all algorithms simulating the DTMROC serial protocol in the PVSS layer. However this leads to slowest clock due to fact that scripting language of PVSS is interpreted and not compiled. The most performant solution would be to modify ELMB firmware embedding in its memory preset bits patterns send to DTMROC by single CAN message. Other, intermediate solutions would be to use modified software of CANOpen level or one acting directly on the driver by calls to its DLL classes. The attractive, firmware based solution has been dropped off since this would mean that our ELMB's become TRT custom equipment and have to be maintained, serviced and upgraded by us – which due to lack of manpower could not be realised right now. However this remains as possible upgrade for control system in future.

2) Custom DLL

We have decided to construct an extension to the standard PVSS CTRL scripting language [10], which allow for user defined functions to be interpreted by PVSS in the same way as PVSS functions. It consists of a set of class methods compiled into new shared library DLL, providing the input, output parameters and return value. The functions access directly the CANbus driver. The DLL contains following functionalities.

- Initialization of the CANbus, ELMB, DTMROC
- Operational:
  - Setting DAC's,
  - Reading back DAC's,
  - Setting *inhibits* in DTMROC's,
  - Reading back *inhibit* state,
  - Enable/disable and read out OCM state
- Diagnostics:
  - reset (soft and hard) of DTMROC's,
  - send given number of clocks to DTMROC's,

- get state of a given DTMROC,
- set ELMB in the requested state,
- read back ELMB state

- Closing connection,

IV. Performance and Results

The tests of complete system have shown that we achieved DTMROC clock frequency ~ 370 Hz (Figure 8:). The limiting factor appeared to be the ELMB firmware. When operating the CAN bus clock at 125 kHz, some messages have been randomly lost due to ELMB input buffer overflow. We had to operate the CAN bus at 50 kHz.

This results in ~ 5 sec. for setting one LVPP (1/32 of detector part – wheel A, B and barrel).

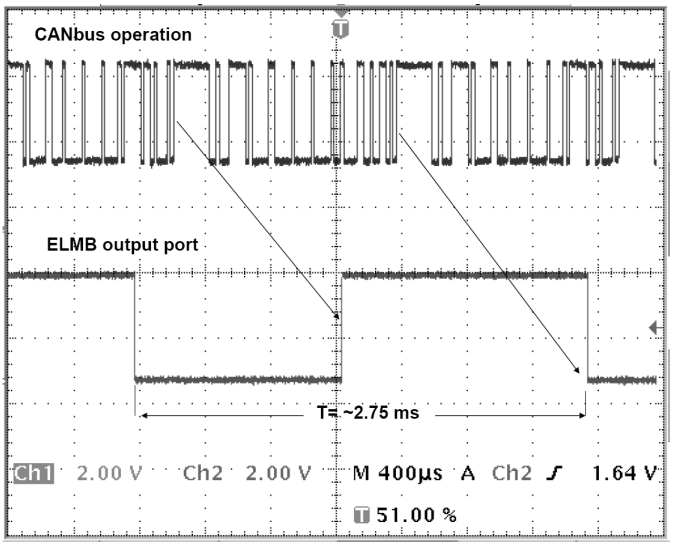

Figure 8: CAN bus messages and corresponding ELMB's digital port output (clock)

Thus the whole TRT can be set in ca. 90 sec's (taking into account topology of LV system, patch panels and configuration of CAN bus branches). If values written in are checked for correctness by read back, quoted time increases to 240 seconds. Since such an operation is foreseen only during cold start up of system (after detector shutdown) this time is deemed fully acceptable. Sequence of the control signals from ELMB is shown on Figure 9:

The plots of the regulators (8 channels) outputs for full range DAC (0-255) swing are shown on Figure 10.

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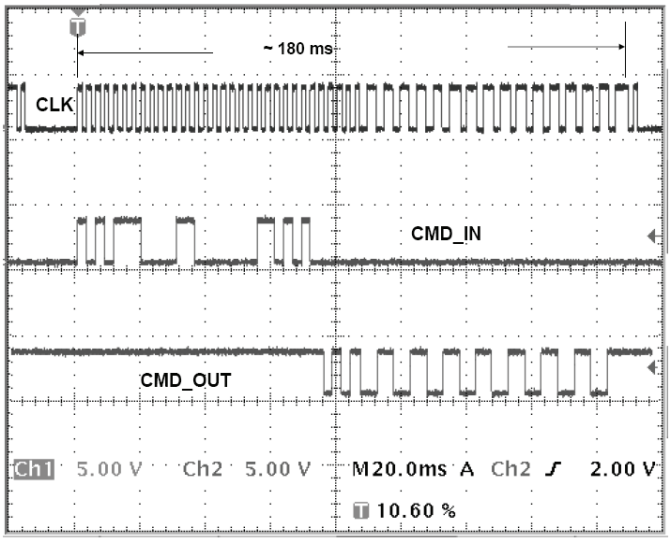

Figure 9: Exemplary scope plots observed on control lines during 'read' operation.

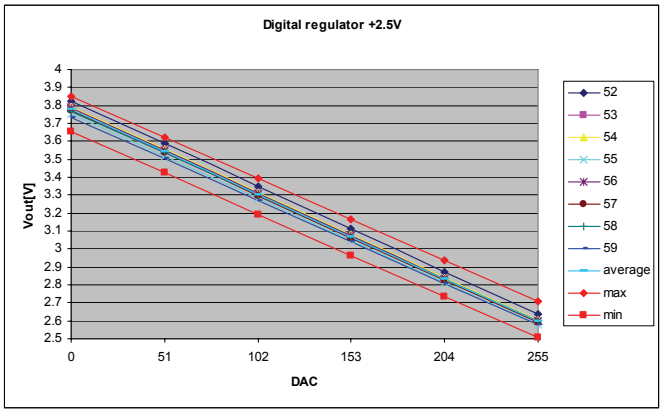

Figure 10: Output voltage of digital regulators

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Electromagnetic Compatibility of a Low Voltage Power Supply for the ATLAS Tile Calorimeter Front-End Electronics

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Abstract

The front-end electronics of the ATLAS Tile Calorimeter is powered by DC/DC converters that sit close to it. The performance of the detector electronics is constrained by the conducted noise emissions of its power supply. A compatibility limit is defined for the system. The noise susceptibility of the front-end electronics is evaluated, and different solutions to reduce the front-end electronics noise are discussed and tested.

I. Power Distribution Scheme for the Tile Calorimeter

The front-end electronics of the Tile Calorimeter [1] is organized in drawers that are inserted in detector modules. Each drawer is 3 meter long and contains the front-end analogue and digitizing electronics for 45 photomultiplier tubes [2] in the case of the barrel modules. It is powered by eight regulated low voltage lines, and it is rated to consume a maximum power of 300W.

Because a drawer requires a tight voltage regulation on its power lines, the low voltage power supply was designed to fit in its vicinity, as an extension of it. The environmental constrains such as radiation and magnetic field tolerance were solved with the design of custom DC/DC converters that are remotely controlled by an ELMB [3]. The power supply is located in a closed volume known as *finger*. The power supply is water cooled.

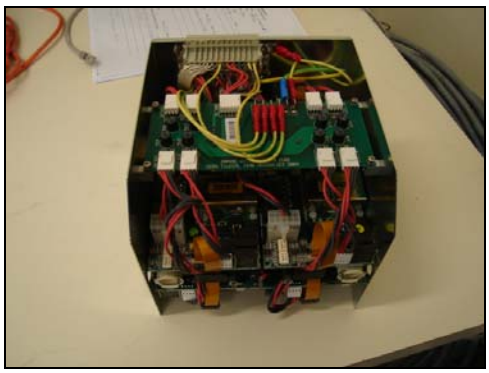

Figure 1: Finger low voltage power supply of the ATLAS Tile Calorimeter.

The finger low voltage power supplies (figure 1) are fed by bulk power supplies (200VDC) located in a control room. Auxiliary power supplies in the same control room are also required to power separately the monitoring and control circuitry. The power system (figure 2) is controlled by the Detector Control System (DCS) through a CANBus line that communicates with the ELMB of the power supply.

The low voltage outputs are isolated from earth, but all the return lines are put in common inside the drawer.

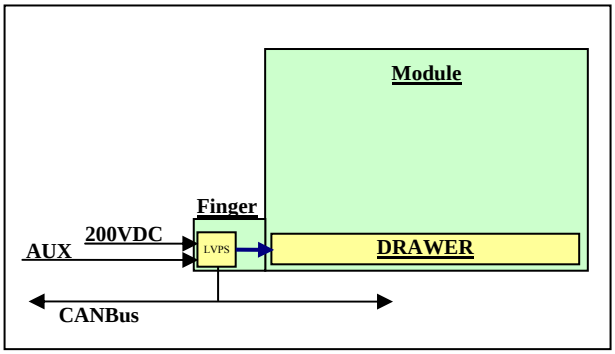

Figure 2: Tile Calorimeter power distribution scheme.

Noise Performance Test Methods

The front-end noise is composed by the drawer electronics noise, by the power supply noise and by the external couplings on the interconnecting cables (not studied here).

A. System Noise.

The achievable performance of the drawer electronics in terms of noise is limited by design. The system noise in each front-end channel was measured in detail on drawers that were powered with low noise linear power supplies. The system noise is evaluated in terms of high frequency and low frequency contributions from the data taken with the full data acquisition chain.

The high frequency noise seen by the fast readout electronics is estimated from the pedestals data. The estimation is based on a selection of parameters computed over several runs and on all the channels of a drawer:

- RMS of the pedestals distribution.
- Gaussian property of the pedestals distribution.

The low frequency noise is evaluated from data sampled by the current integrators ADC. Since the data is sampled sequentially channel by channel, correlation figures between channels are the best method to track low frequency noise.

The system noise requirements are specified as:

- High gain fast readout: RMS ≤ 1.5 counts.
- Slow integrators readout: RMS ≤ 2.0 counts (for any given gain).

B. *Noise Properties of the Converters.*

A DC to DC converter is a source of high frequency noise in the form of common mode current sent to the load. The measurement of the output common mode current into a nominal resistive load allows evaluating the noise performance of a given power converter [4]. The measurement is made on the output of each converter or on the entire voltage bundle, with a calibrated current probe and an EMI receiver (figure 3). The obtained spectrum is then compared with respect to the limit lines specified in the ATLAS EMC policy [4].

The measurement of the total common mode current that enters the drawer electronics and that returns through the steel is measured with the same setup on the low voltage bundle that feeds the drawer.

The low frequency noise is contributed by the output ripple and it varies with the applied load. It is easily measured with an oscilloscope under nominal load conditions.

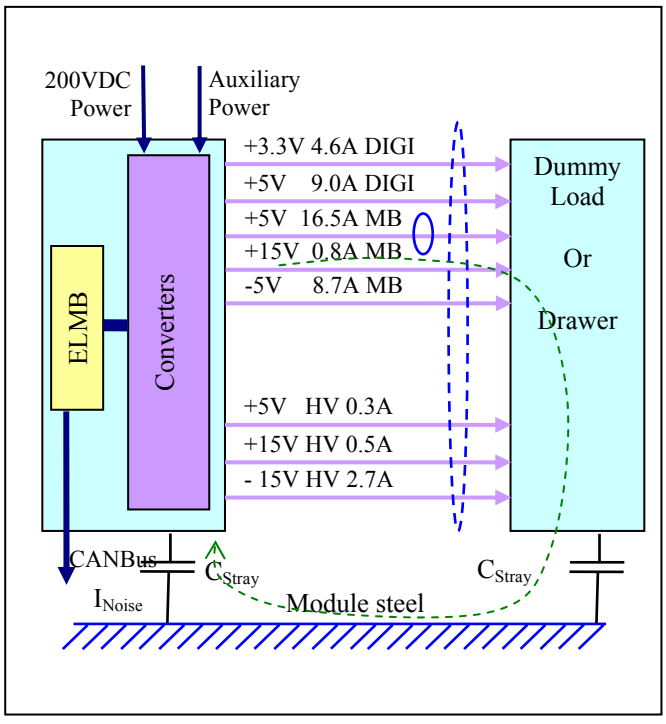

Figure 3: Finger power supply outputs ratings and common mode current measurement method on individual output (plain) or on the whole bundle (dashed). Stray capacitances couple noise currents to the module.

NOISE MEASUREMENTS

The noise performance of the finger low voltage power supply (FLVPS) is compared with the equivalent performance of a temporary commercial, off-the-shelve, switched mode power supply used for the commissioning of the drawers in the ATLAS cavern. The system noise achieved with the temporary power supply and a linear power supply are equivalent. The measurements techniques, tools and reference limits considered here are defined in the ATLAS EMC Policy [3].

A. *High frequency noise susceptibility.*

The measurement on individual outputs connected to a reference load showed that (figure 4):

- Both power supplies exhibit large common mode currents at the main switching frequency and associated harmonics, exceeding by 40 dB the limits in use.
- Above 1 MHz, the FLVPS emits 20dB more common mode current than the temporary LVPS.

The measurement on the whole low voltage bundle showed that (figure 5):

- The switching noise current stays below the limit and is smaller than the same current as measured on individual outputs.
- Above 1 MHz, the FLVPS exhibits up to 40 dB more noise current than the temporary power supply.

The switching noise current of a given converter returns through the cables of the others because they share a common return at the level of the load. The switching noise current path is comprised between the power supply and the common ground point, with a limited impact on the front-end performance.

At higher frequencies, the noise current propagates towards the front-end electronics of the drawer, and reaches the steel of the module through stray capacitances. The module provides a very low inductive return path to the power supply. Because of this, the noise current of each one of the converters is summed up. The high frequency noise current degrades the performance of the front-end electronic.

The larger system noise is expected close to the point where the converters return lines are put in common, namely in the vicinity of the patch panel (figure 6). The noise current leaves the drawer through stray capacitances to the steel, and its magnitude decreases as the distance from the common grounding point increases. This is clearly observed from the raw data (figure 6).

The excess of common mode current also results in a non Gaussian pedestals distribution (figure 7). The non Gaussian part of it is highly correlated for different channels, resulting in an undesirable impact on the jet energy measurements.

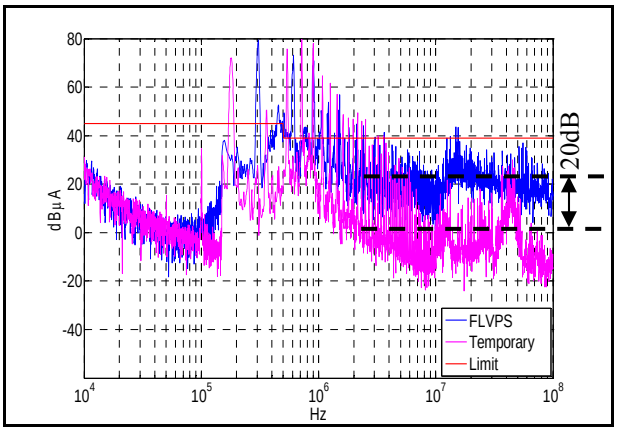

Figure 4: typical single output common mode current.

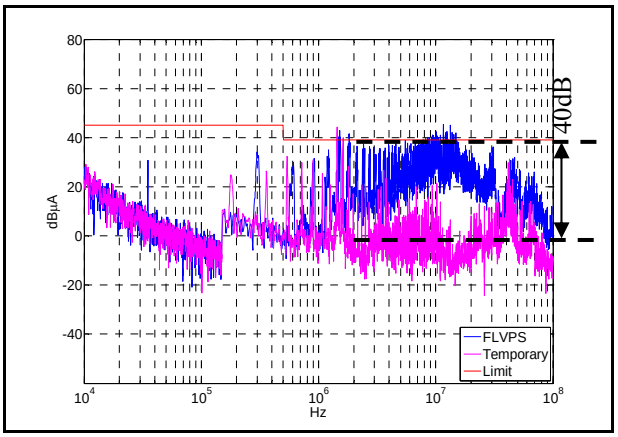

Figure 5: typical LV bundle common mode current.

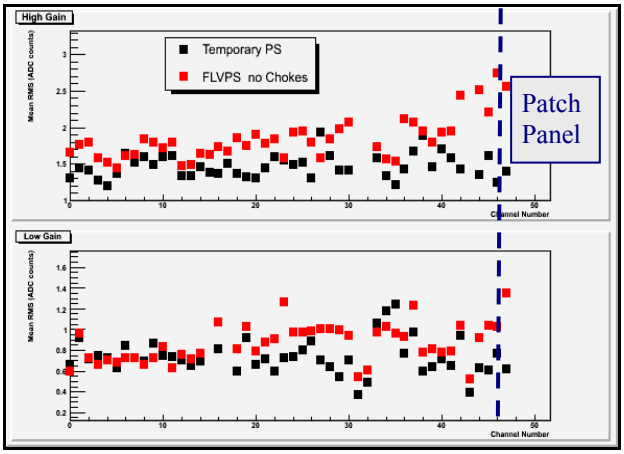

Figure 6: Pedestals RMS distribution across a drawer (patch panel on the right hand side).

B. *Filtering of high frequency noise.*

To reduce significantly the amount of common mode current sent to the drawer, the common mode impedance of the converter output must be increased in the frequency range where the front-end electronics is most susceptible to noise.

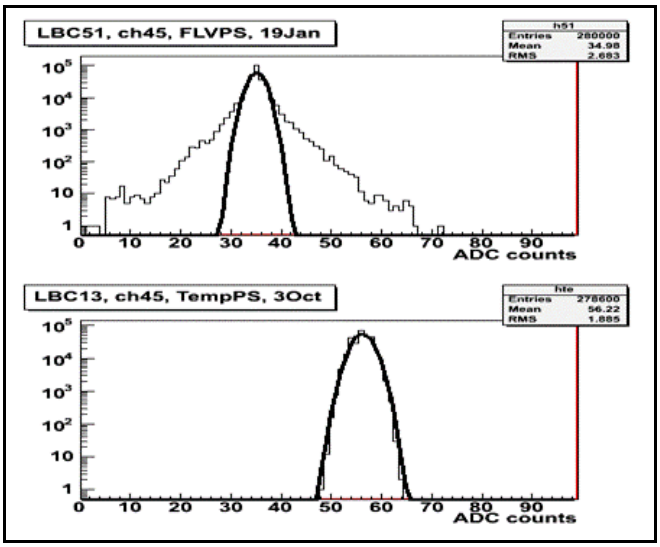

Figure 7: non Gaussian distribution of pedestals when using the unfiltered finger power supply (top) versus Gaussian distribution when using a commercial power supply (bottom).

First, common mode chokes placed on each converter output turned out to be the most efficient way to reduce the common mode current. The selected chokes, rated to 10A, offered an attenuation of more than 20 dB from 100 kHz to 10 MHz (figure 8). The common mode current on the output of each converter was brought below the limit in the switching frequency range and above 10 MHz, and the resulting noise distribution got better than with the temporary power supply (figures 9 and 10). However, because the chokes must be sized for the full load current, they require a non negligible volume that is unavailable for the finger power supply.

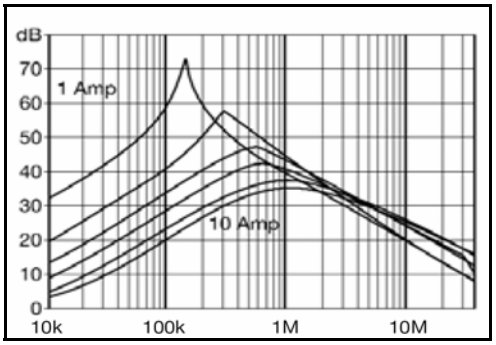

Figure 8: attenuation chart for typical common mode chokes.

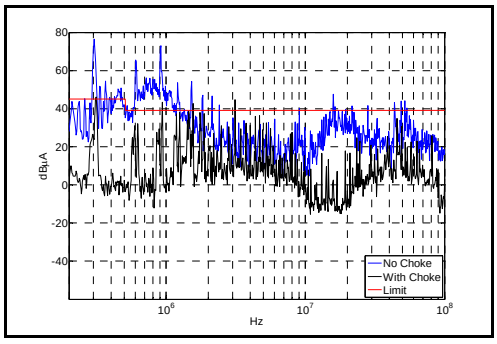

Figure 9: with a 10A common mode choke the single output common mode current is 20 dB below the ATLAS limit.

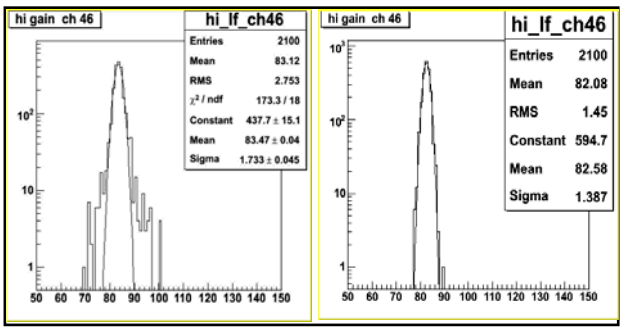

Figure 10: a common mode choke allows recovering the Gaussian property of the high gain fast readout pedestals distribution and its RMS to less than 1.5 counts.

As an alternative, a combination of carefully selected ferrites placed on each low voltage pair allowed to block significantly the common mode current too. The impedance curve of the selected ferrite exceeds 50 Ω between 3 MHz and 500 MHz (figure 11). The addition of two ferrites on the output of each converter allows the attenuation of its common mode current by up to 20dB between 1 MHz and 100 MHz (figure 12). The RMS of the pedestals distribution is improved and the Gaussian property is recovered (figure 13).

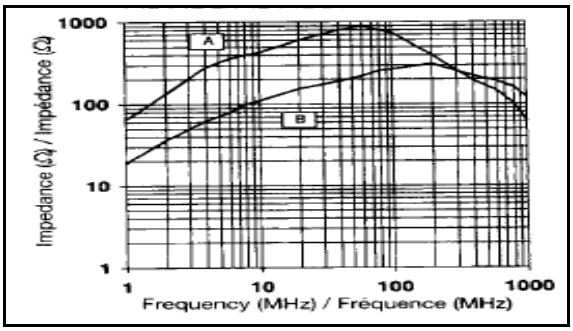

Figure 11: typical ferrite impedance curve for one turn (B) and two turns (A).

It must be noted that the ferrites are only effective above a few MHz, while the chokes offered an extended attenuation down to 100 kHz. However the results are very similar: therefore the drawer electronics is susceptible to high frequency noise above 1MHz, and the switching noise only plays a secondary role in the noise performance.

The power supply must operate in the presence of a magnetic field. No degradation of the ferrite properties was observed when exposing the ferrites to a nominal magnetic field of 200 Gauss.

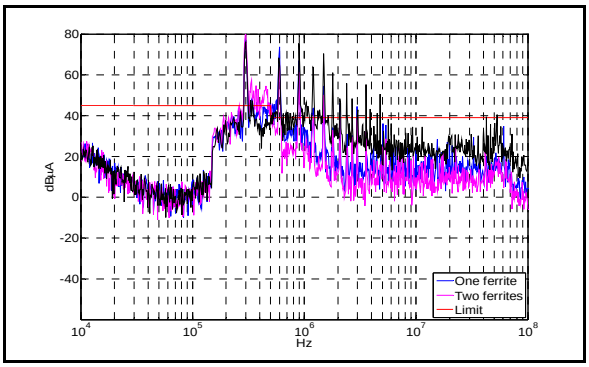

Figure 12: single output attenuation using one (blue) and two ferrites (pink).

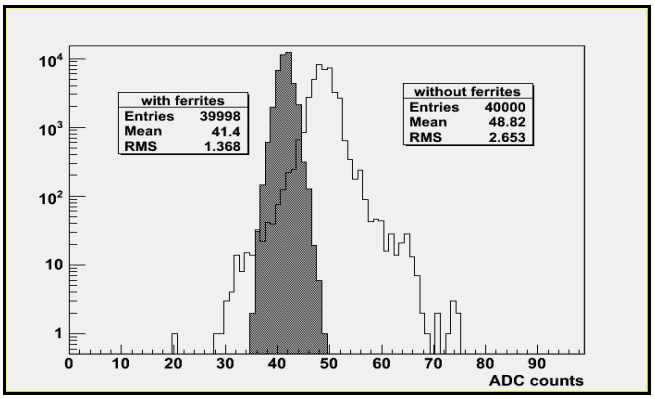

Figure 13: recovery of Gaussian distribution of pedestals using two ferrites on all low voltage outputs.

C. *Low frequency noise susceptibility.*

The slow integrator system of the drawer electronics is designed to scan the average current of the 45 front-end photomultiplier tubes at a rate of 100 Hz. This system turned out to be sensitive to low frequency noise (below 10 kHz) on the low voltage power lines. In this frequency range the differential mode noise dominates in the form of voltage ripple. The correlation factor (Equ. 1) between the distributions of integrators pedestals for two different channels put in evidence the presence of a periodic, low frequency ripple that is added to the sampled voltages.

$$\rho_{i,j} = \frac{\mathrm{cov}(i,j)}{\sigma_i . \sigma_j} \qquad \text{[Equ. 1]}$$

Some lightly loaded (usually less than 10% of the nominal load) converters were found to operate in discontinuous mode, causing a ripple that was out of specification (figure 14). To reduce this ripple, the converter must operate in continuous mode. This can be achieved either by the addition of preload resistors (at expense of reduced efficiency) or with the reduction of the power range of the lightly loaded converters. The latter solution was successfully exercised with the reduction by a factor 2 of the switching frequency. The correlated noise of the slow integrators system was significantly reduced, as seen on the corresponding correlation charts (figure 15).

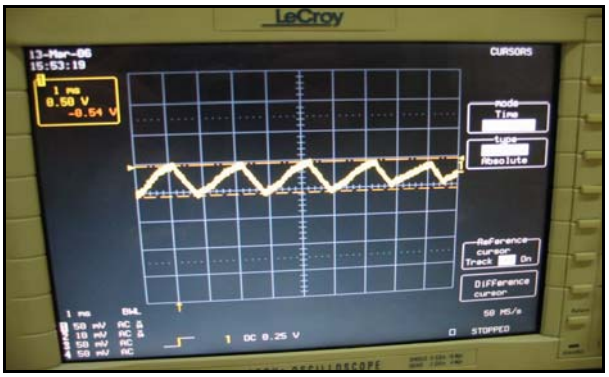

Figure 14: 500mV$_{pp}$, 500 Hz voltage ripple of a weakly loaded converter that operates in discontinuous mode.

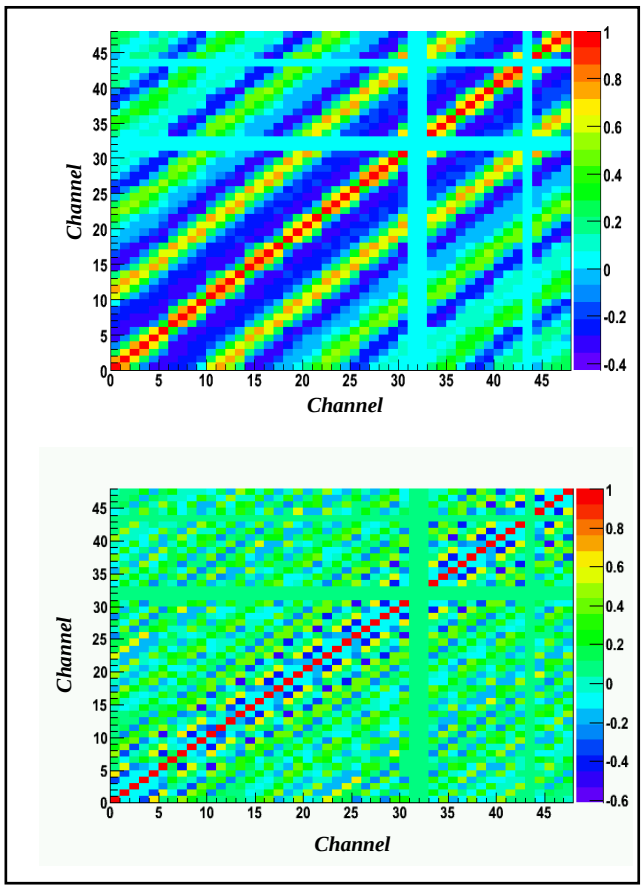

Figure 15: correlation charts of the slow integrators pedestals for a power supply operating in discontinuous mode (top) and in continuous mode (bottom).

CONCLUSION

The electrical and mechanical constrains set on the Tile Calorimeter low voltage power supplies imposed the need for compact, custom made switched mode converters.

The maximum noise that the Tile Calorimeter can afford is specified for the fast readout system and for the slow calibration and monitoring system. The custom made power supply must be compatible with these system noise specifications.

The front-end electronics of the Tile Calorimeter turned out to be very sensitive to high frequency common mode current on the low voltage lines. Noise currents 20 dB below the limits commonly in use in ATLAS are needed to achieve the required performance. The addition of common mode filters on each converter output is needed to reduce the common mode current to an acceptable level.

One obtains the best fast readout noise performance with the addition of common mode chokes on each converter output. Those are however too bulky for the envelope of the power supply. Instead of this, the addition of two ferrites on each low voltage pair of cable between the power supply and the drawer was exercised. It appeared to be effective to block the high frequency common mode currents and to achieve the required noise performance.

The slow calibration and monitoring system is sensitive to the ripple on the low voltage lines. Correlation charts put in evidence the presence of low frequency ripple in the system. To maintain the ripple within specifications, the power range of the converters that deliver less power is reduced in order to raise their operating point into continuous mode. For this the switching frequency of these converters was reduced to half of its initial value.

The noise properties of the DC/DC converters were compared with the susceptibility of the fast and slow readout electronics. From this a noise coupling model was established, and different filtering solutions were exercised. Among those, the use of ferrites and common mode decoupling capacitors appeared to be most suitable method that allows operating the front-end electronics within the detector noise specifications.

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Parallel Session B7

DAQ session

Production Test Rig for the ATLAS Level-1 Calorimeter Trigger Digital Processors

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Abstract

The Level-1 Calorimeter Trigger is a digital pipelined system, reducing the 40 MHz bunch-crossing rate down to 75 kHz. It consists of a Preprocessor, a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce electron/photon, tau, and jet trigger multiplicities, total and missing transverse energies, and Region-of-Interest (RoI) information. Data are read out to the data acquisition (DAQ) system to monitor the trigger by using readout driver modules (ROD). A dedicated backplane has been designed to cope with the demanding requirements of the CP and JEP sub-systems. A number of pre-production boards were manufactured in order to fully populate a crate and test the robustness of the design on a large scale. Dedicated test modules to emulate digitised calorimeter signals have been used. All modules, cables and backplanes on test are final versions for use at the LHC. This test rig represents up to one third of the Level-1 digital processor system. Real-time data between modules were processed and time-slice readout data was transferred to the ROD at a trigger rate up to 100 kHz. Intensive testing consisted of checking the readout data by comparing to hardware simulations of the trigger. Domains of validity of the boards were also measured and dedicated stressful data patterns were used to check the reliability of the system. Tests results have been successful and the Level-1 calorimeter trigger system is proceeding to full production.

I. THE ATLAS LEVEL-1 TRIGGER SYSTEM

The ATLAS trigger chain is a three-level system designed to reduce the raw rate of 1 GHz of proton-proton interactions and 40 MHz beam-beam bunch crossing to ~100 Hz [1]. The first level, or Level-1, selects interesting events down to 75 kHz within a total latency of 2 μs. It provides Region-of-Interests (RoIs) to the Level-2 to build a decision at a rate of 1000 Hz. The third level stores data at the final rate of ~100 Hz.

The ATLAS Level-1 trigger works on a reduced-granularity data from the calorimeter and muon systems. The calorimeter trigger is based on trigger-towers, covering calorimeter cells of 0.1 x 01 in η x ϕ. Potentially interesting events are selected by identifying electron/photon candidates, jets, single-hadron/tau candidates, missing transverse energy, and total transverse energy. Muon candidates are selected with a separate trigger. Informations from both of these system are combined and sent to the Central Trigger Processor where the decision to accept or reject the event is made.

The algorithm of event selection of the ATLAS Level-1 calorimeter trigger system is hardware implemented, with the use of FPGAs to allow flexibility. All board designs have been tested thoroughly, but before launching the full production, a first set of boards were built in order to test the robustness of the design in a heavy populated environment. An adequate number of pre-production boards were manufactured to fully populate a crate, corresponding to ¼ of the final Level-1 Calorimeter Trigger system. Peripheral modules were built to source data of such a subsystem. The development of such a test rig is a vital tool to check the quality of the boards as they will come from the manufacturer.

This paper will firstly describe the architecture of the ATLAS Level-1 calorimeter trigger system. A detailed description of the production crate test rigs will follow, and test results of the boards in such an environment will be presented.

II. THE ATLAS LEVEL-1 CALORIMETER TRIGGER ARCHITECTURE

The ATLAS Level-1 Calorimeter Trigger system consists of three subsystems, namely the Preprocessor (PP),

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electron/photon and tau/Hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP) (Figure 1) [2]. The CP and JEP will receive digitized calorimeter trigger-tower data from the Preprocessor, and send trigger multiplicity information to the Central Trigger Processor (CTP) via Common Merger Modules (CMM). A full description of the Preprocessor can be found in these proceedings. It consists of 124 Preprocessor Modules (PPM), which provide the input data for the CP and JEP system. Using Readout Driver modules (ROD), the CP and JEP will also provide RoIs and intermediate and final results to the data acquisition (DAQ) system for monitoring and diagnostic purposes. This paper refers to these latter subsystems, as described in more details in the following section.

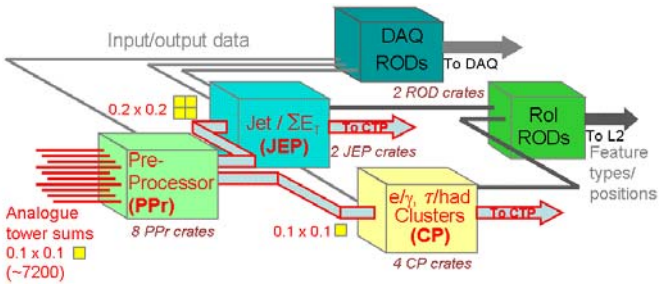

Figure 1 The Level-1 Calorimeter Trigger

III. The Cluster and Jet/Energy Processor

The CP and JEP system work at 40 MHz real time, and provide readout information on receipt of a Level-1 Accept signal.

A. *Real Time Data*

The CP system consists of 56 Cluster Processor Modules (CPM) shared between 4 crates. It identifies and count selectron/photon and tau candidates. The Jet/Energy Sum processor consists of 32 Jet/Energy Modules (JEM) shared between 2 crates. It counts jet candidates and form missing and total transverse energy sums. All final sums of cluster/jet candidates and total and missing energy are merged through 12 CMMs, with a layout of 2 CMMs for each processor crate.

Both systems received their input data from the Preprocessor using LVDS 400 Mbit/s serial 4-links chipset in order to reduce the I/O requirements on cables and pins. The total number of LVDS cables needed is 1888, each 12 m long. On top of the incoming data, large volumes of data are exchanged between neighbouring modules to accommodate the cluster and jet-finding sliding-window algorithms. A common custom backplane has been designed containing over 15000 pins, through which digital signals with speeds of up to 400 Mbit/s differential and 160 Mbit/s single-ended are propagated. Details of such a challenging backplane, design and production, are available in these proceedings.

In total, the CP and JEP process in real time around 550 GBytes/s of data, to reduce them down to ~0.05 GBytes/s toward the CTP to build the Level-1 decision.

B. *Readout path*

On receipt of a Level-1 decision, the CP and JEP send out DAQ and RoI data to 20 Readout Driver modules (ROD). Each ROD can process up to 18 input boards using optical links. The design is such that one ROD should read out one processor crate. A maximum data rate of 800 Mbit/s per link is achieved using Agilent G-link protocol [3]. Data is reformatted into standard ATLAS event fragments, and transmitted on optical links using the ATLAS S-link protocol.

IV. The Production Crate Test Rig

Although boards and backplane have their layout frozen and were ready to go to full production [4], their design has been approved on a scale of a few pre-production boards. The ATLAS Level-1 Calorimeter Trigger is mainly composed of custom made components, down to the backplane, and it was decided to test the robustness of the different design in a fully populated crate environment. A set of additional boards were produced corresponding to a ¼ of the final CP and JEP system.

Calorimeter signals being not available, emulator boards have been designed to deliver the equivalent LVDS calorimeter data needed. These so-called LVDS Source Modules (LSM) have a topology such that each individual board matches a digital board of the CP or JEP system. The final ATLAS LVDS cables were used to connect the LSMs to the modules under test. A total number of 300 cables have to be routed from the LSMs to the backplane. A picture of the setup in the laboratory is shown in figure 2. The table 1 lists the different hardware components used to build such a test system. The crate was equipped with a CPU mounted on an adaptor board to match the custom backplane crate, and a custom board, the Timing and Control Module (TCM), to broadcast the clock to each individual module. The TCM also provided an external CANbus to interface with the DCS system of ATLAS.

Components	Number
LSMs	16
CPMs	14
JEMs	7
TTCrx	30
OPTICAL CABLES	18
LVDS CABLES	308

Table 1 List of Components for the production crate test rig

Since the beginning, all tests of prototypes and pre-production modules used the ATLAS online software. It was easily expandable to such a large scale by just adding the new components in the database files. A simulation program down to the bit level was successfully run to validate the data processed by the hardware.



Figure 2 308 LVDS cables installed at the back of the backplane

V. TEST RESULTS

A. *Cluster Processor Modules*

A total number of 14 CPMs were tested in the crate (figure 3). Stress patterns of alternating words were send to check the stability of the LVDS. Parity correct data were processed, and no parity errors were observed on input or across the backplane after 5 hours of running.

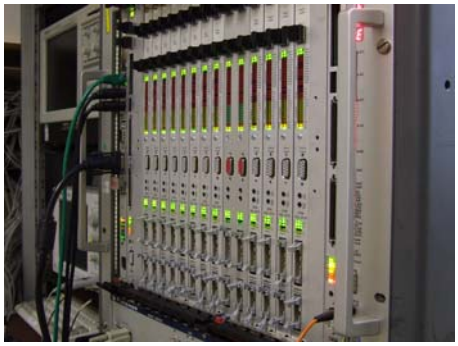

Figure 3 A crate with 14 CPMs

Figure 4 shows the parity-error-free timing window measured on one board, for 8 of the most demanding FPGA chips processing single-ended 160 Mbit/s signals. A window of around 2 ns has been measured, similar to what was measured with just a few boards in the crate.

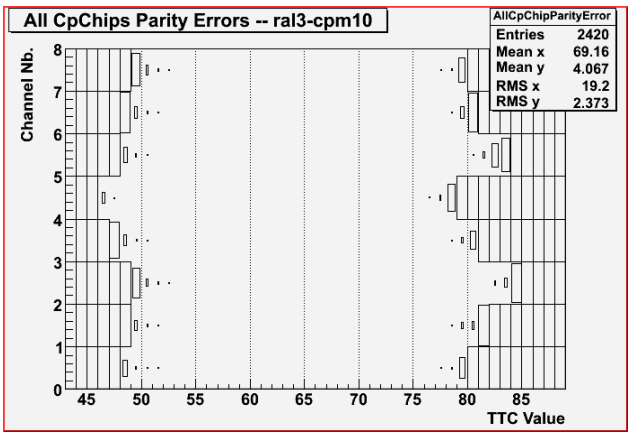

Figure 4 Parity error free timing window for 8 FPGA chips on the CPMs

A power consumption of 1 kW per crate has been measured, but this value is data patterns dependant. Dedicated test pattern with a programmable ATLAS occupancy rate have been sent into the system to explore its limits. Figure 5 shows that for a 10 % ATLAS occupancy rate, the total current of the crate is around 200 A at 5V. Higher occupancy has been used and the total current stays well below the maximum current supply of 300 A. During a run, individual sensors from the on-board FPGAs have been read out, with temperatures around 45 ^{o}C for the biggest parts. The values of their currents were within specification.

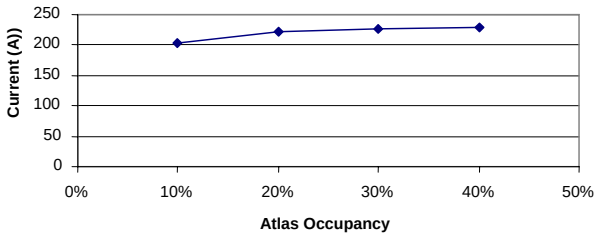

Figure 5 Current consumption as a function of the ATLAS occupancy rate

B. *Jet Energy Modules*

Seven Jet Energy processor boards have been used to populate a crate, completed with a set of 8 CPMs. A full crate of JEMS would have already been half of the final JEP system, so such a mixed configuration was a good compromise to test the JEM design within a noisy environment.

Similar test as with the CPM were performed, and stability of the LVDS links were checked over several hours of run. Unlike the CPMs, JEM data are not parity protected, and dedicated firmware was produced to test the stability of the data across the backplane. After 5-hour run, no data errors were detected across the backplane.

C. *Common Merger Module*

The crate was equipped with two common merger modules. Hit information, energies and jet informations are send through the backplane, and gathered by the CMMs before being sent to the CTP. Data are parity protected, and no parity errors were detected after 5-hour run on backplane inputs. A timing investigation of the data was performed using 14 CPMS as a source of data, and a parity error free window of 10 ns was recorded as shown on figure 6.

D. *Readout Driver*

The availability of several optical G-link transmitter from the boards in the crate was a good test bench for exercising the multitude of inputs of the ROD. A total of 16 G-links (due to a hardware problem, the 2 bottom links were not available) were therefore connected to the ROD, and no parity errors or link down were observed after 1 hour of run with a Level-1 Accept rate around 80 kHz. Event fragments from 5 CPMs were also compared to simulation, and a total number of 200K events were successfully processed before the software analysis stopped.

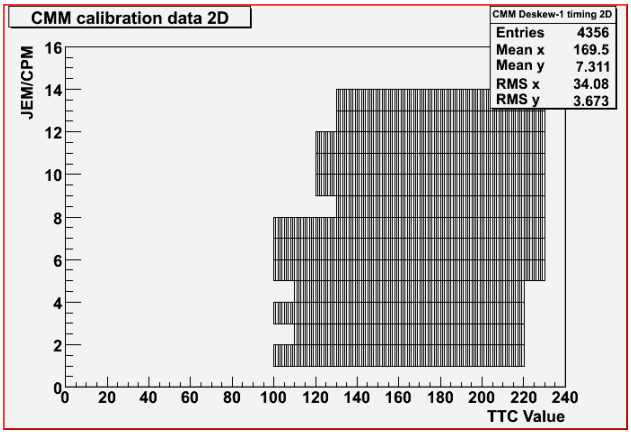

Figure 6 TTC scan of 14 CPMs on the CMM input

E. DCS

The external CANbus was connected to a DCS standard Kvaser card. The ATLAS Level-1 Calorimeter Trigger is not using the ELMB but it still has to provide the slow control information using the CANOpen protocol. Firmware was successfully written and tested, and values of voltages, currents and temperatures of 13 boards were correctly read out using the CANOpen format. Preliminary S/W using the PVSS environment was running, and figure 7 shows an example of the temperature map along the crate. Each column represents one board, and each square represent the color-code temperature of the 8 biggest FPGA chips per CPM. One board was not loaded with the microcontroller F/W, and its equivalent dark column corresponds to no data available. In addition, alarm controls were also implemented and tested by decreasing the thresholds of warning (such as current level). It was checked that the crate was switching off accordingly.

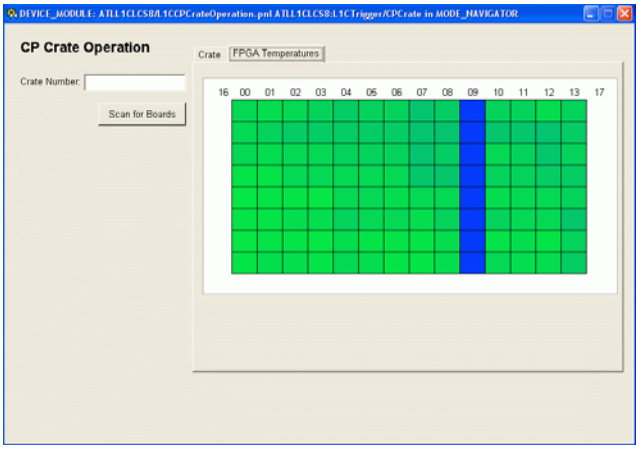

Figure 7 An example of the temperature profile across the crate for 14 CPMs

Such a feature is vital when testing a board for a long run without requiring the presence of a person nearby.

VI. Conclusion

The crate test has been successful in validating the final design of the digital modules of the ATLAS Level-1 Calorimeter Trigger Processor. Problems met and not reported in this note, were corrected in the comfort of the laboratory rather than in the ATLAS pit. Power consumption of the crate has shown that the system is not running on the edge, and currents and temperature measurements show that the components are well inside their specifications.

Boards are now in full production, and will be installed progressively at CERN as they arrive from the manufacturer.

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The Hardware of the ATLAS Pixel Detector Control System

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Abstract

The innermost part of the ATLAS (A Toroidal LHC ApparatuS) experiment will be a pixel detector, built of 1744 individual detector modules. To operate the modules, readout electronics, and other detector components, a complex power supply and control system is necessary. The specific powering and control requirements are described, along with the custom made components of our power supply and control systems. These include remotely programmable Regulator Stations, the power supply system for the optical transceivers, several monitoring units and the Interlock System.

I. Introduction

Being the first sub-detector to be passed by particles coming from the interaction point, the main goal of the pixel detector is to reconstruct secondary vertices, such as present in B decays.

In order to do so, the pixel cells have a size of 50 µm x 400 µm, with 46080 pixels forming one detector module. In the central part the modules are loaded on 'staves', which are carried by three concentric shells, in the end caps the modules are mounted on three disks per side. Half staves and disk sectors with six or seven detector modules and individual detector modules are the relevant ensembles on which the power and control systems can act on.

A pixel module consists of the sensor itself and 16 read out chips, which are connected via bump bonds to the sensor cells and house the analog and digital part of the front end read out chain. The front end chips are supervised by the MCC (module controller chip) which is carried by a flex hybrid circuit attached on the top of each detector module. The data transfer is handled by optical links. While the opto board, the on detector part of the optical chain, sends the data, the BOC (Back of Crate) cards, located with a distance of ca. 100 m in the counting room, receive the data.

II. DCS-HW Requirements

Besides of the specific requirements for a special power supply or monitoring unit, there are some common aspects which must be considered for the design of all devices. The high power density inside the detector volume and the radiation tolerance, dependent on the location of the equipment, have impact on the construction of most of our components. Reliability, meaning any risks to the highly sensitive detector must be avoided, gains even further importance due to the fact that many components will be inaccessible over long terms.

Furthermore the design of our system is driven by the need to find a good compromise between the desire to control and tune small units of the detector individually and low costs on the other side.

Concerning the power supplies and all related monitoring units the ATLAS grounding scheme requires floating designs. Due to the radiation, which the front end chips and the detector sensors suffer during their lifetime, all power supplies must have adjustable outputs. For safety reasons over-current protections and interlock inputs are also required for all power supplies.

As all hardware must be integrated into the pixel and ATLAS wide DCS (Detector Control System) the interfaces of the various components should be compatible to it. Therefore the ELMB (Embedded Local Monitor Board) builds the core of all our applications [1]. The ELMB is a multi-purpose acquisition and control unit, which owns a CAN (Control Area Network) interface. Its communication is based on the CAN-open protocol, which was chosen by ATLAS DCS for its reliability.

III. Overview of the DCS HW System

The DCS hardware system consists of (see Figure 1):

- the power supplies needed to operate the sensors, the front end chips and the opto boards,
- the Regulator Stations,
- temperature, humidity and current sensors,
- monitoring devices for the readout of the sensors,
- the Interlock System and
- the DCS PCs communicating with the HW.

Figure 1 shows the schematic, and in terms of the Interlock System simplified, overview of the DCS hardware.

The pixel power supply system consists of four major components [2]. To operate the front end electronics, two low voltages, Vdd and Vdda, are required. Delivered by the commercial W.IE.NE.R (Burscheid, Germany) power

supplies (PL512), the LVs are regulated closely to the detector by the use of the Regulator Stations. The high voltage (700 V, 4 mA), which depletes the sensors, is provided by the EHQ-F007n-F modules, built by iseg (Rossendorf, Germany). As the high voltage does not require any further regulation, it is sent directly to the detector elements. The related LV-PP4 (patch panel 4) and HV-PP4 units distribute the power and monitor the current consumptions. The opto boards are supplied by the SC-OLink (Supply and Control for the Opto-Link).

Monitoring of various temperatures and some humidity sensors is performed by the BBM (Building block Monitoring) and BBIM (Building Block Interlock and Monitoring) crates. While the first just provide a reading of values, the second additionally create logical signals, which are fed into the Interlock System.

All main power supplies mentioned above (LV, HV, SC-OLink) plus the off-detector part of the opto link, the BOC card, are connected to the hardware based Interlock System. This consists of several units that guarantee safety for human operators as well as for sensible detector parts.

Besides the LV crates, which are connected via TCP/IP all primary power supplies, Regulator Stations, monitoring crates and the Interlock System are connected to the DCS PCs via the CAN-Open protocol.

IV. Power Supplies

All power supplies are located in the counting rooms, where all cables are routed to [3]. This gives an easy access and more flexibility during operation. Additionally this frees from problems due to radiation. On the other side the large distance of more than 100 m between source and load gives need for a LV regulation as close as possible to the detector. The remotely programmable Regulator Stations protect the sensitive read out chips, developed in deep sub-micron technology, against transients. In parallel they allow an individual tuning of each detector module to its optimal operation conditions.

While the LV and HV power supplies deliver the power for half staves, respectively disk sectors the related PP4 units split the primary output onto lines, which connect to each detector module individually. Additionally these PP4 crates provide a current monitoring for single detector modules. In this way a good compromise between the costs for hundreds of power supply channels and maximal available information is found.

The HV and LV power supplies are commercial systems, the Regulator Stations and the SC-OLink are custom made.

A. Supply and Control of the Opto Link

To operate one opto board three different voltages and one control signal are required, these four outputs build one complex SC-Olink channel [4]. While Vvdc (10 V, 800 mA) supplies the transceiver chips as well as the transmitter diode, the receiver diode requires an additional supply voltage Vpin (20 V, 20 mA). Viset (5 V, 20 mA) is used to adjust to operating point of the transmitter diode and the control signal, the fourth output, (2.5 V, 10 µs) allows to send a reset signal to the receiver control chip. In total 272 complex channels are required.

Usage of a single channel DAC (MAX5122, 12 bit), controlled by the ELMB, allows one to adjust the output voltages. Isolation of the floating outputs is given by transformers and opto couplers in all control and monitoring lines. As the DACs are powered separately, the output voltages remain unaffected if a power cycle of the CANbus for resetting the ELMBs is necessary. The precision for setting and monitoring is better than 0.5%. Additionally all channels own a hardware current limitation and there is one interlock input per complex channel.

B. Regulator Station

To protect the integrated circuits of the front end chips, that are manufactured in deep sub-micron CMOS technology, against voltages surges or spikes, a remotely programmable regulation station capable of providing individual floating power output with low ripple has been designed. The station is more 10 m away from the detector, and each FE line is continuously ‘sensed’ down at the module to promptly adjust the output voltages. One regulation station can power up to 84 modules (Vdda, Vdd, Vvdc) and communicate with the ATLAS Detector Control System via a CAN bus interface.

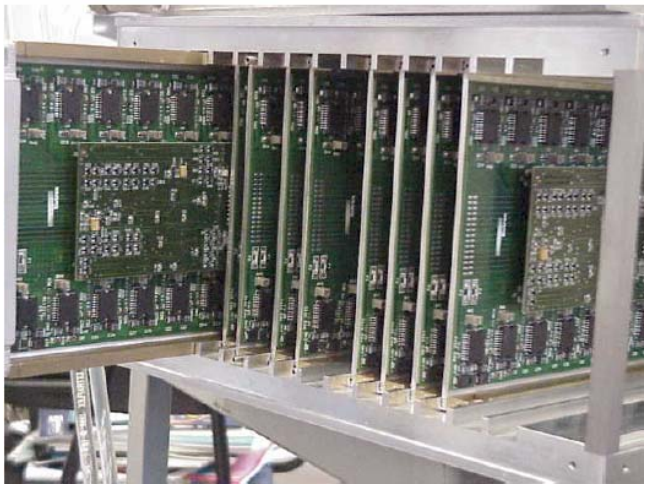

Figure 2: the Regulator Boards, each board is composed by a motherboard and a daughter board

The core of the Regulation Stations are printed circuit boards built on a highly dissipative substrate (approx. 10 W/board), see Figure 2. Each board houses 16 ST rad-hard voltage regulators (LHC4913+) and provide about 1 A at 2 V with 10 mV regulation step, around the typical range of operation of the front end electronics (~ 2 V, ~1 A). All channels are floating up to ± 10 V. Programmable digital trimmers are addressed by control signals that are opto coupled to preserve isolation. Channels can be inhibited individually or per board while kept floating. Further safety is given by a current compensation on each channel and a protection of the output voltages against accidental disconnection of the sense lines.

All adjustment and monitoring functions in a Regulator Station are supervised by one controller board, which is based on a FPGA (APA075 from ACTEL, Mountain View CA, USA). The FPGA can be reprogrammed via CAN bus to facilitate operation during the ten year operation of ATLAS. The need for programming the FPGA on demands derives from the fact that a degradation of the performances of the front end electronics is expected during the life of the experiment. The full system has been irradiated and is rad-tolerant up to a NIEL > 10^{12} 1 MeV n_{eq}/cm^2.

V. Monitoring

A. Low Voltage Monitoring

A distribution of the low voltages is required as six or seven detector modules are supplied by one LV W.IE.N.ER power supply channel each. This is performed by the patch panels no. 4, which are installed in direct vicinity to the LV crates. To have full information about the health of each detector module an additional current measurement per detector module is available. For debugging the system, especially to trace grounding problems, the current of the in- and output lines can be measured.

The core of the LV-PP4 are ELMBs. As done for the SC-Olink the use of opto isolators decouples the measuring circuits, which reach a precision of 2 – 10 mA for a measuring range between 0 and 2 A.

The construction of LV-PP4 is driven by the layout of the services, therefore each LV-PP4 block can handle up to 28 supply lines and 56 measuring channels. The measuring channels are grouped in the way, that a second card housing further op-amp and opto couplers can be added if the measurement of the return current becomes necessary. All together LV-PP4 will consist of 3500 up to 7000 monitoring channels (when all currents and their returns are measured).

B. High Voltage Monitoring

As the required depletion voltage will increase during the detector lifetime, the modularity of the HV system needs to be changed. This has not only effects on the total number of HV power supplies needed, but also on the mapping of the power supply channels to the detector modules, which is performed by the HV-PP4 crates.

A HV-PP4 is therefore not only capable of a current measurement of the HV-lines at a single module level (by the use of ELMBs), but it is also responsible for the correct mapping of the iseg HV channels to the detector modules. 16 HV-PP4 crates will be required for the experiment, each with up to 117 monitoring channels. The strongly varying depletion current requires a large dynamic range of 0.4 mA to 4 μA for these measuring circuits.

C. Building Block Monitoring

About 2000 temperature sensors are required inside the pixel DCS. We have chosen 10 kΩ NTC (negative temperature coefficient) thermistors, as they combine radiation hardness (up to 10^{15} n/cm²), a large relative change of their resistor of 4 %/K and small SMD casings (0603). Also the humidity sensor, Xeritron (from Hygrometrix, Alpine CA, USA) is chosen because of its radiation hardness.

While the signals of the temperature sensors mounted on the detector modules, opto boards and Regulator Stations are fed into the monitoring and Interlock System, see next section, all pure monitoring is handled by the BBM (building block monitoring) crates [5]. This includes the humidity sensors and all temperature sensors which are additionally installed inside the pixel volume.

The core of each BBM is again an ELMB which is used for the data readout. Its input circuitry is specially adapted to supply NTC and Xeritron sensors and to handle their signals.

VI. Interlock System

While the normal operation of the detector is steered by the DCS software, all safety relevant situations are handled by the Interlock System. In order to prevent damages to human beings or important parts of the detector, the hardware Interlock System is able to switch down all necessary power supplies and to operate completely independent from the rest of the control system.

Due to the dense circuitries of the front end chips the power consumption inside the detector volume is very high. As heat ups of the detector modules lead to a faster ageing or can cause severe damages to the detector, their temperatures are being monitored and in parallel the signals are lead into the Interlock System. As over temperature is a risk to opto boards and Regulator Stations as well, these units are also controlled by the Interlock System.

The risks of accidents involving humans refers to the damage potential to the eyes given by the infra-red lasers of the opto links. Therefore all lasers have to be switched off immediately once one of the fibre connectors at the detector or counting room side are opened.

In case of emergency the smallest necessary subset of power supplies is switched off in order to allow the rest of the detector to remain operational. In total the system handles 2150 incoming interlock signals and acts on 1100 interlock controlled devices. All circuits are built in negative logic; as soon as a cable is disconnected the related equipment is interlocked. An overview on the Interlock System is given in Figure 3, its components are described in more detail below [6].

A. Building Block Interlock and Monitoring

The BBIM (Building Block Interlock Monitoring) crates receive the module, opto board and Regulator Station temperatures as analogue voltages. These are digitized by comparator circuits, called Interlock Board, with exchangeable threshold plug-ins which allow to adapt to the needs of the different equipment.

The digital information is then sent as TTL signals to the Logic Unit. In parallel the BBIM crates house ELMBs that monitor the temperatures and deliver the information to the DCS software.

As the processing of the analogue signals should be close to the detector, the BBIM crates are mounted in the radiation

environment of the ATLAS cavern. Therefore all components of the Interlock Board have undergone intensive radiation tests and the required radiation tolerance criteria of 93 Gy and 5 x 10^{11} n/cm^2 (1 MeV) were reached.

B. Logic Units

The LUs (Logic Unit) combine all the incoming signals from the BBIM crates, the PP1 Boxes, the BOC-I-Box and the DSS (Detector Safety System) into logical interlocks with a granularity of half staves, respectively disk sectors. While the BBIM crates deliver the temperature alarms, the PP1 Boxes are sending signals when a part of the optical laser driven read out system is opened. Additionally DSS, an ATLAS wide system, provides an interlock signal in case of more general alarm conditions like smoke or failures in the cooling system.

Core of the LU is a FPGA (APA075) that is able to determine the current situation from the inputs and raises the corresponding interlock alerts.

Although the Interlock System is purely hardware based, it is required to communicate and explain the interlock actions to the rest of the DCS. This is realized by the use of ELMBs within the LU that read out the incoming signals and report them to DCS. In addition, the digital outputs of the ELMB are used to provide test signals to the Interlock System.

C. Interlock Distribution Boxes

The IDB (Interlock Distribution Box) receives the logical interlock signals on the granularity level of no more than seven modules and distributes the interlock signals to the connected power supply channels in order to switch off the smallest possible subset of power supply channels.

Therefore the IDB has to take the correct mapping of the power supplies into account which is especially difficult due to the fact that the modularity of power supply channels connected to detector modules changes during lifetime (HV). Further the number of power supply channels per crate is different for LV, HV and SC-OLink and cabling might change when e.g. single channels are broken. The needed flexibility is achieved by the use of another FPGA (APA075).

An ELMB is used for the monitoring of the interlock signals, outgoing to the power supplies. The combined information of the LU, IDB, PP1 and BOC-I-Box ELMBs ensures a consistent monitoring of all interlock activities.

VII. SUMMARY

The requirements of the pixel detector have made specific developments necessary for the hardware components of the power supply and detector control system.

An efficient operation requires a preferably individual adjustment of the different control parameters. Further design constraints are the high power density in the detector volume, the floating grounding scheme of the ATLAS detector and the sensitivity of the read out chips developed in deep sub micron technology. Especially the power supply system, consisting of nearly 5000 individually controllable supply lines, requires solutions which are adapted to the detector needs and which in parallel are economically priced.

The remotely programmable Regulator Stations, which are installed as close as possible to the detector modules, provide individual floating power outputs with low ripple to the front end electronics. At the same time they protect the sensitive chips against transients. The internal control of the Regulator Station is handled by a FPGA from ACTEL, while the link into the control system is handled by the ELMB, the ATLAS wide used front end IO unit.

The design of the supply system for the opto transceiver boards is based on components, which can directly be controlled by the ELMB. In this way a reasonable priced solution has been found which allows individual setting and adjustment for each of the more than thousand channels.

In the positions where common power supplies are used to provide voltages to several loads, additional monitoring units are integrated which allow to investigate the behaviour of individual modules. The design constraints, precision and compatibility to the ATLAS grounding scheme, are fulfilled by the presented LV monitoring system. In the final system more than 8000 monitoring channels complete the low and high voltage system.

As especially irradiated detector modules are very sensitive to temperature increases or can even be destroyed by heat ups, a thermal Interlock System is developed which acts directly on the related power supplies. In addition other equipment can suffer from extreme heat and human being must be protected against risks due to lasers. Therefore these devices are connected to the Interlock System as well. The presented interlock matrix, whose design is based on the use of FPGAs, allows a dedicated control of small equipment groups and helps in this way to keep the number of channels out of service as low as possible.

The presented hardware components passed intensive electrical studies and investigation in our system tests and are currently under production.

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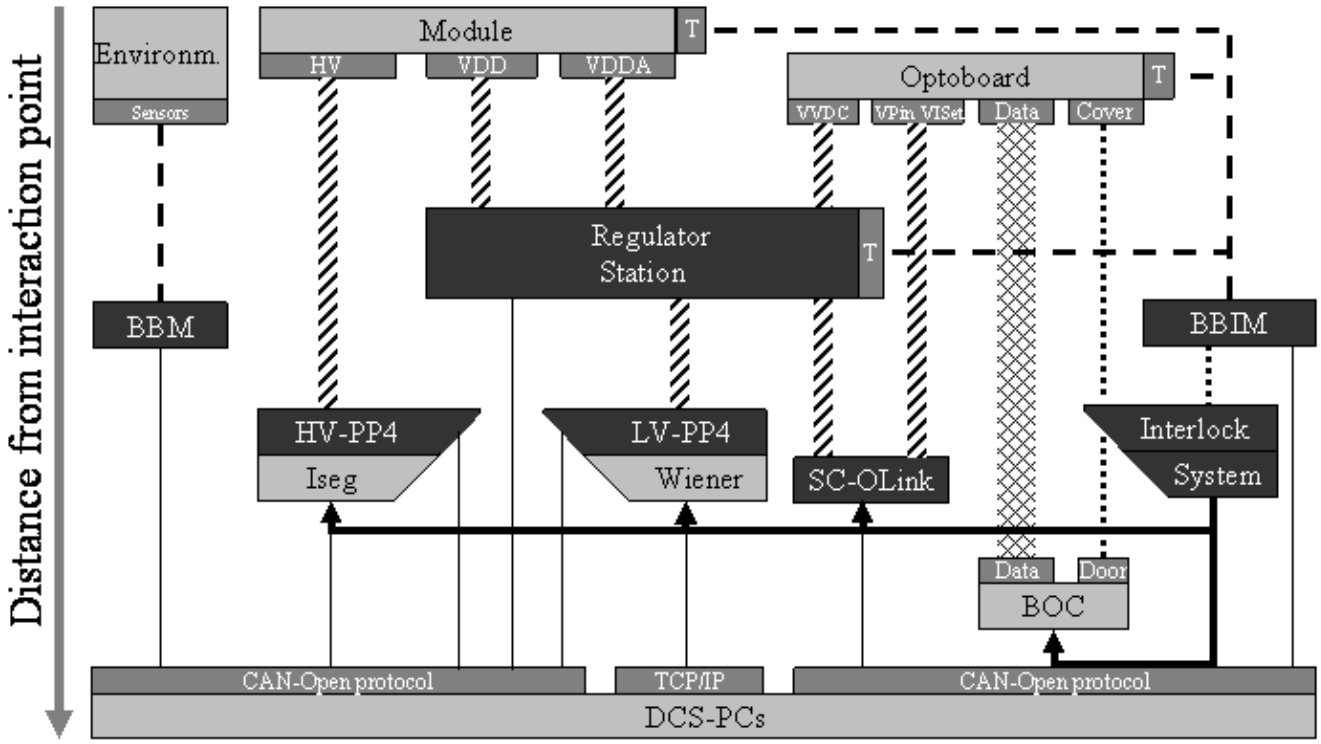
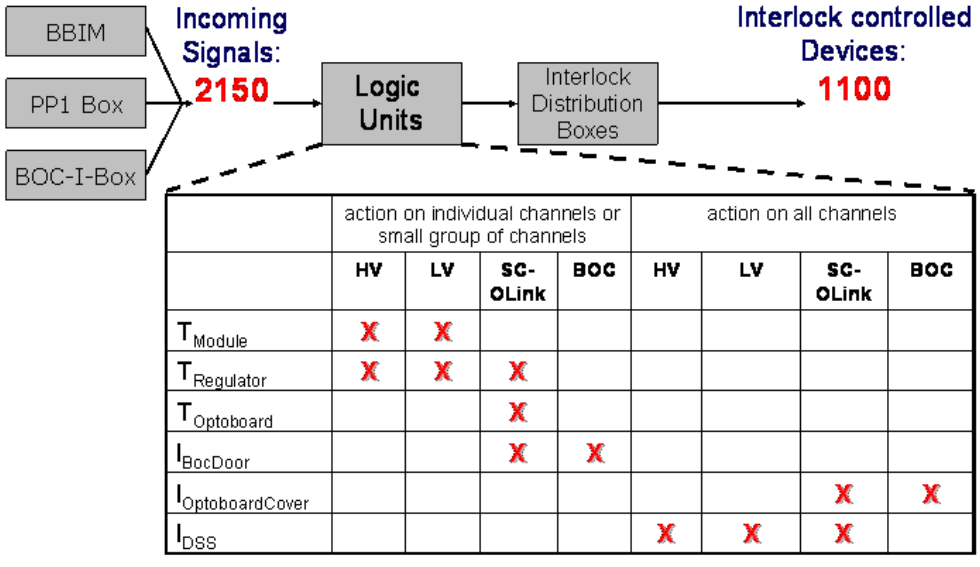


Figure 1: Overview of the DCS hardware (Interlock System simplified)



	action on individual channels or small group of channels				action on all channels			
	HV	**LV**	**SC-OLink**	**BOC**	**HV**	**LV**	**SC-OLink**	**BOC**
T_{Module}	X	X						
$T_{Regulator}$	X	X	X					
$T_{Optoboard}$			X					
$I_{BocDoor}$			X	X				
$I_{OptoboardCover}$							X	X
I_{DSS}					X	X	X	

Figure 3: Schematic overview of the Interlock System and the action matrix

Algorithms for the ROD DSP of the ATLAS Hadronic Tile Calorimeter

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Abstract

In this paper we present the performance of two algorithms currently running in the Tile Calorimeter Read Out Driver boards for the commissioning of ATLAS. The first algorithm presented is the so called Optimal Filtering. It reconstructs the deposited energy in the Tile Calorimeter and the arrival time of the data. The second algorithm is the MTag which tags low transverse momentum muons that may escape the ATLAS muon spectrometer first level trigger.

Comparisons between online (inside the Read Out Drivers) and offline implementations are done showing an agreement better than 95 % for the Optimal Filtering algorithm and up to 85 % for the MTag algorithm. The processing time was measured for both algorithms running together with a resulting time of 29.4 μs which, although above the 10 μs of the first level trigger, it fulfills the requirements of the commissioning trigger (~ 1 Hz). We expect further optimizations of the algorithms which will reduce their processing time below 10 μs.

I. Introduction

The ATLAS detector (see Figure 1) is a general purpose experiment designed to exploit the physics discovery potential of the next proton-proton collider at CERN, the Large Hadron Collider (LHC).

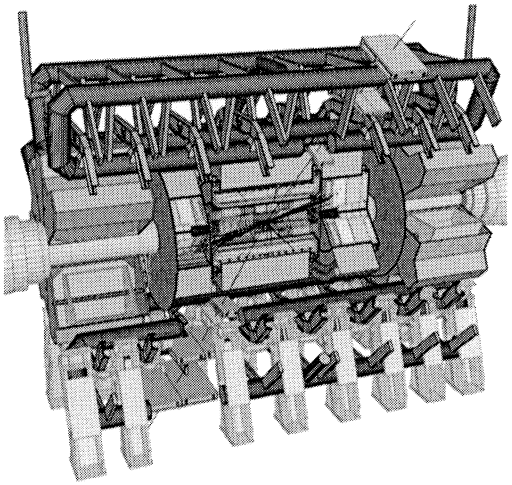

Figure 1: ATLAS detector.

The ATLAS hadronic Tile Calorimeter (TileCal) [1] is a sampling calorimeter made out of iron as absorber material and plastic scintillating plates as active medium. The light produced in the scintillating tiles is collected through wavelength shifting fibers and read-out by photomultipliers. The analogue electrical signal of the photomultipliers is digitized in samples of 10 bits taken each 25 ns, the latency between two consecutive LHC bunch crossings. Therefore, the ~ 10 000 photomultipliers of the calorimeter produce up to ~ 164 Gbps of data that is readout by the TileCal back-end electronics.

The main element of the back-end electronics is the Read Out System [2]. This system is composed of 32 Read Out Driver (ROD) boards (see Figure 2). The RODs are based on a custom 9U VME64x board equipped with up to four Processing Units (PUs) which are pluggable daughter-boards. The PUs process the data coming from TileCal front-end to feed the second level trigger with information of energy deposited in the calorimeter and other relevant quantities.

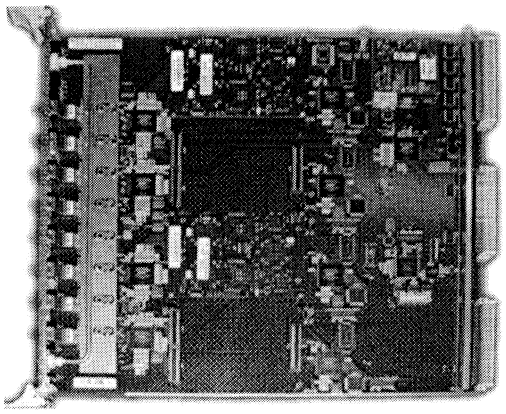

Figure 2: ROD motherboard.

The PUs are equipped with the TMS320C6414x™ Digital Signal Processors (DSPs) of Texas Instruments in order to execute reconstruction algorithms in real time. The latency of the second level trigger is 10 μs which sets stringent requirements on the processing time of the reconstruction algorithms.

In this paper we present the performance of two algorithms implemented in the DSPs. We propose an algorithm for

the energy reconstruction, the so called Optimal Filtering (OF) [3], which reconstructs the amplitude and time of the photomultiplier signal by means of weighted sums of the digital samples. Additionally, we propose a fast muon tag algorithm, named MTag, to identify low transverse momentum (p_T) muons that may escape the muon spectrometer. The tagging of these muons helps to trigger interesting B-physics channels.

Both algorithms have been tested online in the ATLAS commissioning with cosmic rays runs. The performance of both algorithms and the processing time required is presented in this paper.

II. Experimental Setup

Until 2007 the ATLAS detector is being commissioned in the ATLAS cavern. During this period all subdetectors will be progressively integrated into the final ATLAS Trigger and Data Acquisition system.

During 2005 and 2006, TileCal has been fully assembled in the underground experimental hall UX15. A program of cosmic rays data acquisition has been planned for TileCal in standalone mode. The trigger signal was provided by the TileCal trigger electronics, using custom coincidence boards which take as input up to 192 TileCal trigger tower analog signals [4]; half in the top part and half in the bottom part. A signal coincidence in the upper and lower part of the calorimeter triggers the data acquisition. (see Figure 3).

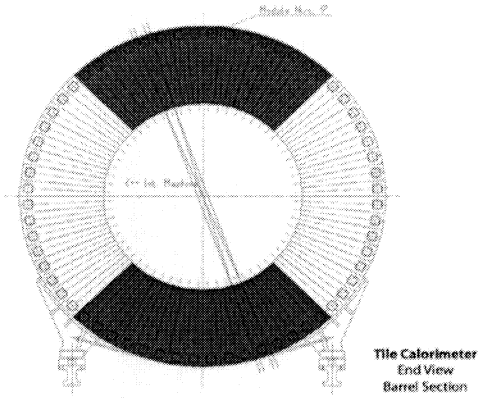

Figure 3: TileCal cosmic muon trigger.

The cosmic muon trigger is not synchronized with the data acquisition system and thus the arrival time of the events follows a flat distribution in a wide time window.

Our goal is to satisfactorily reconstruct the energy deposited by the muons and to check the efficiency of the MTag algorithm.

III. Algorithms

Both the Optimal Filtering and the MTag algorithms are implemented in the ROD DSPs which are the Texas Instruments TMS320C6414x™ DSPs. They are fixed-point processors which perform up to 32-bit data multiply and accumulate instructions. Their CPU contains only multiplier and ALU units; therefore divisions are not allowed and they are implemented as shift instructions, to divide in powers of 2, and with the use of look-up tables to implement more complex operations. Consequently the algorithms inside the DSP should reach a compromise between simplicity and accuracy.

A. Optimal Filtering

The Optimal Filtering algorithm reconstructs the amplitude and phase of a digitized signal by a linear combination of its digital samples, pedestal subtracted (see Eq. 1 and Eq. 2):

$$A = \sum_{i=1}^{n} a_i \left(S_i - p\right), \tag{1}$$

$$\tau = \frac{1}{A} \sum_{i=1}^{n} b_i \left(S_i - p\right), \tag{2}$$

where S_i represents the digital sample i and n is the total number of samples. We define the pedestal, p, as the baseline of the signal. The amplitude, A, is the distance from the pedestal to the peak and the phase, τ, is defined as the time between the central sample and the peak of the pulse (see Figure 4).

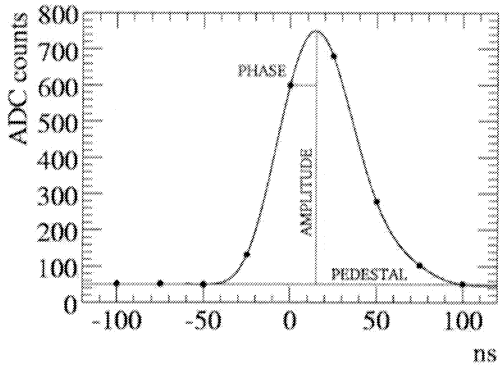

Figure 4: Definition of amplitude, phase and pedestal.

The weights, $\boldsymbol{a}$ and $\boldsymbol{b}$, are obtained from the pulse shape of the photomultipliers and the noise autocorrelation matrix. The process to calculate them minimizes the effect of the noise in the amplitude and time reconstruction [5].

These weights are calculated assuming small phases, which means that increasing τ the quality of the reconstruction decreases. This occurs during the TileCal commissioning since the data is not synchronized with the trigger clock. In order to properly calculate the energy deposited in the calorimeter during the commissioning phase we introduce one iteration in the OF algorithm to estimate the arrival time of the data, although this increases the processing time. Anyway, the expected trigger rate is $\sim$ 1 Hz which slows down the time restrictions.

During the first iteration, the amplitude and the phase are calculated assuming that the peak is close to the central sample, phase equal to 0 ns (see Eq. 3 and Eq. 4):

$$A_1 = \sum_{i=1}^{n} a_i \Big|_{\tau=0} (S_i - p)\,, \tag{3}$$

$$\tau_1 = \frac{1}{A_1} \sum_{i=1}^{n} b_i \Big|_{\tau=0} (S_i - p)\,. \tag{4}$$

This iteration gives a first approximation of the phase. In the second iteration the amplitude and the phase are again calculated assuming that the peak is now around τ_1 (see Eq. 5 and Eq. 6):

$$A_2 = \sum_{i=1}^{n} a_i \Big|_{\tau=\tau_1} (S_i - p)\,, \tag{5}$$

$$\tau_2 = \frac{1}{A_2} \sum_{i=1}^{n} b_i \Big|_{\tau=\tau_1} (S_i - p)\,. \tag{6}$$

Weights calculated for phases between -15 ns and 15 ns are stored in the ROD DSPs memory in order to use them during the iteration mechanism. The result of the second iteration, A_2 and τ_2, is used as input by the MTag algorithm.

B. Muon Tag

The primary goal of the MTag algorithm [6] [7] is to search for muons taking into account the energy deposited in each layer of TileCal. Figure 5 shows the TileCal cell structure with 3 layers (A, BC and D cells) and with a projective geometry in η. In order to identify the muons, the typical energy deposition in each cell is limited by a high and a low threshold:

$$thr_i^{\text{low}} \leq E_i \leq thr_i^{\text{high}} \qquad i = 1, 2, 3 \tag{7}$$

If this condition is fulfilled in each of the 3 layers with a projective pattern in η, the muon is tagged. In order to be efficient on events in where the muon loses a considerable fraction of its energy in one of the layers, muons are also tagged if Eq. 7 is fulfilled in two layers while in the third layer the energy deposition is above the low threshold.

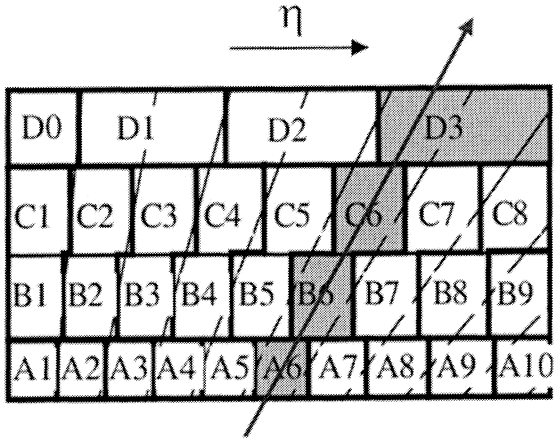

Figure 5: Muon path going through a tower in η.

The low energy threshold is meant to cut electronic noise and minimum bias pile-up events. In this algorithm, all cells have the same low energy threshold values. The high energy thresholds are meant to delimit the maximum muon energy deposition while eliminating hadronic showers and tails. These thresholds are determined for each individual cell, depending on the pseudorapidity of the muon trajectory.

The result of the MTag algorithm is the number of muons inside a TileCal module and the pseudorapidity where they were found.

IV. Results

During July and August 2006 several runs of cosmic rays were acquired and reconstructed online in the ROD DSPs. Figure 6 shows the histogram of the reconstructed amplitude in the ROD DSPs (online) and the offline reconstruction for all the operative channels during the acquisition. The large tail corresponds to energy deposited by cosmic muons, while the peak around zero corresponds mostly to electronic noise. The agreement between both reconstructions is larger than 99 % for amplitudes above 3σ of the noise. For amplitudes smaller than 3σ the difference between the online and offline amplitude reconstruction is expected to be larger. Eq. 4 shows that in order to calculate the phase at the first iteration we need to divide by the amplitude. In the ROD DSPs, this implementation is carried out by the use of a look-up table which decreases the resolution of the phase for amplitudes close to zero.

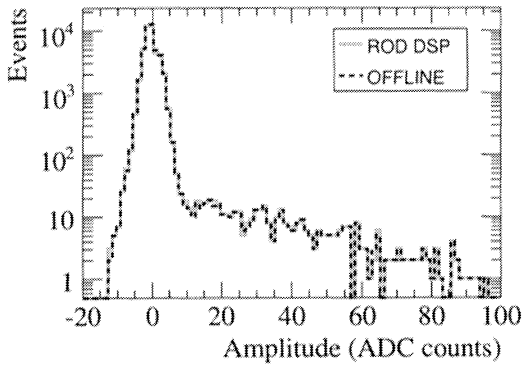

Figure 6: Reconstructed amplitude using Optimal Filtering, offline and inside the ROD DSPs.

Figure 7 shows the online and offline phase reconstruction for amplitudes larger than 3σ. The error of the phase reconstruction is larger than the error of the amplitude. This is due again to the use of look-up tables. The discrepancy with the offline result is ~ 5 %.

Figure 8 shows the energy distribution of the online tagged muons in the ROD DSPs using Optimal Filtering for the energy reconstruction. The results are compared with the distributions of the offline MTag algorithm using the Fit method for the energy reconstruction which is the standard offline algorithm.

Even though the energy taken as input of the offline MTag is slightly different from the online, up to 85 % of the offline tagged muons are also tagged in the ROD DSPs.

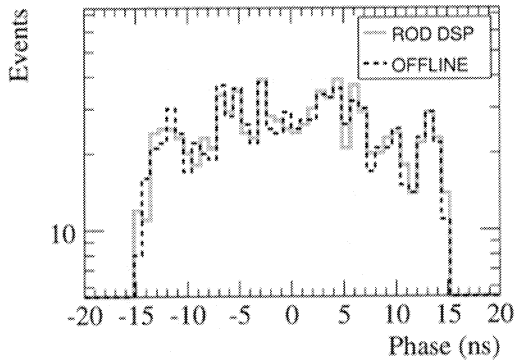

Figure 7: Reconstructed phase using Optimal Filtering, offline and inside the ROD DSPs.

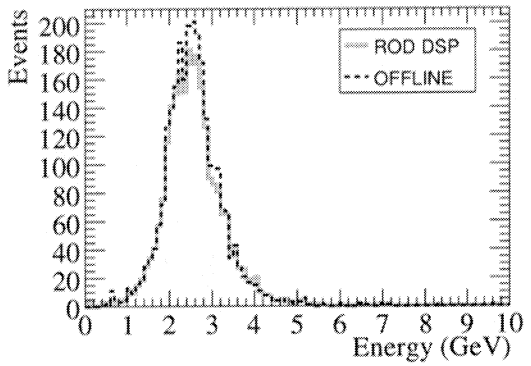

Figure 8: Energy distribution of the tagged muons, offline and inside the ROD DSPs.

The processing time of the online algorithms is a very important issue, since the latency of the first level trigger is 10 μs. However this maximum rate will not be achieved during the first years of the LHC operation and the rate of the cosmic muons acquisition is $\sim$ 1 Hz.

The DSP processing time has been measured in our laboratory (see Table 1). Globally these times are well above to 10 μs, however, the current implementation is coded in C and a great improvement is expected after migrating to assembler. Furthermore, the OF algorithm is adapted to the commissioning conditions and makes use of iterations. Nevertheless, in the final configuration, when timing is fixed with the LHC clock no iterations will be needed and the processing time will be reduced.

Table 1: ROD DSP processing time.

Algorithm	**Time (μs)**
OF	27.1
OF and MTag	29.4

V. Conclusions

During July and August 2006 the Optimal Filtering and the MTag algorithms were tested within the ATLAS commissioning environment. The results of their implementation in the ROD DSPs (online) and offline were shown. For the Optimal Filtering algorithm the agreement with the offline reconstruction was better that 99 % for events with amplitudes larger than 3σ of the noise; for the phase reconstruction an agreement of 95 % was found. The decrease of the online resolution was due to the use of look-up tables in order to implement the division by the amplitude. The results of the MTag algorithm analysis showed that up to 85 % of the offline tagged muons were also tagged in the ROD DSPs, even though the reconstruction algorithms were different.

The processing time was also measured for both algorithms running together with a result of 29.4 μs which is larger than the LHC final requirements (10 μs) but it still fulfills the requirements of the ATLAS commissioning which is $\sim$ 1 Hz.

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Optical Module Front-End for a Neutrino Underwater Telescope: PMT interface

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Abstract

A proposal for a new system to capture signals in the Optical Module (OM) of an Underwater Neutrino Telescope is described. It concentrates on the problem of power consumption in relation to precision. In particular, a solution for the interface between the photomultiplier (PMT) and the front-end electronics is presented.

I. INTRODUCTION

An Underwater Neutrino Telescope uses large area PMTs to detect the Cherenkov light from the muons generated by neutrinos in the seawater. The PMTs are put in a 17" glass sphere at 350 Atm pressure. The signals detected by PMTs must by suitable coded and sent on-shore. A mini-tower equipped with 16 OMs will be deployed in 2006 in front of Catania arbour as a first prototype. It uses a front-end electronics described in [1]. Three main problems are not yet successful resolved: power consumption, PMTs aging and signal dynamics. To overcome these problems a different front-end electronics is proposed.

The research and development work aimed at the developing the low-power front-end for the Optical Modules (OM) of the NEMO submarine neutrino detector [2,3,4] has led to the design of different ASIC prototypes for the development of the Trigger, photomultiplier (PMT) signal classification and fast sampling according to signal classification. Moreover, commercial ADCs and a FPGA, provide digital encoding, data packing and then data transfer towards the shore station for acquisition.

A board containing the PMT interface electronics, the ASIC, the ADC and the FPGA constitutes the OM front-end. By means of the FPGA, this board receives the slow control and transmits the measurements of environmental parameters such as temperature, humidity etc. together with the data.

The final version of the chip has been tested and the single blocks, constituing its architecture, that is, the analog memory, the trigger and single photon classifier and the clock frequency multiplier, have been characterised. The board to test the whole front-end together with the PMT is being prepared.

II. THE FRONT-END

The design of the front-end board and the chip, in particular, are based on parameters and specifications which in some cases are not yet definitive and restrictive, for the performance of the whole detector.

Recently data coming from simulations of high energy neutrino events produced in a submarine detector became available for analysis. These data provide the signals of all the PMTs in the detector in the presence of such events and take into account the ^{40}K background, the optical properties of the sea water, the orientation and position of the PMTs etc. Therefore, using these data, it was possible to define new specifications for the front-end electronics that optimise the detector performances from the front-end point of view. As a result a new architecture has been defined for the chip that performs the sampling.

This new device, called Smart Autotriggering Sampler (SAS), will be composed of functional blocks very similar to those already designed and succesfully tested. This will allow the performance of the blocks to be introduced into the simulations of the whole front-end making the results more significant and realistic[4]. The block diagram of the front-end under design is shown in figure 1. One fundamental part is the PMT interface with the board. It allows the de-coupling, amplification, filtering and delay of the signals, with low power dissipation and with the maximum design reliability and compactness.

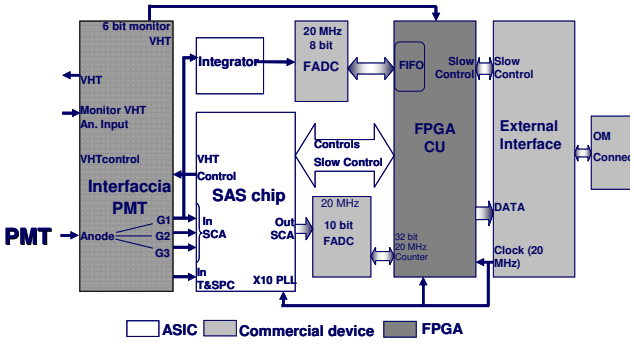

Figure 1 Front-end electronics block diagram

The present work concentrates on this part of the front-end, the PMT interface.

III. SIGNAL SIMULATIONS

From the results of the simulations of high energy neutrino events in a detector, like NEMO, various important points emerge:

- Three main pieces of information must be extracted by the front-end:

- The signal arrival time, with resolution lower than 1 ns;
- The charge of the signal from the PMT with very high resolution;
- The shape of the signal.

- The front-end must have the following characteristics:
  - Wide input dynamics, since the signals to be sampled have a very wide dynamic range according to the signal time duration, that is 1000 photoelectrons (pe) in 500 ns and 10000 pe in 10μs;
  - Negligible dead time. The presence of the single pe background due to spontaneous decay of the ^{40}K present in the seawater, with an average rate of 50 KHz imposes a suitable memory channel depth and a precise relationship between the sampling and conversion frequencies.

IV. THE PMT

The considerations and simulations are related to the 10" PMT selected for the NEMO experiment. The selected gain is $5 \cdot 10^7$.

The PMT base is active and provides single pe signals on an anodic load of 50Ω of about 50 mV amplitude with a rise time of about 2.6 ns. The PMT signal amplitude linearity is up to about 100 pe. Due to the signal frequency spectrum and the resolution required for the measurement of the arrival time we chose to sample the signal at 200 MHz with analog memories. This value is a good compromise between dissipated power and the quantity of samples taken for every signal.

The conversion of each sample is effected by a commercial 10 bit 20 MHz ADC. A consideration must be made on the signal frequency band. It presents components above 100 MHz which can produce aliasing effects. Therefore the PMT signal must be filtered. Furthermore in order to increase the PMT signal amplitude it is possible to use a higher anodic load, for example 800Ω. This allows the gain of the PMT to be reduced, increasing the average life time of the PMT. To cover the wide signal dynamic range in the most linear possible way, a PMT interface is foreseen that provides an input impedance of about 800 Ω, signal filtering, reducing the components above 100 MHz to -60 dB and, in three channels with different gain, produces three signals with different amplitude but identical shape. The three gains have been derived from the simulations in order to use three dynamics of 1 volt that cover signals of up to 512 pe. For istance, the first channel is direct, the second is reduced by a factor 8 and the third by a factor 64. Each channel has a suitable buffer to drive the delay lines and the load of the analog memories. The delay is essential and is of the order of 30 ns: from the moment in which the signal cross a suitable threshold a time interval is required for its classification and the beginning of the appropriate sampling of the signals according to their classification. Integrated delay lines will be used, greatly reducing bulk and having a greater mechanical robustness compared to the classical delay lines made with coaxial cables.

Other specifications are the 3.3 V power supply and the low-power dissipation. As a result of the former each channel has to be protected from PMT signals that go over the 3.3 V. The second channel, having a gain of 1/8 can, for example, sustain signals of up to 24 V. For this reason a switch has been introduced into every amplification branch with a fast JFET that excludes the amplifiers from the signal setting it to high impedance as soon as the voltage at its input goes over an adjustable threshold. This threshold is related to the threshold voltage of the JFET and to its externally applied gate voltage. The selected JFET introduces very low parasite capacitances making it possible to limit the input signal bandwidh to about 40 MHz at -3 dB, allowing the use of a low power operational amplifier with 3.3 V single supply whose power consumption is of about 5 mW. In figure 2 the circuit schematic of the interface board is shown.

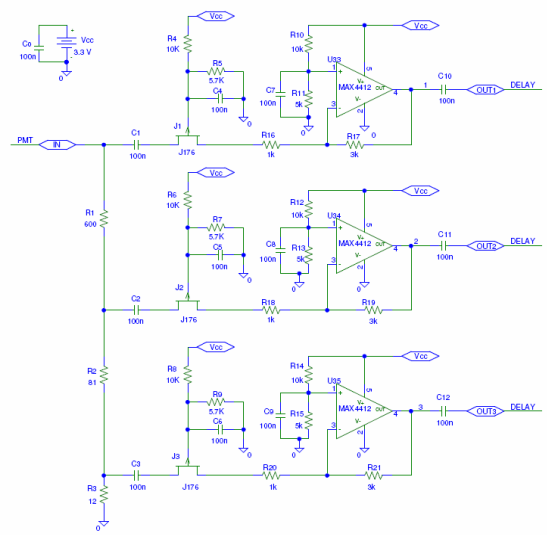

Figure 2 Schematic view of the PMT interface.

In figure 3 a picture of the PMT interface board is shown.

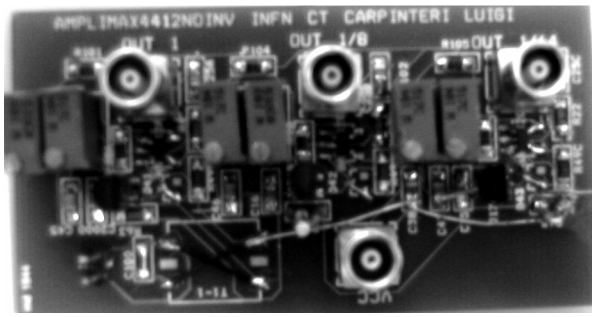

Figure 3 A picture of the PMT interface board.

It has been designed and tested with the NEMO selected PMT in a dark box using a laser to produce light. The typical signals of the three channels in presence of a signal of single pe are shown in figure 4.

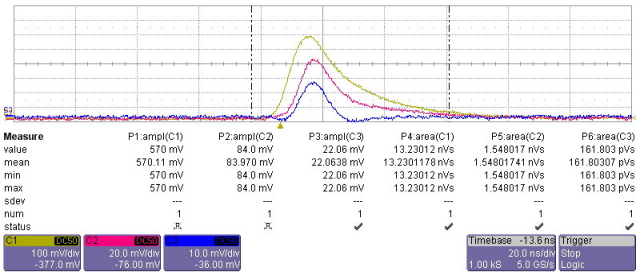

Figure 4 Single pe signal output of the PMT interface board.

In figure 5 the three channels in presence of a signal of PMT of 27 pe are shown. There it is shown how the first channel is saturated and the second presents an exact replica of the PMT signal attenuated of a factor 8 while in figure 6 the output of the board corresponding to 81 pe are shown. Finally in figure 7 all the three channel are in saturation.

The single photelectron signal output is of about 570 mV *and we want to have a voltage dynamic range of 1 V corresponding to 8 pe. So the gain of the PMT must be* lowered by a factor of about 5 which means $1 \cdot 10^7$.

The rise time of the signals is of about 9 ns as a result of the filtering of the signal. This will avoid aliasing effect in the 200 MHz sampling performed by the analog memories.

The values of gain of the three output channels are easily settable by adjusting the resistor ladder at the input. The power consumption of the PMT interface board is of 8 mA at 3.3 V. The board could also work very well with power supply as low as 2.7 V.

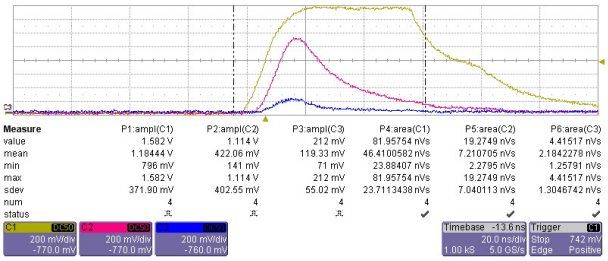

Figure 5 27 pe signal output of the PMT interface board.

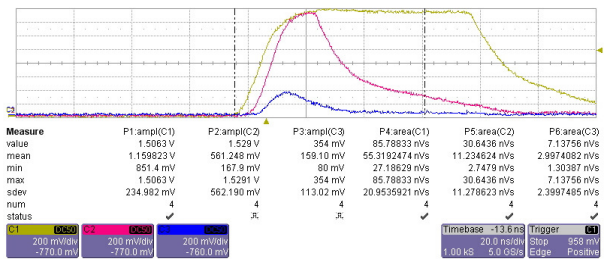

Figure 6 81 pe signal output of the PMT interface board.

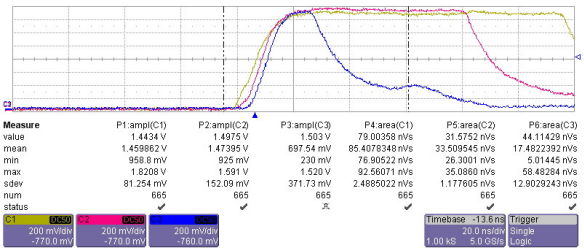

Figure 7 Saturation of all the PMT interface board output.

V. CONCLUSION

A proposal for a system to capture signals in the Optical Module of a Underwater Neutrino Telescope has been described. It pays great attention to the problem of power consumption with relation to precision. All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any Underwater Cherenkov Neutrino Telescope.

The development of the PMT interface board to meet the specifications of power dissipation, filtering properties, anodic load and required gain estabilishes the basis for the definitive design of the SAS chip. As soon as the chip is available, the whole front-end will be tested together with the PMT.

The PMT interface board will, in the meantime, be tested together with the preceding version of the front-end.

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New RPC Front-End Electronics for HADES

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Abstract

Time-of-flight (TOF) detectors are mainly used for both particle identification and triggering. Resistive Plate Chamber (RPC) detectors are becoming widely used because of their excellent TOF capabilities and reduced cost. The new ESTRELA* RPC wall, which is being installed in the HADES detector at Darmstadt GSI, will contain 1024 RPC modules, covering an active area of around 7 m^2. It has excellent TOF and good charge resolutions. Its Front-End electronics is based on a 8-layer Mother-Board providing impedance matched paths for the output signals of each of the eight 4-channel Daughter-Boards to the TDC.

I. INTRODUCTION

HADES is a High Acceptance DiElectron Spectrometer currently installed at the SIS accelerator of GSI Darmstadt (Germany), which has as main goal the detection of electron pairs produced in relativistic hadron-nucleus and nucleus-nucleus collisions, with high acceptance and invariant-mass resolution, to obtain information about the modification of the properties of vector mesons in nuclear matter, both normal and hot and compressed. HADES consists of several detectors providing triggering, particle identification and momentum reconstruction capabilities. Among these sub-detectors there is a TOF system, built of plastic scintillator rods read by photo-multiplier tubes at large angles and of Resistive Plate Chamber (RPC) detectors at low angles, where the particle rate is low enough. This new low angle ESTRELA detector, which has recently been approved, covers a polar angle between 18º and 45º with 2π azimuthal acceptance, and consists of a RPC wall containing 1024 double-sided readout detectors (2048 channels) distributed in 6 sectors, covering an active area around 7 m^2.

Detector cells have 4 gaps of 0.3 mm width inserted inside aluminium profiles [1]. With this design, the crosstalk between neighbour channels is kept below a negligible level. Plates are made alternatively of aluminium and float-glass their widths ranging between 2.2 cm and 5 cm and the lengths between 12 cm and 52 cm. The HV is applied to the inner aluminium plate and the induced signal is read in all the electrodes. Typical applied voltages with respect to the grounded Al electrode placed in the middle of the cell are of the order of 6kV. As ionizing gas, the 'standard mixture' (85% of Freon, 10% of SF6 and 5% of isobutane) was chosen. The narrow electronic peak of a typical signal has a rise time of about 500 ps and a width of 5 ns.

* Electrically Shielded Timing RPCs Ensemble for Low Angles

II. FRONT-END ELECTRONICS

The Front-End electronics consists of 2 different boards: the 4-channel Daughter-board (DB) and the Mother-board (MB), which serves 8 DB (figure 1). Thus, every MB provides an interface for 32 channels from the DB to the TDC readout-board (TRB). The TRB consists on a custom multi-purpose 128-channel Time-to-Digital Converter electronics based on the HPTDC chip [2] with on-board DAQ functionality, needing 1 channel for timing. Further information about the TRB can be found in [3].

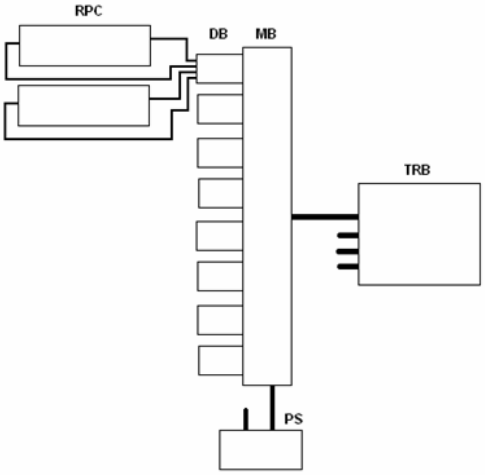

Figure 1: Full chain diagram block.

The DB is the part of the front-end electronics that generates digital signals to be used for TOF and charge measurement. These digital signals are transmitted to the TRB through the MB, which also provides stable supply voltage and thresholds to the DB.

Main requirements of the Front-End electronics for the HADES RPC wall are the following:

- Large bandwidth to deal with very narrow RPC pulses (500 ps rise time).

- Low noise levels (crosstalk < 1%).
- Precise time (electronic jitter < 50 ps) and charge measurements. The overall time resolution (RPC+FEE) should be less than 100 ps, to obtain time resolutions better than 75 ps after slewing correction.
- Low Voltage Differential Signal (LVDS) output signals.
- Output signal for the trigger logic of HADES.
- Stability, reliability, and compact design (max. 4.5 *x* 5 cm for 4 channels).
- Moderate power consumption (about 0.5 W per channel), to reduce heating.

The small space available for the front-end electronics on the detector makes size an important restriction for the DB. Since the DB has been built with discrete, commercially available components, an important requirement for the design of the electronics is the use of the minimum quantity of components, forcing the schematics to be as simple as possible. Other important requirement is the need of low power consumption, to minimize heating.

There are also restrictions in size for the MB, limiting its width to 6 cm to avoid the interaction of the board with the active area of the detector. The MB is a 8-layer PCB, and has a size of 40 *x* 6 cm^2. DB and MB are connected geometrically forming an angle of 90º. Thus, the end of the FEE on the front-side and the back-side of the RPC gas-box will form a channel for air cooling.

III. THE DAUGHTERBOARD

The 6-layer DB provides a digital LVDS output signal containing accurate time and charge information in a compact design, which employs a reduced number of commercially available and inexpensive components.

TOF measurement is performed through a fast discriminator, while the charge measurement is obtained by the Time Over Threshold method (TOT), which gives the charge information as the width of the output pulse.

Since the RPC output signal has frequency components extending up to the GHz range, the preamplifier used in the DB features a 2 GHz bandwidth, with 18 dB power gain and 2.8 dB noise figure. After the amplification, the signal is processed in two parallel ways (figure 2): on one hand, a leading edge discriminator implemented with a fast PECL comparator produces the rising edge of the output signal for time measurement. On the other hand, an integrator, based on a OPA690 voltage operational amplifier, shapes the signal used to measure the charge information. A second leading edge comparator, acting over the shaped signal, determines the width of the output signal, thus encoding information about the charge. In the actual scheme, when the TOF comparator is activated, the output gets locked through the latch enable input. The unlocking of the output is produced by the activation of the TOT comparator. A minimum dead time of 20 ns between the activation of both comparators avoids hang-ups in the digital signal. Further information about the DB can be found in [4].

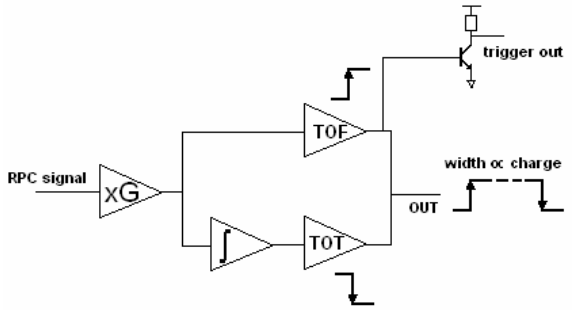

Figure 2: DB diagram block.

In practice, both discriminators are implemented on the MB by the MAX9601 chip, which integrates 2 PECL comparators with latch and 500 ps delay in the same chip. Before transmission to the Motherboard, the output signal is converted into LVDS by the differential translator/repeater SN65LVDS100.

IV. THE MOTHERBOARD

The Motherboard interfaces the very front-end electronics (DB) with the data acquisition system (TRB). Main tasks concerning the MB are to provide:

- Stable and programmable threshold voltages (for TOF and TOT) via DAC.
- Interface for DAC control.
- PCB paths for the readout of all the detector signals.
- Test input signals paths.
- Stable and low ripple power supply voltage and ground.
- Output for low level trigger purposes.

Threshold voltages have been implemented by the LTC2620 DAC. This DAC features 12 bit resolution, low power consumption and very low output noise. To minimize the influence of the noise picked-up along the signal path, every DAC output signal is scaled down through a resistor divider on the DB side, thus, reducing the noise levels by the same factor. The 8 DAC installed in every MB are daisy-chained (figure 3), and can be programmed using the same control lines by Serial Peripheral Interface (SPI).

For signal delivery from/to the MB, the LVDS Standard has been considered as the optimal standard transmission choice [5]. This interface allows communicating data using a very low voltage swing, requiring very low power consumption. This differential signalling technology allows data transmission at hundreds of Megabits per second (Mbps), fitting the requirements of the application.

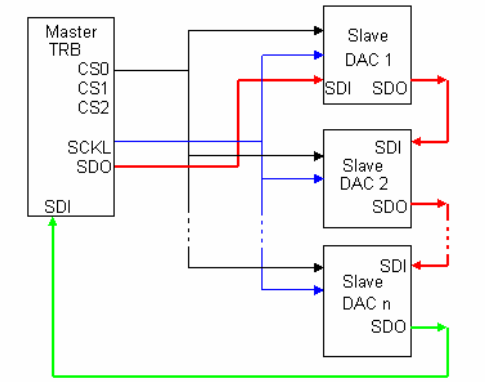

Figure 3: Daisy-chain implementation of the DACs on the Motherboard.

The LVDS interface is used to transmit the control and programming data to the DAC, which are converted to TTL on the MB through a translator. The same differential interface standard is used for the signals coming out from the DB which provide information about the TOF and charge. The main advantage of the differential approach is that noise is coupled to the two wires in common mode (the noise appears on both lines equally) and is thus rejected by the receivers which look at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the cancellation of magnetic fields. In addition, the current mode driver is not prone to switching spikes, and as differential transmission is practically immune to power supply fluctuations there is a further reduction of noise [6]. This is especially important, because switching power supplies are expected to be used to feed the whole system.

Signal paths on MB are completely impedance matched to 100 Ω, terminated on receptor side, to reduce reflections and distortions. Strip-lines (matched traces in the inner layers) between ground and power planes have been implemented [7] instead of micro-strips to increase noise immunity levels. For strip-line, the impedance Z_{DIFF} is given by [8]:

$$Z_{DIFF} = 2 \cdot Z_o \cdot (1 - 0.374 \exp(-0.29 \frac{S}{h}))\Omega \qquad (1)$$

With

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left(\frac{4h}{0.67\pi(0.8W + t)}\right)\Omega \qquad (2)$$

Where S denotes the distance between traces, h denotes the thickness of the board, W denotes the trace width, t denotes the trace thickness, and ε_r is the dielectric constant of the medium.

The DB is connected to the MB through a SAMTEC QSS connector with 16 differential pin pairs of 0.635 mm pitch. The connector is specified for a crosstalk less than 3.6 % and an impedance matching of 100 Ω, with a mismatch less than 10 % up to frequencies of 2 GHz.

As mentioned before, the MB provides appropriate paths to deliver test signals from the TRB to the DB. The DB provides additional test inputs separated from the RPC signal inputs. The goal of the test signals is only to check if a certain channel is working properly. The use of test signals for calibration is not foreseen. For the reasons already exposed, the test signals are also transmitted as LVDS signals. On the DB, test signals pass through a passive RC derivator circuit placed behind a TTL receiver with the purpose of converting them into narrow pulses, similar to RPC signals. Thus, an external test pulse generates a narrow RPC-like test signal of a few nanoseconds width. Test signals are generated on the TRB, where a LVDS driver delivers the signals through a flat-ribbon cable to a connector placed in the centre of the MB. A 4-port LVDS receiver on the MB allows distributing the test signal to the desired output through a dip-switch. The end of every signal path is terminated with a 100 Ω resistor.

The MB supplies three voltages to the DB; +5V, +3.3V and -5 V, managing a current of 80 mA, 40 mA and 35 mA respectively per channel (including MB consumption). Since the MB is feed by a switching power supply, special care was taken in the design of a power ripple filtering scheme.

Switching power supply output produces a relatively low-frequency ripple at the switching regulator clock frequency (typically 100 kHz to 3 MHz) and high-frequency "spikes" associated with power-switch transition times. The switching regulator pulsed energy delivery creates the ripple. Tantalum high capacitance low ESR capacitors were placed at the power input on the MB. These bulk capacitors smooth but do not eliminate the ac content. For this reason, a local ferrite filter in a π configuration was implemented for every DB and each supply voltage. This filter contains very low ESR multilayer ceramic capacitors (MLCC), of different decades (from 1nF to 1μF), together with special 100 nF feed-through filter capacitors placed before and after the ferrite bead. The ferrite used is the BLM18PG121, from Murata, which has very low DC impedance (only 0.05 Ω). Its impedance-frequency characteristic is shown in figure 4.

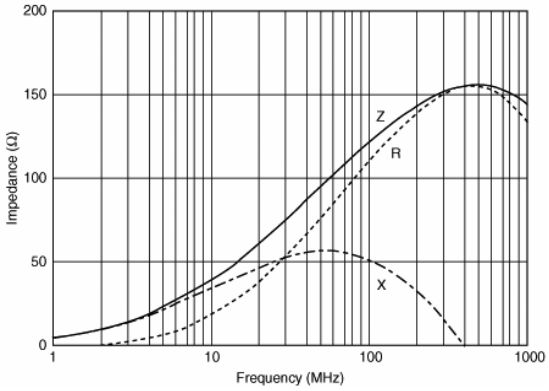

Figure 4: Impedance-frequency characteristics of BLM18PG121 ferrite, from Murata.

The technique of plugged vias was used to achieve short paths from filter capacitors to ground and power, thus reducing the ESL and ESR associated to the layout.

The trigger system (figure 5) provides information about the number of channels fired for a given event. In the MB, the output information of every DB channel is collected and processed to provide an output that is used for low level trigger purposes. This is implemented by a 2-stage circuit with operational amplifiers. Four summing-difference amplifiers and a summing amplifier work in cascade to produce a contribution of -100 mV per fired channel at the output of the trigger. As the number of channels that generate this trigger signal is 32, the output voltage with all channels fired is -3.2V, which is the dynamical range required by the TRB. If there is no channel fired, the output vanishes. The operational amplifier used is the OPA690, mainly because of its high slew rate (1800 V/μs) and high output swing (±4 V).

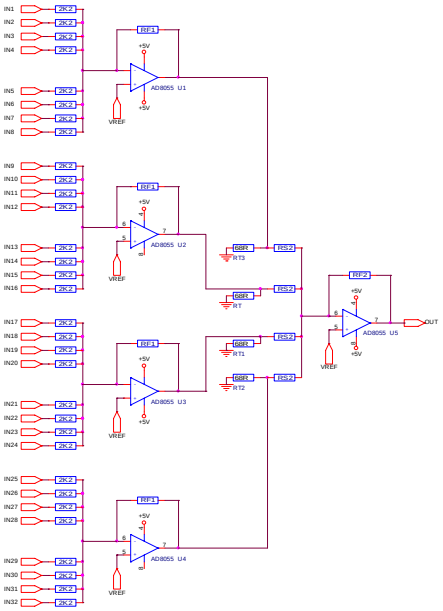

Figure 5: Schematics of the multiplicity trigger signal on the MB.

For simplicity and to reduce the number of pins needed to connect the DB to the MB, multiplicity signals (4 per DB) are transmitted from DB to MB without being converted to LVDS.

V. RESULTS

The Front-End Electronics was tested by pulse generator signals [4], a ^{60}Co radioactive source and a 1 GeV ^{12}C beam delivered by the GSI SIS accelerator.

Measurements performed on the present version of the Front-End Electronics with electronic pulses sources show about 15 ps TOF resolutions (for pulses above 100 fC). Studies of data with several channels firing simultaneously show a cross-talk level below 1% for a threshold of 25 fC, and a worsening of the time resolution of at most 10 ps.

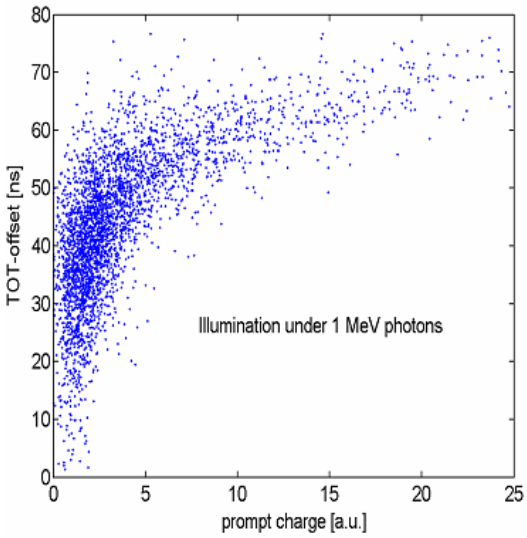

Figure 6: TOT vs charge characteristic for illumination under ^{60}Co photons.

Figure 6 shows the correlation between TOT and prompt charge under gamma illumination, using a ^{60}Co source. The TOT has an offset due to the dead time of the discriminator which was subtracted. Saturation effects are visible in the streamer region. The correlation observed proved to be reasonably good for performing the RPC slewing correction over the time of flight measured. Measurements performed under gamma illumination give an estimation of the TOF resolution of σ=40±5 ps when base-line fluctuations due to cross-talk are included.

Recent data for cosmic rays and secondary particles from 1 GeV C-C collisions show efficiencies of 98-99% (for cosmic rays) [9], and time resolutions around 70 ps (including the detector response) for C-C collisions, as shown in figures 8 and 9.

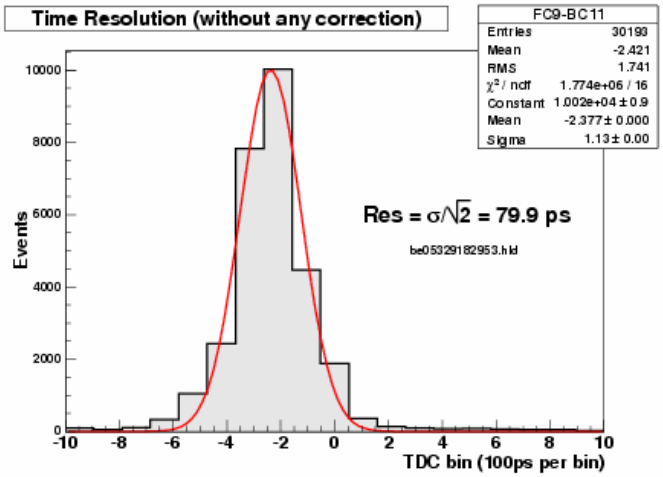

Figure 7: Time resolution for the present Front-End electronics without any correction under 1GeV C-C collisions.

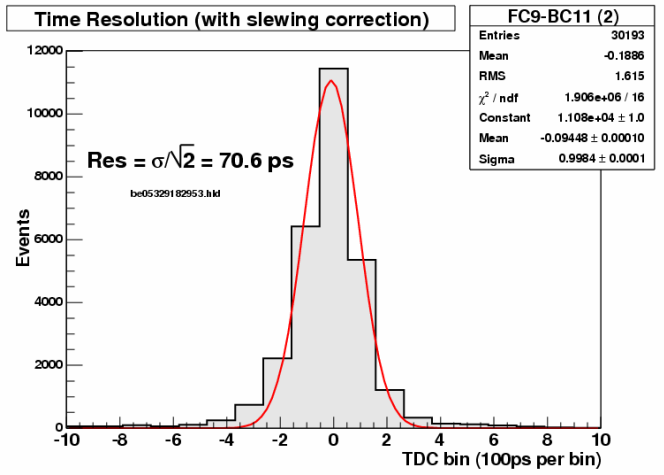

Figure 8: Time resolution for the actual Front-End electronics with slewing correction under 1GeV C-C collisions.

VI. FUTURE WORK

Despite of the good results obtained with the actual version of the FEE, some important improvements are being performed on both, MB and DB boards.

The upgrade of the DB will simplify the charge measurement scheme by using only one of the two comparators. Thus, there will be a double integration with sliding reference threshold, being the integrated signal itself and not the charge comparator the one determining the trailing edge of the output signal (which provides the charge information). This change will improve the resolution of charge measurement and will reduce the power consumption per channel around 30%, which in the actual version is nearly 0.5 W (including MB consumption).

Concerning the MB, the ripple filtering scheme of the power supply voltage will be improved, to increase the power supply rejection ratio, reducing the influence of the switching power supply that feeds the MB. Low drop-out voltage regulators will be included to reduce ripple. A read-back capability will be added to the DAC to check that they are programmed correctly. The manual switch for the test signals will be removed, and a temperature sensing will be added.

VII. CONCLUSIONS

Dealing with the very short rise time RPC signals requires the use of very high speed components and high frequency rules in the PCB design. Differential impedance matched paths with termination resistors were implemented for the transmission of LVDSwhich was considered the optimal interface for the transmission of the digitalized signals.

Special care was taken in noise reduction techniques, thus, multi-layer PCBs with power and ground planes together with many filter capacitors were used in the design of both, DB and MB. For this reason, a local ferrite filter in a π configuration was implemented for every DB and each supply voltage.

Results reveal that the Front-End electronics for the ESTRELA RPC wall of HADES provides very good performances under electronic pulses and gamma ray sources. Tests with ^{12}C beam performed feature an overall time resolution that satisfies the requirements of the project.

VIII. ACKNOWLEDGMENTS

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ALIBAVA: A portable readout system for silicon microstrip sensors

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Abstract

A portable readout system for silicon microstrip sensors is currently being developed. This system uses a front-end readout chip, which was developed for the LHC experiments. The system will be used to investigate the main properties of this type of sensors and their future applications.

The system is divided in two parts: a daughter board and a mother board. The first one is a small board which contains two readout chips and has fan-ins and sensor support to interface the sensors. The last one is intended to process the analogue data that comes from the readout chips and from external trigger signals, to control the whole system and to communicate with a PC via USB. The core of this board is a FPGA that controls the readout chips, a 10 bit ADC, an integrated TDC and an USB controller. This board also contains the analogue electronics to process the data that comes from the readout chips. There is also provision for an external trigger input (e.g. scintillator trigger) and a 'synchronised' trigger output for pulsing an external excitation source (e.g. laser system).

I. INTRODUCTION

There is a need of studying the main properties of highly irradiated microstrip silicon sensors since this type of detectors are used at the LHC experiments. Also as a higher luminosity is intended to be achieved at SLHC experiments, it would be an advantage to be able to predict the behaviour of this kind of sensors under certain circumstances (as the irradiation dose). Among these properties, the collected charge when a charged particle crosses the detector is important for knowing the performance of the detector. At the present time, it is difficult to carry out valuable measurements of the collected charge in microstrip silicon sensors due to different reasons. One of these reasons is that a custom and expensive laboratory set up is needed. Another one is that since different equipments are used depending on the laboratory facility, the measurements obtained are often not comparable. Finally, this type of sensors may have hundreds of channels for reading.

On the other hand, it would be interesting to test this kind of detectors with an electronic system as similar as possible to those used at the LHC experiments. Therefore, a front-end readout chip used at the LHC experiments should be used. An analogue measurement of the pulse shape with this kind of readout chips would be particularly interesting because it would allow to carry out more reliable charge collection research than with a binary measurement.

For generating the charged particles in a laboratory, two main setups are usually used. Firstly, a radioactive source setup can be used. In this setup, the charged particles are generated randomly so a scintillator and a photomultiplier are necessary following the detector to generate a signal which will inform when a charged particle has crossed the sensor. Secondly, a laser setup can be used. In this setup, a laser light is generated exciting a laser source with a pulsed signal. In this case, the same signal used for exciting the laser source can be used as a trigger signal. This kind of setup has already been used for ATLAS SCT End Cap Modules as can be seen in [1].

Taking into account what has been expounded previously, it seems clear that an electronic system which could carry out an analogue measurement by means of a front end readout chip, as those used at LHC experiments, with a laser setup and a radioactive source setup is needed. The main goal is reconstructing the analogue pulse shape at the readout chip front end with the highest fidelity.

In order to fulfil these requirements the system must have a particular characteristics. First, it will be compact and portable. Second, the system will have its own supply system. Third, it will be communicated with a PC via USB, which will store and will process the data acquired. Fourth, the system will be controlled from a PC software application in communication with a FPGA which will interpret and will execute the orders. Fifth, the system will be used with two different laboratory setups so it will have an external trigger input, from one or two photomultipliers (radioactive source), and an external trigger output for pulsing an external excitation source (laser system). Finally, this system will contain two front-end readout chips to acquire the detector signals.

II. SYSTEM ARCHITECTURE

The system will have two main parts, a hardware part and a software part. The hardware part will acquire the microstrip silicon sensor signals, from an external trigger input or a synchronised external trigger output, and will process the data in order to be stored in a PC or laptop.

For dealing with this, the hardware block will be a dual board based system. There will be a mother board which is intended to process the analogue data that comes from the readout chips, to process the trigger input signal in case of radioactive source setup or to generate a trigger signal if a laser setup is used, to control the whole system and to communicate with a PC via USB. The daughter board will be a small board which will contain two Beetle readout chips [2]

and will have fan-ins and detector support to interface the sensors. As it has been stated previously, the hardware part will be divided into two boards because the detectors will be joined to the daughter board and these detectors will be exposed to an aggressive environment for the electronic devices (for instance, radiation or very low temperatures). Both boards will be communicated by 'twist and flat' ribbon cable for the analogue data signals coming from the Beetle chips, slow and fast control digital signals to the Beetle chips, a temperature signal as well as the supply level for the Beetle chips. The high voltage detector power supply will be provided directly to the daughter board.

Regarding the software part of the system, its function is mainly controlling the whole system and processing the data acquired from the sensors in order to store it in an adequate format file. This format file will be compatible with software used for further data analysis. The software will be initially a Windows based program. With this program the system will be able to be configured and calibrated. Acquisitions with a laser setup or a radioactive source setup will be able to be carried out as well. Finally, a file output format will be able to be chosen among various for a particular purpose.

III. DAUGHTER BOARD

As it has been stated previously, the daughter board will be a small board with the minimum components needed for accommodating two Beetle chips, a temperature sensor and the sensors support (fan-ins and power supply). The block diagram of the daughter board is shown in figure 1. The main components of this board will be two Beetle readout chips used to read the detector channel signals. There will be a thermistor as close as possible to the detectors in order to have a temperature readout on each acquisition as well. The analogue signal obtained from this thermistor will be sent to the mother board for digital conversion. For the readout chips power supply and the buffer power supply, a DC level (3.3V) will be sent from the mother board. This supply level will be regulated by a low drop out (LDO) linear regulators for obtaining the DC supply levels required by the readout chips and the buffer stage.

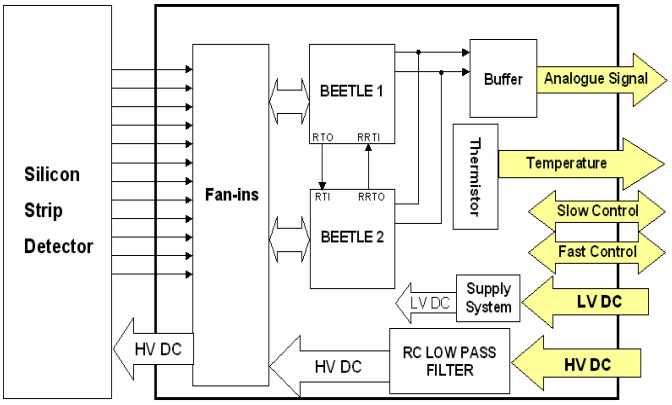

Figure 1: Daughter board block diagram (daisy chain configuration).

A mechanical connection system and fan-ins will be provided for connecting the detectors. Regarding the detector high voltage power supply (up to 1000 V approx.), it will be supplied directly to the daughter board. This supply signal is a low current signal. There will be decoupling stage will for this supply prior to the detector. This decoupling stage will be composed of a RC filter.

The daughter board ground scheme will be very important for the final behaviour of the system, particularly the reliability of the data acquired. There will be three different grounds: analogue ground, digital ground and detector ground. Analogue ground and digital ground for the Beetle chip will be split but with the provision of being able to link them.

The main characteristics of the Beetle readout chip can be found on [2]. As a summary, it can be stated that the chip has been developed for the LHCb experiment and fulfils the requirements of the silicon vertex detector (VELO), the silicon tracker and the RICH detectors in case of multi-anode photomultiplier readout. It integrates 128 channels with charge sensitive amplifiers, shapers and buffers (chip front-end). A comparator per channel can provide a binary signal. There is an analogue pipeline of 187 by 128 cells which is operated as a ring buffer. Either the shaper or the comparator output is sampled into the analogue pipeline with the clock chip frequency (40 MHz). Output stage consists of 128 charge sensitive amplifiers and 4 multiplexers. The chip has two different kind of control: a slow control for configuring the chip (I2C interface) and a fast control for clocking, resetting, calibrating and reading out (LVDS signal format). The output could be analogue or binary through the analogue pipeline or digital related to the binary (four adjacent comparator channels) via LVDS.

On this system the Beetle chip analogue output on one port will be used. In this case the analogue front-end pulse signal is sampled into the pipeline with the frequency of the Beetle chip clock which will be fixed to 40 MHz (period of 25 ns). The peak voltage of the front-end pulse signal is proportional to the collected charge at the detector channel The peak time this signal is about 25 ns (depending on the load capacitance among other parameters) and the remainder of the peak voltage after 25 ns is below 30 %. Therefore, a 75 ns pulse length will be considered in order to reconstruct the pulse. Once the pulse has been sampled into the analogue pipeline, for reading out a particular position of this pipeline will be needed to trigger a signal (TRIGGER) related in time with the readout chip clock (CLK). The analogue pipeline latency will be fixed to 128, so the TRIGGER signal will have to be active 128 CLK cycles (3.2 µs) after a particular front-end signal point of interest has been sampled.

Once (125 ns) the TRIGGER has been activated (at least a 25 ns pulse), the readout of the analogue output on one port data will start synchronous to CLK. A DATAVALID signal will be activated 25 ns before the readout starts and it will be deactivated 50 ns before the readout ends. This analogue output signal is a multiplexed signal composed of a 16 bits header and 128 data channels, whose voltage amplitude will correspond to the particular front-end sample). The width of each header bit or each channel is 25 ns, so the length of each readout frame will be 3.6 µs. The header bits will not be used on this system. The readout chip will be operated in a single readout scheme, that is, the TRIGGER signal will not be activated while a readout is carried out.

Regarding the fast control of the Beetle readout chip, three LVDS fast control signals (CLK, TRIGGER and DATAVALID) has been already presented. There are two more signals that belongs to the LVDS fast control, RESET and TESTPULSE. The RESET signal is used for resetting the Beetle. The chip's slow control interface is a standard mode I2C slave [3]. The bias settings and various other parameters like the trigger latency or the injected test pulse amplitude can be controlled by this control.

The analogue output buffer is a current buffer so the analogue output signals are current differential signals. The loop for each signal will be closed with a 100 Ω resistor on the daughter board and the voltage over that resistor will be the analogue output voltage. These outputs will be buffered at the daughter board by means of a differential line driver (AD8130, Analog Devices). No line equalization will be required at the mother board if the cable is no longer than 10 m [4]. Finally, the analogue output dynamic range will be in the linear area as could be seen on [5]. This will correspond to ± 66000 electrons or ± 0.5 V approximately.

As it has been mentioned before, there will be two Beetle chips on the daughter board. The initial idea is daisy chaining both chips. It would allow several chips to share the analogue output data lines. The daisy chain consist of two signal paths, a token path (RTI, RTO) and a return token path (RRTI, RRTO). The chip position in the chain has to be configured by slow control. However, there is a concern about the readout of a second chip starting too early. Therefore, a parallel configuration will be considered as well. In this case, there will be two different analogue data lines one for each Beetle chip, so the analogue processing stages (signal conditioning, ADC and ADC control in the FPGA) would be duplicated. In both cases, the fast and slow control lines will be shared by the Beetle chips.

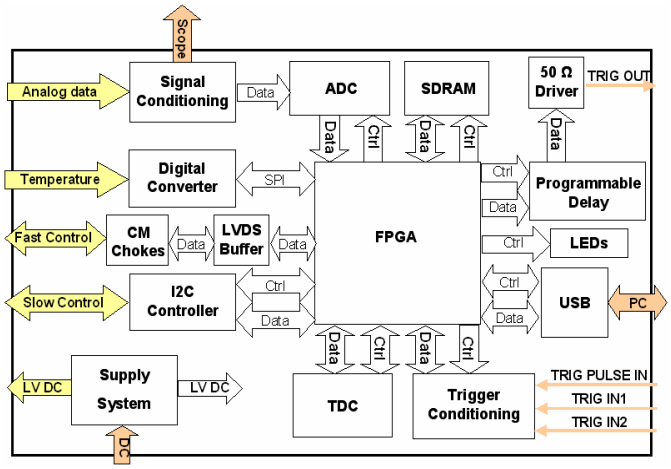

Figure 2: Mother board block diagram.

IV. MOTHER BOARD

The mother board block diagram is shown in figure 2. The main component of the system will be a FPGA which will implement the logic for controlling the rest of the blocks. The signal conditioning block is intended for transforming the differential voltage analogue input signal in order to drive an oscilloscope, which requires a single ended signal, and an analogue to digital converter (ADC), which requires a differential input signal shifted signal. First, a differential to single ended voltage amplifier with unity gain (AD8130, Analog Devices) will be used. The output signal of this block will be split in two signals, one will be connected to a unity gain buffer (and will be the scope output). The other one will be connected to a single ended to differential voltage amplifier with unity gain (AD8139, Analog Devices). This signal will be shifted to the ADC mid-range supply voltage (1.65 V) on this amplifier.

The ADC block is composed of a differential RC low pass filter for suppressing some of the wideband noise associated with high speed amplifiers and an ADC. The ADC is a 10 bit flash type with a sampling rate of 40 MHz (MAX1448, Maxim IC). The nominal resolution of this ADC will be 2 mV because the output will be signed code of 10 bits (1 bit for sign and 9 bits for data). This component has separate analogue and digital power supply as well as a parallel direct interface with the FPGA. The last two blocks are intended for a daisy chain configuration and they should be duplicated in case of a parallel configuration as well as the ADC control in the FPGA. The thermistor signal coming from the daughter board will be digitized at the digital converter block. This block will be composed of a thermistor to digital converter circuit (MAX6682, Maxim IC). It will measure the voltage across the thermistor and will produce a 10 bits plus sign output code. It will have a serial interface with the FPGA.

The Beetle fast control signals will have a LVDS format. The FPGA can manage directly with this format but in order to protect this component these signals will be buffered with two LVDS repeaters, one for the output signals to the daughter board (CLK, TESTPULSE, TRIGGER and RESET) and another one for the input signals from the daughter board (DATAVALID1 and DATAVALID2). Also a common mode noise suppressor choke will be provided for each signal. The slow control signals (SCL and SDA) will be generated by the I2C controller block. This block is just a parallel bus to I2C bus controller (PCA9564, Philips Semiconductors) that will convert the 8 bits parallel data generated in the FPGA I2C protocol. There will be also a memory block on the daughter board. This block will have a SDRAM of 128 Mbits (MT48LC8M16A2, Micron). The function of this memory will be temporally store the digitized data in each acquisition either with the radioactive source setup or with the laser setup prior to be read by the software.

In case of the radioactive source setup, a trigger from an external source will be generated. This input trigger can come from one or two photomultipliers (TRIG IN1 or TRIG IN2) or can be positive/ negative pulse up to ±5V or fast negative NIM (TRIG PULSE IN). From this inputs, the Trigger conditioning block will generate four signals in LVPECL indicating if TRIG IN1 or TRIG IN2 is active (with a leading edge discriminator), or if a negative or a positive pulse have been received on TRIG PULSE IN (with two discriminators). The four discriminators will be implemented with two dual LVPECL high speed comparators (MAX9601, Maxim IC). Four voltage thresholds are needed in this block, two will be the discrimination levels for TRIG IN1 and TRIG IN2, and the other will be the discrimination levels for positive and negative pulses (TRIG PULSE IN). These voltage thresholds

will be programmable by the user and a DAC of 12 bits will be used for this (AD5582, Analog Devices). The TDC block will be used, for instance, with radioactive source setup since the charged particles, and consequently the input trigger signals, are generated randomly in this case. This block will be composed only of a TDC integrated circuit with a resolution better than (TDC-GP1, Acam messelectronic). This TDC will measure the time passed between a start signal generated every 100 ns (time window for reconstructing an 75 ns long front end pulse) and a trigger signal generated if TRIG IN1 and/or TRIG IN2 are active, or TRIG PULSE IN are active.

In case of the laser setup, a synchronised trigger signal (TRIG OUT) will be generated to drive a laser source so that the pulse shape will be able to be reconstructed. For this reason a programmable delay circuit (3D7428, Data Delay Devices) will be used. With this circuit TRIG OUT will be able to be delayed up to 100 ns in 1 ns steps by a 8 bits parallel programming code from the FPGA. Following this block a 50 Ω driver will be incorporated for driving a pulse generator input that will pulse the laser source. For communicating with the PC or the laptop a USB block will be used. This block will have a USB controller (FT245R, FTDI) for USB to FIFO parallel (8 bits) bidirectional data transfer. The manufacturer of this controller also supplies the software drivers for interfacing the controller on the PC software. Three LEDs will be provided to inform about the system state to the user.

The supply system will be centralized on the mother board. A DC input level will be generated with an portable AC adapter. From this DC level the mother board digital levels (1.2 V, 2.5 V and 3.3 V) by means of LDO supply regulators. The mother board analogue levels (5 V, -5 V and 3.3 V) will be generated by a DC-DC converter and LDO supply regulators. The daughter board supply level (3.3 V) will be generated by a DC-DC converter.

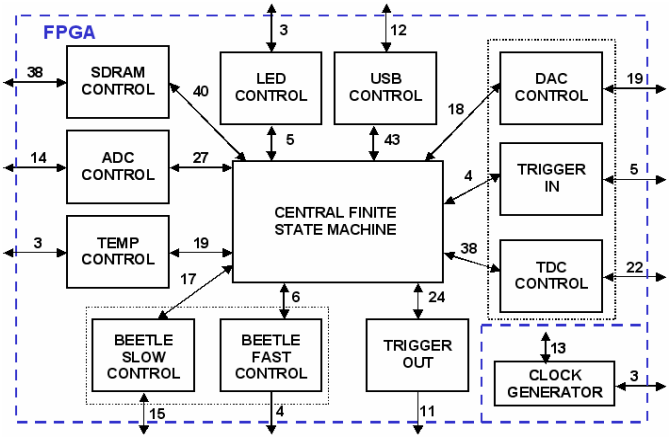

Figure 3: Block diagram of the logic that will be implemented in the FPGA

Regarding the FPGA block, this block will be composed of a FPGA (Spartan 3, Xilinx) and all the support for programming it (Flash PROM and connector). The FPGA will be clocked with a 40 MHz crystal. The main function of the FPGA will be implementing all the logic in order to control the hardware and to communicate with the PC. The block diagram implemented in the FPGA can be seen in figure 3. The slow control block will control the parallel bus to I2C-bus controller in order to program the Beetle configuration registers. The fast control block will generate the LVDS output signals (CLK, RESET, TRIGGER, TESPULSE) for the Beetle fast control. The TESTPULSE will be generated from a calibration signal. The TRIGGER signal will be generated from an internal TRIG_L signal (in case of laser setup) or from an internal TRIG_IN signal (in case of radioactive source setup) taking into account both the Beetle analogue pipeline latency and the particular synchronization delay.

The trigger out block will be used for the laser setup and it will produce an external trigger signal (TRIG OUT) that will be periodic (1KHz) and an internal trigger signal (TRIG_L) for the Beetle fast control block. These signals will be generated so that, in conjunction with the programmable delay circuit, the pulse shape at the Beetle chips front end could be sampled in 1ns intervals from its beginning till its end.

The trigger in block will generate an external and internal trigger signal (TRIG and TRIG IN, respectively) from signals SIN1 and/or SIN2 (discriminated signals from two photomultipliers), PPOS (external positive pulse) or PNEG (external negative pulse) coming from the trigger conditioning block. The coincidence of SIN1 and SIN2, as well as which inputs will be used, will be able to be programmed. The DAC control block will be related to trigger in block. Its function will be to control the DAC that will supply the four voltage thresholds for the trigger conditioning comparators. The TDC control block will be related to trigger in block and DAC control block. Its function will be to control the TDC, which will measure the time from a START leading edge signal (100 ns periodic signal) to the TRIG leading edge. It will also generate a TRIG_R signal (for the Beetle fast trigger control) related in time to the TRIG signal when the last will be active.

The ADC block will control the ADC, will read the digitalized data frames when the DATAVALID signal will be active and will store these frames in a internal FIFO RAM. This block will be duplicated if a parallel configuration of the Beetles chips is needed. The SDRAM control block will control the SDRAM. It also will implement the read/write data and control interface with the CFSM block. Both the digitized data from Beetle chips (256 by 16 bits per two chips readout) and the TDC data (32 bits per readout) will be able to be stored. The USB control will have to control the USB chip and to implement the data input/output and control interface with the CFSM. The clock generator block will supply the FPGA internal clock signals and the SDRAM clock signal. The temperature control block will read the digital conversion of the thermistor signal from the digital converter by serial interface. The LED control block will activate a red LED, yellow LED or green LED depending on its input code value. This will be used to show to the user the state of the system.

The CFSM (Central Finite State Machine) block will control the system hardware part by interpreting the orders that the system software part (PC software) will send by USB. Depending on the current state the CFSM will use different blocks and it will enable the communication among

those blocks. This is the reason why the rest of blocks are not connected to one another but rather they are connected only to CFSM. The CFSM main state will be a waiting state. When CFSM will be in this state, it will wait for an order coming from the PC software (by means of the USB control). Depending on the order, CFSM will choose among the rest of states as it is shown in figure 4.

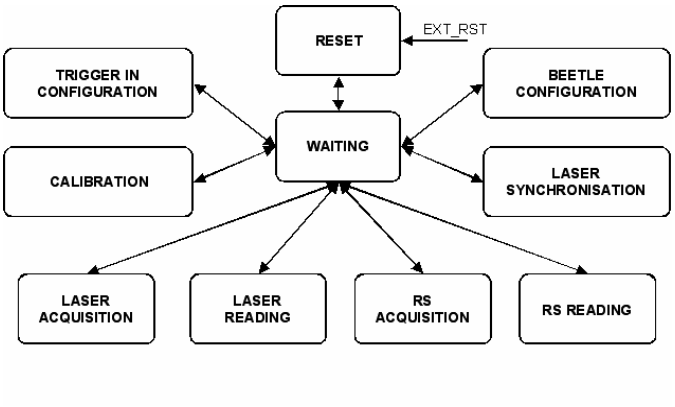

Figure 4: Central finite state machine possible states.

When the system will be powered on or with an external reset, the CFSM will go to the reset state prior to the waiting state. In this state, all the system will be initialized. After the FPGA configuration, the system also will go to this state.

In the Beetle configuration state, the configuration registers of the Beetle chips will be configured by slow control. In the calibration state, only after Beetle configuration state, the system will be calibrated by the Beetle internal test pulse generator, that is, known amplitude readouts will be acquired in order to have calibration data. In the trigger in configuration state, the DAC voltage thresholds will be programmed as well as the trigger inputs scheme will be configured. In the laser synchronization state, only after Beetle configuration state, the system will be synchronized (TRIG OUT and TRIG_L) in such a way that the Beetle front end pulse reconstruction can be carried out by delaying the TRIG OUT signal 100 ns in 1 ns steps.

In the laser acquisition state, a hundred of readouts will be acquired for each 1ns step that TRIG OUT will be delayed. So 10000 readouts will be acquired and stored in the SDRAM. The TRIG OUT frequency will be 1 KHz. A temperature readout will be acquired and stored in this state as well. In the laser reading state, the last laser acquisition will be read from the SRAM and data will be sent to PC with the temperature data. The SDRAM will be reset. In the RS (Radioactive Source) acquisition state, a programmable number of readouts will be able to be acquired. For each event a Beetle chips readout (256 by 16 bits) and a TDC readout (32 bits) will be stored in the SDRAM. Two temperature readouts, before and after the acquisition, will be stored as well. In the RS reading state, the last RS acquisition will be read from SDRAM and data will be sent to PC.

V. Conclusion and future work.

A portable readout system for silicon microstrip sensors has been presented at block diagram level. The system will be divided in a software part and a hardware part. The hardware part will be based in a dual board scheme, a daughter board and a mother board. This system will use two Beetle chips as a readout chips. Also, it will be able to be used with a laser setup and a radioactive source setup.

At the present time, the system is under development. The most of blocks of the mother board and some of the FPGA have already been designed and simulated. After the design will be finished, different blocks of the system will be tested with a FPGA development board [6] and custom boards which will integrate some of these blocks and will be able to be connected to the development board. Design changes will be carried out at this point if necessary. Finally, prototypes of the daughter board and the mother board will be manufactured and tested together. The software part of the system will be designed in parallel with the hardware part. A reduced version of this software will be used for testing the different blocks of the mother board with the development board.

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Poster Sessions

Commissioning and Calibrating the CMS Silicon Strip Tracker

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Abstract

The data acquisition system for the CMS Silicon Strip Tracker (SST) is based around a custom analogue front-end ASIC, an analogue optical link system and an off-detector VME board that performs digitization, zero-suppression and data formatting. A complex procedure is required to optimally configure, calibrate and synchronize the 10^7 channels of the SST readout system. We present an overview of this procedure, which will be used to commission and calibrate the SST during the integration, Start-Up and operational phases of the experiment. Recent experiences from the CMS Magnet Test Cosmic Challenge and system tests at the Tracker Integration Facility are also reported.

I. The Data Acquisition System

The CMS Silicon Strip Tracker (SST) is unprecedented in terms of its size and complexity, providing a sensitive area of >200 m^2 and comprising 10^7 readout channels. Fig. 1 shows a schematic of the control and readout systems for the SST. The control system [1] comprises 300 "control rings" that start and end at the off-detector Front-End Controller (FEC) boards and is responsible for distributing slow control commands, clock and Level-1 triggers to the front-end electronics. The signals are transmitted optically from the FECs to front-end digital opto-hybrids via digital links, and then electrically via 'token rings" of Communication and Control Units (CCUs) to the front-end electronics.

The readout system is based around a custom front-end ASIC known as the APV25 chip [2], an analogue optical link system [3] and an off-detector Front-End Driver (FED) processing board [4]. The system comprises 76k APV25 chips, 38k optical fibres (each transmitting data from a pair of APV25 chips) and 440 FEDs. The APV25 chip samples, amplifies, buffers and processes signals from 128 channels of a silicon strip sensor at the LHC collision frequency of 40 MHz. On receipt of a Level-1 trigger, pulse height and bunch-crossing information from pairs of APV25 chips are multiplexed onto a single line and the data are converted to optical signals that are transmitted via analogue fibres to the off-detector FED boards. The FEDs digitize, zero-suppress and format the pulse height data from up to 96 pairs of APV25 chips, before forwarding the resulting event fragments to the CMS event builder (EVB) and online computing farm.

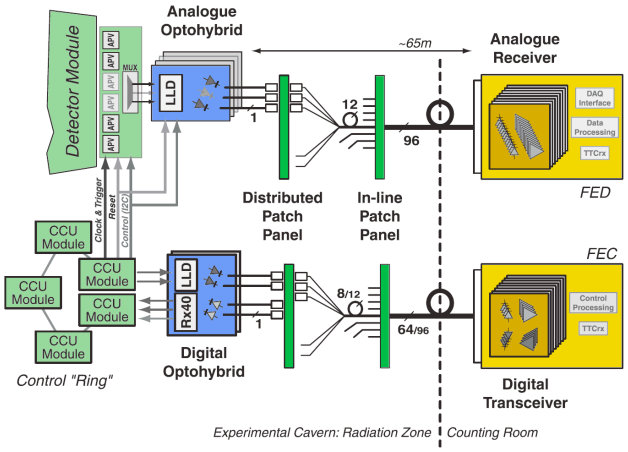

Figure 1: The SST control system uses ~300 control rings (based around the FEC and CCU boards) to propagate clock, trigger and slow control information to the front-end. The SST readout system is based around the APV25 chip, an analogue optical link system and the off-detector FED board.

The event data enter the EVB as a set of fragments distributed over ~700 FEDs (440 of which are used by the SST readout system). The task of the EVB, shown schematically in Figure 2, is to collect all the fragments, assemble them into a complete event, and then forward the event to a processing node on the computing farm. The average event size for CMS is expected to be ~1 MB, meaning that, for a L1 trigger rate of 100 kHz, the event builder network must be able to handle an aggregate throughput of 100 GB/s.

The event builder uses two stages of switch networks. The first stage comprises 64 *FED builders* that perform a first pass of data concentration by taking data from up to 8 sources (pairs of FEDs) and building super-fragments via a small 8x8 switch network connected to ReadoutUnits. In the second stage, complete events are built using the *Readout Builder*, which comprises 64 BuilderUnits receiving super-fragments (of the same event) from the 64 ReadoutUnits via a large 64x64 switch network. The BuilderUnits buffer and forward complete events to FilterUnit processes that are hosted on the computing farm, which apply the HLT algorithms and perform online event filtering and monitoring. This two-stage architecture allows the EVB

system to be scaled from a single Readout Builder (comprising 64 Readout- and BuilderUnits) at Start-Up to eight Readout Builders (providing a 512x512 network) for the final complete system.

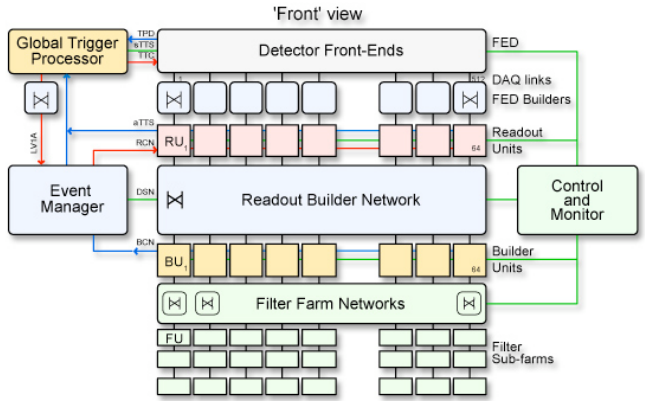

Figure 2: The CMS event builder, comprising a two-stage switch, that reads data fragments from the detector front-ends (via ∼700 FEDs) and constructs complete events for processing by the High-Level Trigger algorithms running on the Filter Farm nodes.

II. Commissioning the SST

The procedure required to bring the detector into an operational state suitable for physics data-taking is complex and comprises several independent *commissioning tasks* that configure, calibrate and synchronize the various hardware components of the readout system. These tasks will be used to commission and validate the detector during the integration, Start-Up and operational phases of the experiment. In addition, error diagnostic and online monitoring tools are being developed that will monitor the functional state of the readout system and guarantee data integrity during detector operation. A brief overview of the commissioning tasks is given below.

Detector partitioning and cabling:
The trigger partitions within the SST (four are envisaged for the final system) are detected using hardware scans that identify all front-end devices and off-detector FEDs that share a common trigger source. In addition, the cabling of the readout optical link system, comprising 38k fibres that connect the front-end APV25 chips to the off-detector (back-end) FEDs, is determined by scanning through the front-end laser devices that drive the optical links and biasing each device in turn so that "light" is observed in the FED data for a single channel, establishing the connection (and any possible faults).

Front-End Module:
Biasing of the ∼15k strip sensors will be tuned using an automated procedure that will perform high voltage scans and guarantee that each sensor is fully depleted. For the front-end APV25 chip, the analogue pulse shape is tuned to achieve optimal S/N and efficiencies, and the various bias and gain settings of the chip are tuned for optimal performance, such as the gain of the multiplexer stage and the analogue baseline level (to optimize the usage of the available dynamic range).

Readout optical link system:
The bias and gain for each channel of the front-end laser devices (that drive optical signals from pairs of APV25 chips to a single FED channel) are tuned in order to optimize the usage of the available dynamic range provided by the FED-based ADCs.

Front-End Driver:
The ADC sampling time for each of the 96 channels of a FED must be adjusted so as to optimize the sampling of the data. In addition, the calibration constants (such as pedestals and noise) used by the zero-suppression firmware algorithms and reconstruction software used by the HLT are measured.

Timing alignment:
Internal synchronization [5] of the SST front-end is achieved using "tick mark" features within the APV25 data stream. This procedure effectively accounts for signal propagation delays in the control system. Global synchronization of the SST system to LHC collisions and other sub-detectors will be achieved using collision data and a track-based analysis. A correct global timing alignment is crucial, as signal is attenuated by ∼4% per ns misalignment for the nominal operating modes.

The procedure for commissioning the sub-detector is now well defined and many of the individual tasks have been implemented for some time. The collaboration has several years experience of commissioning small prototype systems, both in the laboratory and during several beam tests (with many using a 25-ns bunched beam to replicate the LHC conditions). Experience with larger-scale systems, such as the large sub-structures assembled at the various tracker integration centres, is also significant. The final sub-detector is currently being assembled at surface-level within the Tracker Integration Facility (TIF) on the Meyrin site, prior to installation in the underground cavern at Point 5. This period of assembly and integration will be used to maximize our experience and understanding of the detector performance prior to Start-Up.

The one remaining area of the commissioning procedure which requires further study is the global synchronization of the SST to LHC collisions and the other sub-detectors of the CMS experiment. These studies are beginning now and the procedure will be validated (as far as possible) through simulation and analysis of data containing cosmic tracks, collected at the surface prior to installation at Point 5.

III. The Data Acquisition Software

The scale and complexity of the SST readout system imposes significant requirements on the data acquition software that is used to steer the commission tasks and operate the system. Many of these requirements, such as distributed computing, event building, database integration, online monitoring, error handling, etc, are satisfied by the two official software frameworks developed for the CMS experiment, called XDAQ and CMSSW, and the various framework applications defined within them.

XDAQ [6] is the online software framework and provides a core set of services and tools, including: a fast communication protocol for peer-to-peer messaging between processes registered with the framework; a slower communication protocol for configuration of the framework processes; a finite-state machine schema; and event builder and memory manage-

ment tools. CMSSW [7] is the offline framework, within which software for physics simulation, data handling, reconstruction, physics analysis and High-Level Trigger (HLT) algorithms is developed. The framework also provides services such as a conditions database and online monitoring.

The data acquisition (DAQ) software [8] for the SST has been designed to use both the XDAQ and CMSSW frameworks. Dedicated DAQ loops have been implemented to perform the various commissioning tasks. Each loop configures and controls the readout and (local) trigger systems using various *supervisor* applications that interact with the hardware. Communication between the various hardware supervisors, distributed across several PCs, is achieved using the XDAQ framework, which allows to automate the data acquisition loops and so remove the need for repetitive run control sequences and complex bookkeeping. The loops ensure that the appropriate data samples are accumulated for the subsequent (task-specific) analyses. Any configuration information required by the data analysis during the DAQ loop (eg, such as an identifier for the device being configured and its configuration) is encoded within the data stream itself. In this way, the analysis is entirely data-driven and no database access is required during the DAQ loop itself.

The analysis software determines the optimized hardware configurations and calibration constants from reconstructed calibration pulses, timing delay curves, dynamic range curves and other features of the APV25 data stream. The optimized configurations and calibrations are then stored in a dedicated database and are used to configure the readout system for subsequent periods of data-taking.

Unlike the various hardware supervisor applications that are implemented within the XDAQ framework, the analysis software for the commissioning procedure is implemented within the CMSSW framework. The DAQ software uses the standard CMS event building tools and the CMSSW framework so that an online, distributed data analysis can be performed and real-time feedback achieved during detector commissioning. The FED data are assembled into complete events by the CMS event builder and streamed to multiple FilterUnit processes hosted on the computing farm, which use the CMSSW framework to perform data analysis and monitoring. The same analysis software can later be used offline for more detailed studies.

Distributed data analysis is an essential feature of the DAQ software, so that it can handle the huge data volumes generated by the increasingly large readout system as the SST is assembled. The DAQ software uses the standard CMS software frameworks and tools wherever possible, for which support and maintainance is guaranteed for the lifetime of the experiment. In this way, the amount of custom software development (specific to the SST sub-detector), code duplication and maintainance is minimized. Additionally, the possibility to take advantage of new framework tools as they become available is maximised.

Importantly, the chosen design is also sufficiently flexible to allow transparent use of both local or global computing resources. When performing *local* data acquisition, the computing resources available to the SST are in the form of VME crate PCs (one per crate) and possibly a small dedicated machine cluster (comprising $<$10 PCs). The VME crate PCs host the various hardware supervisor, event building and data analysis processes. The FED data are read via the VME backplane and event building is performed using a Gbit ethernet network. This operating mode will be the default during the integration and Start-Up phases of the experiment.

When using the global DAQ systems, the FED data are read out via their SLink interface [9], event building is performed using the CMS event builder, and the data analysis processes are hosted by the global computing farm (the crate PCs will host only the hardware supervisor processes). The data analysis is performed using the same CMSSW-based libraries as for the local DAQ mode.

One added complication when operating with global resources is that of trigger management. When running in local DAQ mode, trigger generation is under the control of the DAQ software. For the global DAQ mode, the trigger is issued centrally by the CMS global trigger system. It is envisaged that dedicated commissioning runs will be scheduled with reduced trigger rates that can be used as desired by the various subdetector systems. In this case, the DAQ software will configure the readout system on-the-fly during the run. The configuration of the readout system for a given event will be encoded in the data stream and used by the data analysis running on the global computing farm.

The ability to use the global DAQ resources is important, as this mode of operation offers vast improvements in terms of trigger rates and CPU processing power with respect to that available when using local DAQ. Due to large data volumes generated by the system during commissioning runs (typically $\sim$750 kB/trigger/crate), trigger rates are severely limited when the FEDs are read out via the VME backplane; system tests have shown that data rates of $\sim$5 MB/s were achieved for a fully populated VME crate (16 FEDs), thus limiting trigger rates to just $\sim$7 Hz. This compares unfavourably with a possible trigger rate of $\sim$2 kHz when reading out via SLink. This increase in trigger rate is highly desirable for those commissioning tasks that require precise measurements (and therefore large statistics), such as track-based timing alignment to synchronize the SST to LHC collisions.

IV. CMS Magnet Test Cosmic Challenge

The recent CMS Magnet Test Cosmic Challenge (MTCC) provided an ideal opportunity to test the DAQ software under operating conditions similar to those expected for the final experiment. The tracking unit, shown in Figure 3, comprised 130 modules within two Tracker Inner Barrel (TIB) half-shells, four Tracker Outer Barrel (TOB) rods and two Tracker End-Cap (TEC) petals. One FEC board and four control rings were used to control the front-end, and four FEDs were used by the readout system.

Several important milestones were achieved during the test. The DAQ software was fully integrated with the SST configuration database and the CMS Run Control environment. These developments allowed expert users, trained by the DAQ team prior to the test, to commission (and re-commission when necessary) the complete system via the Run Control interface in just a few hours. Complete prototypes of the Detector Control and Detector Safety Systems were used for the first time, as was a pro-

totype error logging and diagnostic system, providing real-time feedback on the operational status of the readout system. Once commissioned, stable running of the system using the global DAQ was possible for several hours. Approximately 25 million events were collected, of which 10 million events were collected with a magnetic field of up to 4 Tesla. Detailed detector alignment and tracking studies are now being performed offline.

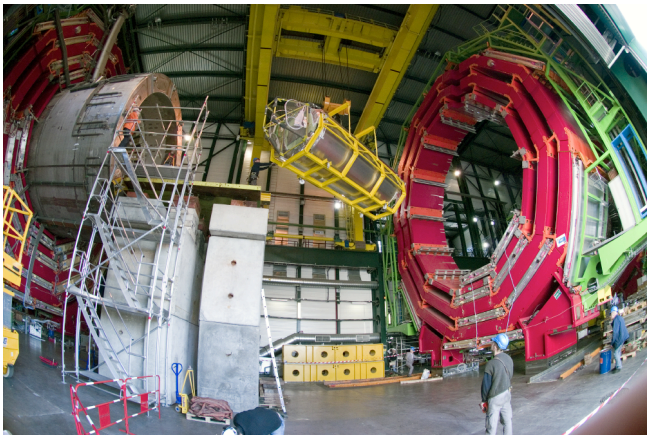

Figure 3: Installation of the tracker setup for the MTCC.

Online monitoring of the data quality using CMSSW software was also achieved for the first time. A small computing farm was used to parallel-process the raw event data and perform: unpacking of the raw event data from the FED buffer payloads; creation of the basic hit objects (known as *digis*) handled by the reconstruction software; assignment of the digis to a readout module (and therefore a geometrical position) using cabling information; booking and filling of histograms to provide online monitoring information. Remote online monitoring was demonstrated using a web-based client that subscribed to the monitoring histograms available on the computing farm nodes.

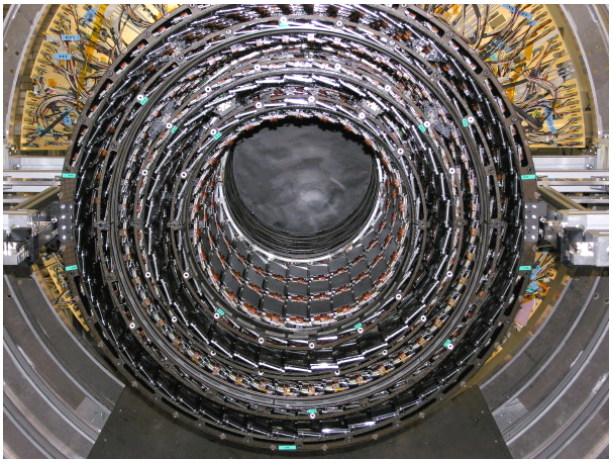

Figure 4: Assembly of the inner barrel at the TIF.

V. Tracker Integration Facility

The Tracker Integration Facility (TIF) is a large clean room environment in which the final SST is being assembled and commissioned. Large sub-structures, such as the TIB, are delivered from the various integration centres around the world and installed within the final mechanical support structure. The facility provides all the necessary services to fully commission and validate the detector prior to being transported to Point 5 and installed within the underground cavern. It is envisaged that final commissioning of the system will be done at the level of a tracker partition; this corresponds to approximately 2.5 M readout channels (ie, $\sim$25% of the total). Nine VME crates will be fully populated with FEDs in order to read out the tracker partitions in a configuration that is essentially identical to that which will be used for the final system. The DAQ software will be hosted on the VME crate PCs and online (distributed) analysis will be performed in order to provide real-time feedback.

Large sub-structures from all four partitions of the tracker have been installed at the TIF. Figure 4 shows the completed TIB backward sub-structure, comprising four barrel layers. Cabling of the detector front-end to the off-detector FEDs is in progress and large-scale validation tests have recently started.

In addition to the TIF, a Tracker Analysis Centre (TAC) has been installed on the CERN Meyrin site, in close proximity to the TIF. The centre will provide a small computing farm and mass storage so that the large data volumes generated during commissioning can be analysed in more detail offline. It is envisaged that the TAC will evolve into the tracker operations centre for experts and users alike during CMS operation.

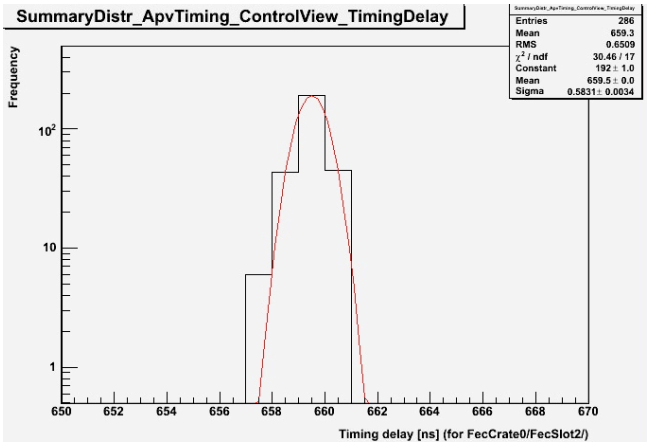

Figure 5: Timing delays measured for 286 channels of the readout system (where a "channel" in this sense refers to a pair of APV25 chips). The channels have been synchronized to better than 1 ns.

The analysis components of the DAQ software will be used both online to commission the detector and offline to perform detailed studies at the TIF and TAC. Detector experts are now using new tools developed within CMSSW that perform analyses of the raw data and generate summary plots that show system-wide information. An example is shown in Figure 5, which shows the timing delays measured for 286 channels of

the readout system (where a "channel" in this sense refers to a pair of front-end APV25 chips). The figure demonstrates that the 286 pairs of front-end chips (that read signals from ∼73k detector strips) have been synchronized to better than 1 ns.

Summary plots are essential when commissioning the detector, as they provide immediate feedback that can be easily interpreted by non-experts, allowing problems to be quickly identified and located. These summary plots can be generated online (and offline if necessary) by the DAQ software and are viewable at remote sites using web technology.

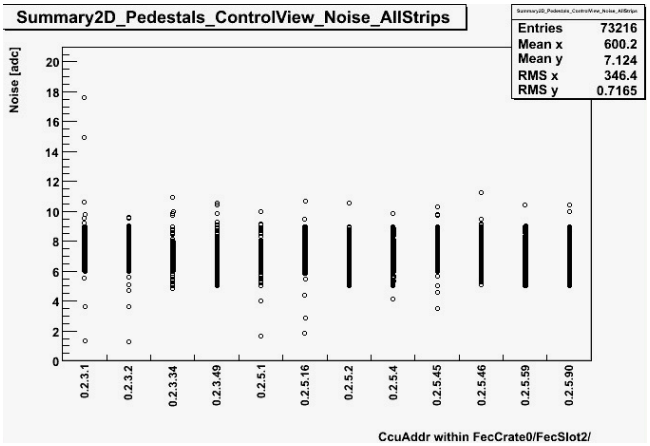

Figure 6: Channel noise (where a "channel" in this sense is at the level of a single detector strip), binned according to which rod the channel (detector strip) belongs. The twelve bins represent twelve different rod structures that are controlled by two control rings.

An example of a typical summary plot is shown in Figure 6. The plot shows the noise measured for ∼73k channels (where a "channel" in this sense is at the level of a single detector strip) of a TOB structure being commissioned at the TIF. The noise values are organized (binned) according to which sub-structure the channel belongs. For the example shown, each bin contains noise values from front-end modules controlled by the same CCU module (each of which controls a *rod* structure comprising six or twelve front-end modules). The plot clearly shows that a (non-calibrated) channel noise of ∼8 ADC counts is typical. Dead and noisy channels, exhibiting abnormally low and high noise values respectively, are clearly seen. The plot highlights the excellent quality and uniform behaviour of the tested system, with just a handful of detector strips ($\ll 0.1\%$) exhibiting anomolous noise values.

The CMSSW software is sufficiently flexible to produce a range of summary plots that display information on all aspects of the detector quality and performace. These plots act as an excellent diagnostic tool and will be used extensively during assembly and integration of the final silicon strip tracker.

VI. Conclusions

The CMS Silicon Strip Tracker (SST) requires complex procedures to optimally configure, calibrate and synchronize its 10^7 readout channels. The DAQ software provides the implementation for these procedures in a scalable design (using distributed computing) that will be able to handle the large data volumes produced during detector commissioning. The DAQ software is now a mature project and will be used to validate the quality and performance of the detector during the integration, Start-Up and operational periods of experiment.

Several important milestones were achieved during the recent CMS Magnet Test Cosmic Challenge, including the successful use of: the DAQ software to commission the system, detector control and safety systems, error diagnostic tools, and online monitoring. Stable operation of the readout system was achieved using both local and global data acquisition resources.

The final sub-detector is currently being assembled and commissioned at the Tracker Integration Facility. The DAQ software is being used to commission the sub-detector and new analysis tools will allow detailed online and offline studies to quantify the detector quality and performance prior to installation at Point 5.

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Electronic Devices for Controlling the Very High Voltage in the ALICE TPC detector

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Abstract

The Time Projection Chamber (TPC) is the core of the ALICE experiment at CERN.

The TPC Very High Voltage project covers the development of the control system for the power supply that generates the 100kV necessary for the drift field in the TPC.

This paper reports on the project progress, introducing the control system architecture from the electronics up to the control level. All the electronic devices will be described, highlighting their communication issues, and the challenges in integrating these devices in a PLC-based control system.

I. Introduction

The ALICE TPC is an 88m^3 cylinder filled with gas and divided in two drift regions by the central electrode located at its axial centre (Figure 1). The drift field is generated by a 100kV power supply. A Control System was designed in order to supervise and control the power supply.

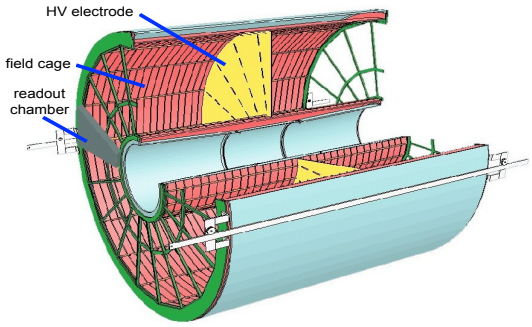

Figure 1: The TPC

II. System Overview

The Power Supply (PS) is a Heinzinger PNC 150000 neg-2, customized for the experiment needs [1]. It can provide up to 150kV DC. The PS is controlled by a RS232 interface. A Programmable Logic Controller (PLC) controls the ramping and several safety features. Thanks to its simple architecture and its stand-alone characteristic, the PLC provides more reliability than a common PC. The chosen PLC is a Schneider Electric P575634M. As it directly controls the PS through the RS232, dedicated communication routines were implemented. Currents in the resistor rods of the field cage are monitored as voltage drops over a resistor. Monitoring is performed by two ELMBs [2] reading 16 analog inputs. Each ELMB is connected to the PLC through CAN bus.

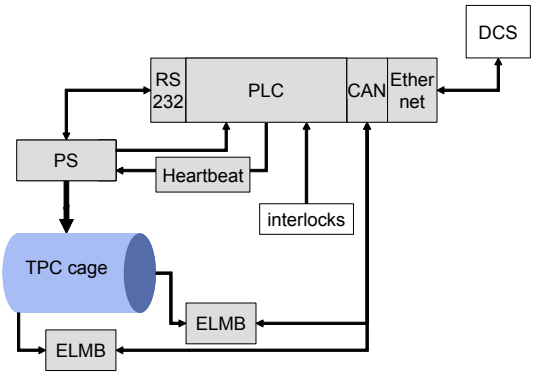

Figure 2: System overview

The PLC checks that the voltages remain in range. Other relevant parameters for the operation of the PS are monitored through 13 interlocks (digital inputs) connected to the PLC.

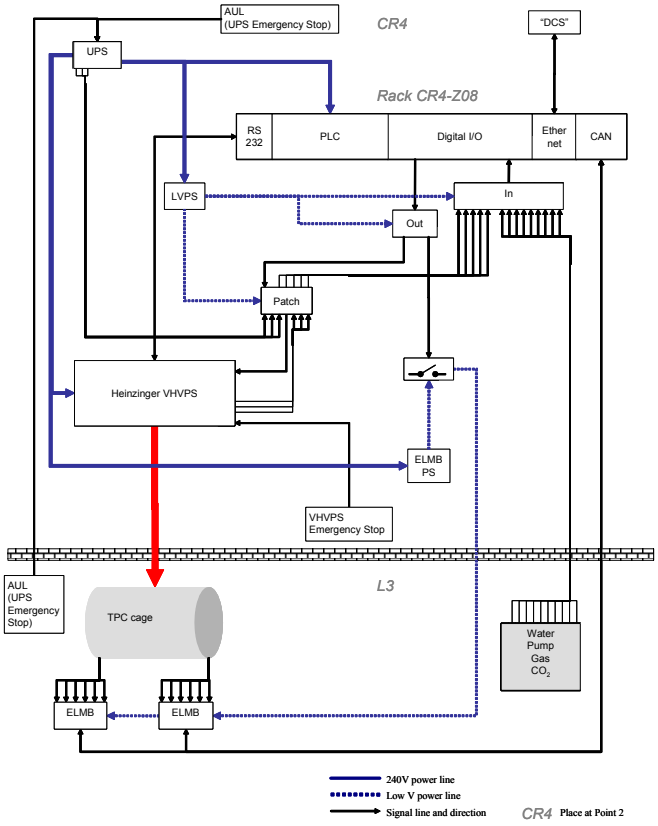

Figure 3: System detailed scheme

They provide status information about cooling water, UPS, gas condition and circulation. Figure 2 shows an overview of the system. The detailed scheme is presented in Figure 3.

III. Control System Features

Under operating conditions the system must safely apply a DC voltage of 100kV to the central electrode placed half way between the two end plates of the detector. Four resistor rods supply the proper potential to the field cage [3].

The Control System (CS) was developed following the TPC subsystem requirements, covering the following features: control and monitoring of the PS, of the current in the resistor rods, of the cooling, and some additional equipment.

A. Normal operation

Voltage must be applied by a smooth ramp. Each ramp step of 10kV is followed by one minute pause during which the voltage is held while the system is checked (Figure 4). After 50kV, check pauses last 2 minutes. During the periodical check pauses voltage and current over the resistor rods are verified. At all times, the control system checks the state of all the services used by the TPC (cooling, gas, UPS…). In case any problem occurs, the control system performs a ramp down.

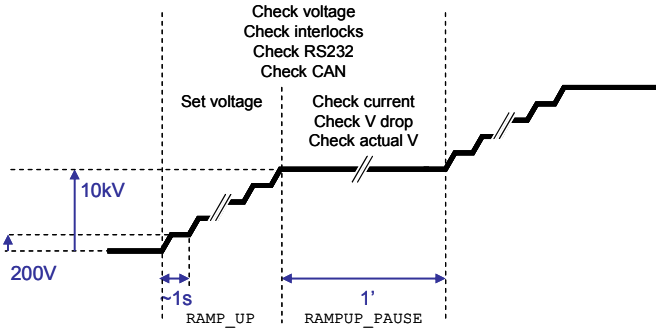

Figure 4: Ramping up scenario

Ramp down can be software-controlled (i.e. smoother and with intermediate pause) or direct (i.e. performed by the hardware slew rate limiter of the PS - faster). The former is executed in case of low priority faults, the latter in case of severe faults. All the parameters (final voltage, ramping speed, nominal values…) are downloaded by the supervisory system and accepted by the control system only in predefined, safe states. Final voltage reaches 100kV after about 20 minutes ramping.

B. Abnormal situation detection

Relevant external parameters need to be within a certain range to allow the operation of the PS. Such parameters are analog (voltage drops over the resistor chains and over the water) and digital (integral current, gas quality, water pump, UPS status) [4].

All relevant parameters are updated and compared to their nominal values at least once a second. In case one or more of these parameters are outside their nominal ranges, the voltage cannot be automatically ramped up. Should a similar situation occur during the standard operation (ramping up, fixed voltage at nominal value) an automatic ramping down of the output voltage is accomplished by the PLC. The reaction time of the PLC system which is controlling the PS is around 600ms after the deviation of one or more parameters is detected. However, before action is taken, several readings within about 3s are done to verify that the particular value is out of range over that time period.

Table 1: Error actions

Error	Action	Time [s]
Any interlock is open	SW ramp down	intlk dep
Voltage trip	SW ramp down	<4
ELMB not active	HW ramp down	<7
RS232 comm. failure	HW ramp down	<40
Current trip	HW ramp down	<1
HV Output is off	HW ramp down	<15
Enable Set Value is off	HW ramp down	<1
PLC not running	HW ramp down	<1

Table 1 summarizes the action to the possible abnormal situations that may occur. Errors associated with HW ramp down have higher action priority. The interlock error reaction time depends on the interlock. The long delay before detecting a RS232 communication failure was set in order to foresee the possibility of a temporary interruption of communication due to a strong magnetic field. If after 40s the communication has not yet recovered, then the ramp down is triggered.

IV. System Details

A. Power Supply

The PS was customized for matching the TPC requirements. Its main modification is the addition of an electronic controller that limits the slew rate in case of sudden power up or down. It is the first time that such a high voltage power supply integrates this feature. It makes use of an operational amplifier used as integrator and controlling a Pulse Width Modulator, as shown in Figure 5.

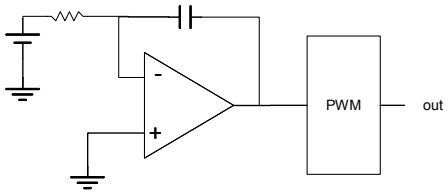

Figure 5: Ramp generator principle

The ramp generator can drive the output at a slew rate ranging from 333V/s to 1000V/s. This is performed in both ramping up and down.

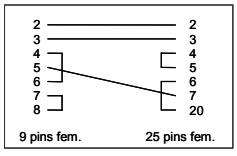

Figure 6: RS232 pin connection

The PS integrates a RS232 interface. This is used for communication PLC - PS. Data flow control is not provided by the PLC board. Therefore, commands and queries are sent through a low level layer implemented in the PLC routines. Those routines control that the data was correctly exchanged

between PLC and PS. The RS232 pins configuration is set to software handshake (Figure 6).

B. ELMB

Two Embedded Local Monitoring Boards (ELMB) are used for reading relevant analog parameters directly from the TPC. The ELMBs are placed on one side of the TPC and reads 8 channels. Analog input was set to the range 0-5V. The connector adapter used for voltage reading is the standard 1kΩ resistors network [5].

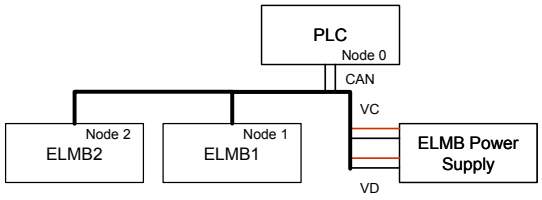

Figure 7: CAN bus connection

The loop interval between two SYNC messages was set to 50ms. This allows a total loop interval among all the channels of around 600ms. At every loop, the 8 channels are scanned and one PDO message is sent from each channel. Power lines are integrated in the CAN cable as shown in Figure 7.

C. Controller

The Schneider PLC controls the PS and monitors all the relevant parameters. It is a stand-alone system, able to react to abnormal situations independently from the supervision level status or actions. The PLC was configured and programmed through the Unity environment. Unity allows a mixed programming method that makes use of any PLC programming convention. Scripts and SFC programming were used in this project. The device was expanded in order to support RS232 and CAN bus connection. Relevant parameters are monitored through digital inputs, CAN connection to two ELMBs and RS232 interface.

Interlocks are directly connected to the PLC's digital inputs. For each interlock an action is triggered with different reaction time, after which the PLC starts a ramp down or does not allow to ramp up the system.

The ELMBs provide analog reading of voltage drops over the TPC resistor rods. CAN bus communication is implemented at the Application Layer. The information is retrieved at low level. For each scanned channel, the ELMB sends a Third Transmit Process Data Object (PDO3) message to the PLC CAN interface. The PDO3 frame is used for transferring analog values. A memory slot was allocated in the PLC for storing the message. The CAN interface stores in the memory the received CAN frame [6]. The data frame sent by the ELMB to the host (node 0 - the PLC) consists of the parts shown in Table 2.

Table 2: PDO3 frame

PDO3 COB-ID	Byte 0	Byte 1	Byte 2-5
380h+NodeID	Channel #	Ch status	ADC val.

Each ELMB (i.e. node) sends cyclically the value of each active channel. Byte 0 contains the channel number, while Bytes 2-5 contain the 32-bit ADC value in μV, LSB first. For each of the two ELMBs the PLC memory slot is periodically read (asynchronously). A routine was implemented for getting the PDO3 message, extracting information and storing it into an array. The same memory slot is then overwritten by the next incoming PDO3 message belonging to the next scanned channel. The time cycle is set to 600ms for each node. At each cycle 8 channels are refreshed for each node.

The PLC is interfacing to the PS through RS232. It allows control and monitoring of the PS: current (I) and voltage (U) setting, I and U reading. The communication was implemented at hand-shake level, since the PLC itself is not able to natively manage a message send and request. Basically, each send/receive command implies a routine similar to the example shown in Figure 8. The setting speed is around 200ms/message. The reading speed is lower (from 1s to 4s), due to the time needed by the PS to read the actual U or I.

Such an implementation is needed also to check if the communication is active. The PLC does not provide, functions for opening or closing the Com port.

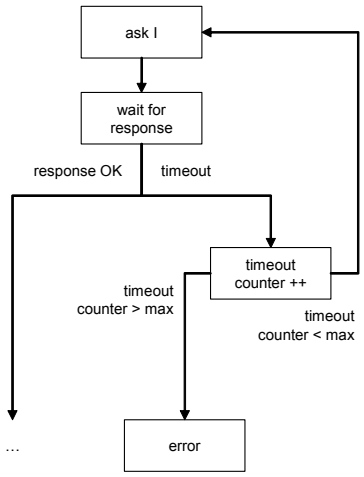

Figure 8: Example of the implemented RS232 messaging routine: asking for current

A RS232 communication failure may lead to a non controlled and potentially unsafe status of the system. For this reason the PS output is directly activated by an interlock controlled by the PLC. If the serial communication is lost, then the PLC sets the PS output to U=0V through the interlock. This triggers a fast ramp down. Such an interlock is implemented with a device working in the following way (see Figure 9 for a simplified schematic): it receives from the PLC a square signal of frequency 6.6Hz (heartbeat).

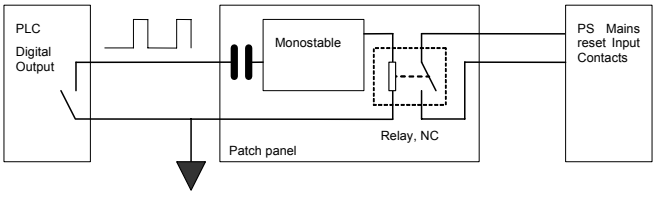

Figure 9: Heartbeat - interlock device

If the signal is on, the device keeps its output contact open. If the signal is flat, the output closes and the PS goes to 0V with internal slew rate limiter. Such an interlock is useful also for detecting a failure in the PLC. If the PLC is not able to produce the heartbeat during 220ms, then the interlock locks the PS to U=0V. A hardware ramp down is then triggered.

V. Conclusion

The system was successfully tested and used during the commissioning stage of the TPC.

The control system design had to match the main criteria of safety issues. Therefore, a PLC controlled and SCADA supervised architecture was chosen. PLC was preferred to PC for its reliability. Also, ELMB was found more adequate for taking measurements in the harsh environment of the experiment. Special effort was put on the communication within the electronic devices that, in conventional systems, are usually controlled in a transparent way by a common PC. Safety requirements were fulfilled.

The PLC is supervised by ETM PVSSII and ready to be integrated into the ALICE Detector Control hierarchy. A graphic interface allows full control by an operator. The safety procedures are anyway independent from the SCADA system. The output of the controlled PS is shown in Figure 10.

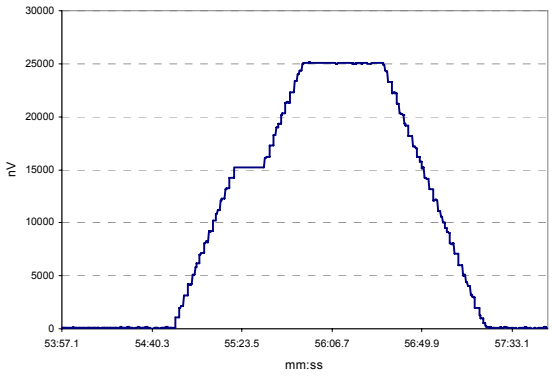

Figure 10: Ramp test of the PS. This plot shows the voltage drop over the last resistor. In this test intermediate voltage corresponds to U=3kV. Final voltage corresponds to U=5kV. Ramping speed was 100V/s. During normal operation the PS reaches 100kV.

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System tests and debugging with Python

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Abstract

The methodology used to produce the CMS Global Calorimeter Trigger (GCT) control and test software is described. An interpreted interface to an object-oriented model of the system has allowed the hardware to be controlled and tested in an intuitive interactive environment. This benefits both firmware and software designers, in terms of productivity, development cycle time, and firmware/software integration.

I. Introduction

Testing, debugging, integration and commissioning of complex custom hardware demands similarly complex software. One approach employed in high energy physics has been to produce an ad-hoc set of stand-alone executables that allow the operator to perform a pre-defined set of tests on the hardware. Other approaches employ more sophisticated single executables that can carry out a wide variety of tests and procedures, driven by a text or graphical menu system. We describe an alternative approach to software for tests and debugging, that has a variety of benefits over these methods.

Our approach is based around an object model of the system hardware and firmware, known as the *GCT Driver*, written in C++ and compiled for performance. It will become the API for final system software; this offers the advantage that the Driver will be well tested when the final software is required. Using an object model of the system provides excellent flexibility for adding functionality that may not be foreseen from the outset, and allows the Driver to be easily understood.

What distinguishes this approach from standard OO design practice, is that we produce bindings for the Driver such that it can be used within an interpreted language. This allows the Driver to be used in an interactive environment, and through scripts. Interactive use is ideal for debugging, where the operator can choose the exact sequence of operations as they are performed. The capability to run scripts is useful when particular sequences of operations are frequently used, but may require regular revision, or are not considered ready for inclusion in the Driver for other reasons. Obviously, the use of an interpreted language speeds up the development cycle, as the compilation stage is not required. In our experience with this design, the integration of software with firmware followed a cycle where initial tests were carried out interactively, then encoded in scripts. These would then undergo some cycles of modification and testing, before a mature version is included in the compiled Driver.

II. Software tools

The GCT Driver is written in C++, which offers both the object-oriented environment we require, and the capability to produce very fast byte code when required. The Driver object model includes the GCT specific hardware. We use the HAL (Hardware Access Library) [1], another object-oriented class library written in C++, to model and access the VMEbus and PCI-VME bridge used to control the GCT.

A. Python

"Python is a dynamic object-oriented programming language that can be used for many kinds of software development. It offers strong support for integration with other languages and tools, comes with extensive standard libraries, and can be learned in a few days." - http://www.python.org

Python [2] is used here to provide an interpreted object-oriented interface to the Driver. Being easily learnt offers the advantage that tests and debugging can be performed by anyone with some knowledge of the hardware system, and do not require detailed knowledge of the Driver software.

B. SWIG

"SWIG is a software development tool that connects programs written in C and C++ with a variety of high-level programming languages." - http://www.swig.org

SWIG [3] is used to automatically produce the python library that provides the interface to the Driver. SWIG takes as input one additional (trivial) header file per class. It is installed easily, hence producing the python interface to the Driver requires almost no additional effort.

III. CMS Global Calorimeter Trigger Software

The CMS Global Calorimeter Trigger comprises several different modules, populated with FPGAs [4], [5]. The GCT Driver design is shown in a pseudo-UML diagram in Figure 1 (which shows the inheritance structure on the same diagram as class associations). The system is accessed via a singleton system object (an instance of GlobalCaloTrigger), which contains STL vectors of objects that represent the cards in the system. Each card object contains STL vectors of FPGA objects that represent the FPGAs on the card. Functions common to all FPGAs, including register read and write, are implemented in the FPGA base class. Classes specific to particular FPGAs in the system inherit from the FPGA base class, and provide specialised functions. Finally, functions associated with common firmware blocks are encapsulated in classes named after the firmware block (eg. LUT, Buffer) and are members of FPGA sub-classes where required.

Each class provides two types of method. First, accessor functions are provided that return member components. This allows the user to trivially navigate the system in an intuitive way. This is of particular importance during interactive use via python. The second type of method invokes some operation on

the hardware. These are built up from the read and write methods provided by the FPGA class. Sub-classes of FPGA provide specific sequences of reads and writes, while the 'card' and 'system' classes provide methods that repeat a specific operation on multiple FPGAs or cards.

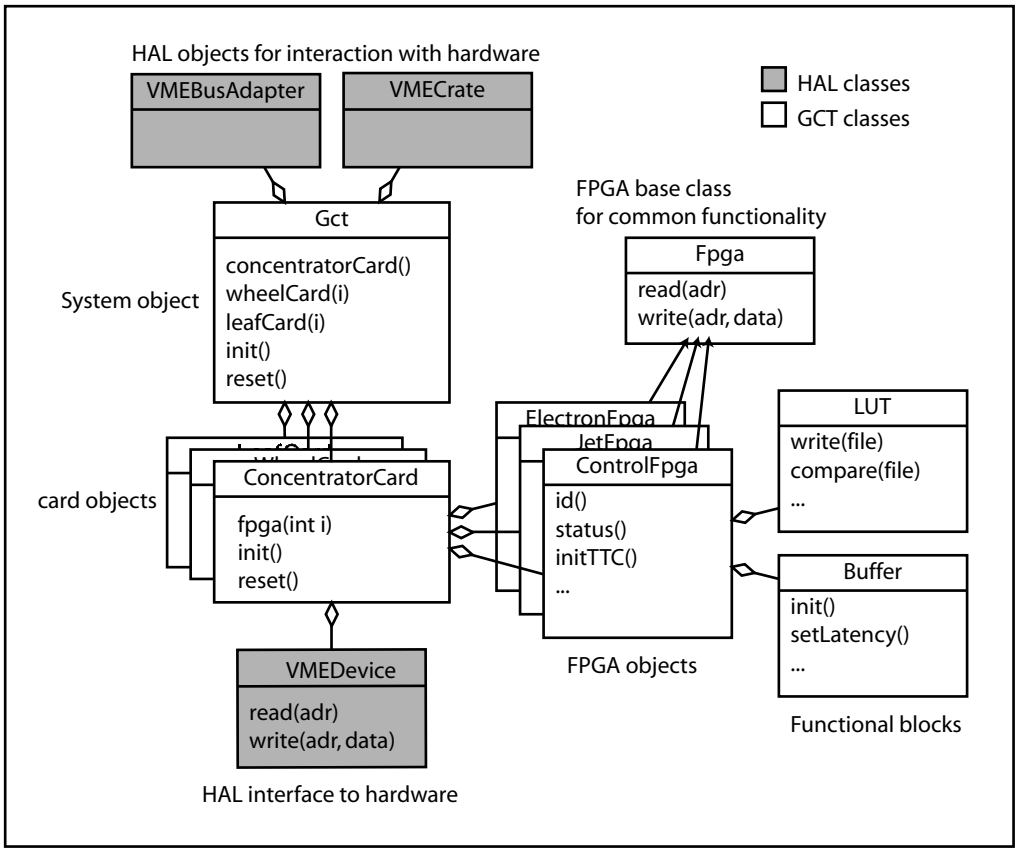

Figure 1: Pseudo-UML diagram of the GCT hardware driver

A. GCT software in use

At the time of writing, the GCT hardware is under production. However, this framework was used extensively in testing and debugging a previous version of the GCT hardware. The system started with nothing more than register read/write functionality implemented in the C++ model. This allowed the user to test the software/hardware combination via the python shell, then set up a more complex procedure in a script to test some more complex function. Once this function had become established, it would be migrated to the C++ model. This migration is a simple procedure, since the python script and the new C++ method make use of the same class library, and hence class, object and method names. A new round of testing would follow this, building increasingly complex functionality on top of code that is well integrated with the hardware. It should also be noted that the python language was simple enough that anyone familiar with the system could write complex test scripts; no prior software knowledge was required, or knowledge of the internal implementation of the GCT Driver or the HAL.

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[5] G. Iles *et al.*, these proceedings.

A Test Stand System for High-Energy Physics Applications

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Abstract

The Front-End R&D group at Fermilab has been developing pixel hybridized modules and silicon strip detectors for the past decade for high-energy physics experiments. To accomplish this goal, one of the activities the group has been working on includes the development of a flexible high-speed and high-bandwidth data acquisition and test system to characterize front-end electronics. In this paper, we present a general purpose PCI-based test stand system developed to meet the stringent requirements of testing silicon strip and pixel detectors. The test stand is based on a platform that is flexible enough to be adapted to different types of front-end electronics. This system has been used to test the performance of the electronics for different experiments such as BTeV, CDF, CMS, and Phenix. The paper presents the capabilities of the system and how it can be adapted to meet the testing requirements of different applications.

I. PCI Test Adapter

A peripheral component interconnects (PCI) based test stand was developed to meet the high-speed readout requirements of the electrical characterization of the silicon strip and pixel modules used in HEP experiments. This test stand is developed around a PCI test adapter (PTA). The PTA has a Xilinx Virtex4 field programmable gate array (FPGA) that gives it the flexibility necessary to meet, for example, the changing demands of the pixel module characterization (e.g., as new ICs are designed) and different applications. Figure 1 shows a functional block diagram of the PTA.

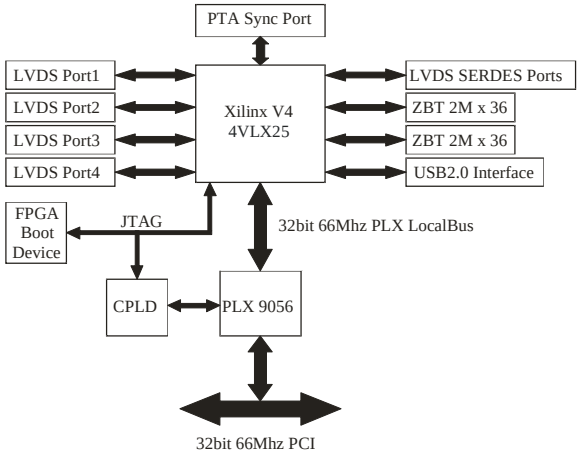

Figure 1: Functional diagram of the PTA

The data bus from the pixel modules is connected to low-voltage differential signaling (LVDS) ports, and the data is packed by the FPGA and stored in the local ZBT memory banks until further readout by the PCI bus. A 66MHz PCI-mastering device (PLX Technology PCI9056) maps the local ZBT memory banks to the computer's memory using direct memory access (DMA). The PTA has other features such as a USB2.0 interface (useful for applications using a laptop computer) and a pair of high-speed serializers - deserializers (SERDES) used to expand the data traffic capabilities of the board. Figure 2 shows a picture of the PTA board.

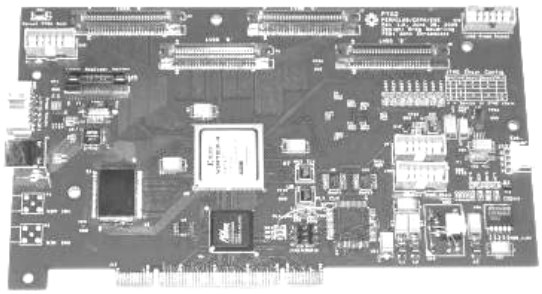

Figure 2: Photograph of the PTA

The PTA is distributed with drivers and middleware that works in both Windows and Linux environments. Data acquisition and data analysis software have been developed for both operational systems as well. A screenshot of the data analysis software is shown in Figure 3.

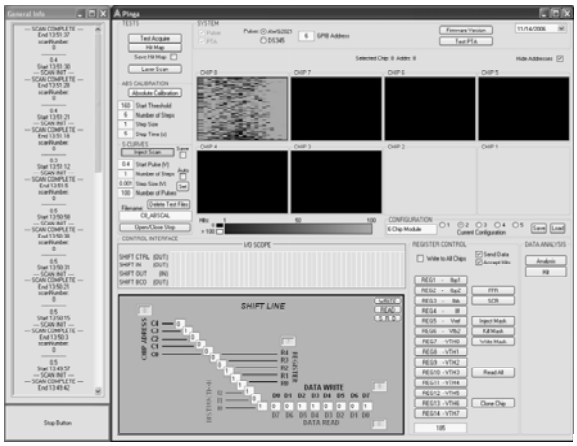

Figure 3: Screenshot of the DAQ software

Over 200 PTAs have been produced, distributed, and used in test stands around the world. One of these applications is testing pixel modules using the third version of the Fermilab pixel chip (FPIX2). Figure 4 shows a photograph of this test stand at Fermilab.

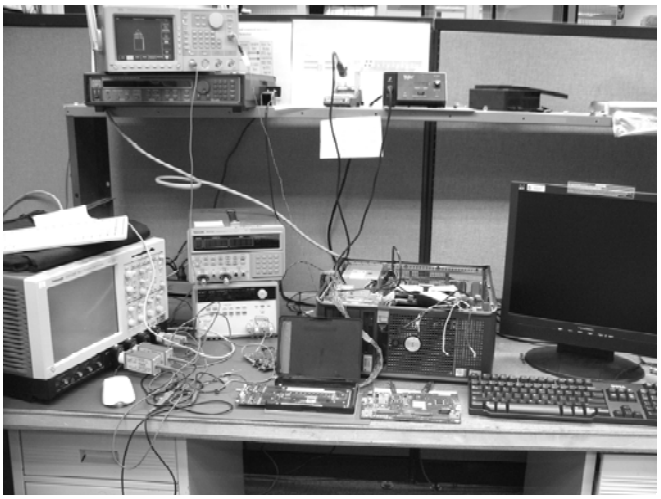

Figure 4: Photograph of the test stand with a PTA and pixel module

A. PTA Specifications

PCI: The PTA uses the PCI9056 Bus Mastering PCI interface from PLX. The PLX9056 is a 32bit/66Mhz PCI Master that has a 32bit/66Mhz local bus.

FPGA: The PTA uses the Xilinx 4VLX25 Vertex4 FPGA. The Vertex4 series FPGA's have built in LVDS termination resistors that save PCB space and make it much easier to change designs.

LVDS Ports: The PTA has 4 I/O connectors. In the default PTA configuration the 4 ports will be configured for LVDS. The LVDS termination resistors can be turn on and off inside of the Xilinx FPGA. No resistors will have to be placed and/or removed when the PTA is used for different test stands. Each connector has 18 pairs of signals, and 6 pairs of grounds. The signal pairs can be used as 18 differential pairs or 36 singled ended signals.

Memory: The PTA has two banks of 8M ZBT memory that runs up to 266MHz. The Xilinx FPGA has 1.3Mbits of memory.

USB: The PTA uses the Cypress FX2 USB2.0 interface chips. The PTA has a connector for an external power supply so it can be powered out of a PC. The PC is then able to use the PTA through the USB port. The Cypress FX2 chips have transfer rates above 20MB/s.

Miscellaneous: The PLX9056 is able to boot the Xilinx FPGA via the JTAG port. The Virtex4 FPGA has LVDS SERDES ports. Each port has TX data and clock pairs and RX data and clock pairs. Depending on the speed grade of the FPGA, the SERDES can run up to 1Gbit/Sec.

II. Front-End Module Interface Card

The Front-End Module Interface Card (FEM) is a test module designed to support test stands instrumented with the PTA [1]. The FEM is used in tandem with the PTA to supply digital and analog signals to the devices under test. In summary, the FEM has the potential to replace four of equipments commonly used to test front-end electronics in HEP: pulser, low voltage supply, high voltage supply, and temperature sensor signal conditioner. Figure 5 shows the functional diagram of the FEM.

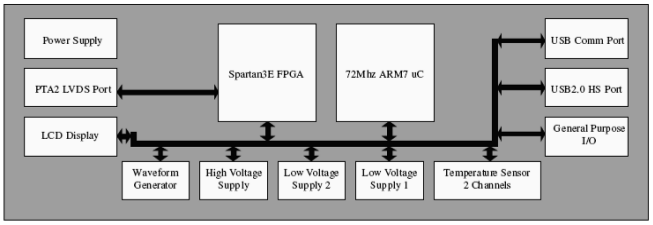

Figure 5: Functional diagram of the FEM

A. FEM Specifications

Microcontroller: The FEM uses an ARM7 LPC2348 microcontroller from NXP Semiconductor. The LPC2348 is the heart of the FEM as it controls all of the various test module functions and communicates with a PC via a USB2.0 high speed interface.

FPGA: The Spartan3E FPGA is used for various FEM glue logic, thus allowing a flexible interface between the FEM and the various front-end devices under test.

USB2.0: The USB2.0 High Speed Port is used by the FEM to communicate with a PC running the test stand software. The port is a high speed port that can do USB bulk transfers at 480Mbps.

USB COMM: The USB COMM port is used by the microprocessor for debugging purposes. It can be used to connect the FEM to a terminal for debuggin messages or it can be used to update the LPC2348's boot loader firmware. This port will not be used in normal operation.

RTD Temperature Sensor Interface: The FEM can monitor two different RTD temperature sensors. The sensors are placed near or on front-end electronics under test.

Low Voltage Supplies: The low voltage supplies are used to power the devices under test. Normally one channel of the supply is used for the analog part and the other for the digital part of the device under test. The output voltage is programmable via the USB port and can be adjusted from 1.2V to 4.0V. Each supply can source 1A of load current. Both the voltage and current are monitored by the microprocessor and passed on to the test PC via the USB port.

High Voltage Supply: The FEM's voltage is used to bias the sensor on the front-end module. The output voltage has a range of 0VDC to -500VDC and can supply 2mA of current. The voltage and the current of this power supply can be monitored via the USB port.

Waveform Generator: The waveform generator is used to generate a pulse that is used to inject charge in the preamplifier of the front-end chips. The waveform generator uses a DAC connected to the FPGA to generate the pulse. All of the pulse attributes can be programmed via the USB interface.

LVDS Port: The LVDS port is a standard connector to interface to the PTA.

General I/O Port: The I/O port is used for general purpose signals that can be configured as inputs or outputs as needed. The outputs can source/sink 24mA @ 3.3V/5V and the inputs can handle 5V signals.

LCD Display: The LCD display is used to show current FEM operating conditions. It can be programmed to show the monitored voltages and currents, RTD temperatures, and various other things.

Mechanical Specifications: The FEM is housed in a 6.3"H X 6.3"L X 2.1"H extruded aluminum enclosure.

Input Power Supply: The FEM uses an external desktop switching power supply as its main supply. The supply is rated at +12V, 7A.

III. Case Studies

A. Test of Pixel Multichip Modules

One of the recent applications of the PTA is the test and characterization of the pixel multichip modules for the Phenix LDRD project at Brookhaven National Laboratory [2]. The pixel sensor is bump-bonded to the Fermilab Pixel chip version 2.1 (FPIX2.1). The readout chip is wire bonded to a high-density interconnect (HDI). Figure 6 shows a picture of the pixel sensor bump-bonded to 8 FPIX2.1 chips. The pixel module is assembled onto a thin-film HDI. The HDI is then wire bonded to a test card, and the test card has matching connectors to the PTA.



Figure 6: Pixel multichip module

The 8-chip pixel module has a total of 22528 pixels that read out data at a maximum rate of 700 Mbps. The serial lines out of the FPIX2.1 chips can be configured so that data is read out in 1, 2, 4, or 6 parallel lines per chip. The PTA supports all these different readout modes. The readout chip doesn't require any trigger; hence there is a continuous flow of data through the serial lines. When the chip has no data to transmit, the synchronization word is sent out to the PTA continuously. This provides steady power consumption with no current bursts and no need for DC balancing the transmission lines. Figure 7 shows the data structure out of the FPIX2.1 chip into the PTA when 1 serial line is used.

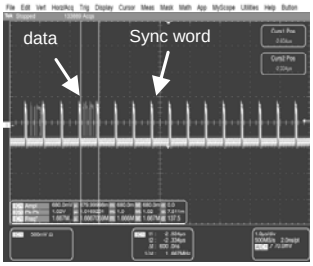

Figure 7: Data output from FPIX2.1 into PTA

The test stand software also does the full characterization of the pixel modules. Figures 8 show the results of calibrating the digital registers of the FPIX2.1 chip and the pixel sensor using X-ray sources with different energies.

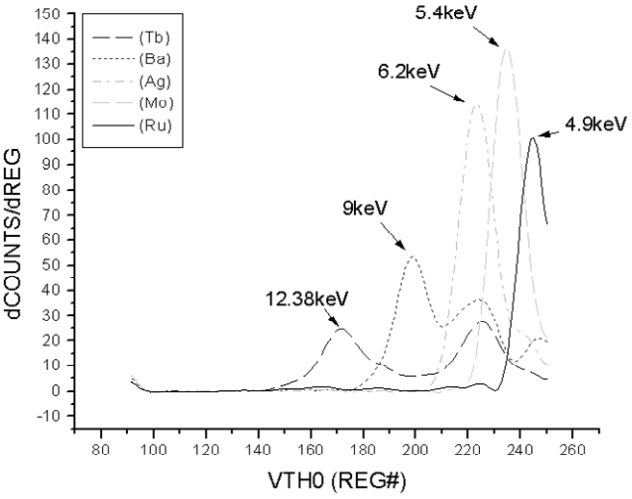

Figure 8: Test results of a pixel sensor using radioactive sources

The test stand also allows the visualition of the hit map using a beta gun (Sr^{90}). The hit map is very useful for the determination of the quality of the bump-bonds. Figure 9 shows the hit map of the pixel sensor when the radiactive source is shined at the edge of the module. The gap between the chips is shown.

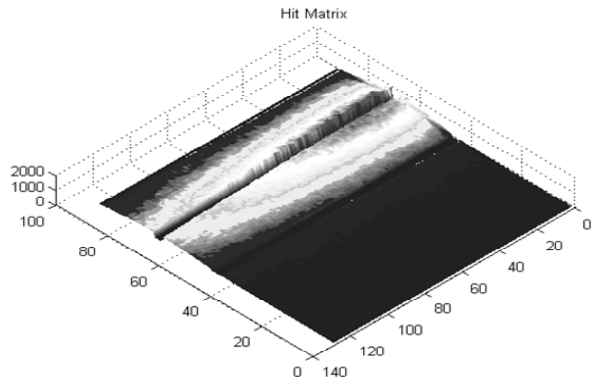

Figure 9: Hit map detail between two FPIX2.1 chips

Figure 10 shows the hit map of the region where the high voltage bias was connected to the sensor using silver epoxy. In this figure it is possible to observe the footprint left by the high voltage connection. When an aluminum wire bond is used no foot print can be seen on the hit map

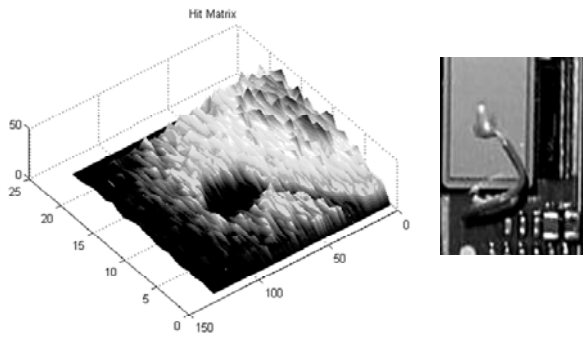

Figure 10: Hit map footprint of bias connection

B. *Test Beam DAQ*

The scalability capabilities of PTA allowed us to use the test stand described in the previous section as the building block to develop a complete DAQ for the test beam of pixel modules. The functional diagram of this DAQ is shown in Figure 11.

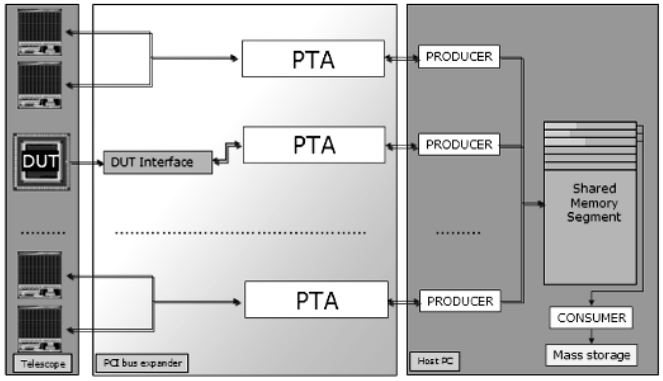

Figure 11: Functional diagram of the test beam DAQ

Each set of two pixel boards located at the telescope is connected to a single PTA sitting on the PCI bus of the DAQ computer. This application is employing a 13-slot PCI bus extender that allows the connection of 13 PTA cards. The arrangement of the test beam pixel telescope and the device under test is shown in Figure 12.

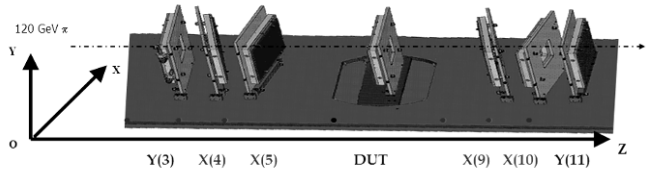

Figure 12: Telescope of 6 pixel detectors and device under test (DUT)

The telescope has a total of 6 pixel planes, 2 Y-measurement planes and 4 X-measurement planes. The pixel cells are 50 μm × 400 μm, and each chip has 2,880 cells. The device under test (DUT) is placed in the center of the telescope. The track projection error achieved by this telescope is ~3 μm on X-direction and ~8 μm on Y-direction.

1) *DAQ Architecture*

The FPIX2.1 chips does not require a trigger to send data out, hence the PTA-based DAQ must be fully data driven DAQ. Hits from the detectors are sent to readout as soon as they are above threshold (the process is driven by a clock synchronized with the accelerator clock). Each hit is tagged by PTA cards with a hardware generated time-stamp. An event, defined as "*a collection of equal time-stamp hits from multiple detectors*", is built by the consumer process using an efficient sorting algorithm.

Data is produced by the FPIX2.1 at a variable rate while the host computer receives them at its own rate (depending upon CPU clock and processor current activity). The PTA has been programmed to get data from the FPIX2.1 chips and to act as an intermediate rate-balancing buffer. This is accomplished by a periodic switching of the data flow between two RAM banks.

The architecture has been designed to allow for a continuous, lossless sustained data-rate. In a test-beam setup several detectors are read-out simultaneously and data made available to the even-builder. The DAQ framework (C++) allows adding and replacing different event-building algorithms by defining an abstract interface to the appropriate implementation. This allows for different detectors, with different event-building strategies, to be read-out by the same DAQ system.

IV. Conclusions

A multi-purpose DAQ system has been developed to test and characterize front-end electronics for HEP applications. The system is flexible enough to accommodate different types of detectors as well as different event-building strategies. The system has been used extensively in test beams as well as in various laboratories to characterize detector performances.

The PTA and the FEM have proven to be a useful, low cost and efficient approach to readout detectors in demanding environments like bench test and beam test. The design and implementation of a low/mid-size DAQ system in C++ has been successfully achieved, and the code is available to future collaborators upon request.

V. References

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[2] Turqueti, M., et al., "Pixel Multichip Module Development at Fermilab for the PHENIX Experiement," IEEE Nuclear Science Symposium, San Diego, November 2006.

”CMAD”, a Full Custom ASIC for the Upgrade of COMPASS RICH-1

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Abstract

An 8 channel, full-custom ASIC prototype, named ”CMAD”, designed for the readout of the RICH-I detector system of the COMPASS experiment at CERN is presented.

The task of the chip is amplifying the signals coming from fast multi-anode photomultipliers and comparing them against a threshold adjustable on-chip on a channel by channel basis.

CMAD, developed using a 350nm commercial CMOS technology, occupies an area of $4.7x3.2mm^2$ and consumes $26mW/Ch$ power from a 3.3 V single source.

I. Introduction

COMPASS [1] is an experiment at the CERN SPS designed to study the structure and spectroscopy of hadrons with diverse types of high intensity beams. One of the key components of the experimental apparatus is a Ring Imaging CHerenkov (RICH) detector, used to perform particle identification.

In order to improve the reconstruction efficiency of the RICH, an upgrade is under development [2]. The experience gained with the first physics runs has, in fact, shown that a trigger rate of 100 kHz and a single channel rate of 5 MHz should be sustained in order to reach optimal performance. These tight requirements can be achieved by detecting the photons produced in the sensitive volume by photomultiplier tubes equipped with fast read-out electronics. The granularity of the system demands the use of compact multi-anode photomultipliers (MPT). The increased event rate that the system has to cope with has motivated the development of a new front end (FE) ASIC. This chip will replace the MAD-4 [3] presently used in the read-out of the RICH-I.

This chip named CMAD is presented in this paper. Produced in AMS 0.35 μm CMOS technology, the chip performs binary read-out of the MPT signals.

Section II gives an architectural overview. Section III deals with circuit design. Section IV summarizes preliminary test results.

II. Architecture

Fig. 1 shows the architecture of a single channel. Each processing channel features a low-noise transimpedance amplifier followed by a shaper with 10 ns peaking time, a baseline restorer, a comparator, a programmable oneshot and an LVDS driver.

The gain of the preamplifier can be adjusted from 0.4 mV/fC to 1.2 mV/fC in steps of 0.08 mV/fC. This allows to compensate at least partially for the channel-to-channel gain variation of the MPTs. Additionally, the threshold of each comparator can be adjusted on a channel by channel basis via a local 8-bit digital to analog converter (D/A). The gain of the front-end and the D/A codes are programmed using a digital control unit and the I2C standard.

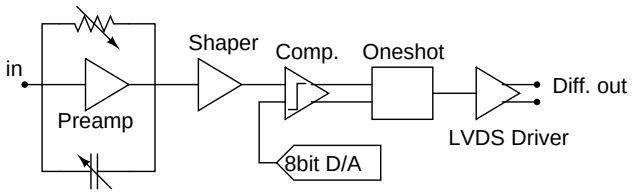

Figure 1: Binary read-out architecture of a single channel.

The fast shaper shown in Fig. 2 is based on a class AB operational amplifier [4] around which two feedback networks are implemented. A fast path performs high frequency filtering while a slow feedback provides the AC coupling with the previous stage and guarantees baseline stabilization [5].

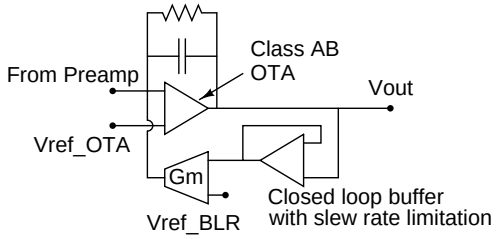

Figure 2: Architecture of the shaper in the channel.

A fast unity gain buffer with limited slew rate is used in the baseline control loop. Fast output signals at the output of the shaper are clipped before arriving at the transconductor stage. The baseline stabilization circuit is designed to reduce the baseline shift to less than 3 mV for output pulses with a 3 V amplitude and 10 MHz rate.

The peaking time at the output of the shaper is 10 ns. The system has been designed to cope with a rate in excess of 5 MHz/Ch. The output pulses are stretched by a programmable one-shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels (Fig. 1).

III. Circuit Design

Fig. 3 shows the implementation of OTA used within the shaper. The class AB CMOS OTA circuit dissipates 3 mW of

static power from a 3.3 Volts power supply and drives a 10 pF load with a slew rate of more than 500 $V/\mu s$.

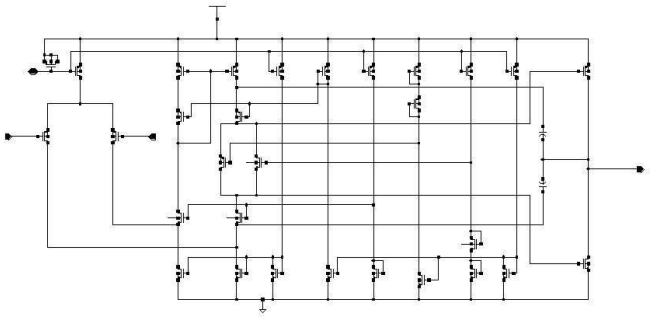

Figure 3: CMOS AB class OTA.

In the binary architecture given in Fig. 1, a global D/A can not be used since each of the read-out channels needs its own comparator that operates independently from the rest. This brings the necessity of a low power and small area D/A architecture, since it would be used for each read-out channel and thus more than once per chip.

Conceptually, the simplest D/As use a binary-weighted architecture, where n-binary weighted elements (current sources, resistors or capacitors) are combined to provide an analog output (n = D/A resolution). Digital encoding circuits are minimized, but the difference between the MSB and the LSB weights increase with increasing resolution, making accurate element matching difficult.

Among others like Kelvin divider or segmented architectures, the R-2R, or ladder, architecture relaxes component-matching requirements since only two component values are required in a 2:1 ratio. The R-2R architecture can be configured as a voltage- or current-mode D/A, together with different advantages and disadvantages.

A drawback of a current-mode R-2R architecture is the inversion introduced by the opamp which usually exists as an output current-to-voltage converter. Another disadvantage is the complicated stabilization of the opamp due to the fact that the D/A output impedance varies with digital input code. Current mode operation also results in higher glitch, since the switches connect directly to the output.

Advantage of voltage-mode R-2R configuration is that the output voltage has constant impedance, thus simplifying amplifier stabilization. Glitch generated by switch capacitance is also minimized. The drawback of voltage-mode R-2R configuration is that the reference input impedance varies widely, so a low-impedance reference must be used. Also, the switches operate from ground to Vref, restricting the allowed range of the reference.

CMAD implementation employs Low Drop-Out regulators (LDOs) for setting the reference voltage and bias current of the D/A together with other blocks. The technology used (0.35 μm) has relatively a high analog performance compared to recent low feature size technologies, so the amplifier compensation is easily achievable for the whole operation range. Relatively a high accuracy of matching is also feasible with proper layout.

Concerning the above discussion, CMOST-only current-mode R-2R architecture is a suitable solution as it is composed of only transistors that are compact and that consume very low power. An important concern is also the output impedances driving the comparator, namely the outputs of the shaper and the D/A. For proper functioning of the comparator input stage which is basically a differential pair, it is desired to equalize these impedances. The shaper has a low output impedance, thus requiring the same for the D/A.

Fig. 4 shows conceptually the architecture of the small area-low power 10-bit D/A used for setting the threshold of the comparator [6]. In such an architecture, transistors in the ladder do not necessarily emulate identical resistor values but instead, successful operation is based on linear current division principle [7]. The accuracy of the division technique used is based on the characteristic I-V curve matching of the two transistors but not on their linearity [8].

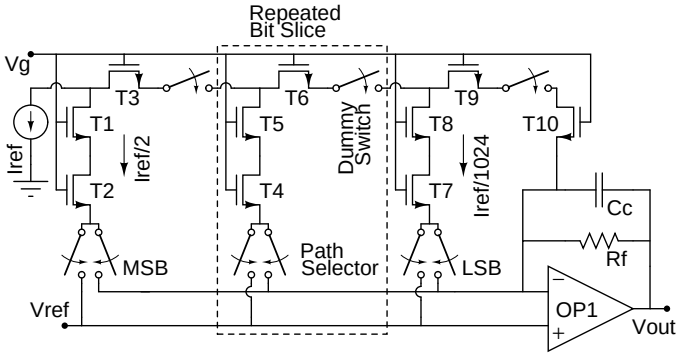

Figure 4: 10b CMOS-Only R-2R architecture.

In operation, first two MSBs are set globally together with the base line and the effective resolution required by the channel is 8 bits. Additional pads are also provided for the flexibility of disabling the on-chip LDO reference to be able to apply external sources. The LSB, thus the resolution, of the D/A can be adjusted for different conditions, in this way.

Power consumption of the D/A in Fig. 4 is approximately 1.1 mW including the opamp. A current mirror implementation with the same functionality and power consumption would exhibit a much larger output impedance. CMOST-only R-2R core operates with 50 μA of current which is negligible compared to the one consumed by the opamp.

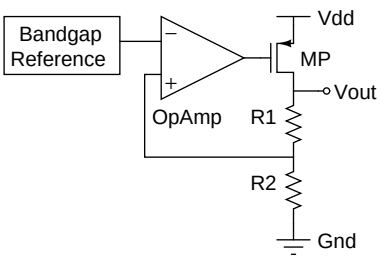

Figure 5: LDO voltage reference.

On-chip biasing is implemented via reference sources based on LDOs driven by band-gap voltage sources, as seen in Fig. 5. Linear voltage regulators use an active pass element (MP) to reduce the input voltage (Vdd) to the regulated output voltage (V_{OUT}). Linear voltage regulators force a fixed voltage level to appear at the output terminal.

The LDOs implemented for CMAD are optimized for sub-circuit requirements and consume 0.9 mW from 3.3 V single source.

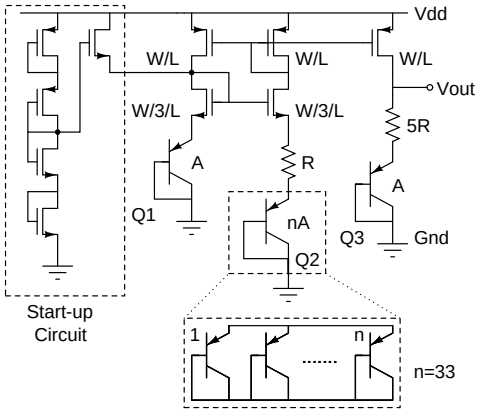

Figure 6: Implemented opamp-less band-gap reference.

Fig. 6 shows the implementation of the opamp-less band-gap reference driving the LDOs. The reference voltage output is given as $V_{REF} = V_{BE3} + 5V_T ln(n)$ where V_{BE3} is the B-E potential difference of Q3, V_T is the thermal voltage and n (=33) is the area ratio between Q2 and Q1. Band-gap in Fig. 6 consumes 93 μW from 3.3 V single source.

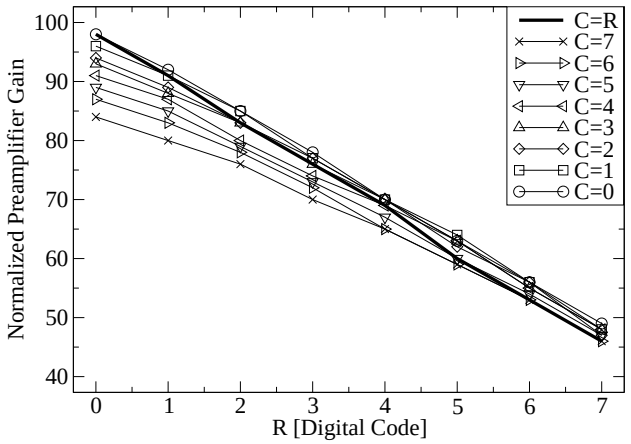

Figure 7: Measurement results for adjustable gain of the preamplifier as a function of R and C binary D/A converter inputs.

IV. Test Results

Measurements showed good agreement with simulation results. Gain and the output pulse shape of the preamplifier is adjustable by controlling the values of capacitive and resistive components in the feedback path. These component values can be set either independently or in a correlated manner in order to preserve the shape of the output signal.

The gain of the preamplifier is a strong function of the resistor as seen in Fig. 7. Gray curves show the gain variation due to change in resistor while the capacitor value is preserved. In order to keep the signal with the optimum shape, the capacitor should be adjusted in such a way that the time constant remains the same. The black curve (R=C) shows the gain for which the digital inputs are equal, thus the output signal shape is maintained. As seen in Fig. 8, capacitor value has only a slight effect on the preamplifier gain. It is utilized to adjust the time constant but not the gain itself. An increase in the binary code for resistor must be accompanied by an increased capacitor code. Reverse logic is used internally in the chip to preserve the direction of the digital code change maintaining optimum signal shape.

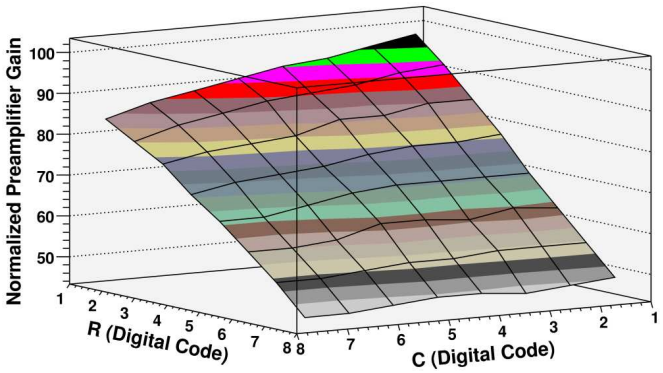

Figure 8: Measurement results for adjustable gain of the preamplifier as a function of R and C binary D/A converter inputs.

Linearity of the preamplifier output is important for proper operation. Fig. 9 shows the measurement results. In the upper plot, circles represent the normalized preamplifier output values and the solid line is the linear fit. The nonlinearity is less than 2%, as seen in residual between data and linear fit given at the bottom.

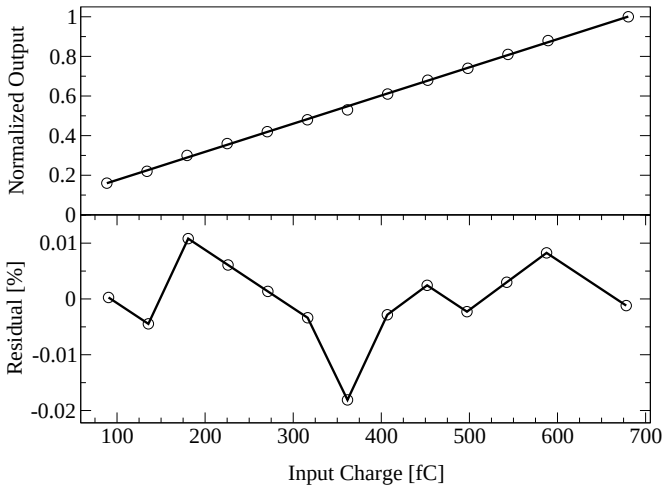

Figure 9: Gain linearity of the preamplifier; measurement and linear fit (upper plot) and the difference between fit and measurement.

V. CONCLUSION

An 8 channel, full-custom ASIC prototype, named CMAD, designed for the readout of the RICH-I detector system of the COMPASS experiment at CERN is presented.

In CMAD, threshold of each channel can be adjusted independent from the other channels. Thanks to low noise preamplifier, lower thresholds can be set individually to improve front-end performance. Table 1 summarizes the specification details. The ASIC, shown in Fig. 10, implemented in AMS 0.35 μm commercial technology, occupies $4.7x3.2mm^2$ of area and consumes $26mW/Ch$ power from a 3.3 V single source.

Table 1: CMAD Specifications

Technology	0.35 μm
Number of Channels	$8/Chip$
Preamplifier Gain Range	0.4-1.2 mV/fC
Preamplifier Gain Resolution	0.08 mV/fC
Peaking Time	10 ns
Speed	$>$5 MHz/Ch
Chip Size	4.7x3.2 mm^2
Power (w/o LVDS Drivers)	26 mW

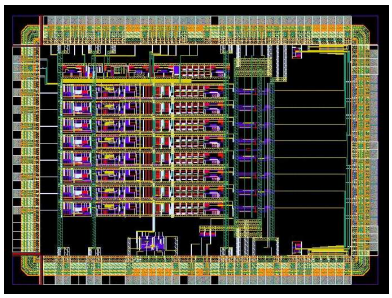

Figure 10: CMAD chip layout.

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Radiation Tolerance Qualification Tests of the Final Source Interface Unit for the ALICE Experiment

For the ALICE collaboration

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Abstract

The ALICE Detector Data Link (DDL) is a high-speed optical link designed to interface the readout electronics of ALICE sub-detectors to the DAQ computers. The Source Interface Unit (SIU) of the DDL will operate in radiation environment. Previous tests showed that a configuration loss of SRAM-based FPGA devices may happen and the frequency of undetected data errors in the FPGA user memory area is also not acceptable. Therefore, we re-designed the SIU card using another FPGA based on flash technology. In order to detect bit errors in the user memory we added parity check logic to the design. The new SIU has been extensively tested using neutron and proton irradiation to verify its radiation tolerance. In this paper we summarize the design changes, introduce the final design, and the results of the radiation tolerance measurements on the final card.

I. The ALICE Detector Data Link (DDL) and Radiation

The ALICE Detector Data Link (DDL) is a high-speed, duplex, point-to-point optical link designed to interface the readout electronics of all the ALICE sub-detectors to the DAQ computers in a standard way [1]. The DDL consists of the Source Interface Unit (SIU), an optical cable of up to 300 meters, and the Destination Interface Unit (DIU). The DIUs are integrated onto the Read-out Receiver Cards of the DAQ (D-RORC). The DDL provides enough bandwidth to transfer data from the detectors to the DAQ at 200 MB/s per link [2]. The SIU will be attached to the Front-end Electronics; hence, it will be exposed to the radiation caused by the interacting particles. According to the latest simulations, the highest radiation level for the SIU card is expected at the inner radius of the TPC detector [3], where the total ionising dose is 1.6 krad, the neutron fluence is 3.9×10^{11} neutrons/cm^2, and the proton fluence is 8×10^9 for 10 years of operation [4]. The 1MeV neutron equivalent total hadron fluence is 1.5×10^{11} neutrons/cm^2. (The SIU card is not placed directly into the inner tracking system, where the radiation is even higher. From those sub-detectors data is transferred through custom radiation hard links before it is being multiplexed and sent over the DDL.)

The SIU hardware consists of three main components. The DDL protocol and additional logic functions are implemented in a programmable logic device (FPGA). The prototype SIU card has been built around an SRAM-based Altera APEX-E FPGA. The electrical transceiver performs serial-to-parallel and parallel-to-serial data conversion. The full-duplex optical transceiver makes the conversion between the high-speed differential electrical data and the optical signal. Auxiliary components are voltage regulators and a crystal oscillator.

The first radiation tolerant measurements of the prototype SIU components and the prototype SIU card are described in details in [5]. According to these measurements several electrical and optical transceivers, crystal oscillators, and voltage regulators have successfully passed the tests. We had not observed any functional errors at these components and the single-bit transmission errors of the optical transceivers also proved to be much below the permitted error rate.

According to these first measurements we found that from point of view of radiation tolerance, the most vulnerable component of the whole SIU card would be the FPGA device. We identified two issues that had to be investigated in details, namely the *device configuration loss* and the *data corruption* due to SEUs in the embedded user memory and the registers. In this paper, we shortly summarize these two problems and their solutions. We describe the final design, and show the new radiation tolerance test results.

II. Configuration Loss and its Solution

Tests have shown that though the FPGA tolerates the required level of total ionisation dose (TID), single event upsets (SEUs) caused by neutron or proton irradiation have a frequency higher than acceptable. These SEUs may produce data errors during operation, or if they happen in the device configuration SRAM cells, they may provoke corruption (or even loss) of the device configuration. The later is very critical, because it causes an immediate functional interrupt on the given device.

According to the tests, we have calculated the MTBF value and found that we would face 1 loss of configuration every hour in the DAQ system containing 400 DDL SIU cards. We also tested FPGAs of about the same size and complexity from Xilinx, but found very similar results as they are also based on SRAM configuration cell technology. See *Table 1* for the measurement results.

Table 1: Measurement results on configuration loss in Altera APEX-E and Xilinx VIRTEX II SRAM-based FPGAs

SEU cross sections /configuration cell	
$\sigma_{config\ cell}$ of 5-14 MeV neutrons	$(0.17 - 0.71) \cdot 10^{-13}$ cm^2 /logic cell
$\sigma_{config\ cell}$ of 48-50 MeV protons	$(5.5 - 10.7) \cdot 10^{-13}$ cm^2 /logic cell
$\sigma_{config\ cell}$ of 94-100 MeV protons	$(5.5 - 10.2) \cdot 10^{-13}$ cm^2 /logic cell
$\sigma_{config\ cell}$ of 171-180 MeV protons	$(4.5 – 9.0) \cdot 10^{-13}$ cm^2 /logic cell
^{60}Co γ irradiation (dose rate: 40 Gy/hour)	no damage up to 100 Gy
Calculated number of configuration errors	
# of config. loss in 10 years in 1 SIU card	20 – 50 (neutrons) 9 – 20 (protons)
# of config. loss per hour in 400 SIUs	~ 1 not acceptable

Since it was not acceptable for the DAQ system, a new, radiation tolerant DDL SIU had to be designed. We considered three possible ways to solve the problem.

The first option was to continue using Altera or Xilinx SRAM-based FPGAs and work out special mitigation techniques to recover from configuration losses. However, none of the discussed solutions seemed to be simple, all require additional logic circuits on the board (that are also target of radiation tolerance problems), and even with these costly (in terms of design and test work) additions we can not entirely eliminate the problem.

The second option was to use a custom, radiation hard ASIC. Although, this option is technically the most reliable, because the number of links in ALICE is small, we could not afford this solution (high NRE cost). Finally, the last option was the use of another kind of FPGAs that is based on a different silicon technology. In those FPGAs where the configuration is stored in flash memory cells, the configuration is intrinsically much more protected against irradiation. A detailed discussion of the options we considered can be found in the first part of [6].

Finally, we chose the flash-memory based ProASIC device family of Actel. These programmable logic devices combine the power of the FPGAs and the resistance against configuration loss seen in other type of FPGAs.

The block diagram of the re-designed SIU card is shown in *Figure 1*.

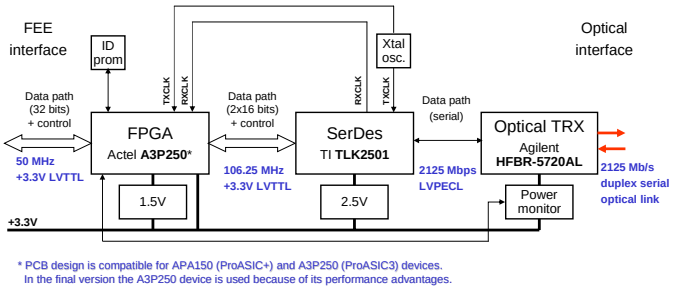

Figure 1: Block diagram of the final SIU card

The physical level of the data transmission is the same as before, the logic part has been re-built around an Actel ProsASIC+ or ProASIC3 device. See [6] for details.

After choosing the new FPGA device we had to verify its expected resistance with measurements. We found that neither a ProASIC+ evolution board nor a new SIU prototype board built with this device (see *Figure 1*) showed any configuration loss in proton and neutron irradiations. See *Table 2* for the measurement results.

Table 2: Measurement results on configuration loss in Actel ProASIC flash memory based FPGAs

SEU cross sections /configuration cell	
$\sigma_{config\ cell}$ of 5-14 MeV neutrons	no error
$\sigma_{config\ cell}$ of 171-180 MeV protons	no error
^{60}Co γ irradiation (dose rate: 40 Gy/hour)	no damage up to 100 Gy
Calculated number of configuration errors	
# of config. loss in 10 years in 1 SIU card	no error
# of config. loss per hour in 400 SIUs	0

III. Data Corruption Measurements

The other consequence of SEUs in the FPGAs is that upsets may change the status (content) of registers (logic cells) and/or the embedded user memory cells during operation. Although these events may not cause a functional interrupt of the device (it does not stop working), they result in bit errors in the data transmission. From the DAQ point of view a certain rate of data bit errors are acceptable if they are detected by the link protocol. From the beginning (i.e. the first prototype SIU) we measured not only the configuration loss of the FPGAs but the data corruption during operation as well. We developed several special test firmware to be able to measure data errors generated in the *register cells* (logic cells) and in the embedded *user memories* (e.g. FIFOs) separately. The method of these measurements is described in [5]. The results are summarized in *Table 3*.

It can be seen that the cross sections for errors generated by the irradiation are in the same magnitude for register cells and for memory cells. However, there are much more memory cells than register cells in the SIU design. It results that the vast majority of the single bit errors caused by the irradiation are generated in the memory cells, namely in the two FIFOs used in the design (one on the transmitter and on the receiver side). The goal was to achieve that these data errors are all detected. We had to re-design the SIU logic to fulfil this new requirement. This needed careful firmware development work but, fortunately, there was no need for change in the hardware.

Table 3: Data corruption measurements of SIUs with different FPGAs

	ALTERA APEX-E (0.18 mm CMOS) SRAM-based		**ACTEL APA150** (0.25 mm CMOS) Flash-based		**ACTEL A3P250** (0.13 mm CMOS) Flash-based	
	$\sigma_{register\ cell}$ [10^{-14} cm^2 /logic cell]	$\sigma_{memory\ cell}$ [10-14 cm2/bit]	$\sigma_{register\ cell}$ [10^{-14} cm^2 /logic cell]	$\sigma_{memory\ cell}$ [10-14 cm2/bit]	$\sigma_{register\ cell}$ [10^{-14} cm^2 /logic cell]	$\sigma_{memory\ cell}$ [10-14 cm2/bit]
5-14 MeV neutrons	0.166 - 0.706	0.29 – 0.51	No error	0.61	0.269	3.02
171-180 MeV protons	4.90 – 8.20	3.08 – 4.24	0.607	5.43	0.267	11.5
# of errors in 10 years in 1 SIU card	20 – 50 (n) 9 – 20 (p)	44 – 55 (n) 9 – 18 (p)	No error (n) 0.21 (p)	59 (n) 8 (p)	4.36 (n) 0.09 (p)	206 (n) 16.94 (p)
# of errors per hour in 400 SIU cards	0.91 (n) 0.22 (p) Config loss! Not acceptable	0.94 (n) 0.27 (p) Not acceptable if not detected	0 (n) 0.003 (p) Acceptable	0.84 (n) 0.115 (p) Not acceptable if not detected	0.063 (n) 0.00014 (p) Acceptable	2.94 (n) 0.24 (p) Not acceptable if not detected

IV. The Final SIU Design with Parity Check

There are several possible mitigation techniques, which can be used to avoid and/or detect the errors caused by SEUs.

One of the widely adopted methods is the so-called triple module redundancy (TRM). This solution, however, requires many extra logic resources, and therefore a larger FPGA device. The increased number of device resources (logic and memory cells) would also increase the chance of being affected by the high-energy particles.

In order to detect the bit errors that may occur in the FPGA's memory cells, one can use error detection schemes based on cyclic redundancy codes (CRC) or parity bits. The CRC checksum is a powerful protection mechanism used in serial transmission protocols. However, the behaviour of the error caused by SEUs in the embedded memory cells (isolated single bit errors) does not justify the complexity required by the CRC calculation. Therefore, a simple yet efficient error detection based on *parity check* logic has been implemented in the FPGA device.

The new and final functional block diagram of the SIU logic can be seen in *Figure 2*.

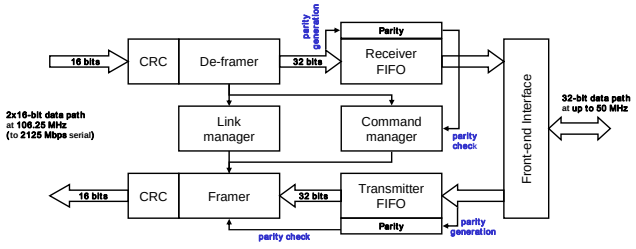

Figure 2: Block diagram of the FPGA design on the final SIU

V. Final Measurement Results

In order to test and verify this redesigned, radiation tolerant SIU we developed and carried out several series of radiation tolerance tests and measurements. With these tests we measured the bit error rates both in the registers and in the embedded memory cells, and tested their detection in radiation environment. Data corruption due to SEUs is detected by the parity check logic. If detected, the firmware attaches an error bit to the control information sent together with the data. During the measurements, the transmitted data was consisted of different known data patterns (alternating patterns, flying 0s or 1s, incremental data). We designed two different tests.

During the so called *loop-back tests* the SIU received data from the DDL link and the special firmware in its FPGA sent these data back trough the link. In this case the data went through the FPGA's memory cells twice. In the other measurement method the SIU, loaded with the final firmware, was plugged into a radiation tolerant *data generator*, which produced data according to the DDL protocol. In this case the data flow is only uni-directional. In both cases the measurement software compared the received data against the expected one and checked whether the error bit had been set in case of erroneous data. If it was set we considered the error to be *detected*. We carried out the measurements up to the neutron fluence of 10^{11} n/cm^2, which corresponds to the radiation level expected during 2.5 years of SIU operation.

During these measurements we found the SIU-imposed error bits attached to all erroneous events, that is, the data corruptions caused by the irradiation were fully detected by the parity check logic. The results of the measurements are summarized in *Table 4*.

Table 4: Measurement results on neutron, proton and γ irradiation of the final SIU card

	SIU card (v. 2.3) w/ ACTEL A3P250 FPGA
$\sigma_{\text{data error}}$ for 5-14 MeV neutrons	(0.4 - 1.0) * 10^{-14} cm^2/bit
$\sigma_{\text{data error}}$ for 171-180 MeV protons	(6 - 7.2) * 10^{-14} cm^2/bit
Co^{60} gamma irradiation	No effect up to 100 Gy (10 krad)
# of data errors in 10 years in 1 SIU	26 - 70 (n) 4 - 10 (p)
# of data errors per hour in 400 SIUs	0.4 - 1 (n) 0.06 - 0.15 (p)
Percentage of detected errors relative to all errors	**~ 100 %**

VI. Project Status

The ALICE Detector Data Link has been developed in collaboration of CERN and KFKI Research Institute for Particle and Nuclear Physics, Budapest. One component of the project was to test and evaluate a radiation tolerant version of the SIU card. With the measurements described in this paper we completed the evaluation of the radiation tolerant Source Interface Unit.

The detector data travelling through the DDL link is protected now in threefold way:

- 8 bit / 10 bit data coding is part of the DDL low level protocol,
- 16 bit CRC words accompany the data on its way between the Source and Destination Interface Units,
- and now, parity bits protect the data in both directions (to and from the detector) inside the SIU subject to irradiation.

The production of the DDL SIU cards has been started this year. More than the half of the 550 cards needed by the ALICE experiment has already been produced and their installation on the sub-detectors has been started. The production will be completed in the 4th quarter of 2006.

VII. Acknowledgment

This work was carried out within the framework of the Hungarian National Development Plan supported by the European Community and the Hungarian State. Contact number: GVOP-3.1.1-AKF-0423.

All proton irradiation were done at the cyclotron facility of TSL, (Uppsala, Sweden). All neutron irradiation were done at the cyclotron facility of ATOMKI (Debrecen, Hungary), as well as the total ionising dose measurements using their ^{60}Co gamma source.

The authors thank these institutions for their extensive help and support in carrying out of these measurements.

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Ideas on DC-DC Converters for Delivery of Low Voltage and High Currents for the SLHC / ILC Detector Electronics in Magnetic field and Radiation environments.

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Abstract

For more efficient power transport to the electronics embedded inside large colliding beam detectors, we explore the feasibility of supplying 48 Volts DC and using local DC-DC conversion to 2 V (or lower, depending upon on the lithography of the embedded electronics) using switch mode regulators located very close to the front end electronics. These devices will be exposed to high radiation and high magnetic fields, 10 – 100 Mrads and 2 - 4 Tesla at the SLHC, and 20 Krads and 6 Tesla at the ILC.

I. INTRODUCTION

We have been involved with the ATLAS and CMS detector construction at CERN. Yale designed and constructed the low voltage regulator cards for the ECAL of CMS (see fig. 1). The 3,100 low voltage regulator cards that we constructed each deliver 16 amps at 2.5 volts to the front-end CMOS chips. The total current drawn by the cards is 50 Kamps. The power supplies are located 30 meters away on the magnet yoke and supply 6.3 volts. After a loss of 1 Volt in each leg of the power cable, the regulator card input is 4.3 volts. The required voltage across the regulators (LHC4913 made by S.T. Microelectronics) is 1.8 volts for the minimum dropout voltage needed after 10 years of exposure to the radiation. These are linear regulators and are insensitive to the high magnetic field. They have low power efficiency but also have low output noise and low EMI. Figure 1 is a layout of the DC powering system to emphasize the low efficiency of delivering power to the detector (in this case, only 40%, 2.5/6.3).

For the International Linear Collider (ILC), the Silicon Detector (SiD) will require 50 Kamps. The CALICE detector at the ILC requires 300 Kamps. The feature size of the front end silicon is migrating towards 65 nanometers, and in the future will operate with higher currents at less than 1 volt.

To us, the only feasible alternative power delivery system requires DC-DC switching converters. These can have very high power efficiencies of up to 95%. If we could supply 48 Volts and the local regulators convert it to 2 volts for the chips, the result would be a x24 reduction in the supply current and at least a x24 reduction in conductor (copper or Aluminum) cross section. Smaller conductor cross section will result in less dead material in the detector, less multiple scattering and possibly an increase in the detector coverage. The power dissipation in the power delivery system (which also must be removed by the cooling system) will be lower due to the high conversion efficiency of the DC-DC switching regulators and the lower currents in the supply cables. The main challenges are the radiation and the magnetic field. We must have radiation hardening of the semiconductors in the DC-DC regulator, the controller ASIC and the MOSFET switches. There are many groups who are experts in this field and we intend to utilize their expertise. The other challenge is the operation in the high magnetic field that we shall address in this paper. The inductors usually used in DC-DC converters are made with a ferrite core, and are not suitable for high magnetic fields. In 2005, we became aware of the work of Intel Corporation in integrating air core inductors on their 90 nanometer CPU chips [1-3]. By using higher switching frequency, air core coils can replace the ferrite coils usually used in switching DC – DC converters. Their exploratory work tested operation at up to 480 MHz. There was an attempt made at NIKEF to use air core coils for the Atlas detector but it was not successful [4].

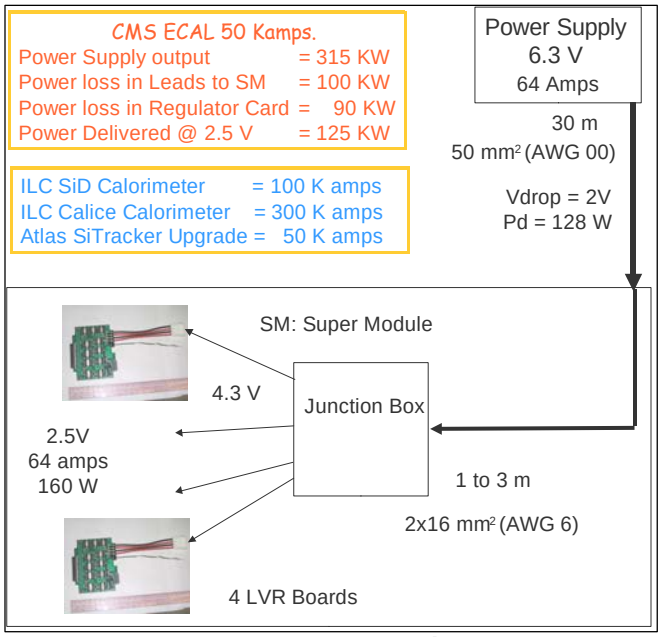

Figure 1: ECAL Power Distribution

II. Overview of Existing Technologies

Let us look at some DC-DC converter technologies currently in use (Charge pump, switch mode and resonant switch converters):

A. Charge pump

A charge pump charges several capacitors in series to the input supply voltage and then connects them in parallel across the load. The input to output voltage ratio is given by the number of capacitors. It is usually limited to small (< 1 ampere) currents but can provide negative voltages.

B. Switch Mode: Synchronous Rectification.

A switched-mode power supply (SMPS), is an electronic power supply unit that incorporates a switching regulator (a control circuit that switches the current rapidly on and off) to regulate the output voltage. This is the most common technique being used for single chip implementations with either internal or external MOSFET switches. PWM (pulse width modulation) is used to translate high input voltage to low output voltage by pumping current into an inductor with shorter ON times and longer OFF times.

Switching regulators are used as replacements for linear regulators when higher efficiency, smaller size or lighter weight is required. They were, however, more complicated and more expensive, and their switching currents can cause EMI and noise problems if not carefully designed. Power converters are becoming increasingly commonplace in the electrical industry. Product manufacturers and suppliers of electrical equipment are demanding ever-increasing performance (i.e., higher efficiencies, lower output voltages, higher currents, faster transient response) from their power supply systems. To meet these demands, switching power supply designers in the late l990s began adopting Synchronous Rectification (SR) using MOSFETs to achieve the rectification function previously performed by diodes. SR improves efficiency, thermal performance, power density, manufacturability, and reliability, and decreases the overall system cost of power supply systems.

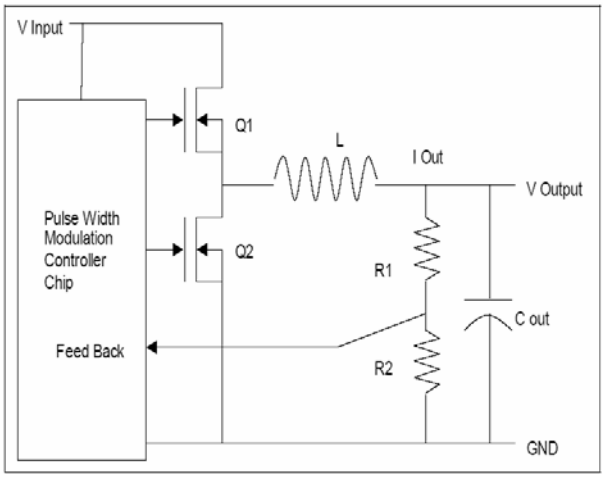

Figure 2: Synchronous Rectification

Referencing Figure 2, when Q1 is switched ON, current into the load increases and energy is stored in L. When Q1 is switched OFF, Q2 is switched ON providing a current path to allow energy stored in L to be transferred to the load. A simple power rectifier may be used in place of Q2 (as a *catch* or *flyback* diode) but the forward voltage drop of a Schottky power diode will cause an efficiency loss. When a MOSFET is used as a synchronous rectifier in this topology, the controller chip must carefully control the switching of Q1 and Q2 to prevent shoot-through – i.e. an overlap of the ON times of Q1 and Q2 that can momentarily short the input power.

In DC-DC Converters, the average DC output voltage must be controlled to be equal to a desired level though the input voltage and output current may fluctuate. Switch mode DC-DC converters utilize one or more switches and an inductor to transform DC from one level to another. Generally the controllers work at a fixed frequency to make it easier to filter the output ripple. In Figure 2., Q1 and Q2 are turned on in a sequence to connect the inductor input to the input voltage or to ground. The duty cycle is determined by the ratio of the Output / Input voltage. A feed back from the output adjusts the duty cycle to keep the output voltage at the specified level. Typically, DC current always flows through the inductor (continuous conduction mode)

When Q2 is replaced by a Schottky diode it is called a non-Synchronous Rectification. The diode keeps the current in the inductor flowing when the MOSFET is off. There is more power lost in the diode since the forward voltage is much larger than the voltage across the MOSFET when it is conducting.

C. Resonant Switch Converters

In certain switch-mode converter topologies [6], an *LC* resonant circuit can be used to shape the switch voltage and current to change the power factor seen by the switch. This allows zero-voltage and / or zero-current switching. In such resonant-switch converters, during one switching-frequency time period, there are resonant as well as non-resonant operating intervals. Circuits with inductors and capacitors are used at or near resonance for transforming power to high voltages or higher currents. Class-E RF amplifiers can convert DC to RF at very high efficiencies.[5] and then synchronous rectification for DC output. Therefore, these converters in the literature have also been termed quasi-resonant converters.

They can be sub-classified as follows:

(a) Zero-current-switching (ZCS) converters

(b) Zero-voltage-switching (ZVS) converters

Vicor Corporation [7] is the leader in making Quasi resonant high density DC-DC converter modules. This is shown in Figure 3. Their VTM /BCM power train has dual H bridges and extensive use of transformers to adjust the input to output voltage transformation. The input voltage range is 38-54 volts, and modules are available with output voltages from 0.8 to 54 V. The match box size hybrid module delivers 200 watts with current up to 100 amps. The efficiency is greater than 94%. Vicor has one ASIC controller chip, one power transformer T1, and gate driver transformer T2. The circuit Q is about 10 and they use proprietary techniques to achieve both ZCS and ZVS as shown in figure 4..

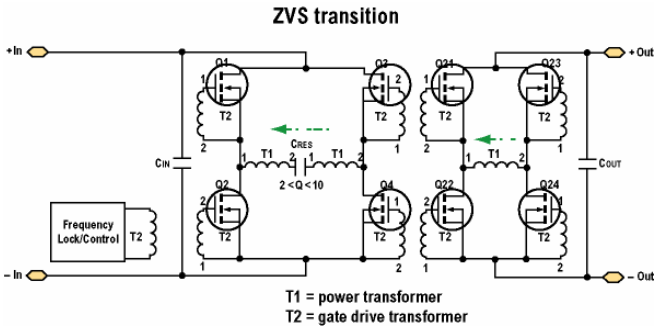

Figure 3: Vicor VTM circuit.

The Vicor VTM has no regulation circuitry in it. A 1% change in input appears at 1% change in the output voltage. This may be adequate for HEP applications if the 48 V power supply has remote sense capability and is well regulated. For other applications a pre regulator called PRM containing a buck boost regulator delivers 48 volts to the VTM from a 36-75 volt unregulated source.

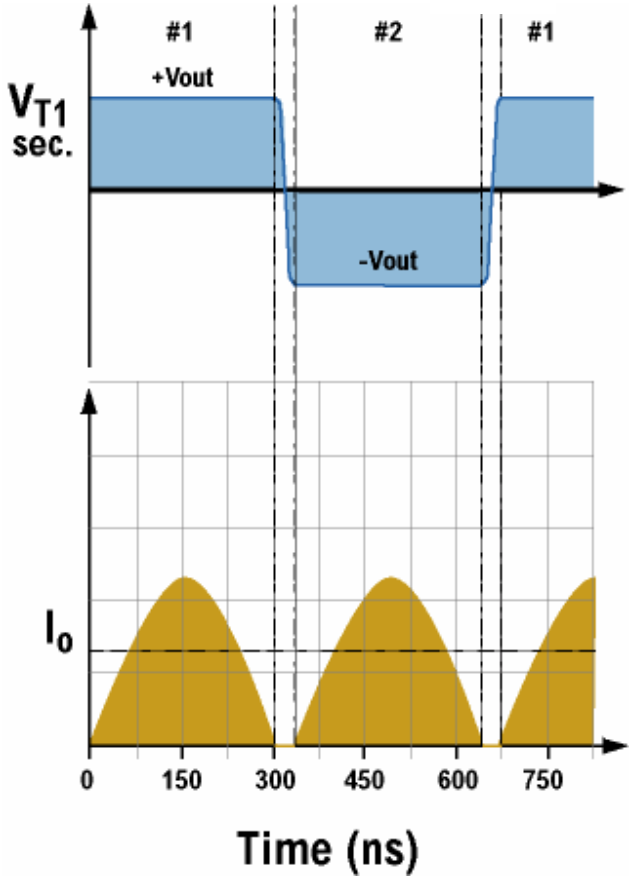

Figure 4: Vicor VTM circuit operation.

Our objective here is to focus on a relatively high supply voltage (48 V) with output currents in the range of 2 – 50 amps. This work is limited to using only air core coils.

III. Powering of Silicon Trackers

We look at the problem of powering the Silicon trackers in SLHC and ILC detectors. Figure 5 shows a prototype "stave" mounted with six 4 x 6 cm^2 silicon sensors. Each sensor is read out by a multi-chip module containing four custom readout chips. All control signals and power to the modules are routed via Kapton flex circuits. Such modules may draw as much as 4 amps at 1.3 volts. Staves may contain 10-40 modules depending upon the required acceptance. We'll consider a 10 module stave that requires 40 amps of current.

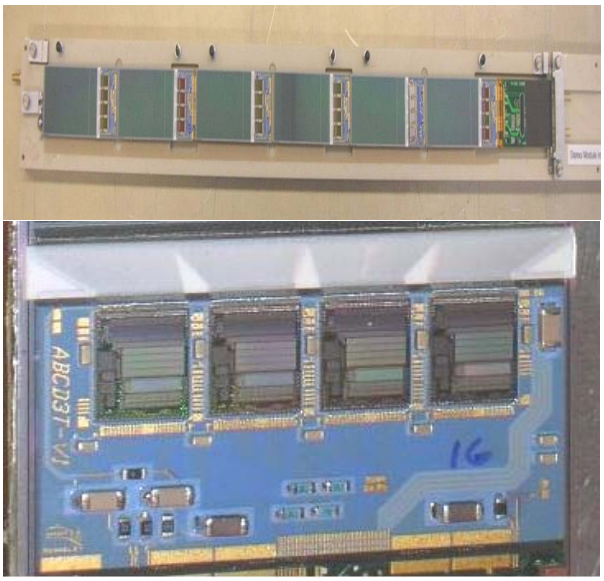

Figure 5: Stave with 6 sensors and the hybrid card.

A. Two power schemes with DC-DC converters are possible;

Four Amp DC-DC converters are mounted on each module. 48 volts are delivered to each module in parallel via Kapton traces.

Forty Amp converters are mounted at or near the end of each stave. Here the Kapton power and ground traces carry increasingly more current towards the supply end of the stave

For this exercise we assume that the SLHC and ILC requirements are somewhat similar but there are some differences.

Four Amp converter units are located near the front end and may be exposed to > 30 Mrads of radiation in the SLHC, but only 20 Krads at the ILC. The units should be made of low density materials. It may be possible to integrate the FETs on the ASIC.

Forty Amp units can be located in a off-detector service area with lower radiation exposure for both the SLHC and ILC.

SLHC needs the power to be on continuously and that adequate cooling be provided. In the ILC, the power can be switched on for the brief time when the beams are colliding. Here the duty cycle is 0.5% and the cooling solutions are simpler than for the SLHC. We ignore the Lorentz force problem in switching current in the ILC. It may be necessary to provide slow current cycling.

SLHC detectors use lower magnetic fields while the ILC detector is being designed for 6 Tesla. The converters have to be designed to run in a field from 1 to 6 Tesla.

IV. Power Converter Design Issues

The critical components are the ASIC controller chip, MOSFETs and the air coils. These are some of the issues that need to be explored:

MOSFET radiation hardness for 48 Volt silicon processes may be difficult (or impossible) for SLHC but achievable for the ILC.

It may be possible to use air core transformers to reduce the voltages to be handled by the ASIC and the FETs. There is a tradeoff between voltage and current handled by the FETs for the same output power level. The higher switching frequency requires smaller inductor values that are more easily satisfied with air cores. The noise at the output is tens of millivolts and substantially more at the input supply rail.

The Vicor units are in a different class due to the use of Quasi-resonance and sine waves. The output noise and ripple are very low. A test done at BNL indicated no obvious degradation of low noise preamplifiers

V. Test Results with an Air Core Inductor

We are now concentrating on using air core inductors with existing DC-DC converter chips. Most of the available controllers operate at less then 500 KHz, but there are a few operating at several MHz with a smaller inductor. We tested the following controller chips using company supplied evaluation boards, replacing the ferrite inductor with an air core inductor.

Texas Instruments TI 5430: Operating frequency is 500 KHz. Input range is 5.5 to 36V. Minimum output is 1.22 V. The evaluation board is set for 5 V. Output is rated at 3 amps. We tested by switching 2 amp loads.

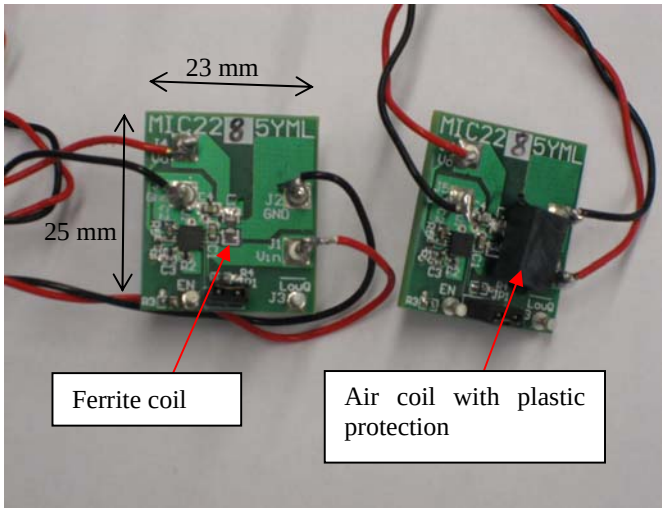

Figure 6: Photograph of Micrel with Ferrite (left) and Air Coil (right).

Micrel MIC2285: Operating frequency is 8 MHz using a 0.47 µH inductor. Input range is 2.7 – 5.5 V@ 0.5 amps output load.

Linear Technology LTC3415: Operating frequency is 1.5 MHz. using a 0.2 µH inductor. Input range 2.25 to 5.5V. Output spans 1.8 – 3.5V @ 7 amps. The evaluation board is preset for 1.8 V, and we tested by switching 6 amp loads.

The results are shown in table 1. The low inductance air coils are made by Coilcraft Corp. with a maximum inductance of 0.538 µH. At Yale, we wound 6.25 mm diameter solenoid with AWG22 magnet wire; a 40 turn coil has inductance of 5.9 µH, while 30 turns give 2.8 µH.

The load was a Datel active load with a maximum rating of 20 amps. The duty cycle was about 20% and we did not need to provide any cooling.

There were no special filters used except what was on the evaluation boards. The ripple and noise can be much reduced by using standard filters for the low noise amplifiers.

There were 2 Micrel evaluation boards, the air coil was mounted on one board. The TI board had a large ferrite core, so we decided to put the air coil in parallel. The resultant inductance is mainly from an air coil.

The Vicor board results is shown for comparison with the LVRB load as shown in figure 1. The output and input and output ripple signals are shown in figure 8. The 48 Volt power supply did not power output for more than a 24 amp load.

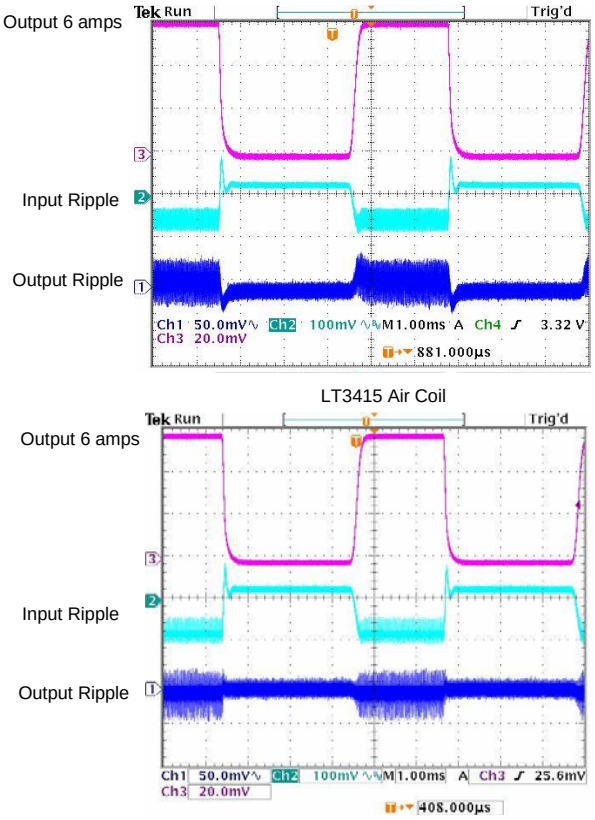

Figure 7: Comparison of the LT3415 DC-DC converter chip with the ferrite coil versus the air coil.

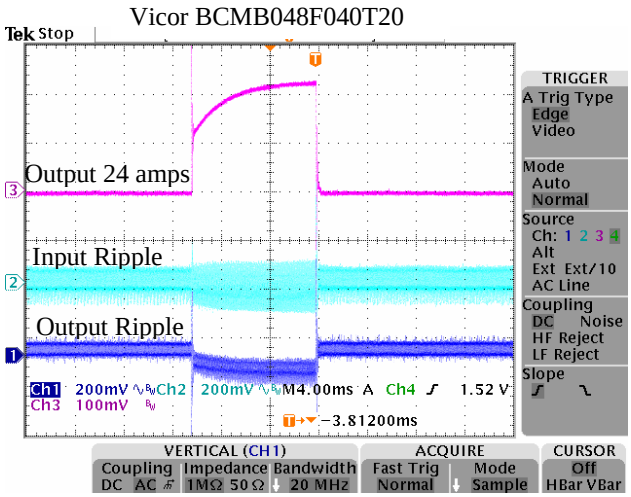

Figure 8: Results for the Vicor multi chip hybrid with ferrite based transformers.

VI. Conclusions

In conclusion, there is no difference between the ferrite and air coils if the inductance is the same. This can be seen in figure 7 with LT3415. The noise is increased if a lower inductor value is substituted.

Vicor match box size module is a good candidate for delivering 2 Volts at up to 100 amps. It is a multi chip hybrid with ferrite based transformers. The ASIC in it now can withstand 20 krads. It is feasible to design air core transformers if the operating frequency is increased by a factor of 10 to 15 MHz. Needless to say, there are many challenging problems to overcome.

We are very encouraged by the tests with the air coils using standard switch mode controller chips. For better operations (noise, efficiency, EMI shielding etc.) in the magnetic field the switching frequency should be an order of magnitude higher. We would like to encourage other groups to work with us on pursuing this development.

VII. Acknowledgements

We thank the following companies for supplying us their evaluations boards and samples at no charge, Vicor Corporation, Micrel Inc and Linear Technology Corporation.

VIII. References

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Table 1. Test Results

Devices Tested	*Specifications*					*Coil Inductance*			*Ripple with Ferrite Coil*		*Ripple with Air Coil*	
Manufacturer	**Device #**	**Input Range V**	**I_{out} amps**	**Freq. MHz**	**V_{out}**	**Ferrite Coil µH**	**Air Coil µH**	**Pulsed Load Amps**	**In mV**	**Out mV**	**In mV**	**Out mV**
Linear Technology	**LTC3415**	2.25 – 5.5	7	1.5	1.8	0.2	0.169	6	60	40	60	40
Micrel	**MIC2285**	2.7 – 5.5	0.5	8	1.8	0.47	0.538	0.5	10	70	25	80
Texas Instruments	**TPS5430**	5.5 – 36	3	0.5	5	18	5.9	2	80	180	120	200
							2.8	2			250	240
						air coil in parallel with ferrite coil						
Vicor	**B048 F040T20**	38-55	58		4			24	220	100		

Inductance	*Coil Specifications*
0.169 µH	Coilcraft Part Number 132-20SM
0.538 µH	Coilcraft Part Number 132-12SM
5.9 µH	Yale 6.25 mm diameter 40 turn Solenoid
2.8 µH	Yale 6.25 mm diameter 40 turn Solenoid

Functional and linearity test system for the LHC beam loss monitoring data acquisition card

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Abstract

In the frame of the design and development of the beam loss monitoring (*BLM*) system for the Large Hadron Collider (*LHC*) a flexible test system has been developed to qualify and verify during design and production the *BLM LHC* data acquisition card [1]. It permits to test completely the functionalities of the board as well as realizing analog input signal generation to the acquisition card. The system utilize two optical receivers, a Field Programmable Gate Array (*FPGA*), eights flexible current sources and a Universal Serial Bus (*USB*) to link it to a *PC* where a software written in LabWindows/CVI© (National Instruments) runs. It includes an important part of the measurement processing developed for the *BLM* [2] [3] in the future *LHC* accelerator. It is called Beam Loss Electronic Current to Frequency Tester (*BLECFT*).

I. HARDWARE

The *BLM LHC* data acquisition card (*BLECF*) also called tunnel card is used to measure the current of the ionization chambers, to digitalize and to send it to the surface through optical fibers. To design, operate and test the tunnel card the *BLECFT* card has been designed. The analog part must be able to handle 8 orders of current settings from 10pA to 1mA and to be able to decode the information sent by optical fiber. The final system includes the card and the power supplies in an easy transportable housing. It is powered by the 230V 50Hz or by a *PC* through the *USB* connections (for the portable version without power supplies).

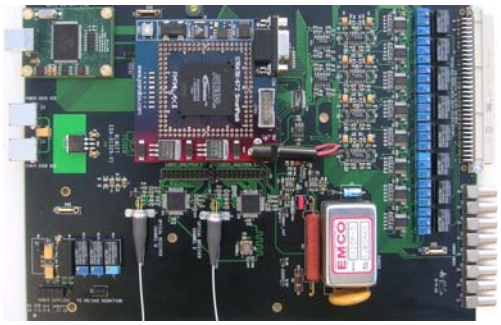

Figure 1: The *BLECFT* card.

The second use of the *BLECFT* is to emulate the processing of the future *LHC* system. For this reason, the choice of a compatible *FPGA* to the BLM one was taken to simplify the integration of the hardware description processing. Because this feature was implemented in a small integrated system, the *BLECFT* was often used in proton irradiation campaigns for the design validation of the tunnel card.

A. FPGA Description

The programmable logic has a central role on the board. It connects the *USB* module with the rest of the components like the *DAC*, relays and analog switches as well as processes and transmits the measurements and information received from the tunnel card.

The used *FPGA* type on the board belongs to the same family (Altera Stratix©) as the one of the *LHC BLM* system but with less logic elements. With this feature, it is possible to reuse code from the *BLMTC* (Running Maxima). The number of channels is reduced from 16 to 8, except this modification the code is identical (to the *BLMTC*). It permits to get similar data as the final *LHC* processing to realize test in real situations.

To implement the different modes, the description take advantage of the parallel processing of programmable logic to allow real time analysis of packets (Running Maxima mode) even during visualization in another mode (Frame Mode). The user can choose the information downloaded into the *PC* by selecting the correct input of the multiplexer corresponding to the mode of operation selected.

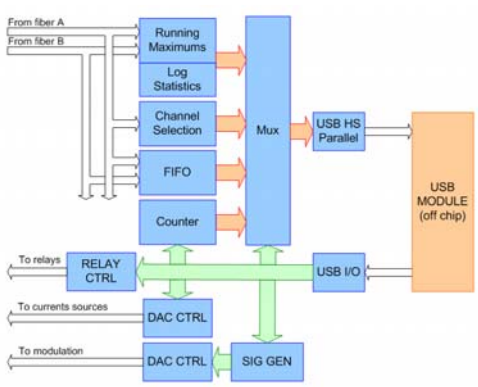

Figure 2: The *FPGA* description blocs.

There are two data channels between the hardware and the *PC*. The control of the *BLECFT* is done through a low speed connexion between the PC-*USB* and the *FPGA*. The I/O are directly controlled by the software to create an 8bits parallel bus where transit addresses of registers (8 bits) and data (16 bits). These data are then parallelized and distributed to all registers. A simple protocol has been specified using these addresses and data to modify the registers values. To get the measurements and status information quickly, the *FPGA* uses a high speed connection with 16 bits parallel bus to the *USB* chip.

The *BLECFT FPGA* includes also logic to control the current sources through *DAC* converters, relays and analog

switches. To reduce the use of output pins on the *FPGA*, the control and data signals are multiplexed. There are two *DACs*, which share their lines. To simplify the logic needed for the control, the update is done continuously between the *FPGA* internal registers and the *DAC*. When the user changes one voltage, the software actually writes in the *FPGA* register the new value. When the refresh process starts, the new setup value will be taken and the *DAC* output voltage updated. With this implementation, the software doesn't have to be specialized for each functionality of the card, it just writes to registers and the *FPGA* does the rest.

There are at least 3 clock domains which have to cohabite together. The speed rate of the data from the tunnel card is 40 MHz, which is synchronised with its own quartz. The second domain is the global clock of the *FPGA* at 40 MHz. The last one is the link to the *USB* module, which runs at 48/33 MHz, because the master of this link is the *USB* mezzanine module. The used bus speed used is 33 MHz to avoid errors due to latency. The clock has to travel from the *USB* to the *FPGA* before the data are updated for the next clock cycle. Even for small connection length, we experienced wrong behaviour using the 48 MHz transmission. In order to separate correctly these clock domains, *FIFOs* are wildly used.

B. Optical link

The optical link consists of two one way fibres connecting the tunnel card to the *BLECFT*. Data packets of twenty words (16 bits) are sent through this 800Mbps single fibre mode link every 40µs. The encoding is 8b/10b, which is compatible with the transceiver *TLK1501* from Texas-instruments. The parallel link between this chip and the *FPGA* is a parallel 16 bits bus working at 40MHz. The used components are identical to the one of the BLM receiver card of the *LHC* system.

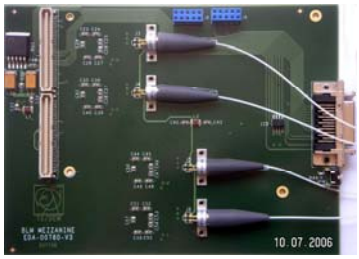

Figure 3: The *LHC BLM* Mezzanine receiver card.

The photodiodes and the transceiver have been directly integrated on the board next to the *FPGA* on the *BLECFT* card. The packets contain card identification number, packet identification number, status of the card, measurements from the *ADC* and counter results of the current to frequency circuit. These data are then processed or send directly to the *PC*.

C. USB module

The use of a *USB* module has been launched by the thesis work of R. Leitner [4] prior to the building of the *BLECFT*. The use of a *USB* transceiver and hardware core inside the *FPGA* has been studied but the effort for adapting a driver under Windows© was too high for the purpose of the project.

Another option for the link was given by the use a dedicated chip with embedded handling of the *USB* protocol. The chips from *FTDI* are components specially made to handle the entire link and provide different interfaces (serial or 8 bits parallel) to the user. The *PC* side is handled by a library provided by the company and permits to access the chip by calling some simple functions in this specific library.

The last product tested is a module with the famous Cypress chip FX2©, which is an USB2 controller and a microcontroller on one chip with high throughput capabilities via a direct data channel path and FIFO, bypassing the processor. The module developed by a small company is provided with a custom library to be used with the module. The *USB* protocol is hidden and the user can focus on the functionality of the system.

The choice between these modules has been determined by the transfer speed they can reach (use of *USB* 2.0 and 16 bits parallel bus) and by the availability of a complete library of functions. For the *BLECFT*, the last module presented has been used.

D. Current sources

The current source provides currents from 10pA to 1mA on eight channels to feed the inputs of the tunnel card. The central component of this circuit is a Digital to Analog Converter (*DAC*) providing voltages for a resistor network. If the resistor value is high enough compared to the input resistance of the board (worst case: 1MΩ over 2.7kΩ, 0.27%), the error can be neglegted. To select the current range, an analog multiplexer permits to choose between the resistor values from 1MΩ to 10GΩ. The variation of the components and systematic errors can be compensated by the calibration (voltage control at the output of the *DAC*) stored into an independent file on the *PC*.

To provide the high currents accurately enough (10µA to 1mA), its generation had to be designed separately from the rest with a current sense feedback. The voltage across the control resistors and the second analog switch (to select the range) is measured by a differential circuit, which regulates the voltage on the control resistor in order to reach the needed current (the voltage on the *DAC*).

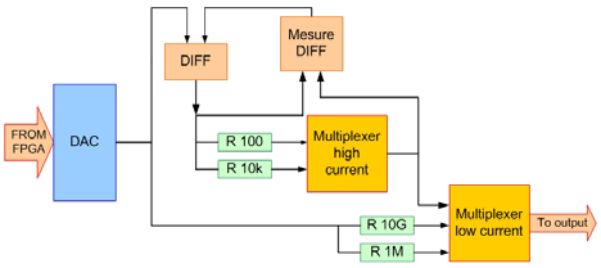

Figure 4: Current source schematic.

E. High voltage module

The *BLECFT* has also the capacity to generate a high voltage to feed one or more ionisation chambers to simulate test procedures. Because of the working voltage (1500V) of these ionisation chambers, there is a need of a specific module capable of generating such high voltage.

One of the tests implemented in the *LHC* system is the modulation of a small portion of the high voltage power supply (*HVPS*) and to check in the Running Maxima if a variation is seen. The hardware and software of the *BLECFT* is available to realize this function. The *FPGA* generate a harmonic signal with a memory based processing, which is added to the base control voltage of the *HVPS* with an anaolg addition. This voltage is connected to the high voltage power supply module and is multiplied with a factor of 1000. Due to the capacity of the signal electrodes of the ionisation chamber, a small current is induced and measured with the tunnel card. The *BLECFT* process these measurements (Running Maxima) and returns the results to the *PC*. This test will be implemented in the *LHC* system to check the connection of the whole acquisition chain.

II. Software

The Windows© based application has been developed to provide to the user a graphical environment to configure the hardware and read/store/show measurements in a user friendly way.

The software has been written with a graphical environment called LabWindows/CVI© from National Instruments, which provides all graphical facilities and required "C" as programming language. It helps the programmer to focus on functionalities rather than on details.

It includes analysis of raw data coming from the tunnel card as well as result visualisation of the real-time processing done in the *FPGA* similar to the future *LHC* one [3].

A. Event driven coding

The software is event driven and is separated on different files and functions to clarify the code. When the user want to start to read information from the tunnel card, a click on a specific button starts an interrupt with a definite period. Each time the interrupt is called, a function is started, which reads the data from the *USB*, process it in the appropriate way depending on the mode of operation (see II.C) and display it for the user. This style of programming permits to save computer processing power. The program is more often in wait state than in processing state. It is also very easy to add functionalities to the core code without changing timings and initial code.

B. Structure

There are tree principal windows composing the software. The first one is dedicated to show and control the way the information from the hardware is handled. The second one contains the options to configure this hardware. The last one is the test window which includes all control and visualisation objects to do the functional test of the tunnel card.

C. Modes of operation

The software has been segmented in 3 modes. 1) The Frame mode catches the raw information directly from the tunnel card, analyzes and displays it as the data are arriving. 2) The running maximum works exactly as the future *LHC* system [3]. The data are processed inside the *FPGA* and the software takes the results with a user defined period for the display and storage.

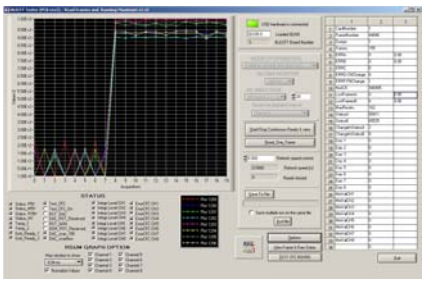

Figure 5: The Running maxima mode of the software.

The last mode is the oscilloscope mode which permit to see all the data (40us period) of a given channel for a defined window. In mode 1 & 2, it is possible to visualize the status of the tested card, save the data shown on the screen and control the parameters like the applied test current or the applied high voltage.

D. Functional test and calibration

The test procedures have been implemented as an upper layer of the existing functions of processing, visualisation and analysis of data. When a test is launched, the appropriate mode is set and the readout starts. The test function configures the parameter to be tested and analyses the resulting behaviour. The result of each step inside a test is written in a log file and the number of errors and the severity is totalised in order to label each card for the repair management.

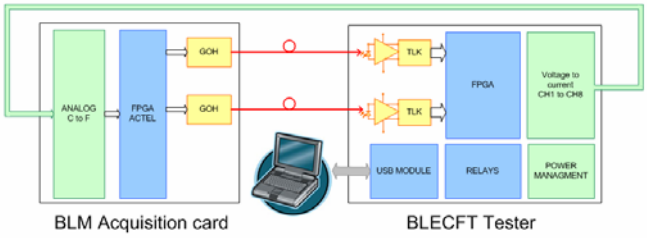

Figure 6: Test setup of the tunnel card.

There are numerous parameters to check during the functional test; the optical link connection status, the board status, the test mode response and the linearity of the inputs.

1) The optical link connection

Prior to further test, the optical link must be working as defined. In addition to the connected/not connected test, the error detection is checked (*CRC*) and reported.

2) The tunnel card status and auto-test functionalities

There are 32 statuses to be checked. There are 16 for the state of the inputs; if one channel is not functioning like defined (the voltage on the integrator is saturated at the maximum) a status is showing this. If this status stays longer than 100 seconds another status is set. To realize this test, a feature in the current sources permits to invert the current sent and then saturate the input stage.

The power supplies are also monitored on the tunnel card. To test this, the *BLECFT* includes a command to lower the

power supplies feeding the tunnel card and then setting the status warning.

The rest of the statuses are related to the auto-test functions. To enter in these test modes and be able to verify their correct behaviour, the input of the high voltage survey has to be controlled by the *BLECFT* with a *DAC*. For each auto-test and command (4 in total) the voltage is set by the test function and the result is controlled.

3) Calibration of the tunnel card inputs

The system is used to calibrate accurately the gain and input offset current of the tunnel card. The operator has to adjust the 16 potentiometers on the card. The software is showing the actual values and informs when the correct position is reached while the operator is manipulating the card.

4) Linearity of the measurements

One of the most important verification is the linearity check. For this purpose the current sources have been carefully built and calibrated. The test is driven by a text file, which specifies every measurement. The software follows each step and compares the measurements with predefined thresholds to determine if the input is usable or not and saves the result into a file.

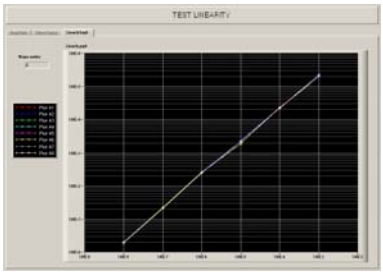

Figure 7: Window of the linearity test result.

Summary

The beam loss monitoring system for the *LHC* uses a radiation tolerant acquisition card (*BLECF*) to measure the current of the ionization chambers. The data are transmitted to the surface to a *VME* board (*DAB*) using optical links. The data are processed in it and decisions are taken in case of dangerous losses. In order to visualize and test the *BLECF* in an efficient way, a single card with dedicated software has been developed with flexible and powerful features.

The card is able to check the linearity of the measurements from the *BLM* acquisition card. A complex current source has been developed to be able to feed the inputs with currents from 10pA to 1mA (8 orders) with a reasonable accuracy (better than the input tolerance). To check if the results are in the expected tolerances a sequence of current settings is launched with the software to scan the whole dynamic range. When the system operates in the similar mode as the future *LHC* system (Running Sums acquisition), it is possible to check different indicators like the number of wrong Cyclic Redundancy Check (*CRC*) of the optical link or the type of error appearing in the receptions of the packets. In order to check specific data during the development of the *BLECF*, visual displays have been implemented in the software to display the acquisitions versus time values of the current-to-frequency converter and the sampled value of the Analog to Digital Converter (*ADC*), which are entering in the calculation of the final current.

The optical receivers use photodiodes with automatic gain control and are interfaced with an 8b/10b transceiver. The *FPGA* holds the reception logic for the data, the processing of them (taken from the future *LHC BLM* system) and the logic for the link to the *PC* (including control and acquisition). The software is able to integrally control the card in its different mode of operation including a reading of the raw data, a high speed reading, visualization of the resulting processing of the *FPGA* calculation (running sums) and the functional and linearity tests. The program has been written in C and linked with a user friendly interface. The board can be powered over the *USB* of a laptop.



Figure 8: The *BLECFT* final box.

The system has been successfully used during the development phase at *CERN* and especially used for the *BLECF* during the validation of the *FPGA* description. Since the processing of the data is similar to the final system and very compact, the box has been successfully used as readout system during radiation tolerance campaigns for the *BLECF* at *PSI*. For the same reason, the system will also be used during installation and commissioning of the *LHC BLM*. Another use of this system is the investigations for the beam condition monitors of the *CMS* experiment using diamond detectors.

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Development and Setup of a Prototype System of Distributed Analysis for ATLAS Tier-2

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Abstract

The ATLAS experiment currently under construction at CERN's Large Hadron Collider (LHC) presents data processing requirements of an unprecedented scale. ATLAS will accrue tens of petabytes of data per year, distributed around the world: the collaboration comprises more than 1800 physicists from 150 institutions in 34 countries. The Distributed Analysis (DA) has the goal of enabling ATLAS physicists to perform analysis on distributed data using distributed computing resources. Both data and resources are widely distributed throughout the world at CERN and at ATLAS Tier-1 and Tier-2 centers. Since DA is of strategic importance there is a large development activity going on in this area: the ATLAS production system has being evolving to support the analysis jobs which will have a seamless access to all ATLAS resources, as well as another activities that aim to support user analysis by submitting directly to the separate grid infrastructures (Panda at OSG, direct submission to LCG and Nordugrid). The test of DA functionality will be addressed in the final Service Challenge 4 (SC4), in which the system will exposed to the expected large number of final analysis users.

The Spanish ATLAS Tier-2 facility formed by IFIC, IFAE and UAM groups, is participating in several aspects of the Distributed Analysis System. In support of the ATLAS DA activities the IFIC Tier-2 centre has developed and deployed a local computational facility which comprises many service nodes, computational clusters and large scale disk and tape storage services. The resources contribute to a variety of activities such as the analysis centre facility for the next SC4 in which the technical aspects of DA will be tested and evaluated. In this paper we describe the ATLAS DA as well as we present our experience with the deployment, maintenance and operation of the mentioned DA prototype from the whole ATLAS collaboration and from the framework of the Spanish Tier-2 user's point of view.

I. INTRODUCTION

The ATLAS collaboration [1] is preparing for data taking and analysis at the CERN LHC [2], scheduled to start operating in 2007. Physics studies in ATLAS will require analysis of data volumes of the order of petabytes per year. The analysis will reply on the computing resources and the data will be distributed over the world-wide collaborating institutions. These will be collected together and shared in a coordinated way using grid technology that provides the infrastructure required to facilitate the distributed of data and the pooling of computing and storage resources between these institutions. Data for the large samples of simulated interaction, needed to well understand the detector behaviour, will also be distributed between multiple locations.

The grid-based ATLAS distributed analysis aims to deal with the challenge of supporting distributed users, data and processing enabling physicists to exploit the whole computing resource provided by the three ATLAS grid infrastructures: LCG [3], OSG [4] and Nordugrid [5]. DA must support all the analysis activities, including the simulated data production, hiding users from the complexities of the grid environment.

DA is fully described, with emphasis on the ATLAS strategy for distributed analysis in a heterogeneous grid environment. In the following sections we present the IFIC Tier-2 facility available for SC along with our experience gained from using Ganga.

II. DISTRIBUTED ANALYSIS

According to the ATLAS computing model [6], DA will enable users to submit jobs from any location helping them to effectively use the grid for performing their analysis activities. In addition, DA should satisfy the ATLAS analysis model requirement: data is distributed among several computing facilities and analysis jobs in turn routed base on the availability of relevant data. ATLAS activity within DA has several approaches to fully exploit its major grid deployments. Many of these activities are in prototype stage and are not yet deployed on a larger scale. Figure 1 shows the different distributed analysis sub-systems.

DA makes use of several different front-end and back-end systems that are described in the next sections, respectively.

Ganga[7]: Front-end for job definition and management. It is being developed to meet the needs of a user grid interface with the ATLAS and LHCb[8] experiments. Ganga provides user's access to generic distributed systems such as the all grid infrastructures supported by ATLAS; and local batch system, including LSF, PBS and Condor. It is planned to include also the ATLAS production system and further grid flavors like OSG and Nordugrid.

Pathena: Interface to the ATLAS offline software framework (Athena [9]) that is implemented in Python [10]. Pathena allows direct submission of the user-defined jobs to the Panda job management system [11]. Pathena approach is well aligned with Panda and Panda capabilities [12].

ATCOM [12]: Dedicated graphical user interface to the ATLAS production system. It allows user to create tasks and

define jobs in the database. Some activities are going on with the aim to improve it like front-end distributed analysis.

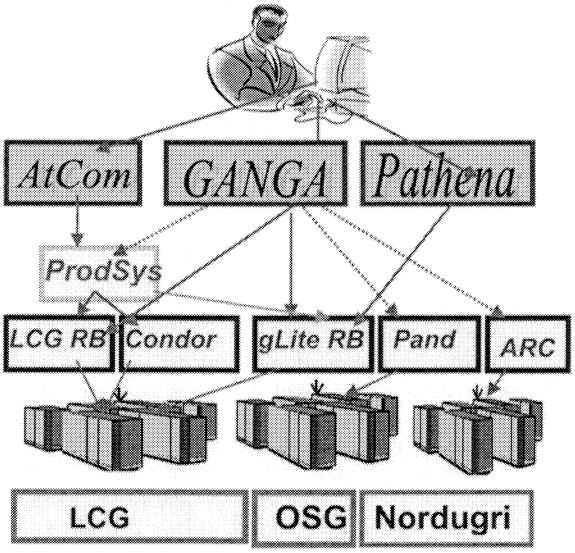

Figure 1: ATLAS Distributed Analysis strategy.

As mentioned ATLAS has adapted a strategy for DA in its heterogeneous grid environment by providing a series of backend job submission systems, which can be illustrated in the middle layer of figure 1.

LCG: Project to build and maintain data storage and analysis infrastructure for the physics community. The main DA target is to access to the LCG resources either via LCG Resource Broker (RB) or CondorG. Both systems showed a good functionality and performance in recent large-scale production exercise.

gLite: Job submission system based on gLite WMS (Workload management system), the EGEE middleware [13], that is the next grid middleware generation. The gLite WMS has a feature which is of particular impact from the distributed analysis point of view: bulk job submission along with improving support for output result retrieval.

ProdSys: ATLAS Production System [14] based in several grid flavours (LCG, OSG and Nordugrid). Jobs are supported by specific executors on the different infrastructure (LCG lexor and CondorG, OSG Panda and Nordugrid Dulcinea). It is being investigated [15] the possibility of submitting analysis jobs using Atcom as front-end.

Panda: Job processing system for production and analysis deployed in OSG. Its key design features are its tight integration with the distributed data management system [16], having a pilot jobs mechanism and a resource brokering.

ARC: Advance Resources Connector, ARC [17] based on the Globus Toolkit [18]. It is a light-weight solution, designed to support a dynamic, heterogeneous Grid facility. ARC client makes intelligent used of the distributed information and data available on the grid. ARC has a job delivery rate of approximately 40 jobs deliveries/min making it useful for distributed analysis. It offers user-friendly monitoring service [19]. Integration ARC into Ganga is currently under test.

III. IFIC ATLAS TIER2

The IFIC ATLAS computing resources are built on the Tier2 centre in Valencia that is a part of the Tier-2 Spanish federation, formed by 3 groups: IFIC, IFAE and UAM. It consists in a farm of 126 Worker Nodes (WN) disposed in racks specially prepared to the adaptation of communication equipment (Table 1). IFIC farm has Fast Ethernet of 100 Mbps. Five disk serves with a capacity of 5 TB and a tape robot with a potential capacity of 140 TB is also available. In terms of software, resources include ATLAS offline releases as well as the Grid infrastructure which is based on the most recent LCG-2 middleware. IFIC site contains all node types to make up a complete Grid. Core services are Resource Brokers (RB), Information Index (BDII), Proxy Sever (PXY) and Virtual Organization Management (VOMS). Resources are provided by the site information Services (GIIS), Computing Element (CE) with Worker Nodes and Castor-based Storage Element (SE) as a back-end to the mass storage facility. IFIC Tier-2 facility serves the dual purpose of providing resources to the ATLAS production and providing Spanish physicists with infrastructure to perform analysis jobs in grid.

Table1: Worker Nodes characterisation.

Athlon K7	63 WNs	63 WNs
CPU	1.2 GHz	1.4 GHz
RAM	1 Gbytes	1 Gbytes
Hard Disk	40 Gbytes	40 Gbytes

IV. SERVICE CHALLENGE 4 PROTOTYPE

The fundamental aim of the Service Challenge (SC) program is to achieve the goal of a production quality world-wide grid that meets the requirements of the ATLAS experiment in term of functionality and scale. DA will be tested for the first time within SC4, where the different DA components will be run in an environment that is as realistic as possible:

- Random job submission accessing data at Tier-1s (some) and Tier-2s (mostly)
- Tests of performance of job submission, distribution and output retrieval

IFIC Tier-2 is contributing in the preparation of DA SC4. This requires a set of resources, where some of them are being put in place on the preproduction service. Next, the steps which are being performed are described.

A. Dada transfer

The Distributed Data Management (DDM) [16] system provides a set of services to move data between grid-enabled computing facilities. In addition to maintain a series of databases to track these data movement. Access to the distributed data is managed by DDM efficient tools. This is crucially important for distributed analysis; hence analysis

jobs are routed based on the data availability in the sites analysis facility.

IFIC Tier-2 is contributing in data transfer task for SC4. It was asked to put in place resources such as a SRM-based Storage Element. A FTS (File Transfer Server) channel to and from the associated Tier-1 (PIC) should be set up on the Tier-1 FTS server with a FTS client software running in the IFIC User Interface (UI). As part of the Tier-2 SC4 milestones, several tests were performed to exercise the FTS channel, between PIC Tier-1 and IFIC Tier-2. Connectivity at high bandwidth from PIC Tier-1 to IFIC Tier-2, with a target rate of ~43Mb/s was demonstrated as well as the FTS channel stability linking the two sites.

As mentioned above the distributed analysis model requires that analysis jobs lend where data exists. To satisfy this with the goal to preparing for the distributed analysis program, a series of activities was started aiming to distributed data using the subscription mechanism from Tier-0 to Tier-1 and then from Tier-1s to its associated Tier-2s, willing to take part in DA SC4. For that purpose, a Disk-only area of 4 TB capacities was put in place and dedicated storage endpoints were created at IFIC Tier-2 for the data flow between PIC Tier-1 and IFIC Tier-2. Figure 2 shows data transfer between PIC-Tier1 and Spanish Federation Tier-2s

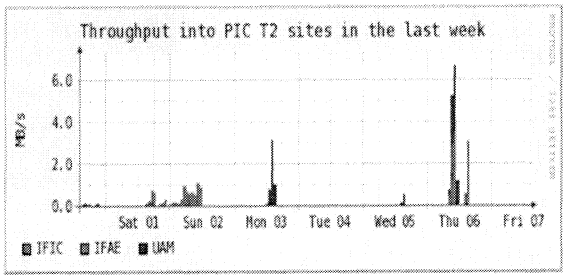

Figure 2: Data transfer from T1 to the its associated T2s in the first week of July 2006

B. Job Priority

As it is mentioned previously, gLiteRB and CondorG/LCG RB are the main job submission systems that ATLAS plans to use for submitting jobs to sites for SC4. On the current infrastructure a site has typically a configuration with one CE per Virtual Organization (VO). In addition, CE is the common entry point for ATLAS production and analysis jobs. This configuration is suitable for large scale very long lasting production jobs, whilst causes a long waiting time for analysis short jobs that require much more less CPU consuming and few time execution.

On the other hand, several batch system configurations scenarios were considered such as specific slots for analysis jobs and CPUs that will to be kept with the production jobs until analysis jobs arrive. These scenarios were excluded because of 1) resources will be wasted when no analysis jobs are arriving on the site and 2) some required resources do not support the model, respectively[20]. ATLAS is putting in place a system for the management of priorities on the LCG/EGEE infrastructure to support that analysis jobs could be performed in parallel to the production ones. The implementation was based on the use of the VOMS (Virtual Organization Management System) mechanism to assign role to a job, and then the role will direct the job to a specific share of the batch system [21]. Driven by the ATLAS requirements, the system, in an initial phase, support limited subsets of roles to control job priority (table 2).

IFIC Tier-2 is taking part of this activity by providing pre-production service (PPS-IFIC). The implementation and configuration of the system was done on PPS-IFIC CE and it works as follows:

- Resources are selected with VOMS credentials
- Ranks are computed using VOView[21] specific information
- Mixing atlas jobs with different roles are executed with the corresponding priorities

Table 2: VOMS Roles defined by ATLAS

VOMS roles	Description
/atlas	All atlas VO users
/atlas/Role=production	Used for Production activity
/atlas/Role=software	Used to software installation
/atlas/Role=lcgadmin	Vo management operation

C. Ganga experience

Although Ganga is still in the development phase it already has functionality that makes it useful for physics studies. An analysis job example for a user task based on the ttbar algorithm was exercised using Ganga. The ttbar reconstructed algorithm is provided by the Physics Analysis Tools (PAT) [22]. Ganga provides a set of ATLAS-specific features such as application configuration based on the Athena framework and input data location based on DDM. It can be run either on the command line, with Python scripts or through a graphical interface. The IFIC Tier2 infrastructure was used to process jobs using our CE with dedicated queues for analysis jobs. The processing is started within a few minutes on all Worker Nodes behind this CE. After job termination program logging and error messages are automatically stored in a job archive together with the job configuration. Also jobs were sent to several LCG sites. In this case the waiting time to get the job executing was very long because of the CE queues were occupied by the production job. Hence, the deployment of the job priority mechanism is relevant important to take full advance from the whole grid infrastructure for distributed analysis. Concerning to Ganga, in terms of configuring, submitting, monitoring and output retrieving has demonstrated a good performance. However, error handling and recovery of failed jobs in the user analysis code needs to be improved by an automatic error parsing.

V. CONCLUSIONS.

The IFIC Tier-2 facility for ATLAS experiment offers functional resources to Spanish physicists willing to perform distributed analysis using grid. In order to face the challenges of real data analysis, the facility needs more functionality and

performance as well as growing in size. To provide good analysis facility, we have therefore to continue installing and testing available software tools to acquire expertise in using and debugging the different pieces of distributed analysis system.

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ATLAS Pixel Detector Timing Optimisation with the Back of Crate Card of the Optical Pixel Readout System

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Abstract

As with all detector systems at the Large Hadron Collider (LHC), the assignment of data to the correct bunch crossing, where bunch crossings will be separated in time by 25 ns, is one of the challenges for the ATLAS pixel detector. This document explains how the detector system will accomplish this by describing the general strategy, its implementation, the optimisation of the parameters, and the results obtained during a combined testbeam of all ATLAS subdetectors.

I. Context

The ATLAS experiment is one of the general purpose detectors that will start exploring unprecedented energies in 2007. One of the major challenges of operating in the LHC environment is the high bunch crossing rate, which is needed to observe rare physics events. After a short ramp-up phase in 2007, this bunch crossing rate will reach 40 MHz. This results in the need to assign the detector information to the correct 25 ns timing window.

The ATLAS pixel detector will act as the vertex detector within the ATLAS experiment. Although it is not included in the first level of the trigger system, it will be the device to tag B-jets by finding secondary vertices. This is one of the key techniques in much of the physics analysis that has been prepared for the next years. For this, the spatial resolution of the pixel detector is the most important feature, as can be seen in the fact that over 90% of the roughly 90 million channels of the whole ATLAS experiment are concentrated in the pixel subsystem, while occupying only 1/400000th of the volume.

To have any chance of exploiting sophisticated tracking algorithms, the hits seen by the sensor need to be assigned to their correct bunch crossing, meaning to the correct 25 ns timing window. As the pixel detector won't be read out every clock cycle, hits wrongly assigned are lost or, if the event to which they've been incorrectly assigned is read out, they will appear as ghost hits.

For the ATLAS pixel detector, as the innermost tracking device, there are several contributions to the timing to be taken into account. As a silicon detector, the collection of the charge released by the passing particles is below 10 ns [5]. This is degrading with irradiation, but can be treated as a constant offset of all pixel cells. The processing of the signal within the first electronic stages is limited by the permitted power-budget.

The timing of each individual ATLAS pixel detector module is important in the sense that the individual clock phases they are running with needs to be adjusted with a precision of less than 1 ns to not lose detection efficiency or produce ghost hits by assigning them to the wrong bunch crossing. To be able to separately adjust each of the 1744 modules within the pixel system, each is driven by its own clock. To cope with all different contributions to the timing difference, this can be delayed in steps of 300 ps with respect to clock delivered from the LHC, to which all internal pixel system clocks will refer. This report shows the results of a study made during the ATLAS combined test beam using a 25 ns timing period. A technique to determine the optimal setting for these clocks is described.

II. The Detector System

As a high energy physics general purpose experiment, the ATLAS experiment provides muon spectrometry, high performance calorimetry, and a very high resolution tracking system. The innermost part of the tracking system is the pixel detector. It is made of 1744 hybrid detector modules. Each module is comprised of: a $2 \times 6\,\mathrm{cm}^2$ sensor, implementing 46080 sensor cells, most of $50 \times 400\,\mu\mathrm{m}^2$ area; 16 readout chips per module, designed in a radiation tolerant deep sub-micron process; and a module controller chip (MCC) to steer the module, mounted on top of a flexible circuit providing the intra-module connectivity. The MCC collects and formats the outgoing data, as well.

III. Electronics

A. ATLAS Pixel Readout System

The readout electronics of the ATLAS pixel detector consists of four major parts:

- The Timing Interface Module (TIM, [1]) receiving the ATLAS-wide timing, trigger, and control signal, and distributing it to the BOCs as clock and command information.
- The Readout Driver (ROD)
  - preparing the control data sent to the modules
  - formatting (event fragment building) of the data sent by the modules
  - performing on-line histograming and calibration.

  To fulfil this, the ROD makes use of a chain of FPGAs for treating the data streams, and independent DSPs for the on-line monitoring and calibration calculations.

- The Back of Crate Card (BOC) acts as the off-detector opto-electrical interface. This is the main component of the timing. The modules are served with individual clock signals. These are derived from the TTC clock as received from the TIM.

- The Opto-Board, acting as the on-detector opto-electrical interface.

B. Back of Crate Card

This card was developed under the leadership of the Cavendish Laboratory, Cambridge (UK), for use in the ATLAS SCT and adapted to pixel detector usage by the authors. It's main function is the opto-electrical conversion of the signals sent to and received from the detector [3]. Conversion and alignment of received data for the first processing stages is done here. For the steering of the detector, clock and data are combined into a single optical signal.

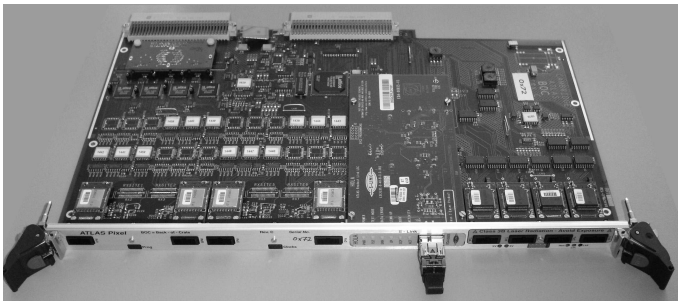

Figure 1: Back of Crate Card

On the detector, the opto-board [4] decodes this into clock and data, which are sent electrically to the modules. As the decoding is done synchronously, this enables the adjustment of the phase of the clock applied to each individual module. For this, the output stage of the Back of Crate Card is able to delay the output stream in steps of 300 ps, up to a maximum of 40 ns. This will allow one to compensate for the differences in cable lengths used, the variations in time of flight caused by the positions of the modules, and other module to module runtime variations.

C. Front End Electronics

The analogue part of each pixel electronics cell is made of a current feedback amplifier, a pulse shaper, and a discriminator applying a threshold to eliminate noise.

1) Time Over Threshold

The current feedback allows for measuring the charge collected within the connected sensor cell by counting the number of clock cycles the signal stays above threshold. Nominally, the feedback current is adjusted to result in a "Time Over Threshold" (ToT) value of 30 for a charge corresponding to the traversal of a minimum ionizing particle (20 ke^-). It is important to realize that for most hits, the charge will be shared by up to four detector cells. Thus, this charge measurement improves the spatial resolution [2] by means of a centroid algorithm, which will be applied off-line.

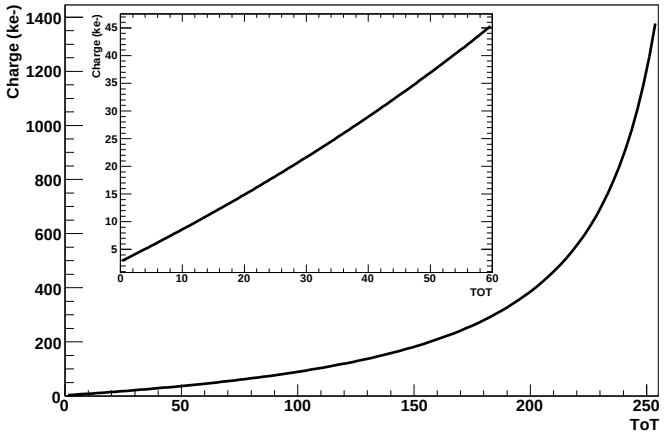

Figure 2: Mean translation of the time over threshold value into charge.

The averaged translation of the measured time over threshold values into the amount of charge collected is given in Figure 2. The time over threshold is measured in number of clock cycles; thus, in discrete numbers. The calibration of the translation into charge is sensitive to many parameters, such as supply voltages and temperature. Therefore, this translation is not applied in the following, but all analysis is done in ToT-values, only.

2) Timewalk

As an effect of the limited power budget and the pulse shaper of each amplifier, lesser charges are registered later than greater ones. This can be by up to three clock cycles.

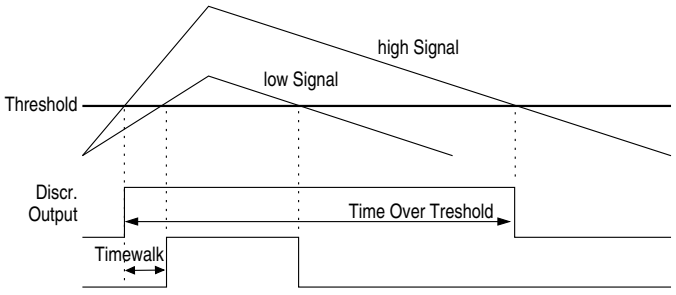

Figure 3: Sketch of time walk

In Figure 3, this is sketched by superimposing a high and a low output signal of the amplifier/shaper stage of a pixel. The slope of the falling part of the signal can be adjusted by the feedback current of the amplifier. This enables the tuning of the ToT. To first order, one can presume that the maximum output of the analogue stage is reached at the same time after particle

traversal, independent of the amount of charge collected.

The timewalk effect will cause a shift of hits with a ToT below a certain value into following events. This is unavoidable, but to be minimized.

IV. MEASUREMENT

In 2004, a slice of the barrel section of the ATLAS experiment was built up at CERN. This combined testbeam setup detected the results of collisions of highly energetic particles with a wire target in front of the slice, in addition to the particle beam itself. The pixel subsystem was comprised of six detector modules arranged in three layers. Each module had an incident angle consistent with what will exist in the barrel section of the final system. This results in a most likely cluster size of two to three pixels.

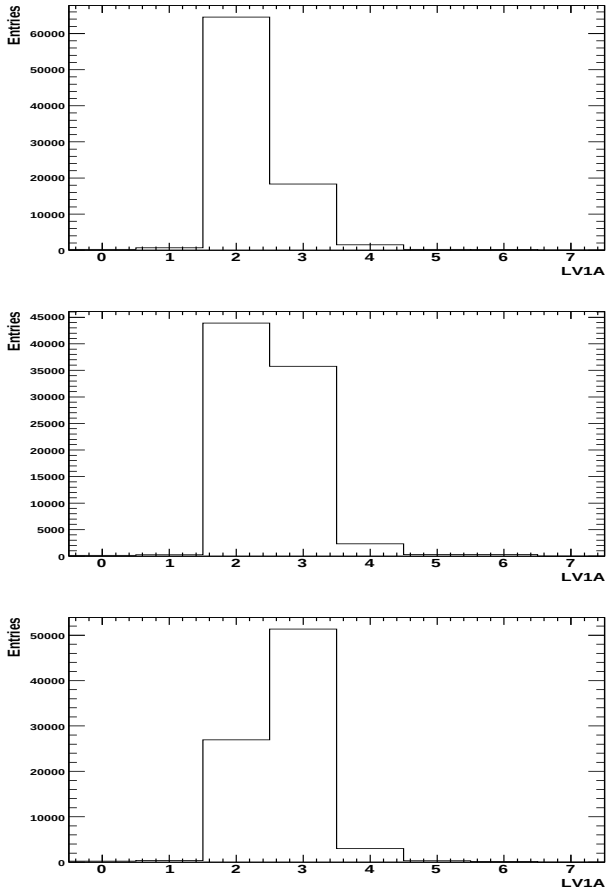

Figure 4: Number of hits per clock cycle for different clock phase settings.

A prototype of the trigger system enabled the recording of track data with the pixel system. For this measurement, an additional feature of the front-end readout electronics was used. For each trigger received, it is possible to cause up to 16 continuous clock cycles to be read out. (Because of bandwidths limits, it will not be possible to make use of this feature at an occupancy given by the ATLAS environment.) As the trigger signal has a fixed latency of 100 clock cycles, this can be used to read out not only the one clock cycle (bunch crossing) that caused the trigger, but also a selectable number before and after this trigger cycle.

Figure 4 depicts the number of hits recorded as a function of clock cycle for three different settings of the delay between event and readout time. One can see that the hits are assigned to different clock cycles by varying this setting.

As Figure 5 shows, the different bins are filled with hits of different charge collected. This is due to the timewalk explained before. For this arbitrary setting of the clock phase of the module, all hits are spread over three clock cycles.

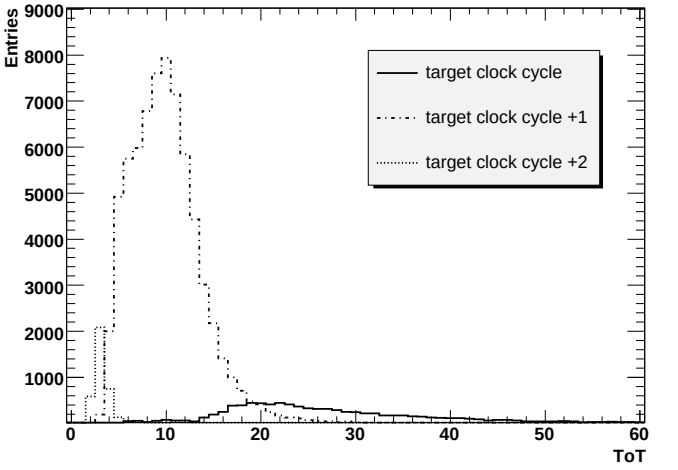

Figure 5: ToT distributions of hits registered to three consecutive clock cycles at arbitrary delay setting

A. *Efficiency*

One may define a registering efficiency as the fraction of hits with a given ToT value assigned to the expected bunch crossing, relative to all hits with this ToT. For one ToT value, the dependence of this efficiency on the delay is shown in Figure 6. Three values can be extracted from this. One is the height of the plateaux, which is the efficiency one can reach for the ToT value inspected. The other two are the delay settings, at which 50% effciency is reached. For the left edge, this is called the “in-time delay”, as for the right edge this is called the “out-of-time delay”. The difference of these values is the assignment time-window defined by the clock-cycle, which is 25 ns.

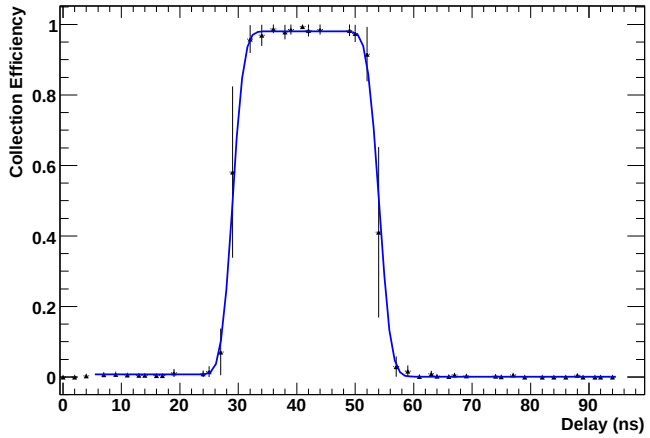

Figure 6: Efficiency vs. delay (fixed ToT=10)

If we now inspect the in-time delay for different ToTs, we can fit a function describing the time-walk behaviour of the front-end electronics. This function approximates the front-end behaviour by presuming that the time when the maximal output of the amplifier stage is reached is independent of the amplitude (see signals sketched in Figure 3). Geometrically, the in-time delay is then given by:

$$T(a) = \frac{t_0 \cdot s}{a} + c,$$

with t_0 the time of the maximum signal, a the amplitude of the signal, s the threshold applied, and c the minimal runtime.

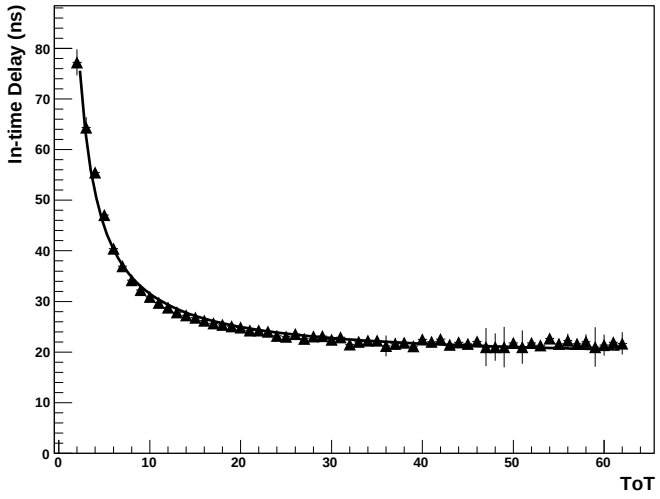

Figure 7: In-time delay as extracted from the rising edges of the efficiency vs. delay plots.

The minimal runtime is fitted as 18.4 ± 0.15 ns in the example shown. Adding the registering window width of 25 ns, one sees that low ToT hits will be registered too late. This is unavoidable. To optimise the delay setting, a map of all registering efficiencies for all ToT-Delay pairs is evaluated in Figure 8. One can think of Figure 6 as a horizontal slice of this.

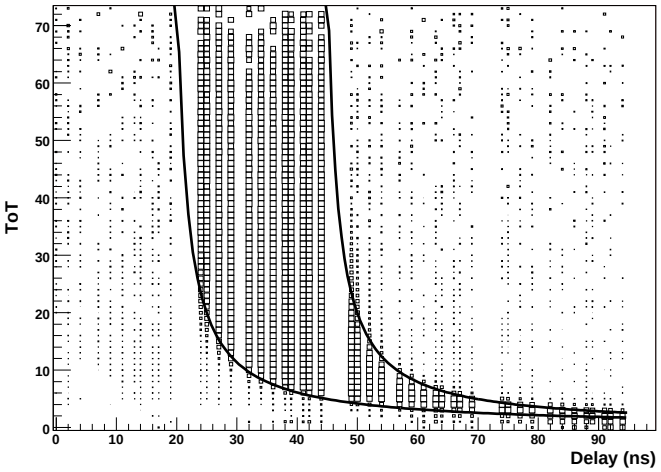

Figure 8: Efficiency of registering a hit correctly.

The curves shown in this map are derived from the fit to the in-time delay (Figure 7) and the registering window width. As one can see, they fit well with the borders of the high efficient region, except of for very low ToT values, which drop below the in-time (the lower) line. This is because the assumption that the time of maximum output of the amplifier is independent of the amplitude is not true.

The optimal delay setting may now be found in the maximum of Figure 9. Here, the sum over all ToTs of the efficiencies for a given delay is plotted. This is the integral of the vertical slices of Figure 8.

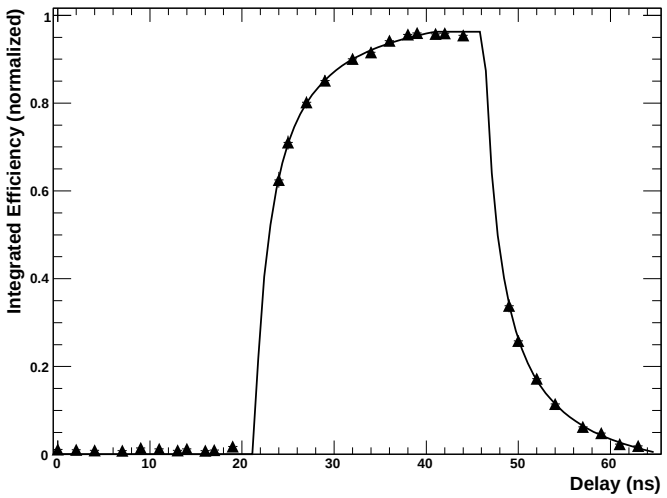

Figure 9: Total Efficiency.

The function fitted to this takes into account the values ob-

tained by the fit to Figure 7 and the fact that the ToT range is limited. In addition, there's a scaling factor applied to account for the fact that the curve does not reach 100%. This is caused by the structure of the beam used, as one can observe in the "out of band" entries in Figure 8. These are caused by out of bunch particles.

V. Results

As Figure 10 demonstrates, it is possible for nearly all hits to be registered correctly, except for those of very low charge. This does not effect the detection efficiency, as these hits with a very low amount of charge are primarily caused by unequal charge sharing of neighbouring sensor cells.

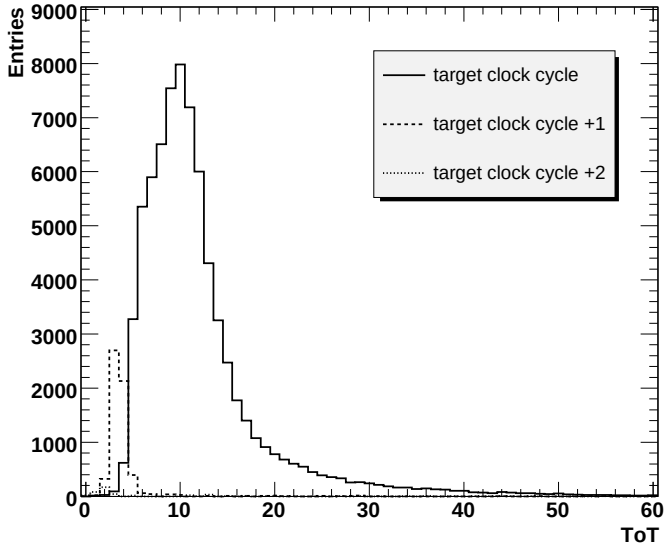

Figure 10: ToT distributions of hits registered to three consecutive clock cycles at tuned delay setting

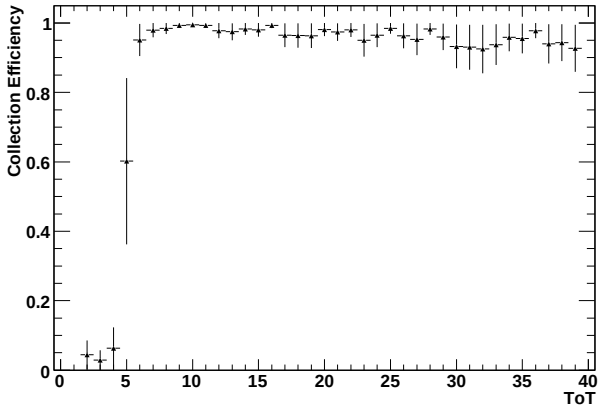

Figure 11: Efficiency vs. ToT (optimised Delay)

A simplified method is demonstrated in Figure 11. Here, only the in-time delay of hits with ToT=30 was measured, and the delay was set to this value minus 5 ns. This results in a competitive setting, where ToTs above 5 are assigned to their event correctly.

VI. Conclusion

A method was implemented and tested to optimise the clock phases of the ATLAS pixel detector modules with respect to the correct assignment of tracks to their bunch crossing. It measures the in-time and out-of-time delays and determines the maximum efficiency. This results in a very good performance of the detector system. Further modifications are needed to apply this method to the high occupancy environment of the LHC. For this, an "inverted" method minimising the hits registered to empty clock cycles is envisaged.

The authors would like to thank all who contributed to the ATLAS combined testbeam.

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Time Resolution of a Few Nanoseconds in Silicon Strip Detectors Using the APV25 Chip

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Abstract

The APV25 front-end chip for the CMS Silicon Tracker has a peaking time of $50\,\mathrm{ns}$, but confines the signal to a single clock period (=bunch crossing) with its internal "deconvolution" filter. This method requires a beam-synchronous clock and thus cannot be applied to a (quasi-) continuous beam. Nevertheless, using the multi-peak mode of the APV25, where 3 (or 6,9,12,...) consecutive shaper output samples are read out, the peak time can be reconstructed externally with high precision. Thus, off-time hits can be discarded which results in significant occupancy reduction. We will describe this method, results from beam tests and the intended implementation in an upgrade of the BELLE Silicon Vertex Detector.

I. Introduction

In today's high energy phyics experiments, silicon strip detectors are typically used to measure particle tracks thanks to their good spatial resolution. The original detector signal also provides very precise timing, but this information is lost with the common architecture of a shaping front-end amplifier with a single sampling point. However, preserving the time information can be essential for tracking in future experiments with high particle density and frequency, such that detected hits can unambiguously be associated to each other and to a certain point in time, thus allowing to discard all hits which do not belong to the event of interest. Such a procedure would allow significant reduction of data on-line, and hence ease computing, storage and off-line efforts.

The potential application of a silicon strip detector with time information ranges from upgrades of existing systems to new detectors such as the ILC. In particular, this work was performed in the framework of the BELLE experiment at KEK (Tsukuba, JP). Its present Silicon Vertex Detector (SVD2) [1] is facing the limits imposed by the slow front-end amplifier with a shaping time of $800\,\mathrm{ns}$, which causes an occupancy of about 10% in the innermost layer at the present luminosity of about $1.6 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

II. The APV25 Front-End Chip

The APV25 [2] was developed for the CMS experiment at the LHC. It is manufactured in a $0.25\,\mu\mathrm{m}$ CMOS process and tolerates up to $100\,\mathrm{MRad}$ of radiation. The APV25 is designed for operation at $40\,\mathrm{MHz}$ with a default shaping time of $50\,\mathrm{ns}$ (adjustable between $35\,\mathrm{ns}$ and $200\,\mathrm{ns}$) and has an analog pipeline of 192 cells depth for each of the 128 input channels, where sampled values of the shaper output are stored at the beam synchronous clock frequency of $40\,\mathrm{MHz}$.

A "deconvolution" analog pulse shape processor [3] (switched capacitor filter) is included on the chip which creates a weighted sum of three consecutive samples. This results in a narrowed output pulse which is (ideally) just a single clock wide, and hence the measured signal can unambiguously be assigned to a certain bunch crossing of the clock synchronous LHC beam. This gain in time resolution is traded off against a higher noise figure.

The "deconvolution" method requires shaper output sampling (APV25 clock) which is synchronous to the bunch crossings, as it is the case at CMS. In other experiments with a (quasi-) continuous beam such as BELLE, this feature does not work, since the APV25 sampling is always clock-synchronous and also its trigger input is synchronized internally. However, the APV25 also offers the functionality to read out three consecutive samples without processing. By repeatedly sending a trigger pulse in this "multi-peak" mode, one can read out up to 30 consecutive samples of the shaper output, spaced by the clock period of $25\,\mathrm{ns}$.

III. Peak Time Determination

Peak time and amplitude can be obtained by applying a fit function to the sampled shaper output values. Fig. 1 shows a typical event with twelve samples, where two different fit functions were applied: The function

$$v_{\mathrm{out}} = A\,\frac{t}{T_p}\,e^{-\frac{t}{T_p}} \quad , \tag{1}$$

denoted "Exp fit", is the output of an ideal CR-RC shaper with the shaping time T_p, but the actual output slightly deviates from this waveform, particularly in the rising edge and the tail. Hence, another fit was performed with the waveform obtained by internal calibration of the APV25, where the measured points were connected with cubic splines ("IntCal fit"), which yields better fit results.

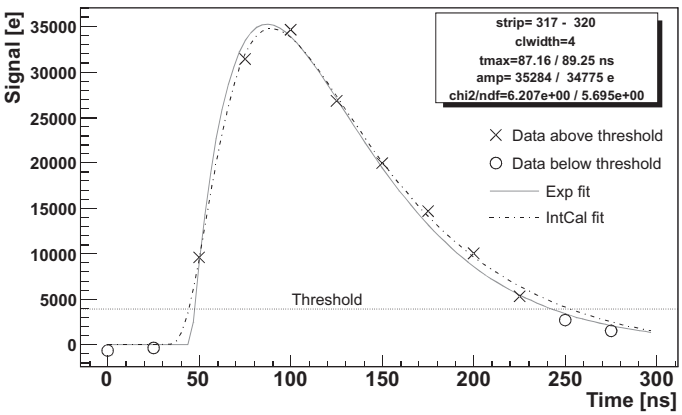

Figure 1: Sampled shaper output values with two different fit functions applied. See text for details.

The actual shaping curve depends on the capacitive load at the input (i.e. the detector geometry) and the bias settings of the front-end amplifier, which can be adjusted in a wide range. Thus, the waveform can be tuned to achieve shaping times between 35 and 200 ns. Clearly, this has implications on power consumption, signal-to-noise and achievable timing precision. All results shown here were performed with the default shaping time of 50 ns for which the APV25 was designed.

IV. Test Setup

Two different detector modules were built for studying the peak time finding. Both use double sided silicon detectors designed for BELLE SVD upgrades. The "UV striplet" [4] type is a candidate for the innermost part of the SVD3 which is a conceptual design for Super BELLE. It has short strips (10 mm) arranged at an angle of 45° against the edge. The strips on the opposite side are rotated by 90° to achieve stereo measurement. The thickness of this sensor is 300 μm, and it has AC coupled strip implants with 51 μm readout pitch on both surfaces. On the p-side, an intermediate floating strip is located between each pair of readout strips, while the n-side readout strips are enclosed by an "atoll" type p-stop. Fig. 2 shows one side of the sensor-hybrid assembly with four APV25 chips on each side.

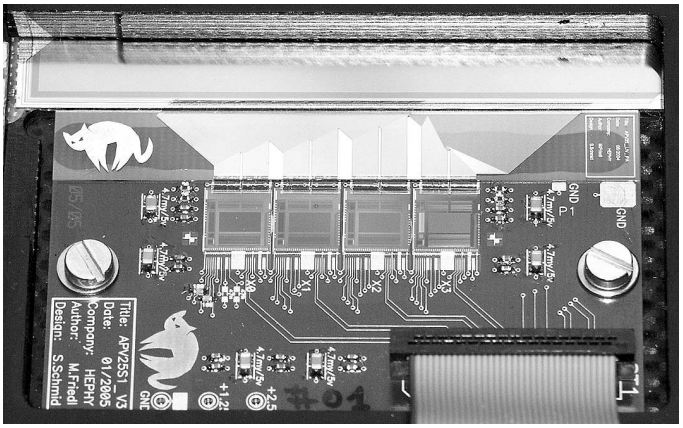

Figure 2: One side of the "UV striplet"-APV25 front-end assembly. The opposite side is an exact mirror image hidden by the support structure.

The other module is based on a bigger silicon detector ("DSSD") which is very similar to the existing SVD2.0 and will be used in the intermediate SVD2.5 upgrade. Its dimensions are $80 \times 28\,\mathrm{mm}^2$ with a thickness of 300 μm. The p-side has long and dense strips (51 μm readout pitch), while the n-side contains the same number of strips which are consequently short and wide (152 μm readout pitch). Both sides are equipped with floating intermediate strips, and again "atoll" p-stops are used on the n-side.

The BELLE SVD consists of ladders composed of one or more sensors read out from the short edge which is also the boundary of the detector acceptance. Thus, the p-side readout is trivial because its strips are all accessible on the short edge. For the n-side however, there is no such option. The traditional solution is to use a fanout (or double metal layer) at an angle of 90° against the strips to guide each strip to the short edge. The length of the resulting lines ranges from (almost) zero to the full length of the sensor, thus introducing a considerable additional capacitance which increases the noise figure. It becomes even worse when concatenating two (or more) sensors.

In order to avoid this problem, a novel approach was chosen for the arrangement of the readout chips on the n-side. Those are mounted on a thin double-layer flex circuit which sits on top of the silicon sensor. A thin layer of Rohacell [5] is put between sensor and flex-hybrid for thermal and electrical insulation. The APV25 chips are thinned to 100 μm to minimize the material budget and carbon fiber pipes are used as a support structure and for cooling. The pitch adapter between sensor and the APV25 inputs is a part of the flex circuit. Since this technology requires a certain feature size, the lines are arranged on both layers of the flex in an alternating way. Fig. 3 sketches the cross-section of the module assembly.

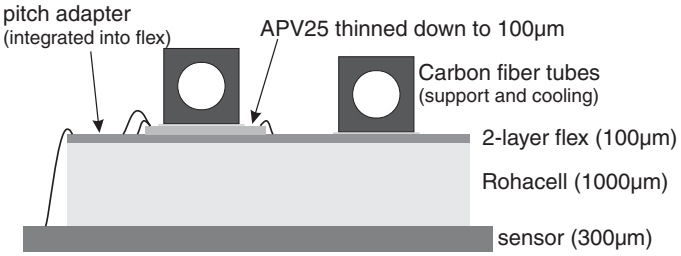

Figure 3: Schematic cross-section of the flex-hybrid module (drawing has different scales in x and y directions).

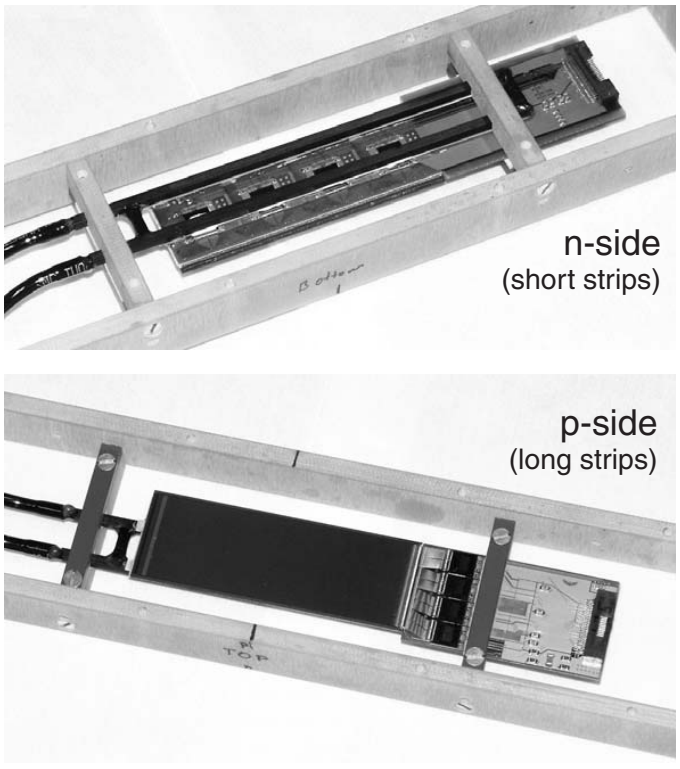

Figure 4: The two sides of the flex-hybrid module.

Fig. 4 shows photographs of the real module. While the n-side flex-hybrid is mounted on the sensor as described above, the p-side is read out from the side in a conventional way using the same type of flex-circuit, such that it could be put on top of the adjacent sensor in case of long ladders,

The detector modules were controlled and read out by the home-made "APVDAQ" system, consisting of a repeater board and a VME module for each hybrid. A floating power scheme is adopted on the repeaters, where the front-end local ground is connected to the bias voltage of the corresponding detector side. This method requires floating power supplies for each side and the translation of signals for both control and data, which is performed with optocouplers in case of slow signals (I2C and reset) and capacitors for fast signals (clock, trigger, analog data).

Since we measure several samples along the shaper output waveform, the data processing requires additional steps compared to the standard single-sample procedure. Analysis starts with the usual pedestal subtraction, common mode correction and zero suppression algorithms independently for each time slice. Then, a "clump finding" procedure is applied which is the extension of cluster finding in the space-time domain to determine contiguous hit blocks. The clump signals are summed up for each time slice, resulting in a curve as shown in fig. 1. Finally, a fit is applied to each curve, returning amplitude and time information.

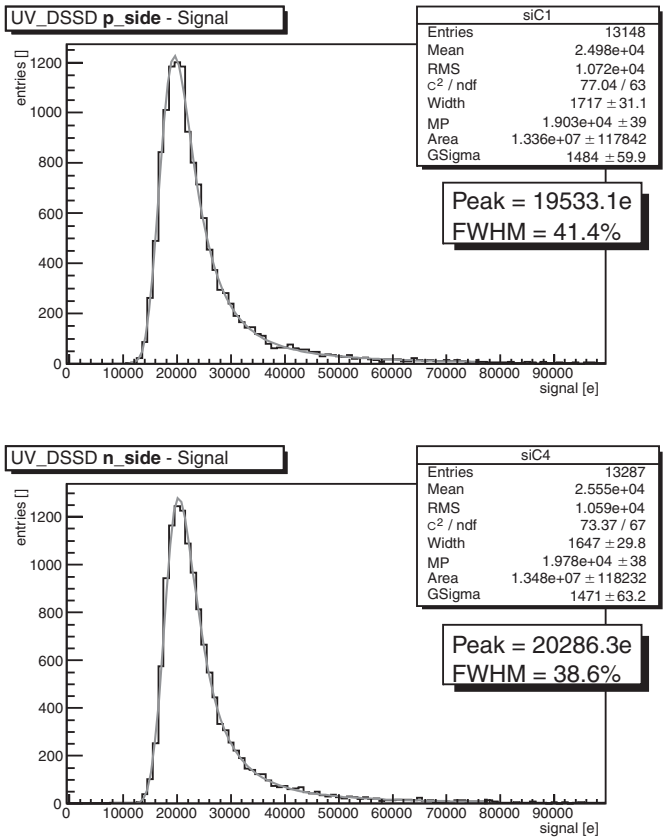

Figure 5: Signal distributions for p- and n- sides of the UV striplet detector at perpendicular incidence, fitted by a convolution of Landau and Gauss. The APV25 internal calibration was used to convert the ADC scale into charge.

V. Experimental Results

The UV striplet module was tested in beams at KEK in April 2005 and four months later at PSI (Villigen, CH), where the DSSD module was also tested in August 2006.

The depletion voltages of the sensors were obtained by CV measurements and found to be $65\,\mathrm{V}$ for the UV striplet and $46\,\mathrm{V}$ for the DSSD sensors, respectively. A bias voltage scan in the KEK beam test confirmed the CV result for the UV striplet sensor. Throughout the tests described here, a bias of $80\,\mathrm{V}$ was applied to the sensors, which is the standard value used in the BELLE experiment and ensures full depletion.

The APV25 chips were operated at $40\,\mathrm{MHz}$ which was completely unrelated to the particle beam. Since the APV25 only accepts clock-synchronous triggers, a jitter of $\pm 12.5\,\mathrm{ns}$, corresponding to the width of one clock cycle, is introduced by the synchronization of the scintillator/photomultiplier trigger signal. In order to obtain a reference time, the distance between the unsynchronized trigger and the next clock edge was measured by a TDC. The flat distribution of measured TDC values confirms the independence of beam and clock.

The "IntCal fit" (see section III.) returns two parameters, peak amplitude and peak time. By histogramming the fitted amplitudes, one gets the signal distribution which perfectly fits to a Landau shape, convoluted with a Gaussian component to account for electronic noise and (dominantly) intrinsic detector fluctuations [6]. Fig. 5 shows the signal distributions for both p- and n-sides of the UV striplet detector.

Fig. 6 shows the correlations between TDC measurement and fitted peak time as well as the residual distributions (error) for both p- and n-sides of the UV striplet detector. An RMS resolution of 2.2 and $1.6\,\mathrm{ns}$ was obtained, including the uncertainty of the scintillator/photomultiplier which is estimated to be about $1\,\mathrm{ns}$.

These measurements were performed at a cluster signal-to-noise of 25. Obviously, the precision of the time finding method strongly depends on that number. A preliminary analysis of the DSSD module, which has longer strips than the UV striplet sensor and thus higher capacitance and noise, returns a cluster signal-to-noise of 14 and 19 for p- and n-sides, respectively. The RMS residuals for the time measurement become 3.9 and $2.3\,\mathrm{ns}$ which is consistent with simulation.

Since each particle creates a signal that is read on both p- and n-sides, correlations between those measurements are another indicator of the quality. Fig. 7 shows the relations obtained with the UV striplet module at perpendicular beam incidence, where a linear fit was applied to determine the associated error. For the signal, the offset was fixed at zero, obtaining a slope slightly higher than one, which can be attributed to the different detector layout on p and n sides, regarding floating strips and p-stop, respectively. For the fitted peak time, the slope was held at unity, while the intercept was returned by the linear fit. The offset in the fitted peak time reflects the difference in the clock phase for p- and n-sides, which stems from the clock distribution scheme

used in the KEK beam test and was confirmed by direct measurement at the front-end.

The RMS residual of the signal correlation is in the same order of magnitude as the Gaussian component in the signal fit, while the fitted peak time error matches with the individual measurements against the TDC. Hence we conclude that the method works fine and yields reasonable results from the statistical point of view.

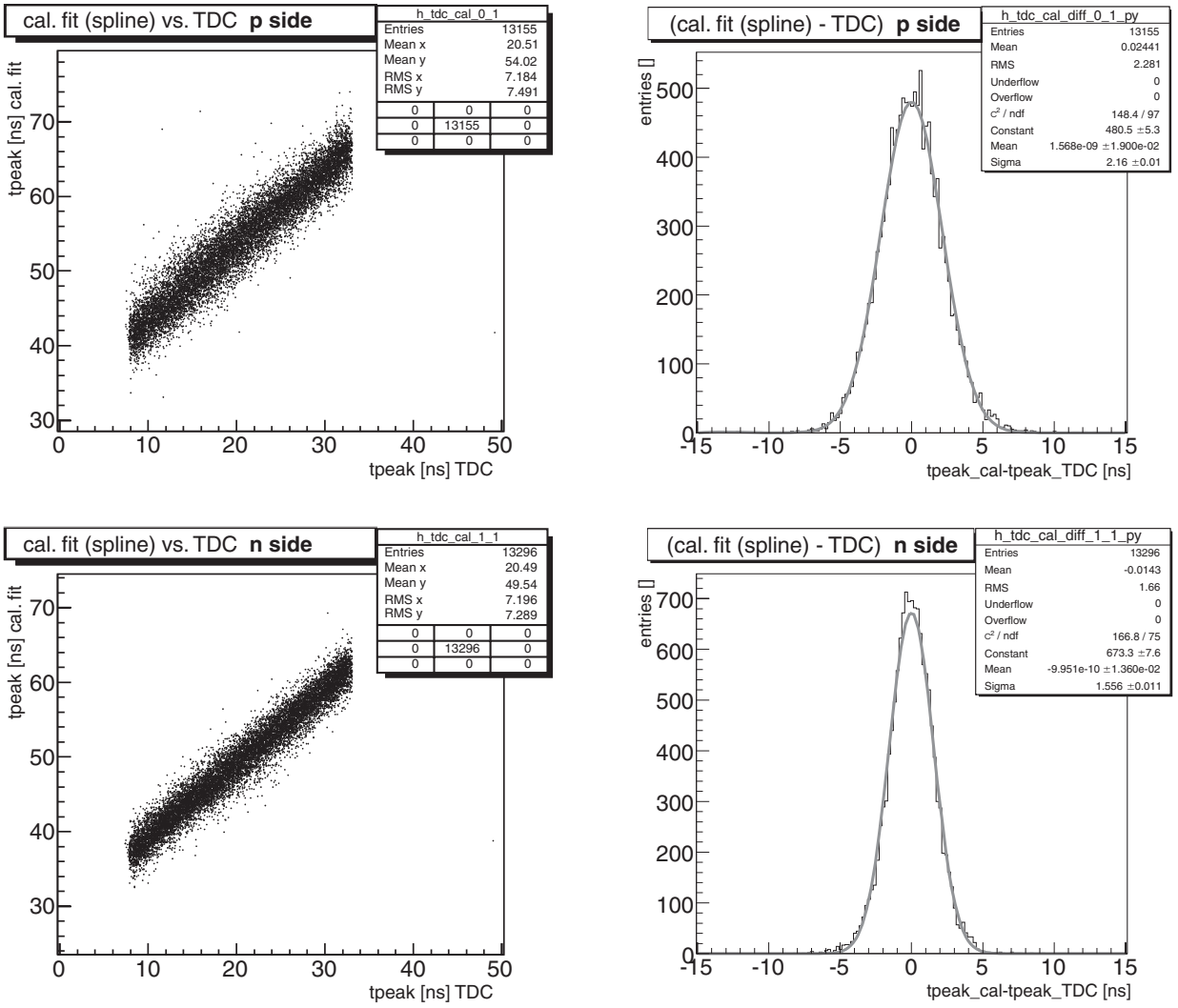

Figure 6: Top row: p-side. Bottom row: n-side. Left column: Correlation between TDC and fitted peak time (offsets are arbitrary). Right column: Residual distribution (error) of the fitted peak time. See text for details.

VI. Future Implementation

Using a numeric fit for each hit is useful for the analysis of a beam test, but not feasible for real-time processing in an experiment with a large number of channels and hits. Hence, we will replace the fitting algorithm by a look-up table which can be implemented in an FPGA. It has been shown that the timing information is essentially contained within three samples around the peak which reduces both readout and processing effort.

The amplitudes of the three samples around the peak will be combined to form the address of the look-up table (RAM array). Each memory cell contains peak time, amplitude and a quality value that specifies their reliability (similar to the χ^2 value of a fit). In parallel, the trigger timing will be measured with a TDC. No matter whether a numeric fit or a look-up table is used, the peak time measurement is not exact due to noise, hence a certain tolerance has to be allowed depending on the quality value. The internal calibration feature of the APV25 can be used to fill such a look-up table, where timing and amplitude are specified and sample triplets are measured.

The FADC processor module for an upgrade of the BELLE Silicon Vertex Detector is being developed. This board does not only digitize incoming APV data, but also performs pedestal subtraction, a two-pass common mode correction, and zero suppression (sparsification). Finally, the timing of hits will be determined by a look-up table as described above.

Several variants of such a look-up table, all compatible with the FPGAs used for processing, were evaluated by simulation and compared to the fit method. Only minor differences were observed between the implementations, and the deviation from the fit results was negligible compared to the required precision in all cases.

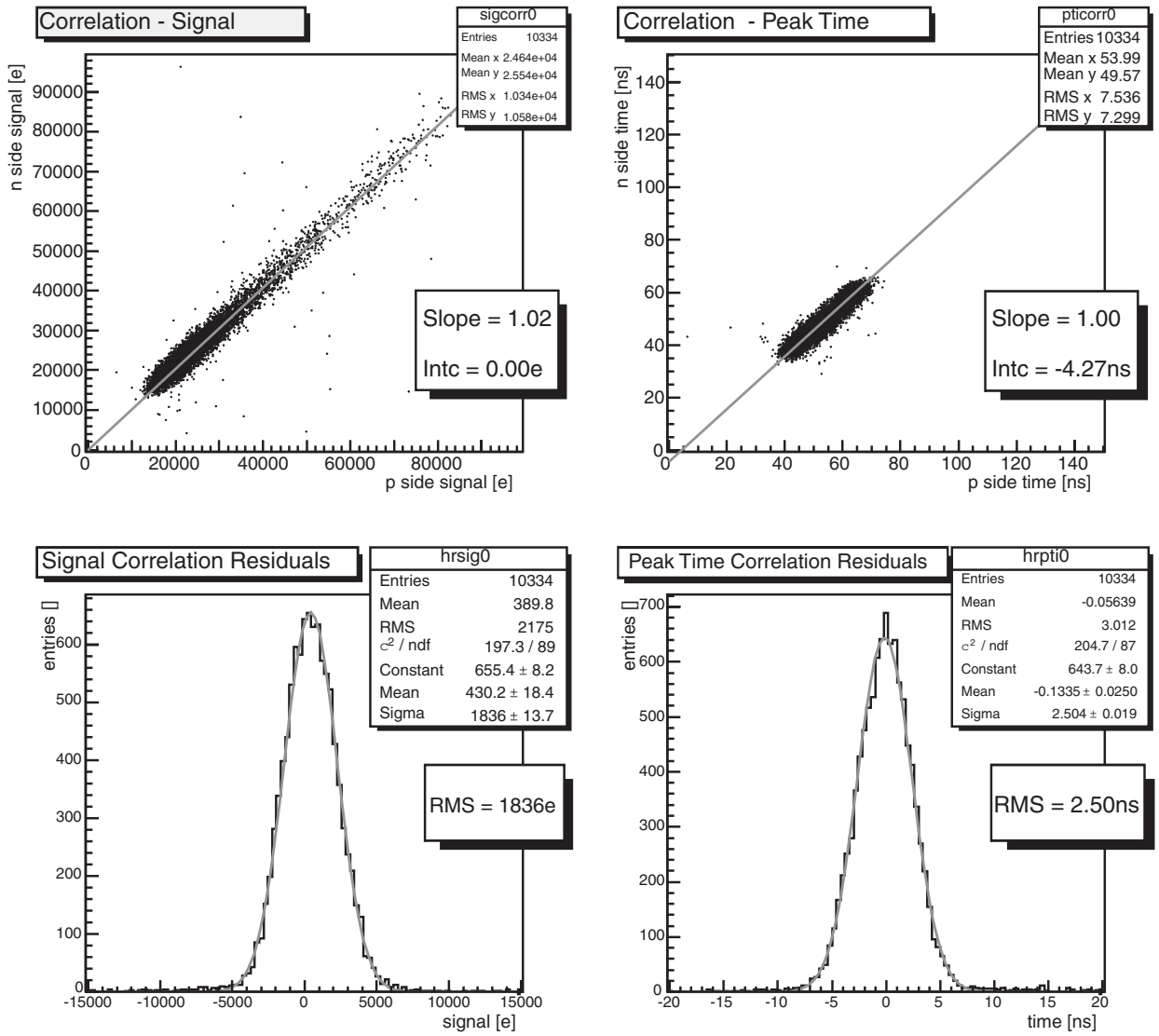

Figure 7: Correlations for signal and fitted peak time obtained at perpendicular incidence. See text for details.

VII. Summary

The APV25 front-end chip can preserve the timing information of silicon detector signals, either by using the built-in "deconvolution" circuit, or by reconstructing the shaping curve from multiple sampled points. Using the latter method, a time resolution of about 2 ns RMS was obtained in a beam test with the UV striplet sensor at a cluster signal-to-noise of 25. Measurements performed on the DSSD sensor with longer strips returned an RMS error of 3.9 ns at a cluster signal-to-noise of 14. Correlations between p and n sides show a spread consistent with that obtained by independent measurements. In the SVD2.5 upgrade of the BELLE Silicon Vertex Detector, this method will be implemented using FPGAs with look-up tables to determine the hit timing on-line. With that information and the trigger time, which will also be measured as a reference, hits can be associated to each other and off-time background can be discarded, allowing a high trigger rate with significant on-line data reduction.

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Revised CMS Global Calorimeter Trigger Functionality & Algorithms

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Abstract

The Global Calorimeter Trigger (GCT) is a device which uses data from the CMS calorimeters to search for jets, produce isolated and non-isolated electron lists and compute all the transverse and missing transverse energy sums used for the Level-1 trigger decision (L1A). GCT performs these functions by receiving and processing the data from the Regional Calorimeter Trigger (RCT) and transmitting a summary to the Global Trigger (GT) which computes the L1A decision. The GCT must also transmit a copy of the RCT and GCT data to the CMS DAQ. The vast amount of data received by the GCT (230 Gb/s) as well as the necessity for data sharing required by the jet finder impose severe constrains on the GCT design. This paper presents an overview of the revised design, in particular, the algorithms, data flow and associated latency within the revised GCT.

I. INTRODUCTION

The GCT is the last stage of the calorimeter trigger chain. Its primary purpose is to reduce the number of calorimeter trigger objects that need to be processed by the GT to produce the L1A decision [1]. The pipeline memories that store the event information prior to a L1A decision have only a limited depth and thus the trigger latency is limited to 3.2μs.

A detailed description of the GCT is beyond the scope of this paper and is covered in detail in the CMS Trigger TDR [1] and several subsequent CMS internal notes [2,3].

The trigger objects computed by the GCT from data supplied by the RCT are listed below and described in subsequent paragraphs.

- 4 isolated and 4 non-isolated electrons of highest rank
- 4 central, 4 forward , 4 tau clustered jets of highest rank
- total transverse energy
- total missing transverse energy
- total jet transverse energy
- 12 jet counters

The 'rank' of an electron or jet is at present its transverse energy; however, in principle it could also be derived from jet location.

The electron sort operation must determine the 4 highest rank objects from 72 candidates, supplied by the RCT, for both isolated and non-isolated electrons from a significant data volume (29Gb/s per electron type).

To sort the jet clusters according to rank the GCT must first perform jet cluster finding and convert the clustered jet energies to rank. The clustered jets are created from regional transverse energies supplied by the RCT. The latter are the sum of contributions from both the hadronic and electromagnetic calorimeters. This is a substantial extension of the GCT capability beyond that specified in the Trigger TDR [1].

The jet cluster finding and subsequent sort is more challenging because of the larger data volume (172.8 Gb/s) and the need to share or duplicate data between processing regions to perform cluster finding. The latter can require data flows of a similar magnitude to the incoming data volume depending on the clustering method used. The clusters, defined as the sum of 3x3 cells, are located using a new method, which is described in Section III. It requires substantially less data sharing than the sliding window method.

Jets are subdivided into central, forward and tau jets based on the RCT tau veto bits and the jet pseudorapidity, η.

The GCT must also calculate some additional quantities. The total transverse energy is the sum of all regional transverse energies. The total missing transverse energy is calculated by splitting the regional transverse energy values into their x and y components and summing the components. The resulting vector, after a rotation of 180°, provides the magnitude and angle of the missing energy.

The total jet transverse energy is the sum of all found clustered jets. There are 12 jet counters that are calculated from rank and position criteria.

In addition to these tasks the GCT: (a) acts as a readout device for both itself and the RCT by storing information until receipt of a L1A and then sending the information to the DAQ via a SLINK64 interface (b) extracts trigger information for the muon system from the calorimeter data stream (c) monitors the LHC luminosity.

The revised design is discussed, although the hardware details are kept to a minimum as they are presented in a separate talk at this conference [4]. The data processing firmware, in particular the algorithms and associated latency within the revised GCT, are presented.

II. System Overview

The GCT is a challenge to build because (a) the data volumes and processing require many large FPGAs and thus multiple PCBs (b) the PCBs must be connected together to allow data sharing and to eventually concentrate the data into a single location for the sort algorithms (c) the latency allowed is 24 bunch crossings for jets and 15 bunch crossings for electrons. Ideally one would use high speed serial links to transport the large data volumes between FPGAs; however, these typically require several clock cycles to serialise/deserialise the data and thus they have to be used sparingly to keep the latency low. The final architecture (fig. 1) uses high speed optical links (1.6 Gb/sec actual and 1.28 Gb/sec effective) to concentrate the data in the main processing FPGAs, followed by standard FPGA I/O to connect to downstream FPGAs. There are two main trigger data paths; electron and jet.

A. *Dataflow*

A block diagram of the GCT system is shown in figure 1. The input to the GCT is 18 RCT crates. The 72 Source cards retransmit the data on optical high speed serial links (shown by dashed arrows). For each RCT crate, the electron data is transmitted on 3 fibres, the jet data on 10 fibres and the muon data on 1 or 2 fibres (not shown).

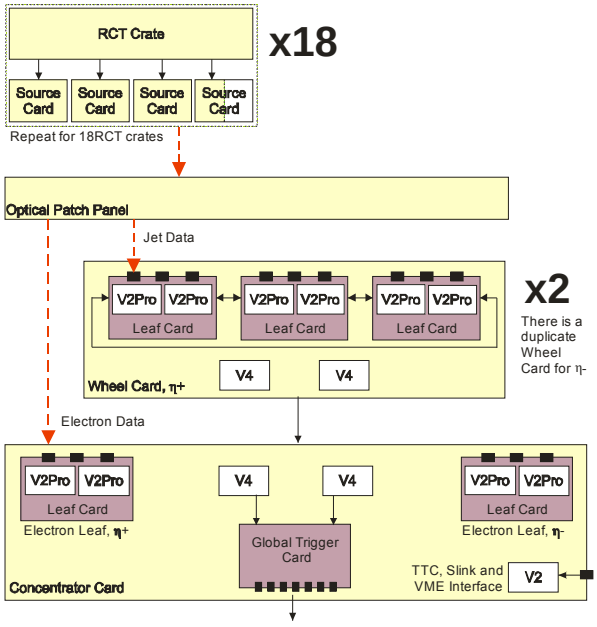

Figure 1: Block diagram of GCT system. Dashed arrows indicate high speed optical links. The 23 large FPGA devices in this design are indicated as squares with the either a symbol 'V2P' (Virtex-II Pro), 'V4' (Virtex-4) or 'V2' (Virtex-II) inside.

The jet data are sent to Leaf cards (configured for Jet finding) mounted on the Wheel cards. The Leaf cards are connected in a circle to search for clustered jets in one half of the CMS calorimeter (either in the positive or the negative η). The Wheel card collects the results from 3 Leaf cards, sorts the clustered jets and forwards the data to the Concentrator.

The electron data are sent to Leaf cards (configured for electron sorting) mounted on the Concentrator.

The Concentrator performs a final sort of electrons and clustered jets and send the results to the Global Trigger.

In addition to this the jet data is also used to calculate the transverse energy sums and jet counts; however, these tasks do not impose the significant constraints on the design, other than some extra FPGA I/O.

B. *Source Card*

The 6 differential ECL cables per RCT crate are fed into Source cards (fig. 2), which will be installed in the same racks as the RCT. The Source cards have been designed by Imperial College. They receive up to two RCT cables and transmit the data over 4 fibre links using 4 HFBR-5720 single fibre transmitters operating at 850nm. This has several advantages. It allows the Source cards to be electrically isolated from the main GCT system. It allows the different data within the RCT cables to be rearranged (e.g. electron data can be split from muon data so they can be sent to different destinations). It allows a large amount of information to be concentrated so that it can be delivered to the processing FPGAs on Leaf cards. It allows data to be duplicated.

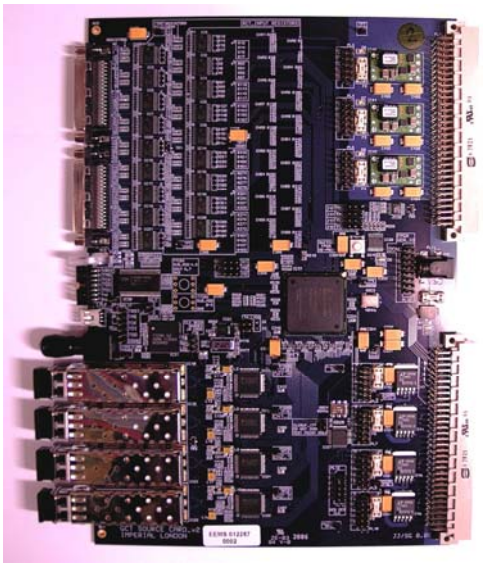

Figure 2: The Source card. The RCT inputs are visible in the top right of the picture. The 4 SFP cages are in the bottom right. All the signals are routed through a Xilinx Spartan 3 (XCS1000-5FG676C).

C. *Leaf Card*

A Leaf card (fig. 3) is the main processing block in the GCT design. It is a dual CMC card designed at CERN and produced by LANL. The most difficult task in the GCT is the jet clustering. This is made simpler by concentrating the data in as few FPGAs as possible. Consequently, the Leaf card has 2 Virtex II Pro FPGAs (XC2VP701513C), each with 16 multi-gigabit transceivers that are used to bring the raw data in. Three Agilent AFBR 742B 12 channel receivers provide the opto-electronic interface. The large standard I/O are used

to transmit the data to the Wheel card. Each Leaf card in jet finding mode transmits to the Wheel card the 18 clustered jets, total transverse energy and missing transverse energy.

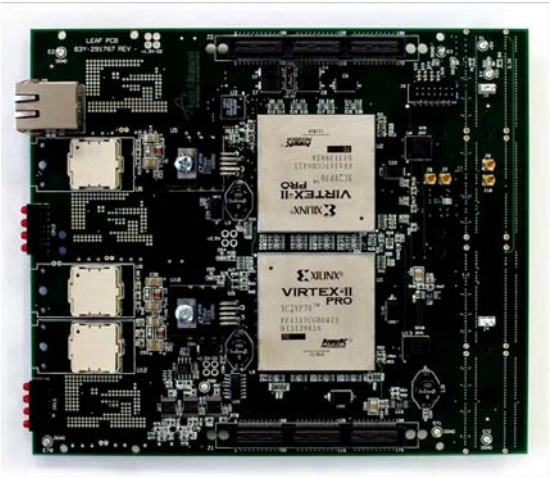

Figure 3: The Leaf card. The LVDS Samtec connectors that provide Leaf-to-Leaf card connection are visible at the top and bottom.

D. *Wheel Card*

There are 2 Wheel cards, one for each half of the detector. They are 9U, 400mm, VME cards (albeit without a VME interface) that act as carriers for 3 Leaf cards and further concentrate the data. They sum the energy values and jet counts (number of clustered jets found in η-φ regions). They also sort the 54 clustered jets by rank into the 3 types (forward, central, tau). The Wheel cards then forward the information to the Concentrator card via high speed Samtec LVDS cables.

E. *Concentrator Card*

The 9U, 400mm, VME Concentrator card performs similar actions to that of the Wheel Card after which it transmits the resulting trigger objects to the Global Trigger and stores the information in a pipeline until receipt of a L1A trigger. The Concentrator also carries 2 Leaf cards, which process the electron data. These Leaf cards record the incoming RCT data in a pipeline memory until receipt of a L1A and perform a fast sort on the incoming data.

The interface to the GT is another dual CMC card that contains National DS92LV16 SERDES chips, of which 14 are used to transmit data to the GT and 2 are used for loopback testing. Infiniband High Speed Serial Data 2 connectors and cables are used to receive/transmit the data in pairs at an effective rate of 2x1.28 Gb/s per pair.

III. Processing Methods & Algorithms

A. *Clustering*

Traditionally, the clustering method used in the CMS trigger design was based on a 3x3 sliding window. The jet clusters, defined as the sum of 3x3 cells, were found by a sliding window that traversed the η-φ space of 22x18 regional transverse energy values. In this method a cluster was created if the central value of the 3x3 array was larger than the 8 neighbouring cells.

This method was simple and symmetric; however, the processing could not easily be split into regions without sharing or duplicating the boundaries of the regions.

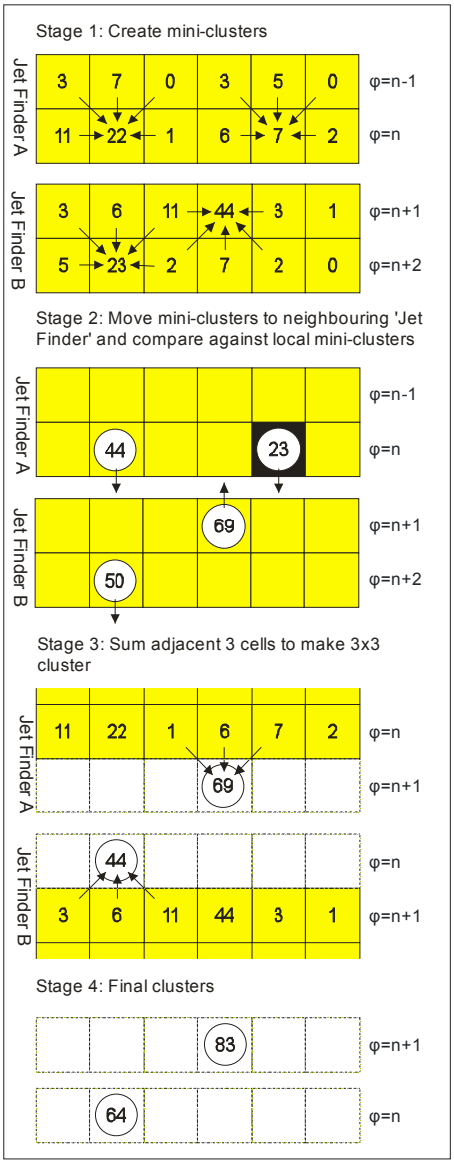

Figure 4: The Jet cluster method. There are 6 cells in η shown, but there are 11 cells per 1/2 detector.

The current method, called the 'Jet Finder', receives data from a single RCT crate that spans 2 cells in φ (40 degrees) and 11 cells in η (half the detector). It also receives duplicated data from the next 2 adjacent cells in η (i.e. at η = 0) that are located in the other half of the detector (i.e. these 4 cells span the same φ region, but have η with the opposite sign). Duplicating the cells at η = 0 allows the processing regions to be independent and thus in physically different locations. The current method only uses the immediately adjacent cells in η and thus the Jet Finder operates on a 2x12

region in φ and η. A 1x12 region of constant φ is known as a φ strip.

The 1st stage of the current method (fig. 4) is to create 2x3 mini-clusters, when the central cell is larger than neighbouring cells. When a central cell is larger than or equal to neighbouring cells the situation is more complicated (e.g. a jet divided equally between two cells). In this scenario a clustered jet should still be created. The equality statements between cells are set-up so that in particular directions the central cell must be greater than its neighbours, whereas in other directions it must only be greater than or equal to. This ensures that clustered jets are never formed adjacent, including diagonally adjacent, to each other.

The 2nd stage of the process is for the Jet Finder to transfer the 3 largest mini-clusters in each of the two φ strips in opposite φ directions. In practice this can be an inter-FPGA, inter-Leaf or Leaf-to-Leaf connection because the 9 Jet Finders for a given η sign are distributed across 3 Leaf cards. On the Leaf card the 3 Jet Finders are split 2/1 across the 2 FPGAs.

The Jet Finder therefore receives 3 mini-clusters from each φ direction from neighbouring Jet Finders. These are compared against the existing mini-clusters on the receive φ strip. Mini-clusters adjacent or diagonally adjacent to a larger mini-cluster are removed. The equalities are again setup in such a way so that should two mini-clusters have the same value only one will be removed.

In the 3rd and 4th stages the received mini-clusters that survive have their 3 adjacent cells in the receive φ strip added to themselves to make a 3x3 cell. A consequence of this method is that the Jet Finder that initially operates on φ strips n and n-1 produces full clusters centred on φ strips n+1 and n-2.

The current jet clustering method takes advantage of the fact that in a given strip of constant φ, viewed by one RCT crate, in either positive or negative η it is sufficient to consider a maximum of 3 clusters rather than 6. It is this possibility that enables the current method to reduce the data sharing requirement from 66% to 25% of the aggregate input data in the revised GCT design. This allows the Leaf-to-Leaf transfers to operate at 40MHz DDR (80MHz) rather than 160MHz DDR (320MHz). The latter is possible given the LVDS Leaf-to-Leaf connections; however, the timing constraints and thus the design is more difficult.

B. Sort

Sorts must be performed on the Leaf, Wheel and Concentrator. The Wheel card has the most challenging sort. It has up to 54 clustered jets, which must be reduced to 4 with the highest rank. In the Concentrator the sorts must produce the 4 highest ranked objects in order of rank.

The generic sort operates on 16 bit words of which the rank (on which the words are sorted) occupies 6 bits. A diagram of the sort is shown in figure 5. The 1st stage of the sort is the creation of a comparison matrix in which every input is compared against every other input. The matrix is constructed so that two different inputs are only compared once and the result inverted for the other comparison (i.e. $M_{ij} = M_{ji}^{-1}$). This has the benefit of not simply reducing the amount of logic, but more importantly that where two input values have the same value then one is given preference (e.g. if two input values were the same and were both in 2nd place then one value would be placed 2nd and the other 3rd). In the resulting matrix an input value which had the highest rank has a row in the matrix consisting entirely of logic '0's. The next highest ranked object has a row consisting entirely of '0's except for one logic '1' and so on.

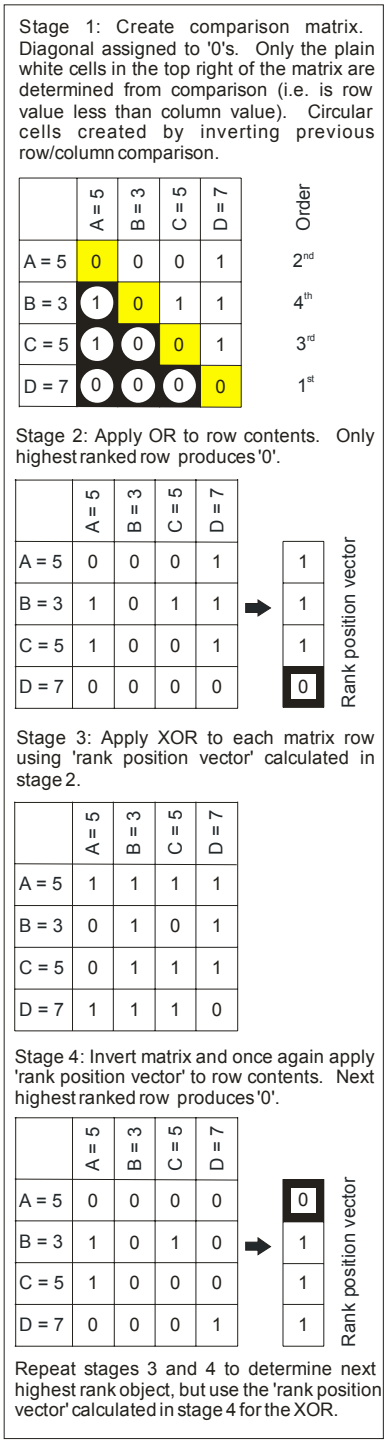

Figure 5: An example of the sort algorithm applied to 4 inputs; however, it is optimised for handling many more inputs.

In the 2nd stage the highest ranked input is found by applying an OR to all values in a matrix row. Only the row with highest rank will produce logic '0'. The result from all rows is stored in a rank position vector.

In the 3rd stage the next highest ranked input is found by applying an XOR between the rank position vector, just calculated, and the rows of the comparison matrix.

In the 4th stage the entire matrix is inverted. Stages 3 and 4 modify the comparison matrix so that the same method can be used to find the next highest ranking object (i.e. An OR is applied to the values in each matrix row. Only the row with highest rank, or now in our case next highest rank, will produce logic '0').

The 3rd and 4th stages are repeated to find next highest rank input, albeit with the latest rank position vector (i.e. that calculated in the 4th stage).

The output stage of the sort (i.e. selection of the highest ranked inputs) is performed by a wide OR rather than multiplexers because this enables the synthesis tool to use the 5 input LUTs rather than the 2 input multiplexers and thus make the combinatorial chain shorter. The maximum so far sorted is 36 to 4 in a Virtex 2 Pro (XC2VP70-7FF1517C) in a single LHC bunch crossing (25ns).

IV. Latency

The latency is 15 bunch crossings, excluding cable delays between the RCT/GCT and GCT/GT, and excluding any contribution from the serialising/deserialising the data over GCT/GT links. The jet data arrive 9 bunch crossing cycles earlier and thus there is more time to process this data

	Jet latency in bunch crossings	Electron latency in bunch crossings
Source Card, including RCT cable	2.5	2.5
Source to Leaf Fibre	(4)*	(4)*
Leaf Deserialise	3	4
Leaf Processing A	3	1
Exchange Leaf Data	3	N/A
Leaf Processing B	2	N/A
Move to Wheel	2	N/A
Wheel Processing	3	N/A
Move to Concentrator	2	2
Concentrator Processing	1	1
Move to Serialiser	0.5	0.5
Total latency	23	11
Allocated latency	24	15

Table 1: The contributions to the latency for both the electron and jet data paths. Note that the "Source to Leaf Fibre" delay is not included because the equivalent delay is excluded in the Trigger TDR [1].

Table 1 shows the various contributions to the latency for the two different trigger paths. Achieving a nominal 15 bunch crossing latency for the Jet processing is difficult despite the data arriving significantly earlier. It should be noted that this table is based on synthesis of key components of the system. The full firmware is not yet complete and the system has yet to be commissioned and thus the latency may change slightly.

The DS92LV16 latency is not included in the table yet it will obviously contribute to the total latency of the final trigger system. The latency from registering the data with the transmit clock to presenting the data with the receive clock is 3 bunch crossings with no allowance for cable delays.

V. Status

Two Source cards have been manufactured and extensively tested. They have passed a successful integration stage with the RCT. A further 8 cards have been produced and are under test.

The Leaf card has already passed preliminary tests and testing of the Multi-Gigabit serial links will commence shortly, followed by Source-Leaf integration.

The Concentrator is in manufacture and is expected to return in mid-October. The Wheel card manufacture will commence after the design aspects that are common between the two cards have been verified.

The core parts of the firmware have already been simulated and synthesised to verify that the latency target can be met. The electron trigger path is scheduled for installation in the first months of 2007, with the jet data path following soon after.

VI. Acknowledgements

We would like to thank the following; Pascal Vulliez (CERN), William Billereau (CERN), Sarah Greenwood (Imperial) and Tom Cote (Los Alamos) for their layout of the designs; PPARC for financial support; Wesley Smith and Sridhara Dasu for their help in understanding the GCT requirements.

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[1] The Trigger and Data Acquisition Project, Vol. I, The Level-1 Trigger, CERN/LHCC 2000-038, CMS TDR 6.1, 15 December 2000.

[2] CMS-IN 04-009, Updated Interface Specification for the CMS Level-1 Regional Calorimeter Trigger to Global Calorimeter Trigger.

[3] CMS-IN 02-069, CMS Level-1 Global Calorimeter Trigger to Global Trigger and Global Muon Trigger Interfaces.

[4] M. Stettler et al., "The CMS Global Calorimeter Trigger Hardware Design", These proceedings.

The Level-1 Global Trigger for the CMS Experiment at LHC

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Abstract

The electronics of the First Level Global Trigger for CMS electronics is described. It is the last stage of the Level-1 trigger system and decides for every LHC bunch crossing whether to reject or to accept a physics event for further evaluation by the High Level Trigger. The Global Trigger receives trigger objects from the Global Calorimeter Trigger and the Global Muon Trigger and applies in parallel up to 128 physics trigger requirements, so-called 'Algorithms'. In addition, up to 64 so-called 'Technical Trigger' signals can be used to either accept or reject events. The Algorithm and Technical Trigger bits are then combined to a Final_OR signal to start the readout procedure of an event.

I. OVERVIEW

The Global Trigger (GT) is the final step of the CMS Level-1 Trigger [1, 2, 3]. It consists of several VME boards mounted in a VME9U crate together with the Global Muon Trigger boards (GMT) and the central Trigger Control System (TCS) [3, 4, 5].

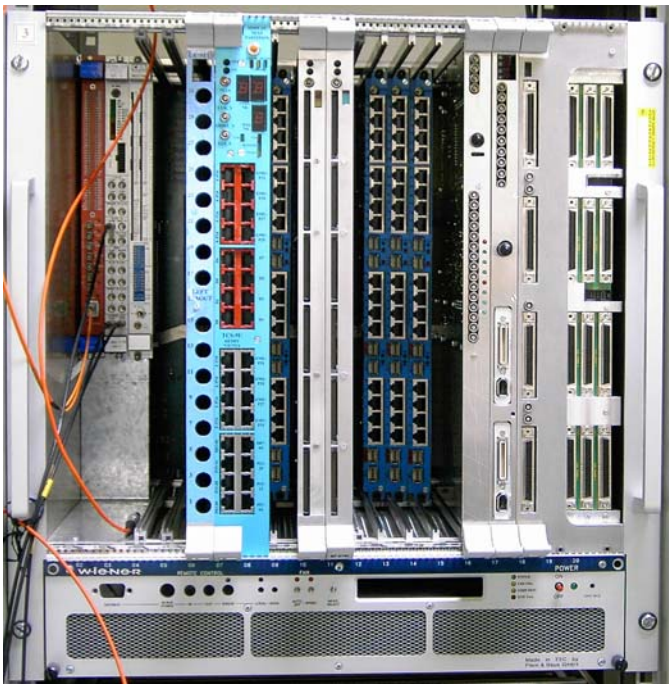

Figure 1 Global Trigger crate with prototype modules

The rightmost 4 VME slots (21-18) contain the GMT boards, slot 17 the GTFE readout board, slot 17 the TIM board, which broadcasts the clock and fast control signals to all boards. In slots 15-13 PSB boards receive trigger data from the Global Calorimeter Trigger. Slot 12 is free and in slot 11 the GTL Logic module calculates up to 128 Algorithms, which are combined to Final_OR signals on the FDL board in slot 10. In slot 9 a PSB board receives 'Technical Trigger' signals and sends them to the FDL board. The Final_OR signals go to the central Trigger Control board (TCS) in slot 8 and are transmitted via 'L1AOUT' modules in slot 6 and 7 to the TTC system of CMS(see also Fig. 1).

For every LHC bunch crossing the GT decides to reject or to accept a physics event for subsequent evaluation by the High Level Trigger. During normal physics data taking the decision is based on trigger objects, which contain information about energy or momentum, location and quality. In addition special trigger signals – so-called Technical Triggers - delivered by the subsystems are also used. The trigger objects are received from the Global Calorimeter Trigger (GCT) and the Global Muon Trigger (GMT). The input data coming from these subsystems are first synchronized to each other and to the LHC orbit and then sent via the crate backplane to the Global Trigger Logic module, where the trigger algorithm calculations are performed. For each quadruplet of "particle-like" input channels (4 μ, 4 non-isolated and 4 isolated e/ γ , 4 central and 4 forward jets, 4 τ -jets) Particle Conditions are applied. A condition for a group of up to 4 particles of the same type may require that E_T or p_T is above a threshold, that the particles are within a selected window in η or in ϕ or that the absolute difference in η or/and ϕ between two particles is within a required range. In addition, so-called 'Delta Conditions' can calculate relations in η and ϕ between two particles of different kinds. Conditions can also be applied to the trigger objects total E_T, missing E_T and H_T, the sum of the transverse energies of the highest-E_T jets. There is also a possibility to trigger on jet multiplicities.

Several Particle and Delta Conditions are then combined by a simple combinatorial logic (AND-OR-NOT) to form Algorithms. Of course, each Particle Condition bit can be used either as a trigger or as a veto condition. Each of the 128 possible algorithms applied during a given data taking period represents a complete physics trigger requirement and is monitored by a rate counter. As a last step, the Algorithms are combined by a final OR function to generate a 'L1_Accept' signal that starts the Data Acquisition System and the Higher Level Trigger software. All Algorithms can be prescaled to limit the overall Level-1 trigger rate. Eight final ORs are provided in parallel to operate sub-systems independently for tests and calibration.

In case of a readout request ('L1A' signal) the Global Trigger is read out like any other subsystem. The L1A signals arrive via the TTC network and are broadcast by the Timing board (TIM) to all other boards, including those of the Global Muon Trigger, where the arrival time of the L1A signal is translated into the corresponding Ring Buffer address. On each board a Readout Processor circuit extracts data from the Ring Buffers, adds format and synchronization words and sends the event record to a readout module, the Global Trigger Front-end board (GTFE). The incoming data are checked there, combined with GMT data to a GMT-GT event record and sent via an S-Link64 interface to the CMS Data Acquisition.

II. SYNCHRONISATION OF INPUT SIGNALS

The Global Calorimeter Trigger (GCT) sends calorimeter trigger objects over fast 1.28 Gbps serial links to three PSB input boards.

A PSB board contains 4 *Infiniband* connectors and 8 DS92LV16 Serializer/Deserializer chips from National Semiconductor to convert the serial data back to 80 MHz, 16 bits wide data streams each carrying data of 2 calorimeter channels that are multiplexed in time. Four calorimeter channels are combined to one 'quadruplet' of 32 bits that means that one Infiniband cable sends data of one 'quadruplet'. A PSB board therefore transmits data of 4 quadruplets to the logic board (GTL) board via the backplane.

As the precise arrival time of the data bits is unknown the SYNC chip on the PSB board first samples the input bits 4 times per 12.5 ns tick to find the switching point of the input data. Normally the sample furthest away from the switching time is selected and transmitted. [2] Then the SYNC chip delays the trigger data for a programmable time and sends the data as 80 MHz GTL+ signals over the backplane to the GTL board.

Phase selection and delay adjustment is done separately for each 16-bit stream to compensate for any time skew between cables and link chips. The SYNC chip also writes the input data into Ring Buffers and, in parallel, into SPY memories. The Ring Buffers keep data for some time until a L1A signal arrives. Then the Readout Processor (=ROP) moves data belonging to the L1A signal from the Ring Buffer into a Derandomizing Memory and transfers them embedded in a formatted record to the GTFE board.

A counter provides the write address for the Ring Buffer and the common BCRES signal resets the counter. The Ring Buffer has been synchronized correctly to the LHC orbit when the first data word of the first bunch crossing is written into the first memory address. The program of the synchronization procedure uses an 8k SPY/SIM memory running in parallel, which accepts the data of a full LHC orbit. It starts the SPY/SIM memory to acquire data of one complete orbit and checks if the data of the first bunch crossing were really written into the first address. If not, the delay for BCRES has to be adjusted accordingly. The BC0-data are flagged by a special sequence in bit 15 of the trigger objects.

During data acquisition a 'private' monitoring program can force the SPY memory to run continuously and to stop in case of an L1A signal to check the history of the input data.

In test mode, software can load the SPY/SIM memory with test data or simulated input data to send them instead of real data.

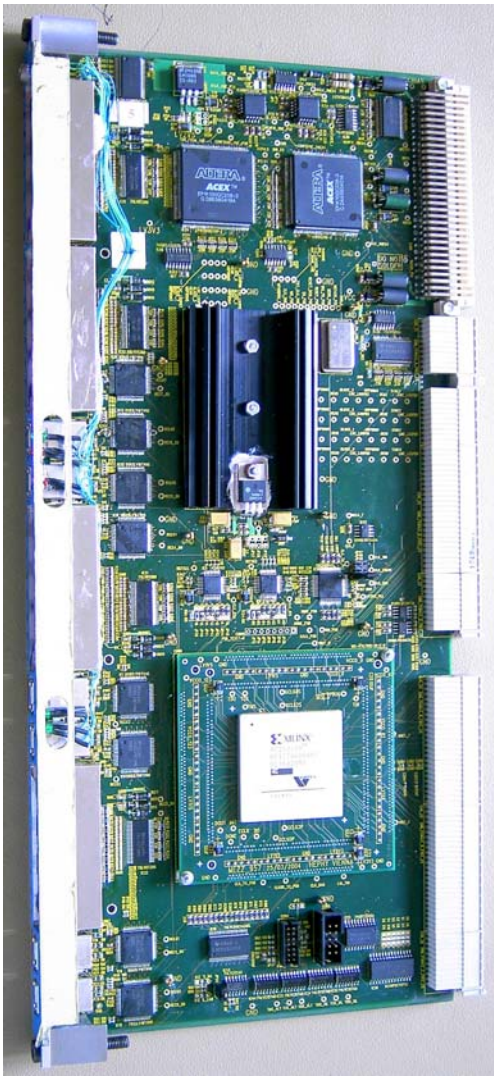

Figure 2 PSB board Version 1

Alternatively to using the two serial receiver chips, a PSB module may accept up to 64 parallel LVDS input signals via RJ45 connectors at 40 MHz frequency. Up to 16 bits are reserved for trigger signals of the TOTEM detector to include it into the CMS data acquisition. The parallel data are sampled 4 times per bunch crossing to synchronize them to the local clock signal. Then they are interlaced into an 80-Mhz data stream and transmitted and monitored instead of one of the quadruplets. The synchronization circuit exists for each group of 4 parallel input bits.

One dedicated PSB module receives Technical trigger bits as parallel LVDS data and sends them directly to the Final_OR circuit in the Final Decision Logic board (FDL).

III. TRIGGER LOGIC

On the 'Global Trigger Logic' board (GTL) the three programmable receiver chips accept the 80-MHz trigger data and distribute them to two Condition Chips (COND). Each Condition chip receives all input data, converts them to 40-MHz objects, applies Trigger Conditions and combines the results to up to 64 Algorithms. The Algorithm bits are sent as parallel signals via short flat cables to the Final Decision Logic board (FDL) located in the adjacent slot.

As each COND chip receives all trigger bits, all kinds of logical relations between the trigger data could be implemented. Only latency requirements and chip resources restrict the number and type of triggers. But resources could be increased by replacing the Stratix chip EP1S40 by EP1S60 from Altera. [8]

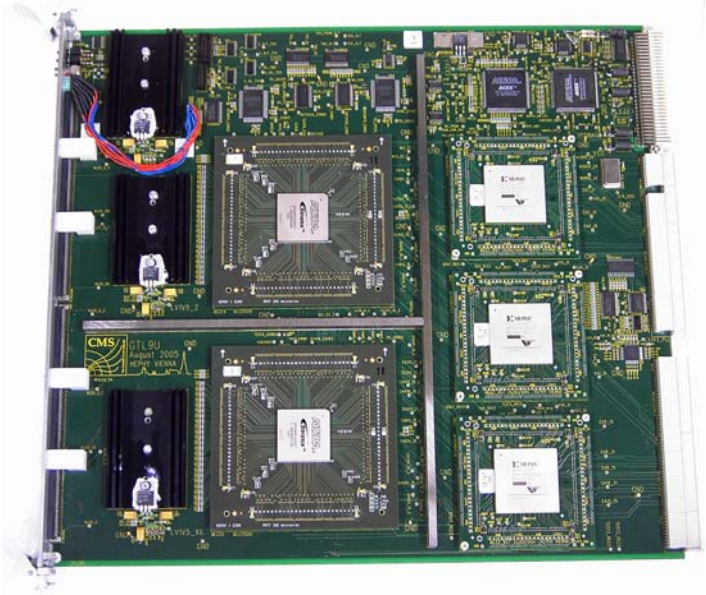

Figure 3 GTL Logic board

A. *Algorithms and Conditions*

To implement the Algorithm logic, small predefined VHDL modules are used to compose more complex trigger requirements. 'Single Particle Templates' and 'Correlation Templates' were defined for 'particle' groups (muons, electron/gamma showers, jets). A **Single Particle Template (*SPT*)** compares p_T or E_T against thresholds and checks if the particle is inside an η and/or ϕ window. For muons the required Isolation-, MIP- and Quality bits are checked in addition, and another p_T threshold can be set for isolated muons. A **Correlation Template (*CT*)** compares the differences $|\Delta\eta|$ and $|\Delta\phi|$ between two particles of the same type against thresholds and checks the charge bits for muons.

To make a '**Condition',** the required SPT is instantiated four times to apply them to all four 'particles' and - if asked for - also the CT is instantiated as illustrated in Fig. 4. Then the results go to a combinatorial logic circuit to find 'n out of 4' particles fulfilling the requirements set by the SPTs and CT. Four Conditions types for each 'particle' group are defined:

1s …to find one particle out of 4

2s …to find two particles out of 4

2wsc …to find two particles out of 4, correlated in η and ϕ

4s …to find four particles out of 4

If three objects are required for a particular algorithm the unused sub-condition is set to trivial values (e.g.: E_T =0 GeV, $0° < \phi < 360°$ etc.).

Conditions for the total transverse energy, the hadron transverse energy, the missing transverse energy and 12 numbers of jets above different thresholds consist only of comparators. As a last step the Condition bits are combined by a simple combinatorial logic to form a trigger **Algorithm**. All Condition bits can be used either as trigger or as veto bits.

To run the trigger Algorithms, the p_T or E_T thresholds of existing Conditions are loaded into registers using VMEbus instructions.

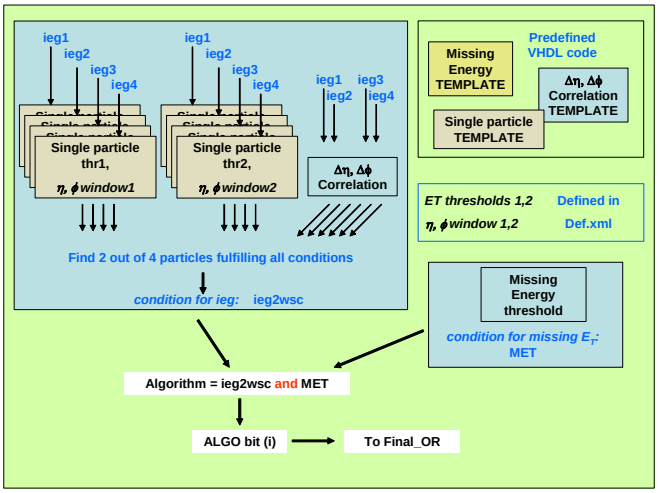

Figure 4 Algorithm composed by Conditions

When designing a new trigger setup first the Algorithms and Conditions are defined with a Java program ("gt_gui ") that runs on all machines. Its output (file "def.xml ") is used by a C++ program ("gts") that generates the variable VHDL files and a file ("vme.xml") that contains addresses and contents for all threshold registers.

A second set of thresholds will be defined for lower luminosity periods. The new VHDL files are merged with the fixed code and used by the "Quartus" software from Altera company to generate a new firmware version. The new firmware must then be loaded to run the new trigger setup. Several firmware versions will be defined to handle data taking as well as calibration and testing periods.

IV. FINAL_OR LOGIC

The 'Final Decision Logic' board (FDL) receives 128 ALGORITHM bits from the GTL board and 64 Technical Trigger bits from a dedicated PSB board. Rate counters monitor each trigger bit and pre-scalers reduce the average rate if required.

The CMS data acquisition system (DAQ) can be divided into 8 DAQ-partitions to test and calibrate parts of the readout and trigger electronics in parallel. Therefore the FDL board combines all or a subset of the Algorithm and Technical trigger bits to 8 Final_OR signals, one for each DAQ-partition, to trigger the DAQ-partitions independently from each other. Mask bits are used to include the Algorithm and Technical Trigger bits into the Final OR gates. For the Technical Trigger bits there exist also veto-mask bits to inhibit Final_OR signals.

The Final_OR signals go to the central trigger control board (TCS) that forwards them - when allowed – as 'Level 1 Accept' (=L1A) signals to the front-end electronics to read the data of the bunch crossing that has generated the trigger signal and also the data of one bunch crossing before and one after.

The FDL board can be read-out like any other front-end electronics module and contains also Ring Buffer memories which store all trigger bits. When an L1A arrives, a Readout

Processor (ROP) copies data of the correct bunch crossing into a Derandomizing Buffer, embeds them into a formatted record and sends the record via a Channel Link interface and the backplane to the Global Trigger readout (GTFE) board.
As on the other boards, so-called SIM/SPY memories allow either to spy all Algorithm-, Technical Trigger- and Final_OR bits or insert simulated bits for tests. In spy mode the SIM/SPY memories run in parallel to the Ring Buffer so that latency and synchronization to the LHC orbit can be checked and adjusted.

V. DATA ACQUISITION

The FDL and the PSB input boards move all trigger input data into Ring Buffers to store them until a L1Accept signal arrives. The Ring Buffers are implemented as dual port memories inside the FPGA chips and accept the data of one full orbit. On the one side a constant write enable signal writes the trigger data of every bunch crossing into the memory. At the end of an orbit the write address returns to the first location, overwriting old data but keeping the history until a L1A signal arrives after the local latency. The local latency is the time between trigger data passing through and the time when the L1A generated by these data returns.
A delayed BCRES signal resets the counter that provides the write address so that data of BC=0 (=BC0 data) are written into location 0. To adjust the BCRES delay correctly, the software can read the SPY memory which runs in parallel to see if the BC0 data were written into the first memory word. On the other side of the Ring Buffer a counter provides the read address which lags behind the write address by the amount of the local latency minus 1 BC, so that a L1A signal reads the correct data words from the BC before until the BC after the event's BC. The L1A signal is extended to 3 BC and is applied as a write-enable signal to the Derandomizing Buffer FIFO, which extracts the data of 3 BC per event. When for debugging purposes 5 BC per event are read, the reset signal for the read counter is delayed by 1 BC less and the L1A signal is extended to 5 BC.
A readout processor (ROP) designed as a state machine reads the FIFO data of one event and wraps them with format words to create event records. The ROP is located either in the same chip or in a ROP chip if the board contains multiple FPGAs.
First the ROP sends a 'read FIFO' command to all FIFOs on the board or in the chip, respectively, to store all data words and their BC-numbers in registers. Then it sends the format words (24-bit event number, board identifier, …) to the Channel Link and fetches one 16-bit word after the other from the FIFO registers to transmit them also to the Channel Link. The ROP sends the next 'read FIFO' command to the FIFOs and repeats this procedure for the next two BC data. Finally the ROP sends an 'End_of Record' to the Channel Link and then switches to an 'IDLE' code to keep the link alive.

A. Readout board (GTFE)

The Global Trigger Readout Board (GTFE = *Global Trigger Front End)* receives event records via the backplane from the boards in the crate. The readout processor chip (ROP_DAQ) receives event records from the GMT, the FDL, the TCS and all PSB boards, checks the incoming format, combines them to a Global Trigger event record and sends it to the SLINK64 mezzanine board [7]. The ROP_EVM chip uses an identical control logic and receives event records from the TCS and FDL boards, adds GPS time - received via a TTCrq mezzanine board - and sends the compiled record via a second SLINK64 to the Event Manager of CMS. Both ROP chips use a Xilinx XC2V2000 FPGA that is mounted on a mezzanine board. [9]

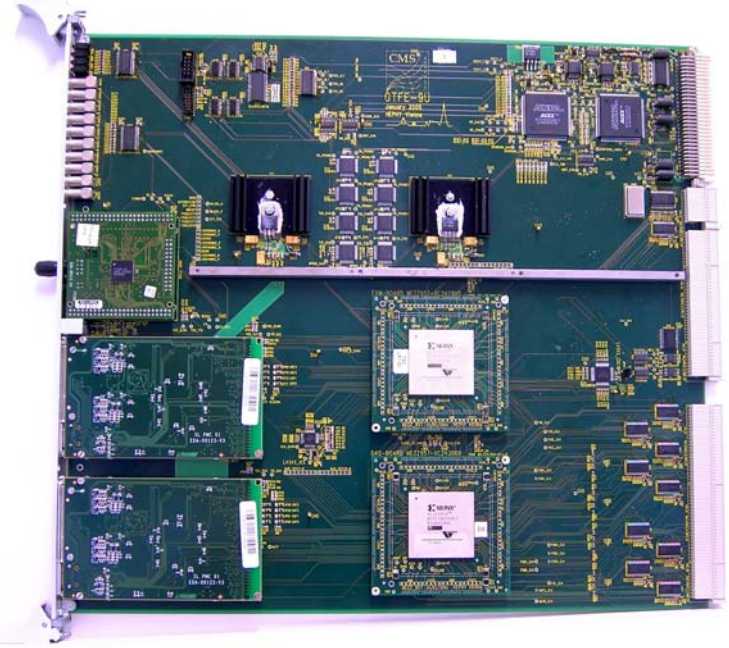

Figure 5 GTFE readout board

The GMT and the GT boards use 28-bit Channel Links to send the readout records to the GTFE board. The Channel Link bits 15-0 carry trigger data going into the data FIFOs, bits 23-16 could carry private monitoring data going into separate Monitoring memories, and bits 27-24 carry control bits going to the control logic that detects the begin and end of records. As long as IDLE data arrive the FIFOs remain inactive. The FIFOs are configured so that the output width is 4 times the input width, reordering the trigger data into 64-bit words for the SLINK64 and thus replacing a 4-to-1 multiplexer. A synchronous reset input enables the common L1Reset signal to erase all events in the FIFOs. All FIFOs can keep more than 20 events, are written with 40 MHz and are read with an 80 MHz clock. When the FIFOs become 75% full, a 'Warning' flag is sent to the Trigger Control board to reduce the trigger rate. The capacity of the FIFOs could be doubled by replacing the Xilinx XC2V2000 by a XC2V3000 chip. [9]
Both GTFE chips receive also the common signals L1A, BCRES and Event Counter Reset and create for each event a local Event and BC-number used as reference.
The Crate Readout Processor (Crate-ROP) is implemented as a state machine that reads the FIFOs of all active boards. When the first active FIFO has received an 'end-of-record' flag, the ROP applies the standard HEADER word to the SLINK64 and reads all the data of one event on a board, then switches to the next active board FIFO and continues until the last connected board.
A comparator circuit checks if the number of events in each channel since the last 'Event Number Reset' signal agrees with the reference number. Any difference is flagged as error

bit in the EVENT_STATUS byte. Nevertheless the event transmission continues until the end. Such errors will show up until the synchronization of all boards has been done correctly.

Finally, the Crate ROP appends as the last word the Event Status, the updated CRC number and the Event length. During the transmission the CRC and Event status are updated but the Event length is preloaded via VME because it is constant and depends on the number of bunch crossings per event and the boards which contribute data.

The Crate-ROP transmits data as long as there are records in the FIFOs and as long as the SLINK64 is ready. When the SLINK64 returns a 'full' flag, the Crate-ROP simply waits until the SLINK64 becomes ready again. When the off-time is too long the board FIFOs will be filled. When the 75% level is reached, the Crate-ROP sends a 'Warning' flag to the central trigger control system to reduce the trigger rate. When running with an 80-MHz clock, the Crate-ROP transfers a normal GT/GMT event (200 64-bit words) within 2.5 μs. Even when running only with a 40 MHz clock the event is transferred within 5.0 μs, thus still exceeding the required 100-kHz event rate.

When the SLINK64 for the Event Manager goes into status 'not ready', the corresponding status signal is sent directly to the TCS board to stop all DAQ-partitions.

In both ROP chips a dual port memory spies all event data which are sent to the SLINK64. The SPY memory can also be used to insert test data instead of readout data to test the reliability of the SLINK64. The other side of the SPY memory is accessed by VME-software.

VI. SUMMARY

The Global Trigger boards have been built, and all except the GTFE readout board are being integrated into CMS. Four of the PSB boards have been tested and production of the others has started. The complete trigger chain has been tested with cosmic muon data and the Global Trigger is functioning according to specification.

VII. LIST OF ACRONYMS

BC bunch crossing
BCRES common bunch crossing counter reset signal
DAQ data acquisition system
Event Manager: controls data flow of events in DAQ
FIFO First-In/First-Out memory
GCT Global Calorimeter Trigger of CMS
GMT Global Muon Trigger of CMS, mounted in GT-crate
GTL+ Gunning Transceiver Logic Plus : JEDEC JESD 8-3
L1A trigger signal to read all Front End buffers of CMS
LVDS Low Voltage Differential Signals
Quartus Altera company's Software to design and implement firmware
S-LINK64 Fast data Link extended to 64 bits (see references)
RJ45 Connector type, used by Ethernet
TOTEM Experiment measuring Total Cross Section, Elastic Scattering and Diffraction Dissociation at the LHC
VHDL VHSIC Hardware Description Language
VHSIC Very High Speed Integrated Circuit

VIII. ACKNOWLEDGEMENTS

The authors would like to thank R. Eitelberger and R. Stark for designing and machining all mechanical parts of the Global Trigger electronics. We also thank Wesley Smith from the University of Wisconsin and Joao Varela from IST, Lisbon for many helpful discussions and Fritz Szoncso (now Cern) for starting this project.

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Wafer test of the LHCb Outer Tracker TDC-chip

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Abstract

The OTIS-TDC is the front end readout chip for the LHCb Outer Tracker. It is designed to measure drift times with a resolution better than 1 ns. As the chip will be directly mounted to its board, the test have to be performed on the wafer itself. As the testing period for 7 000 chips was only three weeks, many test routines have been implemented on a FPGA. Each chip is subjected to detailed probe testing to ensure the full functionality as well as a good performance.

Overall 47 wafer have been tested. From the chips passing the test 2 000 have been used in the Outer Tracker front end electronic.

I. INTRODUCTION

The LHCb Outer Tracker is a straw tube detector. In order to measure the drift times of the electrons in the straws, the OTIS chip was designed. A detailed description can be found in [1]. It is a 32 channel time to digital converter (TDC) chip and was developed at the ASIC laboratory at the Heidelberg University It is implemented in a 0,25 μm commercial CMOS process using radiation hard layout techniques. The chip can be divided into four major components:

- The TDC core
- The control algorithm
- The pipeline memory and derandomising buffer
- The I^2C slow control

The TDC core performs the drift time measurement, performed by a 64 stage delay lock loop (DLL). Therefore the clock cycle is divided into pieces of 390ps length at the LHCb frequency (40MHz). If a channel is hit, the logic latches the clock position in the DLL into the corresponding 6 bit channel hit register. At each clock cycle this information is passed on to the pipeline register along with further status informations.

The control algorithm prepares the data for read out. Two read out schemes are implemented. In the first mode (encoded hitmask) the logic searches for the first hit in each channel. Up to 3 bunch crossings (BX) are looked at. A second hit within the 3 BX is not transferred to the memory in this mode. The second mode (plain hitmask) provides a multi hit capability. It first encodes, in which channel and BX a hit occurred. This hitmask is followed by the pure 6 bit drift time informations. Therefore several consecutive hits on the same wire can be read out with one trigger.

The pipeline memory is build with dual ported SRAM cells with a dimension of 164x240 bit. Organized as a ring buffer, each line is stored for 4s (164x25ns) in the memory awaiting the L0 trigger decision. After this time the information is overwritten by a new data set. Up to three lines are copied into the derandomising buffer on a positive L0 decision. The buffer compensates for trigger rate fluctuations that may occur.

A schematic overview of the OTIS-TDC chip can be seen in figure 1.

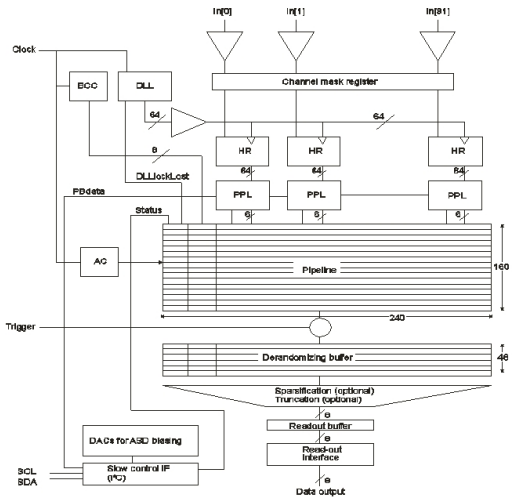

Figure 1: A schematic overview of the OTIS-TDC chip

The chip was produced as part of the multi project wafer run 15 by CERN. The wafer contained two versions of the OTIS-TDC, namely 1.2 and 1.3. The difference between these versions are very minor modification which promised a better performance in extreme conditions. For this wafer test these variations can be neglected and therefore the two versions are treated in the same way. The wafers were delivered in one lot of 47 wafers, each containing 71 Otis chips of each version. The lot was received on November 15th 2005. Due to the other projects the wafers had to be send back on December 5th.

The chips were identified by the wafer name and location on the wafer. The test results were stored into log-files and summarized in a wafer map. Only chips passing all tests are used for the Outer Tracker front end electronic.

II. THE WAFER TEST

The test should verify the digital functionality of the chip and study its performance. The test setup is divided into three parts. The first part is the semi-automatic probe station. The probe station is controlled by a PC running a vendor specific software. This software can receive commands from other computers and provides status information.

These commands are given by the master PC of the test

setup. This PC orchestrates the complete test procedure. It is running a LabView application to control the test flow. It also performs measurements of analogue voltages, monitors the power consumption and provides a test of the slow control.

The final part of the test setup is the slave PC. It is also running a LabView application which communicates with a FPGA card via the PCI-bus. The FPGA card contains an ALTERA Stratix S25 chip which is also the DAQ of the real experiment. The FPGA is needed to get a reliable and fast DAQ in the test. It also provides all fast control signals such as clock and resets. Figure 2 shows an overview of the test setup.

The complete test procedure consists of ten steps:

1. Access next chip and make contact
2. Switch on power of the needle card
3. Measure power consumption
4. Program and verify the register on the chip
5. Start the FPGA measurement
   (a) Check header bits and data integrity
   (b) Check all 32 data channel
   (c) Time measurement on 4 channel
   (d) provoke an error condition
6. Program and verify the register on the chip with a second setting
7. Set and measure DAC values of the chip
8. If one of the steps 3) to 7) fail, repeat them with a separation of the needle card and chip performed
9. Switch off power
10. Separate needle card and chip and go to 1)

The repetition of test steps in case of an error was due to the imperfections of the probe stations. As its chuck and therefore wafer was not completely flat with respect to the needle card, the contact quality to the chip pads changes. A short separation of the needle card and the wafer solves this contact problem.

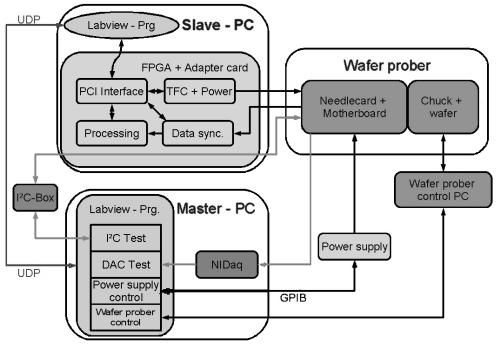

Figure 2: A schematic overview of the test setup

A. Tests by the master PC

Apart from steering the test flow, the master PC also performs some of the infrastructure tests. The first check includes the power consumption. It verifies, that there are no short circuits on the chip. If too much current is drawn, the chip is marked faulty by power consumption.

The second test concerns the slow control. It writes a chequer pattern into the I^2C register. The register values are read back and compared to the initial ones. Any failure is marked as a digital error. The read only register are compared to the expected value. After the FPGA test is performed, this test is repeated with a second pattern on another I^2C address. This should exclude any stuck bits in the slow control register part of the chip.

The third test done by the master PC is the measurement of the analogue voltages. In order to produce the threshold voltages for amplifier chip, the Otis contains a DAC to provide four voltages. These voltages can range from 0 to 2,5 mV and can be set via $I2C$ register. The test sets now these 8 bit register with values of 0,1,2,4,8,16,31,64,128 and 255. The measured voltage has to be in range of 50 mV from the expected value. Also the difference of all four DAC values have to be in the same range compared to each other. An error in this test is marked as a threshold voltage error.

B. Tests by the slave PC

The tests done by the slave PC concerns the data received from the Otis chip. In order to handle the high data rate all the test function are implemented on a FPGA chip. The Stratix FPGA chip was chosen due to the fact that the same chip type is also used in the buffer boards of the LHCb experiment.

FPGA firmware

The firmware of the can be divided into four parts:

- Infrastructure
- DAQ
- Analysing functions
- PCI interface

In order to get the Otis chip working, a infrastructure, namely the fast control signals have to be provided. These signals contain the clock signal, the trigger signal and all reset signals such as L0 reset and event count reset. In order to get a time measurement, a pulser was also implemented. It is based on the PCI clock signal and therefore it is completely independent of the LHCb clock signal. This ensures a kind of random hit signal.

The DAQ part searches for the OTIS data in the data stream. It tries to synchronize using the data valid signal as well as the comma word. A successful synchronization is a check of the data quality in itself. The data found in the data stream are then prepared for the histogram unit. The raw data is also written into a Fifo for debugging propose.

With the histogram unit errors in the header bits are counted. It also builds a histogram of the event IDs as a check of the data quality. It counts the hits in each of the 32 channel and makes a detailed time histogram for one channel.

All these parts are read out and controlled by the PCI interface. An overview is shown in figure 3

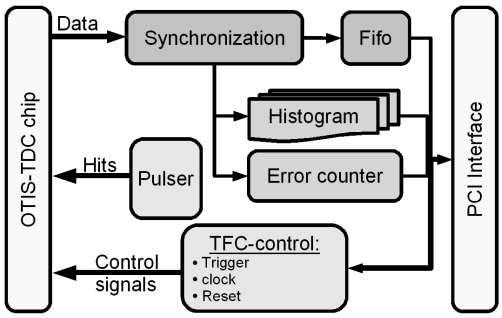

Figure 3: A schematic overview of the FPGA firmware

FPGA tests

Four tests are performed by the FPGA. The first test is a general look at the data integrity. All the header bits are compared to an expected value and errors are counted. It is also checked, if the number of event matches the number of triggers. Any error in this test is marked as a digital error.

The second test checks all the channels. This is done by pulsing first the even channel and requesting 10 000 data sets. It is then looked, if each even channel have measured 10 000 hits. All the odd channel are expected to have seen only view hits. In a second round the odd channel are pulsed. Any channel which does not receive 10 000 hits in its round is marked as dead channel.

The third test performs a time measurement on the four most critical channels. This is done by calculating the differential non-linearity (DNL) for each channel.

$$DNL(i) = \frac{Hits(i) - Hits(i-1)}{expected\ Hits(i)}$$

$$i = channel\ number$$

$$Hits(i) = hits\ seen\ in\ channel\ i$$

The DNL is a indication on the size of each time bin. The DNL for the complete chip is then calculated by adding the absolute values of the minimum and maximum of the DNL(i).

In the actual test a ”random hit” signal is send. In an perfect chip this would result in a DNL of zero. As this can not be achieved by the OTIS chip due to the design the limit was set to two time bins (780 ps). All chips with greater DNL are marked an error in the time measurement.

The final test provokes an error condition and checks the reaction of the chip. On a failure in one of the test steps results in one repetition of all the test steps. An error is only marked if the failure occurred in the repetion as well.

III. Test results

Overall 7332 chips have been tested. The yield obtained was 91,5% for the version 1.3 chip and 88,7% for version 1.2 . From the over 6000 chips passing the test, the LHCb OT will use around 2000.

The distribution of errors is given in table 1. Figure 4 shows the yield of each wafer.

Table 1: Distribution of errors

Error	OTIS 1.2	OTIS 1.3
Time measurement	1,8%	1,9%
Threshold voltage	2,4%	0,8%
Dead channel	7,6%	4,5%
Digital	10,0%	7,2%
Power consumption	3,0%	1,3%

IV. Acknowledgment

We would like to than the Heidelberg ASIC Laboratory Team for supporting this work.

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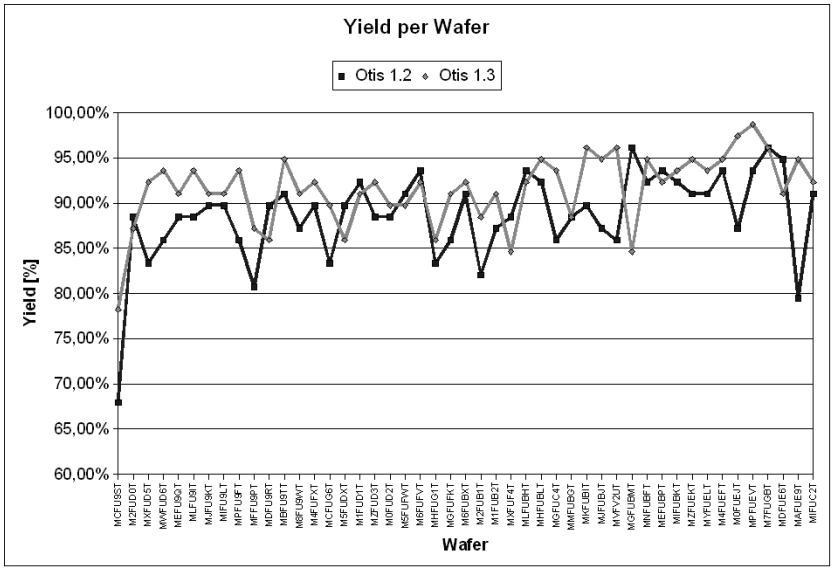

Figure 4: A figure caption

The Gigabit Optical Transmitters for the LHCb Calorimeters

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Abstract

This report presents the boards developed for the optical data transmission of the calorimeter system of the LHCb experiment and test results.

We developed two types of transmission boards: the single-channel and the multi-channel ones. Multi-channel boards can be equipped with a variable number of transmitters, depending on the need, with a maximum allowed of 12 channels. Each optical channel allows transmitting 32 bit data at 40.08 MHz.

The boards have been designed and built using radiation hard devices produced at CERN.

The optical links have been qualified using the eye diagram and the BERT at 1.6Gbps.

I. INTRODUCTION

The report describes the optical links developed for the data transmission of the LHCb calorimeter system. They are used to establish high speed (1.6Gbps) connections over long distances of about 100 m among the front-end electronics cards of the calorimeter system, the L0 trigger system and the DAQ boards.

The optical transmitters are built as mezzanines boards, i.e. as cards to be plugged to carrier-boards (to the CROC calorimeter boards, to the SPD control boards and to the validation cards). They get power, control signals and reference clock from the underlying carrier-boards. To plug the mezzanines boards to the carrier-boards we plan to use the high-speed connectors by Samtec.

To transmit 32 bits patterns at 40.08MHz through the optical fibers we use the GOL chip [2] (Gigabit Optical Link), radiation hard, produced by the CERN Microelectronic Group. The data transfer rate, running the transmitter at 40.08MHz, including header and parity bits, using the 8B/10B encoding mode, is of about 1.6 GHz per link.

The reference clock will be generated by the carrier-board and distributed to the GOL chips from a clock distributor. The jitter introduced by these devices is guaranteed to be less than 2ps RMS.

As optical transducer in the single-channel transmitter boards we use the VCSEL [3] (Vertical Cavity Surface Emitting Laser) laser diode (1mW at 6mA) by ULM Photonics. It operates on multimode optical fibers at a wavelength of 850nm and is equipped with SMA type fibre connector.

In the multi-channel boards we use a parallel transmitter made by Agilent. The optical transducer is the SNAP12 standard compliant, equipped with the MPO/MTP ribbon fibre connector interface. It operates on multimode optical fibre at a wavelength of 850 nm.

The start up of the GOL is managed by means of the CRT4T power switches.

Special care has been spent in projecting the PCBs and in placing the bypass capacitors, in order to minimize the noise level and the bit error rate.

The report will describe the test performed on the prototypes to fully qualify the optical link. The link has been qualified using the eye diagram and the BERT. The results show that the BER is better than 10^{-13} as expected.

II. MEZZANINE SINGLE-CHANNEL

The block diagrams of the mezzanine boards are shown in the following figures.

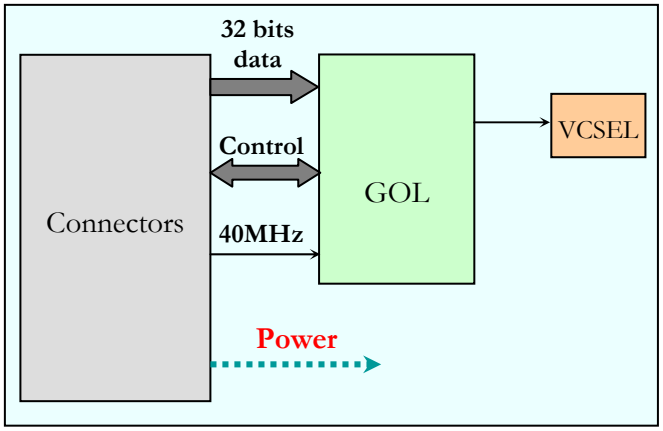

Figure 1: Block diagram of the single-channel mezzanine

In order to plug the single-channel mezzanine board to the carrier-board we plan to use the high-speed connectors by SAMTEC 0.635 mm Hi-Speed Header [5], two connectors, QTS-025-01-L-D-A, located in the bottom layer of the mezzanine board.

The height of the connectors determines the distance between the mezzanine and the carrier-board. The distance in this case is of 5 mm.

To transmit 32 bits patterns at 40.08MHz through the optical fibers we will use the GOL chip (Gigabit Optical Link), produced by the CERN Microelectronic Group. The data transfer rate, running the transmitter at 40.08 MHz, including header and parity bits, using the 8B/10B encoding mode, is of about 1.6 GHz per link.

Optical transducer of the single-channel mezzanine boards we plan to use the VCSEL (Vertical Cavity Surface Emitting Laser) laser diode ULM850-05-TN-USMBOP (1mW at 6mA and 3.3 V anode biasing), made by the ULM Photonics. The VCSEL laser diode will operate on multimode optical fibers at a wavelength of 850nm. It will be equipped with the SMA type fiber connector.



Figure 2: Picture of single-channel mezzanine

III. MEZZANINE MULTI-CHANNEL

The block diagrams of the mezzanine boards are shown in the following figures.

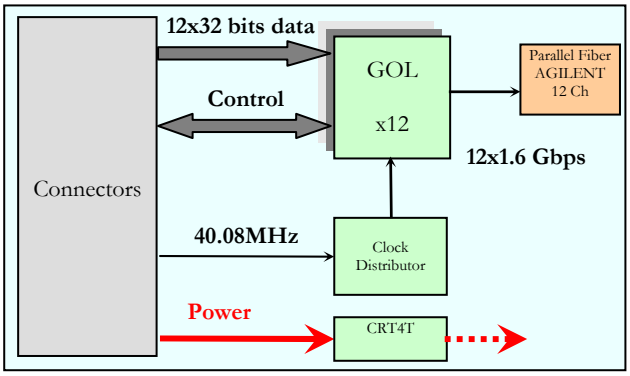

Figure 3: Block diagram of the multi-channel mezzanine

To plug the multi-channel mezzanine board to the carrier-boards we plan to use the high-speed connectors by SAMTEC 0.635 mm Hi-Speed Header, two connectors, QTS-125-03-L-D-A, located in the bottom layer of the mezzanine board.

The distance between the multi-channel mezzanine and the carrier-board in this case is 11 mm.

To transmit 32 bits patterns at 40MHz through the optical fibers we will use the GOL chip (Gigabit Optical Link).

The reference clock will be generated by the carrier-board and distributed to the GOL chips through the connectors without any clock filter. In order to distribute the clock to the GOL chips in the multi-channel case we will use a clock distributor. As a clock distributor we plan to use a 1:20 differential PECL clock driver, made by On Semiconductor, model type NB100LVEP221FA. The jitter introduced by this device is guaranteed to be less than 2ps RMS.

The quality of the clock used to drive the GOL is a critical parameter.

The GOL maximum tolerable jitter value is 100 ps (peak-to-peak).

The clock signal from the LHC TTC (Timing Trigger and Control) system to the GOL is distributed to the Optical Transmitter board from the Carrier Board through the connector clock pin and then distributed by the NB100LVEP221FA.

The quality of the clock measured at the GOL clock pin after having passed through the entire distribution chain shows rather a good σ value of about 7 ps.

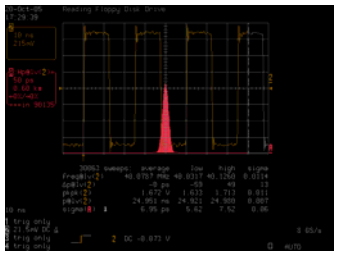

Figure 4: The quality of the jitter at the pin clock of the GOL improves σ = 6.95 ps

As optical transducers of the multi-channel mezzanine boards we will use a parallel fibre optical link transmitter, made by Agilent. The optical transducer model type is the HFBR 772BH [4], SNAP12 standard compliant. It will be equipped with the MPO/MTP ribbon fibre connector interface. It will operate on multimode optical fibre at a wavelength of 850 nm.

To implement the GOL power switch, two PMOS devices are used in parallel in order to reduce the "on" resistance of the switch (this reduces the voltage drop across the switch). An NMOS device is additionally used to short the GOL power to ground when the power switch is open. This device guarantees that the GOL power supply rail is pulled to ground even in the presence of active inputs [2].

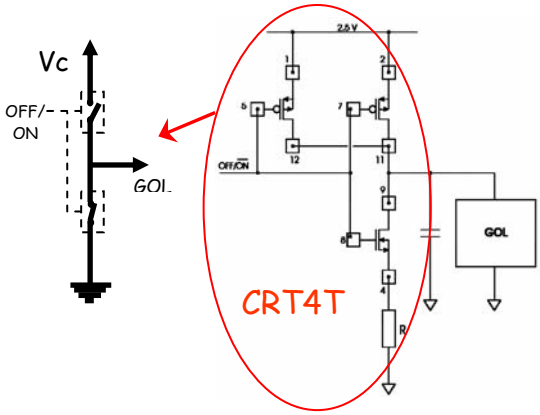

Figure 5: Using the CRT4T as a power supply switch for the GOL

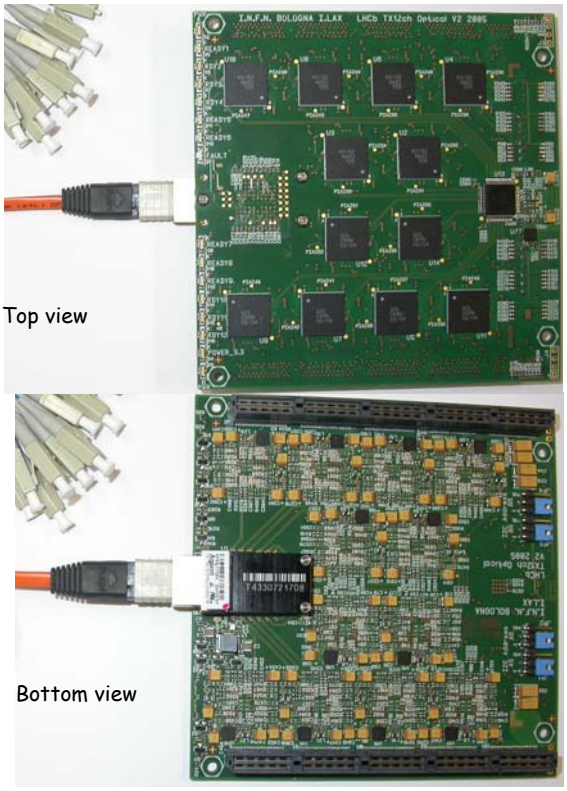

Figure 6: Picture of multi-channel mezzanine

IV. MEASUREMENTS

To qualify the optical transmitters [7] we have tested the main functionalities of the boards: synchronization capabilities of each optical channels, level of the bit error rate while operating in normal conditions, reset capabilities in case of error; we evaluated the effects of the optical pulse attenuation on the quality of the transmission channel by measuring the corresponding bit error rate in data transmission. We also studied the electrical behaviour of the mezzanine boards in a range from ambient to maximum operating temperature.

The setup used for testing purposes is shown in the block diagram.

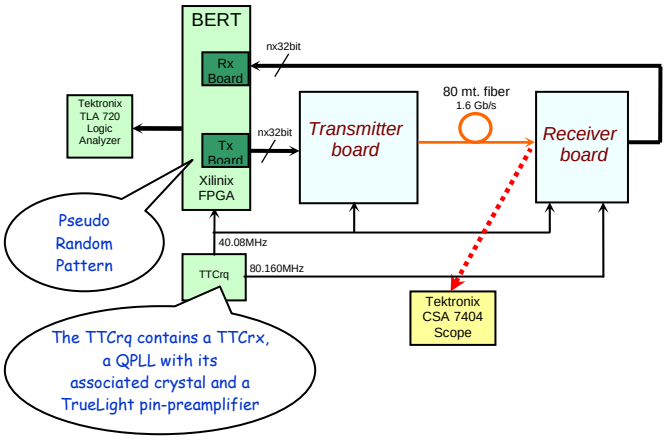

Figure 7: Comparison between transmitted and received patterns

$$BER = \frac{bits\_received\_in\_error}{total\_bits\_received}$$

Table 1: BER vs. Time

BER	n(bits)	Time
10^{-12}	$2.3 \cdot 10^{12}$	30 min
10^{-13}	$2.3 \cdot 10^{13}$	5 h
10^{-14}	$2.3 \cdot 10^{14}$	50 h

To reach a sensitivity of 10^{-12} in measuring the transmission error probability with this technique, when no error is detected during the entire data transmission, aiming a confidence level of 90%, lasts about 30 minutes.

The "Q" value has been measured with the digital scope embedded software (see figure 8), specifically developed by Tektronix for eye-diagram analysis.

An approximation of the effective Bit Error Rate (BER) can be obtained as follows:

$$BER = \frac{1}{2} erfc\left(\frac{\sqrt{SNR}}{\sqrt{2}}\right) \approx \frac{e^{\frac{-Q^2}{2}}}{\sqrt{(2 \cdot \pi)} \cdot Q}$$

This formula returns estimated values better than 10^{-13}.

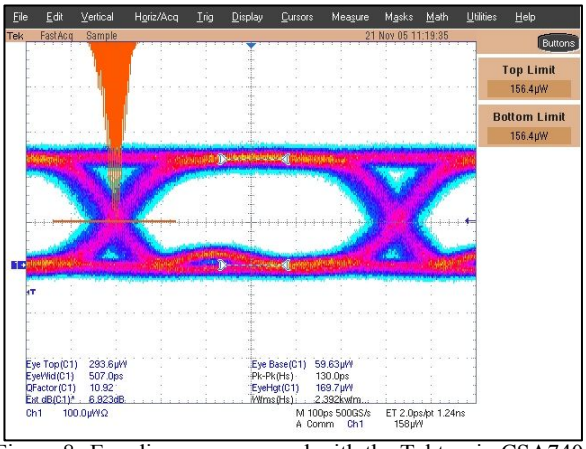

Figure 8: Eye diagram measured with the Tektronix CSA7404 digital scope

Attenuation of the light pulses has been varied to establish the range within the transmission is errors free. Data shall go through 100m long cables and two optical patch panels.

Table 2: BER vs. Optical Attenuation

Attenuation (dB)	Eye Top (µW)	Time (hours)	Errors (C.L.95 %)
0	462,8	24	$<10^{-13}$
3	232	24	$<10^{-13}$
6	114,5	120	$<10^{-14}$
9	57,6	24	$<10^{-13}$
12	27,34	24	$<10^{-13}$
14	18,29	24	Errors Observed

The optical attenuator used in our test is the Amphenol AFO 46946. it is an adjustable attenuator without pre-definite steps. The attenuation level can be varied by rotating a milled ring.



Figure 9: Optical Attenuator, Amphenol AFO 46946

V. Conclusion

The power consumption of the single-channel mezzanine is of about 150mA at 2.5V while is of about 8.9mA at 3.3V.

The power consumption of the multi-channel mezzanine has been measured to be of 150mA per channel at 2.5V and 1.07A at 3.3V due to the laser and to the clock distributor power consumptions.

We heated the boards up to 60ºC to test their behaviour. We didn't observe any transmission problems on runs lasting several hours.

The I2C bus and the JTAG bus of the mezzanine has been connected to Credit Card PC through the LHCb Glue-Card bus converter named the Glue Card. Thanks to a dedicated control program, running on the Credit Card PC, one can set and control the status of each GOL of the boards.

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Low-noise Design Issues for Analog Front-end Electronics in 130 nm and 90 nm CMOS Technologies

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Abstract

Deep sub-micron CMOS technologies provide well-established solutions to the implementation of low-noise front-end electronics in various detector applications. The IC designers' effort is presently shifting to 130 nm CMOS technologies, or even to the next technology node, to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. In this work the results of noise measurements carried out on CMOS devices in 130 nm and 90 nm commercial processes are presented. The behavior of the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width. The study is focused on low current density applications where devices are biased in weak or moderate inversion. Data obtained from the measurements provide a powerful tool to establish design criteria in nanoscale CMOS processes for detector front-ends in LHC upgrades.

I. Introduction

Deep sub-micron CMOS technology has met the challenging design requirements for front-end electronics in various High Energy Physics (HEP) detector applications. For instance, CMOS commercial technologies of the quarter micron node have been extensively used for the implementation of radiation tolerant, low noise, low power readout circuits with very high channel density for analog and digital processing in pixel and microstrip detectors at the Large Hadron Collider (LHC) experiments under construction at CERN [1-4]. The increased luminosity and track densities expected in the experiments at the next generation colliders (LHC upgrades, International Linear Collider, Super B-Factory) set the demand for moving to more scaled CMOS technologies [5-7]. Nowadays, CMOS processes with 130 nm minimum feature size are widely available for Application Specific Integrated Circuits (ASICs) design, and 90 nm processes are coming on-line as the next industrial generation; therefore, the IC designers' effort is presently shifting to these technology nodes to implement readout integrated circuits for silicon strip and pixel detectors, in view of future HEP applications. At nanoscale geometries, below 100 nm feature sizes, modeling the behavior of the analog parameters of these devices is a tricky problem, since some effects which can deeply affect short channel MOSFET performance, become more difficult to foresee. This work presents the results relevant to the noise characterization of single CMOS devices belonging to two commercial CMOS processes with minimum feature size of 130 nm and 90 nm manufactured by STMicroelectronics. The devices were characterized at drain currents from several tens of μA to 1 mA, that is, the usual operating currents of input devices in integrated charge-sensitive amplifiers. In these conditions, deep sub-micron devices are biased in weak or moderate inversion. The behavior of the main noise parameters modelling the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width to account for different detector requirements. The wide set of measurements provides a powerful tool to establish design criteria in 130 nm and 90 nm CMOS processes. The analysis of the experimental results also includes the comparison of noise parameters obtained from the two technology generations. This is expected to provide useful hints for the choice of the proper CMOS node to be used for detector front-end electronics in view of future applications in the field of HEP electronic instrumentation such as LHC upgrades.

II. Experimental Details

A. Investigated Devices

The MOSFETs studied in this paper belong to two commercial CMOS processes with 130 nm and 90 nm minimum feature size manufactured by STMicroelectronics. The maximum allowed supply voltage V_{DD} is +1.2 V for devices in the 130 nm process and +1.0 V for devices in the 90 nm process. The physical thickness of the gate oxide t_{OX} is 2.0 nm, and 1.6 nm respectively; for devices in inversion the electrical gate oxide thickness can be estimated to be 2.4 nm and 2.0 nm [8], therefore, the corresponding effective gate capacitance per unit area C_{OX}, is about 15 fF/μm^2 and 18 fF/μm^2. In the 130 nm process PMOS and NMOS devices with gate length L of 0.13, 0.2, 0.35, 0.5, 0.7 and 1 μm, and gate width W of 200, 600 and 1000 μm were investigated. In the 90 nm process we studied devices of both polarities with gate length of 0.1, 0.13, 0.2, 0.35, 0.5 and 0.7 μm, and gate width of 200 and 600 μm. Devices with such a large W are commonly used as front-end elements in readout systems for particle detectors, in order to achieve the best noise performances [9]. In both processes all NMOS devices were laid out using a standard open structure, interdigitated configuration.

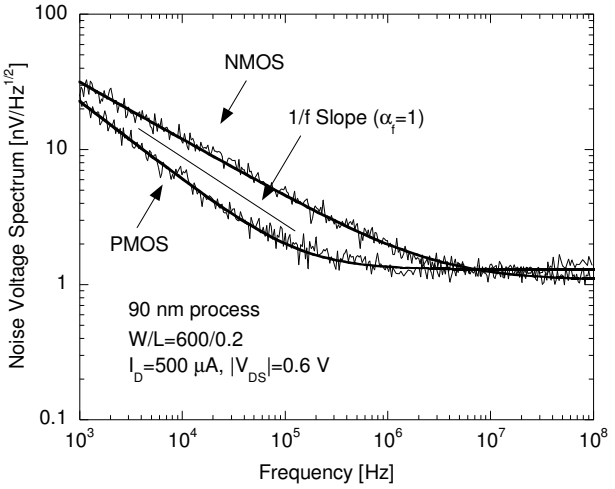

Figure 1: Gate referred noise voltage spectra for NMOS and PMOS devices with *W/L*=600/0.2 belonging to the 90 nm process (I_D=500 µA, $|V_{DS}|$=0.6 V).

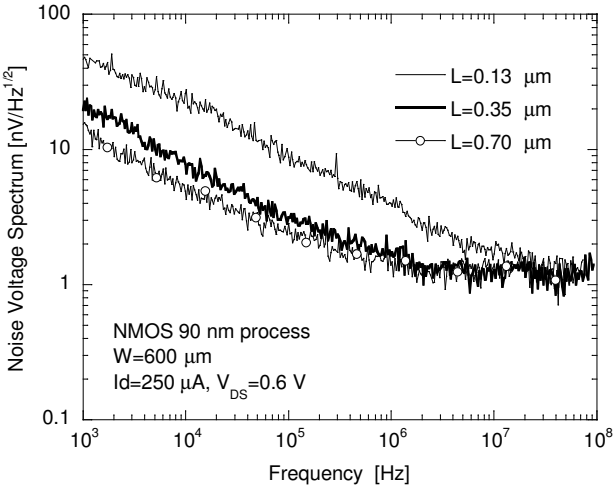

Figure 2: Noise voltage spectra of NMOS with gate width *W*=600 µm and different gate length *L* belonging to the 90 nm process (I_D=250 µA, V_{DS}=0.6 V).

B. Measurement setup

Measurements of static and signal parameters were carried out with an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules. The spectral density of the noise in the channel current of the examined devices was measured using instrumentation purposely developed at the Electronic Instrumentation Laboratory, University of Pavia. The noise of the DUT is amplified by a wideband interface circuit and detected by a Network/Spectrum Analyzer HP4195A [10]. This system allows for noise measurements in the 100 Hz–100 MHz range.

III. NOISE MODEL AND PARAMETERS

In a MOSFET, the noise in the channel current can be expressed by an equivalent noise voltage generator referred to the gate of the device. A rather general expression for the power spectral density of the voltage noise is expressed by means of equation (1) where the first term is determined by channel thermal noise and noise contributions from parasitic source/drain, gate and bulk resistors while the second term is given by 1/f noise in the channel current [11].

$$S_e^2(f) = S_W^2 + S_{1/f}^2(f) \tag{1}$$

In the low current density operating region, the white noise voltage spectrum S_w^2 is dominated by channel thermal noise and can be expressed by means of its equivalent noise resistance:

$$R_{eq} = \frac{S_W^2}{4k_BT} = \alpha_W \frac{n\gamma}{g_m} \tag{2}$$

were k_B is the Boltzmann's constant, T is the absolute temperature, g_m is the device transconductance, n is a coefficient proportional to the inverse of the subthreshold slope of I_D as a function of V_{GS}, γ is a coefficient ranging from 1/2 in weak inversion to 2/3 in strong inversion and $\alpha_W \geq 1$ is an excess noise factor [12]. The 1/f noise in the channel current can be modeled by the relationship:

$$S_{1/f}^2(f) = \frac{K_f}{C_i}\frac{1}{f^{\alpha_f}}. \tag{3}$$

K_f is an intrinsic process parameter for 1/f noise and $C_i=C_{OX}WL$ is the gate oxide capacitance, whose value depends on the size of the MOSFET. The exponent α_f determines the slope of this low frequency noise term and its value is usually between 0.8 and 1.2. According to equations (2) and (3) the noise parameters α_W, γ, K_f and α_f, together with static and signal parameters n and g_m, fully characterize the noise performance of MOS transistors.

IV. NOISE MEASUREMENT RESULTS

Noise voltage spectra were measured for PMOS and NMOS with different gate widths and lengths belonging to both the investigated technologies. Fig. 1 to Fig. 5 are a typical set of experimental results concerning devices in the 90 nm process. For the devices in the 130 nm process, noise measurement results can be found in [13], while the effects of ionizing radiation on the noise properties are studied in [14]. The device parameters were characterized at drain currents I_D below 1 mA, as dictated by power dissipation constraints in high density monolithic front-end systems. In these conditions nanoscale devices are biased in weak or moderate inversion. Fig. 1 compares the noise voltage spectra of a PMOS and an NMOS with the same gate dimensions. The devices are biased at I_D=1 mA, that is in the moderate inversion region, where the NMOS has a larger transconductance with respect to the PMOS. This results in a smaller channel thermal noise for the NMOS, as it appears in the high frequency part of the spectra. The PMOS retains an advantage on the NMOS in terms of 1/f noise, which dominates the low frequency portion of the spectra. Figs. 2 and 3 show noise voltage spectra relevant to NMOS and PMOS devices with *W*=600 µm and different gate lengths *L*, biased at the same drain current. The devices are close to weak inversion, therefore, white noise should not be sizably affected by *L* variations. At low frequencies, 1/f noise

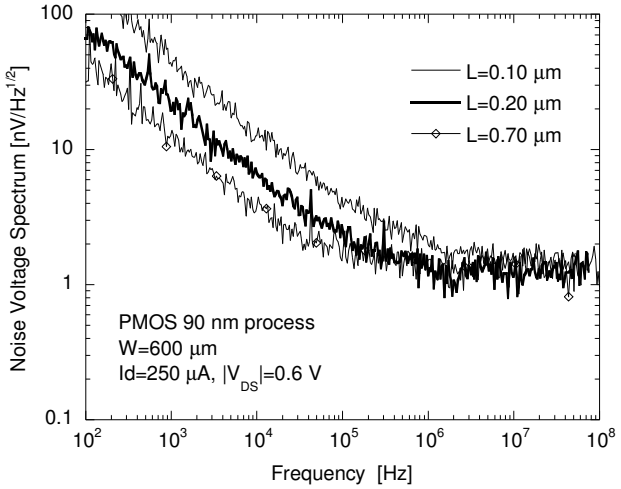

Figure 3: Noise voltage spectra of PMOS with gate width W=600 µm and different gate length L belonging to the 90 nm process (I_D=250 µA, $|V_{DS}|$=0.6 V).

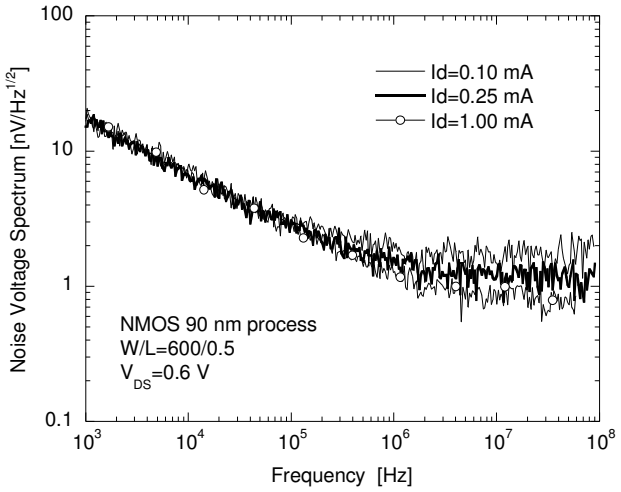

Figure 4: Noise voltage spectra of an NMOS with W/L=600/0.5 belonging to the 90 nm process at different values of drain current I_D (V_{DS}=0.6 V).

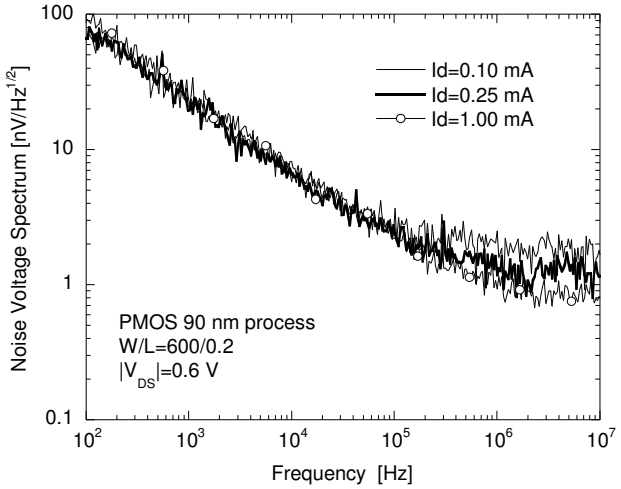

Figure 5: Noise voltage spectra of a PMOS with W/L=600/0.2 belonging to the 90 nm process at different values of drain current I_D ($|V_{DS}|$=0.6 V).

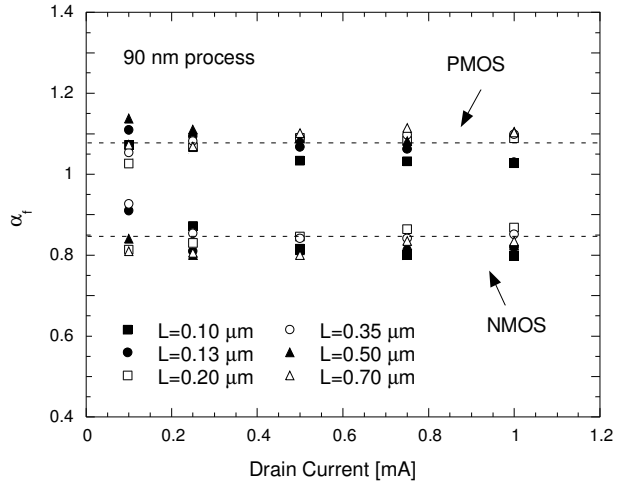

Figure 6: Slope of the 1/f noise term as a function of the drain current I_D for NMOS and PMOS devices with W=600 µm belonging to the 90 nm process ($|V_{DS}|$=0.6 V).

increases with decreasing L. According to (3), this is due to the reduction in the input capacitance C_i. Figs. 4 and 5 show the effect of the drain current I_D on the noise voltage of an NMOS and a PMOS. Channel thermal noise is reduced by increasing I_D in agreement with (2), since the transconductance correspondingly increases. As far as the 1/f noise component is concerned, it is not affected by I_D variations for NMOS devices while a slight increase with the drain current is detected for PMOS devices. In the following the behavior of the 1/f and white noise parameters is studied as a function of the device polarity and of the gate length and width to account for different detector requirements at different drain currents. A comparison of parameters concerning the two investigated technologies is also shown.

A. 1/f noise parameters K_f *and* α_f

In Fig. 1 it can be observed that the slope of the 1/f noise component of the spectrum α_f is not equal to 1. The analysis of the experimental results shows that α_f is consistently smaller than 1 in NMOSFETs and larger than 1 in PMOSFETs. This behavior was detected in other deep submicron processes [15,16] and could be related to a different profile of oxide traps interacting with carriers of different polarity. Typical values of α_f obtained for devices of both polarities in the two investigated processes are reported in table 1 together with the spread across samples with different gate dimensions and tested in different bias conditions. From the measured noise voltage spectra it has been found that 1/f noise parameter α_f does not exhibit any clear dependence on the channel length L nor on the drain current I_D as shown in Fig. 6. Fig. 7 shows the behavior of the

Table 1: Slope coefficient of the low frequency noise term.

	α_f	
Process	130 nm	90 nm
NMOS	0.85±0.05	0.85±0.05
PMOS	1.19±0.05	1.09±0.05

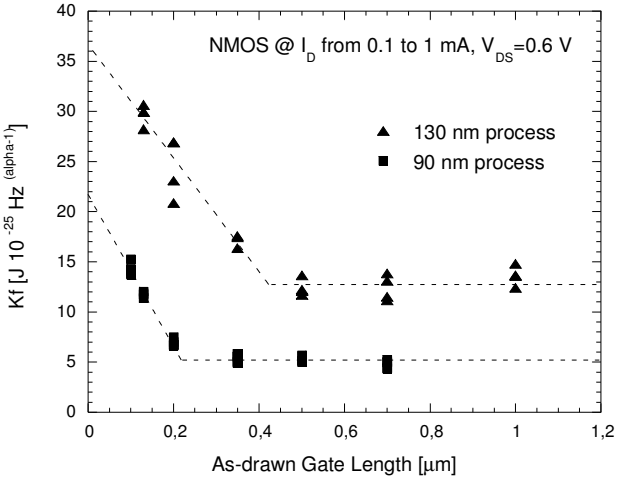

Figure 7: 1/f noise coefficient K_f as a function of the gate length L for NMOS belonging to the 130 nm and 90 nm processes (V_{DS}=0.6 V).

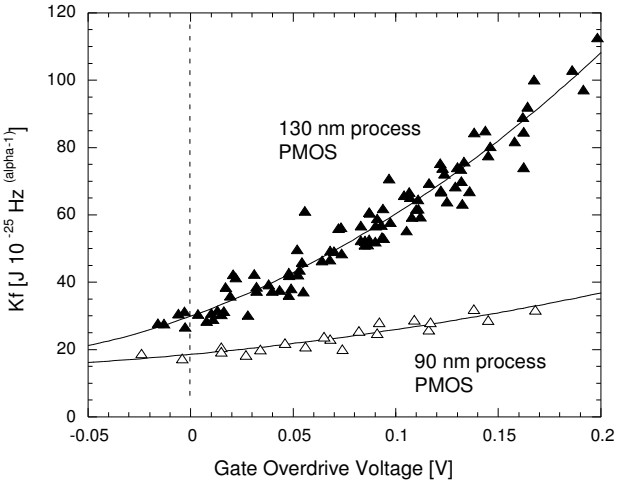

Figure 8: 1/f noise coefficient K_f as a function of the overdrive voltage for PMOS belonging to the 130 nm and 90 nm processes ($|V_{DS}|$=0.6 V).

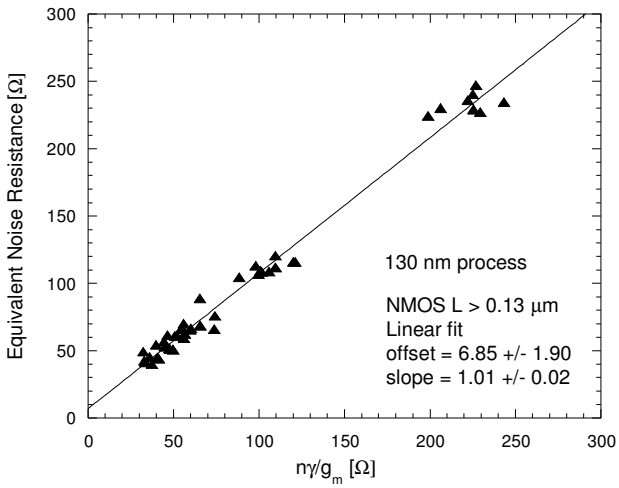

Figure 9: Equivalent channel thermal noise resistance R_{eq} for NMOS devices belonging to the 130 nm process (V_{DS}=0.6 V).

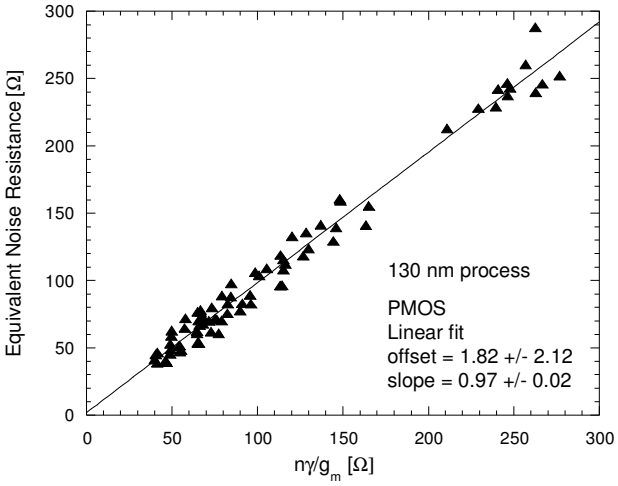

Figure 10: Equivalent channel thermal noise resistance R_{eq} for PMOS devices belonging to the 130 nm process ($|V_{DS}|$=0.6 V).

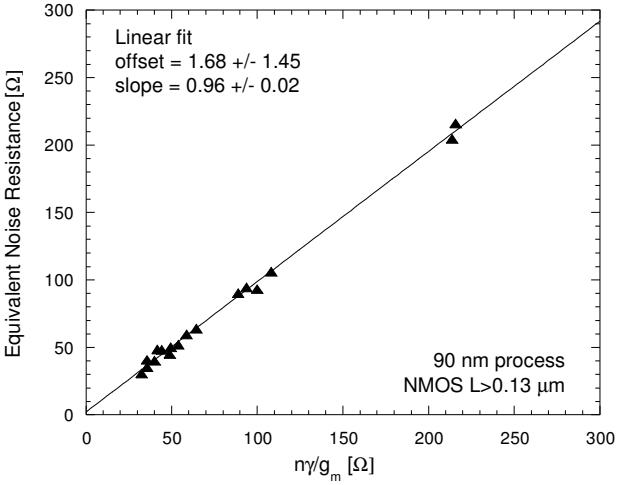

Figure 11: Equivalent channel thermal noise resistance R_{eq} for NMOS devices belonging to the 90 nm process (V_{DS}=0.6 V).

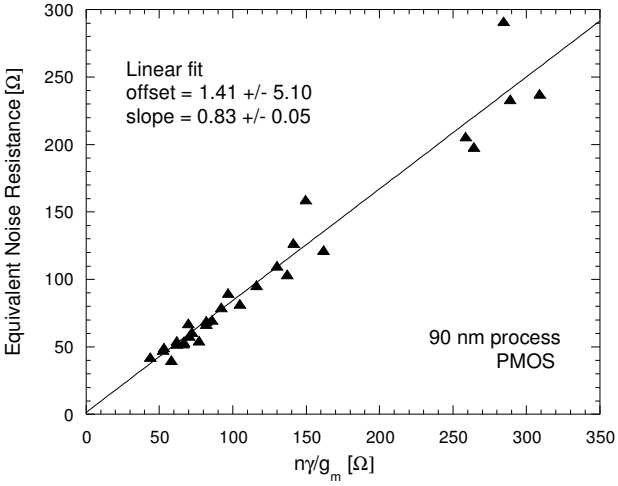

Figure 12: Equivalent channel thermal noise resistance R_{eq} for PMOS devices belonging to the 90 nm process ($|V_{DS}|$=0.6 V).

1/f noise coefficient K_f for NMOS devices as a function of the channel length. In both processes the 1/f noise coefficient K_f is larger for devices with channel length close to the minimum allowed by the technology and is lower in the 90 nm process with respect to 130 nm process. Moreover it is independent of the drain current in the NMOS. Measurements on PMOS devices show an increase of K_f both with the channel length L and the drain current I_D. According to [16,17] this behavior is due to the origin of flicker noise that, in p-channel devices, is often attributed to mobility fluctuations, and shows an increase of K_f with the overdrive voltage. In Fig. 8 values of K_f obtained for devices with different gate geometry and bias condition are reported as a function of $(V_{GS}-V_T)$. According to this plot K_f is larger for devices in the 130 nm process and its bias dependence is weaker in 90 nm technology.

B. White noise parameters α_W and γ

White noise is evaluated in terms of the equivalent channel thermal noise resistance R_{eq}. Figs. 9 and 10 show values of R_{eq} as a function of $n\gamma/g_m$ obtained for NMOS and PMOS devices belonging to the 130 nm process. According to equation (2) the slope of the linear fit is determined by the coefficient α_W while the offset is due to contributions from parasitic resistance. Values of α_W close to unity were found for all devices except for NMOS with the minimum feature size allowed by the technology. This means that there are no sizeable short channel effects in the considered operating regions. Negligible contributions were found from parasitic resistance. Same results were obtained for 90 nm process devices as shown in Figs. 11 and 12. In this case no data are available for channel thermal noise in NMOS devices with $L \leq 0.13$ μm.

V. CONCLUSIONS

The paper presents noise measurement results concerning devices belonging to two different CMOS technology nodes, namely the 130 nm and the 90 nm STM processes. The analysis of the experimental results show that channel thermal noise equations developed to describe the device behavior in the considered operating regions provide a reliable model, with short channel effect playing a minor role in both the considered processes. 1/f noise results confirm the behavior detected in previous submicron processes as far as the dependence on device polarity and bias and gate geometry is concerned. Extracted noise parameters show that using the 90 nm process may ensure an improvement in the noise performances in applications where large signal dynamic range is not needed while miniaturization can be an asset.

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Evaluation of Data Transmission at 80 MHz and 160 MHz Over Backplane, Copper and Optical Links

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Abstract

The bunch clock frequency of the LHC accelerator at CERN is specified as 40.07897 MHz [1]. Most of the LHC experiments will utilize this frequency, its multiples or derivatives as the main frequency of data transmission for their synchronous Trigger and DAQ electronic systems. For example, the triggering system of the Cathode Strip Chamber (CSC) sub-detector at the CMS experiment comprises the on-chamber anode and cathode electronics, the off-chamber boards housed in 9U crates mounted on the periphery of the Endcap iron disks, and one Track Finder (TF) crate located in the underground counting room (Fig.1). Due to the significant amount of data from the front end, the trigger patterns are multiplexed and sent from the CSC chambers over copper cables using the LVDS standard at 80 MHz. For the same reason the data patterns transmitted over backplanes in the peripheral and TF crates are also multiplexed and sent at 80MHz using the GTLP standard. Optical links from the peripheral crates to the TF are operated at 80 MHz as well. Finally, the parallel LVDS links to the Global Muon Trigger (GMT) run at 40 MHz.

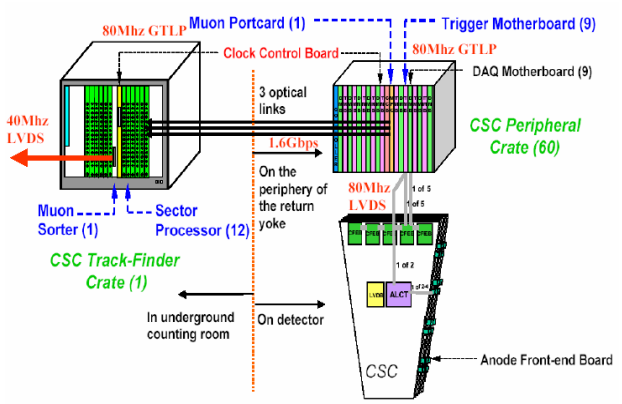

Figure 1: CSC Trigger Electronic System

A proposed Super LHS (SLHC) upgrade [2] would increase the operating frequency of the accelerator, and be challenging for many synchronous data transmission systems. The goal of this work was to evaluate possible solutions for data transmission at 80 MHz and 160 MHz suitable for the SLHC era. We have used an existing hardware designed for the CSC electronic system for evaluation of data transmission at 160 MHz using the LVDS and GTLP logical standards. We have designed a new evaluation board to study the optical links operating at 160 MHz. The results of measurements and possible solutions are presented.

I. GTLP Backplane Interface

Gunning Transceiver-Logic Plus (GTLP) is a widely used logical interface for point-to-point and bussed data transmission over backplane. Within the CSC electronic system it is used for the point-to-point transmission in the peripheral and TF crates at 80 MHz. The total number of data sources is 288 (9 boards) in the peripheral and 384 (12 boards) in the TF crate. The boards that receive all these signals reside in the middle of each crate (the Muon Port Card (MPC) [3] in the peripheral and the Muon Sorter (MS) [4] in the TF crate). Both backplanes also utilize a 40 MHz control GTLP bus. The TF backplane is a 6U, 21-slot multiplayer custom board residing in the 9U crate below the J1 part of the VME64x backplane. A pairs of Texas Instruments SN74GTLPH16912 transceivers are used in the TF crate and pairs of National Semiconductor GTLP16612 driver and Fairchild GTLP18T612 receiver are used in the peripheral crate.

There are three parameters that may be adjusted to optimise the GTLP performance: termination resistance Rt, termination voltage Vt, and a reference voltage Vref for GTLP receivers. Termination resistors of 56 Ohm for all point-to-point GTLP lines are located on the receiver boards (MPC and MS) while the 100 Ohm terminations for a control bus are located on both ends of the custom backplane. The termination voltage is provided from a custom backplane and fixed at +1.5V. The reference voltage Vref can be adjusted (0.9V… 1.1V) with a potentiometer on a receiver board. We found that the best performance (duty cycle close to 50% and widest “safe window”) is achievable with the Vref=0.9V.

In both backplanes the main master 40 MHz clock is distributed to all slots over individual LVDS lines of equal length from a common source, the Clock and Control Board (CCB) [5]. This board carries a mezzanine TTCrq card that is an interface to LHC Timing, Trigger and Control system [1].

All the peripheral and TF boards are based on various Xilinx FPGA devices. They produce internal 80 MHz clocks by doubling the master CCB clock. These 80 MHz clocks are well aligned on all trigger boards and are used to send data to the MPC and MS. After GTLP-to-LVTTL conversion on the MPC and MS boards an input data patterns are clocked in into the FPGA on adjustable 80 MHz clock produced by the DLL or DCM modules in the FPGA. The fine clock adjustments can be as low as 100..250 ps.

We have chosen the MS board for evaluation purposes. The main Xilinx Virtex-2 FPGA on the MS receives as many as 384 80 MHz data bits, performs sorting “4 best tracks out of 36” and transmits the four best selected patterns to the

GMT receiver. Existing MS firmware is based on demultiplexing of all incoming signals down to 40 MHz and further processing and transmission at 40 MHz. The average "safe window" of clocking data in into the FPGA while all 32 sources (on one board) and 384 sources (on all 12 boards) are sending their 80 MHz data patterns was measured as 8.0 and 6.5 ns respectively. The factors that affect the "safe window" are: variations in signal propagation from slot to slot (can be as large as 2 ns), chip-to-chip and channel-to-channel delay variations, delay changes within the transceiver with a number of switching channels, and non-ideal line termination. In overall, we found that the "safe window" of 6.5 ns is sufficient to provide a reliable operation at 80 MHz of the fully loaded TF crate.

The maximum operating frequency of the GTLP transceivers is specified as 150 MHz for the GTLP16612 and 175 MHz for other parts mentioned above. We have used a TF custom backplane for evaluation of data transmission at 160 MHz. The 40 MHz master clock from the CCB was replaced with a 80 MHz master clock and the Xilinx Virtex-2 FPGA produced a doubled clock of 160 MHz to clock data out on a transmitter board and clock it in on a receiver MS board. The main question was whether reliable data transmission at 160 MHz from several sources distributed over backplane within acceptable "safe window" is achievable. For evaluation purposes all the MS inputs were considered 160 MHz signals being demultiplexed down to 80 MHz and processed at this frequency. The sorter unit was modified and proven to work at 80 MHz. We found straightforward to double the performance of the Virtex-2 FPGA from 40 MHz to 80 MHz for a given implementation of the sorter logic.

One data source board called the Muon Tester [6] was placed in slot 6 (farthest from the MS which resided in slot 14) and the "safe window" was measured as 1.25 ns. Then another similar data source board was placed in slot 11 (closest to the MS) and the "safe window" was measured as 1.15 ns. However, when both of these boards were sending data simultaneously at 160 MHz, no "safe window" could be determined. This is not surprising since the difference in propagation delays between these slots is comparable with the measured "safe window". Even for a single 32-bit source, the "safe window" of 1.15…1.25 ns is only ~20% of the theoretical maximum (6.25 ns at 160 MHz) which is not good enough for reliable operation. So, while selected GTLP transceivers are still capable to transmit and receive data at 160 MHz, for our specific application with several 32-bit backplane sources they do not provide an acceptable solution.

II. LVDS Cable and Backplane Interfaces

The Low Voltage Differential Signaling (LVDS) technology provides a unique combination of very low output voltage swing (350 mV), low power consumption (~1.2 mW per load), high speed (up to 1 GHz) and high noise immunity (since the switching noise cancels between two lines). A current mode LVDS driver requires a termination on a receiver end. Several receivers have an integrated termination resistor to simplify the design. Both point-to-point and bussed LVDS options exist; however, we will focus on point-to-point configurations only.

For evaluation we have used a Muon Sorter board that has four 31-bit output LVDS links and one 31-bit input link (Fig.2). Texas Instruments SN75LVDS387 drivers and SN75LVDT386 receivers with integrated 110 Ohm termination are used. The data was sent out and received by the Xilinx Virtex-2 FPGA residing on a mezzanine board.

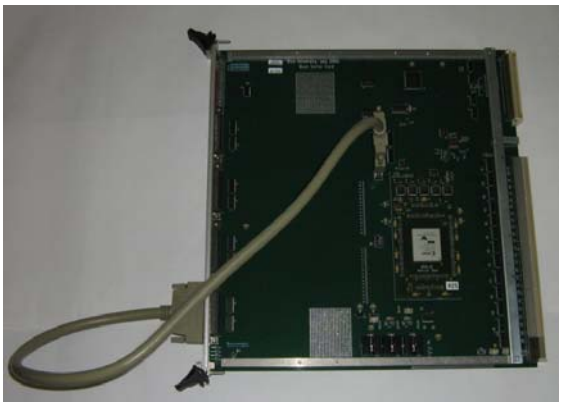

Figure 2: Muon Sorter Board

A Madison Cable 20276 Universal Ultra 320 SCSI 30 AWG 34-pair cable was tested. A non-halogen version of this cable will be used to transmit data from the Regional to Global Muon trigger systems at the CMS. Random 31-bit data patterns were sent out from FIFO_A at 80 MHz or 160 MHz on fixed clock and received after LVDS-to-LVTTL conversion into FIFO_B on an adjustable 80 MHz or 160 MHz clock (Fig. 3).

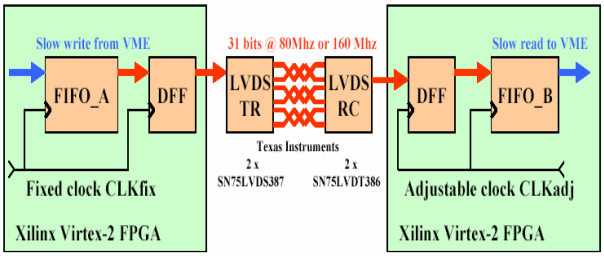

Figure 3: LVDS Testing Setup

It was found that for a 0.9 m cable the "safe window" of clocking data in into FIFO_B was 10.2 ns at 80 MHz and 3 ns at 160 MHz. For a longer 12.7 m (500 in) cable the "safe window" was measured as 9.6 ns at 80 MHz and 3 ns at 160 MHz. We consider these results as perfect for data transmission at 80 MHz and acceptable at 160 MHz. As was mentioned in section I, for a single 32-bit GTLP source link, the "safe window" was measured to be 8.0 ns at 80 MHz. The differential attenuation for a given cable is 0.09 dB/ft at 80 MHz and 0.129 dB/ft at 160 MHz. Allowed attenuation for a given LVDS chipset can be calculated as 20log(100mV/247mV) = -7.9 dB (where +/-100mV is a receiver input threshold and 247 mV is a minimum output voltage magnitude). So, based on allowed attenuation, the maximum cable lengths can be estimated as 26.4 m for data transmission at 80 MHz and 15.5 m for data transmission at 160 MHz. A skew between differential pairs (25 ps/ft

maximum for a given cable) would be below 2.2 ns and 1.2 ns respectively for these lengths.

LVDS backplane or cable links can be used as an alternative to GTLP at 160 MHz. Separate cables from each of 12 source boards in the TF crate can be easily made of equal length to avoid the differences in signal propagation from slot to slot. High density connectors (for example, from Samtec) and the Amphenol Spectra-Strip flat twisted pair cable can be used. For a backplane implementation, families of 5-, 6- or 8-row connectors for differential signaling are available from several vendors, for example, Teradyne VHDM-HSD or FCI Metral series. While the number of signal lines doubles due to the differential nature of the LVDS standard, the number of ground lines can be significantly lower than for the GTLP backplane implementation where a large number of ground pins is required to provide a low impedance path for the return current.

III. Optical and Copper Serial Links

An existing optical link between the CSC peripheral and Track Finder crates is based on the Texas Instruments (TI) TLK2501 gigabit serializer/deserializer (SERDES) and a Finisar FTRJ-8519 optical transceiver. The results of its evaluation at 80 MHz were reported in [7]. However, the Virtex-E FPGA, TLK2501 and FTRJ-8519 optical transceivers do not support data transmission at 160 MHz. We have decided to evaluate another TI device, the TLK3101 [8] and a higher speed Finisar optical transceiver, the FTRJ-8524 [9] (Fig. 4). The FTRJ-8524 transceiver supports data transmission up to 4.25 Gbps. The TLK3101 however is only rated up to 3.125 Gbps, so one of our main goals was testing at the slightly higher data rate of 3.2 Gbps. The internal core and inputs and outputs of the chosen FPGA (Virtex-2 XC2V250) can reliably operate at 160 MHz. An evaluation board [10] with two optical links was designed and built (Fig. 5).

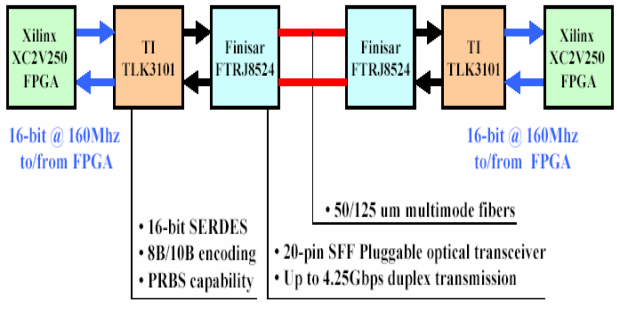

Figure 4: Optical link under evaluation

Our evaluation board carries a TTCrq mezzanine card [11] with the QPLL ASIC which provides one of the sources of 160 MHz clock for the TLK3101 devices and FPGA. The other sources of clock signal for the serializers are an on-board oscillator and the output from an external generator. Both links are identical, independent, duplex and fully controllable via VME. For each link the 16-bit data patterns can be loaded into FIFO_A buffer inside the FPGA and sent out to the TLK3101 TXD[15:0] lines upon VME command. After serial-to-parallel conversion, the RXD[15:0], RX_ER, and RX_DV lines are clocked in into the FIFO_B on recovered RX_CLK signal individually for each link. All FIFO buffers are 511-word deep and available for write and read over VME.



Figure 5: Evaluation Board

Our evaluation board carries a TTCrq mezzanine card [11] with the QPLL ASIC which provides one of the sources of 160 MHz clock for the TLK3101 devices and FPGA. The other sources of clock signal for the serializers are an on-board oscillator and the output from an external generator. Both links are identical, independent, duplex and fully controllable via VME. For each link the 16-bit data patterns can be loaded into FIFO_A buffer inside the FPGA and sent out to the TLK3101 TXD[15:0] lines upon VME command. After serial-to-parallel conversion, the RXD[15:0], RX_ER, and RX_DV lines are clocked in into the FIFO_B on recovered RX_CLK signal individually for each link. All FIFO buffers are 511-word deep and available for write and read over VME.

Our tests were conducted with random patterns transmitted from FIFO_A and verified at FIFO_B (Fig. 3) as well as with the Pseudo Random Bit Stream (PRBS) pattern generator embedded into the TLK3101 devices. The data patterns were transmitted between two links on each board and between 4 links on two boards, with optical fibers of 5 m and 100 m length. We ran transmission tests of various configurations for several hours. The results of measurements of the Bit Error Rate (BER) are summarized in Table 1.

Table 1: Results of Measurements

Clock Source	Frequency, MHz	Bit Error Rate (BER)
Epson EG-2101-CA oscillator (peak-to-peak jitter ~ 25 ps)	155.52; 161.132	$< 10^{-14}$ (PRBS), $<10^{-9}$ (Data)**
QPLL ASIC on TTCrq mezzanine board (peak-to-peak jitter ~ 50 ps)	160.3147	$~10^{-14}$ (PRBS)*, $<10^{-9}$ (Data)**
Cardinal Components CPPHV7-A7BC programmable oscillator (jitter ~ 80 ps)	160.3147	$~ 10^{-10}$ (PRBS)
Xilinx XC2V250 Digital Clock Manager (peak-to-peak jitter ~ 250 ps)	40…160	$~ 10^{-9}$ (PRBS)

* 3 errors observed, ~2.3×10^{14} bits transmitted

** Random patterns transmitted from FIFO_A to FIFO_B

A low-jitter (~25 ps peak-to-peak) clock from an EPSON EG-2101-CA oscillator provided an error free data transmission within several hours of operation. The 160 MHz clock from the QPLL is marginal, and the other two clocks, from the programmable oscillator and the Digital Clock Manager of the FPGA are unacceptable due to large jitter.

We have investigated whether the BER depends on the power supply voltage on the TLK3101 parts. While according to the specification, the supply voltage may vary between 2.3V and 2.7V with a typical value of 2.5V, we found that error free data transmission is achievable if the supply voltage is above 2.42V and within the specified range.

We also measured the total link latency. Due to silicon process and implementation variations the total link latency for both TLK3101 serializer and deserializer may vary between 110..145 bit times, or 34..45 ns at 160 MHz. Our measurements conducted at room temperature and 2.5V power for six TLK3101 parts indicated that the total link latency is between 40 and 43 ns at 160 MHz. While the exact value is different at each link initialization in increments of the serial bit clock (310 ps), it has never varied more than the 3 nanoseconds total.

A Molex 73929 SFP copper patch cable as a replacement of Finisar optical modules was also tested. This 5 m long part is made of Amphenol Spectra Strip Skewclear cable with two shielded parallel pairs. The attenuation is 0.57 dB/m at 1.562 GHz and the skew within pair is only 7.14 ps/m. We haven't seen any errors in data transmission test with PRBS patterns within 48 hours, so the BER is below 10^{-14}. Reliable transmission over longer cable can be achieved with the cable equalization using, for example, 3.2 Gbps Maxim MAX3800 Adaptive Equalizer and Cable Driver.

IV. Conclusion

As we have seen, existing GTLP parts can not provide reliable data transmission from multiple (as many as 400) distributed backplane sources at 160 MHz. Cable and backplane LVDS point-to-point links may be a good alternative solution. Reliable operation of the 31-bit LVDS link was demonstrated over 12.7 m long Madison 20276 cable at 80 MHz and 160 MHz.

Based on our experience with three identical evaluation boards (6 links total) in laboratory conditions we can conclude that the TLK3101 devices may provide reliable data transmission at 160 MHz over up to 100 m of 50/125 um multimode optical fiber (with the Finisar FTRJ-8524 optical transceivers) and over 5 m Spectra Strip Skewclear copper cable without equalization. A low jitter (less than 40 ps peak-to-peak) clock for the serializer must be provided. With various clock options, our board can be used for evaluation of other pluggable optical and copper modules as well as for pre-selection of the TLK3101 parts, if required.

Embedded FPGA serializers and deserializers may provide a good alternative to discrete devices like the TLK SERDES available from TI. However, they have a longer latency than the TI TLK devices. Among attractive features of the newest Xilinx FPGA family, the Virtex-4, are up to 24 duplex channels capable to serialize and deserialize data at 106...644 MHz.

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Unified Model Generation for FPGA-based LHCb VeLo algorithms

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Abstract

We show an alternative design approach for signal processing algorithms implemented on FPGAs. Instead of writing VHDL code for implementation and maintaining a C-model for algorithm simulation, we derive both models from one common source, allowing generation of synthesizeable VHDL and cycle- and bit-accurate C-Code. We have tested our approach on the LHCb VELO pre-processing algorithms and report on experiences gained during the course of our work.

I. Introduction

Considerable digital signal processing takes place in the TELL1 front-end electronics board [1], receiving data from the LHCb Vertex Locator (VELO) subdetector. All digital signal processing on the TELL1 has been implemented on FPGAs which allows for updates of the algorithms even after installation. This situation enables continuous algorithm improvement and therefore tuning of the overall detector performance. Evaluation of algorithms requires C-models to be integrated into the LHCb VELO simulation suite VETRA. Subsequently, matching VHDL-code needs to be developed and tuned for minimal hardware resource usage. As this typically requires modifications to at least the accuracy of the originally evaluated algorithm, one would in principal need to propagate the modifications back to the C-model and iterate again on the evaluation. Experience shows that this is unfeasible with limited manpower. Consequently, small design teams do either not iterate on algorithms, therefore limiting the theoretical performance of the detector, or C- and VHDL-models are not synchronized, making evaluation incomplete and bug tracking very cumbersome and time-consuming.

To improve upon this situation, we have suggested a unified model generation which derives needed models for simulation and implementation from one common source [2]. Parts of the FPGA-based algorithms for the VELO have been developed using the suggested design flow. We will report on experience gained during development and deployment of the derived models.

II. Confluence

Confluence [3] is a functional hardware description language (HDL) for design of digital synchronous systems. Although systems are described at register-transfer level (RTL), descriptions are more generic and less verbose than VHDL. The key reasons for this being:

- focus on synchronous systems, allowing implicit declaration of clock-, reset-, and enable-signals.
- type inference, allowing automatic type propagation through design hierarchies.
- recursion and list type, allowing for a very generic circuit description.

The Confluence compiler generates an independent netlist description (FNF) from which cycle- and bit-accurate C-models, as well as synthesizeable VHDL- and Verilog-models can be derived.

III. C-models

The C-models generated from the Confluence source code are cycle- and bit-accurate with regard to the generated VHDL-models.

The generated C-code defines a data structure containing all of the circuit's observable signals and memory elements. Each signal (including clock-, reset- and enable-signals) or bus is mapped into the least significant bits of an array of `unsigned long`. Functions acting on this data structure are `new_simulator, delete_simulator, init_simulator` and `calc_simulator`. `calc_simulator` takes the values of all input-signals and current values stored in registers and memories and propagates them through the circuit's combinatorial logic. Cycling the clock input and invoking `calc_simulator`, thus updating the respective values of all registers and memories, achieves a basic simulation cycle.

The provided cycle-accuracy is not necessary for physics simulation, but can complement advanced hardware debugging. Bit-accuracy is crucial to achieve results identical to the ones delivered by final hardware implementation. Physics simulation provides extended statistical routines to obtain overall detector performance parameters. With the integration of bit-accurate models of algorithm variations, it becomes possible to establish a convenient link between hardware design exploration and overall physics impact.

A. integration

Digital synchronous hardware is inherently clock-driven and so is the generated C-model. To match existing VETRA interfaces, it is necessary to encapsulate low-level clock-driven functionality such that it can cope with sets of data typically passed on as function parameters in C. This encapsulation is done manually and should be taken care of by the original hardware designer.

The VETRA coding guidelines enforce certain C++ code

structures, which are not fulfilled by the automatically generated C-code. This currently requires some manual intervention.

In order to allow for appropriate data probing in between different DSP modules, it is mandatory to keep data structures used in simulation close to their real counterparts implemented in hardware. While this might seem obvious, it is not. Hardware designs benefit from processing data in parallel. Data structures therefore have to allow for easy extraction of the respective data being processed by one processing unit. The same is true for merging of results, received from different processing units. At the same time, they should be simple enough to serve programmers without intimate knowledge of the inner structure of the hardware design.

B. simulation speed

When comparing execution speed of generated and hand-written C-code, an overhead can be expected due to the cycle-accuracy, added control-signals and expensive signal propagation. For some modules, execution speed differs up to a factor of 24. Measurements have shown that execution speed of the signal processing algorithms is still only a small fraction of the overall simulation time, though. Modifications to the code generation process are likely to reduce execution time considerably, but have not been investigated. The execution times shown in B. were measured on an AMD Athlon 64 X2 running SLC3 Linux.

Module name	exec. time
VeloPedestalSubtractor	$800ms$
FastVeloPedSubtractor	$30ms$
FIRFilter	$10ms$
VeloBitLimit	$10ms$
VeloChannelReorder	$190ms$
VeloClusterMaker	$< 1ms$

Table 1: Various VELO DSP module's simulation times

IV. VHDL MODELS

The generated VHDL models are fully synthesizeable and can be integrated into existing VHDL designs. Confluence does not keep the original signal names, therefore generated VHDL-code should be considered a black-box in existing designs.

Most VHDL synthesizers can infer RAM from VHDL models, as long as they comply to specific coding requirements. These requirements are however tool-dependent. Consequently Confluence struggles to provide universally synthesizeable VHDL memory descriptions. We have chosen to work around this problem by excluding memories from the common models.

A. integration

Due to the lack of memory-modeling, the generated models are quite fine-grained and therefore need to be integrated on a very low level. This makes integration into existing designs a laborious work.

V. CONCLUSION

We have shown that code, generated automatically from Confluence source code, can be integrated into VETRA and into existing VHDL designs. While the design-flow is promising considering future improvements on the algorithms and the improved quality of simulation data, it also became clear that more work is needed to simplify integration of generated models.

It has been observed that definition of interfaces for hardware and software takes very different routes even when encapsulating identical functionality. This seems to be due to the very different background present in hardware and software engineering. We believe that adopting the unified modeling approach suggested, could also improve mutual understanding and therefore overall system design quality.

VI. FUTURE WORK

Many of the Confluence-related problems encountered during our work have stimulated input to discussions on possible language improvements. Out of these discussions, a new design language implementation evolved. It is called HDCaml [4] and has laid the ground to overcome many of the problems described here. It especially eases direct access to different code generators. So far, no VELO algorithms have been implemented in HDCaml, though.

The mismatch between C-models and C++ coding guidelines poses an obstacle to fast integration. Consequently generated models should move to full C++ and Gaudi [5] compliance. The generated C-code should be analyzed for possible execution speed improvements and the code generation process should be modified accordingly. HDCaml shows a promising way to explore possible solutions to these problems, but no results can be reported so far.

The intended fast iteration on more advanced DSP algorithms will only become efficient if the original description allows for enough abstraction to modify algorithms in a convenient way. We are currently extending HDCaml by an abstract fixed-point data type [6].

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LTPIM – Local Trigger Processor Interface Module

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Abstract

The *Local Trigger Processor Interface Module (LTPIM)* is 6U VME 64x board housing two Altera Cyclone *FPGAs* for VME interfacing and control. It is the interface between the *Central Trigger Processor (CTP)* and the *Local Trigger Processors (LTPs).*

I. Introduction

The interface between the *ATLAS Central Trigger Processor (CTP)* and the sub-detectors read-out systems is done through the *Local Trigger Processor (LTP)* modules. These modules allow each sub-system to either run in global mode, when it gets the timing and trigger signals from the *CTP*, or in local mode when it handles locally those signals. During the commissioning phase of the detector, and for test purposes, it may be necessary to have several sub-detectors able to run locally with the same timing and trigger signals (e.g the calorimeters and the level-1 calorimeter). Although feasible with the current *LTP* modules, an extra interface module, *LTPIM*, has been designed in order to avoid the need for ad-hoc cabling.

II. Location on the *ATLAS*

The *LTPIM* is the interface between the *CTP* and the *LTPs*. There is one *LTPIM* for each *Trigger Timing and Control (TTC).*

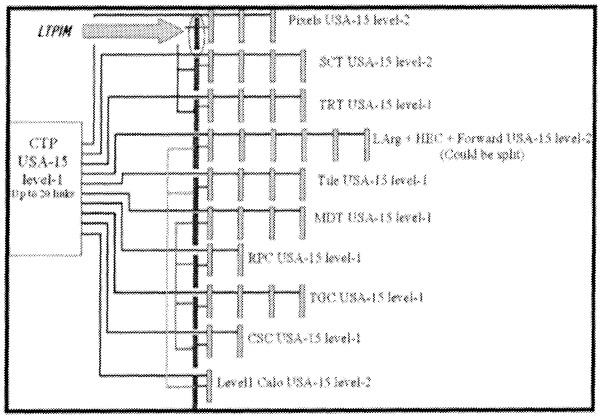

Figure 1: Location on the *ATLAS*

III. *LTPIM* Description

The Board has 8 layers which are two grounds (Analogue and Digital) and has 5 power supplies. The +5v and +3.3v are taken from the *VME* interface and there are DC/DC converters in order to provide for +1.5v, +2.5V and -5V.

There are two *CTP* links for interfacing with the *CTP* and the *LTPs* and two differential ports that connects the Interface modules.

There is also *LEMO* connectors on the front panel that can be used for monitoring signals.

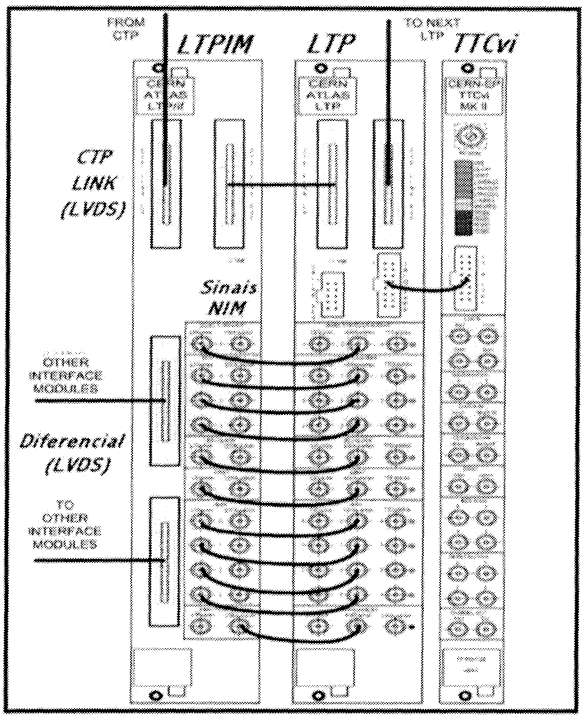

Figure 2: *LTPIM* Front panel

Since the *LTPIM* will be far from the *CTP*, special care has been taken in order to prevent for the possible loss of signal in cables. There are active equalizers for each signal coming from the *CTP*.

These active equalizers can provide a gain and equalization controlled by an analogue voltage. The analogue

voltage is provided by a four independent channel *DAC* connected to the control *FPGA*.

There are also delay circuits that are able to delay all the signals (except the *BC* clock) in order to synchronize or to provide necessary delay.

The delay circuits are programmed using an *I2C* bus.

The *I2C* bus master is implemented on the control *FPGA*.

LVDS signals from the *CTP* links and from the differential ports are converted to *LVTTL* for monitoring by the control *FPGA*. *NIM* signals from the *LEMO* inputs are converted to *ECL* and then into *LVTTL*.

All signals can be monitored by *VME* using the monitoring registers implemented on the control *FPGA*.

IV. Operation Mode

All connection where made in order to maximize testing capability and according to the *ATLAS* needs.

At the moment it is expected the *LTPIM* to work in three different modes of operation. However the possibility of having other configurations was accounted for. There are the "transparent" mode, the "slave" mode and the "master" mode.

Master and slave mode are to be used mostly during tests and commissioning and transparent mode should be used when the ATLAS detector is running.

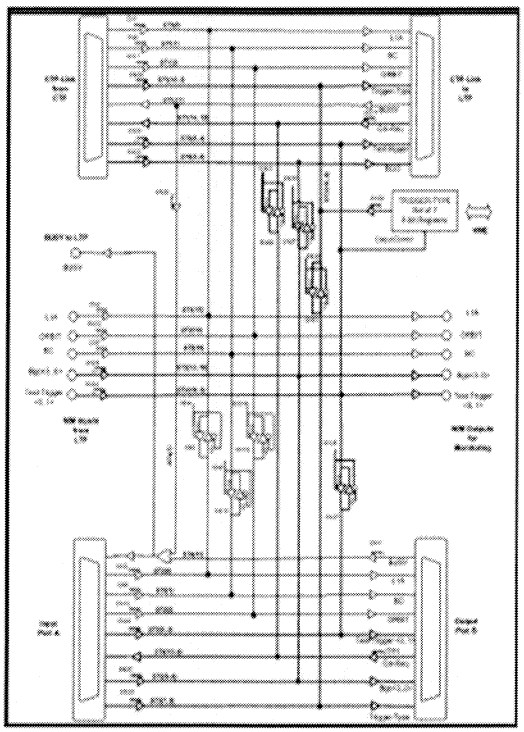

Figure 3: *LTPIM* connections

A. *"Transparent mode"*

All signals from the *CTP* link input are directly sent to the *CTP* link output. Is this configuration the *LTPIM* is only used to provide gain and equalization into the active equalizers on the *CTP* link input and to provide for signal delay on the *CTP* link output. The path delay without any signal delay was kept to minimal and should be 10 -15 ns.

B. *"Master mode"*

Using this configuration we have a master *LTP* sending the signals to the *LTPIM*. The master *LTPIM* will send them to the slave *LTPIM* of the slave *LTP* on that partition.

Signals can be put in using the differential input, the *NIM* inputs or the *VME* interface.

The active equalizers may not be used in this configuration but the delay circuits can be quite helpful in testing, calibration and commissioning.

C. *"Slave mode"*

Using this configuration, the slave *LTPIM* receives data from a *LTPIM* master or from another slave and sends it into the *LTP* of the sub partition.

Active equalizers and delay circuits can be used in this configuration.

V. Configurable Logic

The *LTPIM* houses to Altera Cyclone *EP1C4F324C6 FPGAs* for *VME* interfacing and control. It has an *EPSC4* serial memory configuration device for *FPGA* configuration.
The control *FPGA* is also responsible for the *I2C* bus communication.

A. *"VME Interfacing"*

The *LTPIM VME* interface implements a standard *VME* 64x slave with a simple state machine.

It recognizes address only cycles, data transmission cycles and interrupt cycles. Interrupt cycles are disabled at this moment because it is not expected the *LTPIM* to generate interruptions. However the connections were made in order to account for that possibility in the future.

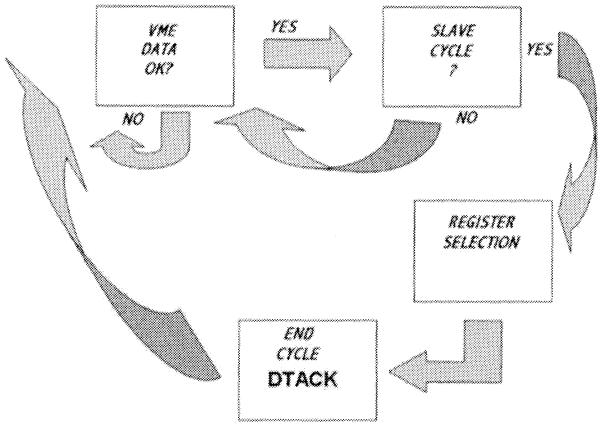

Figure 4: *LTPIM VME* slave simplified schematic

The *LTPIM VME* slave interface is designed for 24 bits addressing and 16 bits data cycle.

Bits 23 to 8 are used to select the *LTPIM* board and bits 7 to 0 are used to select the internal registers. Upon an addressing to the *LTPIM*, information about the register being addressed is sent to the control *FPGA*.

It is generated a delay in order to permit the control *FPGA* to capture data from the *VME* data bus.

When the transmission is complete, the *VME* slave interface generates a *DTACK*, signalling the end of the transmission.

B. *"Control FPGA"*

The control *FPGA* is divided in three blocks: *VME* and monitoring registers, control and tri state gate selection and *I2C* master.

Is has eleven 16 bit registers. Seven of that are accessed by *VME*, the other four are for monitoring.

Register selection is made using a select bit coming from the *VME* interface *FPGA* that will select the proper internal register.

Monitoring registers are used to monitor each line of the *LTPIM*. This condition can be extremely helpful in testing and debugging not only the *LTPIM* but also the *LTPs* and the signals between the *ATLAS* partitions.

Special care has been taken in order to prevent bus conflicts when using the tri state gates. There are codes of operation programmed by *VME* that prevent possible multiple buffers to drive the same bus line.

On power up, the *CTP* links and the differential links are transparent and the *NIM* and transceivers are tri stated.

This is necessary to insure that the board will not be damaged when a cable is connected to his input gates.

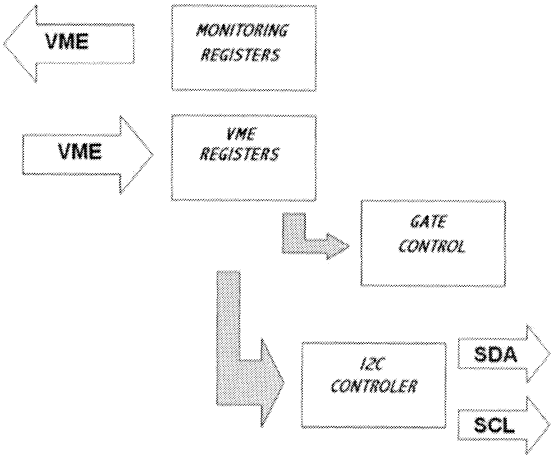

Figure 5: *LTPIM* control slave simplified schematic

The *I2C* bus communication developed by Philips(1) uses only two lines. There are the *Serial Clock (SDC)* and the *Serial Data (SDA)*. This bus however simple in structure provides a very reliable communication and since it only uses two lines is quite simple to layout.

The *I2C* communication is used to program a four independent channel *DAC* that will provide the analogue voltage used by the active equalizers.

It is also used to program the delay circuits on the *CTP* link output.

There are five registers that are needed to program the *I2C* communication, all accessed by *VME*.

The user can program the clock speed, and has total control of the bus communication at any time by *VME* access.

The *I2C* master core is an improved version of the Opencores version developed by Richard Herveille(2).

VI. TESTS

The tests done so far were in the prototype *FPGAs* and *VHDL* codes.

The *VME* interface was tested with success for all registers and for all *VME* bus configurations.

The *VHDL* control code was also tested in register write and read access and on the *I2C* communication with the slaves on the board. The hardware tests are undergoing on *CERN*, and despite a few problems regarding the active equalizers, they are proceeding well.

Hardware extensive tests as well as integration tests are still to be made.

VII. FUTURE WORK

Future work will address manly the high level software in order to program and control the *LTPIM*. There are some minor changes to be done on the *VHDL* codes in order to make then easier to understand. Schematic design will also suffer modifications before the *LTPIM* board goes into production.

VIII. LTPIM

All files regarding the *LTPIM* are available on the *CERN's EDMS* service.

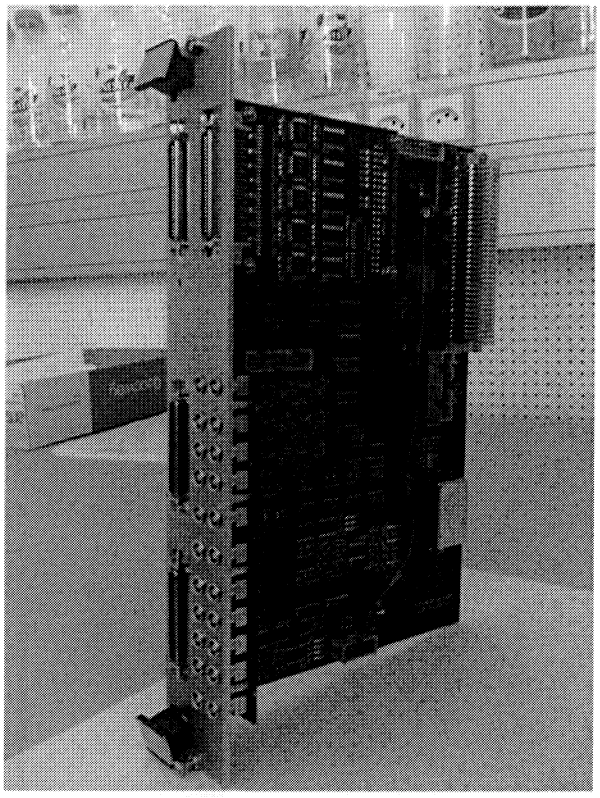

Figure 6: *LTPIM* Picture

IX. ACKNOLEDGES

We would like to thanks to Marcelo Perantoni and all of level one trigger team at *CERN* for all the excellent work and help during this project…

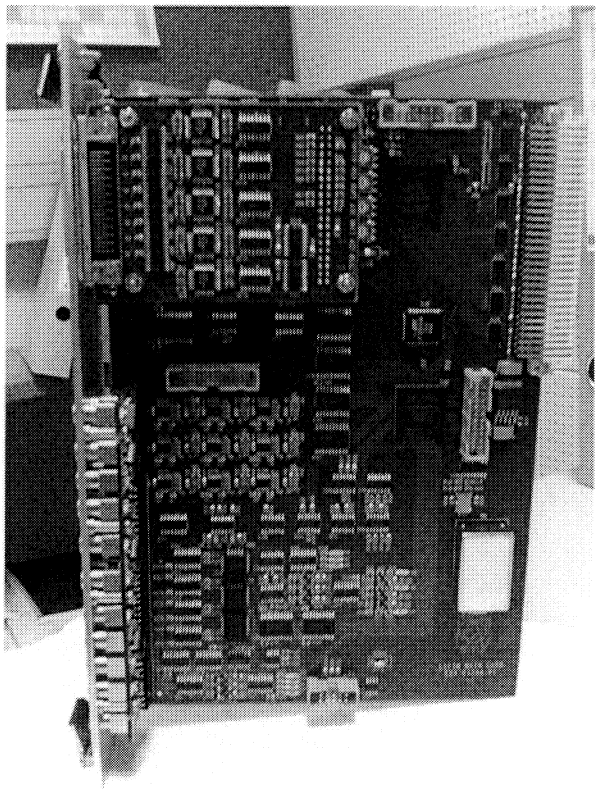

Figure 7: *LTPIM* Picture

X. . BIBLIOGRAPHY

(1) http://www.nxp.com/products/interface_control/i2c/

(2) www.opencores.org/Richard Herveille

Signal Integrity Analysis of High-Speed Interconnects

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Abstract

LHC detectors and future experiments will produce very large amount of data that will be transferred at multi-Gigabit speeds. At such data rates, signal-integrity effects become important and traditional rules of thumb are no longer enough for the design and layout of the traces.

Simulations for signal-integrity effects at board level provide a way to study and validate several scenarios before arriving at a set of optimized design rules prior to building the actual printed circuit board (PCB).

This article describes some of the available tools at CERN. Two case studies will be used to highlight the capabilities of these programs.

I. INTRODUCTION

Increasing clock-speeds and decreasing signal rise- and fall-times means that printed circuit board (PCB) traces on typical high-speed designs can no longer be considered as perfect point-to-point connections. Typical signal-integrity effects can lead to crosstalk, reflection and power-distribution noise problems that can cause false signal switching. These problems are exacerbated with the introduction of vias or other discontinuities.

It becomes necessary to provide more accurate models of interconnects and associated discontinuities on a typical PCB. Electromagnetic field solvers can be used to provide very accurate representations of interconnections but they are time- and compute-intensive to obtain so can only be used to characterise relatively small regions of the design. Using such a method for a full board simulation is impractical. To overcome this problem, the electromagnetic tool derived model is typically extracted and used in a conventional circuit simulator to analyse signal-integrity effects more fully.

Two examples will be presented. The first illustrates the design of an optimum low-mass cable which minimizes crosstalk between a pair of 2.5Gbps signals and the adjacent traces. The second case involves the study of the transmission of 1.6Gbps signals through via discontinuities within a 18 layer PCB stack-up.

The two case examples were analysed using commercially available programs to investigate if they could provide an efficient and practical way to take into account design aspects affecting signal propagation.

II. LOW MASS CABLE DESIGN

The Gigatracker is to be used in the proposed NA48/3 experiment as part of the high performance hodoscope to track a high density beam of one thousand million particles per second [1]. The Gigatracker Low Mass Cable **(**LMC) is used to bring data outside the high radiation environment for digital processing.

A. Low Mass Cable

Gigatracker's LMC is designed as a 3-layer PCB on an aluminium/kapton substrate [2]. The initial proposal for the design of the LMC is shown in Figure 1.

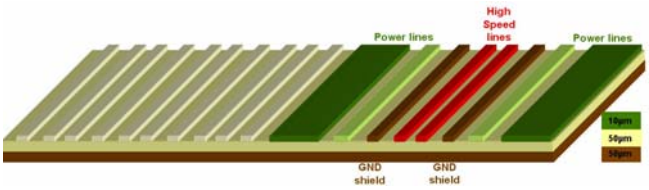


Figure 1: LMC initial design proposal

High-speed data (running at 2.5Gbps), control information (at 40MHz rate) and power are transferred through adjacent microstrip traces on the top layer of the LMC's PCB. In between signals, the initial design considers shielding (GND shield) to minimize the electromagnetic fields transfer to neighbouring traces.

B. Objectives

The Gigatracker design calls for an optimum LMC which minimizes signal integrity issues such as reflections and crosstalk.

Starting from the initial design proposal and taking into account given constraints, we focussed on how to find an optimum design for the LMC such that to reduce the coupling between different traces. Another objective was to extract a corresponding model for the LMC and use it in the HSPICE simulation of a full transmission channel incorporating a custom designed LVDS transceiver.

C. Constraints

One of the most important constraints of the LMC design, with direct impact on the amount of coupling and induced crosstalk, is the imposed maximum limit of 10mm for the cable's width. Due to this, the crosstalk cannot be reduced by placing the traces further away from each other. Other constraints of the design were accounting for a fixed 3-layers PCB stack-up build with aluminium as conductive material for low material budget, and with kapton as dielectric due to its mechanical flexibility.

D. Strategies

Theory states that the coupling between adjacent traces is influenced by the distance and the shielding. The analysis focussed therefore on crosstalk minimization by studying the influence of the shielding and the effect of bringing the power lines closer to the signal traces.

E. Tools and Methodologies

The HFSS electromagnetic field solver from Ansoft [3] was used to analyse and provide verified rules to be applied in the design of the LMC.

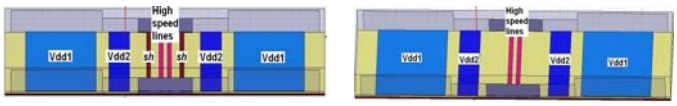
In order to be able to compute Maxwell's equations in the frequency domain using Finite Element Method, HFSS requires a 3-D geometry problem description, the specifications of the electromagnetic characteristics of materials composing the geometry, the setup of the excitation ports and the boundaries along with the required frequency bandwidth and the desired computation accuracy.

The program uses an adaptive mesh refinement algorithm to discretize the geometry into small mesh elements - such as tetrahedrons - in the 3D space. Maxwell's equations are computed within each individual mesh element for different frequency points. The final solutions from HFSS are represented by electromagnetic fields, Scattering-parameters and impedance values, all results being obtained after interpolating the individual values computed within the previously user-defined frequency range.

F. HFSS Results

The HFSS results for the LMC design presented in this section are obtained over a frequency range from 100MHz to 25GHz.

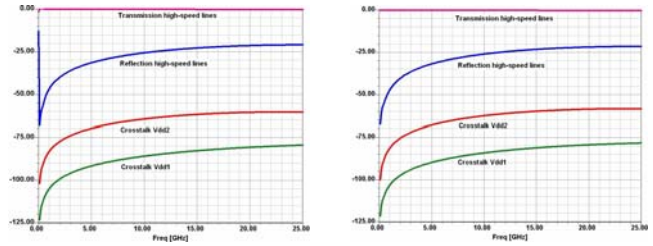
HFSS was used to analyse the LMC geometries with and without the shielding traces to examine their influence on the induced crosstalk from the high-speed signals into the power lines (Figure 2 a. and b.).



a.) shielding b.) No shielding

Figure 2: LMC geometry

The Scattering-parameter results, in terms of transmission through the high-speed lines, reflection at the incident port and crosstalk into the power line Vdd2, respectively Vdd1 are presented in Figure 3 a. and b.



a.) shielding b.) No shielding

Figure 3: S-parameter results from HFSS

The crosstalk induced into the closer power line Vdd2 stays below a level of -60dB at 25GHz; this corresponds to a level of induced noise of less than 0.1%. By removing the shielding, the crosstalk, induced into the same line, increases with 2dB (0.125%), value which is still considered very low. From these results we could conclude that the influence of the shielding on the overall crosstalk level is minimal. A first design rule would therefore suggest building the LMC without the shielding. This, in turn, will result in an important economy of aluminium material.

We further studied the impact of bringing the power lines closer to the high-speed signals. The geometry analysed and the corresponding S-parameters for this case are shown in Figure 4 and Figure 5.

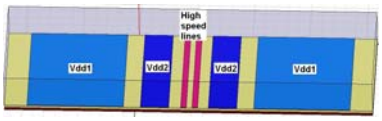


Figure 4: New LMC geometry

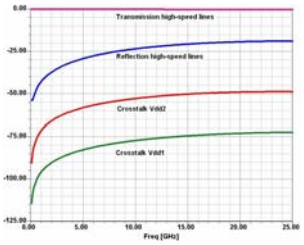


Figure 5: S-parameter results

In this case, the crosstalk induced from the high-speed lines into the power increases evidently more. However, a value of -47dB at 25GHz could be considered acceptably low. A second design rule suggests therefore bringing the power traces closer to the serial lines. This would allow the final LMC to be even narrower than the designer imposed constraint.

G. Time-domain Results

The previous results from HFSS can also be made available to other simulators via the implemented Spice-extraction scheme or through Touchstone export.

The resulting equivalent full-wave model provided by HFSS was exported to HSPICE and simulated as part of a larger electrical circuit. The extended transmission channel from the read-out chip to an ideal receiver, across the LMC, is shown in Figure 6. The read-out chip on the detector is a custom ASIC design realized by the MIC group at CERN.

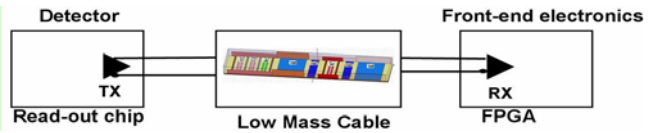
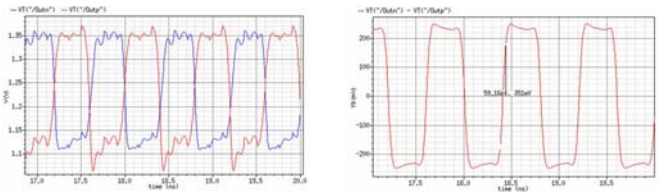


Figure 6: Simulated transmission channel

The time-domain simulations were performed in Cadence Specctre and the single-ended and differential results seen at the receiver are shown in Figure 7.



a.) Single-ended b.) Differential

Figure 7: Time-domain simulation results

The simulation shows very good signal characteristics: the rise time is not degraded and the desired amplitude level is reached after switching with no obvious ringing present in the received signal.

H. Conclusions

Starting from an initial design proposal, we highlighted the usefulness of a 3D electromagnetic field solver such as HFSS. By employing frequency-domain modelling in the analysis of different configurations, we developed pre-layout analysis rules to be followed for an optimum design of the LMC. An accurate SPICE model, extracted from the field solver analysis, was used to simulate and estimate in the time-domain the signal transmission quality between the read-out and the processing electronics using the LMC.

III. PCB VIA DESIGN

At increasing clock-speeds and decreasing signal switching times, it becomes necessary to provide accurate modeling of vias and connectors, as part of an usual PCB design.

A. Differential pair of vias

As a concrete example, we look into the design of an inter-layer connection represented by a differential pair of vias built within a 18 layer PCB stack-up. This via structure, shown in Figure 8, is used to pass LVDS signals at 1.6Gbps from one layer to another of the muon trigger processing board used in the LHCb experiment [4].

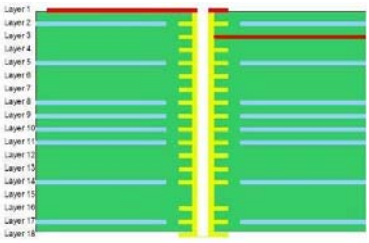


Figure 8: Differential pair of vias within the PCB stack-up

B. Objectives

While PCB interconnects, such as microstrip and stripline, can be modelled accurately using 2D solvers, the complexity of via interconnects warranted deeper study and therefore requires the use of 3D electromagnetic programs. Our goal throughout this exercise was to model the vias throughout the electromagnetic analysis and then to incorporate the obtained model within a full-transmission channel simulation at the circuit-level.

C. Tools and Methodologies

The differential via geometry was analyzed using 3D electromagnetic field simulation in Microwave Studio from CST [5]. Microwave Studio (MWS) is an electromagnetic field solver based on Finite Integration Technique, method which solves in the time-domain the integral form of Maxwell's equations. For this, MWS requires the input of the geometric model, the materials' definition, the boundaries' specification and the setup of the signal ports.

The main results from MWS are transient (time-domain) fields and signals, allowing a direct study of possible signal integrity issues without an immediate need for a SPICE simulation. MWS also provides the electromagnetic field distribution and the S-parameters of every port at any given frequency.

D. MWS Results

We analyzed with MWS the following 3D geometry (Figure 9) which includes a differential pair of signal vias and their adjacent via connections to the analogue, respectively the digital ground planes within the PCB's stackup.

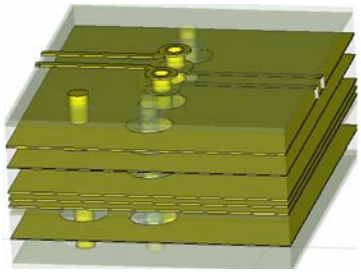


Figure 9: Differential vias geometry in MWS

MWS analyses the structure by applying a Gaussian signal automatically defined according to the user-specified frequency range. The structure's response to a pulse excitation is obtained through post-processing based on the original Gaussian simulation response. The resulting pulse signals are presented in Figure 10.

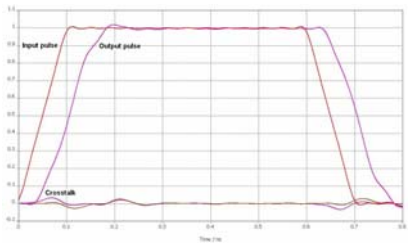


Figure 10: Time-domain pulse signals from MWS

The pulse transmitted through the via maintains good signal integrity characteristics: no obvious ringing is present, the steepness of the slope of the rise- and the fall-times is maintained and the induced near- and far-end crosstalk between the two vias is minimal (3 %).

From MWS we can also indirectly obtain the S-parameters for the studied via geometry (Figure 11).

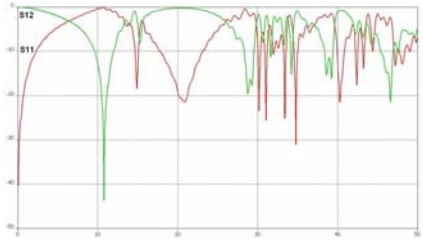


Figure 11: Time-domain pulse signals from MWS

The transmission (S12) and the reflection (S11) parameters show that via inclusion has little effect up to a frequency of 7GHz.

E. Time-domain results

The results obtained from a MWS computation gives a first indication of the signal integrity characteristics of the studied via geometry. However, on a real PCB, a signal is transmitted not only across vias but along a whole channel including different lengths of transmission lines and other discontinuities. All these elements must be included to give a more realistic estimation of the final signal arriving at the receiver.

In order to simulate the entire transmission channel, the via model was exported to HSPICE. A simplified representation of the final simulated circuit is shown in Figure 12.

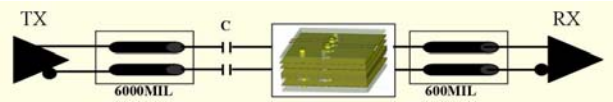
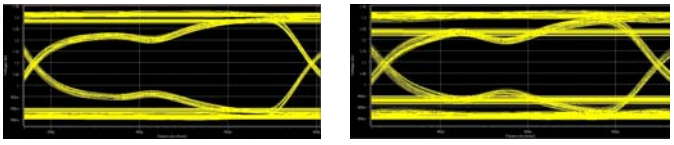


Figure 12: Simplified transmission channel on the PCB

HSPICE models were obtained for the Altera StratixGX FPGA transmitter and receiver. The transmission lines were modeled as W-elements using the Cadence Allegro PCB SI 2D solver [6]. The complete channel was simulated with and without the via models extracted by MWS. The resulting eye-diagrams seen at the receiver input are plotted in Figure 13.

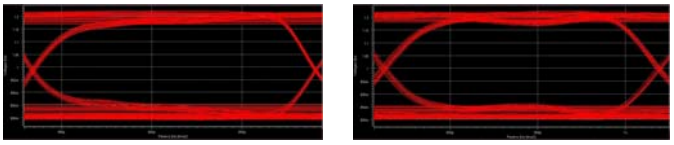


a.) No vias b.) Vias from MWS

Figure 13: Eye-diagrams before the receiver's package

The eye amplitude diminishes for the case in Figure 13.b due to energy loss in the reflections encountered at the via discontinuity. Both plotted eye-diagrams show a 'pear shape. This is probably caused by a reflection at the receiver die returning back along a short transmission line length (representing the chip package) to the receiver external pins where it sums with the original incoming signal.

The eye-diagrams at the receiver die were also examined (Figure 14).



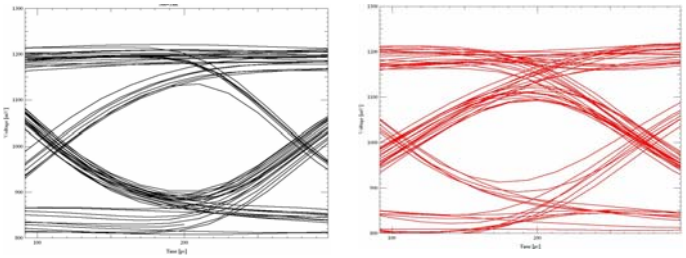
a.) No vias b.) Vias from MWS

Figure 14: Eye-diagrams after the receiver's package

The previous 'pear' shape completely disappears as no negative reflection affects the signal at this point. In addition, we note that the receiver's capability of recovering the incoming signal makes little difference for the cases with and without the vias. Close inspection reveals a slight vertical closure in the middle of the eye for the channel including vias (Figure 14. b).

It appears that the via influence on the overall quality of the transmitted signal is almost negligible on the LCHb processing board. Indeed, a 1.6Gbps signal has spectrum components at a maximum frequency of 4GHz (5th order frequency component) and the S-parameters of this via show excellent characteristics up to 7GHz (see Figure 11).

This via will start however degrading faster signals. To illustrate such a case, we increased the data rate from 1.6 to 6Gbps and simulated the same channel with and without the vias. The results at the receiver's die are presented in Figure 15.



a.) No vias b.) Vias from MWS

Figure 15: Eye-diagrams after the receiver's package

The via's contribution manifests itself as a reduction in the eye amplitude and increase of the added jitter.

F. Conclusions

The differential vias geometry was analyzed using CST Microwave Studio. The time-domain results from MWS have given a first indication of the quality of the transmission through this structure. The resulting model of the geometry was exported to HSPICE where a complete transmission channel was simulated with satisfactory results. We concluded that the signal running at 1.6Gbps on the LHCb processing board can be properly recovered despite the vias discontinuity.

Throughout this example we presented a practical simulation methodology which can be applied for the analysis of any PCB discontinuities. Using this method we verified, through simulation in post-layout, that the overall quality of the received signal corresponds to the specifications and we showed that the current via design has minimal influence on the 1.6Gbps signal running on the LHCb processing board.

We have also shown how the signal would deteriorate if the switching rate was increased.

IV. FINAL CONCLUSIONS

Throughout the two examples presented in this paper, we showed how using commercially available programs provides an efficient and practical way to study signal integrity effects and to help minimise the number of design iterations for completing projects within time and budget constraints. These tools are readily available and supported at CERN.

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Implementation of the Control System for the LHCb Muon Detector

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Abstract

The Muon Detector of LHCb will be equipped with 1368 Multi-Wire Proportional Chambers and 24 Triple-GEM Detectors. Within the Framework of the CERN Control System Project, using PVSS as the main tool, we are developing an instrument to manage the Muon System of LHCb. Adjustment and monitoring of High and Low Voltage power supplies, on-line diagnostics and fine tuning of the Front-End read-out devices, data acquisition from the gas system and the monitoring of pressure and temperature of the experimental hall are being implemented. The system will also look after long term data archiving and alert handling. The Control System performance is currently under evaluation in a cosmic ray station. Built as a final quality control of the LHCb Multi-Wire Proportional Chambers, allowing acquisition of data from as many as 600 Front-End readout channels, the cosmic ray station is fully managed by means of a Control System prototype.

I. The Muon System of LHCb

The LHCb Muon System [1], [2] will be composed of 5 stations (for a total active surface of 435 m^2) equipped with 1368 Multi-Wire Proportional Chambers of 20 different sizes. The LHCb level-0 trigger, based on a 5-fold coincidence within 25 ns, requires a fast and precise measurement of the muon transverse momentum and a high efficiency in the bunch-crossing identification. This translates in the requirements for each bigap of the chambers:

1. high efficiency ($\geq$95%) in 20 ns;

2. less than 1.1 hits per chamber per track (in average);

The LHCb MWPCs were designed in order to fulfill all those requirements. Fig. 1 shows that a time resolution of about 3.8 ns (r.m.s.) is achieved [3]. The detection efficiency in a time window of 20 ns and the pad-cluster size were measured as a function of the high voltage (HV) applied to wires. The results reported in Fig. 2 show that the above conditions 1) and 2) are satisfied for

$$2530 \leq \mathrm{HV} \leq 2700 \text{ V}. \quad (1)$$

These values define the HV working region (WR) of the chamber. The ageing test was performed at the ENEA-Casaccia centre, using the Calliope gamma facility [4]. During this test a total charge of 440 mC per centimetre of wire was integrated, without any significant deterioration of the chamber gain [4].

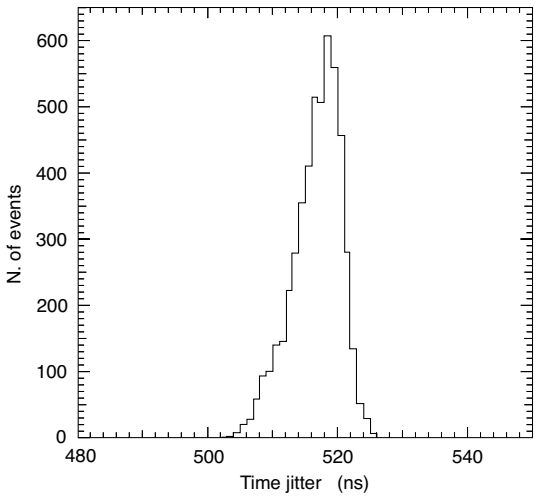

Figure 1: Typical time jitter of a four-gap chamber having a gas gain of about 5 $\times 10^4$. The zero of the time scale is arbitrary.

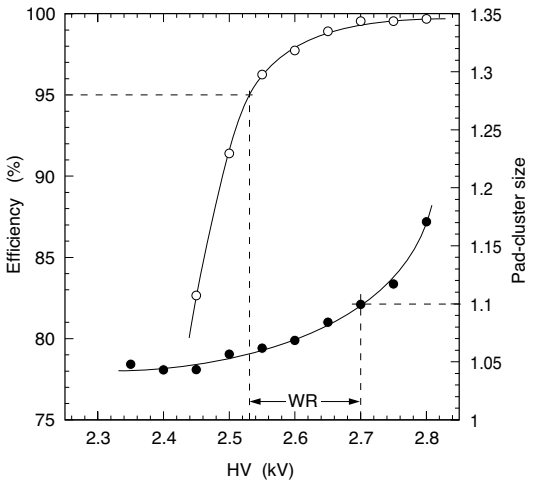

Figure 2: Efficiency (left scale and open circles) and pad-cluster size (right scale and solid circles) of a double-gap MWPC as functions of the high-voltage (HV). The working region (WR) is shown. Curves are drawn to guide the eye.

In region R3 of station M3 a charge of 3.5 (6.0) mC/cm is expected to be integrated in 10 years by a chamber operating at the centre (upper bound) of its HV working region and at an av-

erage collider luminosity of 2×10^{32} cm^{-2}s^{-1}. This ageing test proved that, for HV within the working region, the MWPC can operate safely in the LHCb experiment and that the HV upper limit is determined only by the upper limit on the pad-cluster size (Fig. 2).

II. The Muon Detector Control System

In order to manage and monitor the LHCb Muon Detector a Control System is now being developed and tested. A Finite State Machine architecture has been adopted, following the CERN Joint Controls Project (JCOP) recommendation: "*The experiment control systems are modelized as a hierarchy of Finite State Machines (FSM). In this model there is a state/command interface between a parent and its children. Commands are passed from a parent to its children and the states/alarms of the children are passed to the parent who derives its state from those of its children.*" Each item (Device Unit) is thought of as having a set of stable states. Items can move between their allowed states by making transitions triggered either by commands or state changes of a dependent FSM. After a change of state the Device Unit generates a signal to inform the Control Unit about its state. For the Muon System, the hierarchy in Fig. 3 is being implemented.

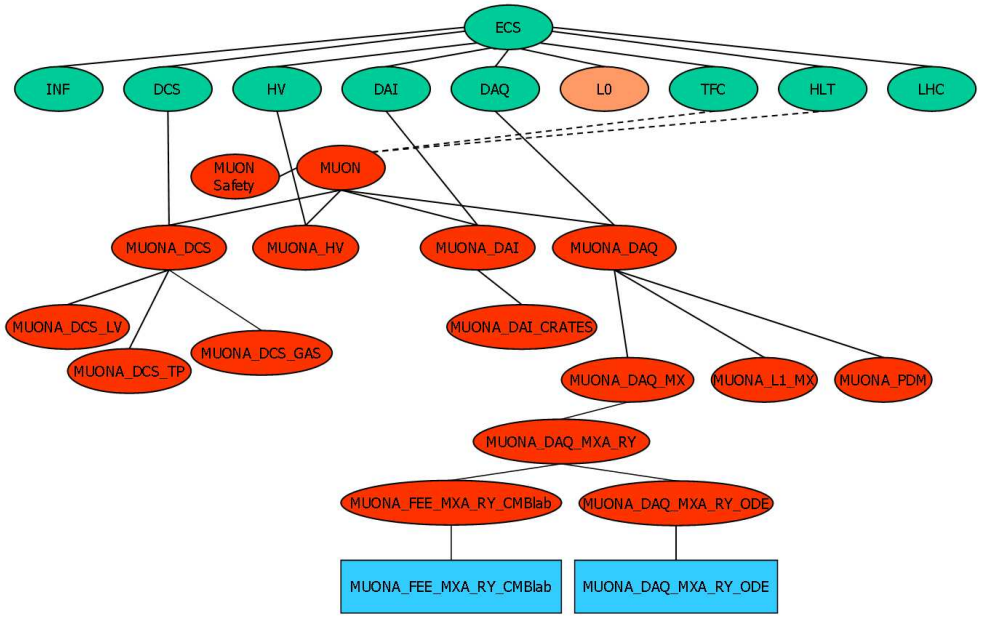

Figure 3: Hierarchy tree for the Muon Detector Control System.

The main Control Unit is called Muon and is subdivided in two Control Units for the A(ccess) and the C(ryogenics) sides. They sends commands and receives States and Alarms to and from a set of subdomains:

- *Detector Control System (DCS)* that controls the Low Voltage, Gas System and enviromental parameters (such as the temperature and the pressure);
- *High Voltage* that manages the high voltage system of the apparatus;
- *DAQ Infrastructure* that controls infrastructures needed for DAQ (such as crates and vans)
- *DAQ* that manages all the data acquisition tools. The DAQ domains is divided in subdomains controlling the electronics of each Station (M1–M5) and Region (R1–R4) of the Muon System. Different domains are foreseen for the frontend (FEE) and off detector electronics (ODE and PDM) and Level-1 boards (Tell1).

III. Detector Control System

A. Low Voltage

An array of low voltage supplies, used to provide power to the front end readout devices, will also need supervision, because of the high radiation levels in the experimental hall, and their main parameters, such as current, voltage as well as their overall status will be will be acquired.

B. Gas System

The data coming from the gas distribution system, regarding the supply of the gas mixtures to the detectors will be monitored and acquired.

C. Temperature and Pressure Sensors

Performance of the chambers in the Muon System will strongly depend on the temperature (T) and pressure (P) of the gas. For little T and P variations the dependence of the gas gain can be linearized:

$$\frac{\Delta G}{G_0} = \alpha \left(\frac{\Delta T}{T_0} - \frac{\Delta G}{G_0} \right)$$

The value of α was measured ([8] and [9]) to be 5.34 as shown in Fig.4.

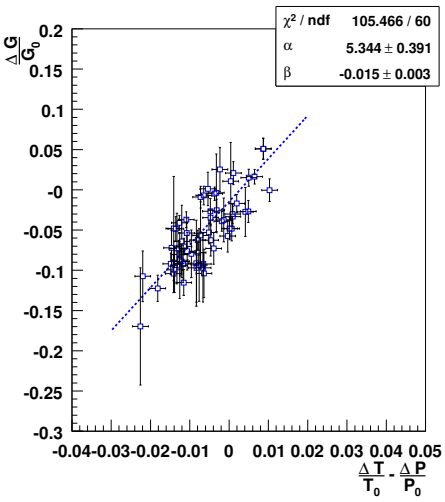

Figure 4: Dependence of the gas gain variations as a function of little temperature and pressure variations.

While the temperature inside the experimental hall will be controled and constant within 1 K, variations in of the atmospheric pressure of ± 30 mbar are expected. Consequently, the chamber gain can vary up to $\pm$ 15%. Therefore it will be mandatory to monitor and acquire the environmetal parameters.

IV. High Voltage

The MWPC will be supplied with 2 or 4 (depending on the region) HV channels, while the triple-GEM detectors will need 4 HV channels each. Therefore that there will be more than 4000 HV channels. The high perfomance required and the high particle flux foreseen in the Muon System, suggest to have all the chambers working at the same gain value in the middle of the efficiency plateau. An equalization and a stabilization of the gain will be achieved by tuning the high voltage supplies on a case by case basis.

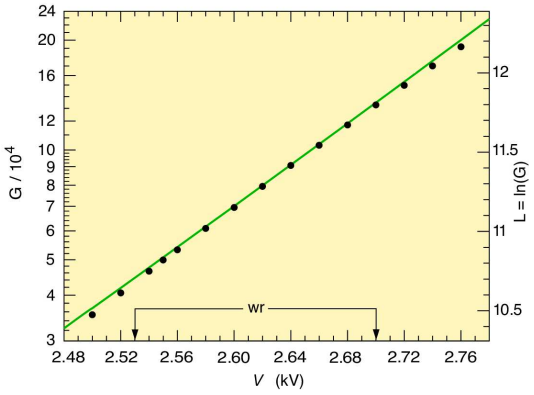

Figure 5: Dependence of the gas gain as a function of the voltage applied to the wires in the LHCb working region.

As shown in Fig. 5 the gas gain doubles each 100 V. The Control System will also manage the ramp-up and ramp-down phases of the entire high voltage system, monitoring of the current drawn at the same time.

V. DAQ

The Muon System will be made up of 120,000 readout channels. The front-end readout devices performance will require appropriate supervision. In the PVSS framework there will be one DataPoint Type for each type of chamber (20 in total). An example of a DataPoint Type for an M5R4 chamber is showed in Fig. 6. Each DataPoint is a Folder containing as many subfolders as the number of Front End Boards of the chamber. Each FEB folder contains 11 DataPoint Element: 9 dynamic arrays of integers and 2 integers. Each DataPoint element is directly linked to an equivalent SDO.

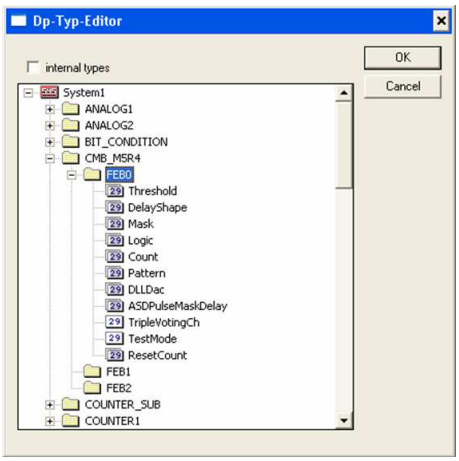

Figure 6: Example of a DataPoint type for M5R4 Muon Chamber

In this way it will be possible to exploit all the PVSS tools for data Control, Archiving and Alarm. The CANBus com-

munication is based on the segmented SDO transfer. For each chamber on the apparatus a DataPoint will be created (for a total of 1380 DataPoints). Electronic channels will need a constat monitoring of their parameter in order to single out dead or noisy channels and adjust the channel settings, such as thresholds and masks. A set of states and procedures is being developed (Fig.7).

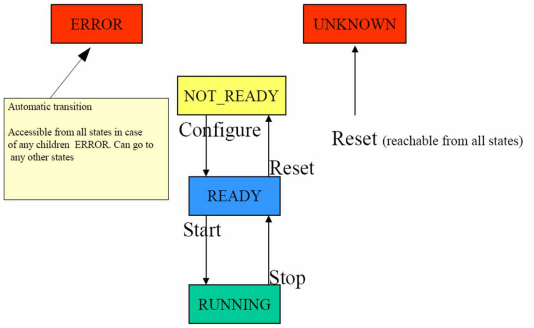

Figure 7: States and procedures of the DAQ domains

Following the general guidelines [6] of LHCb the states foreseen for the Font End Domain are:

State	Meaning
NOT-READY	The FEE boards are working and communicating properly,but they need a heavy configuration (i.e. the CONFIGURE procedure) before they can be used
READY	The FEE is correctly CONFIGUREd but it needs a light configuration (i.e. the START) procedure before acquiring. Only from this state it is possible to run the CALIBRATION procedures
RUNNING	The FEE is taking data and its configuration cannot be changed.
ERROR	An important fraction of the Front End boards has published an ERROR state and is not able to take valid data.
UNKNOWN	It is not possible to communicate with part of the system.

They can be divided into two main groups: INTERNAL (only the FEE domain is involved).

- CONFIGURE: loading of all default values from the Configuration DB or from some preloaded memory in the Service Board;
- START: fine tuning of main parameters (threshold, logic, masks) according to different possible acquisition runs;
- STOP: reset the value of FE channels to the default ones;
- MONITORING: during the runs we'll be interested in a continuous monitoring of the FE channels (mainly the noise levels);
- CALIBRATION: threshold scan, measurements of noise level, DLL calibration;

EXTERNAL (other system are involved)

- TIME ALIGNEMENT: when detector is switched ON after long time we'll need to synchronize the response of the chambers. This procedure requires a tight communication between OffDetectorElectronics and FrontEndElectronics;

VI. The Cosmic Ray Test Station for the LHCb Muon Chamber

A first down scaled implementation of the Control System is now being used and tested to fully manage a cosmic ray station built for the studies of the LHCb MultiWire Proportional Chambers. The cosmic ray stand is able to house 6 MWP chambers and allows the acquisition of as much as 600 Front-End channels. The CS controls high and low voltage supplies as well as the front-end readout devices, stores data regarding the system status and manages the alert and the alarm situations. The CS test is giving a unique possibility to study in details their different features and is an usefull tool to test the robustness of the Muon Detector CS. In the Fig. 8 some of the results of the cosmic ray measurements are reported: a typical time jitter (top) and the time resolution of three chambers as a function of the voltage applied (bottom).

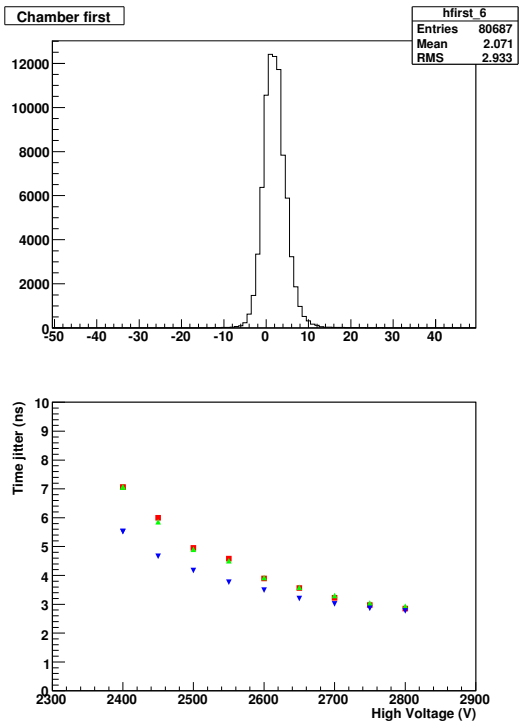

Figure 8: Top: Typical time jitter of a four-gap chamber studied with the cosmic rays. Bottom: Time resolution as a function of the high voltage applied for three types of MWP Chambers

VII. Conclusion

Management of the LHCb Muon Detector requires the monitor and set of many different parameters. Following the recommendation of the CERN Joint Controls Project group, the Finite State Machine architecture was adopted. A Control System in the PVSS FrameWork is being developed. Control Units are created to manage the main System aspects. Usage of the tools developed to manage a Cosmic Ray Station, already in use for tests and performance evaluation of the LHCb Muon Chambers, makes possible to have a fast feedback on the usefullness of the implemented features and to test for robustness of the Control System itself. Routines for calibration and diagnostics of the front-end electronics and for high voltage setting and monitoring have already shown to work very well and result of great importance for the automation of the Muon Detector Control System.

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A compact plug-in module for LHC-like trigger emulation

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Abstract

A compact trigger emulation module for evaluating electronic systems for LHC applications has been built using off-the-shelf components. The emulator, which is based on an FPGA, generates both programmable and true-random trigger patterns in compliance with the LHC triggering rules. For the true-random trigger part, the source of randomness is the avalanche effect on a transistor emitter-base diode. The system can be used either as a plug-in module for VME systems or as a standalone device controlled via a standard USB link by a PC running LabVIEW.

I. Motivation

The need of a flexible device emulating realistically the random arrival of particles on a detector is apparent, especially during the construction/testing phases of the corresponding on and off-detector electronic systems. Having the ability to define certain parameters such as the mean rate and the distribution of the randomly generated trigger signals would make such a device extremely useful. Additionally, if the device could be portable and work in stand-alone mode, it would make it even more attractive. All these led to the development of a compact plug-in trigger emulator module based on a source of true randomness.

Such a device, apart from being useful for High Energy Physics experiments, is also suitable for nuclear physics and radiology experiments where the emission of a radioactive source needs to be emulated.

II. Hardware Implementation

The trigger emulator plug-in module is based on an FPGA and a random noise generation circuitry. The circuitry that forms the random generator produces pulses with random intervals. The source of randomness is the avalanche effect on a transistor emitter-base diode, biased by a digitally controlled voltage source.

Figure 1 illustrates the schematic of the random number generator. The transistor on the left side of the schematic is the avalanche noise generator. The output is amplified by a two-stage transistor amplifier. The amplified noise signal is superimposed on a configurable DC level (created by a digital potentiometer) and it is fed to an FPGA internal gate which acts as a comparator and produces random transitions. The programmable voltage source on the left side of the schematic controls the biasing of the transistor emitter-base diode, changing in this way the mean value of the distribution. Figure 2 displays the distribution of 1024 random triggers generated by the emulator, where the solid curve is an exponential fit to the histogram.

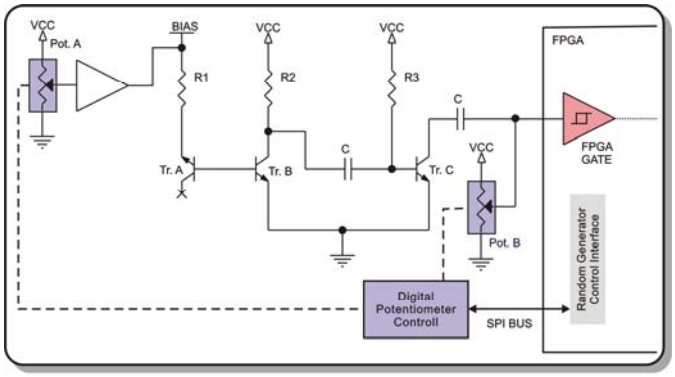

Figure 1: Schematic of the true random interval generator.

The output of the random generator is treated by a digital processing circuitry implemented in an FPGA. Its principal function is to measure the time intervals between the transitions generated at the output of the logic gate extracting in this way random numbers. Additionally it applies specific rules and functionality depending on the application (details of the functionality can be found in section III). Finally the FPGA provides the necessary communication interface for setting the desired working parameters. The module includes also an optical transceiver for inter-connection with the various off-detector electronic systems.

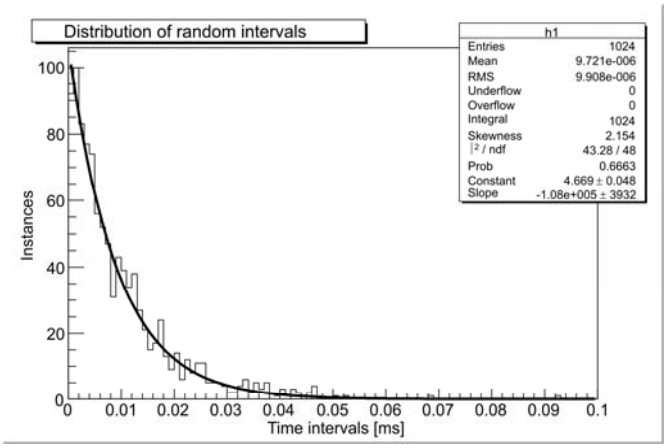

Figure 2: The exponential distribution of 1024 generated true random trigger intervals with mean rate ~100 KHz.

This compact module (12.3cm x 4cm x 1.2cm) can be plugged as a mezzanine on various readout systems i.e. VME64 [1] but it can also work as a stand-alone device with the help of a support board that provides the necessary power and a USB interface in order to communicate with a standard PC. The support board can be viewed in figure 4.

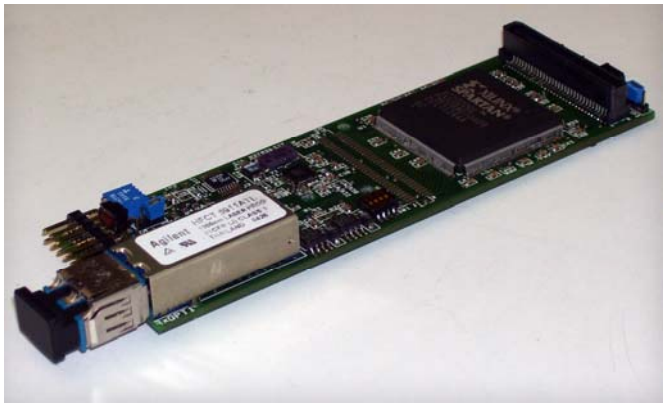

Figure 3: The trigger emulator plug-in module. On the left, the optical transceiver is shown while on the right, the FPGA and the mezzanine connector.

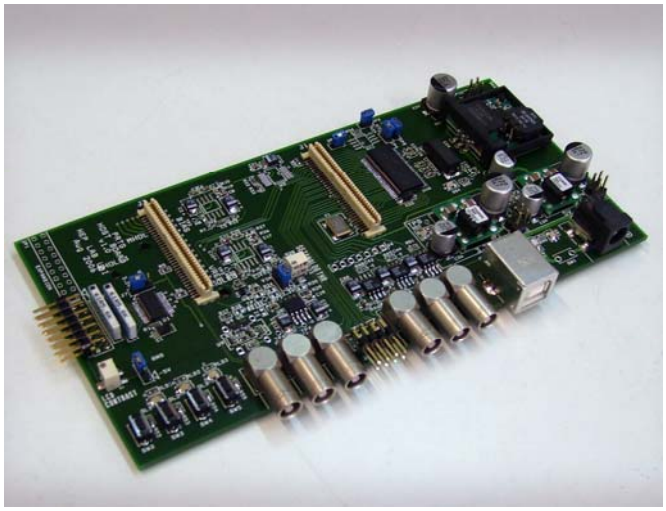

Figure 4: Photograph of the support board that provides power, additional clock, JTAG and USB interface to the trigger emulator mezzanine, used for evaluation purposes.

III. FUNCTIONALITY

The purpose of the trigger emulator is to generate sequences of trigger signals (trigger patterns) either based on the random number generator or on user defined parameters. In addition it can provide other timing and fast command information (clock signal, resynchronization signal etc) to the front-end (on-detector) system in a programmable way in order to facilitate various system tests. The 40.08MHz clock signal used in all LHC systems, is produced locally by a QPLL [2] ASIC configured as a local oscillator using a 160.32MHz quartz[1] [3] as a reference. Using the 40.08MHz clock, the triggering emulator generates four encoded fast commands as described in table 1.

[1] This quartz has been specially produced for LHC applications.

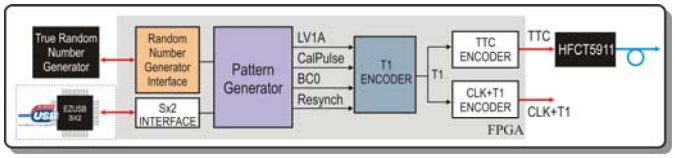

Figure 5: Block diagram of the functionality of the emulator.

The encoding scheme used (called "T1" [4]) is a 3-bit pattern, thus it requires 3 clock cycles to be transmitted serially. The first bit of the pattern is always '1' denoting the existence of a fast command and the remainder denotes which of the four fast commands is being transmitted ("00"=LV1A, "01"=BC0, "10"=Resynch, "11"= CalPulse).

The trigger emulator is developed in such way that it can generate bursts of triggers by specifying the time between consecutive triggers expressed as a number of clock cycles. Figure 6 shows how a burst of (one clock cycle width) pulses can be defined by a sequence of numbers (t1, t2, t3 … tN).

The implementation of the burst generator is based on a RAM, where the values t1, t2, t3 etc are stored. Firstly, the address pointer is reset and therefore the first value stored in the RAM (t1) appears at its output. This value is then loaded to a decrementing counter. When the counter reaches zero, the terminal count output is asserted. At the same time the address pointer of the RAM is incremented providing the next value (t2) to the decrementing counter and so on. Figure 7 shows a simplified block diagram of a burst generator based on a RAM.

The trigger emulator comprises four identical stages, one per fast command. From the four identical stages, only the one associated with the trigger generation can either be loaded from the true random number generator or defined by the user. The user has the option to mask any of the four generated fast commands.

Table 1: The encoding of the four fast commands.

Name	Description	Priority	Encoding
Resynch	Soft reset of the front-end chips	1 (high)	110
BC0	Bunch crossing zero	2	101
CalPulse	generate internal injection pulses	3	111
LV1A	Level 1 Trigger Accept	4 (low)	100

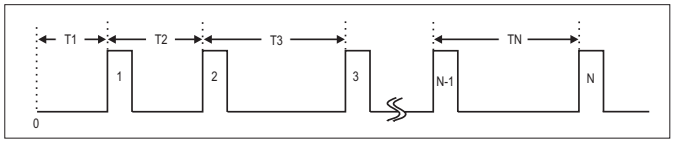

Figure 6: Programmable or random burst.

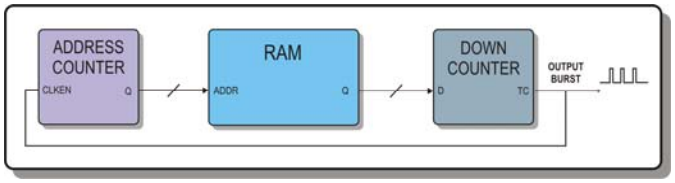

Figure 7: Programmable burst generation.

The trigger emulator is able to generate bursts of up to 1024 triggers. The time between two consecutive pulses can be between 3 and 2^{32} clock cycles[2]. If the user wishes to generate bursts with N<1024 triggers, he can set the end of the burst by writing a zero (or an illegal) value to address N of the RAM.

It is worth mentioning that the emulator includes a machine that emulates the Proton and Ion bunch disposition at LHC [5]. Where there is supposed to be a gap in the disposition, the machine suppresses the (random or programmable) output of the trigger pattern generator.

The fast commands generated need to be encoded properly in order to be transmitted to the front-end electronics. Prior to the fast command encoder, a state machine is introduced to ensure the respect of the fast command priority. The encoding and priority of the signals can also be found in table 1. After the selection of the command with the higher priority, its encoding follows, as described in table 1.

In order to minimize the necessary connections for the transmission of the clock and the T1 information, an additional encoding combines the two signals into a single one. The trigger emulator implements two different methods of combining the clock encoding and the T1 information. The first method ("CLK+T1" [4]) combines the two signals by removing a pulse from the clock signal whenever the T1 signal is '1'. This is the encoding scheme used by the CMS Tracker front-end control chipset [6] and adopted by other sub-detectors. The second encoding method is based on a 160.32 MBaud bi-phase mark encoder with time-division, which multiplexes 2 channels using a balanced DC-free code. This encoding scheme is fully compatible with the scheme used for the CMS TTC system [7], although channel B which normally transmits broadcast and individually-addressed commands is currently not used. Figure 8 illustrates the TTC-like encoder implemented in the emulator.

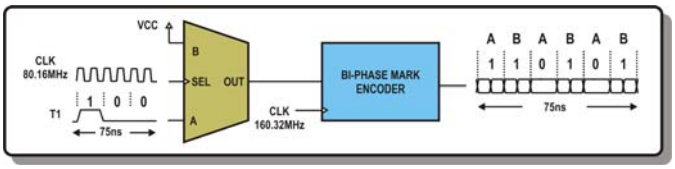

Figure 8: TTC encoding.

IV. User interface

The trigger emulator comes with a LabVIEW [8] user's interface when it works in stand-alone mode. This LabVIEW interface allows the user to define the working parameters (such as desired mean rate, number of triggers etc) of the functionality discussed in section III. The LabVIEW application includes among others, a graphical display of the fast timing signals generated by the emulator. It is worth mentioning that the application developed is compatible with both Windows and Linux operating systems.

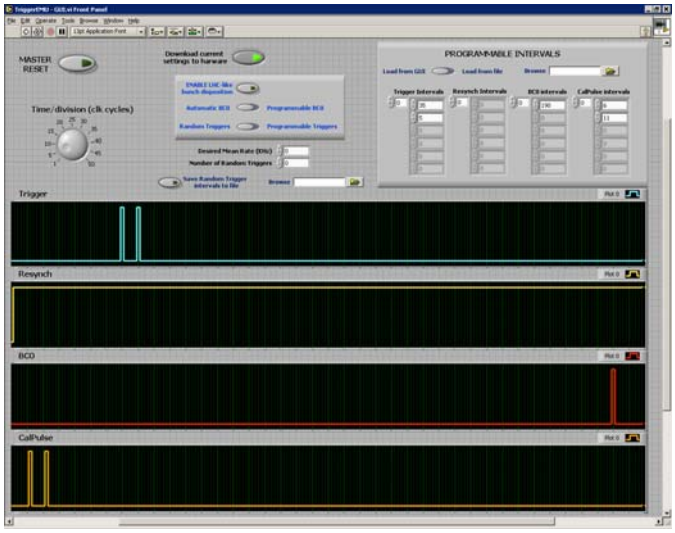

Figure 9: The front panel of the emulator's LabVIEW interface.

V. Summary and conclusion

A plug-in module able to emulate trigger and fast commands for LHC applications was built. The most important feature of this device is the ability to produce trigger patterns based on true random number generation. The source of randomness is the avalanche effect on a transistor emitter-base diode, biased by a digitally controlled voltage source.

The emulator produces randomly generated trigger pulses with time intervals following an exponential distribution with programmable mean between 1 KHz and 1 MHz (trigger rate). Therefore it can be used in emulating the arrival of particles on a detector enabling this way the testing of the corresponding on and off-detector electronic systems.

The device can either be used as a mezzanine card on various systems (VME based systems) or in stand alone mode controlled by a PC running LabVIEW.

Such a device, apart from being useful for High Energy Physics experiments, is also suitable for nuclear physics and radiology experiments where the emission of a radioactive source needs to be emulated.

VI. Acknowledgements

This work was partially supported by the Greek General Secretariat of Research and Technology and was co-funded by the European Union in the framework of the program "Heraklitos" of the "Operational Program for Education and Initial Vocational Training" of the 3rd Community Support Framework of the Hellenic Ministry of Education, funded by 25% from national sources and by 75% from the European Social Fund (ESF).

[2] In the case of CMS, values less than 3 are considered as illegal because the CMS trigger rules define that 3 LHC-clock cycles is the minimum time between two consecutive LV1A commands.

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High-Density Backplanes: Problems and Solutions

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Abstract

The backplane and crate infrastructure for the digital processors of the ATLAS Level-1 Calorimeter Trigger (L1Calo) are presented, The L1Calo system is a compact, high-performance real-time system based on a custom, monolithic 9U backplane populated almost completely with 2mm Hard Metric connectors.

The high pin count and monolithic design present challenges including high insertion/extraction forces, and maintenance and repair over the lifetime of LHC. We have developed solutions for these issues, as well as providing infrastructure for power distribution and cable strain relief, while maintaining accessibility,

I. Introduction

Real-time systems developed for LHC typically require high channel density and interconnectivity between modules. To achieve these goals, most system designers use 2mm Hard Metric (HM) connector systems to provide the desired pin counts. 2mm HM connectors introduce new problems for system designers. With insertion forces of up to 0.75N per pin, a 9U module requires hundreds of Newtons to insert or remove. Exposed male backplane pins are easily bent and damaged, presenting serious long-term maintenance issues over the lifetime of LHC. Crate infrastructure and power distribution must be designed to allow maximum accessibility for maintenance.

The ATLAS Level-1 Calorimeter Trigger [1] uses a common system-crate architecture for the EM/τ cluster and Jet/Energy-sum processor subsystems based on a custom monolithic backplane with very high signal density. This architecture has required us to address these issues by developing integrated solutions for force reduction, cable strain relief and power distribution that provide maximal access for testing as well as long-term maintenance and repair.

II. Backplane and Crate

The processor backplane (Figure 1) is a monolithic construction with 9U height and 21 single-width module positions. It is populated almost entirely with 2mm HM connectors, with 1148 signal and ground pins to each processor module. The PCB is 4.9mm thick, with 8 signal layers and 10 ground planes, Up to 384 serial LVDS cable assemblies, plus two rear transition modules for system merger cables, are connected to the rear side of the backplane. Three high-current DIN connector pins at the bottom of each module position deliver up to 20A of low-voltage (3.3V and 5V) current.

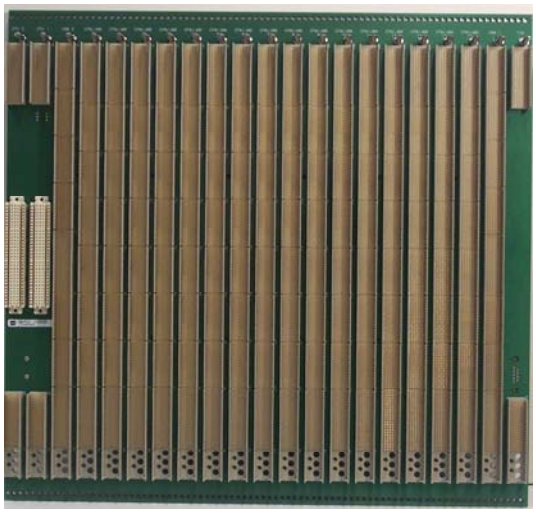

Figure 1: Front view of processor backplane.

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The backplane is installed in CERN-standard Series 6000 LHC crates [2]. This allows us to use standard solutions for power, cooling and crate control. Because our backplane is nonstandard, however, certain modifications have been made including longer power cables, a custom sense-wire assembly and card guides for two small daughter modules in the rear.

III. Mating Forces

With 1148 signal and ground pins per module position, the nominal insertion force for a typical module is nearly 500N, and the extraction force over 400N. Without reinforcement the backplane PCB bows horizontally during insertion/extraction. The resulting pin misalignment adds dramatically to the mating forces.

Each backplane is equipped with six vertical reinforcement ribs (Figure 2). They are made of 5mm thick brass, fitting exactly in the gap between two module positions, and are 2 cm deep. They are bolted to the top and bottom crate extrusions through the backplane's mounting holes, and secured directly to the backplane at 1/3 and 2/3 of the backplane's height to prevent bowing during extraction. This configuration reduces the maximum movement of the backplane to less than 1mm. Threaded mounting points on the back of the ribs provide support for the power bus bars and cable strain-relief system (Figure 3).

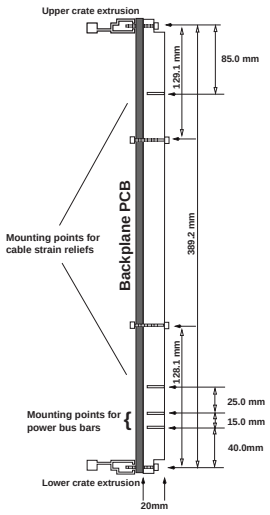

Figure 2: Mechanical sketch of vertical reinforcement ribs.

Handles manufactured to IEEE 1101.10 specifications [3] apply leverage against special front crate extrusions to provide the high insertion/extraction forces necessary. We have observed that these extrusions bow vertically from the force of the handles, which causes the handles to lose their grip and causes excessive wear on both the handles and extrusions. We have addressed the handle wear issue by using solid aluminum handles for the final production modules [4]. Extrusion flexing can be reduced by regularly securing module front panels to the extrusions, providing vertical reinforcement during insertion/extraction of nearby modules.

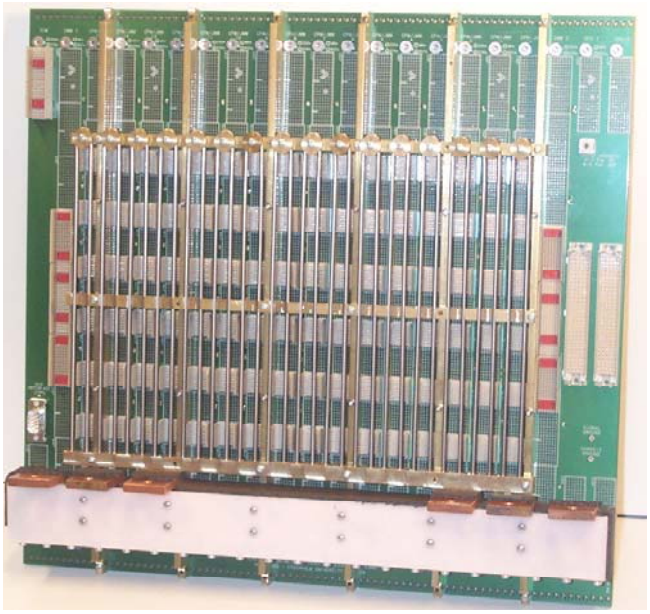

Figure 3: Rear view of the processor backplane, including the reinforcement ribs, cable strain reliefs and power bus bars.

Finally, guide pins on each module [5] ensure correct alignment during mating. This reduces the force of initial contact, and protects the pins from damage through misalignment.

IV. Services

The backplane reinforcement system also serves as a mounting point for the cable strain relief system and the power distribution bus bars.

The cable strain relief system provides secure retention for up to 384 4-pair LVDS serial cable assemblies that provide the processor modules with input data. Vertical "forks" straddle the cables at each module position, and secure the connectors within the connector shrouds.

A robust power bus bar assembly of 6mm copper is mounted at the bottom of the backplane and distributes 5V and 3.3V power to each of the 21 modules through three high current pins [6] rated at 20A each. The ground pins are make-first break-last to minimize the risk from an accidental live extraction.

V. Maintenance and Repair

When signal pins become damaged, a repair and replacement procedure is critical. Tyco/AMP produces a toolkit [7] that we have successfully used for field replacement of single connector pins, without removing the backplane from the crate. This kit works best for AMP brand connectors, whose pins are loaded into the front of the shroud and held in place by friction. Other connector brands such as ERNI are less suitable for field repair, since the pins are loaded from the back of the shroud, and are therefore less easily extracted. Nevertheless we have also succeeded in replacing several ERNI pins with the AMP toolkit with satisfactory results.

For more extensive damage the backplane should be removed from the system and entire connectors replaced, usually by an external company. The backplane and its hardware are assembled as a single unit that can be relatively easily removed and replaced for this purpose.

VI. Conclusion

The performance requirements for the Level-1 Calorimeter Trigger led us to design a system backplane with high signal density and pin counts. We have successfully developed solutions for reducing and dealing with mating forces, providing power distribution and cable support, and long-term maintenance. It is hoped that our experiences and solutions may be useful in future high-density systems..

VII. References

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Development and Test Results of a Readout Chip for the GERDA Experiment

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Abstract

This paper describes the F-CSA104 architecture and its measurement results. The F-CSA104 is for γ spectroscopy with Ge detectors. It is a low noise, fully integrated, four channel XFAB 0.6µm CMOS technology ASIC, that has been developed for the GERDA experiment. Each channel contains a charge sensitive preamplifier (CSA) followed by a 11.7MHz differential line driver. It has been particularly designed to operate in liquid argon (T = 87K/-186°C) and to have a measuring sensitivity of 660e^- with an ENC of 110e^-, after offline filtering with 10µs shaping, when connected to a 30pF load. Special techniques are used to improve the SNR such as a large input PMOS FET, an integrated 500MΩ CSA feedback resistor and a noise degeneration drain resistor.

I. INTRODUCTION

The GERmanium Dectector Array (GERDA) experiment [1] under construction at the Lab**Error! Reference source not found.**oratori Nazionali del Gran Sasso (LNGS) is searching for neutrinoless double beta (0νββ) decay of ^{76}Ge. Isotopically enriched Germanium diodes, suspended in a 70m^3 liquid argon (LAr) cryostat, serve as sources and detectors (330e^- per keV energy deposition). The LAr cryostat is immersed in a 630m^3 water tank that acts as a neutron moderator and Čerenkov medium. Since the detectors are operated in an unprecedented low background environment the analog amplifiers, which are operated close to the diodes in LAr, have to fulfill stringent requirements on low radioactivity, noise performance and be able to drive the signal off detector. The F-CSA104, alias Gulinbursti, has been designed by FBE ASIC Design & Consulting to fulfill these requirements by an appropriate technology choice and optimised architecture. The following sections outline the required detector electronic specifications and the F-CSA104 chip architecture, gives details of a few critical F-CSA104 circuit blocks, and presents measured performance results from the chip in both room and LAr temperatures.

II. DETECTOR ELECTRONIC SPECIFICATIONS

- Operating temperature 77K (- 196°C).
- Fully integrated system.
- Low power, no bubbling of the LAr. 50mW/channel.
- Differential voltage output to drive 10m of twisted pair cable.
- Total gain 277mV/MeV (5.1mV/fC).
- Measuring sensitivity 2keV (660e^-).
- Dynamic range 5keV - 10MeV.
- Amplifier output rise time < 30 ns.
- System linearity will fit to a 14-bit ADC.
- ENC 110e^- at 30pF load, cold.
- Approximately 300 channels in total.
- 0νββ event rate <10 per year.
- Background in the sub Hz range.
- Detector signal rise time in the order of 300ns.

III. F-CSA104 ARCHITECTURE

The F-CSA104[1] has been fabricated in the XFAB 0.6µm

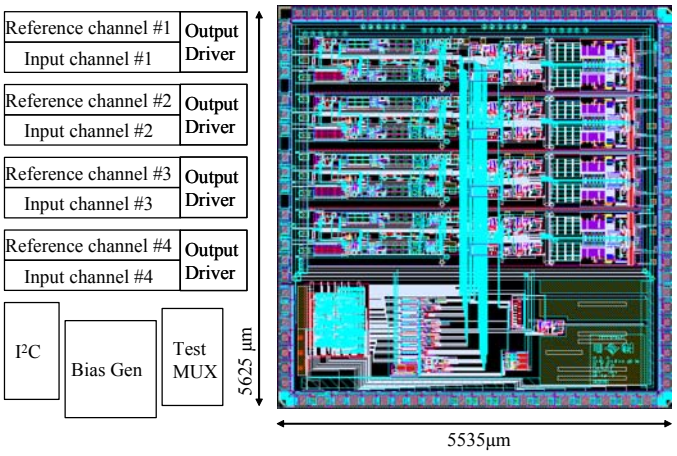

Figure 1: The F-CSA104 Floor plan & Layout.

5V CMOS process as it offers a large signal output voltage swing, substrate isolated NMOS and PMOS FET devices that

[1] The data sheet can be found at http://www.fbe-asic.com/solutions/assp/f-csa104.html

allow an improved noise immunity and, most importantly, do not exhibit bulk effect, which in combination with low temperatures causes prohibitory large changes in the threshold voltages. Figure 1 shows the F-CSA104 floor plan and layout. Each of the four input channels has, except for the scaled-down input FET and unity gain, an identical reference channel for DC subtraction.

Figure 2 shows the F-CSA104 block diagram. Charge delivered by a semiconductor detector is collected and amplified by the CSA. Its output voltage V_{out} is given by $V_{out} = q/C_{fb}$, where q is the charge delivered to the input and C_{fb} is the feedback capacitance (1pF after calibration).

A range of F-CSA104's parameters (all having room temperature start-up defaults pre-programmed), including offset and the CSA decay constant, can be programmed via I^2C commands for optimisation. Further to this, several options exist to select various reference points for sensitive nodes. An example of this would be the bulk node, labeled as BULK_EXT in Figure 2, of the input transistor which can be selected to the external bulk or the quiet ground point. The linearity and offset have been designed for use with 14 bit ADC systems. The high current differential line drivers allow for directly driving a 100Ω twisted pair cable over 10m.

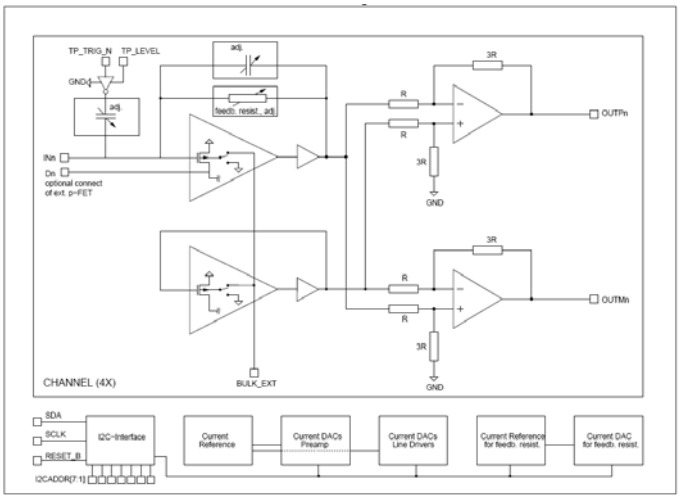

Figure 2: The F-CSA104 Block Diagram.

The internal current source has been designed to be insensitive to -200°C to +50°C temperature variations. Circuit biasing is achieved with 5-bit binary weighted current DACs utilising the current reference, followed by multiple current buffers for on-chip distribution. An internal test pulse circuit has been incorporated to allow functionality tests.

A. Integrated feed back resistor (Rfb)

A feedback resistor sets the DC operating point of the CSA, thus preventing it from going into saturation as a consequence of leakage current or high rate input pulses. For best noise performance, the feedback resistor should be as large as possible. However, this is limited by the need to avoid the CSA saturation just discussed. So as to cater for numerous input pulse rates, it is therefore desirable to untilise a wide-ranging-variable resistor for noise optimization.

It is advantageous to have a completely integrated circuit. Measurements have shown that the use of discrete components within the cryogenic vessel greatly reduce the radio-purity. For example, external components such as a carbon resistor for Rfb typically have in the order of 100 times more radioactive impurities than its integrated counterpart. However, integrating such a large resistor required the use of a substrate isolated NMOS (NMOSi) FET operating in the sub-threshold region. The resistance is adjustable from 1MΩ to 1.7GΩ.

Special electronic circuitry and layout has been used to allow the NMOSi FET resistor, labeled Rfb in Figure 3, to work in the sub-threshold region for both signal input polarities, selectable or autonomously, and to maintain a reasonably accurate and stable resistance. Sub-threshold FET operation is now briefly discussed.

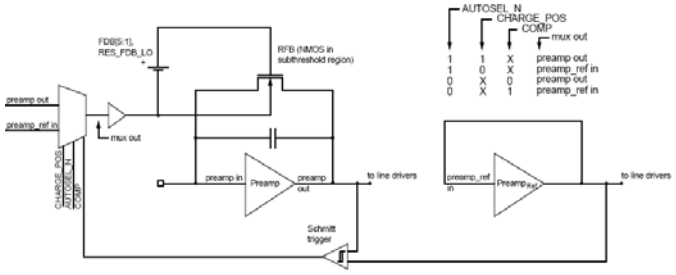

Figure 3: The NMOSi FET Feedback Resistor.

When $V_{GS} < V_{th}$, where V_{th} is the threshold voltage of the device, according to the threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a sub-threshold current that is an exponential function of gate-source voltage and is given as [2]

$$I_d \alpha \exp\left(\frac{V_{GS}}{n.V_T}\right), \qquad Equ\ 1$$

where V_T is the temperature voltage derived from $V_T = (k.T/q)$, k is the Boltzmann constant, T the absolute temperature, and q the electron charge. The slope of the line is named 'sub-threshold slope' with the symbol n. From *Equ 1* it is clear that a stable V_{GS} is required. Furthermore, as the FET-channel conduction due to V_{GS} also has a dependency on the voltage between the source terminal and the bulk (V_{sb}), a stable and constant V_{sb} is also called for. How this is achieved in hardware is now described.

Referring to Figure 3, the very small value of V_{GS} needed to keep Rfb in the sub-threshold region is generated by a current mirror diode-connected configuration, which is a 10-times scaled version of Rfb. Both FET devices are within the same bulk area for better device matching. To maintain a fixed Rfb resistive value, tracking circuitry connected controlling the feedback MUX ensures that, in the case of positive input polarity operation, both NMOS bulk and gate voltage follow the negative going CSA output pulse, while N-tub has a fixed reference value. This ensures that V_{GS} and V_{sb} of Rfb remains a constant value. For negative input polarity, the N-tub tracks while the P-tub has the fixed reference.

B. Input transistor

The F-CSA104's noise performance has been optimized for use with detectors having a load capacitance of 0 - 100pF. Measurements have shown that the PMOS input transistor suffered less flicker noise than that of an NMOS **[3]**; Flicker noise being an important noise contributor at LAr temperatures. The total series voltage noise (e_n^2) for the input FET is **[4]**

$$e_n^2 = \frac{K_f}{C_{ox}^2 WLf} + \frac{8}{3}kT\frac{1}{g_m}, \qquad Equ\,2$$

where C_{ox} is the capacitance between the gate and the conduction channel, K_f is the flicker noise coefficient, WL are the FET width and length dimensions respectively, f is frequency in Hz, k is the Boltzmann constant, T is the temperature in Kelvin, and g_m is the transconductance given by $g_m = \sqrt{2k'(W/L)}.\sqrt{I_D}$, with k' being the process conduction parameter. The total parallel current noise source (i_n^2) representing shot noise is negligible for a FET device and is not discussed further. The first term in Equ 2 represents the flicker noise of the input transistor and the last term represents the input transistor channel thermal noise. It is clear that both flicker and thermal noise can be reduced by utilising a large width over length input FET. In this case a

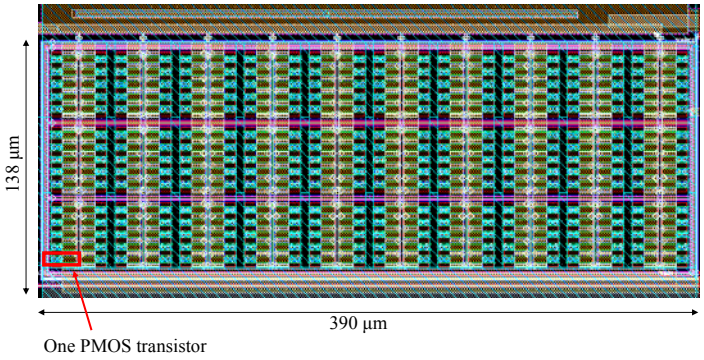

Figure 4: The NMOSi input FET.

PMOS input transistor channel of 9000/0.6 has been implemented using 600 parallel FET devices, see Figure 4. Special layout techniques have been used to reduce the stray capacitance and to screen the input line from bulk noise. So as the F-CSA104 may find use in other applications where the noise matching to higher capacitance detectors is vital, an external PMOS or a p-channel JFET may be connected to the IC and thus operates in place of the integrated input transistor, refer to the Dn input node of Figure 2.

C. Source degeneration resistor

Figure 5 shows a conceptual view of the input stage of the CSA. In principle it is of the folded cascade type, M1 being the large W/L input transistor just discussed in section B, M4 is operating as a constant current source, M3 is in a common gate configuration, M2 is the active load resistor of M3 and R1 is the degeneration resistor, the reason for its use is now given.

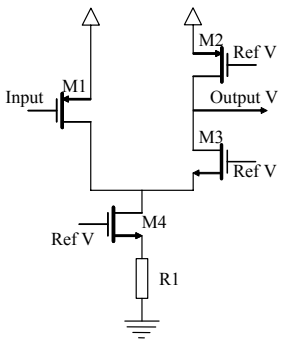

Figure 5: Conceptual view of the input stage.

In this configuration, neglecting other noise sources, the thermal channel noise current of M4 adds directly to M1 and can be written as **[5]**

$$i_n^2 = 4kT\gamma_1 g_{m1} + 4kT\gamma_4 g_{m4}, \qquad Equ\,3$$

where g_m is the transconductance and γ is a complex function of the basic transistor and bias conditions. In this case M4 carries the largest current, being the sum of both branches of the circuit, and its noise current can contribute a noticeable portion to the overall noise figure. One way to reduce its g_{m4} transconductance is to choose a small M4 W/L aspect ratio, but this is at the cost of a required increase in V_{GS}, which limits the dynamic range of the circuit. A better method is to 'degenerate' M4 by adding the resistor R1 in series with the source of M4. The thermal channel noise current of the M4 tail can now be written as **[5]**

$$i_{n(tail)}^2 = 4kT\frac{1}{R1} + \left(\frac{\frac{1}{g_{m4}}}{\frac{1}{g_{m4}} + R1}\right)^2 4kT\gamma_4 g_{m4}. \qquad Equ\,4$$

In the case of F-CSA104 the optimum R1 resistor value was found to be 200Ω giving, from simulation, in the order of a 20% reduction in the noise contribution. Care has to be taken of the R value selected to ensure that its own thermal noise does not significantly contribute.

D. Internal current source

A new compact, high precision, temperature-compensated, all-MOS current reference has been designed to allow the chip to work in both room and LAr temperatures. Its principle design and operation is given in the paper 'Compact temperature-compensated CMOS current reference' **[6]**. The paper discusses a second order temperature compensation obtained with a temperature-dependent current ratio using a MOS inverse Widlar current mirror. In this case the operating range is -30°C to +100°C. For the F-CSA104 the design has been enhanced to operate in the range of -200°C to +50°C with an expected mean temperature drift of 28 ppm/°C.

E. Offline filtering

The signal of the preamplifier will be digitized with a sampling rate of typically 100 MHz, enough to allow for detailed pulse shape analysis of the rising edge of signals from large germanium detectors, which have in the order of a 300ns rise time. A digital filter implementing a RC-(CR)^n network with optimised shaping times of typically 10µs reduces the noise to the design value. The limitation of such a filter is to be able to cut off the low frequency noise while maintaining the broad spectrum range from the input pulse.

IV. Measured Performance Results

The F-CSA104's preliminary measured noise, signal output rise and fall times, linearity, gain and feedback resistor values are given for both room and LAr operating temperatures. Figure 6 shows a photograph of the test set-up. The F-CSA104 is mounted on, for LAr operation reasons, a flexible kapton PCB. The board has the option of supply filtering, which will ideally not be the case for the experiment. However, for laboratory testing it is a necessity. For test charge input, there exists a 15:1 resistor attenuation network that couples into a series capacitor, nominal value of 1.5pF. A surface mounted capacitor emulates the load capacitance of

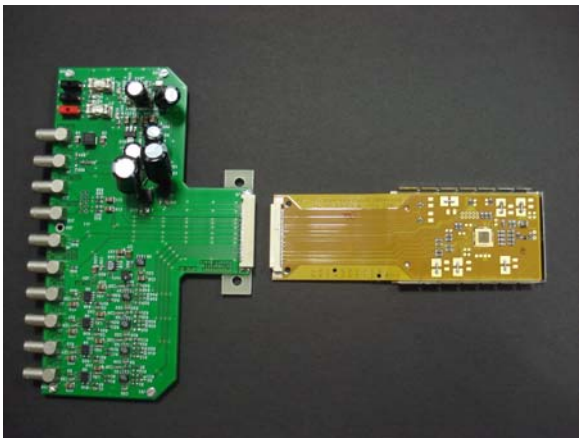

Figure 6: Photograph of the test set-up.

the diode detector. The flexible PCB can be connected to the receiver board, shown on the left side, either directly or via a 10m cable. The receiver board utilizes LM317EMP and LM317EMP voltage regulators, and 270MHz AD8130AR differential receiver amplifiers.

A. F-CSA104 resistor feedback

The measured value of the feedback resistor, discussed earlier in section II-A, has been extracted from the relationship between the amplifiers bandwidth and its feedback time constant using $R = \frac{T_{r(10-90)}}{2\pi 0.35.C}$, where C is the feedback capacitance of 1pF, after calibration. It should be noted that the amplifier's discharge slope is signal dependent and therefore only obeys a *RC* discharge curve for small input signals, but has a constant-rate discharge for larger signals. There are two modes of Rfb adjustment, the first is a fine-resolution step over the range of 10MΩ, and the second is a coarse-resolution step ranging 1.7GΩ. Figure 7 and 8, coarse and fine resolution step, respectively, are plots of *Rfb resistance vs. the resistor-select register*, for both simulation and hot/cold measurements. The input signal was ~500keV.

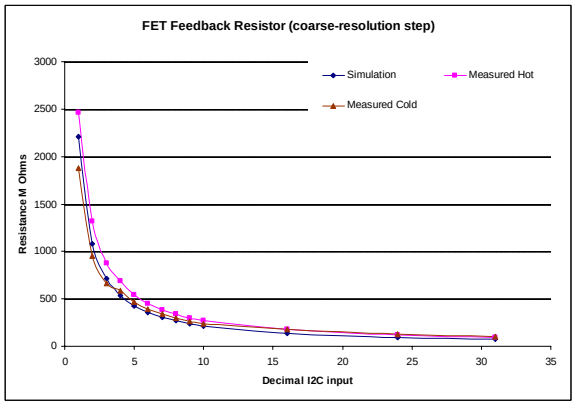

Figure 7: *R vs. coarse-resolution Rfb step settings.*

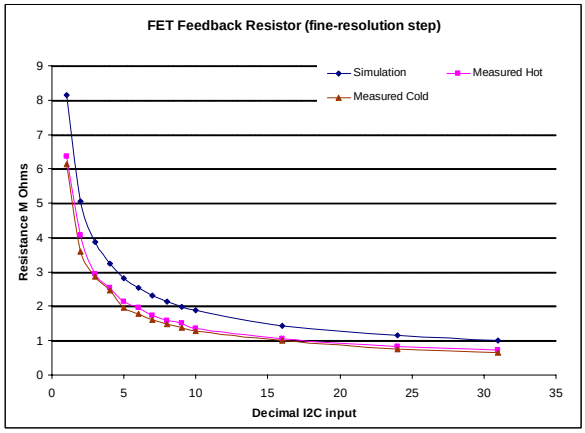

Figure 8: *R vs. fine-resolution Rfb step settings.*

As is clearly seen from these results the measured value of Rfb matches simulation well, and is only slightly effected by LAr temperature operation.

B. Noise measurements

For the preliminary noise measurements, the kapton flexible PCB had power supply filtering added, and the two boards shown in Figure 6 were directly coupled together. However, the differential receiver amplifiers were bypassed to eliminate their noise contribution. The output of each channel was shaped with a 20µs RC-(CR)^4 in-house-built filter and sampled by an 8-bit TDS784D oscilloscope. The oscilloscope took 5000 samples at 2.5Ms/s. To aid the removal of common mode noise, two of the channels were subtracted from each other and the single channel noise contribution was found from

$$\sigma = \frac{\sigma(Ch_A - Ch_B)}{\sqrt{2}}, \qquad Equ\,5$$

Where σ = *RMS* of scope voltage. The noise of the oscilloscope, approximately 20e$^-$, was also accounted for. The Equivalent Noise Charge (ENC) vs load capacitance is shown in Figure 9.

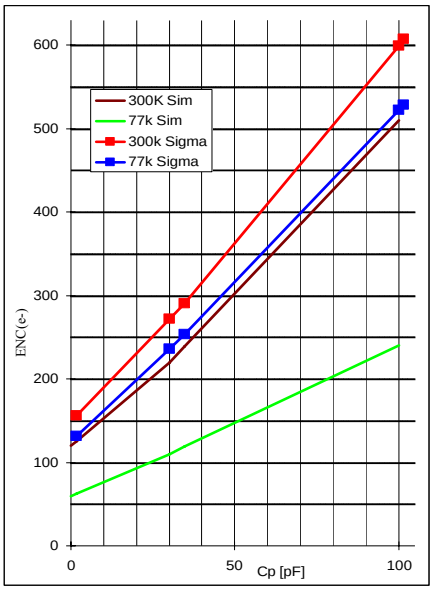

Figure 9: *ENC vs. load capacitance* noise plots.

The results for room temperature are in reasonable agreement with the simulation. However, there is evidence that this measurement is degraded due to a correlated source on the sensitive ground line. For the LAr operating temperature the result falls short of the GERDA requirements, but in this case it is plausible that the correlated source degrades the results more apparently then for the room temperature measurement. It is clear that the CMRR of the measuring circuit needs to be improved.

C. Output signal rise times

The output rise times for 10-90% have been measured with 33pF and 100pF, for both hot and cold conditions. The charge input was 22fC and Rfb set at ~100MΩ. The results are given in table 1.

Load capacitance fF	Rt_{cold} ns	Rt_{hot} ns
33	10	18
100	12	24

Table 1: Output rise time.

D. Linearity and gain

Figure 10 shows a plot of Non-Linearity (*NL*) *vs.* amplifier charge input. For the measurement of the extremely demanding linearity requirement of 0.006% a Total Harmonic Distortion + Noise (THD+N) method is utilised. THD of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental. THD+N means THD plus noise. This is measured by inputting a sine wave and measuring both the input signal and output signal with a spectrum analyser; without shaping. In this way the proportion of *NL* relative to each output signal can be given. The circuitry resembles the IEEE standard **[7]**.

The red horizontal line in Figure 10 indicates the 0.006% requirement. The first measured point on the plot at q_{in}=0.6x10^{-18}C is the measured output without any input charge signal. The results show that the chips *NL* is less than the 0.006% limit for q_{in} above 5fC. Below this the noise

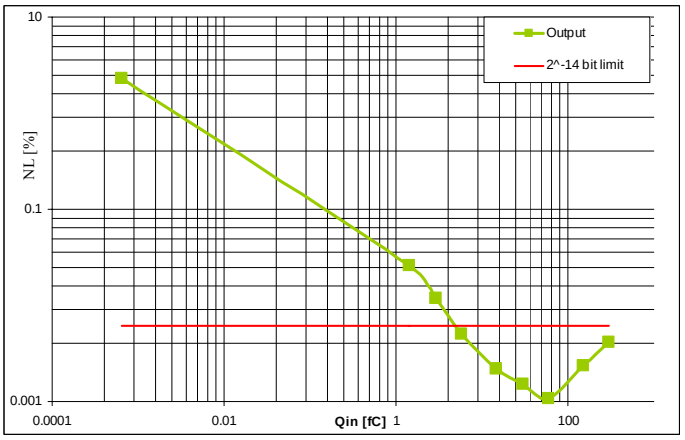

Figure 10: V_{out} *vs.* q_{in} linearity plot.

limits the measurement. One plausible explanation for the upward trend seen for input charge above 60fC is a *NL* contribution from the NMOSi feedback resistor Rfb. The measured gain is 4.75mV/fC.

V. Summary And Future Work

A four channel fully integrated low noise CSA for operation in the GERDA LAr cryogenic chamber, has been successfully designed, fabricated and tested. It is expected that the ENC noise figures will improve once the source of the correlated noise has been found and removed. The stability and dynamic resistive range of Rfb is better than the temperature limited simulation models predicted. Furthermore, its stability at very large resistor values, for both hot and cold operation, is testament to how well the constant current source behaves. The current source, full dynamic linearity, all bias nodes, the supply rejection ratio, along with all the other standard data-sheet measurements, will be fully evaluated in the near future.

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Preamplifier-shaper prototype for the Fast Transition Detector of the Compressed Baryonic Matter (CBM) experiment at FAIR

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Abstract

In this work a preamplifier-shaper prototype for the Fast Transition Detector of the Compressed Baryonic Matter (CBM) experiment at FAIR fabricated using a 0.35 μm CMOS technology will be presented. The ASIC integrates 16 identical Charge Sensitive Amplifiers (CSA) followed by a Pole-Zero network, two bridged-T filters, Common-Mode FeedBack (CMFB) network and two non-inverting level shifting stages. The circuit is optimized for a detector capacitance C_d of (5-10)pF. Measurement results confirm the noise of 330 e^- + 12 e^-/pF obtained in simulations for a pulse with a Full Width Half Maximum (FWHM) of 71 ns. The circuit recovers to the baseline within 200 ns. The conversion gain is 12.64 mV/fC. An integral nonlinearity of 0.7% is also achieved. The maximum output swing is 2 V. The power consumption is 16 mW/channel where the main contributors are the input transistor and the level shifting stage with 5.3 mW and 6.6 mW, respectively. The total area of the chip is 12 mm^2. Although the circuit was designed for a positive input charge it has in addition the ability of handling negative current pulses of about 85% of the typical charge of 165 fC without any degradation of the signal. The chip was submitted for manufacturing in AMS's C35B4M3 0.35 micron CMOS technology in October 2005. This circuit has been successfully used in the CBM test-beam at GSI Darmstadt in February 2006.

I. Introduction

The CBM experiment is a dedicated fix target heavy-ion experiment for the future accelerator Facility for Antiproton and Ion Research (FAIR). The major experimental challenges are posed by the extremely high reactions rates of up to 10^7 events/s. These conditions require unprecedented detector performance concerning speed and radiation hardness. The high reactions rates require electronics with fast shaping time. A Fast Transition Radiation detector will be part of the CBM experiment. A sketch of the proposed CBM experiment is shown in Figure I.. The setup will measure both hadron and electrons with large acceptance up to beam energies of about 40 GeV/u following a new concept [1].

In the field of radiation detectors a fundamental role is played by the analogue front-end, which is responsible for the signals generated by the detector to the digitization circuitry and for optimizing the signal to noise ratio. In many cases the measured quantity is the energy deposited by each ionizing particle or photon. This is usually accomplished by measuring the amplitude of the electrical pulses generated by the detector. After a first low-noise preamplifier a second stage is needed to filter as much noise as possible while preserving the useful information. This function, along with an additional amplification, is accomplished by the shaping amplifier. A unipolar filter is needed for an optimum measurement of the pulse amplitude that carries the information of the incident energy.

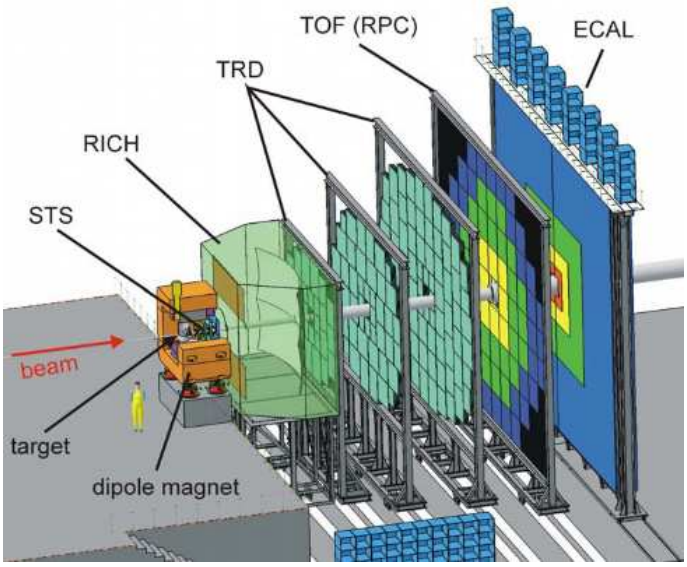

Figure 1: Sketch of the proposed experimental setup for the CBM experiment. The beam enters from the left hand side. The Fast TRD detector is shown as the light blue part.

II. CBM Preamplifier-shaper overview

A block diagram of the preamplifier-shaper chain is shown in Figure II.. Each channel of the 16-channel version consist of a preamplifier, a Pole-Zero network, two bridged-T filters, two non-inverting amplifiers, a CMFB network and a self-adaptive bias network.

The principal parameters in the design were Equivalent Noise Charge (ENC), Full Width Half Maximum (FWHM), Integral Non-Linearity (INL) and conversion gain (Table 1).

This topology has successfully and extensively been used in other applications like the ALICE TPC [2] and the ALICE TRD [3]. Each of the parts of the circuit is briefly explained in sections III, IV and V. The simulated and measured results are presented in sections VI, VII and VIII.

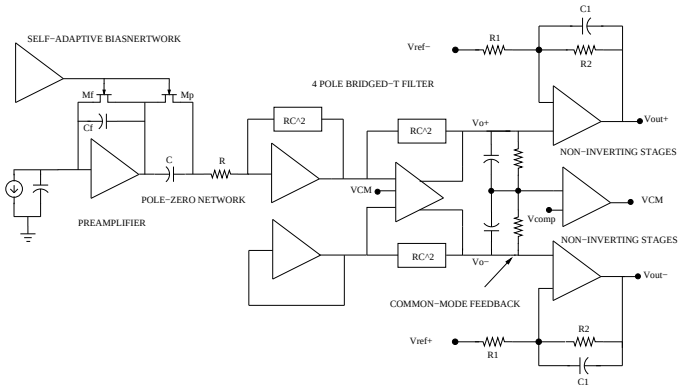

Figure 2: Block diagram of the preamplifier-shaper chain of the realized ASIC. All parts, the preamplifier, the Pole-Zero network, two bridged-T filters, two non-inverting amplifiers, the CMFB network and the self-adaptive biasnetwork are shown.

III. The preamplifier and the Pole-Zero network

Since the required FWHM of the preamplifier shaper circuit is 70 ns, a NMOS transistor is preferred at the input due to higher transconductance (gm) and to the lower white noise compared to a PMOS transistor at the same current. The chosen architecture for the preamplifier is the well known folded cascode CMOS circuitry shown in Figure III.. The input is optimized for a detector capacitance of about (5-10) pF. This gives for the input transistor a width over length ratio (W/L) of 800/0.35 and a drain current of 1.85 mA.

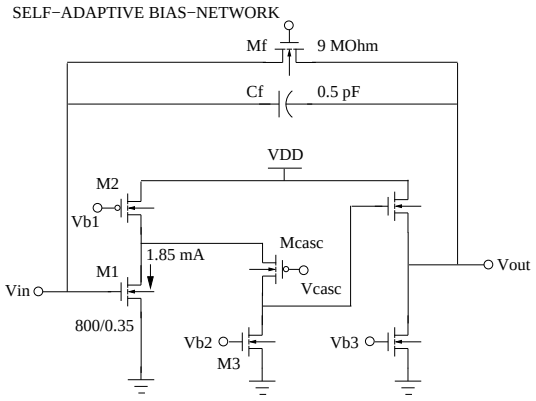

Figure 3: Block diagram of the preamplifier Folded cascode CMOS circuitry

This part has in addition an active feedback network consisting of a capacitor Cf (0.5 pF) and large feedback transistor Rf in the area of 9 MΩ to reduce the parallel noise contribution. The time constant for the feedback network was chosen as a trade-off between noise and ballistic deficit. This relatively long time constant given by the feedback network RfCf, has the disadvantage that the CSA produces a very long tail at the output due to the long discharge time. This long discharge time, relative to the short rise time, makes this topology inefficient for high count rate application due to its sensitivity for pile-up. Therefore a high-pass filter consisting of the CR part FigureII. is included to reduce the length of the tail. The reduction the tail (low frequency part) and the following quick return to base-line (< 200 ns) increases the circuits capability to process events with high occupancy.

Also the implementation of the 9 MΩ integrated resistance could be a problem due to the large area occupied. A resistance of this size is only doable if a MOSFET biased in the triode region is used. The use of the MOSFET as a replacement for the feedback resistor has also the advantage that it reduces the parasitic capacitances associated with the large resistor. To bias the feedback transistor Mf the well known self-adaptive bias network is used. The chosen self-adaptive biasing scheme with non-linear pole-zero cancellation allows us to use a MOS device operated in triode region as the DC feedback element while eliminating non-linearity and sensitivity to supply, to temperature and to process variation. The circuit is continuously sensitive and requires no external adjustment to set the feedback resistance. This part of the circuit is designed following the design procedure given in [4]. This is normally realized as a copy of the CSA, but in our case we use a scaled version. We do not see any visible effect in doing so, confirming previous experience where the same scaling strategy has been used.

The presence of large input signals increases the drain-source voltage of this feedback transistor, which in turn decreases the feedback resistance. This feature has the advantage that the time constant of the feedback network reduces, and as a consequence the probability for pile-up with large pulses will also decrease.

To reduce any possible crosstalk between channels, each channel has its own independent self adaptive bias-network.

IV. Shapers

In order to decrease the rise and the fall time of the produced pulses, to meet the gain specifications, and to reduce the noise through the bandwidth reduction of the filters, the CSA and the P-Z network are followed by two bridged-T filter stages that give in total a CR-RC4 semi-Gaussian shape as seen in Figure 4. The first shaper must fulfill the following requirements, keep the Vgs relative to ground equal to the Vgs of the CSA for process, temperature and supply voltage variation, in addition to amplification and bandwidth limitation. To preserve a perfect Pole-Zero cancellation one of the requirements is that the first shaper input transistor has the same Vgs relative to ground as the CSA. This is best done by choosing the same topology as the CSA. A scaled version of the preamplifier is here used to save power and area. This will not influence the quality of the Pole-Zero cancellation as seen in Figure 4 and Figure 5 for simulation and measurement results, respectively. The pulse return smoothly to the baseline without any undershoot in about 200 ns.

The second shaper is built around a fully differential folded cascode amplifier that converts the signal from a single ended output signal to a differential output signal. To hold the common-mode voltage of the differential output at a known

voltage Vcomp, a CMFB circuit is used to sense the average of the amplifier output Vo+ and Vo-. The output of the CMFB network is VCM. The average of the Vo+ and Vo- is generated with the help of the resistor/capacitor combination applied at the input of the CMFB network. This voltage is compared with an equally and externally given voltage (Vcomp). These two voltages are then compared, and the output of the CMFB circuit is then fed back through the VCM to adjust any deviation from the externally given Vcomp. These scheme ensures fully balanced outputs [5] over a voltage range limited by the CMR of the two non-inverting amplifiers and the source follower output of the second shaper. The combination of these two filters gives a very good semi-Gaussian pulse with a peaking time of 70 ns from 0 - 100% of the maximum pulse amplitude. Due to the symmetry of the fully differential folded cascode topology, the different polarities of the signal will be handled equally around the common mode voltage. This part of the topology together with the part described in the following section is therefore optimal for a dual polarity detector.

V. The non-inverting output stages

After the signal is shaped and optimized for noise, the differential output signal from the differential amplifier is split in two around the common-mode voltage, in this case 1V, in order to increase the maximum output swing. The output DC-level is set by Vref+ (1.5V) and Vref- (0.5V), giving a DC level at the output of 0.5V (Vout+) and 1.5V (Vout-), respectively. The amplifier used here is a Miller CMOS OTA. The two equally designed amplifiers are then used in an non-inverting topology (Figure II.), each with a closed loop gain of 2. The proposed topology can easily be adjusted to adapt to both polarities by interchanging the two reference voltages Vref+ and Vref-. This allows a symmetrical system so that the CBM CSA chip will have nearly identical response to both the negative and positive input signal, only limited by the cut-off region of the feedback transistor Mf and the cut-off region of the output stage of the first shaper. The circuit has been proven to handle a negative input charge of 140 fC without any visible degradation of the signal or of the specifications. With this topology the user can change the DC level as wanted, and to some degree decrease the gain of this stage by adding externally a resistor with appropriate value in series with R1 in Figure II.. This will, of course, also change the output DC and must be compensated for by increasing/decreasing the reference levels.

VI. Transient analysis

A simulated pulse response for a delta input charge of 165 fC with a detector capacitance of 5 pF is shown in Figure 4. The pulse response shown here, has a FWHM of 71 ns, a conversion gain of 12.6 mV/fC, a simulated noise of 350 e^-, a return to base-line after 200 ns and no undershoot. Therefore, we can conclude at this stage that the circuit fulfills all the requirements (Table 1) from the simulation point of view.

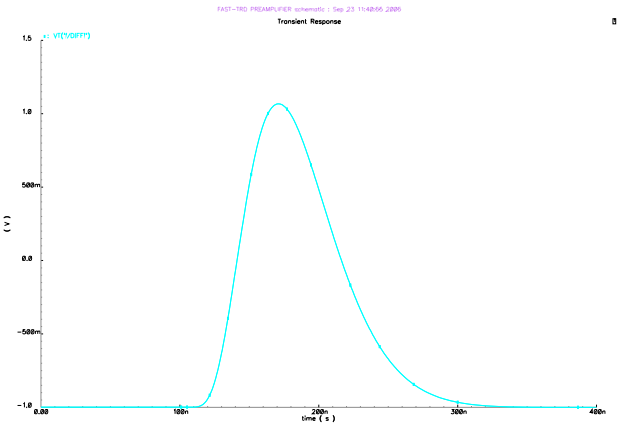

Figure 4: A typical simulated pulse response of the circuit for a delta input charge of 165 fC with a 5 pF detector capacitance.

VII. Measured characteristics of the circuit

The first prototype preamplifier shaper for the Fast TRD at CBM has been tested. The circuit has been realized in AMS's C35B4M3 0.35 um CMOS process.

Parameters	Specifications	Simulated (typ.)	Measured
Equivalent Noise Charge	1000 e^- C_d 5-10pF	350 e^-@5pF 412 e^-@10pF	387 e^-@5pF 446 e^-@10pF
Conversion Gain	12mV/fC	12.6 mV/fC	12.64 mV/fC
FWHM	70ns	71 ns@5pF	71 ns@5pF
Undershoot		1mV	-
Baseline shift		3mV	-
INL	$< 1\%$	$<0.45\%$	0.7%

Table 1: Main requirements given for the preamplifier shaper design. Simulated and measured values are also given.

The total power consumption of the circuit is 256 mW for 3.3 V power supply. The ASIC consist of 16 channels, so this gives a power consumption of 16 mW/channel. The circuit has a typical output range of 2 V.

The circuit was tested for ENC, conversion gain, INL and FWHM.

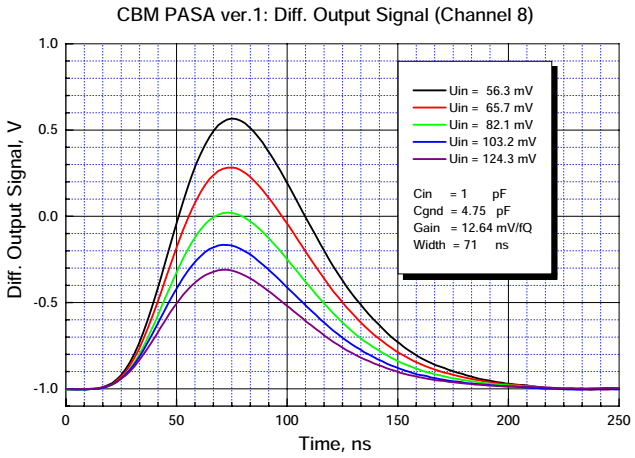

Figure 5: Measured pulse response with a typical load of about 5 pF for several different input charges.

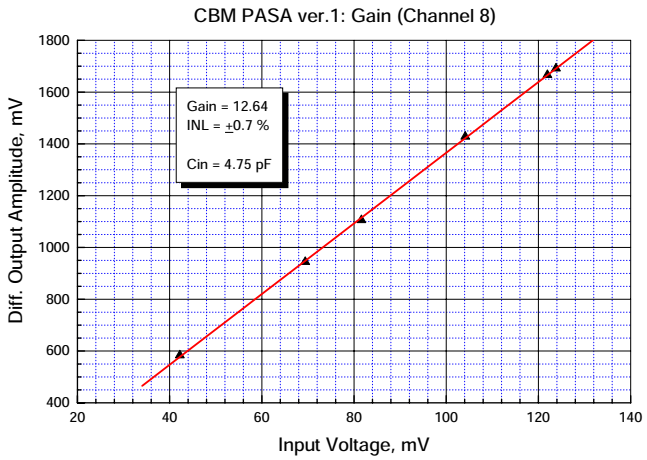

Figure 6: Measured conversion gain and integral non-linearity as a function of input charge.

The pulse response was measured with a typical detector capacitance of 5 pF, with an input signal ranging from 56 mV (56 fC) to 124 mV (124 fC) through an injection capacitance of 1 pF. The measured result (Figure 5), gives an FWHM of 71 ns, showing a superior agreement with the simulated value of 71 ns for the same detector capacitance. An equally good agreement is also observed between the measured conversion gain (12.64 mV/fC) and the simulated one (12.6 mV/fC).

The INL has been measured for input signal from about 40 fC to 125 fC. The overall INL obtained here is 0.7% as seen in Figure 6. This is well below the required INL of 1% and close to the simulated value of 0.45%.

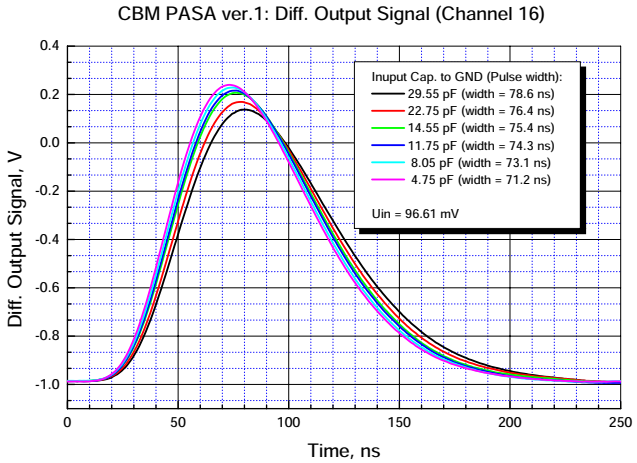

Figure 7: Measured pulse response for different load capacitances.

The measured pulse response for different detector capacitances are shown in Figure 7. The signal shape for both FWHM and conversion gain shows a weak variation with the input capacitance due to the reduction of the bandwidth of the CSA as obtained in simulations. The measured results are shown in Figure 8. The amplitude (conversion gain) decreases when increasing capacitance (Figure 8,bottom) while the width increases (Figure 8,top). The two effects compensate resulting in a constant area (Figure 9).

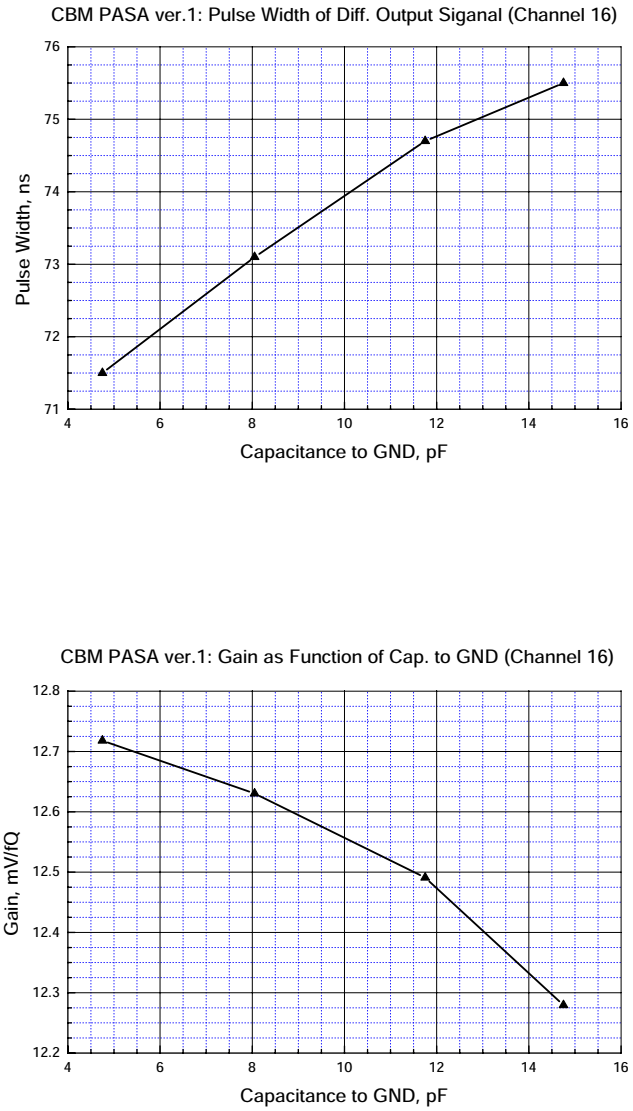

Figure 8: (Top): Measured FWHM of the signal for different load capacitances. (Bottom): Measured conversion gain for different load capacitances.

The ENC measured noise for 5 and 10 pF (detector capacitance working area) is 387e and 446e, respectively (Fig. 10,top). The small offset in noise compared to the simulated results is given by the pick-up as seen in Fig. 10,bottom. This gives a measured noise slope of 11.8e/pF compared to 12.4e/pF simulated. This shows again a very good agreement between simulated and measured values.

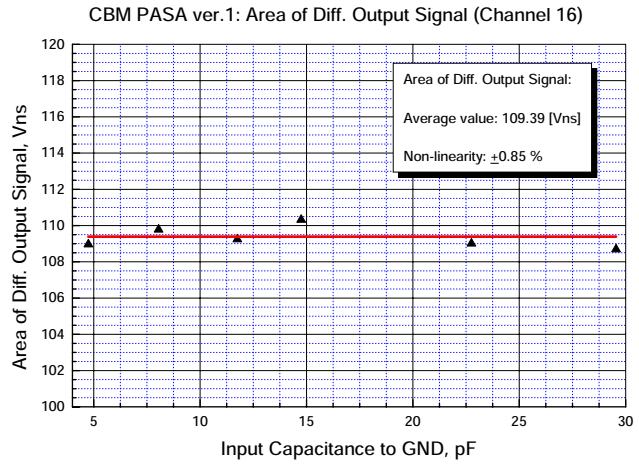

Figure 9: Area of the measured signal for different load capacitances

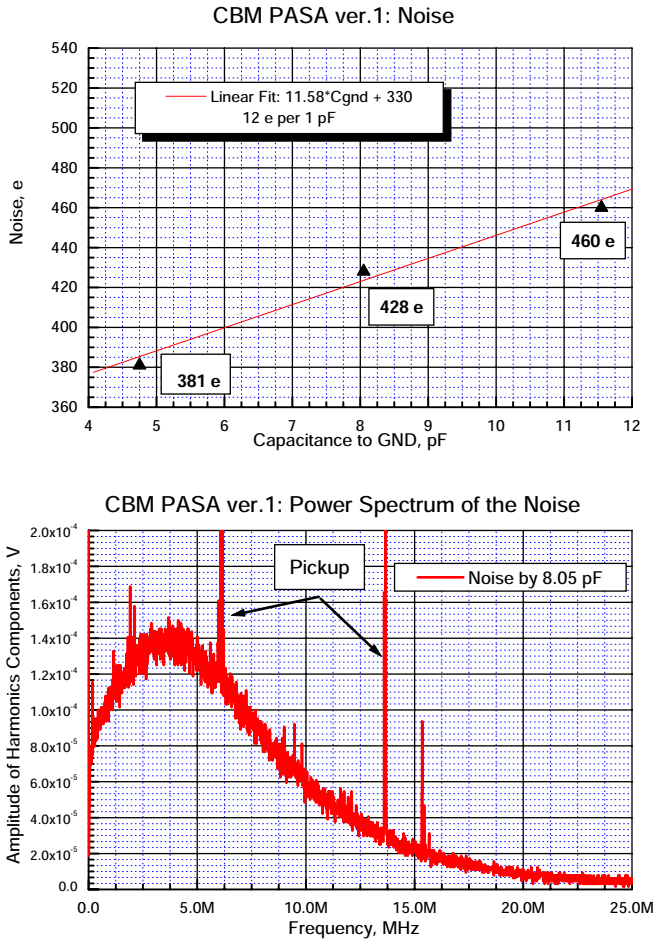

Figure 10: (Top): Measured Equivalent Noise Charge (ENC) for different load capacitance. (Bottom): Measured noise spectrum for a capacitance load of about 8 pF.

VIII. Conclusions

A new low noise multi-channel Application Specific Integrated Circuit (ASIC) has been designed with the AMS's C35B4M3 0.35 um CMOS process for use in CBM test-beam at GSI Darmstadt February 2006. This circuit has successfully been used in that test-beam for both polarities. The ASIC consist of 16 channels, and the total power consumption is 256 mW. The chip is designed to handle a typical input charge of 165 fC. The ASIC is optimized for capacitance in the region of about 10 pF. The total area of the chip is 12 mm^2. In total 15 circuits out of 15 have been measured successfully. The presented circuit fulfilled all requirements. A superior correlation between simulated and measured values has been shown.

IX. Acknowledgments

This work has been supported by the GSI F&E program and EU 6th framework hadron physics I3HP. The authors are grateful to Dr. I. Rusanov for performing the test of the chips in order to be ready for the test-Beam at GSI Darmstadt February 2006.

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Data Acquisition and Management in the Calibration Processes of the CMS Barrel Muon Alignment System

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Abstract

In order to be able to match correctly the track elements produced by a muon in the Tracker and the Muon System of the CMS experiment [1] the mutual alignment precision between the Tracker and the Barrel Muon System must be no worse than 100-400 micrometers depending on the radial distance of the muon chambers from the Tracker. To fulfill this requirement an alignment system had to be designed. This system contains subsystems for determining the positions of the barrel and endcap chambers while a third one connects these two to the Tracker. Since the Barrel muon chambers are embedded into the magnet yoke of the experiment a non-conventional alignment method had to be developed. In this paper we restrict ourselves to the Barrel Alignment System and the calibration methods of its components.

I. THE BARREL MUON ALIGNMENT SYSTEM

The CMS Barrel Muon Alignment System (Fig. 1) is based on an optical network of LED light sources and video-cameras. The full system contains very large number of cameras (approx. 600 pcs) and LEDs (approx. 10000 pcs). Overwhelming part of these LEDs are mounted on the 250 barrel muon chambers while the cameras observing these LEDs are mounted on rigid structures called MABs (Module for Alignment of the Barrel). The MABs (36 pieces altogether) are fixed on the iron yoke of the magnet. Furthermore, there are about 300 LEDs and 100 cameras making direct connections between the MABs (called diagonal connections). Finally there are 6 long carbon-fiber bars located inside the barrel muon system containing in total 144 LED light sources allowing direct measurement of the Z coordinates of 24 MABs (where Z direction in the experiment corresponds to the direction of the proton beam path).

The results of individual measurements are the positions of the centroids of the images of the LEDs measured by the cameras. In order to be able to reconstruct the positions of the muon chambers additional data -in addition to the measured centroids- is required. These are the parameters of the cameras (magnification, and tilt angles of the sensor with respect to the optical axis of the camera, sensitivity and homogeneity of the video-sensors of the cameras) and the positions of the LEDs on their holders. Also, the positions of the cameras and the LED holders in their embedding objects (muon chambers, MABs, Z-bars) are also needed. These additional data are obtained by the calibration of the elements.

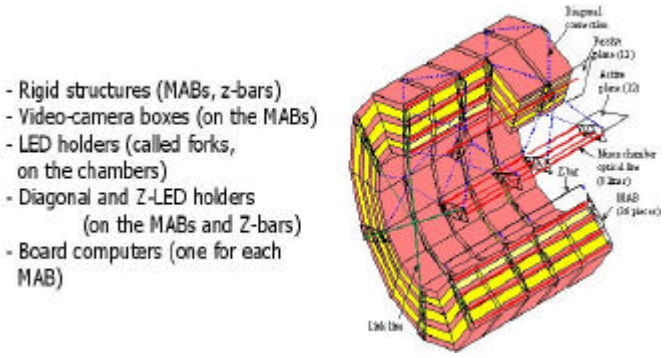

Figure 1. CMS Barrel Muon Alignment scheme

II. CALIBRATION OF THE COMPONENTS

The main requirement on the muon chamber alignment precision is in the range of 100-400 microns. Since this value depends also on the calibration precision of the components, the calibration methods had to be established such that the resulted precision of the full system could meet the above mentioned requirements. The individual calibration steps of the light source-related objects are the LED holder calibration and the barrel muon chamber alignment calibration, while calibration steps of the camera related objects are the camera quality control, the camera calibration and the MAB calibration.

A. *Light source related objects*

As it is mentioned above the basic components of the Barrel Muon Alignment System are the LEDs and the cameras. Individual LEDs are grouped into mechanical structures called LED holders containing 10 (for DT chambers), 3 (diagonal LED holders) or 6 (Z-LED holders) LEDs according to the measurement type.

During the calibration process positions of the LED centroids in the frame of the LED holder are determined. The optical network requires most of the LED holders to be observed from both sides. This can be solved by introducing an auxiliary frame of reference which can be seen from both sides. Technically, this is a calibration tool containing multimode optical fibers illuminated by noncoherent light sources and shining into both directions. Positions of these

light sources are measured in a high precision metrology lab and produce light distributions similar to those of the LEDs to be measured. Since the light spots are observed by cameras there was a requirement to exclude geometrical distortions and the error on centroid calculation caused by the un-even gain on the sensor surface. This has been solved by mounting the calibration tool (and therefore the LED holders) on a precise two-dimensional moving table and by constructing a successive method for moving all the centroids to a predefined position on the sensor surfaces. Therefore LED positions correspond to the position readouts of the moving table.

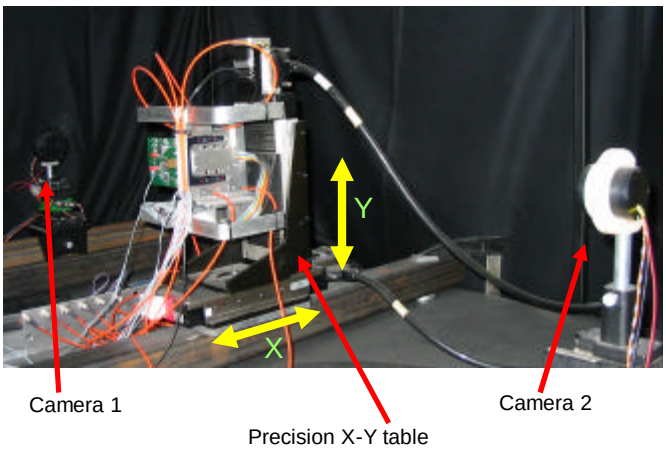

Figure 2. Calibration bench for the LED holders.

As the amount of LED holders is very large (>1200 pieces) a highly automated measurement method had to be developed. Both the successive centroid measurements and the control of the moving table and the LED holders are computerized. The operator only has to change the LED holders, identify it and start the measurement. The successive status then can be monitored on the computer console.

Also due to the large number of LED holders an effective way of data handling and storage had to be developed. For such a large number of data (five complete measurements of all the LED holders ~ 100 k lines of raw data + 20 k lines of analyzed data) the use of a commercially available database solution is inevitable. Our team decided to use MySQL because it supports all the programming languages used in this calibration process under all operating systems. This database server also had an advantage because its installation requires only a moderate disk space and it is also freely available for research purposes. For data security reasons measurements are recorded as ASCII files which are automatically uploaded as the measurement finishes. Therefore one can assure to have two identical copies of the raw data and in case of critical failure of the database server data can be recuperated by using the same method used for synchronizing the database to the ASCII files. However, storage of data in a relational database provides a very easy way to compare the individual measurements therefore pinpointing any measurement errors based on statistical methods. This statistical analysis and the data recuperation are done by web-based Perl scripts allowing the access to the data from virtually everywhere without the need for special data handling software.

Calibration methods of the diagonal and Z-LED holders are very similar to that of those ones described above.

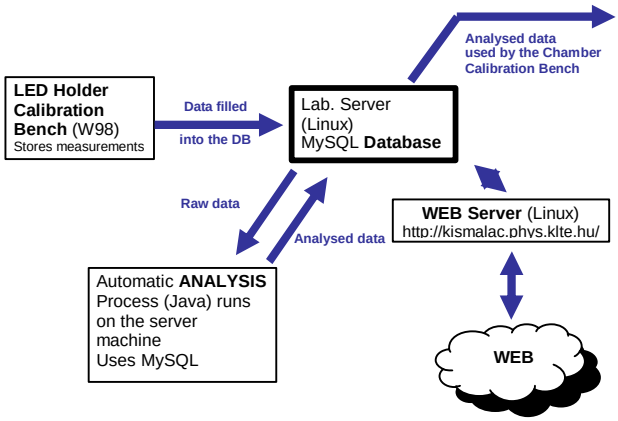

Figure 3. Data flow during the LED holder calibration [5]

The main goal of the alignment system is to locate the anode wires of the muon chambers with respect to the Tracker.

Muon chambers have a construction which doesn't allow the observation of their anode wires after construction. This construction doesn't allow either to determine the LED holder's position with respect to the wires during chamber building. To overcome this problem the following technology has been developed:

1. During construction position of every anode wire (approx. 400 per chamber) is measured during the construction with respect to mechanical reference objects known as corner blocks mounted on each corner of a muon chamber's Super Layer [2] (4 pieces per Super Layer). Since a muon chamber consists of two or three Super Layers depending on its type, a muon chamber can have eight or twelve corner blocks in total. These corner blocks serve as position references.

2. Since the position measurement of the LED holders is based on a centroid measurement while positions of the corner blocks can be determined by standard survey techniques (photogrammetry) an additional calibration bench had to be built. Here the corner blocks can be located by photogrammetry and the LED holders mounted on the chambers can be measured by cameras with pre-calibrated (known) positions with respect to the calibration bench. For this pre-calibration a specially designed calibration plate containing both optical fiber light sources and target holes for the photogrammetry is used. Internal parameters of these plates could be determined by a metrology laboratory. During the pre-calibration of the chamber bench these plates are localized by photogrammetry while a simultaneous measurement of the optical fibers has been performed by the cameras. A geometrical reconstruction is able to recuperate both the camera positions and their internal parameters needed for a correct measurement of the LED holders.

3. Applying mathematical transformations the positions of the LED holders can be determined in the chamber's frame. As a byproduct the localization of all the Super Layers in the chamber's frame can also be performed.

The number of muon chambers to be measured was 264, therefore this calibration step also requires a reliable data handling strategy. Since during LED holder calibration the

previously mentioned strategy has proved its strength a similar system has been built: data are stored primarily in ASCII files and later uploaded automatically into a MySQL database. As soon as the data are uploaded a data analysis could be started on the survey data to determine the chamber's internal parameters. This calibration process is equipped with a Perl-based web reporting system.

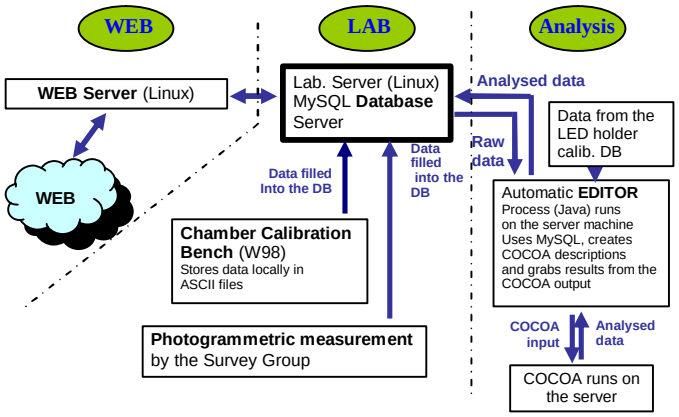

Figure 4. Data flow during the muon chamber calibration

The reporting system is also able to perform a fast check on the LED holder centroids. It fits the LED holder calibration data to the centroids recorded during chamber calibration. Despite the fit is done only in two dimensions (this is much faster than trying to fit the values in 3-D) it is enough to pinpoint if the centroid recognition fails and accidentally identifies a reflection as a direct spot.

B. Camera –related objects

The second most fundamental devices in the Barrel Muon Alignment System are the cameras. The number of these devices is in the range of 600, therefore only a cheap device could be taken as an economically reasonable solution. As a result a very cheap black-and-white one-chip video sensor has been chosen. However, to ensure the reliability of the data recorded by this type of camera every single sensor has to be studied, this is called sensor quality control. During this study gains of all pixels have to be recorded. During this process both the "dead" and "hot" pixels have to be discovered. In order to meet these requirements a device has been constructed where an array of specially selected LEDs and an optical diffusor can produce a uniform illumination on the sensor. Array of LEDs is necessary because uniform light must be provided on a relatively large area. LEDs are driven by a 16-channel 12 bit ADC controlled current generator between 0 and 60 mA. To ensure the comparability of different measurements a monitoring semiconductor sensor has also been installed on this bench.

During the sensor quality control several images are taken at different light intensities and stored as uncompressed bitmap images (Fig. 5). As the measurement finishes, average, sigma and noise images are calculated from the recorded images and stored next to the raw images. Only the numerical results are stored in the database. However the Perl-based web reporting system can retrieve both the raw or calculated images together with the numerical values.

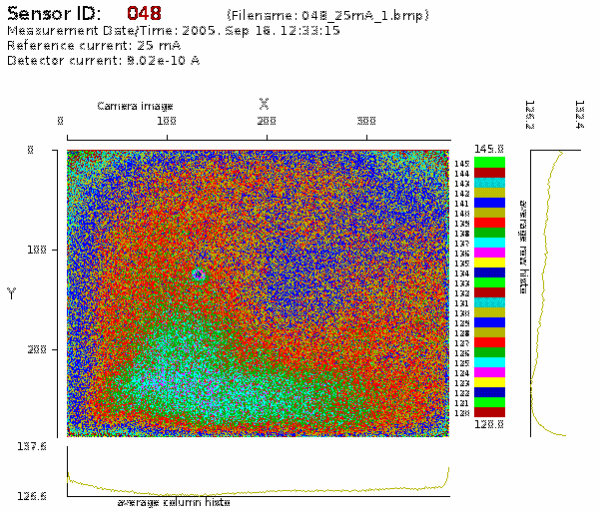

Figure 5. Result of a camera quality measurement

On this figure a dirty spot can be seen at position X~120, Y~120. As As a result of this quality control this sensor has been sent back for further cleaning

After the camera quality check sensors are built together with a small lens and the housing to form a very simple pinhole camera. Internal parameters of this camera to be determined are the distance between the pinhole and the sensor center and the tilt angles of the sensor with respect to the axes perpendicular to the line connecting the pinhole and the sensor center. These values can be determined using a bench where plates equipped with optical fiber light sources are installed (see Fig. 6).

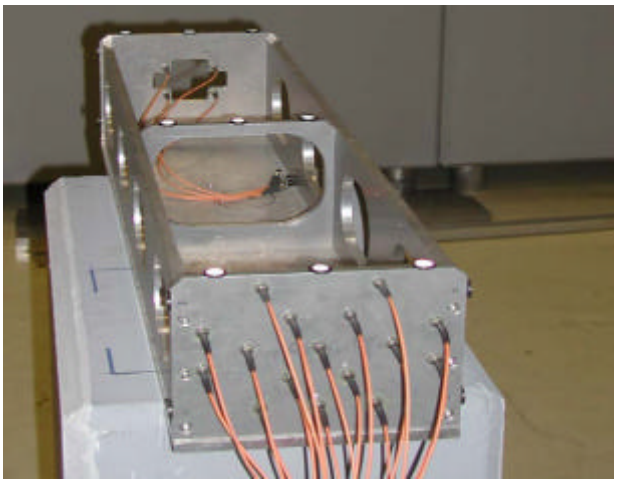

Figure 6. Camera calibration bench

It has been proven from the preceding simulations that two well designed plates can help to find the above mentioned parameters if they are located precisely (~ 20-30 microns) in the laboratory frame and their internal parameters (fiber positions) are known down to the 3 micron level. In order to localize these plates they need to have holes that can accept photogrammery targets. These holes should be localized with the same precision as the fibers are. Measurement technique is very similar to that of the chamber measurement's that is cameras observe the centroids of spots created by the fibers. This process is still under development therefore it is still not equipped with all the database and web reporting techniques

as the above mentioned ones, but it is desired as these measurements are started.

As soon as the camera internal parameters are determined the camera gets mounted on the rigid supporting structure called MAB. The main role of the MAB is not only to support the cameras but also to define a coordinate system where these cameras can be located. The structure of the MABs has been chosen to be as rigid as possible, to have the smallest thermal expansion constant and have the smallest weight in order to prevent the geometrical distortion due to the gravity. The material that meets these conditions is the carbon-fiber structure. Since it defines a local frame of reference for every object it incorporates must be localized within it. The camera localization process is very similar to the processes mentioned so far: it makes use of a specially designed plates having optical fibers attached and mapped in a high precision metrology lab. The measurement process is also very similar, centroids of spots created by the fibers must be measured and then a geometrical reconstruction is to be performed to get the camera positions in the laboratory frame. In the meantime the carbon fiber structure of the MAB is localized in the same frame by common survey methods therefore the transformation of the cameras from the laboratory frame to the MAB's frame can be done. This is also a method under development therefore all the database and web reporting tools are not yet ready, but will be finalized by the start of the mass measurements.



Figure 7. MAB calibration bench

III. APPLICATION OF THE CALIBRATION DATA

Data recorded during the various calibration processes are used on one hand during the already described successive calibration phases and on other hand serve as input data to the main geometrical reconstruction process called COCOA [3],[4]. Result of this reconstruction gives the positions of the muon chambers at the end.

In order to allow the reconstruction process to use the calibration data, they should be uploaded to the main CMS databases. Since the reconstruction uses these data in POOL-ORA format and stores the values in an Oracle database, all data have to be converted during the upload. Test of this data conversion have already been done. However, the upload of the full data set has not yet been done.

IV. SUMMARY

Each piece of all element types in the CMS Barrel Muon Alignment System have to be identified, calibrated and the position of each embedded element on the enveloping object must be known and followed.

Given the large number of elements and the complexity of the system, the data handling procedures of the calibration and assembly was automated as much as possible.

Five calibration facilities have been built to calibrate the LED holders, the chambers, the sensors, the camera-boxes and the MABs. They are very different in size and complexity but similar in nature: in all of them LED-type light sources have to be switched on and off and driven with given current and their images have to be captured by camera-boxes. These functions are complemented -depending on the task- by other control and DAQ functions like 2D-motion table control, video-multiplexing or environmental (temperature and humidity) measurements.

Therefore all the facilities are also similar from control, data acquisition and data handling point of view.

The core hardware elements of the control and data acquisition system are the microcontroller-based modular units [6] that - together with the control software - can easily be adapted to any particular calibration step. As the primary result of all the measurements are either full video-images or light spots, the image processing and transfer solutions can be reused at each calibration step.

The direct database connection is providing a correct, reliable and searchable storage of raw and processed data also in view of the fact that the validation and processing for the given calibration process is using the results of the preceding calibration steps. A dynamic WEB-based reporting tool makes it possible to follow the status of calibration and assembly and to search for any data in an easy way without direct database-operations. In the paper these points are discussed in detail.

The intermediate and final calibration values are stored in a relational database. Each step of the calibration procedure heavily relies on the results obtained in the previous steps, so the online query and update features offered by the database system are vital to our design.

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CMS Optical Links - Lessons learned from Mass Production

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Abstract

The CMS Tracker will install over 40000 optical links in its data-readout and control system, representing an unprecedented deployment of this technology in a Particle Physics Experiment. After reviewing the Quality Process employed in this project, a summary of the performance data measured during production will be shown. The analysis of this data will then be used to illustrate how the performance of the installed system may be predicted, giving confidence that the specified functionality will be attained in the final system. Completion of the production has allowed reflection upon the processes used and improvements for future such projects will be given in the form of some lessons learned.

I. Introduction

The CMS Tracker[1] is currently in the final stages of assembly of its sub-structures in preparation for installation within CMS as a whole in time for first collisions at the LHC in 2007. The readout and control system of the Tracker uses optical data transmission with a channel density unparalleled anywhere – 40000 analogue readout channels are combined with 3000 digital control channels. Once the success of the design of the Tracker systems was proven in system tests the optical components on which it is based were adopted for use by other Sub-detectors of CMS. With the addition of readout and control systems for ECAL, Preshower, RPC and Totem the total quantities increased by an additional 22000 fibre channels that re-use the Tracker components for Digital transmission systems. This scale of production of components has not been seen before in particle physics and with the production now complete it is timely to sum-up the project and reflect upon the lessons learned so that they may serve future projects of this scale and/or nature.

The CMS Tracker Optical Readout and Controls systems[2] are shown schematically in Figure 1. The readout system consists of laser transmitters coupled to a Linear Laser Driver (LLD) on the Analogue Optohybrid that is connected to the Silicon Microstrip Detector Modules distributed throughout the Detector Volume. The lasers are individually pigtailed with MU connectors that allow for the highest connection density available from a standardised optical connector at the first patch panel that is also distributed across the detector volume at the edges of the various mechanical support structures of the tracker. At this distributed patch panel the individual lasers connect to optical fan-outs that bring the fibres into 12-fibre ribbon cables. These cables connect via MFS-type connectors to high-density rugged multi-ribbon cables at the In-line Patch Panel located inside the CMS cryostat just beyond the level of the ECAL. The Multi-ribbon cables containing a vertical stack of 8 ribbons span the 40-65m to the shielded counting room where each ribbon connects to an Analogue Receiver (ARx) Module. These modules are directly mounted on the 9U Front-End Driver (FED) VME boards that form the CMS Tracker interface to the CMS Data Acquisition (DAQ) system. The Bi-directional Digital Control system re-uses the same fibre plant as the Readout system described above. Control data generated on the Front-End Controller (FEC) 9U VME board in the Counting room. These data are converted to optical by the transmitter side of a bi-directional 4-channel optical Transceiver (DTRx). They are received by individually pigtailed photodiodes and interpreted by the Rx40 receiver ASIC mounted on Digtial Optohybrids distributed throughout the Tracker volume. After passing around the electrical control ring the signals are re-transmitted to the Receiver part of the DTRx on the FEC by the analogue laser transmitter and driver that are re-used in a digital fashion.

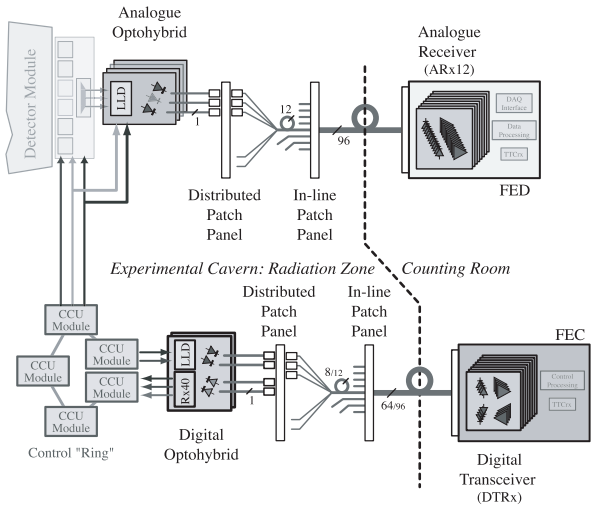

Figure 1: Showing the CMS Tracker Optical Readout and Control Systems.

It is also important to note that there are a few peculiarities that distinguish how a particle physics collaboration (albeit represented by CERN) is constrained in its dealings with industrial partners responsible for turning designs into reality on a large scale. The first important constraint to note is that the timescales from first discussion of feasibility with a manufacturer to the placing of a large-volume order and then completion of production is measured in significant multiples of years. This may prove to be difficult for industrial partners to manage, especially in the fast-moving high-technology area. To mitigate this it is imperative to build a good, strong, relationship with the manufacturer from the start – this will also become important when overcoming the inevitable problems when they occur during production.

II. Quality Process

The Quality Plan [3] put in place in order to ensure the required quality during mass production of optical link components led to the flow of actions shown in Figure 2. The project was divided into four distinct phases, starting with Prototyping and ending with the Assembly of the components into the structures of the CMS Tracker. Industrial partners were vital to provide the production capacity needed for the large number of components in the system. For this reason all components are COTS or COTS-based with minimal modifications. Testing of the key performance parameters was carried out by the manufacturers at the 100% level, with the measured data being made available to CERN. Validation was then carried out at CERN by measurement of a similar parameter set on a per-batch sampling-basis to maintain confidence in the manufacturing data.

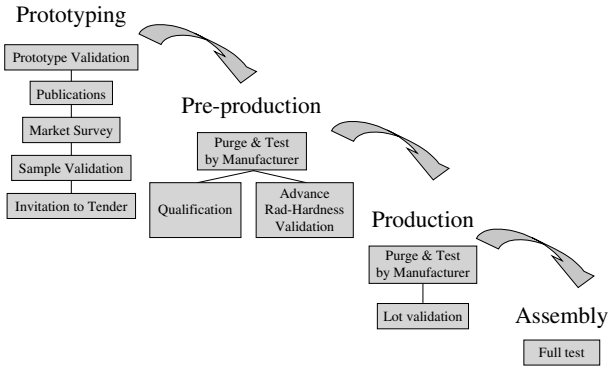

Figure 2: Showing the Project Quality Process, moving from Prototyping via Pre-Production and Production to Assembly.

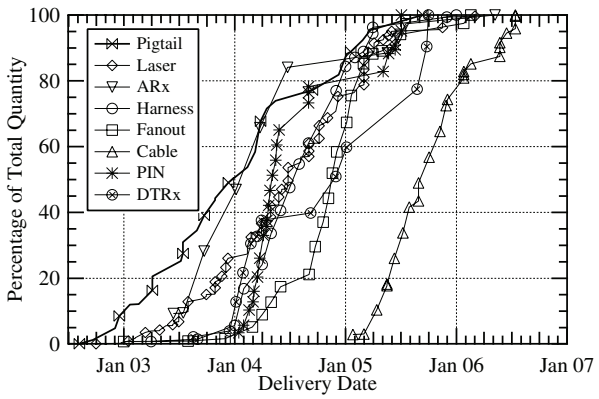

Figure 3: Showing the delivery of components over time. Each symbol represents a delivery that required QC testing at CERN.

Figure 3 shows all deliveries of all components over time. Since each marker also represents a Quality Control (QC) test carried out at CERN, the QC workload can be seen to be non-negligible during the entire 4-year production period.

III. Production Data

A. Laser Diodes

The contract for supply of laser diodes was awarded to ST Microelectronics of Milan, Italy, in 2002 for a total quantity of 45000 for the CMS Tracker Readout and Control systems. The same component was then also re-used by the ECAL readout and the ECAL and RPC control systems, leading to an increase in total quantity to over 65000 lasers. After some initial difficulties for the manufacturer to ramp-up production due to staff training issues and vacations, the target rate of 3000/month was achieved and maintained for over one year. Lasers were assembled from COTS laser die manufactured by Mitsubishi Electric of Japan and Terminated Fibre Pigtails manufactured by Sumitomo Electric of Japan.

Performance in terms of uniformity of measured parameters remained excellent throughout production, as shown in Figure 4 and Figure 5. Values measured during production remained centred within the specification window.

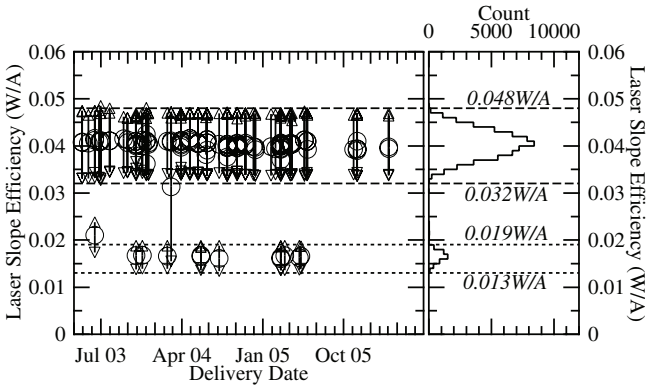

Figure 4: Showing the production trend (left) in terms of minimum, (inverted triangles) maximum (triangles and mean (circles) values of the laser slope efficiency over time for all delivered batches. The corresponding histogram for all delivered lasers is shown on the right. The specification is shown for both readout (top family) and control (bottom family) lasers

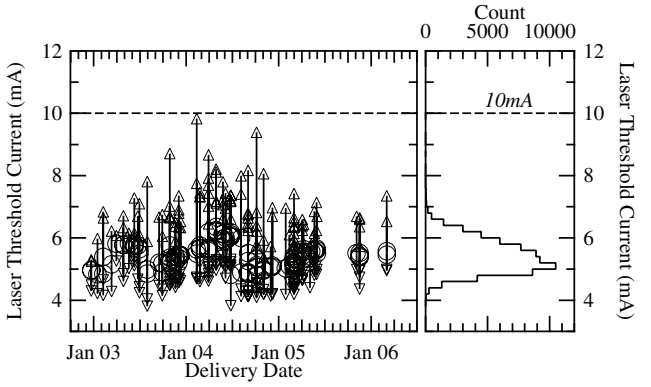

Figure 5: Showing the production trend and histogram for the threshold current of the laser diodes. All lasers have room temperature threshold currents below the specified 10mA.

B. Analogue Receiver Modules

The CMS Tracker Readout system requires a total of 4500 analogue receiver modules (ARx12). NGK Ltd of Japan delivered the intitial quantity of 85% in the first 6 production batches up to July 2004 and subsequently had to wait for almost a full year before the order confirmation was granted by the Tracker for the full quantity. This explains the first gap in Figure 6 and Figure 7. A final purchase was made for spares in 2006 before the supplier closed their optoelectronics manufacturing facility. This component is the only one to have passed the qualification testing in the first pass, a testament to the high production quality achieved.

Figure 6 and Figure 7 show that the production is well centred within the specification window for the gain (Figure 6), and in excess of the typical specification on bandwidth (Figure 7).

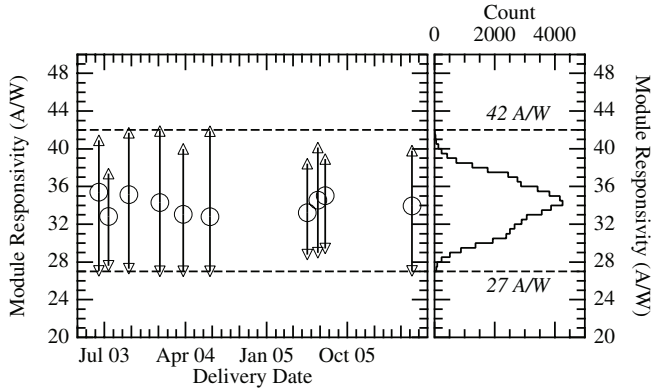

Figure 6: The production trend and histogram for the responsivity of 12-channel Analogue Receiver Modules show all channels of all modules to be have min. 27 and max. 42 A/W responsivity.

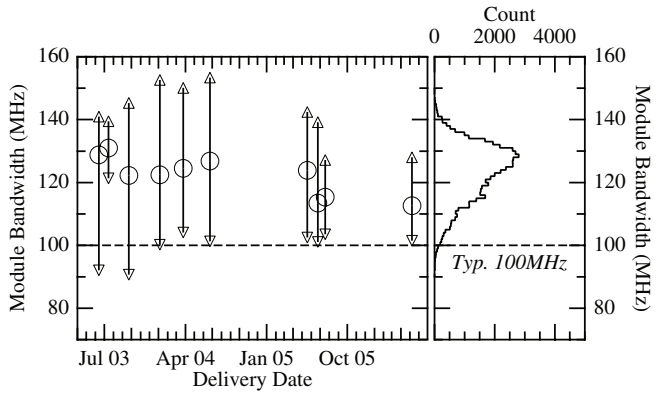

Figure 7: The production trend and histogram for the bandwidth of 12-channel Analogue Receiver Modules show that the typical spec of 100MHz is comfortably met.

C. Rugged Fanouts

Single-fibre connectors are used in the CMS Tracker to connect the highly distributed transmitters and receivers of both the control and readout systems to high-density 12-fibre ribbons. The connector type chosen by CMS for this task is the industry-standard MU, which provides the highest stacking density of any standard connector. This high density is required due to space constraints inside the Tracker. The optical fibre (SMF-28 from Corning USA) was ribbonised and made into a rugged cable by Ericsson of Sweden.

Production of the sMU-MFS (single-fibre to multi-fibre ribbon) fanouts proceeded in two steps: in the first Sumitomo of Japan produced symmetric harnesses with individual fibres broken-out of the ruggedised ribbon at both ends and connectorised with sMU connectors; this assembly was then cut by Diamond of Switzerland who terminated the ribbon directly with the chosen ribbon connector (MFS). Both manufacturers required some ramp-up time for their production process to reach the specified performance. Once this stage was overcome both manufacturers were able to sustain a high production rate over approximately one year. The last deliveries were delayed by the need to reach a consensus within the user community for final needs and funding.

Figure 8 shows that the high performance of the single-fibre sMU was achieved throughout the production. Figure 9 shows the same for the ribbon connectors mounted on rugged fanouts. The low losses achieved are in marked contrast to the expectation that the distribution would be a rectangle within the specification window.

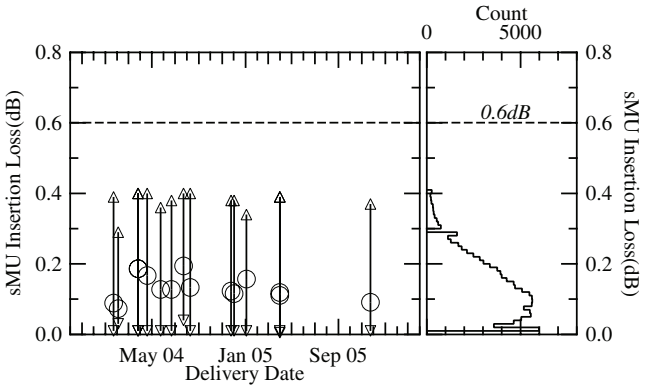

Figure 8: The production trend and histogram of the single-fibre connectors (sMU) on rugged fanouts shows that the insertion loss spec. of 0.6dB is comfortably met.

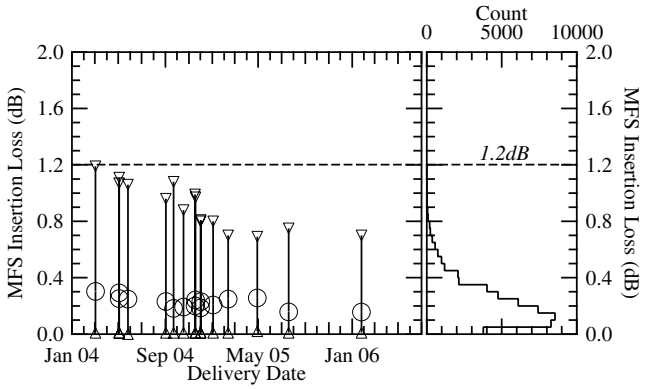

Figure 9: The production trend and histogram of the 12-fibre ribbon connectors (MFS) on rugged fanouts, showing the improvement in insertion loss achieved as production proceeded, always staying within the spec. of 1.2dB maximum.

D. Multi-Ribbon Cable

Rugged high-density multi-ribbon cables carry the signals over the longest span in the CMS Tracker Readout and Control links. These cables were the last items to be produced due to the long time required to obtain accurate lengths for these cables. Lengths must be known before cable production since the termination must be carried out in a controlled manufacturing environment. As for the Fanouts, the optical fibre used is SMF-28 from Corning USA that was ribbonised and made into a rugged 8-ribbon cable by Ericsson of Sweden.

Performance of ribbon connectors is generally worse in terms of insertion loss than that of single-fibre connectors due to the difficulty in achieving geometrical alignment between multiple fibres simultaneously. Insertion loss of the connectors manufactured by Diamond of Switzerland (shown in Figure 10 and Figure 11) was uniformly good throughout

production for the connectors at both ends of the cable (MFS at front-end & MPO at back end).

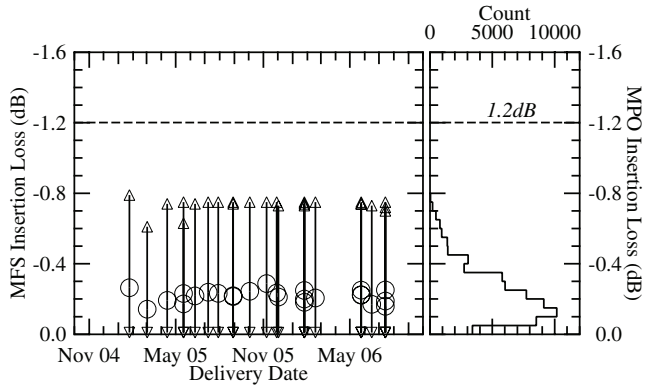

Figure 10: The production trend and histogram of the MFS ribbon connectors on the multi-ribbon cable – all below max. of 1.2dB.

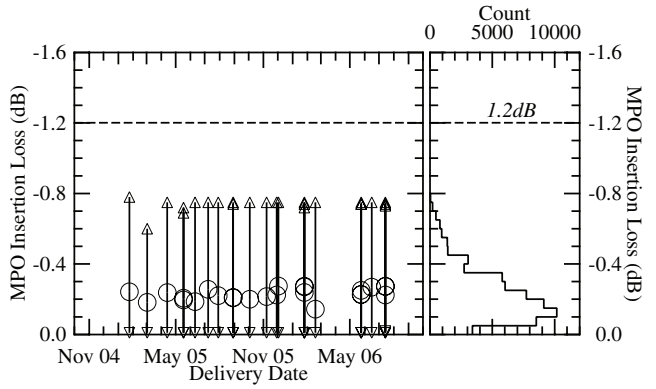

Figure 11: The production trend and histogram of the MPO ribbon connectors on the multi-ribbon cable – all below max. of 1.2dB.

E. Photodiodes

Once development of the digital control system of the CMS Tracker had been completed, several other sub-detectors in CMS decided to use it (ECAL, RPC & TOTEM). This led to an overall doubling of the required number of digital control links and thus of components.

This change was known before the production of photodiodes had ramped-up and the bulk of the production could occur at once. The last quantities of spares and late additions were delivered in mid-2005. Production uniformity was good, with Fermionics of California, USA, taking sufficient margin for device responsivity w.r.t. the specification - as shown in Figure 12. Other parameters showed a similarly good overall performance which gives confidence that the digital link will operate with sufficient margin.

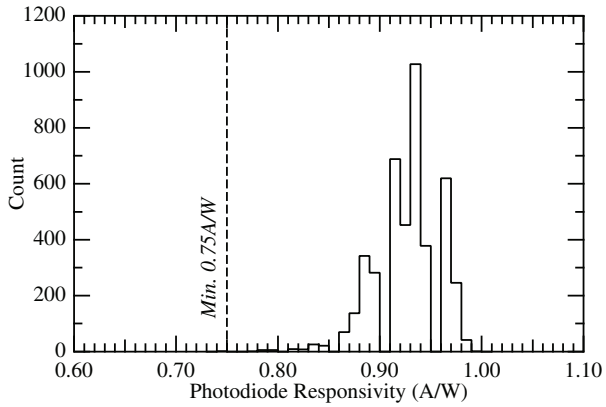

Figure 12: Showing the histogram of Photodiode Responsivity for all delivered components.

F. Digital Transceiver Modules

The digital transceiver (DTRx4) is the only part in the entire system that was a pure COTS part from NGK of Japan. This module was designed for digital operation at 2.5Gb/s per channel, which would yield a bi-directional 10Gb/s link with 4+4 (Tx+Rx) channels between modules.

The first task of qualification was thus to ensure that the modules would operate at the CMS Tracker Control System data rate of 80MB/s. Production of DTRX4 started before funding was fully available for the parts of CMS that were late to make use of the Tracker Control System, which led to a distinct step in the production with a 6-month gap. Finally, funding for spares was long in being made available and came just in time for the last buy notice that preceeded the closure of the manufacturing facility.

Once again the manufacturer's production measurements (Figure 13) show that production met the specified performance targets. The Optical Modulation Amplitude is the size of the signal produced by the Transmitter portion of the DTRx.

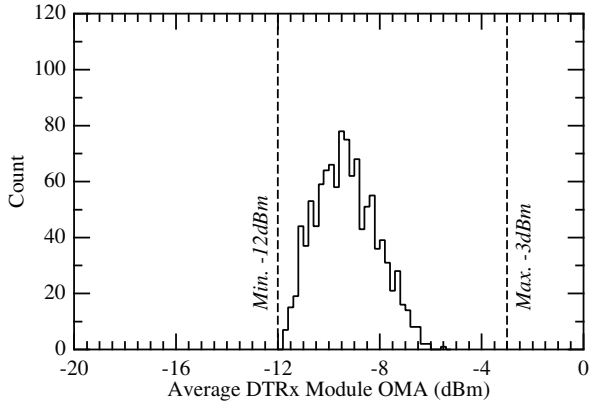

Figure 13: Showing the histogram of the average Optical Modulation Amplitude (OMA) for all delivered DTRx modules.

IV. Verification of Full System Functionality

In the analogue readout system of the CMS Tracker the gain is a critical parameter. The overall gain is the product of the gains of all of the components in the chain, as represented schematically in Figure 14.

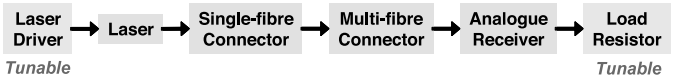

Figure 14: Schematic view of optical readout chain.

Since we have access to the production data (that includes the gain of each component) we can simulate the statistical gain distribution of all links that will be installed [4]. For the case where all gains are combined and no tuning is carried out we achieve the solid line histogram shown in Figure 15 that is centred on the target typical gain of 0.8V/V. As shown in [4], we can tighten the final "in-use" spread to only ± 20% so that the final distribution is bounded by the dot-dash lines of Figure 15.

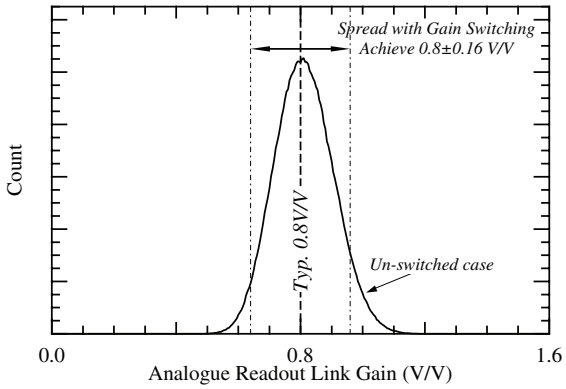

Figure 15: Gain distribution of analogue readout links based on production data of components, showing that a tight tolerance around the target typical gain of 0.8V/V will be achieved.

Having access to the detailed performance measurements has been invaluable to implementing a fully functional analogue readout system. The high delivered performance of all components, especially the optical connectors, would have caused the final installed links to have too high a gain and thus a reduced dynamic range had it not been for the fact that it could be detected early enough to act. By reducing the size of the load resistor at the end of the chain it has been possible to produce a system that will meet the overall dynamic range requirement by re-centring the histogram in Figure 15 on the target gain of 0.8V/V.

This would not have been possible without the detailed production measurements carried out by all the manufacturers. System testing using samples from production also allowed the scaling of gains measured during production at room temperature to the low (-10C) operating temperature of the final installed system.

Using the production measurements of digital link components it is also possible to predict the margin of operation of the installed digital control system. By comparing the signal output of the DTRx module with the minimum allowed signal size (sensitivity) of the front-end receiver with which it must operate we calculate a system margin of 6.8dB including connectors. The digital control system thus has a comfortable margin of operation.

V. Lessons Learned

For a large-scale production such as this it is imperative to have detailed specifications, derived from user requirements, in order to have fruitful discussions with manufacturers at a sufficiently detailed level to overcome the inevitable problems related to the ramp-up of production.

The procedures used to qualify and accept production components must be in place before production starts for discussion with the manufacturer. Failure to do this leads to delays as the discussion on how to do testing is re-opened when a component fails a test.

Ramping up of production took longer than predicted in all cases. This was due to a number of things, including optimism about the complexity of producing custom parts and poor quality of initially delivered components. The timescales on which problems were solved was measured in months, due to the complexity of the processes & components and the need to understand the root causes of problems.

The funding profiles available to large particle physics experiments appear to leave large gaps in procurements as decisions to fund additional parts and/or spares take time. Where the manufacturer is dealing with a relatively standard product, such as connectors, this only poses a problem of fitting the new requirements into their production plan. However, where the components are customized the knowledge of how to produce them may go stale, leading to poorer performance of components produced later.

Overall, production of components took 4 years to complete and, barring problems in start-up and re-starting, went very smoothly thanks to good preparation.

VI. Summary & Conclusions

Component production for the CMS Tracker optical links is now complete, a process that has taken 4 years overall – not including the time needed for contract negotiation and placement. This seemingly lengthy time period was necessary to ensure the high quality of all produced parts.

It has proven to be invaluable to have traceability of component performance through production testing carried out at the 100% level. This has allowed us to verify the proper functioning of all links (assemblies of components) built.

Acknowledgements

The excellent overall production quality reported here would not have been possible without the diligent and professional attitude shown by all manufacturers mentioned in the text, an effort for which we gratefully acknowledge their contribution.

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n-XYTER - A CMOS Read-Out ASIC for a new Generation of High Rate Multichannel Counting Mode Neutron Detectors

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Abstract

For a new generation of 2-D neutron detectors developed in the framework of the EU NMI3 project DETNI [1], the 128-channel frontend chip n-XYTER has been designed. To facilitate the reconstruction of single neutron incidence points, the chip has to provide a spatial coordinate (represented by the channel number), as well as time stamp and amplitude information to match the data of x- and y-coordinates. While the random nature of the input signals calls for self-triggered operation of the chip, on-chip derandomisation and sparsification is required to exploit the enormous rate capability of these detectors ($\geq 4 \times 10^6 \mathrm{cm}^{-2}\mathrm{s}^{-1}$). The chosen architecture implements a preamplifier driving two shapers with different time constants per channel. The faster shaper drives a single-pulse discriminator with subsequent time-walk compensation. The output of this circuit is used to latch a 14-bit time stamp with a ≤ 2 ns resolution and to enable a peak detector circuit fed by the slower shaper branch. The analogue output of the peak detector as well as the time stamp are stored in a 4-stage FIFO for derandomisation. The readout of these FIFOs is accomplished by a token-ring based multiplexer working at 32 MHz, which accounts for further derandomisation, sparsification and dynamic bandwidth distribution. The chip was submitted for manufacturing in AMS's C35B4M3 0.35µm CMOS technology in June 2006.

I. Neutron Physics' Experiments

High energy physics usually relies on accelerators as particle sources. These machines also provide a suitable time reference (the so-called bunch clock) which is used to disentangle the signals resulting from different particle collisions. Thus position reconstruction can be easily realised by deriving a coincidence period from the accelerator's timing.

In contrast, neutron physics' experiments, as sketched in fig. 1, use (at least on the time scale of interest) continuous sources like nuclear reactors. In turn the appearance of scattered neutrons is Poissonian distributed and not related to any external signal. As a consequence, the synchronous readout of such a detector with an external clock would require an enormous readout bandwidth. Alternatively a self-triggered system can be employed, which would allow for derandomisation and sparsification already in the front-end electronics.

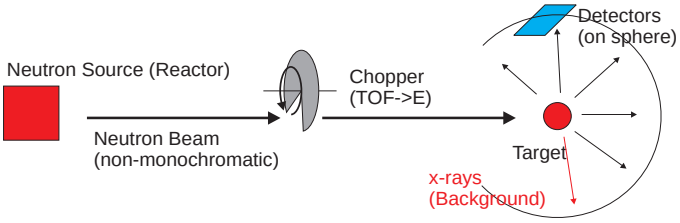

Figure 1: Strongly simplified layout of a typical neutron scattering experiment. The chopper wheel is used for energy determination, based on a slow (µs) TOF measurement.

II. The DETNI Detectors

Targeted for the next generation of neutron sources, in the framework of the EU FP-6 NMI3 project DETNI a new generation of neutron detectors for imaging and time-of-flight applications is being developed. In particular these detectors are:

- Gd-Si-MSD, a double-sided Silicon-Microstrip detector with a solid ^{157}Gadolinium converter.
- CASCADE, a gaseous detector using multiple GEM[1] foils coated with a ^{10}Boron converter.
- Gd/CsI MSGC, a hybrid MSGC employing a solid ^{157}Gadolinium converter.

Any of these detectors is characterised by a high number of readout channels per coordinate (up to 640 × 640 for the Si-MSD) and a very high event rate, unprecedented in single-event counting 2-D neutron detectors [2].

[1] Gas Electron Multiplier

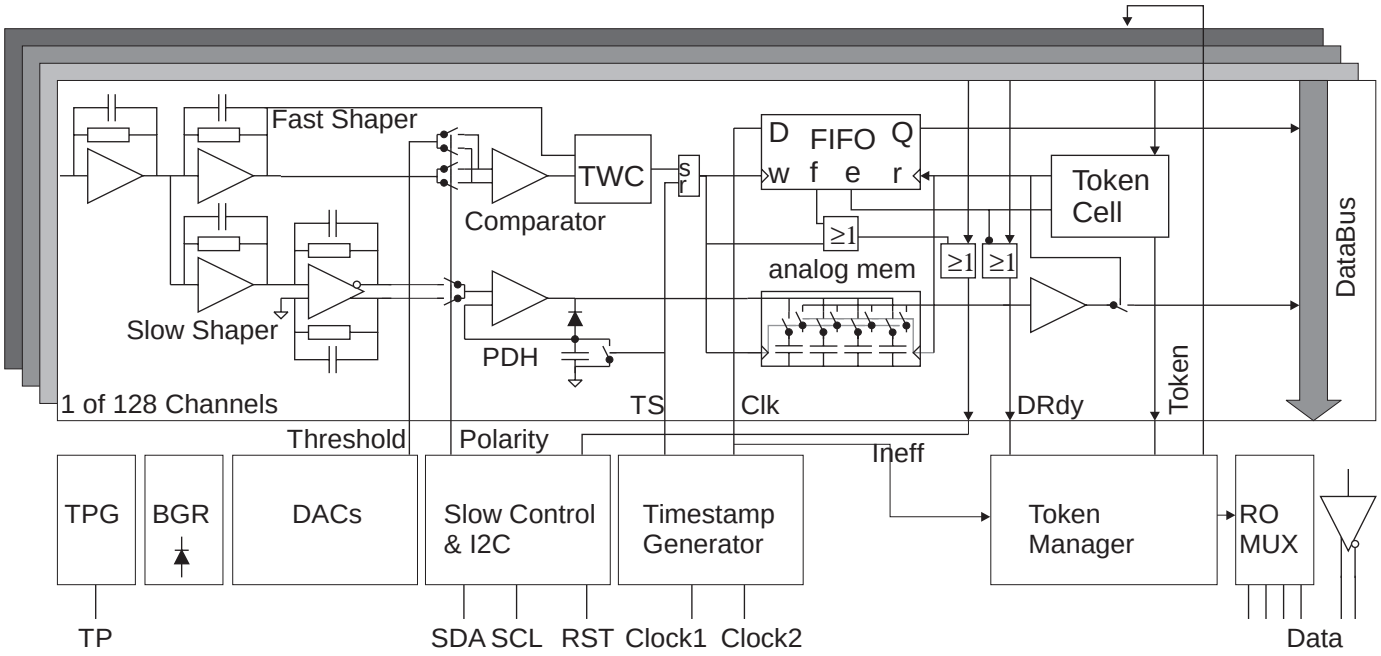

Figure 2: Block schematic of the n-XYTER 1.0 chip. The top part shows one of the 128 channels.

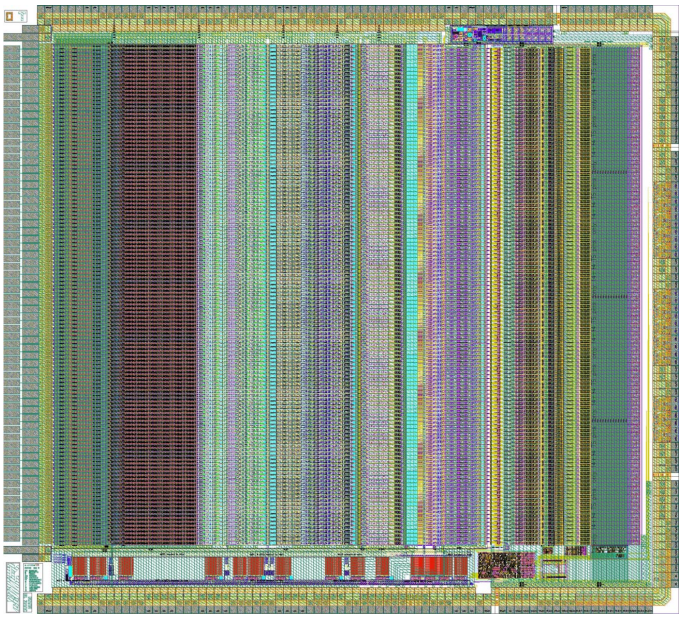

Figure 3: Layout of the 8.0 mm × 8.8 mm n-XYTER 1.0 chip.

III. The n-XYTER 1.0 Chip

To read out the CASCADE and Si-MSD detectors with event rates up to 100 MHz at a 10 % dead time loss, the n-XYTER[2] 1.0 chip has been developed. It integrates 128 channels. To cope with the high-rate statistical input signals, the front-end part of the chip uses an asynchronous, data-driven architecture, which relies on time stamp latching triggered by a time-walk compensated discriminator. The back-end part of the chip is clock-synchronous and accomplishes the derandomisation, sparsification and bandwidth-distribution tasks to limit the dead-time loss. A simplified schematic is shown in fig. 2. After a front-end only test chip[3], the full-scale 128 channel n-XYTER 1.0 chip has been submitted in June 2006. The chosen process, AMS C35B4M3 (0.35 µm) CMOS, includes linear polysilicon capacitors, 4 metal layers, a thick, low impedance top metal layer and MIMCAPs[4]. The latter two features have been extensively used for power supply filtering, implemented via low-impedance connections and local blocking capacitors. The layout of the 8.0 mm × 8.8 mm chip is shown in fig. 3. The following description will follow the chip's signal path:

A. Front End

A charge sensitive preamplifier, constructed around a folded cascode circuit forms the input stage. For its superior noise performance, an NMOS input transistor has been chosen. Unlike conventional readout chips, the signal path is split into two branches after the preamplifier:

- A fast CR – RC shaper, driving the timing-critical path performing the time measurement.
- A slow CR – $(RC)^2$ shaper driving the more noise-critical measurement of the deposited energy.

While the fast branch relies on a single-ended topology for the shaper, the slow branch implements a fully differential second shaper stage. This allows the selection of the correct signal polarity for the subsequent peak detector and hold circuit for either polarity of the input signal. The schematic of the front-end is shown in fig. 4, while figs. 5,

[2] neutron physics X Y T and Energy deposition Readout chip
[3] DETNI_FE10, submitted in 2005 [3]
[4] Metal InterMetal CAPapacitors - Capacitors between two metal layers

6 and tab. 1 detail the performance of this circuit, which had been previously submitted on the DETNI_FE10 chip [3].

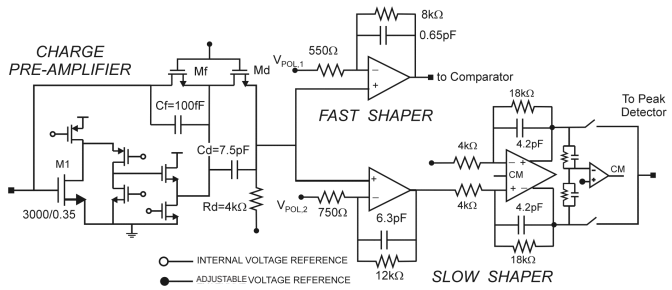

Figure 4: Schematic of the front-end, including the FAST and SLOW shaper branches.

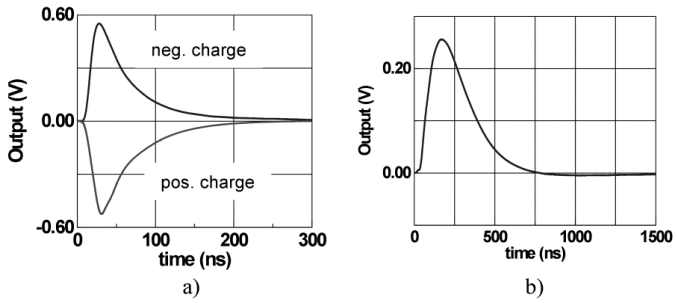

Figure 5: Measured pulse shape of the front-end (from the DETNI_FE10 chip [3]). a) FAST channel b) SLOW channel

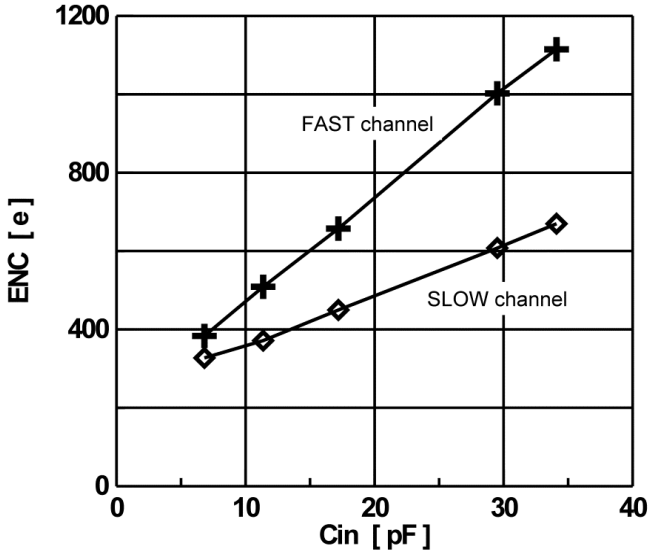

Figure 6: Measured noise performance of the two branches of the front-end, measured on the DETNI_FE10 chip [3].

Table 1: Performance of n-XYTER 1.0's front-end. The measurements were performed with the DETNI_FE10 test chip [3].

	FAST channel	SLOW channel
ENC	$200\,e^- + 26.9\,e^-/pF$	$233\,e^- + 12.7\,e^-/pF$
Rise Time[a] (1 . . . 99 %)	18.5 ns (measured) 20.8 ns (simulated)	139 ns (measured) 138 ns (simulated)

[a] Measured with 30 pF input capacitance

B. Discriminator and Time-Walk Compensation

To correlate the signals on the x- and y-plane of a detector by means of a time stamp, a discriminator has to detect these signals without any dependency on the signal amplitude. The standard approach to accomplish this is the use of a constant-fraction discriminator, which uses a delay line to generate a bipolar pulse. However, delay lines are not available in CMOS technology and a different solution has been chosen [4]: As shown in figure 7, a single pulse discriminator is followed by a voltage controlled delay circuit, which is used to compensate the time walk. With this circuit a reduction of the comparator's time dependency to less than 2 ns has been achieved, as shown in fig. 8. Further results from this circuit are shown in figs. 9 and 10.

The output of the time walk compensation circuit is not only used to latch a 14 bit timestamp, but also to arm the peak detector and hold circuit connected to the slow channel.

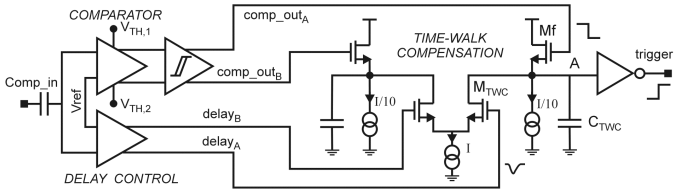

Figure 7: Schematic of the discriminator and time walk compensation circuit. The signals on the delay_a and delay_b inputs control the delay of the circuit by modifying the discharge current of C_{TWC}.

C. Peak-Detector and Hold Circuit

To detect and hold the peak amplitude of the slow channel, the classical peak detector and hold circuit proposed in [5] was adopted. It is depicted in fig 11.

D. Channel FIFO

The slow timing of the peak detector and hold circuit (≈ 150 ns peaking time) permits the synchronisation of the front-end's data with the 32 MHz readout clock already at this stage, without any possibility to introduce additional dead time. The channel FIFO features four stages of analogue and 14-bit wide digital memory. It is used to buffer the data until the channel is granted the multiplexer bus

for a readout cycle.

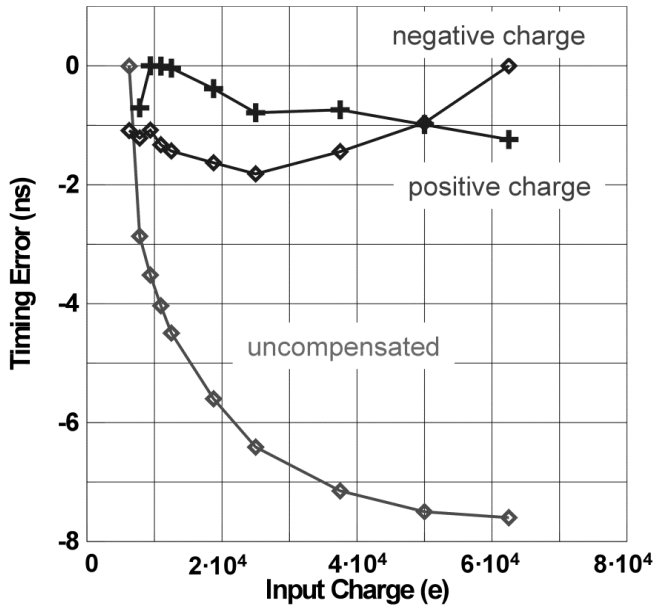

Figure 8: Measured time walk after the discriminator and time walk compensation circuits: The timing error is reduced to ≤ 2 ns (results from the DETNI_FE10 test chip [3]).

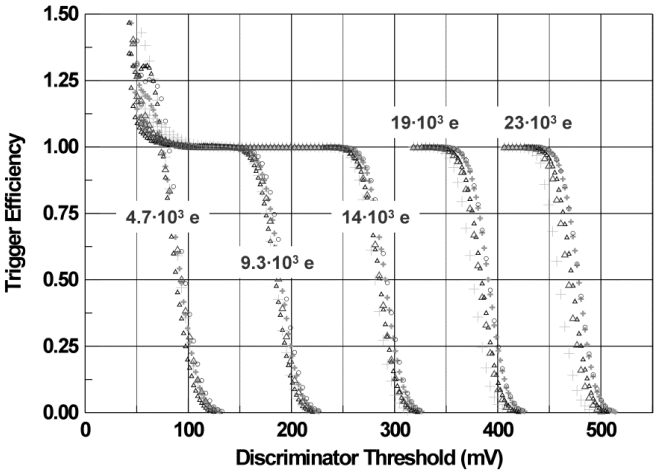

Figure 9: Measured trigger efficiency for different input charges (results from the DETNI_FE10 test chip [3]).

E. Multiplexer

The readout multiplexer is actually implemented as a bus, featuring a token-ring based arbitration schema. It is depicted in fig. 12. This way the readout bandwidth is equally distributed among all channels in case of saturation, while a single channel can still exploit the complete bandwidth, if there are no concurrent requests. Besides the analogue amplitude information and the time stamp, each channel also transmits its ID to provide a spatial coordinate.

The token is injected into the token ring on the rising edge of the 32 MHz readout clock and latched on the falling edge by the token cell of the first non-empty channel. This channel is granted the readout bus for the next clock cycle, while the token is passed on to the next non-empty channel on the next rising edge of the clock. The token manager itself works like a token cell, driven by the logical AND of all channels' empty signals, i.e it will only latch the token, if there is no readout data available.

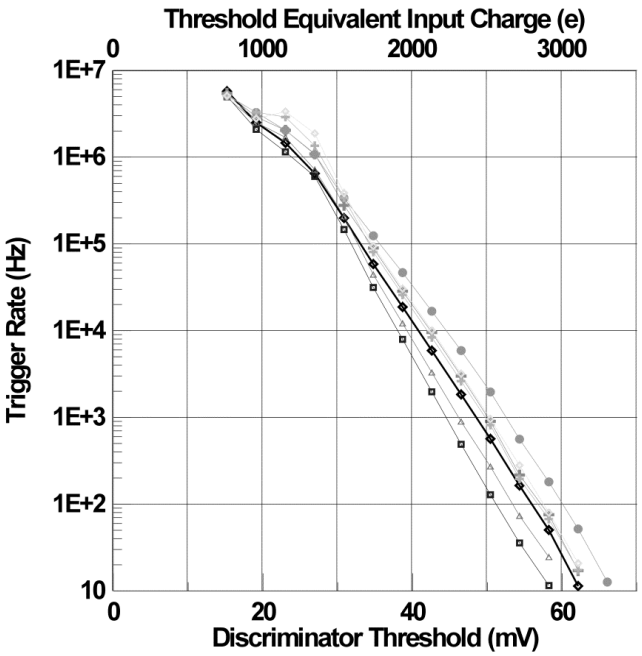

Figure 10: Trigger rate with no signal applied to the input (measured with 28 pF total input capacitance on the DETNI_FE10[3] test chip).

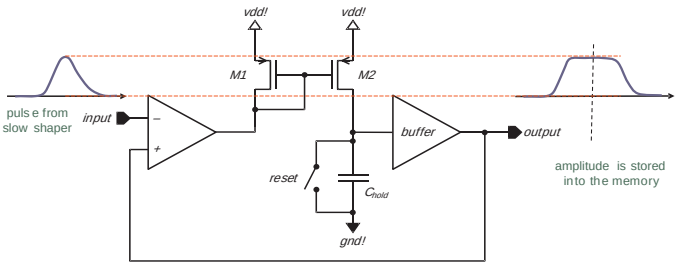

Figure 11: Block schematic of the peak-detector and hold circuit.

Looking at this scenario, the worst case is to have data only in the last channel. Then the token has to pass 127 channels in half a clock cycle, which is not possible for higher temperatures and/or slower corners of the manufacturing process. To overcome this, a token bypass is activated for a group of 16 channels if these are empty, which shorts the token's delay by a factor of 16. In the worst case, the token now has to pass 7 bypasses and 15 token cells to reach the last channel, which ensures the chip's operation even under the worst manufacturing and

temperature conditions.

While the analogue data is driven off-chip via a differential buffer synchronous to the 32 MHz readout clock, time stamp, channel number and other digital data are multiplexed to 128 MHz and driven off-chip via 8 LVDS lines.

While the front end parts of the chip have been tested on the DETNI_FE10 [3] chip, the channel FIFO and readout multiplexer have been evaluated together as an FPGA implementation before the components were implemented on the n-XYTER 1.0 ASIC.

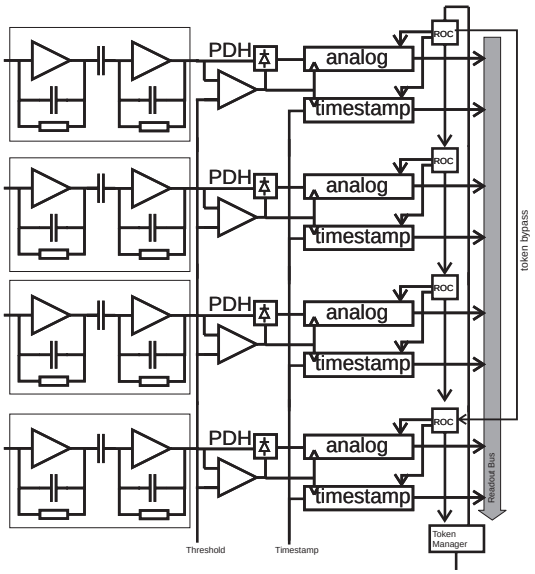

Figure 12: Simplified block schematic showing the readout structure of the n-XYTER 1.0 chip. The token cell is part of each channel's readout cotroller (ROC).

F. Time-Stamp Generator

The time stamp is derived from a 256 MHz clock fed to the chip. A delayed copy of this clock is generated via an adjustable delay line. A logic OR of these two clocks results in a 512 MHz signal used as the time stamp's LSB, fixing the time resolution to ≤ 2 ns. The 13 MSBs are the Gray-encoded output of a counter, derived from the original 256 MHz clock. A global reset signal zeroes this counter and empties all channel FIFOs.

G. Slow Control and Monitoring

A standard I^2C-interface provides access to the control and monitoring functions of the n-XYTER 1.0 chip. It controls the DACs to set e.g. the bias currents of the analogue stages and the discriminator threshold. The latter features circuitry for correction on a per-channel basis to account for interchannel variations. Furthermore, a sophisticated test signal generator featuring programmable amplitudes channel masks and injection points has been included. As an additional feature, counters for latched and rejected events allow an experimental evaluation of the system's efficiency.

IV. Summary

For the new generation of neutron detectors of the EU NMI3 project DETNI [1] a 128 channel readout chip has been developed. It was submitted for manufacturing in June 2006. Its architecture has been taylored to fit the statistical nature and rate of the signals expected from future neutron sources. Thus each channel's charge sensitive preamplifier drives two shapers:

1. A fast one facilitating a time measurement via a time-walk compensated discriminator latching a time stamp.

2. A slow one for energy measurement via a peak detector and hold circuit.

The further signal path includes a 4-stage FIFO per channel for derandomisation and a token-ring based readout multiplexer for sparsification and dynamic bandwidth distribution. While the front-end was was tested on the DETNI_FE10 [3] test chip, the back-end signal path was successfully tested with Monte Carlo data on an FPGA prior to the ASIC implementation.

Due to the unique properties of this architecture an implementation with a lower number of channels (MSGCROC), targeted for applications with even higher rates, has been developed.

The future plans, besides the test of n-XYTER 1.0, include also radiation hard versions of the n-XYTER, intended for future heavy ion experiments.

V. Acknowledgments

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Setup for testing LHCb Inner Tracker Modules

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Abstract

The Inner Tracker of the LHCb experiment is a silicon microstrip detector consisting of 336 detector modules with either one or two sensors. The module production is now underway and we present here the setup employed for module testing during the production. The setup is based on the same electronics that will be used in the final experiment. We perform burn-in and ageing tests with the help of a custom made Temperature Cycling Box controlled with LabVIEW under Windows. The DAQ is done in another PC running Linux. Here we integrate the different C/C++ libraries used to communicate to the LHCb Time and Fast Control system, Experiment Control System and Data Acquisition.

I. The LHCb Experiment and the Inner Tracker

The LHCb experiment [1] is one of the four large experiments at the new Large Hadron Collider (LHC) at CERN. It is a single-arm forward spectrometer, with an acceptance from 15 to 300 mrad, dedicated to B-physics. The tracking system is formed by the Vertex detector (VELO), the Trigger Tracker (TT) station and the Tracking stations (T1-T3) behind the magnet which are split into the Inner Tracker (IT) and the Outer Tracker (OT).

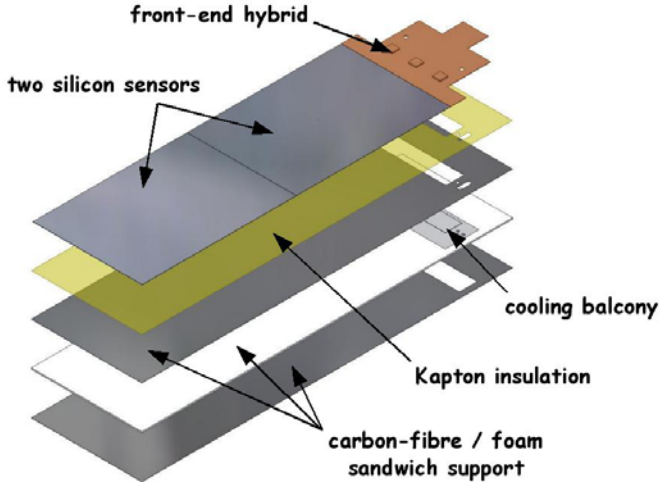

Figure 1: Inner Tracker module composition

The Inner Tracker [2] is a silicon detector covering the high multiplicity region around the beam pipe. With an active area of 4.3 m^2 (1.3 % of total acceptance area of LHCb) and 129,024 channels, it covers the 20% of the tracks. Each station consists of four boxes, and 4 layers of seven modules per box. The boxes on top and bottom of the beam pipe have 1-sensor modules of 320µm thickness while the boxes at the right and left have 2-sensor modules (410µm). The silicon sensors are single sided 108 mm long, 384 AC coupled readout strips, a pitch of 198 µm and a width over pitch ratio w/p = 0.25. The three very front-end readout chips, called Beetles [3], are mounted on an electronics hybrid. A high thermal conductive carbon fibre is used as a support of the sensor/s, the ceramic pitch adapter with gold strips, the hybrid and an aluminium piece "balcony" for positioning and cooling, as shown in Figure 1.

II. Testing Hardware

We use for the module testing a custom made temperature cycling box with temperature and humidity control. It provides a capacity for 6 modules in a volume of 25x30x50 cm^3. The box and its control electronics were fully designed and built in Santiago. It is based on water cooled Peltier elements and allows to maintain fixed temperatures from +50 ºC to -15 ºC with an accurancy of 1 ºC.

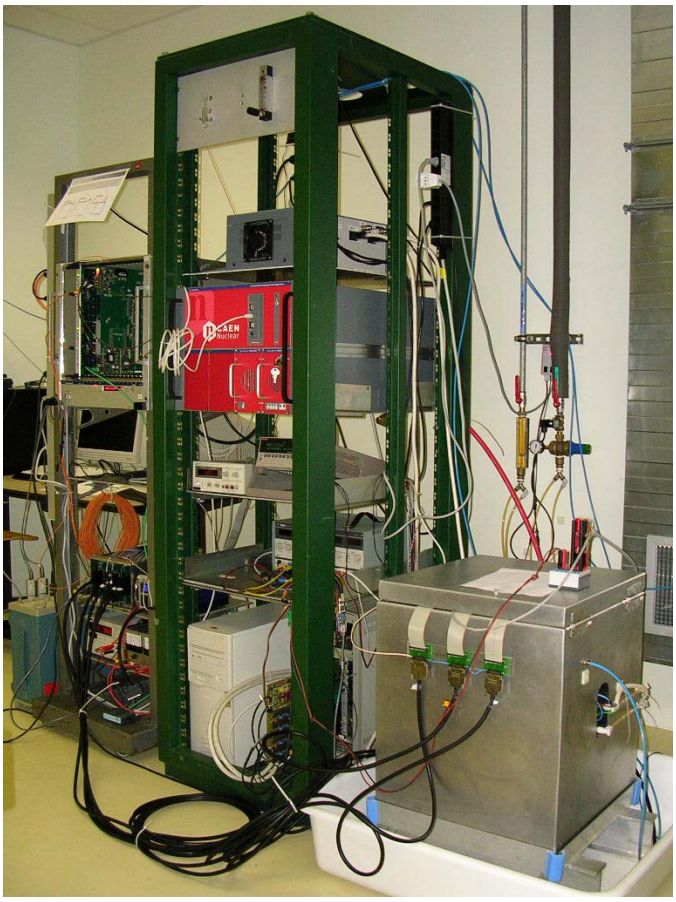

Figure 2: IT module burn-in and temperature cycling setup

The DAQ setup used in the testing uses the same electronics as the final experiment. The frontend readout electronics: Control Boards and Digitizer Boards, the clock and trigger distribution: Readout Supervisor [4], the common LHCb readout board: TELL1 [5], high voltage: CAEN system with module A1511B. The IV-curves are done using a Keithley picoampermeter and the metrology using a XY table with a Leica microscope. Temperatue cycling box and DAQ setup can be seen in Figure 2.

III. Testing procedures

We produce the modules in two sites [6]. In Lausanne the EPFL group glue the sensor, pitch adapter, hybrid and balcony into the support. In the clean room at CERN the USC/EPFL group do the bonding, testing and metrology as well as the final mounting of the modules in the boxes.

Once the modules arrive to CERN we do IV-curves before and after the bonding, then we perform the temperature cycling/burn-in over 44 h, 30 temperature cycles from -5 ºC to 40 ºC. A temperature cycle involves 8 temperature points: 20 ºC, 40 ºC, 20 ºC, 10 ºC, 0 ºC, -5 ºC, 0 ºC, 10 ºC. In order to test modules at different temperatures we take data every 9 temperature points, once per cycle. All hybrids have passed a previous burn-in test in Heidelberg before module assembly. In every data taking we test for open/shorted channels by injecting charge via the Beetle test-pulse in 30K events. After the burn-in we test for pinholes, then we do the metrology of the modules and store them in an inert atmosphere until they are mounted in detector boxes. In Figure 3 the failure ratio for the production chain can be seen.

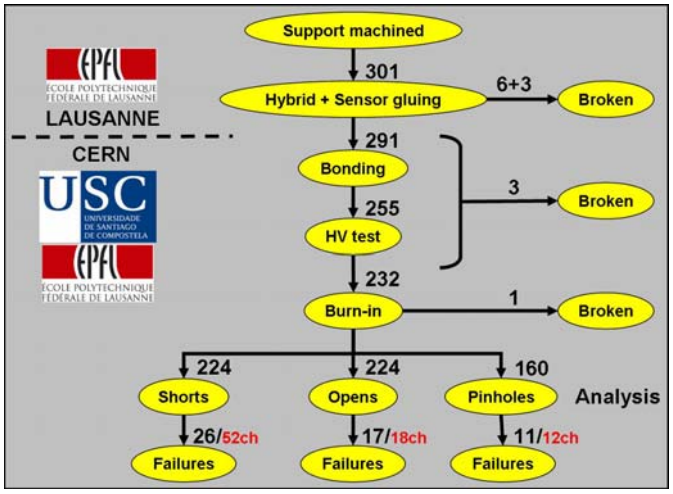

Figure 3: IT module production scheme by August 2006

IV. Testing software

The control of the testing setup is based on LabVIEW. A PC running windows controls the Temperature Cycling Box through the parallel port while another PC running Linux acquires data. The high voltage is controlled via an OPC server. C++ based readout software allows to perform different actions as ADC timing scan, pedestal acquisition, test pulse delay scan. We are forced to test either short or long modules in the same burn-in as they have different pulse timing due to the different input capacity. Some software and firmware adaptations were needed in order to run the final LHCb trigger, control and readout electronics.

V. Analysis

With the data collected during the burn-in we characterize modules and look for bad channels [7]. Raw and common mode suppressed noise are monitored for different temperatures. We also perform a delay scan to determine the pulse-shape of every channel at different temperatures. Shorted channels are identified by smaller signal heights due to larger load capacitance caused by two strips connected to the front-end channel rather than just one. Unbonded or open channels are identified by larger signal heights due to smaller load capacitance. Pinholes are identified in a different test by artificial low noise due to preamplifier saturation under infrared illumination at room temperature. Figure 4 shows a delay scan and shortcut channels for module 121.

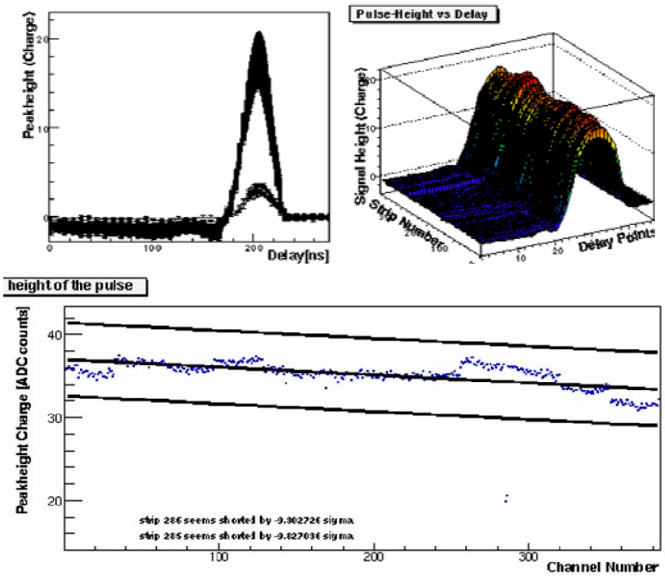

Figure 4: Delay scan and open/short analysis for a IT module

VI. Bonding

We use two wedge bonding machines to perform the module bonding, a Kulicke and Soffa 8060 and a Delvotec 6319. Both use 25 µm diameter aluminium wire. We have encountered large variations in the bondability of pitch adapters, so we have to check and possibly adapt the bond parameters of each individual module by pulling some test bonds placed on strips of the pitch adapter. For this we use a DAGE 3000 pull tester. Figure 5 shows the detail of the bonding of a Beetle chip.

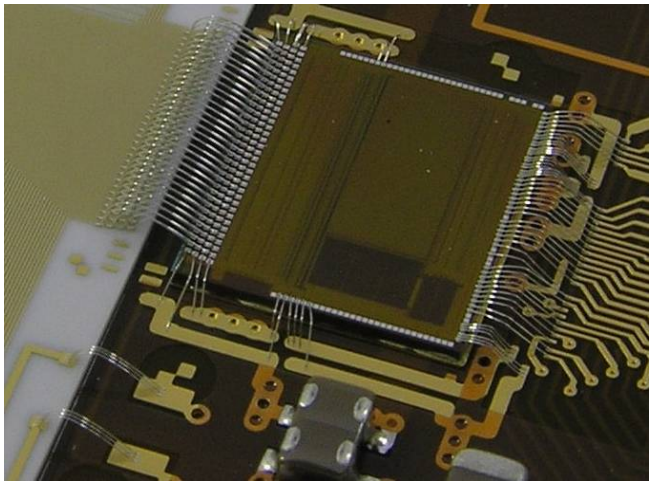

Figure 5: Beetle to pitch adapter bonding in 4 rows of 40 µm pitch

VII. Box assembly

We have assembled the first IT box and we have tested the interface PCB used to interconnect the modules to the external world and to distribute the high voltage lines. The 6 carbon fibre support frames are complete and ready for cabling and installation in the pit. Half of the detector boxes are already produced in Santiago and delivered to CERN. The production of the other half is well advanced.

VIII. Summary

We have presented the setup employed in the testing of LHCb Inner Tracker modules and testing procedures. Using this setup we have tested so far about 250 detector modules and encountered one electronic failure of a module during the temperature cycling. The testing is running smoothly and overall production is progressing well

IX. References

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[4] LHCb TTC. Readout Supervisor

http://lhcb-online.web.cern.ch/lhcb-online/TFC/default.html

[5] TELL1 http://lphe.epfl.ch/~ghaefeli/

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http://lphe.epfl.ch/~lhcb/itproduction/

[7] Electrical test and quality assurance during production CERN-THESIS-2005-052

Large scale production of the Multi-Chip Module of the ATLAS Level-1 Calorimeter Trigger

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Abstract

The Multi-Chip Module (MCM) is the main processing block of the Pre-Processor System in the ATLAS Level-1 Calorimeter Trigger. The MCM holds a dedicated signal-processing ASIC and a Phos4 timing-chip together with seven commercial dice mounted on the substrate. Those are four FADCs and three LVDS-serializers.

The MCM contains the main functionality of the Pre-Processor System, namely the digitization, calibration and Bunch-Crossing-Identification of calorimeter signals. Two output data streams are produced by the MCM. A real-time stream transmits the processed data to the subsequent trigger processors. A readout stream provides readout information of the Pre-Processor.

The MCM is the smallest exchangeable unit of the Pre-Processor. The ATLAS experiment will have 2048 MCMs installed in the Pre-Processor system. Including spares, the total number runs up to 3000. The production phases of the MCMs and test procedures for quality control at different stages of the production are presented.

I. Introduction

The ATLAS trigger system is based on three levels of event selection. These levels are the Level-1 Trigger, the Level-2 Trigger and the Event Filter. The trigger system reduces the initial bunch-crossing rate of 40 MHz to the rate of selected events of 200 Hz. The first selection step is performed by the Level-1 Trigger system , reducing the initial event rate to about 75 kHz [1]. The Level-1 Trigger consists of three building blocks - the Calorimeter Trigger, the Muon Trigger and the Central Trigger Processor (CTP). The Calorimeter Trigger receives about 7200 analog signals from electromagnetic and hadronic calorimeters, summed in projective Trigger Towers (TT) with a reduced granularity in $\eta \times \phi$ of 0.1x0.1. The results from the Calorimeter Trigger together with those from the Muon Trigger are sent to the CTP, which generates the final Level-1 Trigger decision.

The Level-1 Calorimeter Trigger consists of three subsystems: The Pre-processor (PPr), the Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The Pre-processor receives the analog input signals from all ATLAS calorimeters, digitizes and synchronizes them; in addition it performs the bunch-crossing identification (BCID) and uses a lookup table to calibrate the transverse energy (ET). The digitally processed data are then transmitted to the CP and JEP subsystems. The CP subsystem identifies possible isolated electrons, photons and semi-hadronic τ decays. The JEP subsystem identifies jet objects and calculates the global sums for the E_T-miss and sum-E_T triggers. The multiplicities of objects which pass programmable threshold conditions on transverse energy are sent to the CTP . Types and coordinates of identified objects are also sent as Regions of Interest (RoIs) to the second-level trigger system (LVL2) [2]. In order to achieve the required latency of 2μs the trigger is implemented as a system of purpose-built hardware processors. The Multi-Chip Module is the key component of the Pre-Processor system. It holds the PPrASIC chip, where the main data processing functions are implemented.

The testing procedure as well as large scale production of the MCMs will be described in this note. Section II gives an overview of the Pre-processor system as a whole. The Multi-Chip Module functionality and production technique are described in the Section III. The test-setup and test procedures are presented in the Section IV. Finally Section V gives a description of the PPrASIC wafer production and the production cycle of the MCM.

II. The Pre-Processor System

The Pre-Processor System performs complex processing of the analog trigger tower signals, which are received from the electromagnetic and hadronic calorimeters. After reception of differential analog signals, Analog Input boards (An-In) of the

Pre-Processor convert them into unipolar signals and adjust a zero baseline for each input signal.

The rest of the signal processing takes place in the MCM and will be described in the following section. The data processing in the Pre-Processor is done at rate of 40 MHz with a maximum latency of 15 clock cycles (375ns)[3]. As a result the Pre-Processor generates three digital streams, containing the transverse energy deposits with the corresponding bunch-crossing. These data are serialized and distributed via LVDS links at 400Mbit/s to the CP and JEP subsystems. In addition the Pre-Processor provides a readout stream for system diagnostics. The digitized raw data and pre-processed results are sent to the Data Acquisition system (DAQ) as soon as an event has been accepted by the Level-1 Trigger.

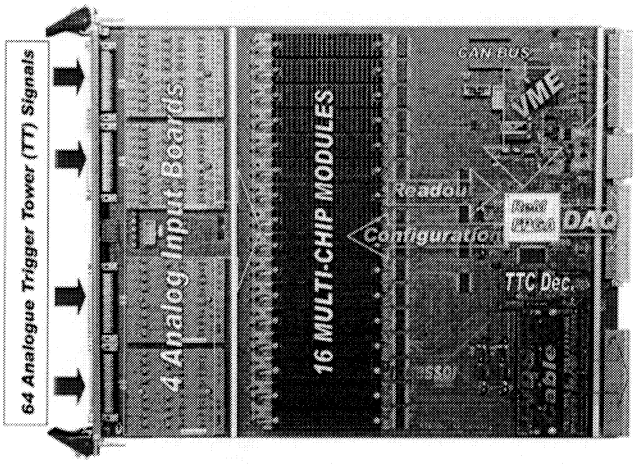

Figure 1: The Pre-Processor Module

The complete Pre-Processor system consists of 8 crates. Each crate contains 16 Pre-Processor Modules (PPMs). The 64-channel PPM is realized as a 9U VME Printed Circuit Board (Figure 1). Each PPM carries 16 MCMs and 7 daughter cards. The 4 An-In boards adjust the analog input signal, before digital processing by MCMs. After digital processing signals are sent to the LVDS Cable Driver (LCD) card where they are routed and fanned out before transmission to the subsequent subsystems. The readout is done by means of Rear G-Link Transmission Module (RGTM), which send the readout data to the ReadOut Driver (ROD) . Temperatures of all units on PPM, as well as board internal supply-voltages are read out by a CAN-controller. The entire data space of the module is accessible through VME.

III. The Multi-Chip-Module

Almost all signal processing tasks of the PPM are performed inside the MCM. Each MCM processes four trigger signals.

A. MCM functionality

MCM is designed as a compact module, which holds 9 components in non-packaged form . A fully assembled MCM without lid is shown in Figure 2.

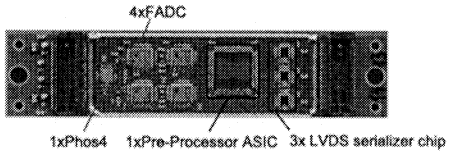

Figure 2: The Multi-Chip Module

The chips on the MCM and their corresponding tasks can be summarized as follows:

- Four Flash ADCs (AD9042, Analog Devices)
  - these FADCs digitize the input signals with 10-bit resolution and a sampling frequency of 40 MHz;
- Timing chip (PHOS4, CERN Microelectronics Group)
  - the Phos4 delays the FADC clock with respect to the system clock in steps of 1 ns within a LHC clock cycle;
- Pre-Processor ASIC (PPrASIC)
  - Each PPrASIC processes four digital channels and provides readout. Further tasks are: real-time bunch-crossing identification, channel synchronization, final transverse-energy calibration, pedestal subtraction, pre-summing of jet elements, bunch-crossing multiplexing, serial data transmission;
- Three LVDS serializer chips (DS92-LV1021, National Semiconductor)
  - The LVDS serializer chips transmit the processed data to the subsequent processors at a rate of 400 Mbits/s;

A simplified block diagram for the processing of one channel is depicted in Figure 3.

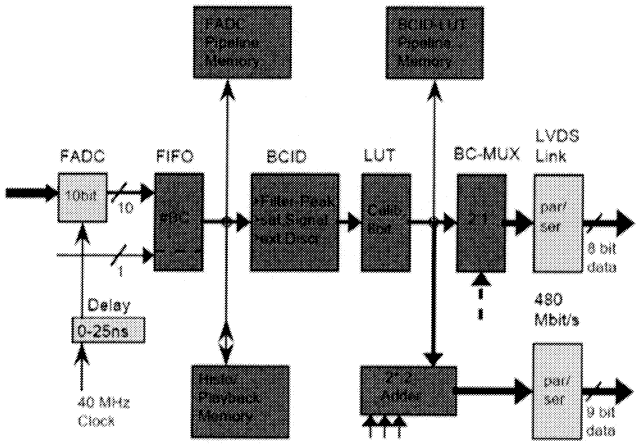

Figure 3: Block diagram for the processing of one calorimeter channel on the MCM

The dark functional blocks are integrated on the PPrASIC, whereas the shaded blocks live on other chips of the MCM. The incoming analog signals are digitized with 10-bit resolution at a sampling frequency of 40 MHz by the FADC. The digitized data are latched into the PPrASIC, which performs all digital processing. The PPrASIC generates three real-time streams of data, which are serialized by the LVDS serializers. 10-bit LVDS data words are sent to the CP and JEP systems. The CP receives two data streams containing multiplexed energy values from four channels. The third stream to JEP contains the energy sums of these four channels. These pre-sums form the jet elements for the JEP. Two serial interfaces provide the readout of raw FADC data as well as all energy values resulting from the BCID algorithms and Look-Up-Table (LUT) calibration. The data can be read out upon each Level-1 Accept. Additional data produced by histogramming and rate-metering blocks in the PPrASIC, come within the readout stream but independently of a trigger decision. These data can be useful for monitoring of trigger and calorimeter performance studies. The detailed description of the MCM and PPrASIC tasks can be found in [6].

B. MCM production technique

The base of the MCM is a multilayer high-density printed circuit board (PCB) with microvias for layer-to-layer contact. The PCB has 4 copper layers, 2 epoxide Prepreg layer and 1 FR4 layer. The copper layers of the PCB are interleaved with Prepreg layers and FR4 core in the center. FR4 material is made of epoxy resin that saturates woven fiberglass. The required micro vias are formed by laser drilling. The combination of this semi-flexible PCB sticking to a 0,8 mm copper plate - to realize an effective heatflow - is manufactured by Würth Elektronik company [8] . This technology is listed by the brand name TWINFLEX®.

All "foot-prints" of dice on the substrate contain a copper-area, covered by a thin gold layer in the center. These areas are studded with so-called "thermal vias" (no electrical function), whose purpose is solely the conduction of dissipated heat to the copper-plate. All nine dice are placed and fixed using heat-conducting glue. A wire-bonding machine connects the pads on the dice to the pads on the substrate. After bonding is done, the "glob-top" coverage is applied to the vulnerable components on the MCM to protect them from environmental, mechanical and electrical damage. The MCM substrate is covered by a brass-lid; it is soldered onto a copper-frame in the top-layer and serves as a electro-magnetic shield against imposed noise from hostile surroundings. And finally a metal body made of studded metal (with enlarged surface) is glued to the copper-plate to provide exchange of dissipated heat with the surrounding air-flow in the electronics crates[7].

Components such as capacitors and resistors are connected to the multi-layer structure using surface-mount technology (SMT). On each end a 60 pin SMD connector from SAMTEC (BTH030) connects the MCM to the Pre-Processor Module[3].

IV. Production tests

Being a complex electronic device, the MCM needs to be thoroughly tested. The MCM test-setup is shown in Figure 4.

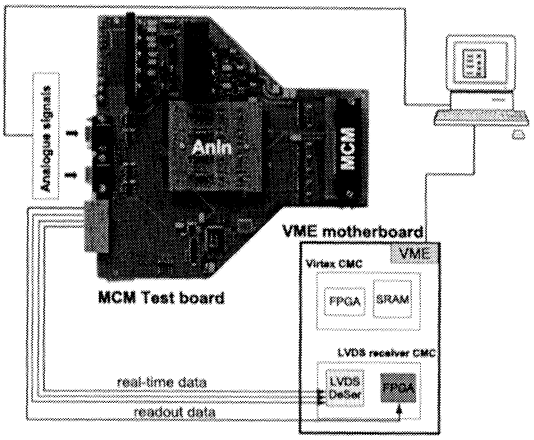

Figure 4: MCM test-setup

A. Test environment

The test environment has VME-infrastructure, which provides computer-controlled input generation and output capture. It consists of:

- a VME crate with a general purpose motherboard containing two daughter boards: LVDS receiver Common Mezzanine Card (CMC) and Virtex CMC,
- a specially developed MCM Test Board,
- a standard graphics card used as analog signal generator ,
- a computer, on which the test software is running.

The main block of the test setup is the MCM Test Board. It emulates the MCM environment on the PPM and holds two components of the final Pre-Processor Module: an Analog Input Board and the MCM to be tested.

The signal generator is programmed to generate the expected pulse shapes, "typical signals" obtained from test-beam studies and special test vectors. The analog output from the signal generator is sent to the analog input of the Test Board. After transformation is done on the An-In board, the incoming analog signal propagates to the MCM for further processing. The output of the real-time path is received by the LVDS receiver Common Mezzanine Card (CMC). The data of the readout path are received by a Xilinx FPGA, on the same CMC card. The data received by the LVDS receiver CMC are transmitted to the Virtex CMC card, which hosts a large SRAM buffering the data of the real-time path. Finally the data from both, the real-time and the readout path, are sent via FPGA on the motherboard to a Dual Ported RAM (DPRAM). This memory is read out by VME and thus data are transmitted to a computer, where they are analyzed.

B. Tests and Test software

A multitude of separate tests were combined in specially developed software for the production tests.The tasks of the test

software are: a complete test of all functions of PPrASIC and MCM in automatic mode, a detection of nonfunctional blocks on the MCM, a provision of a test environment for further investigation of the faulty MCMs. The last two functions are required for the repair cycle, where the faulty chips have to be identified and replaced.

The test software consists of three main packages: the configuration package, the analog handler, the test handler.The first package is responsible for register settings used in the tests, the second package contains the pulse library and generates the analog test vectors, the third package configures and runs the tests. The sources of input data can be two-fold: analog or digital. The analog test patterns are used mainly to test the FADCs, BCID algorithms, and histogramming built into the PPrASIC. The digital patterns - pre-loaded in PPrASIC playback memory - serve to test the digital part of the MCM.The readout and real-time data captured in the memories are compared to each other and to the precalculated expectations. Tests of certain functional MCM blocks with both analog and digital input, allows to determine with high precision any malfunctioning blocks.

During production tests the software can be used in two main testing modes: PPrASIC Wafer test or MCM test. In the Wafer test mode only PPrASIC functional blocks are tested. In addition, the software controls wafer-probe station manipulations, namely stepping from die to die. The single Wafer test takes 1 minute per die; testing a whole wafer in one go needs 5 hours. In the MCM test mode all dice on one MCM are successively tested. This takes 2.5 minutes per MCM.

The test software was written in the C++ language using Qt libraries. A graphical user interface provides a test menu-guide for the user.

V. MCM LARGE SCALE PRODUCTION

The MCM large scale production consists of two major stages: component dice production and assembly of the MCM. At the first stage all components produced have to be tested before being placed on the MCM substrate. This allows elimination of the faulty dice at the first production stage. At the second stage, the complete MCM-assembly is done in several steps with intermediate testing of the MCM functionality. This strategy allows to detect faulty components and assembly failures at early stages of the production, thereby improving the initial production yield.

A. PPrASIC wafer tests

Among the chips on the MCM, the Pre-Processor ASIC is the major component as it performs the ATLAS-specific digital data processing for four trigger towers. The PPrASIC is a custom-designed chip, designed at KIP and fabricated by AMS (Austria Micro Systems). The physical properties of the PPrASIC are briefly summarized as follows:

- The size of a the PPrASIC is 8.370 * 8.375 mm^2.
- The design is realized as a "CUA 0.6 μm" process.
- Each PPrASIC contains logic and memories covering four signal-channels (950 000 transistors equivalent).
- The number of PPrASICs per wafer 192.
- The total Memory per PPrASIC is 8.125 KByte.

Each PPrASIC die is subject to a full functional test before placement on the MCM substrate. The PPrASIC wafers were tested in the KIP "clean-room" using test-hardware and the wafer-probe station to facilitate stepping from die to die(see Figure 5).

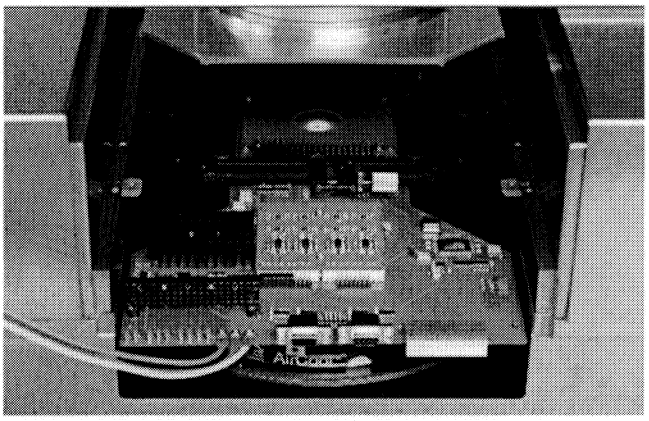

Figure 5: The PPrASIC test-hardware mounted in the wafer-probe station.

The test set-up for the wafer test is similar to the set-up described in Section IV, with some modifications on the MCM side. For the wafer tests the MCM Test board carries a "Needle Card" connected via adapter to an MCM-substrate with missing PPrASIC. The "Needle Card" has the pins to contact all the pads on the PPrASIC die on the wafer. For each wafer undergoing the test procedure, a wafer map is generated(see Figure 6). It contains the test results for each single die using an 8-bit color code. Those dice that passed the test are marked as "Known Good Dice" (KGD) . Later at a company, wafers are cut to individual dice, from which all identified KGD are selected and available for further use.

53 wafers with 10176 PPrASIC dice were produced and tested. Out of this number 4306 dice were found to be KGDs, giving a yield of 42%.

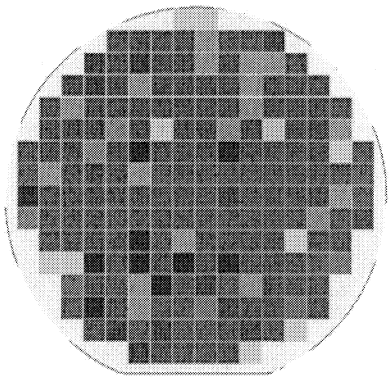

Figure 6: Wafer-maps showing test-results using an 8-bit color-code

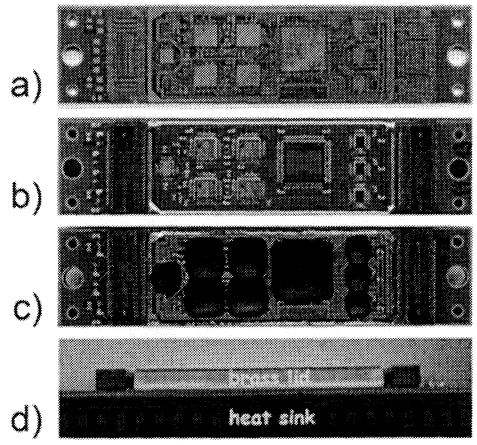

Figure 7: MCM assembly steps: a) MCM substrate; b) MCM with all dice bonded on substrate; c) MCM with glob-topped dice; d) MCM with brass and heat sink (side view).

B. Production Cycle

As the MCM was fully designed and developed at KIP, the first few modules were produced at KIP. Such in-house MCM production helped to understand the production problems and to develop strategies for the large scale MCM production.

The rest of the MCM production was done by industry. The MCM substrates were produced by WÜRTH Elektronik, while mounting of dice and SMD components, wire-bonding, and encapsulation was done by Hasec[9]. Figure 7 shows the MCM assembly at different production steps. Those were:

- production of 4-layer FR4 substrate backed by a 0.8mm copper plate by WÜRTH,
- **electrical test of the routing-tracks,**
- **bonding test by HASEC,**
- passive components soldering applying SMT technology,
- chip mounting,
- ultrasonic wire-bonding,
- **MCM Quality Assurance tests at KIP ,**
- application of glob-top over the 9 active chips,
- encapsulation of MCM hermetic brass lid; gluing of a heat sink for dissipated heat exchange,
- **MCM Quality Assurance tests at KIP.**

C. Production Results

At the time of writing the MCM production is fully accomplished. The number of functioning MCMs is 3012; the number of MCMs, which were found faulty during the production is 776. All test results as well as supplementary information for each single MCM are stored in the database, which is accessible via WWW.

After further investigations all faulty MCMs for which non-working chips could be determined, undergo a repair cycle at the mounting company. Different kinds of failures (short-circuits, faulty chips, bond faults etc.) make the investigation process rather complicated. In cases where the software alone is not sufficient to find the problem, a complex analysis using a microscope, an infrared camera and an oscilloscope is used.

VI. Conclusion

More than 3000 fully functioning MCMs are produced and ready to be installed in the ATLAS Level-1 Calorimeter Trigger. Thorough tests during the large scale production of the MCMs show an overall MCM yield of 80%. The experience gained from the large scale production of the MCM is reported including the optimization of the test procedures, observed problems and corresponding solutions.

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5 years Radiation Testing of electronic components and systems for the LHC experiments and the LHC machine : summary and future

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Abstract

A summary on the last 5 years radiation testing of equipment for the LHC project in dedicated facilities outside CERN is presented. The proton irradiation facilities in CRC Louvain la Neuve and in the Paul Scherrer Institute have given an important contribution to the design of the LHC equipment. The intensive testing efforts from CERN groups in the last 5 years underline that radiation tolerance has become a design and operational constraint for the LHC. Radiation testing will most likely continue during the LHC commission phase when radiation induced equipment failures will start to appear.

I. INTRODUCTION

Already some 10 years before the startup of the LHC, the requirement for radiation tolerant electronics for the LHC experiments was given a very high priority [1]. At that moment, it had become clear that the radiation tolerant designs and radiation hard components would be needed for the inner detectors where the expected dose rates are of the order of a Mrad per year at nominal beam intensity. Commercial off the shelf components and systems were suggested for use on the cavern walls where the expected dose rates are of the order of 100 Rad/year.

In 1998, a proposal to study radiation tolerant electronics was made by the LHC Electronics Board, stressing the importance that all the LHC experiments consider this problem. Initial studies focussed on the tolerance to damage from the total ionising dose but it was soon realised that single event errors were of much bigger concern since they were not taken into account in earlier design phases of the equipment. A specific simulation study [2] revealed that testing with protons at energy of 60-200 MeV is sufficient to compute the Single Event Error rate in a radiation environment such as that of the LHC. Protons also ionise and give displacement which means that all radiation effects could be tested simultaneously with a single radiation source.

The irradiation facilities at the UCL Louvain la Neuve in Belgium and the Paul Scherrer Institute (PSI) in Villingen (Switzerland) provided protons in this energy range and a specific collaboration agreement aimed at components testing for the LHC between CERN and these Institutes was initiated in the year 2000. These facilities have now been used by the LHC experiments for nearly 6 years, representing more than 600 hours of beam time. In 2005, the neutron irradiation facility at the Svedberg Laboratory began contributing to the LHC project by making available their neutron and proton irradiation facilities. Some 54 hours of beam time have been used by LHC groups at TSL to date.

The importance of radiation tolerant electronics for the LHC accelerator was recognised in 1999 when it was decided that the baseline of the machine was to locate equipment under the main magnets in the 27 km long accelerator tunnel. Initial radiation studies focussed mainly on the total dose tolerance but Single Events were soon recognised as a major issue. In 2001, the first machine equipment was irradiated in the proton facilities mentioned here above under the same agreement. Up to date, nearly 350 hours of beam time have been used by the machine equipment groups.

Although organised in entire different ways, the joined irradiation campaigns for machine and detector equipment groups proved very beneficial and efficient for all parties involved. This success underlines the importance of sharing experience and exchanging information on the radiation tolerance of electronic components and systems between CERN users and the radiation effects community at large. For the last 5 years, results on tested components have been presented at the LHC Radiation day [3], a yearly CERN event that takes place in December. In this paper we will summarise on the user experience from the last 5 years and predict the future needs for these facilities in particular in view of a luminosity upgrade of the LHC.

II. RADIATION TEST FACILITIES

A. Proton Irradiation facilities

The main proton irradiation facilities used by CERN are located at the Paul Scherrer Institute in Villingen (Switzerland) and the Catholic University UCL in Louvain la Neuve (Belgium). Both institutes are also involved in other ways in the LHC project and consider the use of their proton irradiation facilities as part of their contribution to CERN and to the LHC project in particular.

At PSI, there are 2 proton irradiation facilities (PIF, [4]). The low energy line (figure 1) provides protons at energies between 6 and 63 MeV at a maximum flux of 1 x 10^9 protons cm^{-2} s^{-1}. The maximum beam size in this facility has a diameter of 90 mm, 90% of the beam being distributed uniformly in an inner circle of 50 mm.

Due to its regular monthly availability with short notice, the low energy line at PSI has proven most popular for CERN users and more than 95% of the CERN irradiation experiments at PSI were conducted here. This represents approximately 370 hours of beam time over the last 5 years.

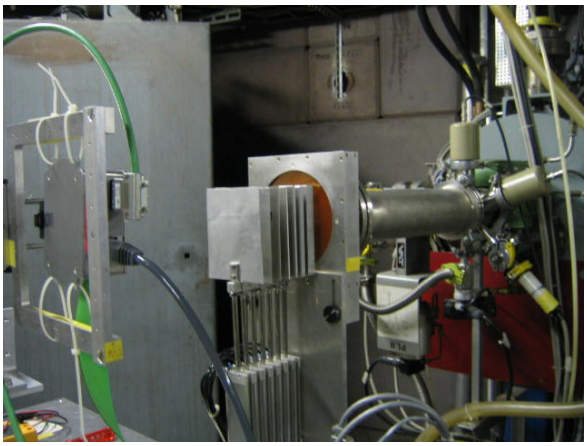

Figure 1: Irradiation of equipment for the LHC in the low energy Proton Irradiation Facility at the PSI.

The high energy line at PSI provides protons with energies between 35 and 250 MeV at a maximum flux of 2.5 x 10^8 protons cm^{-2} s^{-1} (neutron background 10^{-4} per proton per cm^2). The beam profiles in this line are Gaussian shaped and have a FWHM of 6 cm. The maximum beam diameter is about 90 mm.

The high energy beam line has been used occasionally by CERN groups for specific studies on, for example, power electronics for which concerns existed on destructive SEEs at high proton energies. Another example application was to complete a full single event upset cross section curve for proton energies ranging from 10 to 250 MeV.

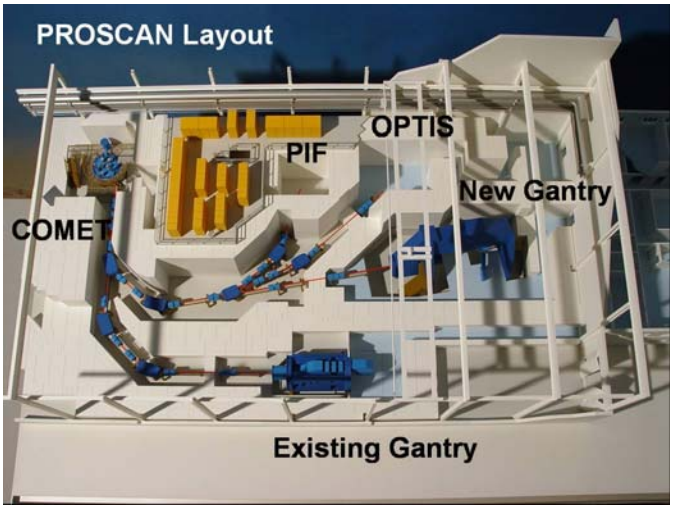

Figure 2: The new PROSCAN Proton Irradiation Facility at PSI for protons with energies between 10 and 250 MeV.

The low and high energy proton facilities at PSI will soon merge into a single facility (the PROSCAN Project, see figure 2) providing a wide range of energies from 5 to 255 MeV. In May 2005 the new COMET cyclotron, designed specifically for medical applications, was installed and commissioned. This superconductive 250 MV facility is also used to generate protons for the irradiation of electronic components and systems. The temporary test area where the PIF facility is installed is operational since January 2006 and the first CERN user group will conduct experiments for the LHC project in this facility in the fall of 2006. The final PIF experimental area will be commissioned in the first half of 2007.



Figure 3: The LIF proton irradiation facility at UCL at LLN

The LIF (Light Ion Facility) at the Cyclotron Research Centre (CRC) of UCL in Louvain la Neuve [5] (figure 3) provides proton beams with energies from 10 to 67 MeV at a maximum flux of 1 x 10^9 protons cm^{-2} s^{-1}. The beam profiles in this line are flat with a beam size of about 10 cm in diameter and less then 10% intensity variation over the irradiated surface. From the year 2000 onwards, some 18 irradiations campaigns for the LHC project took place at the LIF in UCL representing more than 500 hours of beam time.



Figure 4: Proton Irradiation of large objects at TSL in Uppsala.

In 2005, because of the need for high energy proton and neutron irradiations of relatively large complete systems, contacts were established with the Svedberg Laboratory (TSL) in Uppsala (Sweden). TSL can provide proton beams over a circular area 27 cm in diameter, which allows for the irradiation of complete systems in a single run (see Figure 4). Proton energy ranges is 20-180 MeV at a maximum flux of 1.4 x 10^8 protons cm^{-2} s^{-1} for a beam area of 27 mm in diameter [6]. The neutron irradiation facility at TSL provides neutrons with energies up to 180 MeV at a maximum flux of 6 x 10^5 neutrons cm^{-2} s^{-1}. The beam size for neutrons can equally have diameter of 27 mm although not at the maximum neutron intensity. The neutron irradiation facility has been used occasionally by CERN equipment groups for specific

studies and is considered complementary to proton irradiation experiments.

Table I summarises on the total number of irradiation campaigns and beam time in the various facilities since the year 2000.

Table 1: Cumulative number of CERN campaigns and beam hours used for the LHC project since the year 2000

Irradiation Facility	Irradiation Campaigns	Total Beam time in hours
PIF (PSI)	15	382
LIF (CRC/UCL)	18	539
TSL (Uppsala)	4	54

B. Irradiation facilities for cumulative effects

A significant amount of equipment for the LHC project has been tested for total dose effects in the gamma irradiation facilities from CIS-bio International in the nuclear research centre of CEA-Saclay in Paris [7]. Presently, two irradiators are available (named 'POSEIDON' and 'PAGURE') one of which is routinely used for industrial purposes.

The PAGURE irradiator has a ^{60}Co source of 14 kCi and provides dose rates from 3 kRad/hr to 100 kRad/hr for large volume and up to 2 MRad/hr for small volumes. In the latter case, the equipment must fit in a cylinder 5 cm in diameter and 5 cm height. This irradiator is frequently used for the irradiation of electronic components and material testing.

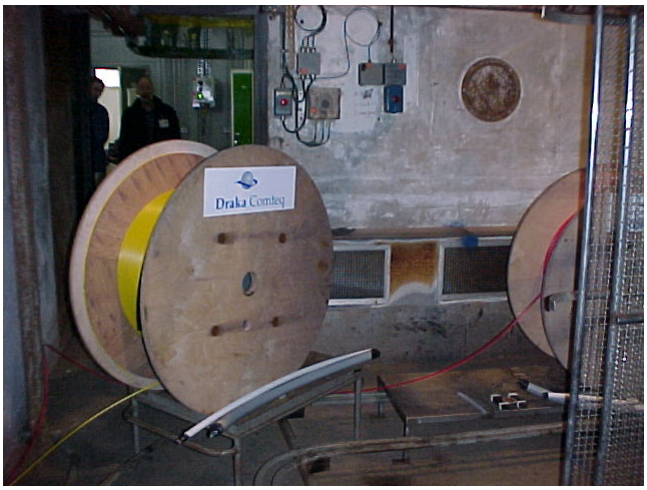

Figure 5: Gamma Irradiation of Optical Fibres for the LHC in the POSEIDON irradiator.

The POSEIDON irradiator (figure 5) also has an intense ^{60}Co source but can accommodate much larger volumes. The available dose rate in this irradiator varies between 3 kRad/hr and 500 kRad/hr. POSEIDON is used frequently used for industrial applications but long continuous irradiation periods can be obtained during the weekends.

A number of displacement damage irradiation tests for the LHC project have been carried out with the PROSPERO nuclear rector (figure 6) located at the military research facility of CEA-Valduc close to Dijon in France [8]. PROSPERO is composed of a ^{235}U core surrounded by a ^{238}Ureflector and a thick steel hood which reduces the gamma dose. It produces a degraded fission spectrum and is operated in a delayed critical state with a continuous power from 3 mW to 3 kW. The average energy of the neutrons is 0.8 MeV.

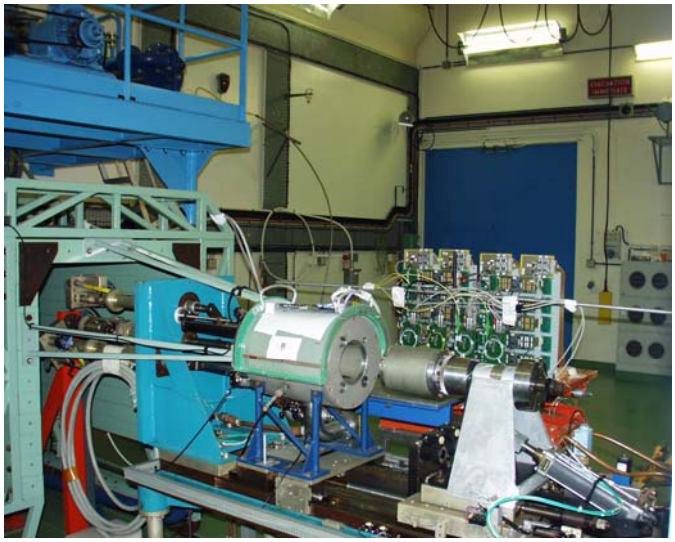

Figure 6: Neutron irradiation of LHC equipment with the PROSPERO fission reactor

This reactor operates in steady state mode and at 3 kW, the maximum fluence is 10^{14} 1 MeV equivalent neutrons per cm^2 for equipment that is placed close to the reactor core during approximately 3000 seconds. The maximum neutron flux is 3.6 x 10^{10} neutrons cm^{-2} s^{-1} and the associated dose rate from gammas in that case is 3.5 Rad/s. Other fluence to dose ratios can be obtained by increasing the distance with respect to the reactor. At 4 m for example, the neutron fluence is reduced by a factor 1000.

Alternatively, the neutron flux can be reduced by operating the reactor at lower power (minimum power 3 mW) while the neutron spectrum can be modified by placing the samples in shielding boxes made of polyethylene, Cadmium, or Boraflex

Table 2 gives a summary of the number of campaigns that have been carried in either of the facilities mentioned above since the year 2000 as well as the total number of different equipment groups involved.

Table 2: Cumulative number of CERN irradiation campaigns for Displacement and Total Dose since the year 2000

Irradiation Facility	Irradiation Campaigns	Equipment groups involved
PROSPERO (Dijon)	5	11
CIS Bio (Saclay)	6	12

In order to make the campaign more efficient, the radiation campaigns usually involve various CERN users groups from both experiments and the machine. Most campaigns take about 2-3 days to complete (including the set up of the experiments and post irradiation measurements). CERN is presently using these facilities on a regular basis and 1-2 times per year.

III. User Experience

A. *Single Event Error tests*

Proton beam irradiation has been by far the most important tool used by CERN equipment groups to evaluate SEE sensitivity of components and systems. The main reasons are probably that proton beams can be used to study single events, total dose and displacement damage in a single test and that the results allows for a straightforward extrapolation of the SEE rate in the LHC environment. As compared to irradiation with heavy ions or neutrons, proton test have relatively low costs and are easy to obtain. Proton irradiations are carried in air instead of vacuum which reduces the complexity of the test set up and shortens the overall time needed to characterise a device. Stopping, starting or adjusting the intensity of the beam is straightforward. Finally, proton beams are sufficiently penetrating to allow irradiation of electronic components in their packaging.

The aim of most user groups has been to obtain a reasonable estimate of the single event error rate of their devices and/or entire system during nominal operation at the LHC. SEE tests were therefore performed at the highest available proton energy (typically 60 MeV as recommended in simulation studies [2]) to compute the error cross section by dividing the total number of errors observed in an irradiation run by the total proton fluence during the run. By assuming that all hadrons above 20 MeV have the same cross section, it is then possible to compute the error rate in the (simulated) radiation environment of the LHC [2]. Although not very accurate, this procedure proved easy to follow for non experts in the field and a good trade-off between the time constraints imposed by the LHC construction schedule and the limited resources available.

Based on our experience over the last few years, a successful SEE test is usually the result of a very careful preparation. Each user group responsible for an electronic system or sub-system for the LHC is also responsible for the radiation test. Users therefore need to acquire at least a minimum knowledge on the subject of radiation effects. The irradiation schedule and beam parameters have to be prepared in advance, preferably with the help of knowledgeable person in the field. The test set up should be completed 1-2 weeks in advance and the devices under test should be available and tested with the SEE test set up. On line visualisation of the test data is highly recommended as it allows for a first check of the data after each run. The number of accesses to the irradiation area and the exposure of the users to ionising radiation can be minimised if the setup has the possibly to reset and power cycle the devices under test remotely. Furthermore, a good mechanical and electrical interfacing between the test facility and the SEE test setup is needed to avoid problems related to, for example, EM interference, stray light or polarity inversion.

Some user groups use the same SEE test set up in consecutive experiments. The setup is then modified and improved over time. This has the advantage that slightly activated cables, connectors or mechanical support structures can be temporarily stored at the radiation facility and re-used at a later point in time.

Single Event Errors have been a concern during many radiation tests for the LHC project to date. In some cases, SEEs occurred in components or systems where they could be expected. In other cases, SEEs occurred while the experimenters were mainly interested in studying the TID tolerance of the equipment. . For custom made in-house designs a few proton irradiation sessions of 8 hours each could be sufficient to make the system design sufficient radiation tolerant and to proceed to series production. . If the constraint of radiation tolerance was added to an existing design (COTS or custom build equipment from Industry) the lead time was in general much longer.

B. *Cumulative damage tests*

Grouped cumulative damage test for the LHC project are carried out once to two times per year. Usually, equipment groups from the accelerator and the experiments decide on a joined expedition to optimise resources and to reduce the amount of equipment that needs to be transported. The campaigns are supervised and prepared by a knowledgeable person from CERN but each user group remains responsible for its own test.

Again, the key point for a successful test has proved to be a very careful preparation together with a setup that interfaces correctly with the facility and that has been tested extensively before departure. Irradiation conditions and user requests have to be combined several weeks beforehand into a feasible irradiation plan.

Neutron irradiations with the PROPERO fission reactor are performed in a single run and a campaign usually takes 3 days to complete. The setting up and testing of the equipment in the reactor hall can take an entire day and represents an important part of the work as there is no possibility to interrupt the test. All exposed material becomes very radioactive after the irradiation and access to the reactor hall is prohibited for several days. Post irradiation measurements are therefore carried out at the facility itself on the final day of the campaign.

Total Dose irradiations experiments with gamma rays from a ^{60}Co source provide more flexibility because they can be interrupted for short periods of time. As material does not become radioactive, it is possible to adjust the test setup or exchange the devices under test.

It is often difficult to estimate the degradation of the components or systems at a given dose rate before the test. Many users therefore begin their experiments at a low dose rate for a short period of time. After a first evaluation of the equipment at a predefined dose, the dose rate can then be increased by decreasing the distance between the equipment and the source.

Although this approach gives the user a first impression, it makes the study of dose rate effects and annealing behaviour more complicated or even impossible.

IV. Future prospects

Figure 7 shows the evolution of the proton beam time usage by the LHC experiments over the last few years. The high luminosity experiments CMS and ATLAS have been the

main users of the proton facilities probably because they incorporate a large amount of equipment in their detectors and because they have the most severe radiation environment. Testing for the smaller, low luminosity experiments ALICE and LHCb started at a later point in time and required less beam time.

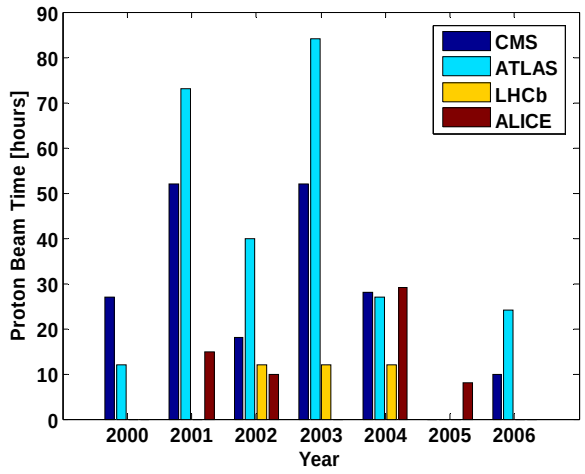

Figure 7: Proton beam time used by the LHC experiments.

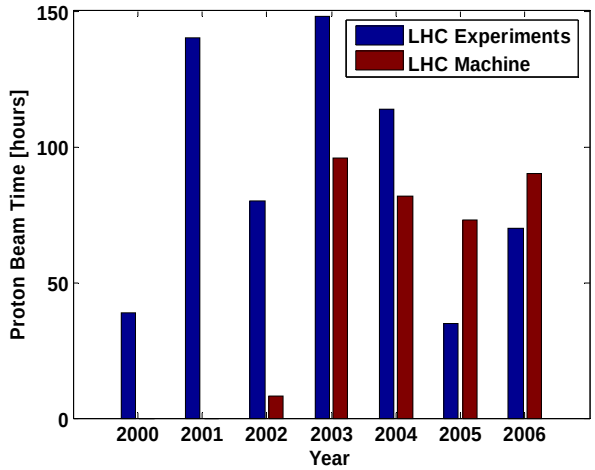

Figure 8: Total proton beam time used for the LHC experiments and the LHC machine.

In 2003, the requests for beam time surged as many groups needed to validate their systems before starting series production of the equipment (figure 7). In the 2 years following the series production and in some cases already installation, the need for beam time decreased.

In 2006, the observed increase of requests from the LHC experiments originates from equipment that was developed late with respect to the LHC schedule, namely the power supplies for the distribution of the low voltage to the experiments. Early prototypes having being designed without radiation tolerance in mind, and due to the complexity of the equipment, several testing cycles were necessary to eventually converge to an architecture and components that could satisfy the radiation tolerance specifications.

The observed increase of requests from the LHC machine in the same period originates mainly from the Beam Loss Monitoring (BLM) system and the RADMON radiation monitoring system. Both systems needed detailed calibration runs for the various sensors or chambers.

This tendency makes us believe that radiation tolerance assurance studies for the machine will probably continue at approximately the intensity in the years to come. In 2007, the request for beam time should decrease as the equipment installation and commissioning activities will be in full swing.

The LHC commissioning run at low beam intensity and low energy (450 GeV) is presently foreseen in December 2007. This event will make the issue of radiation damage to equipment and in particular the issue of SEE rates more specific. Areas with a potential risk of radiation damage to equipment when operating at higher beam intensities will emerge. Furthermore, despite all efforts to assurance the radiation tolerance of LHC equipment, first radiation induced equipment failures will probably appear.

The request from the LHC experiments in the near future will be mainly driven by the LHC upgrade programmes. A small fraction may come from groups that operate equipment in the experimental areas as radiation damage in the experimental areas is only expected when the first beams with physics intensity are put into collision in 2008. At his point, the issue of radiation shielding of the experiments will have become more precise.

V. Acknowledgements

Proton irradiation tests have been of crucial importance for the design and the construction of electronic components and systems for the LHC machine and experiments. We would like to acknowledge the contributions from the Cyclotron Research Centre of the “Université Catholique de Louvain la Neuve” (UCL), the Paul Scherrer Institute and The Svedberg Laboratory. In particular the help, from G. Berger (CRC), W. Hajdas and R. Brun (PSI) and A. Prokofiev (TSL), their extremely good will, their knowledge of their facilities were not only appreciated, but absolutely essential in the setting up of the agreements with their Laboratories, and in the success of every irradiation campaign.CEA-DAM and Cis-Bio International are thanked for their contributions with special thanks to N. Authier and his collaborators.

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The LHC Beam Loss Monitoring System's Surface Building Installation.

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Abstract

The strategy for machine protection and quench prevention of the Large Hadron Collider (LHC) at the European Organisation for Nuclear Research (CERN) is mainly based on the Beam Loss Monitoring (BLM) system.

At each turn, there will be several thousands of data to record and process in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary.

The BLM system can be sub-divided geographically to the tunnel and the surface building installations. In this paper the surface installation is explored, focusing not only to the parts used for the processing of the BLM data and the generation of the beam abort triggers, but also to the interconnections made with various other systems in order to provide the needed functionality.

I. Introduction

The strategy for machine protection and quench prevention of the Large Hadron Collider (LHC) at the European Organisation for Nuclear Research (CERN) is presently based on the Beam Loss Monitoring (BLM) system. At each turn, there will be several thousands of data to record and process in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary.

The BLM system can be easily sub-divided geographically to the tunnel and the surface building installations. The tunnel installation consists of around 4000 detectors, placed at various locations around the ring, tunnel electronics, which are responsible for acquiring, digitising, and transmitting the data. More details can be found in [1]. In the surface installation, electronics receive the data via 2km redundant optical data links, process, analyze, store, and issue warning and abort triggers. The later provide also the connections to the Beam Interlock, the Beam Energy Tracking, the Collimation, the Logging and the Post Mortem systems (see Figure 2). In this paper, the surface building's electronics are explored providing details for the different parts combined to provide the needed functionality.

II. BLM Surface Electronics

The installation at the surface foresees VME crates spread over all of the eight LHC interaction points accommodating the processing modules, a timing card, a CPU card and a Combiner card (see Figure 1). The data acquired at the tunnel installation arrive digitized over redundant gigabit optical links.

A. VME Crate

For the BLM system, 25 VME crates will be used in total, three at each point except LHC's point 7 that will have an extra crate facilitating mainly the detectors observing the Collimation system.

All of them are making use of the extended VME64 [2] specification. This extension defines a set of features that can be added to VME and VME64 boards, backplanes and sub-racks. Some of the features included are a 160-pin connector, a P0 connector, and geographical addressing.

In order to make the best out of those features, CERN's Beam Instrumentation group has defined a custom-made backplane for the P0 connector [3]. Some of the features it provides include connections to create two daisy-chain links for the processing modules, general purpose I/Os, and additional supply voltage outputs.

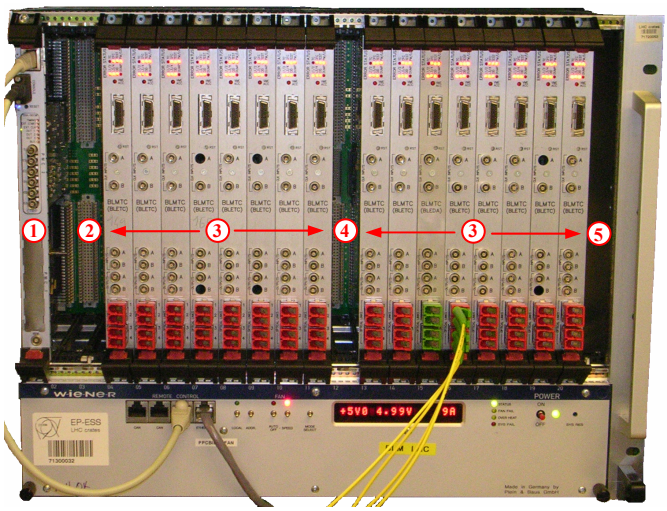

Figure 1: VME Crate's arrangement for the BLM system:
1. Crate's CPU, 2. Timing card (CTRV), 3. Processing modules (BLETC), 4. Timing card (BOBR), 5. Combiner card (BLECOM).

The VME crate, in the arrangement for the BLM system, can host, except the one CPU and two types of timing cards, 16 processing modules and one signal concentrator card (see Figure 1). Finally, its fan tray allows remote monitoring and control.

B. Processing Module (BLETC)

A VME card, named DAB64x [4] that provides the processing power, and a mezzanine card, named BLM Mezzanine [5] card that links the tunnel with this surface installation, comprise the BLETC processing module (see Figure 3). Its main task is to analyse the acquisition data, by

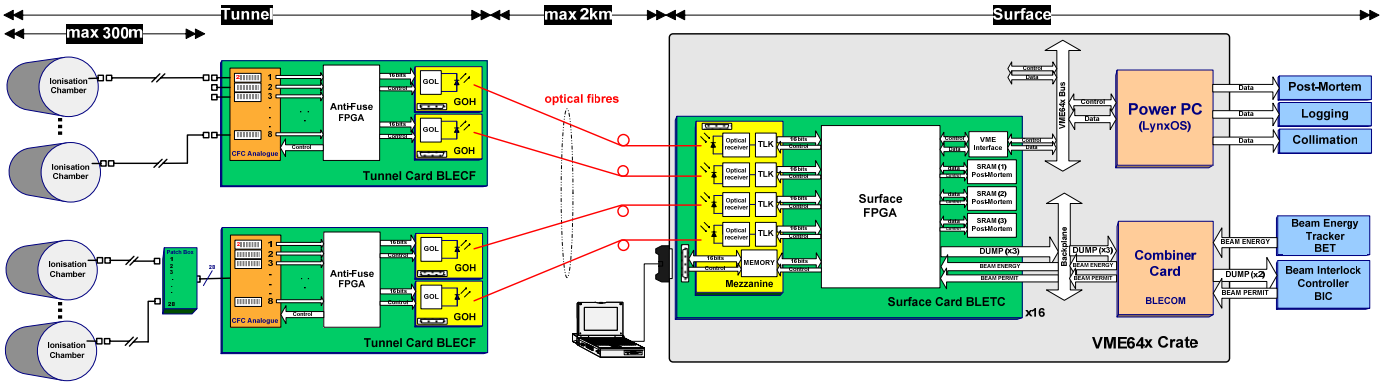

Figure 2: Overview of the LHC Beam Loss Monitoring System (including connections to other dependant systems).

keeping a history of those data and calculating various moving sum windows for each detector. It will decide whether a dump request should be initiated, by comparing those histories with predefined unique threshold values for each detector.

The BLM mezzanine card is hosting the receiver parts for four optical links. It handles the de-serialisation and decoding of the four optical gigabit data transmission lines in parallel and provides the received data to a reconfigurable field programmable gate array (FPGA) device [6], the backbone of the DAB64x card.

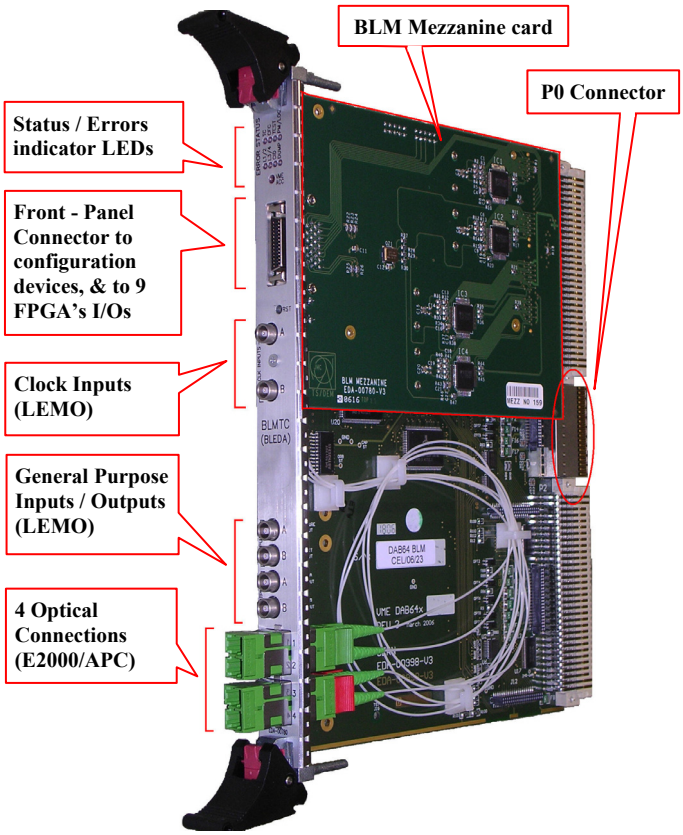

Figure 3: Processing module (BLETC)

Each module has been configured to process in real-time up to 16 detector channels. It will establish communication with the VME-bus and will be accessible through it, but at the same time, the module will be able to work autonomously for protection against main CPU failures.

The availability of all detectors, the acquisitions chain and the generation and communication of the beam abort signal needs to be verified for each channel before each injection into the LHC. The processing module checks first that the communication links are in an acceptable state and then that the statuses of the tunnel electronics (i.e. power supplies, high voltage supplies, acquisition state, etc) are also working.

C. *Timing Cards*

The timing card available on each crate is the BOBR [7] module. It is also a VME format card, designed to interface a VME crate with up to two different Timing, Trigger and Control (TTC) networks and has been developed by the Beam Instrumentation group. In this application it will provide the Time-Stamp and the Post Mortem triggers. Additionally, one of the Controls Timing Receiver (CTR) cards will be installed on each rack to provide to its VME crates the beam energy data distributed by the Safe LHC Parameters (SLP) system [8]. The initial recipient of the CTR's data is the adjustment Combiner card and from there they are re-distributed to the rest of the Combiner cards of the rack.

D. *Crate CPU*

The CPU is a PowerPC with LynxOS as operating system. Its main purpose is to access periodically the processed data from each processing module, to normalise them with their corresponding threshold values and to provide them for the Logging system before they are displayed on the fixed displays in the control room. Moreover, it will collect and time-stamp the Post Mortem and the Collimation data, stored on the circular buffers, whenever the relevant triggers arrive.

Data will be sent over the VME-bus for on-line viewing and storage by the Logging and Post-Mortem systems. The BLM system will drive an online event display and write extensive online logging (at a rate of 1 Hz) and post-mortem data (the acquired data from the last 20,000 turns plus averages of the same data of up to the last 40 minutes) to a database for offline analysis.

At the same time, the CPU will calculate and issue the Warning triggers before transmitting them to the Logging system. The Warning level will correspond to a fraction of the

Threshold value at that moment, provisionally decided to be 30%. The BLETC module will provide to the CPU the calculated Running Sums together with their corresponding threshold values through the Logging process to simplify this process.

E. Combiner card

The final receiver of the two beam permit lines, one for the Maskable and another for the Un-Maskable channels, is the Combiner card, located at the last slot of the crate. The two beam permit lines are daisy chained through each of the processing modules using a custom-made backplane in the crates. If any of the modules decides to break any of these lines a beam dump request will be given to the LHC Beam Interlock System (BIS) [9]. As an additional use, those lines will be used by the Combiner card to provide a continuous supervision of the operation of the cards in the crate. Thus, it will be able to discover immediately a disconnection from the circuit or a module failure and a dump will be requested for any of those cases.

The Combiner card is also responsible of distributing the beam energy to each of the processing modules in the crates, as well as, initiating all the test procedures and checking the results when there is not a circulating beam in the accelerator.

III. Data Processing Overview

The real-time processing of the acquired data is assigned to the FPGA accommodated in the processing module. Figure 4 illustrates an overview of the main processes involved.

The "Receive, Check and Compare" (RCC) process will receive, de-serialise and decode the transmitted packets. It will check for errors on both transmissions (primary and redundant) and compare the packets in order to select one error-free packet. Its additional tasks will be to check the status of the tunnel installation by checking the status information received at each packet. It will collect and report the errors seen. Actually, it will provide a significant part of the Status and Error Logging information by collecting the errors seen from the various checks that will be used by the expert applications to track potential problems.

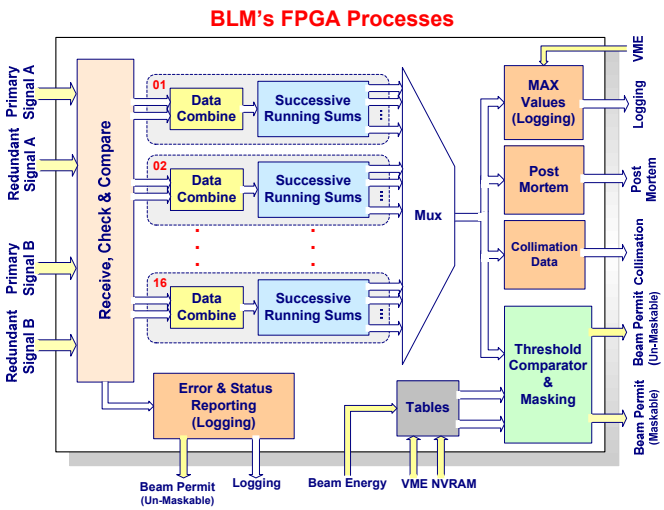

Figure 4: Overview of the Processes in the BLM's FPGA.

The "Data-Combine" process will receive from the packet the two types of data, the counter and the ADC data, coming from each detector and will make use of a merging algorithm to combine them into one value. At the same time, it will make an effort to filter noise passing through the ADC circuitry and normalise the output depending on its working range.

The combined values from each detector will be given, each time they become available, to the "Successive Running Sums" (SRS) process. This process produces and maintains a number of histories, in the form of moving sum windows, for each detector. More specifically, the procedure for the data processing, which was chosen to be followed, is based on the idea that a constantly updated moving window can be kept by adding to a register the incoming newest value and subtracting its oldest value. The number of values that are kept under the window, or differently, the difference in time between the newest and the oldest value used, defines the integration time it represents. Additionally the specific implementation (i.e. the SRS) is making use of the cascading of multiple moving windows to create longer integration periods in order to minimise the resources utilisation. The SRS will calculate and maintain continuously 12 running sums for each detector that span from 40 μs to 84 s. Table 1 shows the complete range covered by the SRS in the configuration for the LHC.

Table 1: Successive Running Sums Configuration.

The red coloured RSs (running sums) outputs, i.e. RS1, RS4, RS6, and RS7, represent their additional utilisation as inputs for the adjacent SRs (shift registers), i.e. SR2, SR3, SR4, and SR5.

Range		Refreshing		Shift Reg. Name	Signal Name
40 μs steps	ms	40 μs steps	ms		
1	0.04	1	0.04		RS0
2	0.08	1	0.04		RS1
8	0.32	1	0.04	SR1	RS2
16	0.64	1	0.04		RS3
64	2.56	2	0.08	SR2	RS4
256	10.24	2	0.08		RS5
2048	81.92	64	2.56	SR3	RS6
16384	655.36	64	2.56		RS7
32768	1310.72	2048	81.92	SR4	RS8
131072	5242.88	2048	81.92		RS9
524288	20971.52	32768	655.36	SR5	RS10
2097152	83886.08	32768	655.36		RS11

In the subsequent stage, those calculated sums are compared with their corresponding threshold limits in the "Threshold Comparator" (TC) process every time they become updated. If one or more of them are found to be higher, a dump request is signalled.

All dump requests are gathered initially by the "Masking" process, which serves the purpose of distinguishing between "Maskable", "Un-Maskable" and unused channels.

The information necessary for the operation of the TC and the Masking processes, that is, the threshold and the masking values, are stored in tables uniquely created for each card. The threshold values that will be provided to the TC process will depend on the beam energy, whose range (450 GeV to 7 TeV) was decided to be divided in 32 steps. Thus, on each processing module a unique table of 6,144 threshold values (or 32KB) and two 16 bit masking registers will be held on each card.

For supervision and logging purposes, two more processes have been added. The "Maximum Values" process, which calculates and keeps the maximum values 'seen' in a period of time by each moving sum window, and the "Error & Status Reporting" (ESR) process, which reports the errors found in the transmissions and the status of the tunnel electronics. The data accumulated by both of them are collected by the crate PowerPC and projected in the Control Room's displays.

Finally, for the correct alignment and setup of the collimators one more set of data is available. Those data, destined for the Collimation system, contain whenever requested the last 20.48 ms of acquired data in the form of 32 x 640 μs sums for each detector.

IV. Reliability and Availability Enhancement

The system has been designed with reliability and availability in mind. The BLM system must guarantee its correct operation and its fail-safety for the system to have a much higher probability of preventing superconductive magnet destruction caused by a beam loss. For those reasons, the processing modules can operate independently of CPU and Timing card failures. There is redundancy in the optical transmission with additional powerful error detection and the connection to the Beam Interlock System (BIS) is tripled.

More specifically, to ensure a reliable communication link, a double, that is, a redundant optical link has been utilised as a first measure. The error free reception of the packet will be ensured using the CRC-32 error check algorithm [10] and augmented by the 8b/10b encoding scheme [11]. By including those digital techniques, a more sophisticated receiver part was produced that is expected to achieve even higher data reliability and system availability. More specific, the CRC is able to discover any error with a length less than the length of CRC and for longer bursts (i.e. 32 bit) the probability of undetected error is small enough (non-detection probability $Pr = 1.16415*10^{-10}$). The 32-bit checksum of the CRC will be additionally used for comparison of the redundant packets. The 8b/10b encoding will provide not only the clock data recovery (CDR) and a DC-balanced serial stream, but also additional error detection capability.

The unique Threshold and Masking tables for each of the monitors can thoroughly be prepared and checked before they are uploaded. They can be quickly and easily upgraded for specific systems when the levels need to be changed and additionally be used as a calibration and offset tool. Their small size allows them to be kept internally by the FPGA device in its available embedded memory blocks, which will decrease the access time and increase the implementation simplicity, if compared to an external memory device.

Extra information embedded in the packet will allow continuous self-checking of the system from problems resulting from user errors or aging. For example, to avoid misplacement of the Threshold or Masking table, the Card ID transmitted on each packet will be used. Each tunnel card holds a unique 16-bit number that will be compared with the one loaded together with the tables.

Similarly, to avoid loss of data, the Frame ID, a 16-bit number that will increment at every transmission, will be also included on each transmitted packet. The Surface FPGA will be able in that way to compare consecutive transmissions and check for missing frames.

Finally, to ensure the correct recognition of system failures and dump requests the surface card's outputs, carrying the beam dump information, will use a frequency signal. At a dump request, reset, failure, or even card disconnection the transmitted frequency will be inevitably altered, thus, always triggering the beam abort.

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