SIC-JFET SWITCHING POWER SUPPLY TOWARD FOR INDUCTION RING ACCELERATORS *

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Abstract

Utilizing a high power discrete SiC-JFET developed by KEK, a switching power supply (SPS) that had a circuit topology of H-bridge was designed and constructed to drive the induction acceleration system for the KEK digital accelerator. The SPS was installed in the actual KEK Digital Accelerator system. Consequently, heavy ion beam acceleration was successfully demonstrated. Moreover, we have started to develop a next generation package for a high voltage SiC-JFET, which has the voltage rating of 2.4 kV. Two in one module construction, bonding wire free connection, and bidirectional thermal flowing are included in the design concept of the new package.

INTRODUCTION

A novel synchrotron called an induction synchrotron (IS) was developed at High Energy Accelerator Research Organization (KEK) in 2006 [1]. In the IS, charged particles are accelerated by pulse voltages generated through 1:1 or 1:2 transformers driven by switching modulators employing high power high repetition rate semiconductor switches. The switches are turned on and off by gate signals which are digitally manipulated from the bunch signal of a circulating ion beam. Consequently, the acceleration is always synchronized with the revolution of ion beam irrespective of the mass and charge state of ion. Thus, an IS is free from the limitation of bandwidth, unlike in RF cavities or amplifiers. Hence this feature allows us to accelerate ions from an extremely low velocity region to the light velocity region. Acceleration of heavy ions, such as gold or uranium, is possible. The IS utilizing no high-energy injector is called a digital accelerator (DA), which is under beam commissioning at KEK at present [2][3].

A switching pulse supply (SPS) that generates bipolar pulses is one of the key technologies for the DA. In the existing DA, the SPS is composed of 7 series connected Si-MOSFET per one arm of a H-bridge because of the limitation of a thermal capacity and a withstand voltage of the device. However, series connection of the device has substantially induced a large complexity in handling gate trigger pulses and hence decreased the system reliability.

To solve these problems, the next generation of SPS utilizing SiC devices is under development. In consequence, a high-power discrete SiC-JFET package was developed, with which successful operation of 1kV-27 A-1 MHz was confirmed [4]. Following the successful results of the device evaluation, we designed and constructed a SPS that had a circuit topology of H-bridge[5]. In this paper, experimental results of the heavy ion acceleration test with prototype SPS and the design concepts of the next generation high voltage and high power SiC-JFET package are described.

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THE SPS

Circuit

The SPS has a configuration of H-bridge. Figure 1 shows a schematic diagram of the SPS. The H-bridge has 4 switching arms, each of which is composed of a SiC-JFET that is mounted on a water-cooled heat sink and a gate drive circuit connected to an insulated dc power supply and is triggered by a light signal. The device performance of the SiC-JFET is summarised in Table 1. Also each arm has a snubber circuit, which has a role of absorbing a discharge energy stored in the parasitic circuit inductances and is composed of a capacitor Cs, a diode Ds, and a Resistance Rs.

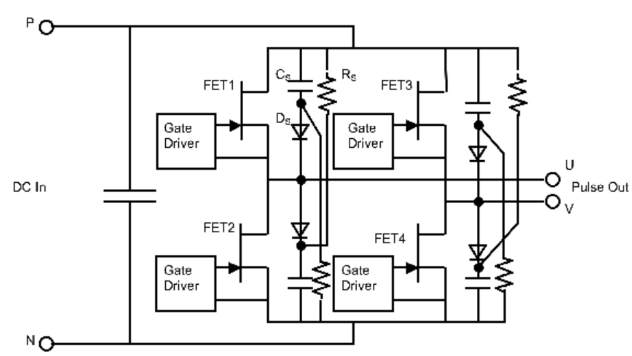

Figure 1: Schematic diagram of the SPS.

Table 1: Device Performances

Parameter	Value	Unit
Blocking voltage	1200	V
Pinch-off voltage	-17	V
On resistance (@150℃)	0.2	Ω
Thermal resistance, junction to case	0.56	K/W
Power dissipation	>250	W

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BEAM ACCELERATION EXPERIMENT

KEK DA

Figure 2 shows the outline of the KEK DA, , which consists of an x-band electron cyclotron resonance ion source (ECRIS) embedded in a 200 kV high-voltage platform, a low energy beam transport line (LEBT), an electric injection kicker (ES-Kicker) induction acceleration cells, extraction kicker/septum magnets, and a high-energy beam transport line (HEBT).

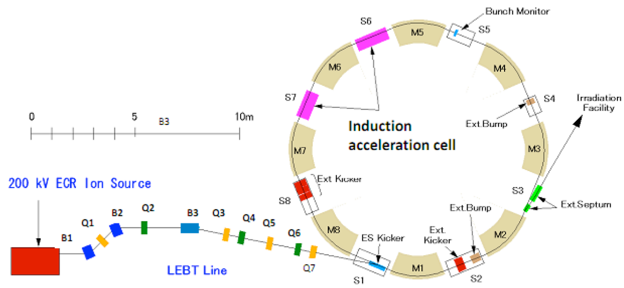

Figure 2: Outline of the KEK-DA.

Parameters of the Beam Experiment

Figure 2 shows the outline of the KEK DA, , which consists of an x-band electron cyclotron resonance ion source (ECRIS) embedded in a 200 kV high-voltage platform, a low energy beam transport line (LEBT), an electric injection kicker (ES-Kicker) induction acceleration cells, extraction kicker/septum magnets, and a high-energy beam transport line (HEBT).

Dominant parameters of the ion-beam acceleration experiment are summarized in Table 2.

Table 2: Parameter List of the Acceleration Experiment

Ring circumference C	37.7 [m]
Bending radius ρ	3.3 [m]
Maximum/Minimum B Field	0.23/0.039 [T]
Frequency of B Field	10 [Hz]
Mass／Charge Ratio	4
Acceleration Voltage V_{AC}	747 V
Orbital period (Injection →Extraction)	12 us → 2.1 us
Extraction Energy	6.9 MeV

In a synchrotron, acceleration Voltage is explained as Eq. 1.

$$V_{AC} = C * \rho * \frac{dB}{dt} . \qquad (1)$$

Substituting the parameters shown in Tabale1, Eq. 1 can be rewritten as Eq. 2

$$V_{AC} = 747 \sin(20\pi t) . \qquad (2)$$

KEK-DA utilizes a pulse density modulation scheme to obtain a sinusoidal acceleration voltage with the SPS. A FPGA (Field Programmable Gate Array) generates pulse timing signals to control the SPS (Fig. 3).

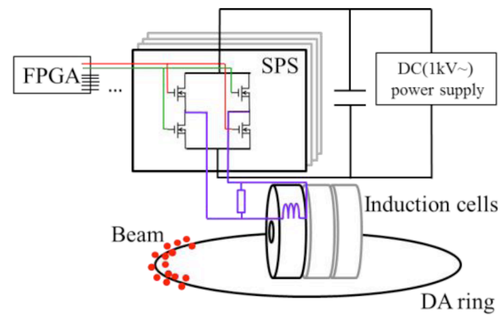

Figure 3: KEK-DA Pulse Timing System.

Experimental Result

Figure 4 shows the bunch signal and the input voltage of the acceleration cell generated by the SPS during the timing of (a) just after beam injection, (b) 20 ms after injection, (c) 35ms after injection. Equivalent acceleration voltage in each period is 58 V, 730V, and 624 V, respectively. Figure 5 shows the projection of the acceleration voltage and bunch profile signal on the time-turn plane. Stable acceleration synchronized to the acceleration voltage is confirmed from this figure.

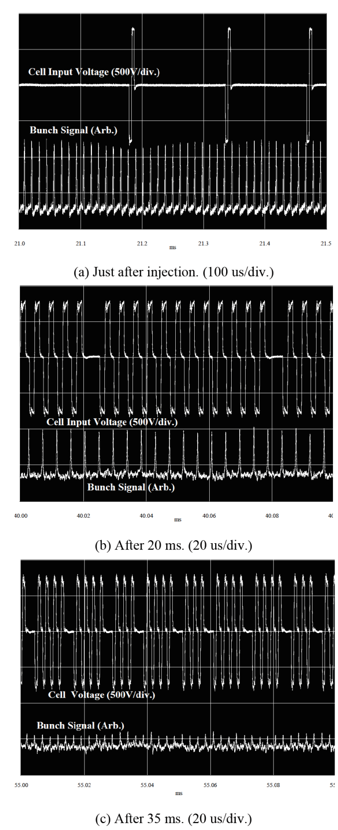

Figure 4: Bunch signal and input voltage of the cell.

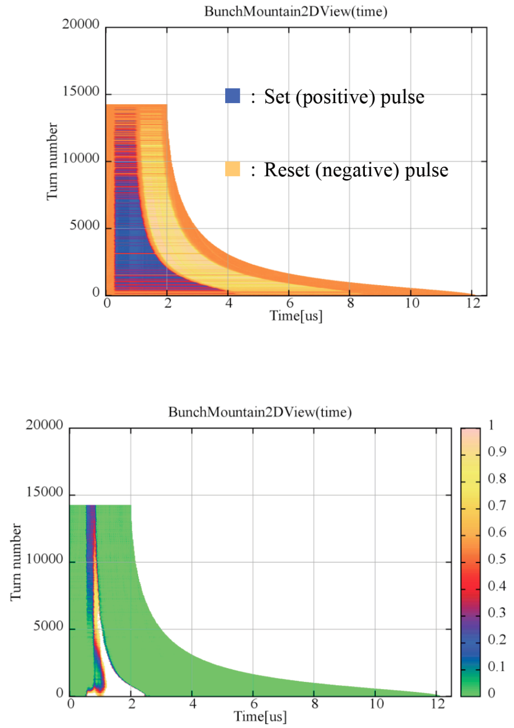

Figure 5: 2D Mountain view of the acceleration voltage (upper) and the beam bunch signal (lower).

DEVELOPMENT OF HIGH VOLTAGE NEW DEVICE PACKAGE

Performance Objectives

Development of 2nd generation package that has higher voltage rating has been started. Development targets are listed in Table 2 as compared to 1st generation package.

Table 3: Comparison of 1st and 2nd Generation Package.

	1st Generation	2nd Generation
Connection	Discrete	2 in 1
Die Size	4.16 mm sq.	2.4 mm sq.
Device Manufacturer	SiCED	SiCED
Withstand Voltage	1200 V	2400 V
Heat Extraction	235 W	> 1000 W
Parasitic Inductance	23 nH	< 10 nH

Package Design

To attain the performances objectives, the new package is designed utilizing a bidirectional thermal flow concept shown in Fig. 6. Shows, where 4 FETs connected 2 in parallel and 2 in series are included; .

Heat Extraction Test utilizing a Mock-up Package

With dummy FETs, a mock-up package was fabricated, and was provided for heat extraction test. Experimental results are shown in Fig. 7. Beyond 600 W, high power heat extraction has been confirmed.

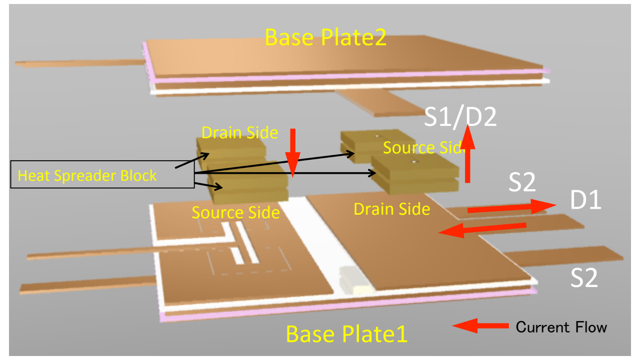

Figure 6: Conceptual view of new package.

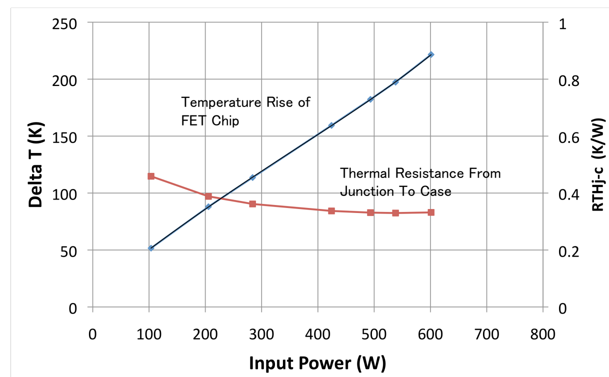

Figure 7: Temperature rise characteristics.

SUMMARY

Utilizing the SiC-JFET based SPS, successful acceleration of heavy ion beam was confirmed. Moreover, development of next generation high power SiC-JFET package is proceeding.

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