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DESIGN A PRECISE STABILITY CONTROLLER FOR HIGH POWER PULSE MODULATOR BASED ON FPGA*

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Abstract

Shanghai Soft X-ray Free Electron Laser Test Facility (SXFEL-TF) has been fulfilled the construction assignments and passed the acceptance check at Shanghai Institute of Applied Physics (SINAP), Chinese Academy of Sciences. The stability of microwave system is one of the major factors to get better beam performance. It is mainly determined by klystron and modulators power supply. The beam voltage stability of pulse modulator, which is the cathode voltage source of the microwave amplifier, is directly affecting the microwave amplitude and phase. The requirement of the microwave stability is 0.04% (rms) for amplitude and 0.05% (rms) for phase tolerance. This paper shows the design considerations of stability improvement and suitable upgrade scheme of the controller for Shanghai SXFEL pulse modulator.

INTRODUCTION

SXFEL-TF is an X-ray Free Electron Laser (XFEL) facility, which has been accomplished at shanghai institute of Applied Physics (SINAP), Chinese Academy of Sciences. This facility is located close to Shanghai Synchrotron Radiation Facility (SSRF) which is the first 3rd generation light source in China. [1] SXFEL-TF consists of a 130 MeV photocathode injector, a main LINAC enhancing the beam energy to 840 MeV, an undulator system with two stages of HGHG-HGHG or EEHG-HGHG scheme and a diagnostic beamline. In the main Linear Accelerator (LINAC) C -band accelerator structure was first used at SINAP. Main parameters of C-band microwave system were listed in Table 1. In order to achieve High-gradient and compact, six C-band microwave acceleration units were used, which can achieve a high acceleration gradient of 40 MV/m [2-3].

Table 1: Parameters of C-band Microwave System

Parameters	Value
Microwave Frequency (MHz)	5712
Repetition Rate (Hz)	10 Hz
Peak Power (MW)	50 MW
Microwave Pulse Width (μ s)	2.5
Amplitude Stability (ppm)	400
Phase Tolerance (deg.)	0.18

Microwave system is mainly consist of klystron and modulator, which requests very stable amplitude stability and very tight tolerances of phase jitter. The performance of microwave system is one of the major factors to get great beam performance. It is mainly determined by a low level microwave driving system and klystron modulators. The beam voltage of the modulator, which is the pulsed power source of the microwave amplifier klystron, directly affects the microwave amplitude and phase.

Beijing Electron Positron Collider is studying a de-Qing circuit aiming at improving the stability of less than 0.15% [4]. De-Qing circuit is a conventional method of regulating the PFN charging voltage. The LINAC Coherent Light Source (LCLS) at Stanford Linear Accelerator Centre (SLAC) improves the pulse-to-pulse stability of the modulator by using solid state modulator [5]. The stability of the existing SSRF LINAC modulator which is used a capacitor-charging power supply (CCPS) charging the Pulse Forming Network (PFN), has achieved 0.05% [6-7]. It doesn't meet the requirements for SXFEL. This paper shows the suitable upgrade scheme of pulse modulators and the stability improvement design considerations of pulse modulators for Shanghai SXFEL. Traditional controller of pulse modulator is mostly based on Programmable Logic Controller (PLC). We add a new circuit based on Field Programmable Gate Array (FPGA) to regular the PFN charging voltage. The relevant stability experiment indicates that pulse to pulse stability of the modulator can meet the requirement of SXFEL.

UPGRADE SCHEME OF CONTROLLER

In order to upgrade pulse to pulse stability of pulse modulator, an upgrade control system was developed. The schematic diagram of stability controller is shown as Fig. 1. We present a real time feedback control system of LINAC pulse modulator to improve PFN charging voltage. The feedback control system is based on embedded FPGA techniques. It consists of an embedded NIOS II processor, a High resolution Analog to Digital Convertor (ADC) and an upper computer. The NIOS II processor manage on chip memory, ADC connector, direct memory access (DMA) function, interrupt request (IRQ) function, and ethernet communication.

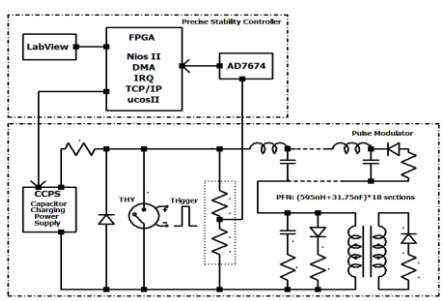

Figure 1: Schematic diagram of stability controller.

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High Resolution ADC Choice

For analog to digital converter, speed and resolution are two contradictory parameters. If we want to achieve high stability control, high resolution ADC is the premise. Due to the existence of noise, effective numbers of resolution bit is smaller than ideal numbers of resolution bit. The relationship between effective numbers of bit (ENOB) and signal-to-noise ratio can be calculated by equation (1).

$$\mathrm{ENOB} = \frac{N-1.76}{6.02} \quad (1)$$

Where N is the ideal resolution bit of ADC. We chose AD7674 model produced by ADI Company. From the data sheet, signal-to-noise ratio is 97dB, so we can calculate the effective numbers of resolution bit by the above equation is 16 bit. Figure 2 shows the picture of AD7674 evaluation board.

PFN charging voltage is acquired by data acquisition system based on AD7674, AD7674 transmit data to FPGA, which embedded with NIOS II processor, in real time. FPGA makes signal and information processing then give a inhibit signal to stop CCPS charging.

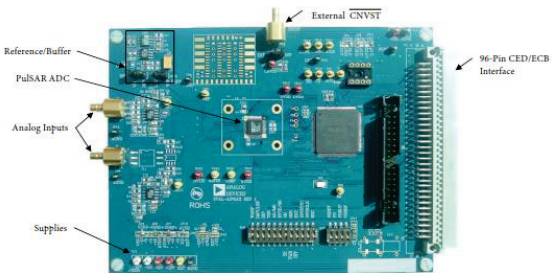

Figure 2: Picture of AD7674 evaluation board.

FPGA Hardware Design

Figure 3 shows the FPGA hardware design block diagram.

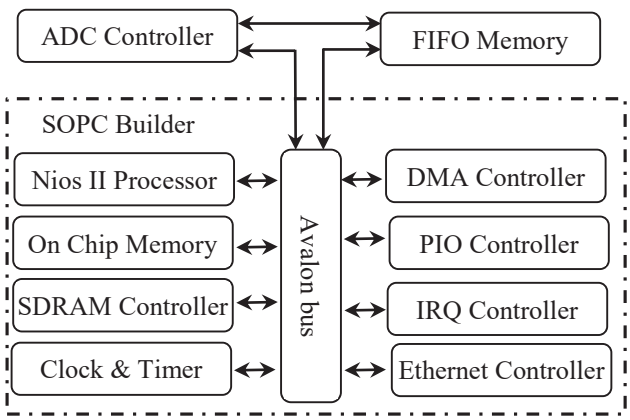

Figure 3: Systematic composition of FPGA hardware.

In order to achieve high speed trigger acquisition, we use soft trigger method. ADC works at continuous conversion mode, IGBT switching on signal is used as trigger for reading conversion result. We set two conversion period delay-time and then calculate average value of five acquisition data after each trigger signal. If the sample data reach the setting value, FPGA generates a inhibit signal to CCPS to stop charging PFN in real time. Meanwhile the sample data is stored in on-chip FIFO memory and then transmitted to the upper computer.

Nios II is a soft processor, implemented in a series of Altera's FPGA devices, which can be defined by hardware description language such as Verilog and VHDL. The most advantage of soft processor is its flexibility. System can be defined by a variety of standard peripherals as well as customize peripherals which can be configured by users to meet the demands of a specific system.

PIO is used for transmitting interrupt signals. While the inhibit signal is generated, the ADC controller issues an interrupt, which causes our interrupt handler to run. The interrupt function implement transmit sample data from FIFO to system SDRAM through DMA operation. After generating the inhibit signal, pulse modulator is waiting for thyratron switch on trigger and then start the next pulse period.

FPGA Software Design

In order to transmit the required acquiring data to upper computer, we apply TCP/IP communication protocol. Software manage the TCP/IP networking task as well as data acquisition and processing task by using MicroC/OS II which is an easy-operation real-time system.

In MicroC/OS II system, we set up two tasks, one is called Socket-Server-Task and the other is Socket-Send-Task. The first task is used to configure TCP/IP protocol and the second task is used to send data to the upper computer by using the TCP/IP protocol configured by the first task. The second task has higher priority than the first one. Socket-Send-Task is configured to be waiting for an effective signal which enables by interrupt request function. PFN charging value after each IGBT switch on period is firstly stored in on-chip FIFO memory. When PFN charging voltage reaches the set value, ADC controller generates a inhibit signal and gives NIOS II processor an interrupt signal to starts Socket-Send-Task.

It's important to illustration that MicroC/OS II operating system will bring in uncertain delay time. So MicroC/OS II operating system is only used to transmit required data to upper computer. All of the data acquisition circuit, data processing circuit and control logic circuit are generated by strict hardware description language.

TEST RESULT

The precise stability controller was tested both in laboratory and with pulse modulator. Laboratory experiment was used to verify the function and performance. And then, we use this controller to regulate the CCPS charging period with pulse modulator.

Experimental Verification of High Resolution

The resolution of ADC has been certificated by using the histogram method. We use three 1.5V dry cell batteries in series as analog input, the images of histogram is shown in Fig. 4. Form the figure we can see the resolution of the data acquisition system can achieve 40ppm. Figure

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5 shows digital conversion results of 4.5V and 4.5001V. 0.1mV is just 20ppm of the full range of analog input. Experimental results show that the data acquisition system has the advantages of high resolution. It is very easy to distinguish out very slight change of CCPS charging voltage.

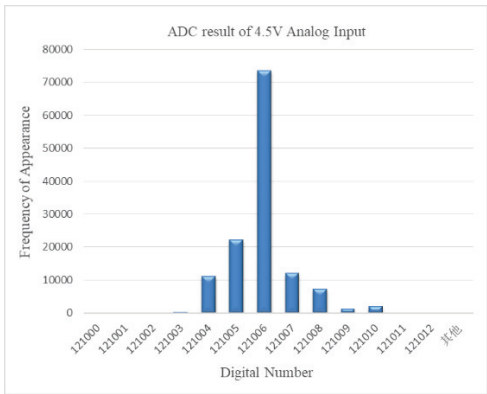

Figure 4: The histogram of 4.5 V analog input.

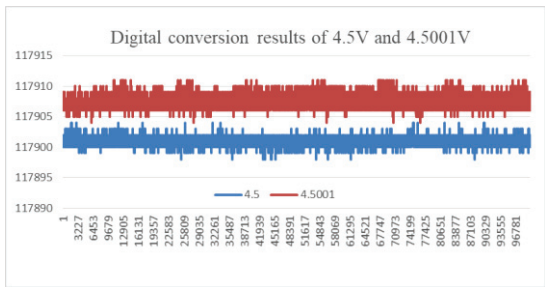

Figure 5: The digital conversion results of 4.5V and 4.5001V.

Experimental Verification of Stability Improvement

Figure 6 shows the picture of stability control experiment. Figure 7 shows the PFN charging value after using this precise stability controller for about 4500 pulse periods. Calculated result of PFN charging voltage is 82ppm. Figure 8 shows the pulse voltage stability test result after applying this precise stability controller. The stability is measured by an oscilloscope and a dual channel differential amplifier which is used to improve the resolution of oscilloscope [8].The stability measuring result is 270ppm.

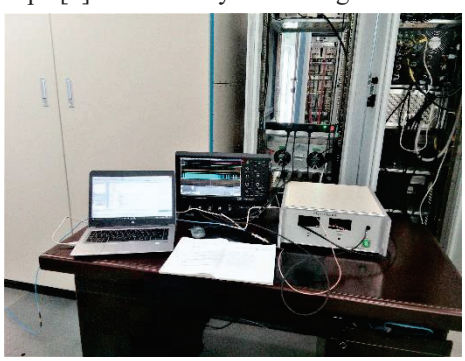

Figure 6: Picture of stability control experiment.

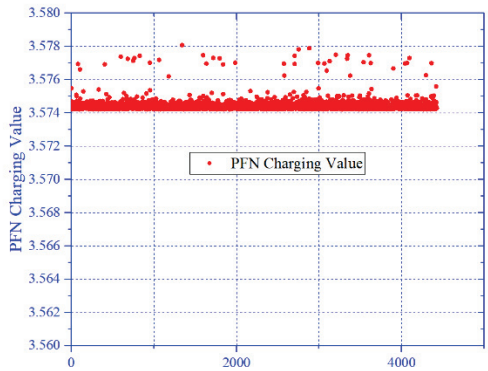

Figure 7: PFN charging value after using precise stability controller.

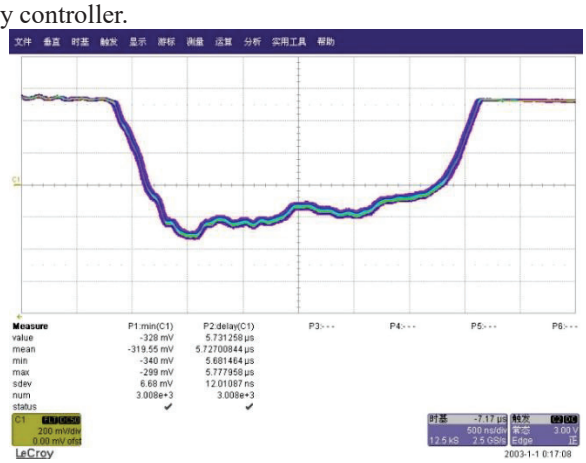

Figure 8: Pulse voltage stability test result.

CONCLUSION AND DISCUSSION

A precise stability controller based on FPGA was developed for pulse modulator. It aims to improve pulse to pulse stability by controlling the PFN charging voltage precisely. The relevant experiments show that the feedback control strategy reaches required function. It can improve the pulse to pulse stability from 500ppm to better than 300ppm.It is useful to improve the stability of existing modulator power supply. Stability of PFN charging voltage depends on CCPS. After determined the parameters of CCPS resonance loop, control mode is becoming very significant. The time response of the control system must be smaller than one IGBT switching cycle. A good control strategy needs a very precise high voltage probe. The high voltage probe must have the characteristics of low temperature coefficient and low ripple.

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