

Cryogenic Electronics Development for CUPID

R G Huang^{1,2}, Y Mei², Yu G Kolomensky^{1,2} and C Grace²

¹ University of California, Berkeley, CA 94720-7300, USA

² Lawrence Berkeley National Laboratory, CA 94720-8153, USA

E-mail: roger.huang@berkeley.edu

Abstract. CUPID (CUORE Upgrade with Particle ID) is a next-generation ton-scale bolometric experiment that will search for neutrinoless double beta decay. CUPID will have reduced backgrounds compared to CUORE through the ability to distinguish between $0\nu\beta\beta$ events and α backgrounds by detecting light emissions. To achieve this, it will deploy on the order of 3000 sensors in its detector array, which will introduce additional technical challenges compared to the 1000 sensors currently in CUORE. Using only room-temperature electronics for CUPID would increase the thermal load on the cryostat from the necessary cabling and increase the complexity of the vacuum system. A multiplexed readout with cryogenic electronics is a potentially appealing solution to these challenges. This work will present a characterization of CMOS devices that will guide future cryogenic ASIC design for CUPID readout.

1. Introduction

The Cryogenic Underground Observatory for Rare Events (CUORE) is an experiment currently searching for neutrinoless double beta decay ($0\nu\beta\beta$) through a cryogenic bolometric approach, cooling 988 750-gram TeO_2 crystals to an operating temperature of about 10 mK and detecting events through their heat deposits in the crystals. CUORE has already set the leading limit on the $0\nu\beta\beta$ half-life for ^{130}Te and plans to reach an operational lifetime of 5 years [1]. The future CUORE Upgrade with Particle ID (CUPID) plans to take advantage of the cryogenic infrastructure developed for CUORE, with the addition of light detectors near the crystals to complement the heat signals and allow active discrimination between α and β/γ events.

CUPID will provide an opportunity to upgrade the electronics infrastructure that was used for CUORE. CUORE uses NTD thermistors on its TeO_2 crystals to detect the temperature changes induced by physical energy deposits, but all the electronics for biasing the NTDs and amplifying and reading out their signals are operated at room temperature [2]. This method introduces additional electronic noise, and for CUPID this will require additional cabling for every channel that is being added. Cryogenic CMOS operated at temperatures of 4K have recently attracted interest in the quantum computing community as precision controllers and low noise amplifiers [3, 4]. Building on these developments, cryogenic CMOS-based ASICs operated at or below 4K offer an alternative approach to signal preamplification in CUPID. Performing preamplification in this manner at the cryogenic stage allows us to reduce electronic noise for CUPID and allows the possibility of introducing a modest multiplexing factor to help deal with the increased number of channels as well.



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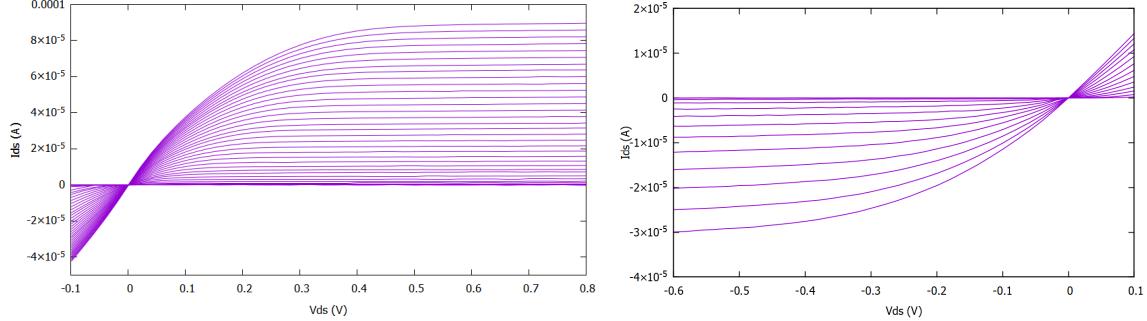


Figure 1. Left: V_d vs I_d scan for a $0.5 \times 0.5 \mu\text{m}$ NMOS at 100 mK, with V_g going from 0.2 to 1.1 V in 0.02 V steps. Right: V_d vs I_d scan for a $1.2 \times 1.2 \mu\text{m}$ PMOS at 100 mK, with V_g going from 0.2 to 0.8 V in 0.05 V steps.

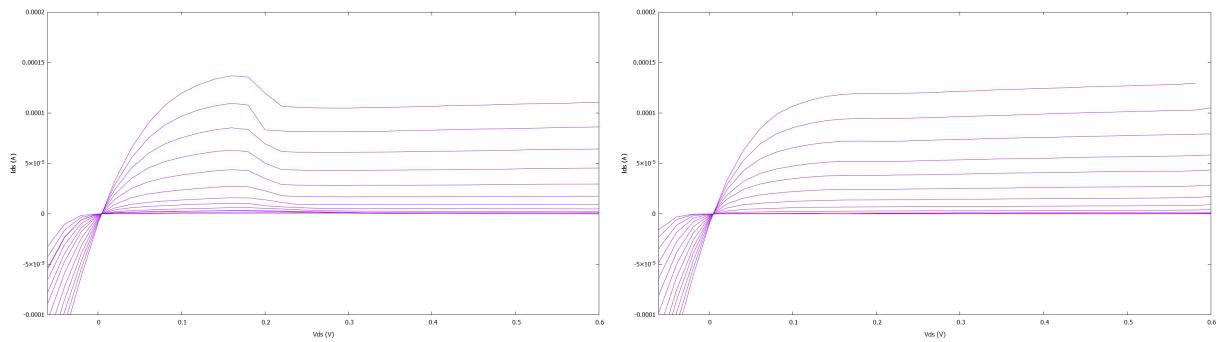


Figure 2. IV scans for a $10 \times 0.5 \mu\text{m}$ NMOS. Left: scanning by increasing V_d , in which a kink is visibly present. Right: scanning by decreasing V_d , in which the kink is no longer present.

2. Results

Due to the scarcity of existing measurements of CMOS behavior below 4K, we begin with characterization of our devices down to temperatures of around 100 mK. Characteristic IV curves for a couple of the MOSFETs are shown in Fig. 1, where we can see that they continue to remain operational down to these temperatures. We also observe a hysteresis effect in one of our NMOS at cryogenic temperatures, as shown in Fig. 2, where there's a visible kink when scanning from low to high V_d but not when scanning from high to low V_d . Investigation of the cause of this effect is ongoing, but similar kinks in the IV curve behavior that show up only at cryogenic temperatures have previously been observed in [3].

We are also able to extract information on how characteristic parameters change as the temperature of the devices decreases. We observe in Fig. 3 that the threshold voltage of the NMOS and PMOS increases as temperature decreases, as expected due to carrier freeze-out. The transconductance g_m for this device as a function of I_d at different temperatures is shown in Fig. 4, in which we see g_m and g_m / I_d rise as the temperature decreases, which will be beneficial for low-temperature amplifier design.

3. Conclusions

We have demonstrated successful operation and characterization of NMOS and PMOS transistors down to temperatures of less than 100 mK, the first step in showing their potential use in cryogenic-level signal amplifiers for readout of heat and light signals in a CUPID-style

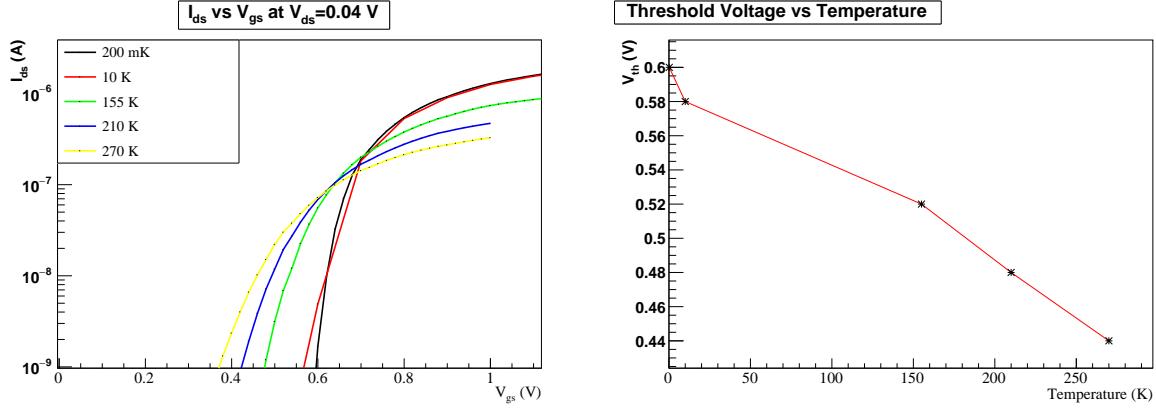


Figure 3. Left: I_d vs V_g for a $0.5 \times 10 \mu\text{m}$ NMOS at different temperatures. Right: the threshold voltages extracted from the leftside plot.

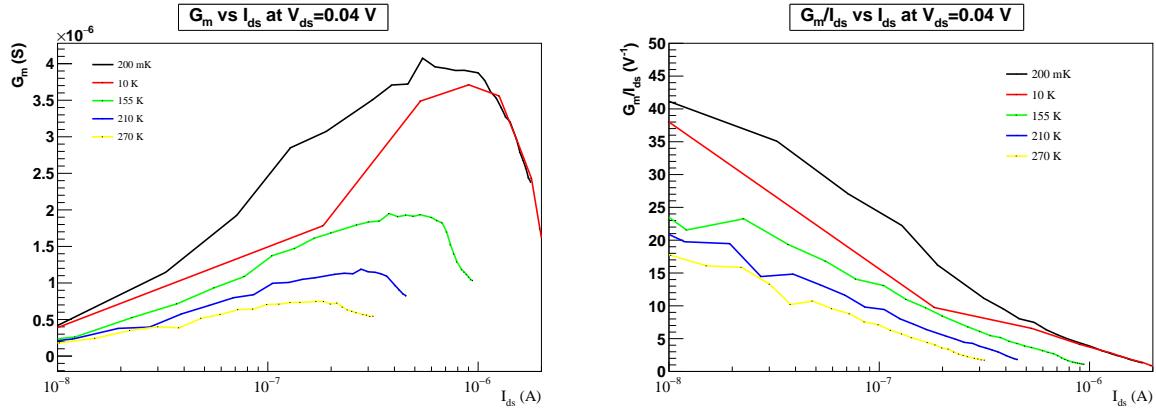


Figure 4. Left: measurements of the transconductance g_m vs I_d of a $0.5 \times 10 \mu\text{m}$ NMOS at different temperatures. Right: the same measurements, but shown as g_m / I_d vs I_d .

experiment. Future work will test the performance of cryogenic CMOS-based amplifiers, with the aim of being able to use them to read out thermal pulses from NTD or TES-instrumented bolometers and light detectors. The temperature stage at which the CMOS could be operated in the final CUPID design will depend on the gain, power dissipation, and reliability we are able to achieve in these tests.

References

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