ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-TUPMP002

OVERVIEW OF SIRIUS POWER SUPPLY SYSTEM

C. Rodrigues†, G. O. Brunheira, B. E. Limeira, R. J. Marcondeli, A. R. Silva, H. Sousa, G. M. Rogatto, A. P. A. Silva, G. R. Oliveira, M. G. Martins, A. R. D. Rodrigues, Brazilian Synchrotron Light Laboratory – LNLS, Campinas, Brazil

Abstract

Sirius is a 4th generation synchrotron light source designed and under construction by Brazilian Synchrotron Light Laboratory (LNLS), which first beam is scheduled to operate in 2019. Almost a thousand Power supplies (PS) will be needed to feed all magnets of the magnetic lattice, with outputs ranging from 10A to 1.1kA and 50W to 333kW. Almost all power supplies were designed at LNLS.

Only three families of power modules were designed: low power (FBP), high power (FAP) and AC (FAC). Each PS can have up to 8 modules in a parallel or/and series association, in order to reach the rated output values.

All PS are digitally controlled by the same hardware and firmware, also developed by LNLS, called Digital Regulation System (DRS), but with different parameter settings. The DRS is also responsible by the communication with other systems, PS monitoring, data management, etc.

This work presents an overview of this system, showing the PS specifications, family topologies and results of tests.

INTRODUCTION

Sirius is a 4th generation synchrotron light source which were designed and is been built by Brazilian Synchrotron Light Laboratory (LNLS) in Campinas, Brazil. LINAC and Booster (BOO) are already operating, and the storage ring (SR) must be ready in the second semester of 2019 [1].

More than 1500 magnets will be used in the magnetic lattice, and to feed them more than 1000 power supplies (PS) will be needed. This quantity includes the following PS that will not be presented in this work:

- LINAC PS, which were provided by SINAP, China, with all other LINAC equipment.
- Insertion Devices (IDs) PS, which will be defined together with them.
- Fast orbit correctors PS, that will be installed later.

One of the initial principles that oriented the design of Sirius' PS was to have few families to reduce the project effort, number of spare parts, number of part numbers adopted, etc. Thus, these PS were divided in only three families, Low Power (FBP, 4-Q), High Power (FAP, 1-Q), AC PS (FAC, 4-Q), as showed in Table 1.

Table 1: PS Distribution in Families

Fam.	Out. Ratings	SR	BOO	LTB	BTS	TOT.
FBP	10A/10V	650	51	21	10	732
FAP	750A/450V	35	-	1	9	45
FAC	1.1kA/800V	-	6	-	-	6

All PS described here were designed by the Power Electronics Group (ELP) of LNLS, which also built and tested the prototypes. A Brazilian company produced the pilot and final lot of FBP family. The power modules of FAP and FAC PS were assembled by other Brazilian companies and integrated by ELP.

DIGITAL REGULATION SYSTEM (DRS)

All PS families use the same hardware and firmware, called Digital Regulation System (DRS), to control the PS and communicates with the high-level system, local computer or IHM. But the DRS presents different configurations and parameter settings according to each application. It was developed by ELP and its initial operation with FBP model was described in [2]. Figure 1 shows the 2 DRS crates used with FAP PS and their boards, which are described below.

Universal Digital Controller

The Universal Digital Controller (UDC) is the heart of the DRS. It is based on the System on Chip (SoC) F28M36P63C2 from Texas Instruments®. It contains two processing cores: one is a microcontroller ARM Cortex-M3, which is responsible for communication interfaces, PS parametrization and low-speed/resolution analog measurements. The second core is a floating point DSP of C2000 family, running with a 150 MHz system clock, which is used to execute the control algorithm (up to 100 kHz) and signal processing, as well to drive the power circuit using its 16 HRPWM (high resolution pulse width modulator) channels.

The board also has 8 12-bit Analog-to-Digital Controller (ADC), 4 Digital Outputs (DI), 12 Digital Inputs (DO), Flash and SRAM memories. It also can have an IHM with touchscreen display, for local operation.

FBP family uses one UDC to control up to 4 PS. In the case of FAP and FAC families, each PS uses 1 to 5 UDCs to work.

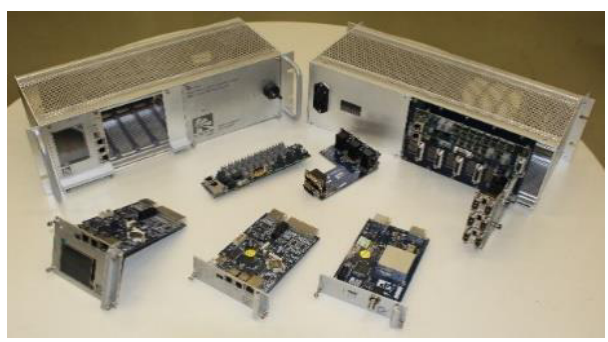

Figure 1: DRS and its boards.

† cleber.rodrigues@lnls.br

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-TUPMP002

High Resolution ADC

In order to have digital measurements with high resolution and speed, a dedicated board was developed, the High-Resolution ADC (HRADC). It uses a 18-bit SAR (Successive Approximation Register) ADC, AD7634 from Analog Devices®, with sample rates up to 600 kSPs.

The HRADC has two input modes, voltage (+/-10 V) or current (up to 1 A). The board also has a CPLD (Altera Max V) that can be used to perform self-calibration, compensate nonlinearities and filtering.

A single UDC can control and read up to 4 HRADC, with a Serial Peripheral Interface (SPI).

Other Parts

For FAP and FAC models, some other components are necessary to complete the DRS system.

DRS Crate Used to house the DRS boards, has a +/-15 V power supply to feed the circuits, on/off switch and a backplane that connects all boards.

Backplane Communication Board (BCB) This board is used to provide the following UDC interfaces to proper connectors:

- Transmitters for PWM plastic optical fibers (POF).
- POF transmitter and receiver for synchronization signal.
- Two DB9 connectors used in an internal CAN chain for communication with the power modules and I2C to communicate with a parametrization dongle.
- Two RJ45 connectors used for communication among UDCs.

Expansion Board (EXB) This board has 6 DB9 connectors to distribute analogic and digital inputs, and digital outputs, used in PS with multiple power modules.

LOW POWER PS (FBP)

FBP family is used to feed all steering magnets (SR: 280, BOO: 50, TL: 21), skew quadrupoles (SR:100, BOO: 1) and quadrupole trim coils (270), as well as the quadrupoles of low energy transfer line (10). All these magnets have a maximum current of 10 A, and the maximum voltage 8 V, already taking in account the cable drop.

This family is an evolution of one model of PS used in UVX [3], the first synchrotron source of LNLS. Figure 2 shows a FBP unit, which can have up to 4 non-insulated independent channels (or PS). Each FBP is composed by:

- Crate, which provides connections to loads, DC-link and AC mains, the backplane that connects all boards and an auxiliary +/-15V PS to feed them.
- Up to 4 power modules, one for each desired PS, which consist of a full-bridge converter with second order damped filter, as showed in Fig. 3 [2].
- One UDC which controls all channels.
- Up to 4 HRADC board, one for each channel.
- Up to 2 DCCT Board, one for each 2 channels, with medium precision DCCTs (ITN12-P from LEM), to make the feedback of the output current.

Figure 2: FBP PS, power module and DCCT board.

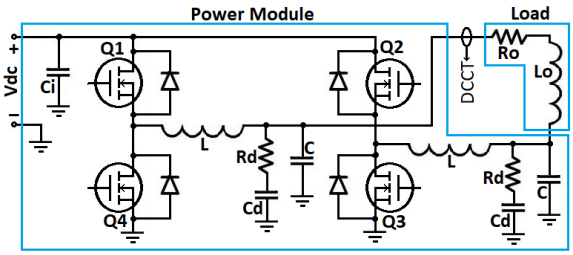

Figure 3: Simplified schematics of a FBP Power Module.

Unipolar switching is used to drive the switches, resulting in 100kHz output ripple with a 50kHz switching frequency.

The PS was designed and tested for 10 A / 10 V (100 W) rate per channel. This PS does not have internal fans and the cooling is performed only with the rack top ventilator. But in cases where there is a high PS density per rack fan trays can be used to improve air flux.

As dc-link it has been used model HWS1500-6 from TDK-Lambda®, which is shared with all crates of the rack. Despite of one unit is enough to feed the whole rack, two parallel units are used to have redundancy.

All FBP PS are already assembled, and Booster and TL PS are installed and being used for Booster commissioning. Now the SR steering magnets are being installed.

Tests after installation are in progress, but those performed in laboratory showed good results.

For the 40 units used in the TL, de RMS output current ripple, for a bandwidth of 10 Hz to 3 kHz, were between 8 to 25 ppm. The maximum value is higher than the specification (20 ppm), but they include the measurement noise.

The 12-h stability was better than 15 ppm, below the specified 100 ppm, and the warm-up time to reach this value was lower than 3 hours.

The bandwidth was adjusted to 3.5 kHz (specification: 100 Hz) and the efficiency of the power module was 89%.

HIGH POWER PS (FAP)

This family of PS is used to feed the magnets showed in Table 2, which also shows the PS quantities and their output rates. It was developed a power module with ratings (300 A, 230 V, 46 kW) that satisfies most of these needs. In the other two cases these modules can be combined in the following way:

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-TUPMP002

Table 2: FAP Maximum Output Values and Quantities

		PS Qt	Io [A]	Vo [V]	Mod/PS
SR	Dip	2	400	460	4
	Quad	12	160	60 to 230	1
	Sext	21	160	70 or 130	1
BTS	Dip	1	750	35	4
	Quad	8	150	10	1
LTB	Dip	1	300	20	1

- SR dipoles: 2 sets in parallel, each one with 2 modules in series association.
- BTS dipoles: 4 modules in parallel.

Figure 4 shows the simplified schematics of a FAP unit with a single module. The power module is based on a 2-phase interleaved buck converter [4] with coupled inductors [5]. This topology was chosen due to the reduction of inductor size and because the output ripple is twice de switching frequency (20 kHz). Moreover, since all these PS will operate with a constant output current, the DC-link can be adjusted to keep the duty cycle close to 50%, what almost eliminates the ripple due to switching in both input and output current of power module.

Hall sensors (internal to power modules) are used to balance the current in both arms. For BTS dipole PS they are also used to balance the current among modules. But for SR dipole PS the equilibrium between modules are made using medium precision DCCTs. Concerning to the main feedback, high precision DCCTs are used in all situations, LEM® ITZ2000 for all dipole PS and PM Measurements® TOPACC for the other ones.

The PWM signals are transmitted from DRS to drivers by POF. Inductor and IGBT heatsink are water cooled.

Off-the-shelf PS are used as DC-link. For transfer line PS, from which output voltage is lower than 35 V, it was used model HFE2500 from TDK-Lambda®. For all others, it was used model Topcon Quadro from Regatron®. Up to 3 units of Dc-link can be series associated to feed up to 4 power modules in parallel.

Transfer line FAP PS are already installed and those of LTB have been used without problems. Figure 5 shows a rack with 4 units of BTS quadrupole PS. SR dipole PS are being installed, and quadrupole and sextupole PS are being integrated.

Measurements with the real load still need be run, but it was obtained 98% of efficiency in laboratory.

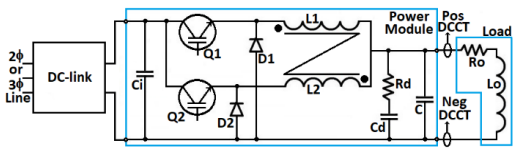

Figure 4: Simplified schematics of FAP model PS.

AC POWER SUPPLIES

Although this PS family has only 6 units (all used at Booster), as showed in Table 3, it is the most complex due to the 2-Hz quasi-triangular output current. It will be described in other work presented in this conference [6].

Figure 5: Front and back view of BTS quadrupole PS.

Table 3: FAC Maximum Output Values and Quantities

	PS Qt	Io [A]	Vo [V]	Mod/PS
Dip	2	1100	800	8
QF	1	120	500	2
QD	1	30	45	1
Sext	2	150	45	1

CONCLUSION

Booster and transfer lines PS are ready and installed, and the first characterizations indicate that they will reach the specification. Storage Ring PS integration is in progress and must be installed in the next weeks, after which tests and measurements will take place to verify their behavior with real loads.

REFERENCES

[1] L. Liu *et al*, "Sirius status update", presented at IPAC'19, Melbourne, Australia, May 2019, paper TUPGW003.

[2] G. O. Brunheira, J. P. Bonaldo, J. N. H. da Rosa, C. Rodrigues, J. A. Pomilio, "Digital control system for high precision power supplies of the new Brazilian synchrotron source", in *Proc. COBEP'13*, Gramado, Brazil, Oct. 2013, pp. 326-331. doi: 10.1109/COBEP.2013.6785135

[3] C. Rodrigues, A. R. Silva, "A new model of bipolar power supplies for LNLS steering magnets", in *Proc. COBEP'11*, Natal, Brazil, Sep. 2011, pp.1004-1008. doi:10.1109/COBEP.2011.6085310

[4] J. N. Rosa, C. Rodrigues, G. O. Brunheira, R. J. Marcondeli, "225A/22V high precision current source using interleaved modules and digital regulation", in *Proc. COBEP'15*, Fortaleza, Brazil, Nov.-Dec 2015, pp.1-5. doi:10.1109/COBEP.2015.7420192

[5] P. Zumel, O. Garcia, J. A. Cobos, J. Uceda, "Magnetic integration for interleaved converters", in *Proc. APEC'03*, Miami Beach, USA, Fe. 2003, pp. 1143-1149. doi:10.1109/APEC.2003.1179360

[6] C. Rodrigues, G. O. Brunheira, B. E. Limeira, G. M. Rogatto, "Design and experimental results of a 1.1kA/800V AC power supply for Sirius booster dipoles", presented at IPAC'19, Melbourne, Australia, May 2019, paper TUPMP001.