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PHASE REFERENCE LINE SYNCHRONIZATION FOR LCLS-I AND LCLS-II AT SLAC*

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Abstract

With LCLS-II commissioning started and transfer-to-operations being scheduled, users will have more choices to use different scales of X-Ray free electron laser (FEL) at SLAC. LCLS-I instrument hutches and the beam diagnostic systems at SLAC have the requirements to use the same facilities to detect the X-Rays or electron beams from both LCLS-I and LCLS-II accelerators. Synchronization of the phase reference systems between the two machines is the prerequisite to achieve this goal. The LINAC Locking System at SLAC replaces the LCLS-I stand-alone 476 MHz master oscillator with one derived from the LCLS-II 1300 MHz phase reference signal. The phase initiation is realized with the timing alignment of the LCLS-I LINAC event generator (EVG) to the LCLS-II timing pattern generator (TPG) using a common subharmonic frequency. The new low noise 476 MHz phase reference is to be distributed to FACET and LCLS-I LINAC and the instrument hutches via RF-over-Fiber (RFOF) system over kilometre distance in an uncontrolled environment. This paper will discuss the system design architecture and the test results gathered during the system's commissioning.

INTRODUCTION

There are two major phase reference systems at SLAC. The Main Drive Line (MDL), originally built about 35 years ago and upgraded over the years, has been providing the low noise phase reference at 476 MHz and its harmonics to the FACET, LCLS-I LINAC, the experimental laser facilities, and timing system over distances of up to 4 km.

With LCLS-II up to operation, users will benefit from the diverse features of the next generation X-ray FEL delivered from a 4 GeV CW superconducting structure and undulator beam lines. The LCLS-II Phase Reference Line (PRL) [1], which contains high stability frequencies is based on a Master Oscillator (MO) from Wenzel at 162.5 MHz disciplined by a Rubidium standard. It is used to derive the 185.7 MHz signal for LCLS-II timing reference clock, and 1320 MHz and 3920 MHz signals for Low Level RF (LLRF) local oscillators. Importantly, it provides the forward and reverse 1300 MHz phase reference signals through the dual-directional couplers to LLRF system. This allows the technique of phase averaging to compensate for phase drift caused by the change in cable length from environmental temperature fluctuation. The LCLS-II PRL currently has two segments (L0-L1 and L2), both of which are phase controlled and power boosted with an active reflecting end at the reference point. A third segment L3 along with the extension L4 will be upgraded to the same scheme when LCLS-II-HE is complete. Measurement results show that the integrated jitter is at ~5fs from 100 Hz to 10 kHz. This phase reference system has been successfully installed and commissioned. And the performance has met the requirements [2].

LCLS instrument hutches and the beam diagnostic systems such as Tender X-Ray Imaging (TXI), and Transverse Deflecting Cavities (STCAV, XTCAV) have been built based on 476 MHz harmonics frequencies. The same instrument will be used for X-Ray detection and electron beam diagnostic from both LCLS-I and LCLS-II accelerators. This requires the synchronization and timing alignment of the frequencies between the two machines. Figure 1 is the overview of the major phase reference and timing systems along with the accelerator and experimental beam structures at SLAC.

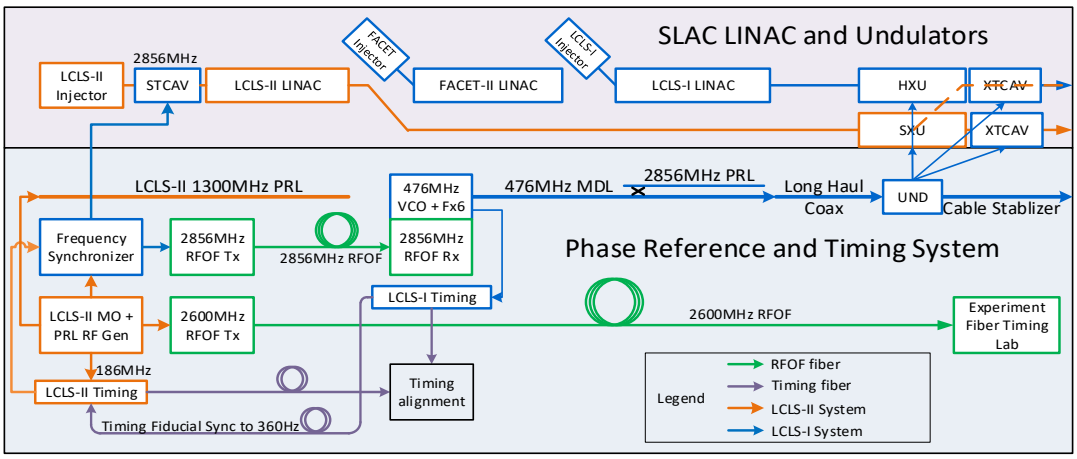

Figure 1: Overview of the phase reference lines and timing system at SLAC.

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SYSTEM OVERVIEW

Frequency Synthesizer and Timing Alignment

The 476 MHz synthesizer chassis is in the same temperature compensated rack as the LCLS-II 162.5 MHz MO. To adapt to the available frequency of the RFOF, the 476 MHz is multiplied up to 2856 MHz and then sent to the RFOF emitter. The RFOF receiver is located at the MDL starting point about 1km away, where a 476 MHz clean-up VCO will be used to replace the existing independent oscillator. Phase ambiguity during the frequency multiplication from 476 MHz to 2856 MHz could lead to phase confusion or "bucket jumps" between the RF drive signals and the beam bunches. To correct the bucket jump, the TTL signals from the LCLS-I Timing Event Receiver (EVR) and the LCLS-II Timing Pattern Receiver (TPR) will be compared and fed back to phase control to line up the 71.43 kHz signal, which is the highest common denominator between the RF frequency harmonics of the two machines. The LCLS-II Timing Pattern Generator (TPG) will be aligned to the LCLS-I Timing Fiducial for 360 Hz AC Line synchronization when the two systems operate in synchronized mode. The timing attribute between the two machines is shown in Table 1. The brief timing relationship is shown in Fig. 2.

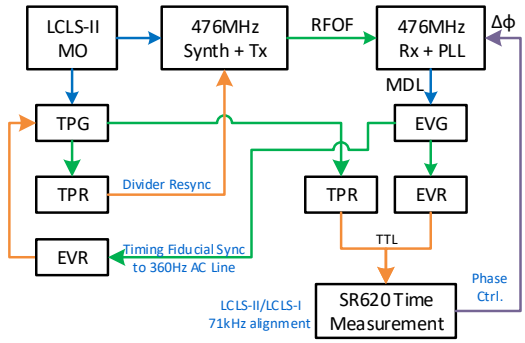

Figure 2: Timing relationship between LCLS-I and LCLS-II.

RFOF

To synchronize the LCLS-I Main Drive Line (MDL) 476 MHz to the LCLS-II PRL 1300 MHz, frequency manipulation needs to be done carefully with the least impact to the existing operating machines. The RFOF solution has been chosen due the many advantages over coax-based systems. This includes lower installation cost, excellent EMI and crosstalk rejection, inherent galvanic isolation, significantly lower transmission loss, higher fan-out capability and the absence of powerful microwave distribution amplifiers with their potential power dissipation. The Libera Sync RFOF system was chosen because of its low drift and low phase noise performance. Normal fiber optic cables have a temperature coefficient at about 40 fs/C/m. With 1 km and 20C diurnal temperature swing, which is normal in California, the phase drift could be as much as 800 ps. This is beyond the available RFOF drift compensation range but using a negative thermal expansion material such as the Linden phase stabilized STFOC with a coefficient < 10 fs/ºC/m helps alleviate this issue.

Table 1: The Timing Attribute and the Frequency Derivation for Synchronization.

Timing Attribute	Value
Master Oscillator (MO)	162.5 MHz
LCLS-II Phase Reference (Linac RF)	1300 MHz
Clock (Timing Ref and GUN RF) = Linac RF/7	185.7 MHz
Nominal Beam Rate = Clock/200	0.92857 MHz
LCLS-II Fiducial Resync Frequency = Linac RF/18200	0.07143 MHz
Fiducial (Power Line Phase)	360 Hz
LCLS-I Phase Reference (MDL RF)	476 MHz
LCLS-I Fiducial Resync Frequency = MDL RF/6664	0.07143 MHz

FREQUENCY SYNCHRONIZATION

The new MDL 476 MHz reference signal will be generated from the LCLS-II 162.5 MHz MO with certain derivatives. The derivative relationship is shown in Table 2.

Hardware Design

Two RF frequencies are picked up from the LCLS-II 162.5 MHz MO and the 1300 MHz PRL Signal Generator. The 162.5 MHz is multiplied up to 487.5 MHz. The 650 MHz is coupled out from the 1300 MHz multiplication circuit. A 11.5 MHz signal is then derived through frequency division and signal mixing as shown in Table 2. The 487.5 MHz multiplied from MO is mixed with 11.5 MHz to generate 476 MHz. Two Phase Lock Loops (PLL) with 11.5 MHz and 476 MHz VCOs are implemented for cleaning up the divider harmonics and mixer products. Figure 3 shows the block diagram of the synchronization process.

Table 2: Frequency Derivation from LCLS-II 162.5 MHz MO to LCLS-I MDL 476 MHz

Linac Locking Derivation	Value
Frequency Division-1 = (MOx4)/26	25 MHz
Frequency Division-2 = 25/2	12.5 MHz
Frequency Division-2 = 25/25	1 MHz
Mixer-1 Frequency = 12.5-1	11.5 MHz
MOx3 = 162.5x3	487.5 MHz
Mixer-2 Frequency = 487.5-11.5	476 MHz

Modern frequency synthesizers can generate a variety of output frequencies with good resolution. However, even with a low noise synthesizer, the close-in phase noise at the offset sideband <1 kHz can only be around -120 dBc/Hz

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for optimal performance, as the downstream system referenced from the same source could be sensitive down to this noise level. An AD9515 frequency divider from ADI provides enough division resolution with low phase noise at the close-in sideband of the carrier. The chip has internal bias that can be configured for all the programmable pins,

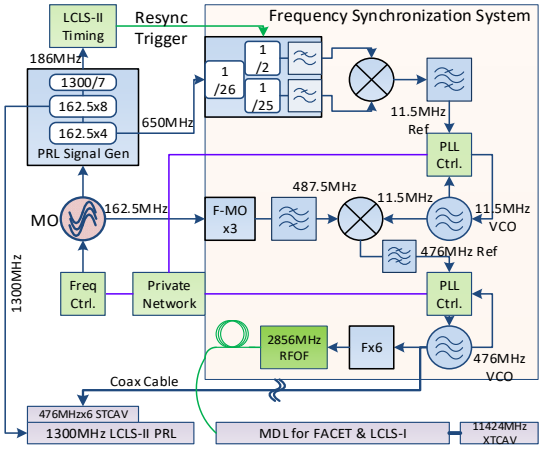

Figure 3: The block diagram of the frequency synchronization.

saving effort with externally controlling the chip. A risk with frequency dividers is that they have the non-deterministic phase due to the different division edge and the initial state at power up. This could lead to phase uncertainty on all subsystems. To fix this, the AD9515 has a SYNCB pin that takes external triggers from LCLS-II TPR for phase initialization. The trigger delays and widths are adjusted to fit the divider setup and hold time.

Careful filtering design helps significantly for low noise signal generation. Our prototype with passive filters in combination with signal balancing has produced good results to suppress the noise from the frequency dividers and the unwanted products from the mixers. New design will consolidate this feature with compact configuration in the future.

Control

As described above, the frequency dividers are selfsustained, so they do not need external control. The PLL control software and hardware take advantage of the LCLS-II PRL design using the in-house designed downmixing electronics and data acquisition units with integrated FPGA. The two PLLs for the 11.5 MHz and 476 MHz signal have similar analog downmixing frontends with free running LOs to generate 250 kHz IF signals for digitization by a 16bit ADC. The IF is further digital down-converted by the numerical controlled oscillator. A Xilinx CORDIC is utilized to convert the in-phase and quadrature signal to phase and amplitude for phase comparison. Because each VCO has a low frequency low pass filter in its V-tune signal path, the unity gain frequency of the loop filter has to be placed around 100 Hz. This presents a challenge as the low frequency gain of the loop will be low, thus hindering the loop's ability to correct large frequency drift. This is not an operational concern because the system will be enclosed in a temperature-controlled rack that has a tolerance of +/-1C. The phase locked loop parameters can be configured, and the loop status is reported via EPICS channel access. All the control modules are accommodated in Stanford Research System SIM platform. Figure 4 is a brief diagram for the PLL control.

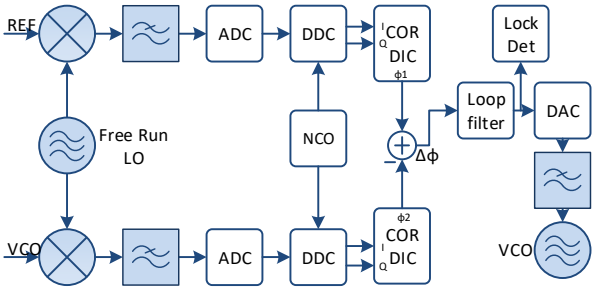

Figure 4: Downmixing and digitizing diagram for the 11.5 MHz and 476 MHz PLLs.

Measurement Results

The prototype chassis has been tested in the lab with the LCLS-II devices and the timing system. The preliminary phase noise measurement result of the 476 MHz from the synchronization chassis is shown in Fig. 5. The integral jitter from 10 Hz to 10 MHz is 17.5 fs, which is lower than the existing MDL phase noise. The added jitter between locked VCO and free running VCO is 1.83 fs. There is potential to optimize the PLL with further fine tuning via the algorithm. The in-house built 476 MHz x6 multiplier was measured to add 0.2 fs of jitter from 10 Hz to 10 MHz. This can be used in many applications with only a 5VDC power supply. The integration test with the RFOF is planned in April 2023.

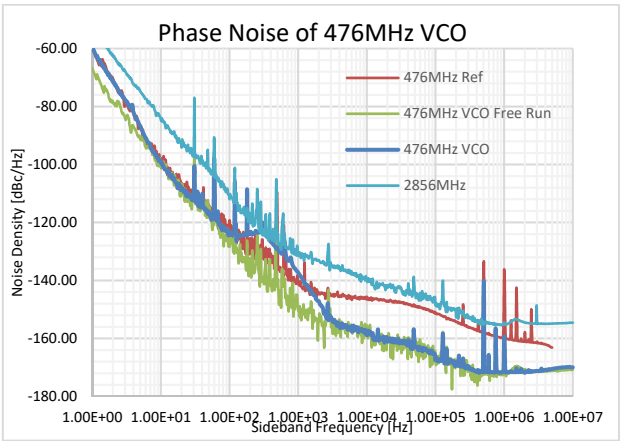

Figure 5: Phase noise measurement of the 476 MHz signal synchronized to 162.5 MHz MO.

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