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Full Length Article

Space resolution measurement and threshold calibration of the iRPC detector☆

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ABSTRACT

In preparation for the High-Luminosity upgrade of the LHC, the CMS Muon spectrometer is undergoing an upgrade, incorporating four new stations of improved Resistive Plate Chambers (iRPC) that will extend the pseudo-rapidity coverage to the range of 1.8 to 2.4. The iRPC chambers explore an approach of 2D readout using the readout strips with a signal collection from both sides. A dedicated Front-End Board (FEB) has been designed to read the iRPC signals and tag them in time using a high-precision Time-to-Digital Converter (TDC). This paper presents two new aspects of the FEB characterization on the test bench and the chamber. First, a precise measurement of the charge to threshold calibration for the FEB. Second, the measurement of the space resolution of the FEB on the chamber using cosmic muons. It is concluded that the FEB on the chamber can operate with a threshold around 40 fC, an absolute space resolution between 0.5–1.5 cm, and an absolute time resolution of 500 ps.

1. Introduction

During the High-Luminosity CERN LHC (HL-LHC) operation phase, the instantaneous luminosity will increase to 5 – 7.5 × 10^{34} cm^{-2} s^{-1}, i.e., a factor 5–7.5 above the LHC design value. The projected integrated luminosity of 300 fb^{-1} for Phase-1, the current LHC period, will increase by an order of magnitude to 3000–4000 fb^{-1} in the coming two decades (Phase-2) [1]. The CMS experiment [2] at the LHC is implementing several upgrades to the current detector to enhance its sensitivity to physics searches and address significantly harsher operating conditions. The background levels, in-time pileup and detectors ageing increases all proportionally to the instantaneous luminosity. One such upgrade includes the addition of new improved Resistive Plate Chambers (iRPC) in the inner rings of two muon endcap stations [3].

The RPC chambers of the CMS experiment could not operate in this region even during the LHC phase due to an excessive level of radiation [3]. In contrast the iRPC were designed to work during the full HL-LHC phase with an efficiency above 95%. The main features that qualify the iRPC chambers for harsher conditions are the reduction of the thickness of the gap from 2 mm to 1.4 mm. Consequently, the charge produced inside the gap by a crossing particle is reduced by a factor of 3. The background capability is therefore increased by a factor of 3. To sense the reduced charge and filter out the background offline using the position and timing, a dedicated 2D readout system was designed with a dedicated Front-End Board (FEB). The RPC chambers instead used a 1D readout with the shortest stips length above 20 cm [4].

The details of the iRPC chambers are provided in previous studies [5,6], while an in-depth description of the iRPC Front-End Board (FEB) can be found in Ref. [7]. This latter reference outlines the FEB architecture, the Time-to-Digital Converter (TDC) calibration, the charge calibration of the Frond-End ASIC thresholds, and the results of irradiation tests. Additionally, it includes a dedicated section on the FEB certification process. In this report, we present updates on the charge-to-threshold calibration and new results on the absolute spatial resolution of the FEB when deployed in the chamber. These results are presented for the final version of the iRPC chamber and FEB, ready to be installed in CMS.

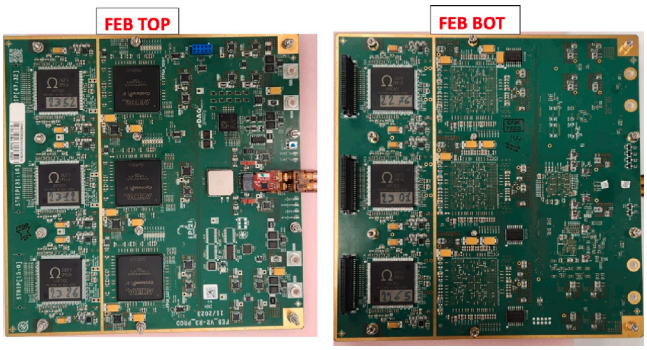

Fig. 1. A photo of the iRPC FEB. LEFT: top view; RIGHT: bottom view.

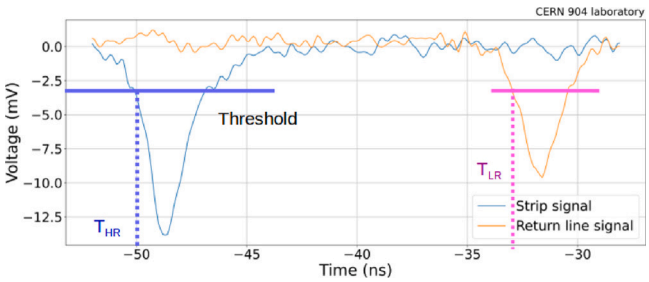

Fig. 2. Example of the iRPC signal and the measurement procedure by the iRPC FEB. The HR (LR) signals are shown by plain blue (orange) curves. The electronic threshold applied by a PetiROC2C are given by blue (purple) thick horizontal lines. The associated time identified by the TDC are given by blue (purple) thick dashed vertical lines.

2. The iRPC project and the FEB

In a nutshell, they are wedge-shaped double gas gap chambers similar to the existing endcap RPC with radially oriented readout strips between two gas gaps. These gaps are made of two High-Pressure Laminate (HPL) electrodes (1.4 mm thick) coated with a thin graphite resistive layer. The distance between the electrodes is 1.4 mm, and a constant field of around 50 kV/cm is applied. When a muon traverses the gaps, it induces an electromagnetic avalanche that generates a signal on the pick-up strips with a typical amplitude of 300 fC.

The pick-up strips are integrated into a three-layer trapezoidal Printed Circuit Board (PCB) containing 48 readout strips with a strip pitch of 0.5–1 cm and a strip length of 1–1.5 m depending on the station and detector area. Each chamber is equipped with two PCBs covering the left and right sides.

Signals propagate to both ends of the strips and are carried via narrow return lines to three ERNI connectors per PCB positioned on the wide edge of the trapezoid. This edge, referred to as High radius (HR), is located 3 m away from the beam axis and benefits from the lowest irradiation levels optimal for the Front-End Board (FEB).[1] The FEB processes and transmits signals from both ends of the 48 strips on each PCB (96 signals in total).

The iRPC FEB version 2 revision 3 is a low-noise front-end electronics board capable of detecting signals below 50 fC. A two-sided photograph of the board is shown in Fig. 1. The signal received from the strips is preamplified and discriminated within the PetiROC2C chip.[2] The fast front-end ASIC, PetiROC2C, is a 32-channel version developed using AMS 0.35 µm SiGe technology. It features a preamplifier with 1 GHz bandwidth and a gain of 25, coupled to a fast comparator with a programmable threshold. Each ASIC utilizes 16 channels out of 32 available to minimize internal cross-talk effects, and the board hosts six ASICs (three on the top side and three on the bottom).

The discriminated digital signal is transferred to an INTEL Cyclone-V FPGA, where it is processed by a Time Digital Converter (TDC) module employing a tapped delay line (TDL) architecture [11]. The main coarse clock of the TDC works at 400 MHz, while a fine 8–bit clock defines the Least Significant Bit to be around 10 ps. The time resolution of the TDC was measured to be 16 ps, using a generated signal injected into two TDC channels with a constant delay between them. The test was repeated for various delay times ranging from 3 to 32 ns, and the TDC response was perfectly linear [12].

An FPGA also serves to slow control two PetiROC2C (one above and one below). Each board carries 3 FPGA's. The central FPGA, referred to as the master, serves as a signal concentrator from the left and right FPGAs[3] and a communication hub with the CERN GBTx chip [13]. It serves to pack the GBT frames for the VTRx optical transceiver [14] sending data to a back-end board. The slow control of the FEB is operated through a CERN SCA ASIC [15]. For all measurements in this report, a simplified back-end board (BEB) from the quality control bench described in Ref. [7] was used.[4]

An example of the iRPC signal readout by a high-frequency oscilloscope is shown in Fig. 2. The LR signal, which travels a significantly longer way through the transmission line than the HR one, is more attenuated. The signal identification procedure involves applying a threshold on the leading edge of HR and LR and tagging them in time using a TDC. Later the HR (LR) timing T_{HR} (T_{LR}) measurements can be used either to measure the absolute signal time with $T_{mean} = (T_{HR} + T_{LR})/2$, or the position along the strip with $\Delta T = T_{HR} - T_{LR}$. The resolution on T_{mean} was measured around 500 ps [16]. It is dominated by the detector effects such as the initial drift time before the showering, signal shape fluctuations, time walk effects, and dispersion during propagation along the strips and return lines (up to 3 m in some cases). For ΔT, detector effects largely cancel, resulting in a better resolution of 160 ps [12].

3. The charge-to-threshold calibration

3.1. The noise pedestal

The threshold is provided by a 10-bit Digital-to-Analog Converter (DAC). For a given channel, if THR is too low, the channel will continuously trigger on noise; if it is too high, the trigger count will be 0. The transition value between the two regimes is called a pedestal: PD.

For each channel i, PD_i is measured individually. A procedure schematic is shown in Fig. 3. The 10-bit DAC value is incremented in steps of 1, and the number of triggers is counted over a 1 ms window. Below PD_i, the trigger activates continuously, limited only by the intrinsic PetiROC2C and TDC dead time.[5] Around the threshold, the count drops rapidly, reaching zero a few units above the threshold. The resulting shape resembles an S-curve.

[1] The total expected integration doses in this region is estimated to be 20 Gy, while the flux of high energy hadrons (with energy above 20 MeV) does not exceed 2000 $s^{-1}cm^{-2}$. After a series of radiation hardness tests, we have demonstrated that the FEB with the Cyclone V FPGA, which is not considered a radiation hard device, can operate in these conditions [7]. This would not be the case if the electronic was positioned on the opposite side of the chamber, Low Radius (LR), around 1.5 m from the beam axis where the radiation levels are 10 times higher.

[2] This chip is an adaptation of PetiROC2 A chip [8–10] for iRPC needs.

[3] The chirality is defined when looking from the optical transceiver side as in Fig. 1.

[4] The simplified BEB can read only one FEB. To read multiple FEBs, another BEB based on micro-TCA crate was developed [12].

[5] The minimal dead time was measured to be around 10 ns.

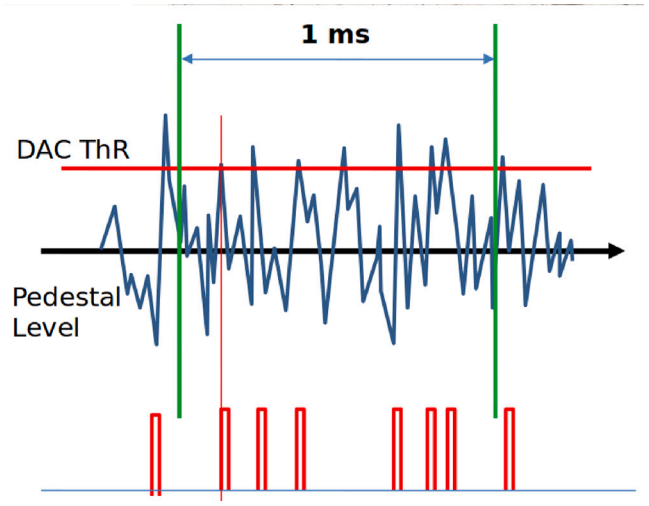

Fig. 3. Schematic view of the procedure used to identify the pedestal PD_i of a channel i.

The S-curves for all 16 channels of an PetiROC2C ASIC are shown in Fig. 4 (Top). To align all PD_i values to a unique PD per ASIC, each channel is equipped with a 6-bit DAC tuner to shift PD_i up or down. A multi-step procedure was developed to finely adjust PD_i to a common value PD.

An example of the alignment procedure is shown in Fig. 4. In the first step, all 6-bit DAC are set to 32, and the 16 S-curves are produced. In the second step, a median PD value is identified (345 in the example), and the 6-bit DAC is adjusted so that all PD_i values coincide ±2 10-bit DAC units. This process can be repeated iteratively for better convergence. During operations, the obtained 6-bit DAC constants and the PD value are saved in a database. It has been verified that the 6-bit DAC values remain stable over years of operation.

3.2. The charge-to-threshold calibration

The applied signal threshold, THR, is defined as

$$\mathrm{THR} = \mathrm{PD} + \mathrm{eTHR}$$

where eTHR is the effective threshold. The eTHR value of 7 DAC units [6] ensures a low noise level in the chamber (less than 1 Hz/cm^2) [7]. A safer value of eTHR = 10 DAC units is still recommended to reduce the residual signal-induced loopback effects such as retriggering [7]. We need to perform a calibration procedure to understand this threshold's physical meaning.

The calibration step establishes the relation between the total charge of a real iRPC signal and eTHR.[6] A typical signal obtained with a fast oscilloscope is shown in Fig. 2. It is approximately triangular, with a sharp leading edge $T = 1.8 - 2$ ns.

The input signal is generated following the scheme in Fig. 5: a pulse generator produces an asymmetric triangular signal with a leading time (τ_G) between 1 and 4 ns, a maximum amplitude in the range [100, 300] mV, and a slow falling edge lasting a few microseconds. The generator is connected to a 40 dB attenuator and an RC circuit with a time constant $\tau_{RC} = 0.5$ ns, using R = 50 Ω and C = 10 pF.[7] The input impedance of the PetiROC2C chip is 200 Ω while one of the pick-up strips was estimated to be 53 Ω, to adapt both a 73 Ω resistor was added on the FEB used in parallel with the PetiROC2C input.

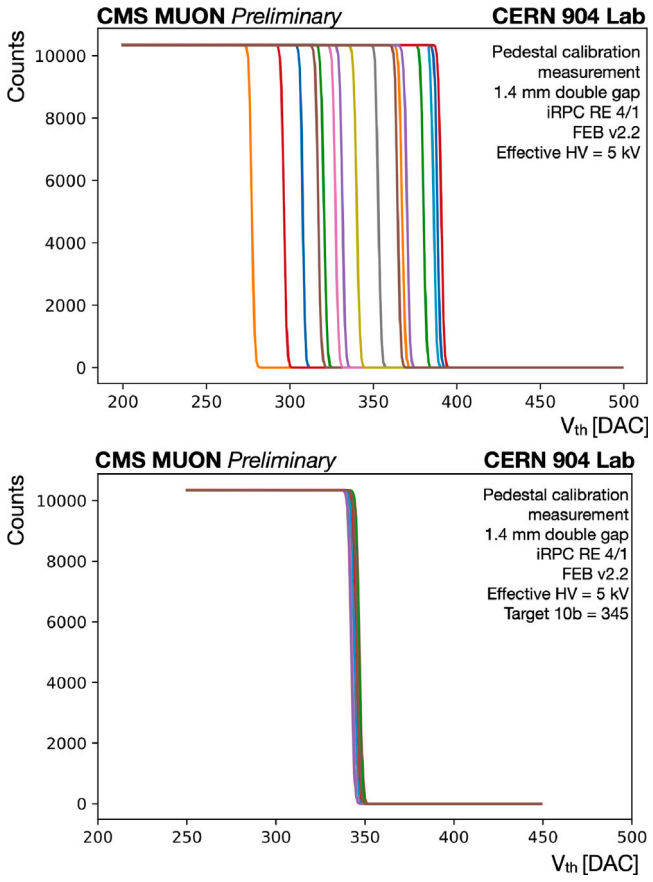

Fig. 4. TOP (BOTTOM): the S-curves of 16 channels used by an PetiROC2C before (after) alignment procedure.

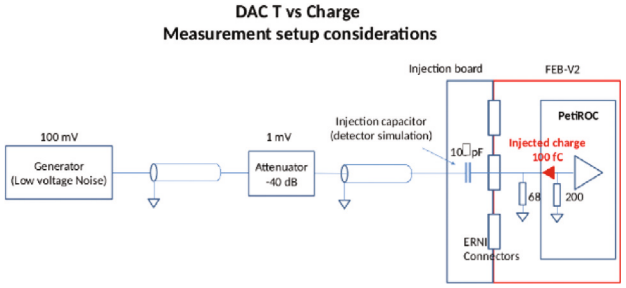

Fig. 5. Experimental setup used to calibrate the iRPC FEB. The components inside the red area are part of the FEB.

The desired signal shape generated by the oscilloscope is sketched in Fig. 6: an isosceles triangle with a base twice the leading time T (ns), height h equal to the voltage drop amplitude (mV), and total area A (green) equal to the signal charge. The latter can be obtained by $A = 2T \cdot h/2 \cdot 50\,\Omega$. Since the capacitor's charge is independent of the leading time or voltage amplitude, increasing the leading time (triangle base) decreases the voltage amplitude (triangle height).[8]

It was verified by varying τ_G between 1 and 4 ns that the total charge remains constant. The effective leading time (τ_{eff}), defined as

[6] It shall be noted that we do not use the ADC output of the PetiROC2C chip, but the trigger outputs sensible to the voltage of the input signal.

[7] The exact capacitor value was measured *in situ*.

[8] It is important to notice that only the left part of the signal before the peak have to match well the iRPC signal since the PetiROC2C discriminates only the leading edge. Therefore, the exact shape of the falling edge does not need to be modeled very precisely.

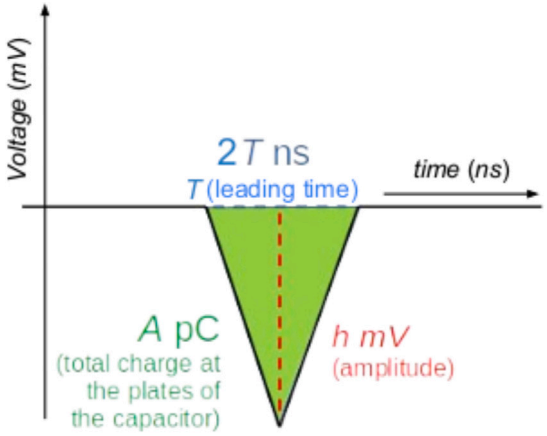

Fig. 6. The simplified model of an iRPC signal. It is a triangle with basis of $2T$ ns, a height of h mV and a total area of A pC obtained by the formula $A = 2T \cdot h/2 \cdot 50\,\Omega$.

the time between 10% and 90% of the signal height, slightly exceeds τ_G due to distortion effects, including those from the RC circuit. The relation $\tau_{eff} = f(\tau_G)$ was therefore precisely measured.

For each channel, various amplitudes were injected for different τ_{eff}. For each amplitude, the threshold in 10-bit DAC units was recorded. The resulting curves were fit with linear functions, as shown in Fig. 7.TOP. The slope of each function was averaged over 4 channels and corrected to establish the linear relation between the calibration factor f_{cal} (fC/DAC) and τ_{eff} (Fig. 7.BOTTOM).

Several systematic uncertainties were considered in the fit procedure:

- Statistical uncertainties when averaging over 4 measurements.
- Measurement uncertainties for C.
- Approximations in $\tau_{eff} = f(\tau_G)$.
- Uncertainties in eTHR.

For a typical iRPC signal, the calibration factor is:

$$f_{cal} = 4.25 \pm 0.05\,\text{fC/DAC} \quad (1)$$

Thus, 7 DAC units correspond to $29 - 30$ fC, and 10 DAC units correspond to $42 - 43$ fC.

4. The measurement of the absolute space resolution

We designed a cosmic ray telescope comprising four small chambers, each consisting of a single electrode with a gas gap of 2 mm and Bakelite electrodes, also 2 mm thick.[9] Each gap is read out by a printed circuit board (PCB) with dimensions $30 \times 50\,\text{cm}^2$, containing 1536 pickup pixel pads of size $1 \times 1\,\text{mm}^2$. The signals from the PCB are extracted using the electronic design developed for the SDHCAL prototype [17].

An iRPC chamber is positioned between two pairs of telescope chambers surrounding the HR region (between 15 and 65 cm), as shown in Fig. 8. Both systems are synchronized in time. Cosmic ray tracks are reconstructed by requiring at least three effective chambers out of four, assuming straight-line propagation. Only high-quality tracks are retained, corresponding to muons that traverse the entire system without significant scattering. The total rate of high-quality reconstructed tracks is approximately 3–4 Hz.

The expected position of a hit in the iRPC chamber is determined by linear extrapolation with a precision of about 4 mm. This position

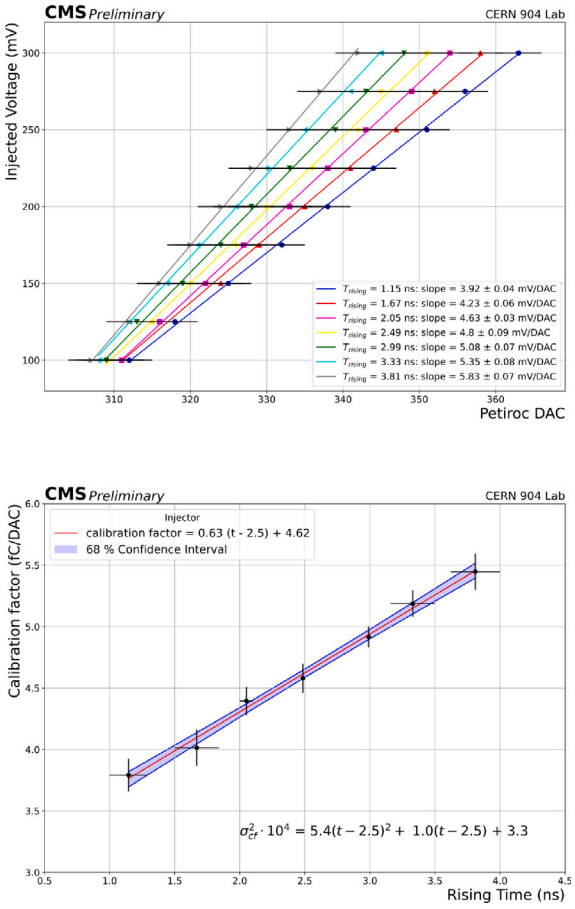

Fig. 7. TOP: Relation between injected voltage and PetiROC2C response for different τ_{eff}. BOTTOM: Calibration factor f_{cal} as a function of τ_{eff}. Error bars represent uncertainties, and error bands are shown for the final linear fit.

is compared to the best estimate of the central position of the iRPC cluster to measure the spatial resolution in directions approximately perpendicular (Δx) and parallel (Δy) to the strips.[10]

The iRPC clustering algorithm is based on strips where the Front-End Board (FEB) collects signals from both sides, referred to as a 'hit'. The local strip geometry determines the x position. In contrast, the y position is calculated from the time difference between the HR and LR, corrected for the strip geometry and the signal propagation speed. The corrected average HR and LR times serve as the absolute time estimate for the hit. The earliest arriving hit is used as the cluster seed, and additional hits are added to the cluster if:

- The hit is adjacent to one of the hits in the cluster.
- The absolute time difference between the candidate hit and the nearest cluster hit is less than 3 ns.
- The distance between the candidate hit and the nearest cluster hit is less than 20 cm.

In all other cases, a new cluster is formed. The central strip of the cluster is defined as the hit with the highest charge. Typically, a cluster consists of three hits, and usually, only one cluster is reconstructed. The cluster position is taken as the location of the hit with the highest

[9] These electrodes are similar to those used in the CMS RPCs

[10] The coordinate system is defined as follows: the x-axis runs along the base of the chamber, and the y-axis runs along the central strip of the chamber. Due to the wedged shape of the PCB, the strips are tilted between 0 and 10° relative to the x and y-axes.

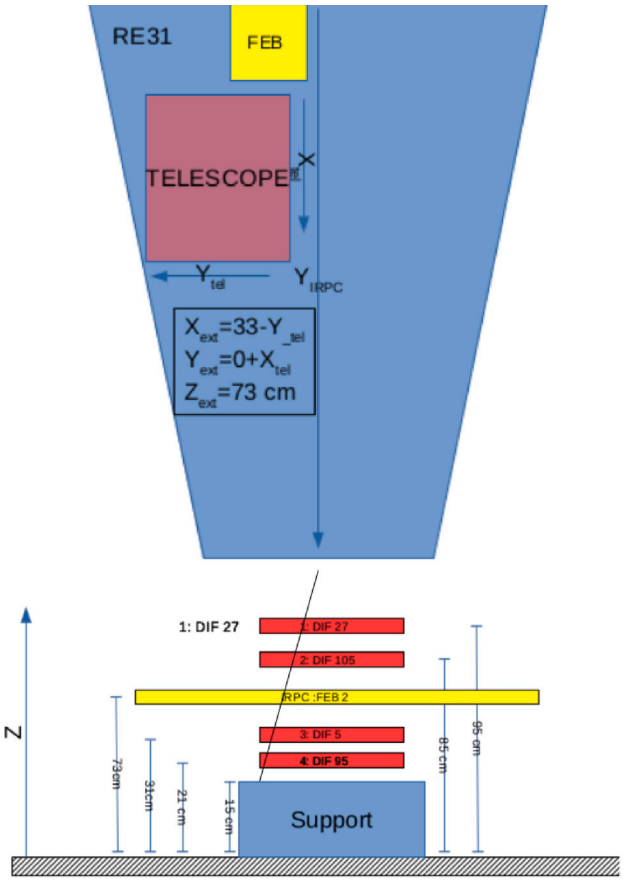

Fig. 8. Top and side views of the cosmic ray telescope.

expected charge. There is a correlation between the measured time and the total charge, referred to as "time walk." The hit with the largest charge is interpreted by the FEB as arriving slightly earlier than the others. Therefore, the earliest hit in the cluster is used to estimate the entire cluster's position. It was observed that, for clusters with three hits, the earliest hit tends to be the most central, as expected based on charge induction models. Resolution and position bias measurements have confirmed this assumption as the most reliable.

The resolution measurements are shown in Fig. 9. The resolution in the Δx direction is better than 0.4 cm, primarily determined by the strip pitch, which is approximately 0.8 cm in this region. No significant bias was observed.

The resolution in the Δy direction is about 1.5 cm, as shown in the same figure. This value is larger than Δx and is primarily influenced by the relative time resolution of the FEB on chamber $\Delta T \sim 160$ ps. The slight asymmetry in the distribution is associated with the tilt of the strips relative to the y-direction. A similar effect is observed in the correlation between the x and y resolutions in the 2D plot. This resolution is improved by an order magnitude compared to a similar CMS RPC chamber and is critical to push further the background filtering using the space information.

The iRPC chambers will be located 9–10 m from the interaction point. The relative resolution of 0.5–1.5 cm corresponds to an angular resolution of approximately 1 mRad, which is within the requirements for reconstructing high-quality muon trajectories in CMS.

5. Conclusion

We characterized the final version of the FEB designed for the iRPC chamber. In the first step, we measured precisely the calibration

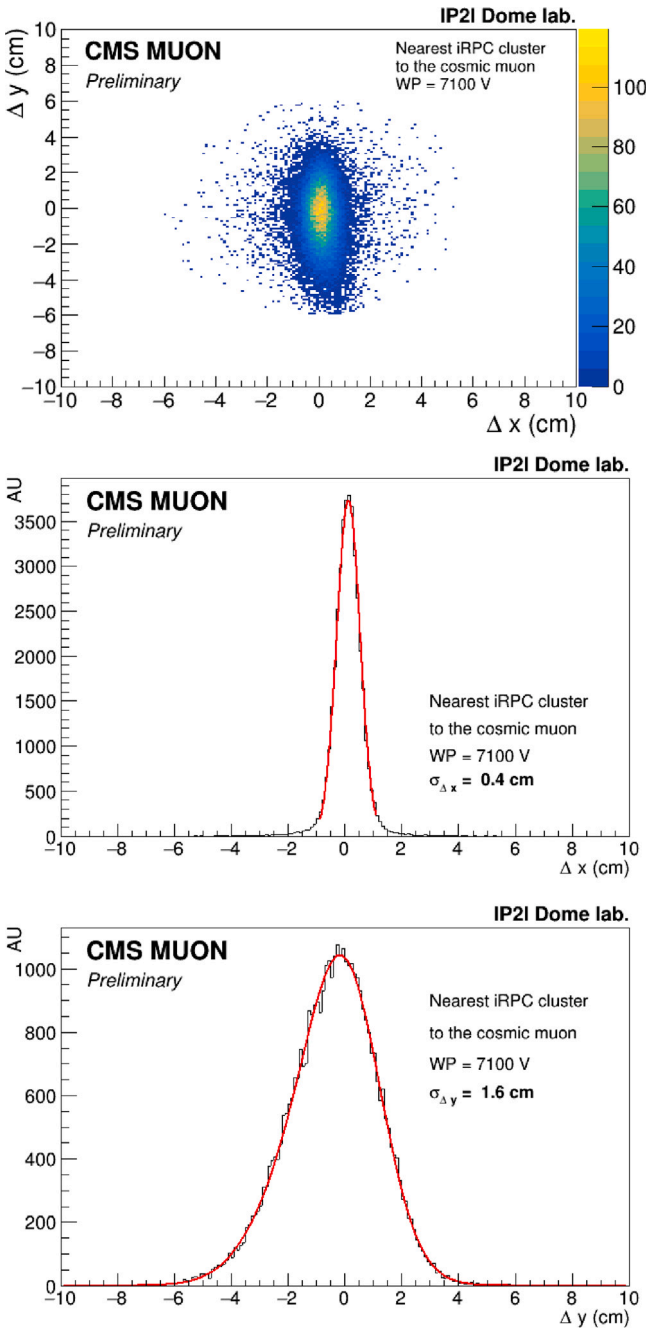

Fig. 9. Top: 2D resolution map of the iRPC chamber. Middle: Resolution along the strips; Bottom: Resolution transverse to the strips.

factor, which allows us to convert the discrimination threshold of the PetiROC2C expressed in DAC units to fC, assuming the RPC signal. It was found that the chamber can safely operate with a threshold around 40 fC. In a second step, we measured the absolute space resolution to be between 0.5–1.5 cm. In the past, we already measured the absolute time resolution around 500 ps. These measurements prove that the iRPC project meets the requirements of the CMS experiment defined at the beginning of the project.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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