ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP10

A HIGH-PRECISION LOW-LATENCY DBPM PROCESSOR FOR HALF*

J. J. Qin, Y. Tang, K. X. Hou, Z. Y. Li, L. Zhao†
State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei, China
Department of Modern Physics, University of Science and technology of China, Hefei, China

Abstract

Hefei Advanced Light Facility (HALF) is a fourth-generation vacuum ultraviolet and X-ray diffraction limit synchrotron radiation (DLSR) light source under construction. It is expected to have an ultra-low emittance and an extremely small beam size, which requires high-precision orbit detection and fast feedback control. The processor is the key component of the digital beam position monitor (DBPM) and control system, which is required to provide a submicrometer resolution in beam position measurement with a processing latency of lower than 90 µs. This paper presents the design and testing of a high-precision low-latency DBPM processor. In order to reduce the latency and ensure the high position resolution, a specific higher sampling frequency is chosen to reduce the quantization noise platform of the analog to digital convertor and an optimized low-order filter is adopted. Specialized efforts are devoted to the low jitter sampling clock generation and low noise analog circuit design. Furthermore, a dual-pilot tone structure was employed to compensate the gain variations across the four channels of the beam monitor sensor. The laboratory test results show that the DBPM has a position resolution of better than 400 nm for turn-by-turn acquisition, better than 90 nm for fast acquisition at 20 kHz rate, and better than 20 nm for slow acquisition at 10 Hz rate, with a total latency of less than 80 µs.

INTRODUCTION

The fourth-generation synchronous radiation source has a higher brightness and smaller beam size compared to the previous light sources which means a higher stability of fast orbit feedback control is needed. Typically, a fast orbit feedback system consists of beam position monitors (BPMs), distributed controllers and correction magnets [1]. The stability of the beam orbit is critically dependent on obtaining high-resolution beam position data and minimizing feedback latency [2-3].

BPMs are non-invasive sensors installed along the cavities of synchrotron light sources to measure the lateral position of the beam. Their general structure is depicted in Fig. 1. Within the cavity, four probes interact electromagnetically with the passing particle beam to capture positional information. The electrical signals collected by these probes undergo analog manipulation, are subsequently digitized, and the beam position is then determined through digital signal processing.

* Work supported by the Fund of National Synchrotron Radiation Laboratory at University of Science and Technology of China (KY2360000005) and the Youth Innovation Promotion Association, CAS.
† zlei@ustc.edu.cn

The Hefei Advanced Light Facility (HALF) is a fourth-generation light source under construction using a diffraction-limited storage ring. Its radiation spectrum is mainly located in the vacuum ultraviolet and soft x-ray regions [4]. The main expected parameters of HALF storage ring are given in Table 1.

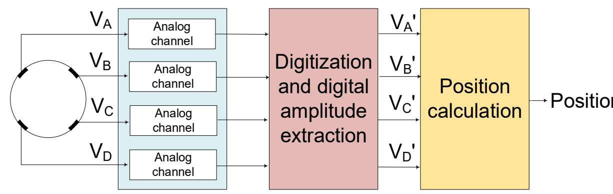


Figure 1: The general structure of beam position monitor.

Table 1: Expected Parameters of HALF Storage Ring

Parameter	Value
Circumference	480 m
Energy	2.2 GeV
RF frequency	499.8 MHz
Harmonic number	800
Current	>100 mA
Natural beam emittance	85.1 pm·rad
Horizontal beam size	>5 µm
Vertical beam size	>2 µm

To achieve ultra-low emittance and an ultra-small beam size, a high-resolution, low-latency beam position monitor is essential. In order to meet the beam orbit stability requirements of HALF, the beam position monitor system must achieve a position resolution of less than 200 nm in Fast Acquisition (FA) mode at a sampling rate of approximately 20 kS/s, providing precise position information for correction calculations. Additionally, the processing latency must be less than 90 µs to ensure that the feedback system maintains sufficient closed-loop bandwidth to suppress high-frequency interference.

This paper presents the design of a HALF Digital Beam Position Monitor (DBPM) prototype electronics. To achieve the desired high position resolution and low latency, we analyze the key factors influencing position resolution and system latency within the beam position monitor system. The design incorporates a pilot tone compensation structure, low-noise analog manipulation, and a low-jitter sampling clock to enhance resolution. Furthermore, a higher sampling frequency combined with a low-order digital low-pass filter is employed to minimize latency.

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP10

ELECTRONICS DESIGN

The block diagram of the DBPM electronics prototype is shown in Fig. 2. The system is composed of three main modules: the pilot tone coupling module, the analog manipulation module, and the digitization and digital signal processing module. Within the pilot tone coupling circuit, the four input signals are coupled with dual pilot tones. After coupling, the signals undergo amplification and filtering before being digitized. The digital signal processing stage then separately extracts the amplitudes of the beam signal and pilot tones. The beam position is subsequently calculated, using the pilot tone amplitude for calibration. In this system, both the sampling clock and pilot tone are generated by phase-locked loops (PLL), with the HALF machine clock serving as the clock source.

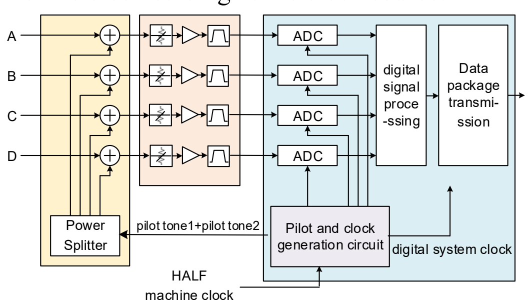


Figure 2: Block diagram of the DBPM processor prototype.

Pilot Tone Coupling Module

The pilot tone coupling module is a passive circuit aiming at coupling the beam signal and pilot tone. It consists of directional coupler and power splitter, as shown in Fig. 3. In this module, a power splitter divides the pilot tone into four equal parts for each channel. Four directional couplers accomplish the coupling of signals with a high isolation of 35 dB. The total channel-to-channel isolation is better than 70 dB.

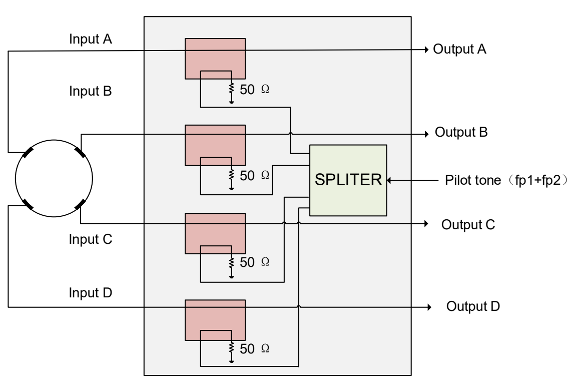


Figure 3: Block diagram of the pilot tone coupling module.

Analog Manipulation Module

Within the analog manipulation module, each channel includes three high-gain RF amplifiers, a digitally controlled attenuator, and RF switches to achieve a large dynamic range. Each RF amplifier provides a gain of 26 dB with a low noise figure. The inclusion of two RF switches allows one of the three amplifiers to be bypassed when the input power is sufficiently high, thereby reducing additional noise. The analog manipulation module also employs a ceramic dielectric bandpass filter, known for its excellent passband flatness and temperature stability, which enhances the effectiveness of pilot tone calibration by approximating the beam signal gain using the gain at the pilot tone frequency.

Digitization and Digital Signal Processing Module

In the digitization and digital signal processing module, four ADCs undersamples signals around 500 MHz, the digital signals are sent to FPGA for digital signal processing. This module also integrates pilot tone and sampling clock generation circuit as shown in Fig. 4.

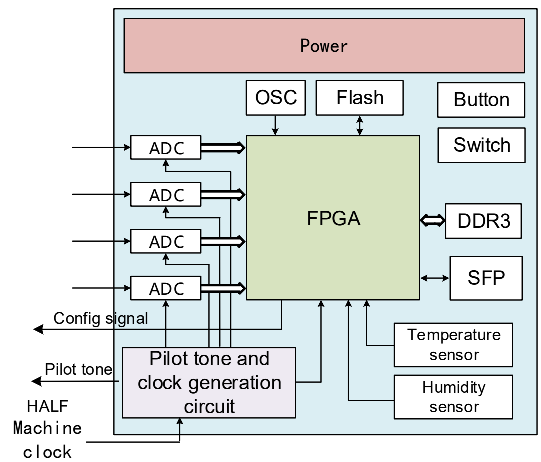


Figure 4: Block diagram of the digitization and digital signal processing module.

It is worth noting that most DBPM systems have a sampling rate of around 100 ~125 Msps. A higher frequency at 186.8 MHz is used for sampling clock to get better signal-to-noise ratio by reducing the quantization noise in the passband when the final position update rate is fixed. A higher signal-to-noise ratio helps reducing the pressure of digital filtering, so that lower digital filter order can be used to get less latency.

FPGA Logic Design

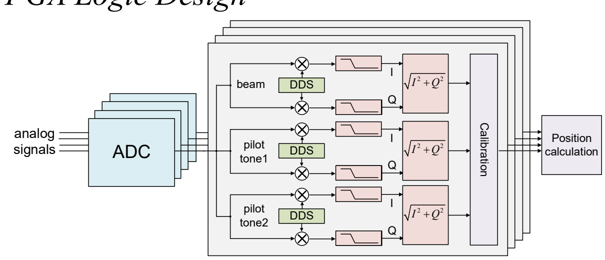


Figure 5: Block diagram of the FPGA logic.

After undersampling, the quantized digital information is sent to FPGA for digital signal processing. The structural block diagram of the digital signal processing in FPGA is shown in Fig. 5. Digital down-conversion at three frequencies is carried out simultaneously in each channel to extract the amplitude of the beam signal and two pilot tones. These

Proc. 13th International Beam Instrumentation Conference,Beijing JACoW Publishing
ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP10

amplitudes are then used for calibration and position calculation.

In order to obtain the position information in different update rate, multistage filtering and decimation are also carried out in FPGA. The digital filtering and decimation are realized by CIC filter cascaded FIR filter as shown in Fig. 6. In the whole process of beam signal processing, the latency is mainly caused by the group delay of digital filtering which is related to the input sampling rate, the decimation multiple and the filter order. The calculation of the group delay is given in Eq. (1) and Eq. (2), where N is the order of the filter, D is the decimation multiple of CIC filter, and Ts is the input sampling rate of filter.

$$t_{CIC} = \frac{NT_S + NDT_S}{2} \tag{1}$$

$$t_{FIR} = \frac{NT}{2} \tag{2}$$

In this design, FA data is obtained through a CIC filter and two FIR filters. The theoretical calculated value of filter group delay is 71.79 µs.

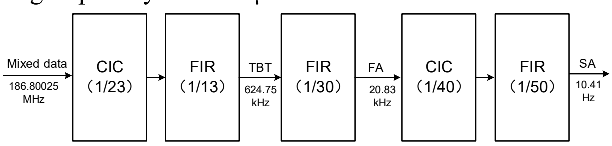


Figure 6: Diagram of digital filtering and decimation.

TEST RESULTS

The DBPM electronics prototype under test in the laboratory is shown in Fig. 7. We employed the high-precision signal source, R&S SMA100B, to generate a continuous 499.8 MHz RF signal and the RF signal is converted into four BPM inputs through a power splitter. Three modules are connected through coaxial cables. In addition to the cable for transmitting four channel signals, there is also a cable for transmitting the pilot tone. The digital module transmits position information to the PC through a network cable.

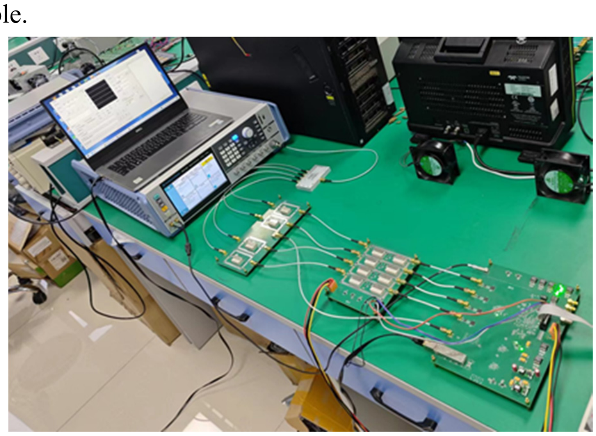


Figure 7: Test setup.

Position Resolution

In HALF, the input power of signal to the front end of the BPM processor is expected to range from -69.5 dBm to -17.4 dBm, corresponding to a beam current of 1 mA to 400 mA. For an input power of -17.4 dBm corresponding to a beam current of 400 mA, the resolution was measured to be 87.3 nm (horizontal)/88.1 nm (vertical) in FA mode at an update rate of around 20 kHz, 365.6 nm (horizontal)/386.8 nm (vertical) in TBT mode at an update rate of 624.75 kHz, 18.8 nm (horizontal)/17.0 nm (vertical) in SA mode at an update rate of around 10 Hz. The value of $K_{x,y}$ in the calculation is 9.2 mm. Figure 8 shows the horizontal and vertical position in 10 seconds in FA mode.

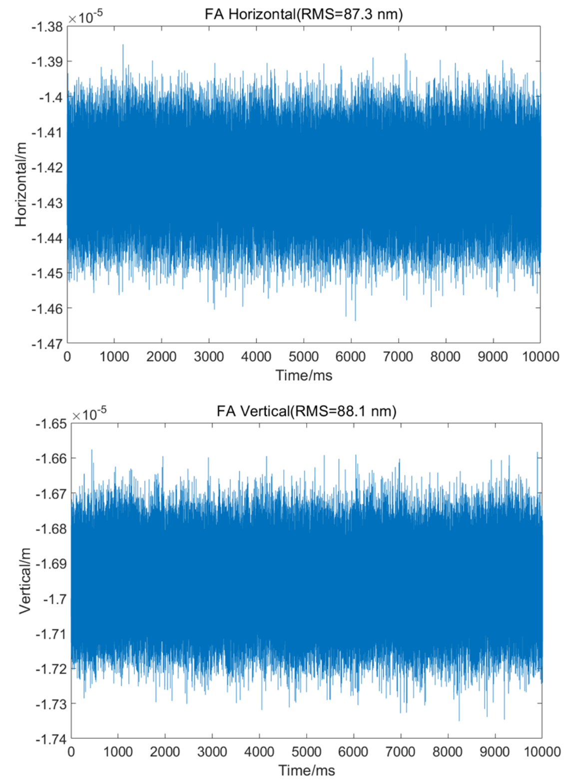


Figure 8: Horizontal and vertical FA data.

The power spectral density of position information is shown in Fig. 9. It can be seen that the noise in the position data basically conforms to the characteristics of white noise. This indicates that through the selection of sampling rate, digital filtering, and asymmetric pilot tone structure, the interference of harmonics and intermodulation components on position measurement have successfully been avoided.

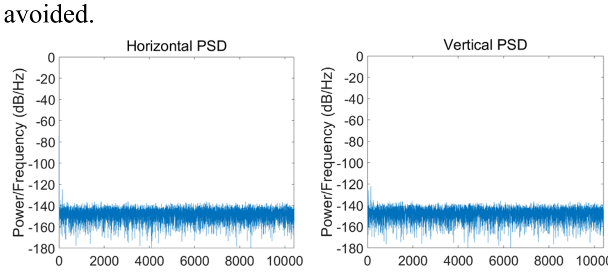


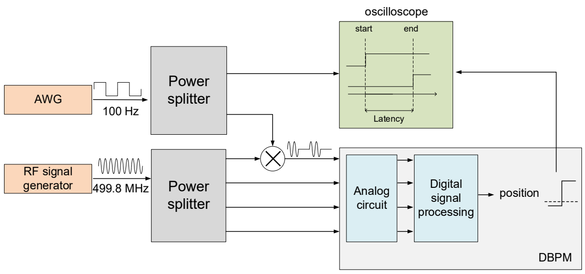
Figure 9: Power spectral density of horizontal and vertical FA data.

Latency

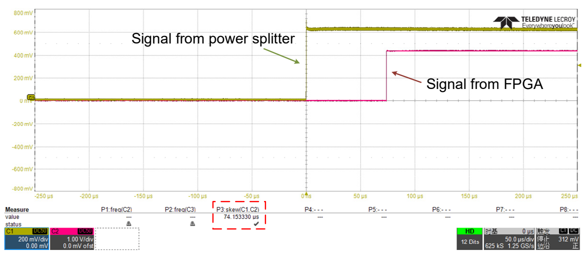
DBPM latency can be defined as the delay between input signal changes and position information changes. In order

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP10

to evaluate the latency, a testing platform in Fig. 10 was built. A 100 Hz square wave generated by an arbitrary waveform generator is mixed with one of the DBPM input signals to make the amplitude of the input signal changes at a frequency of 100 Hz. Meanwhile, the position information obtained by the DBPM will also changes at the same frequency. By comparing the front edge of input square wave and output position change, the system latency is measured to be 74.2 μs.



(a)



(b)

Figure 10: Latency test. (a) Block diagram of the test setup; (b) Latency observed by oscilloscope.

Besides position calculation latency, the total system latency should also include data transmission latency. To evaluate this part of latency, a connection between DBPM and other electronics is established based on UDP, and the data transmission latency between the sender and receiver is measured to be 2.4 μs, so that the total latency is 76.6 μs.

CONCLUSION

A DBPM prototype system has been developed and tested. It consists of a pilot tone coupling module, a high-speed analog manipulation module and a digitization and digital signal processing module. In this system, an asymmetric dual-pilot tone structure is used to improve the position resolution by reducing the influence of third-order intermodulation, and a higher sample rate is used to improve the signal-to-noise ratio so that lower filter order is needed which means less latency. A series of tests were conducted in the lab to verify the performance of the prototype. The test results indicate that the position resolution in FA mode is better than 90 nm, and the latency is less than 80 μs which have met the requirements of Hefei Advanced Light Facility.

REFERENCES

[1] S. Kongtawong *et al.*, "Recent improvements in beam orbit feedback at NSLS-II", *Nucl. Instrum. Methods Phys. Res., Sect. A*, vol. 976, p. 164250, 2020. `doi:10.1016/j.nima.2020.164250`

[2] D.Y. Wang *et al.*, "Design and implementation of data transmission of fast orbit feedback system for HEPS", *High Power Laser and Particle Beams*, vol. 35, p. 074002, 2023. `doi:10.11884/HPLPB202335.220379`

[3] G. Rehm, "Ideal orbit feedback for ultralow emittance rings", *7th low emittance ring workshop.* `https://indico.cern.ch/event/671745/contributions/2794239/attachments/1583439/2502715/Ideal_FOFB.pdf`

[4] Z. Sun and D. L. Feng, "Opportunities of Advanced Physical Studies at the Hefei Advanced Light Facility", *Chin. Phys. Lett.*, vol. 41, p. 037303, 2024. `doi:10.1088/0256-307X/41/3/037303`