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A Shunt-LDO for the Electron Ion Collider in a 110nm CMOS process

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Abstract: In this work we report on the development of a Shunt LDO (SLDO) for use in the serial powering chain of staves and discs at the Electron Ion Collider (EIC). The device is designed in a 110nm CMOS technology and can supply up to 1 A at a voltage of 1.1 to 1.4 V. Simulated PSRR at DC is -56 dB, and efficiency is above 70 %. Safety features such as load overcurrent protection and the ability to shunt the current of failed parallel SLDOs are included. A first prototype has been submitted. In this work we will report on the design of the device, and on simulation results of the prototype.

Keywords: Analogue electronic circuits; Instrumentation for particle accelerators and storage rings - low energy (linear accelerators, cyclotrons, electrostatic accelerators); Particle tracking detectors (Solid-state detectors)

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1 Introduction

The Electron Ion Collider (EIC), planned to begin operation at Brookhaven National Laboratory (BNL) in the early 2030s, will be a unique facility for the study of the internal properties of the atom. The EIC's planned detector — ePIC — plans to make use of a modified version of the ALICE ITS3 MOSAIX chip (the EIC-Large Area Sensor — EIC-LAS) in its outer barrel layers [1], with the goal of reducing design risk and effort. However, using an inner barrel chip in multi-chip staves requires considerable adaptation. A supporting ASIC will be needed, mostly to parallelise the control and powering circuitry. Figure 1 shows how all these components are intended to come together to form the Silicon Vertex Tracker (SVT) of ePIC.

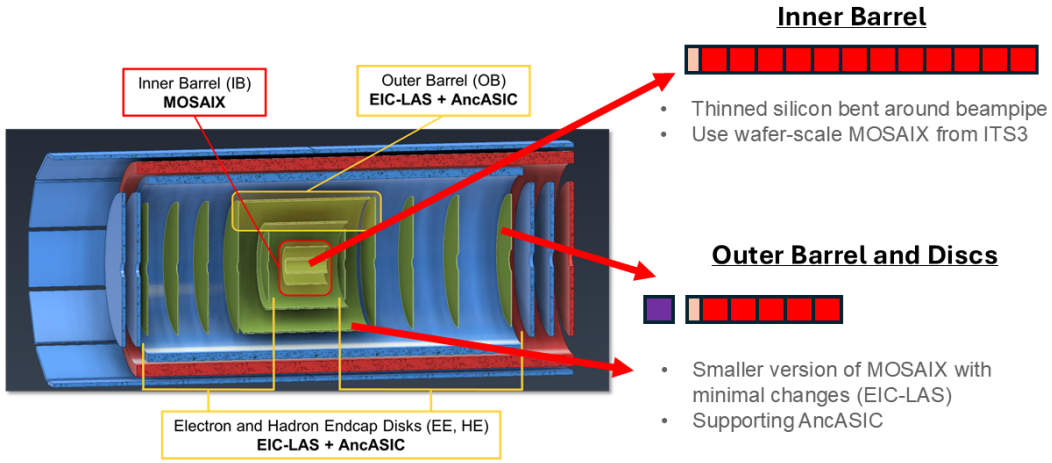

Figure 1. Planned silicon scheme for the ePIC SVT.

1.1 The Ancillary ASIC

The supporting ASIC needed to integrate the EIC-LAS is referred to as the Ancillary ASIC. It is needed because the original MOSAIX design was intended for use as a single chip per layer in only the internal layers of ALICE. This means it has several features which would lead to a high requirement for service cabling when employed in staves and discs. To reduce the cabling, these need to be serialised. This will involve adding an SLDO for serial powering, serilisation of the slow control, and provision of a locally generated negative back bias to work with the serial powering chain.

These circuits could, in principle, be included in the EIC-LAS chip. However, for several practical reasons — decoupling their development schedule from that of MOSAIX, free selection of technology, space in the MOSAIX design and ease of prototyping — it was decided to place them in a separate ASIC. The plan for the eventual AncASIC is shown in figure 2.

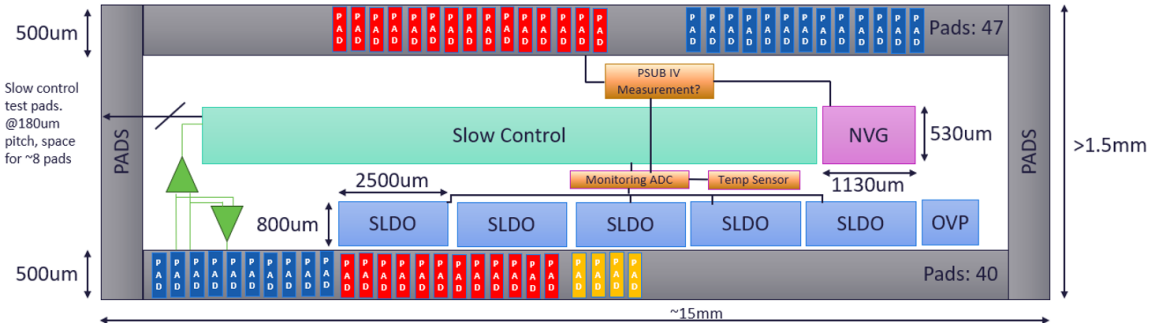

Figure 2. Top level plan for the Ancillary ASIC.

1.2 Specifications

In this work we will focus on the design of the SLDO. Its specifications are driven by the need to supply the EIC-LAS chip, and can therefore be determined from published material on MOSAIX. For example, power requirements can be found in [2]. For Power Supply Rejection Ratio (PSRR) specification, the PSRR of a device intended for the MOSAIX serialiser supply is reported in [3], so this will be used as a target. The device also requires features such as load overcurrent protection and a switchable output to support power seqeuncing of the EIC-LAS. The target specifications are shown in table 1.

Table 1. SLDO Specifications.

Spec	Unit	Value
Current Capacity	A	1
PSRR	dB	<-53 up to 1kHZ, max value below -10 across all frequencies
Efficiency	%	>70
Voltage Range	V	1.1–1.4
Additional Features		Load overcurrent protection
		Switchable high impedance output

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2 Circuit overview

In this section we give a short overview of SLDO scheme and discuss changes that were made to previously published examples to make it suitable for the ePIC detector.

2.1 SLDO scheme

The overall goal of the SLDO scheme is to combine the advantages of shunt regulators (constant input current) with those of LDOs (resistive I-V characteristic). This combination of characteristics results in a circuit which can be parallelised (needed for the supply of multi-power domain chips), and which provides a stable input current (necessary for a serial powering chain). This is achieved using the circuit in figure 3. The function of this circuit has already been well described elsewhere [4, 5], so here we provide only a short explanation:

1. M1 is the pass transistor, and together with R1, R2 and A1, forms an LDO loop which regulates V_{out}. M4 provides an additional path for shunting current when I_{in} exceeds I_L

2. To sense the current in the regulator and determine how much to shunt through M4, a small amount of current is mirrored to M2. This is compared to a reference current generated in R3.The value of this current is:
$$I_{\text{ref}} = \frac{V_{\text{in}} - V_{\text{ofs}}}{R3} \tag{2.1}$$

3. The A3-M4 loop adjusts the gate of M4 until the currents in the M5 and M6 branches match. The current in the M5 branch is $\frac{I_{\text{in}}}{k}$ and therefore
$$I_{\text{in}} = k\frac{V_{\text{in}} - V_{\text{ofs}}}{R3} \tag{2.2}$$

This results in the desired ohmic characteristic.

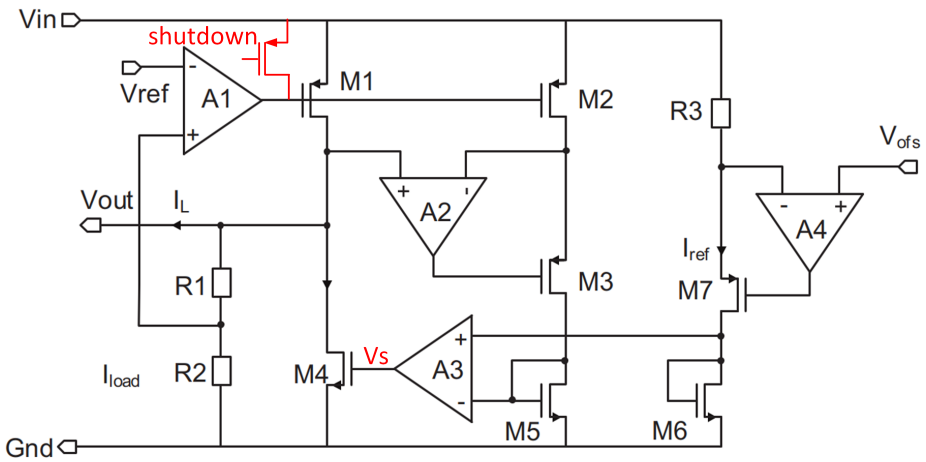

Figure 3. SLDO Circuit. Reproduced from [6]. Published under licence by IOP Publishing Ltd. All rights reserved.

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2.2 High impedance output mode

The biggest change to previously published examples of this architecture is the addition of a high impedance output mode, which this implementation requires in the event of an overcurrent condition and for power sequencing. This is created by placing a transistor switch between the gate and source of M1. This is shown in red in figure 3. This switch shorts the gate of M1 to its source and shuts down the SLDO. The result is that the output enters a high impedance condition.

An overcurrent condition is indicated when the shunted current has fallen to zero. This condition is detected by mirroring a fraction of the shunt current from the point Vs in figure 3 to transistor M1 in figure 4. Together with the current source I_{thresh} this forms a current comparator, as in [7]. When the current in M1 drops below I_{thresh}, the output of the buffer rises, triggering the disable signal and leading to a shutdown.

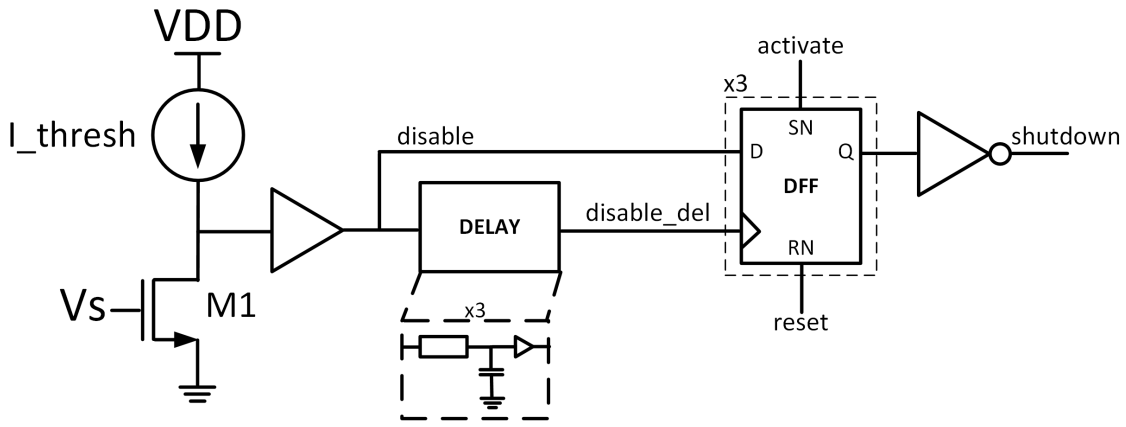

Figure 4. Overcurrent protection circuit of the SLDO.

Since short current transients caused, for example, by other SLDOs in the chain switching on or off, can lead to the shunt current dropping briefly below the detection threshold, unwanted shutdowns can occur. Therefore a small amount of hysteresis is included. The buffer's output is delayed and used to sample the original signal. The delay is implemented using a simple 3 stage RC delay line, with buffers between the stages to preserve edge speed. The purpose of this is to ensure a shutdown is only triggered when the under-shunt condition has persisted for a given amount of time. Transients shorter than around 100 µs are thus ignored. The flip-flop is triplicated for protection against Single Event Upsets (SEU).

This circuit also permits supplies to be turned off and on by setting and resetting the flip-flop, allowing for power sequencing in the case of multi-supply systems.

2.3 DAC

To achieve the required output voltage variation, the device contains a 6 bit current steering DAC which acts on Vref, allowing the output voltage to be tuned. This can vary the output from 1.1 to 1.45 V. The nominal operating voltage of MOSAIX is 1.2–1.32 V, so these output levels permit some margin beyond this. 6 bits provides a resolution of 5 mV, which is more than sufficient.

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3 Simulation results

In this section we report simulation results of the device. Firstly, functional simulations were performed to test the power sequencing using a 4 SLDO version of the AncASIC. Using the circuit in figure 4, it is possible to configure the circuit to start in an enabled state in which all supplies come on as the input current is ramped (Mode 1), or in a disabled state (Mode 0), allowing each supply to be independently enabled in the desired sequence. The results are shown in figure 5.

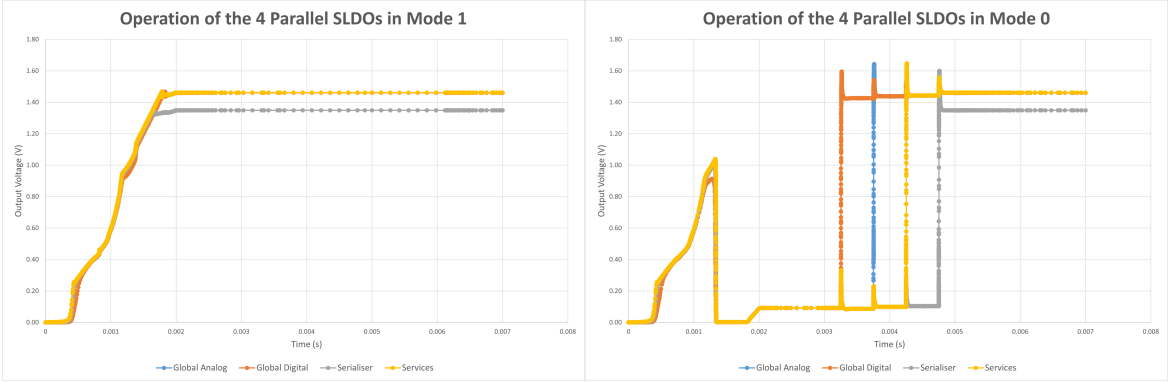

Figure 5. Functional simulation of 4 SLDO AncASIC in Modes 0 (all outputs enabled at startup) and 1 (all outputs disabled at startup and manually enabled). The 4 supplies represent those of the EIC-LAS.

PSRR and efficiency have also been simulated. Results are shown in figure 6. PSRR was simulated using a 5 mm bondwire, a 1 A load current, and a range of capacitive load values. The SLDO itself dominates the PSRR up to around 100 kHz. Beyond this, the value of the capacitive load is more critical. A best case value of -56 dB has been simulated. This is seen to degrade to around -34 dB when 5 mm bondwires are also added to the pins of the SLDO. Efficiency calculations were made across a wide range of process corners and operating conditions. Figure 6 shows a histogram of the results. Efficiency varies from 72–79 %.

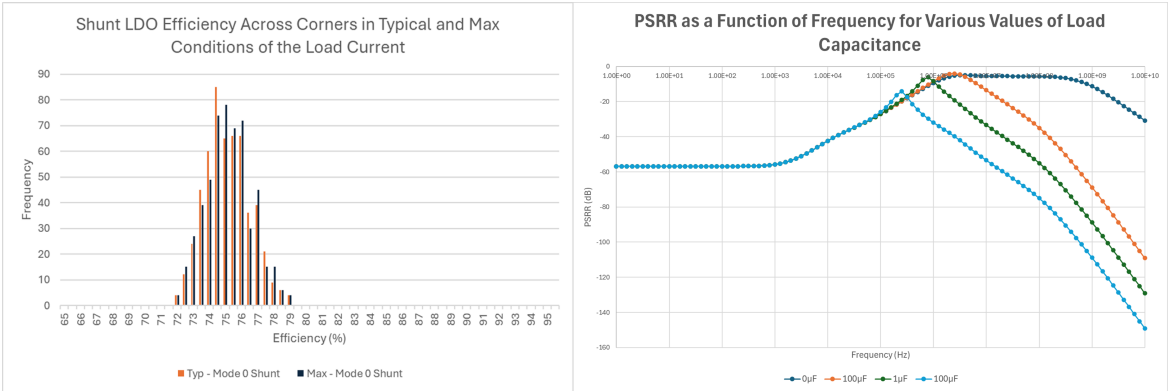

Figure 6. Efficiency and PSRR of the SLDO. Efficiency is measured across a range of PVT corners and operating conditions, with the results plotted as a histogram). PSRR is measured for various load conditions, broadly represented the range of loads that will be seen on the EIC-LAS.

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4 Conclusions

In this paper, we have presented a Shunt-LDO intended for use at the future Electron Ion Collider. Simulation results meet the required specifications. A first test structure has been submitted, and future publications will report on the results. Next steps in the broader design involve assembling a first version of the AncASIC and submitting a first prototype.

Acknowledgments

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