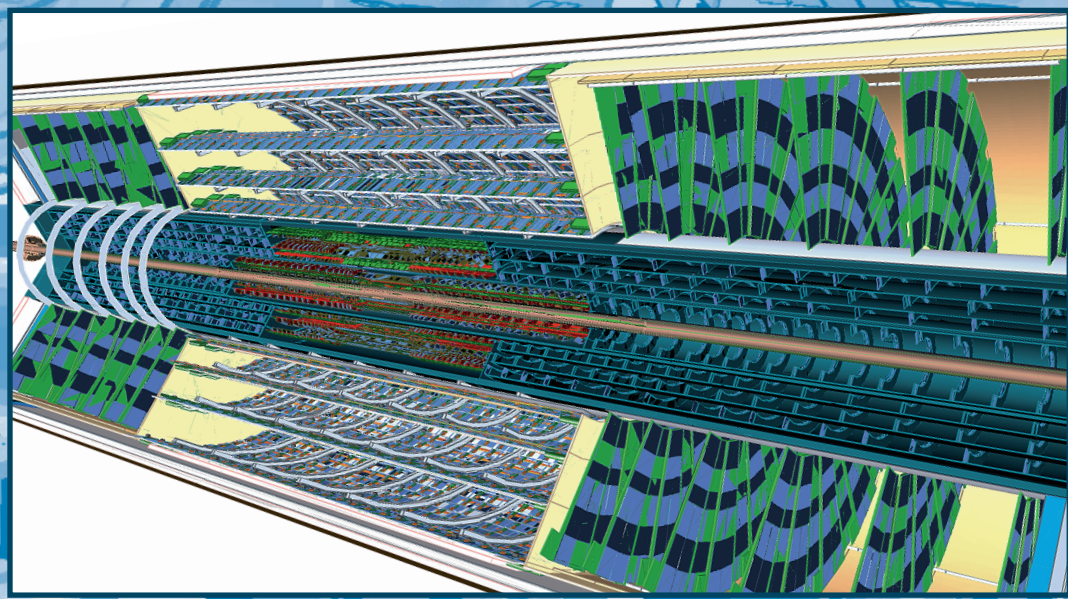
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ATLAS

Inner Tracker Strip Detector



Technical Design Report



Technical Design Report for the ATLAS Inner Tracker Strip Detector

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Abstract
This is the first of two Technical Design Report documents that describe the upgrade of the central tracking system for the ATLAS experiment for the operation at the High Luminosity LHC (HL-LHC) starting in the middle of 2026. At this time the LHC will have been upgraded to reach a peak instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1}, which corresponds to approximately 200 inelastic proton-proton collisions per beam crossing. The new Inner Tracker (ITk) will be operational for more than ten years, during which ATLAS aims to accumulate a total data set of 3,000 fb^{-1}. Meeting these requirements presents a unique challenge for the design of an all-silicon tracking system that consists of a pixel detector at small radius close to the beam line and a large-area strip tracking detector surrounding it. This document presents in detail the requirements of the new tracker, its layout and expected performance including the results of several benchmark physics studies at the highest numbers of collisions per beam crossing. The design, construction and expected performance of the large-area silicon-strip tracker are set out in detail. These include the results of measurements of prototype modules and associated support structures and the plans for their mass production. A short description is given of the state of the development of the pixel tracker, which will be presented in detail in the second Technical Design Report document one year from now. This document will also describe the management of the project, its schedule and major milestones. The costs of the new tracker and the collaboration that plans to build it are also presented.

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Executive Summary

This document constitutes the first of two Technical Design Reports that describe the upgrade of the central tracking system for the ATLAS experiment as part of the preparation for the operation at the High Luminosity LHC (HL-LHC) starting in the middle of 2026. The HL-LHC will operate at an ultimate peak instantaneous luminosity up to $\mathcal{L} = 7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ which corresponds to approximately 200 inelastic proton-proton collisions per beam crossing (pile-up). The new tracker (ITk) will be operational for more than 10 years and in that time ATLAS aims for a total data set of 3000 fb^{-1}. Meeting these requirements presents a unique challenge for the design of an all-silicon tracking system that consists of a pixel detector at small radius close to the beam line and a large area strip tracker surrounding it. The design of the ITk benefits from the enormous amount of experience gained over more than two decades in the construction and operation of the existing inner tracking detector which has been highly successful for the exploitation of LHC physics up to and well beyond its original design requirements.

Since the submission of the Phase-II Upgrade Letter of Intent [1], the layout of the tracker went through a process of optimisation for performance and cost. The trade-offs between performance and cost were reported in the 2015 Phase-II Upgrade Scoping Document [2]. The strip system, which is described in this document, has been reduced from an initial design of five barrel layers to four, the number of disks in the forward region has been decreased from seven to six and the so-called stub layer has been removed. The corresponding area of silicon sensors, at 165 m^2, still corresponds to 2.5 times that of the current Inner Detector silicon strip system. At the same time, the target acceptance has been extended to $\pm$ 4 units of pseudorapidity and the number of pixel layers, the outer radius of the pixel array and its corresponding area have all increased. The new detector layout results in a lower inactive material in the tracking volume (comprising less than one radiation length up to a pseudorapidity of 2.7) and gives a performance that is as good and in many cases better than the existing detector, but in a much more difficult tracking environment with up to an average of 200 proton-proton interactions per beam crossing. The ITk has been designed with efficient pattern recognition and track reconstruction in mind to give high track reconstruction efficiency and a low rate of fake tracks (even at HL-LHC pile-up levels). For muons with transverse momentum above 3 GeV this means greater than 99% efficiency; with efficiencies of greater than 85% for pions and electrons above 1 GeV out to a pseudorapidity of 2.7, while keeping fake rates below 1%. In addition, the performance is shown to be robust against a 10% loss of channels or modules that might occur as a worst case over the lifetime of the experiment.

The strip modules are single-sided with the hybrid circuits carrying the front-end microelectronics ASICs glued to the sensor surface. Modules are sandwiched on both sides of low mass carbon-fibre support structures with embedded bi-phase CO_2 cooling to $-35°C$. Each module consists of multiple rows of strips with a barrel pitch at 75.5 μm and that in the disks ranging from 69 μm to 85 μm. There are roughly 60 million electronics channels in the new strip tracker, nearly ten times that of the current strip system. The local support structures for the barrels are staves with 14 modules on each side while the disks are built from petals with 9 modules of different types per side. Sensor areas for all modules need to be compatible with production on 150 mm diameter high resistivity wafers.

The front-end electronics can be run in single trigger mode at 1 MHz or a split L0/L1 mode with latencies of up to 6 μs and 30 μs respectively. The ITk also provides the information required as input to a track trigger. Some of the details of the trigger systems are presented in this document and more will appear in the TDAQ Technical Design Report that will be presented in 2017.

The technologies and layout choices that underpin the silicon strip system described in this document are now particularly mature, they are largely unchanged since the submission of the Letter of Intent [1] and have benefited from the understanding that comes from more than ten years of development. The sensing elements are high resistivity n-in-p planar silicon strips which are required to withstand fluences at the HL-LHC of up to 1.2×10^{15} n_{eq}/cm^2 and a total ionising dose of up to 50 MRad (including a safety factor of 1.5). The strip sensor signals measured after these doses are 11,500 - 17,300 e^- at 500 V (and 14,000 - 19,500 e^- at 700 V). The electronics for the different lengths of strips (and hence different capacitive loads) has been shown to operate with noise occupancy at least an order of magnitude less than that due to hits on tracks at the thresholds required to retain a hit finding efficiency per layer of 99% after the corresponding doses for the different regions of the strip tracker. These results have been demonstrated in test-beam both with miniature and full-size prototypes irradiated to the required levels. Single event effects have also been studied in detail using the current generation of prototype electronics and not found to present problems at the expected doses.

The front-end architecture is based on the ATLAS Binary Chip (ABCStar) and Hybrid Controller Chip (HCCStar) following the design for the Inner Detector strip tracker. For prototyping, the designs were first ported to 250 nm and then more recently to 130 nm technologies. Although the front-end chip that is described in this document is not the production version, it gives good confidence that the required performance can be met. Considerable reductions in the amount of material inside the tracking volume have been achieved (< 2% per strip layer) with novel multiplexed powering (Low and High Voltage) and cooling choices. Low voltage is now delivered with either serial powering (Pixel Detector) or point-of-load DC-DC conversion (Strip Detector). Single HV lines now provide the bias voltage for multiple modules through HV multiplexing. The ITk takes advantage of a family of high bandwidth radiation hard optical transmitters that have been developed centrally for the LHC experiments.

Most of the R&D initiatives that were launched to demonstrate the feasibility of the ITk Strip Detector are now close to completion and very few choices of components remain for the final system. Large-scale, multi-module prototypes of the low-mass carbon-fibre local support structures with built-in cooling and bus-tapes demonstrate the required electrical and thermal performance, along with the associated construction. Detailed quality control and quality assurance procedures for production of all components have been developed and trialled. A production plan based on a combination of construction in geographically-clustered academic institutes and industry is well advanced and a schedule has been developed that is well matched to the requirements to have a detector ready for integration ahead of a one year testing period prior to installation.

In the last few years the ITk Strip community has also embarked upon a plan to study the feasibility of using low cost CMOS processes for the fabrication of silicon strip modules. Encouraging results with small-scale prototypes have been obtained after irradiations, but limited resources and time to develop this technology with sufficient confidence to produce a large area detector mean that it is unlikely to be used in the final production.

An ambitious plan of final part qualification with the final chip-set through pre-production (5% of the total detector) and radiation testing will follow the TDR. This will allow to place the orders for bulk production with a high degree of confidence. A market survey for the longest lead-time component, the silicon sensors, is in progress, jointly with CMS. The front-end electronics will be purchased using fixed-price frame contracts through CERN. Memoranda of Understanding should be possible with the completion of Market Surveys. Many of the smaller contracts will be negotiated and placed in the countries where the work will be done.

The ITk will be installed as a single monolithic unit into the centre of ATLAS. Particular care has been taken to reduce the time on the beam line and rapid connection techniques have been prototyped so that the detector can be ready for operation a few months after installation. It will be possible to replace the two innermost layers of the ITk Pixel Detector throughout the lifetime of the experiment. In designing the ITk, the aim has been to be able to reuse many of the existing services that are in place for the current Inner Detector. Many of the existing high and low voltage cables can be re-used over most of their length between the side-caverns and patch panels close to the detector. It will also be possible to reuse the cable cooling plant and the gas system which provides dry gas to the existing Inner Detector.

In developing the pre-production and production plans, particular detail has been given to ensuring the long term reliability of all components of the new detector. This has been matched with the preparation of a comprehensive risk mitigation strategy to help guarantee the required quality and performance at a reasonable cost.

In developing the specifications for the ITk, safety factors are used based on the experience gained in the construction and operation of the current detector. For example, a factor of only 1.5 is applied to the projected radiation fluences since these were very well predicted

for the current tracker. In many cases parts have been tested and qualified to well beyond the required limits.

In about one year from now the Technical Design Report for the ITk Pixel Detector will be released. A snapshot of the current progress detailing the active lines of R&D and the state-of-the-art are presented in this document.

The safe decommissioning and disposal of the existing tracking detector, the plans for the insertion and connection of the ITk are also presented in this document. The detailed plans for the removal of the existing detector will be summarised in a decommissioning report end of 2017 as part of the Pixel TDR.

At the end of the document the costs of the ITk Strip Detector and the plans for the period between the submissions of the TDRs to first physics in the middle of 2026 are presented. The management and internal organisation of the ITk, including its interaction with the rest of the experiment is discussed including the multi-level review process that is followed for all items in the project.

1 Introduction

Over the next decades the LHC will be the primary scientific tool devoted to studying the fundamental nature of matter at the energy frontier. Among the most important fundamental questions are:

- The origin of mass
- The nature of dark matter
- New forces and particles
- The nature of the quark-gluon plasma.

The LHC is the most advanced facility in the world for the investigation of the structure of matter at smallest scales and has already made substantial progress in addressing these questions. Since its start-up in 2010, the accelerator has delivered collisions at an increasing rate and at the highest energy ever reached in colliders: 13 TeV in the proton-proton centre-of-mass system. The analyses of the accumulated large data samples have given rise to more than 600 ATLAS publications so far.

In 2012, the successful operation of the LHC resulted in the discovery of a new particle, which was confirmed to be a Higgs boson [3, 4]. This discovery is a major step in our understanding of the universe and studies of the Higgs boson properties and decays provide new and unique insights into the fundamental structure of matter and the origin of mass. As the world's highest energy facility with an ambitious programme to greatly extend the statistical sensitivity to new physics, the LHC will be at the forefront of high energy physics for the next 20 years. This singular scientific potential is the reason that the full exploitation of the LHC (including its high luminosity upgrade) has been given the highest priority by the international high energy physics community as is stated, for example, in the European Strategy for Particle Physics as formulated by the European Strategy Group and adopted by CERN council in May 2013 [5]. Also the strategic plan for US particle physics developed by the Particle Physics Project Prioritisation Panel P5 [6] and presented in May 2014 identified the HL-LHC as its first high priority large-scale project. Recently, the HL-LHC was approved by the CERN council [7].

The scientific programme of the LHC spans over the next 20 years and includes an ambitious series of upgrades that will ultimately result in an accumulated integrated luminosity for proton-proton collisions of 3000 fb^{-1}. This represents an order of magnitude more data than what would be collected prior to the HL-LHC run. The improvements necessary to

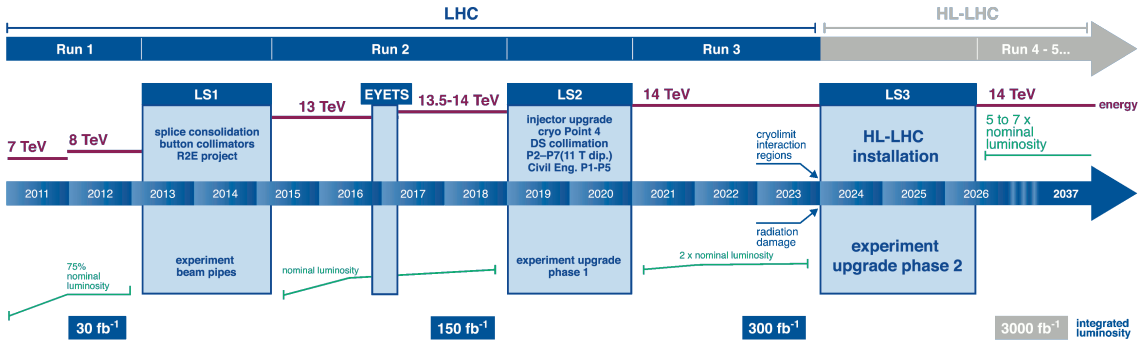


Figure 1.1: Updated status of the LHC baseline programme including the HL-LHC run.

achieve this accelerator performance will be mostly realised during two long shutdowns, each of two to three years duration (see Figure 1.1):

- in 2015, Long Shutdown 1 (LS1) was completed to prepare the accelerator for operation at 13 TeV and its design luminosity;
- for Long Shutdown 2 (LS2) in 2019/20 further improvements of the LHC are foreseen, accompanied by significant detector upgrades (Phase-I);
- Long Shutdown 3 (LS3) starting at the end of 2023 will include major performance upgrades of the accelerator for the high-luminosity phase (HL-LHC) which requires replacement of several major detector components (Phase-II).

With a nominal (ultimate) luminosity of $\mathcal{L} = 5 \times 10^{34}$ cm^{-2}s^{-1} ($\mathcal{L} = 7.5 \times 10^{34}$ cm^{-2}s^{-1}) and an average $\langle\mu\rangle$ = 140 (200) inelastic proton-proton collisions per beam-crossing (pile-up), the HL-LHC will present an extremely challenging environment to the ATLAS experiment, well beyond that for which it was designed. The quoted luminosities are "levelled" luminosities, i.e. the HL-LHC will be designed for a "virtual" peak luminosity limiting the event pileup while maximising the integrated luminosity. The anticipated increased luminosity, along with the associated data rate and accumulated radiation damage render the current ATLAS inner tracker inoperable. The ATLAS collaboration decided that it will replace the Inner Detector with a new all-silicon tracker to maintain tracking performance in this high-occupancy environment and to cope with the increase of approximately a factor of ten in the integrated radiation dose.

New technologies are used to ensure that the system can survive this harsh radiation environment and also to reduce the material, while the new read-out scheme allows the implementation of a track trigger contributing to the major improvements in the ATLAS online data selection (triggering) capabilities. The new tracker will consist of a greatly enlarged Pixel system extending to roughly twice the radius and four times the length of the current pixel array, coupled with a much more segmented strip detector requiring over three times the silicon area of the current detector to cover the full radius of the solenoid inner

bore. The radiation level will exceed 2×10^{16} n_{eq}/cm^2 and 1.7 GRad in the innermost pixel region. The ITk Strip Detector is exposed to more moderate levels of maximal 1.2×10^{15} n_{eq}/cm^2 and 50 MRad, but this is still a factor 10 more than expected for the current silicon strip tracker (SCT). These numbers are based on the calculated fluence and a safety factor of 1.5 was applied. The factor is determined from operational experience with the current detector which shows that the agreement of the expected effects on the detector elements due to radiation with the measured effects is better than 30%. Although a safety factor of 1.5 is assumed, irradiation tests routinely evaluate components up to twice the expected fluences to check there is no sudden degradation just beyond the specified fluence and dose limits. The technology choices and layout have been carefully optimised to maximise the physics reach in the challenging HL-LHC environment while respecting the constraints of the cost and construction schedule.

2 Motivation and Requirements of the ITk

The overarching aim of the replacement tracker is to deliver equal or better tracking performance, for physics objects of interest, to that provided by the current Inner Detector during the highly successful present data taking at the LHC. This needs to be achieved despite the much more severe operating conditions and in the presence of up to 200 superimposed minimum bias events (pile-up) in each beam crossing. This section summarises the requirements implicit in this approach that have been used to inform the design of the ITk. In Section 2.1 the deficiencies of the existing tracking system given HL-LHC conditions are discussed, while in Section 2.2 the requirements on tracking performance are described. Finally, Section 2.3 describes some more general constraints on the ITk Strip Detector system not specifically linked to its tracking capability.

2.1 Status and Deficiencies of Existing Detector

The current ATLAS Inner Tracking Detector was designed for 10 years of operation, at a constant instantaneous luminosity of $\mathcal{L}$ =1.0 $\times 10^{34}$ cm^{-2} s^{-1}, 14 TeV centre-of-mass energy, 25 ns between beam crossings and an average pile-up of 23 proton-proton interactions per crossing. The front-end architecture was designed around a single hardware trigger signal (Level-1) running at a peak rate of 100 kHz. The design of the detector (segmentation, space-point precision, material content and distribution, occupancy etc.) together with the choice of detector technology in the Inner Detector is well matched to these operating conditions and to meet the requirements of the ATLAS physics programme. In 2016 the LHC has exceeded the design parameters, the peak instantaneous luminosity was 1.37×10^{34} cm^{-2} s^{-1}, the peak pile-up at the start of a fill was typically 40, while the average pile-up was 24.2. Despite this much higher than anticipated pile-up, the Inner Detector performance (after upgrades to the pixel read-out) was adequate for the physics programme. The Inner Detector is playing a pivotal role in ATLAS physics analyses that rely on charged-particle reconstruction, heavy-flavour tagging, and on the identification of electrons, photons, muons and tau-leptons produced in both proton-proton interactions and heavy-ion collisions. The Inner Detector is not only used to reconstruct the trajectories of charged particles, it is also used in the identification of primary and secondary vertices; full reconstruction of exclusive decay modes, tracking of interactions and photon conversions; pile-up vertices and pile-up jet rejection; as well as particle identification through transition radiation and $\mathrm{d}E/\mathrm{d}x$. The Inner Detector is also used to improve jet energy measurements,

in the determination of isolation criteria and the measurement of the missing transverse energy $E_{\mathrm{T}}^{\mathrm{miss}}$. The detector elements of the Inner Detector were designed to withstand, with a reasonable margin, the radiation fluences associated with the integrated luminosity of $300\,\mathrm{fb}^{-1}$ anticipated during the running time before the Phase-II upgrade.

After the upgrade of the LHC machine and the ATLAS experiment with first physics data taking around the middle of 2026, 10 more years of operation are planned. The HL-LHC will be able to deliver very high peak instantaneous luminosities with 25 ns between crossings, but this will be levelled down to typically 5.0 - 7.5 $\times 10^{34}$ cm^{-2} s^{-1} in the detector. At the ultimate levelled luminosity, there will be an average of $\sim$200 proton-proton interactions per beam crossing. To cope with these extreme data rates, a major upgrade to the triggering capabilities of the experiment will be required with an extended role for tracking information anticipated in the final trigger architecture.

Initial operation at the HL-LHC is not anticipated to be at the ultimate luminosity. For early HL-LHC running conditions, it is therefore envisaged that a single-level hardware trigger could be adequate, but requiring a 1 MHz rate (Level-0) with a minimum latency of 6 μs, and designed to handle up to 10 μs. In this scenario, inputs for the hardware trigger do not include tracking information but, as part of the next stage, a fast hardware track finding capability would significantly enhance processing time and reduce costs.

However, the system must also be designed to be upgradeable to operating with two hardware trigger stages since the 1 MHz limit to the trigger rate may at the ultimate luminosity compromise the acceptance for purely hadronic final states. In this case, a fast hardware track finding capability is mandatory, as only tracking information can suppress backgrounds to bring a possible Level-0 trigger rate of a few MHz down to a Level-1 trigger rate somewhat below 1 MHz. Specifically for the ITk Strip Detector read-out, the requirements of compatibility with such a two-level trigger have pushed the L0 rate specification, added the need for further on-chip buffering and demand a regional read-out capability (where only a fraction of the strip tracker is read out at Level-0 corresponding to regions of interest identified by the external triggering system). Detailed data-rate requirements and the ability of the prototype on-detector microelectronics to accommodate these schemes are discussed in the appropriate sections.

The existing Inner Detector was not designed to meet the requirements for the Phase-II upgrade and cannot meet the very stringent requirements that will be part of the physics programme that goes with it. There are several compelling reasons, detailed below, why the existing Inner Detector has to be replaced.

Radiation Damage

The current Pixel detector was designed using radiation-hard sensors and electronics to withstand the radiation damage that is equivalent to an integrated luminosity of $400\,\mathrm{fb}^{-1}$. Similarly, the Semi-Conductor Tracker (SCT) was designed and constructed to operate up

to an integrated luminosity of 700 fb^{-1}, although after the insertion of the new innermost B-layer (IBL), increases in fluences due to additional services reduce the luminosity ceiling to that of the Pixel system in some areas of the SCT (end-caps). The IBL itself was designed for integrated luminosities equivalent to roughly 850 fb^{-1}. The specifications for radiation tolerance of the detectors in the current Inner Detector are sufficient to guarantee high efficiency for the integrated luminosity expected to be collected by the end of 2023, but they are not suitable for operation much beyond this level.

Above the design fluences, the intrinsic hit efficiencies drop below the limits required for efficient pattern recognition [1] and the leakage currents from the detectors will both exceed the limits of power supplies and (due to heating as a consequence of the increased leakage current) the capacity of the cooling system. The latter issues also affect on-detector power and cooling distribution.

Bandwidth Saturation

The front-end electronics of both the Pixel and SCT detectors employ zero suppression to minimise the data volume along the optical fibres. Both detectors can accommodate events with about 50 proton-proton interactions per crossing which come with sustained instantaneous luminosity of twice the design value or about 2 $\times 10^{34}$ cm^{-2} s^{-1}. As discussed in the Phase-II Letter of Intent, with 3 $\times 10^{34}$ cm^{-2} s^{-1} at 25 ns bunch crossing rate, limitations in the buffering of the links between the on-detector pixel module electronics (front-end chips) and the read-out driver (ROD) will lead to inefficiencies when the limit of more than 0.2 to 0.4 hits per double column per 25 ns bunch crossing is exceeded. A similar limitation occurs in the SCT at about the same value of instantaneous luminosity where the optical links between the front-end ABCD chip and the RODs will saturate resulting in the loss of data. For an average number of superimposed minimum bias events in each beam crossing (pile-up) of $\langle\mu\rangle$ = 70 at a Level-1 rate of 100 kHz, much of the innermost strip barrel cannot be read out.

Limitations from Detector Occupancy

With $\langle\mu\rangle$=$\sim$200 average proton-proton interactions inside the current detector, the confusion due to additional hits without the compensating increase in granularity, will compromise the efficiency of the pattern recognition and track-finding efficiency. The rate of fake tracks would also increase sharply. It would be difficult to resolve nearby particles inside the SCT, while the TRT occupancy would approach 100 %. The inability of the current Inner Detector to resolve nearby tracks, for example in boosted top-quark jets, would also significantly compromise the physics reach in the HL-LHC era.

Track Trigger

The performance of the trigger system will be one of the main challenges in ATLAS at HL-LHC. The current Inner Detector does not provide any tracking information to the existing first level (L1) hardware trigger system. It was shown in the LoI [1] that by adding tracking information to the trigger objects provided by the calorimeters and muon system, trigger thresholds could be lowered which directly benefits the physics performance. Since then, more detailed studies have shown that sufficient quality tracking information could be provided as input to a hardware trigger using just the strip layers of the proposed new tracking detector together with the outermost pixel layer.

These very substantial limitations, necessitate the complete replacement of the Inner Detector for the Phase-II upgrade of the experiment.

2.2 Performance Requirements of the ITk

The performance requirements that are used as input to the design of the ITk are driven by the needs of the Phase-II physics programme as outlined in the Phase-II LoI and discussed in more detail in dedicated technical reports [8,9]. As stated above, the general requirement for the ITk is to deliver equal or better tracking performance to that provided by the current ATLAS Inner Detector despite an average pile-up ($\langle\mu\rangle$) of up to 200 events. The key features of the physics programme and the reliance on tracking are presented in Chapter 4.

2.2.1 General Conditions

The new tracking detector is designed for 10 years of operation at instantaneous luminosities of 7.5×10^{34} cm^{-2}s^{-1} (after levelling), 25 ns between bunch crossings and an integrated luminosity of 3,000 fb^{-1}. All performance requirements described below must be met for average pile-up scenarios up to $< \mu >= 200$.

The shape of the luminous region is not finalised yet: it may be either Gaussian with a sigma of 5 cm, or having a more complex "flat top" distribution if this can be delivered by the HL-LHC final focus system. To accommodate any choice, a full detector coverage (hermeticity) for each layer must be provided for all tracks with transverse momenta above 1 GeV originating from a cylinder around the nominal centre of the ITk with radius of 2 mm and length of $\pm$ 150 mm along the beam direction. It is also required that beyond this longitudinal region there is no very abrupt reduction in the tracking performance.

The current solenoid magnet will remain in the detector and provide a magnetic field intensity of 2 T.

Tracks from the primary vertex need to be reconstructed up to a pseudorapidity (η) of 4.0. This will be achieved through a system of silicon barrel layers and disks (Strips) or rings (Pixels) with the possibility of inclined pixel modules to better cover the transition from the barrel to the end-cap regions. For the current Inner Detector at full radius, the barrel only components cover up to $|\eta| = 0.6$, although the barrel silicon strip system (with outer radius at 514 mm) extends to $|\eta| = 1.2$. The ITk is designed with a barrel region out to its full radius that covers $\eta \simeq \pm 1$, which then matches the barrel muon system giving the upgraded ATLAS inner tracker an extended central coverage without transition regions (the barrel calorimeters also extend beyond this η range). The current Inner Detector acceptance stops at $|\eta| = 2.7$ just beyond the full extent of the EM and muon trigger systems. In the following, the initial focus will be on tracking requirements up to $|\eta| = 2.7$ where these are set by the need to match or improve the performance of the current Inner Detector. Separate considerations apply for the very forward region (beyond $|\eta| = 2.7$) as the weak magnetic field does not allow similar performance in momentum reconstruction but track finding is nevertheless of significant importance to the HL-LHC physics programme.

The tracking detector design also has to be robust in the sense that its performance is not significantly deteriorated in the presence of 10% dead channels randomly distributed in the detector and 10% of structural (correlated) failure of individual components.

2.2.2 Track Reconstruction Efficiency

Table 2.1 shows the required efficiency to reconstruct different particle types, within the pseudorapidity range of $|\eta| < 2.7$ under all pile-up and system-failure conditions, based on the performance of the current Inner Detector. Muons define the optimal track reconstruction efficiency as they are minimum ionising particles that do not undergo nuclear interactions with the detector material and because of their high mass, muons do not radiate as much energy as electrons. For particles that interact more strongly with the detector material, such as charged hadrons and electrons, it must be possible to reconstruct those originating from within a transverse window of ± 2 mm around the interaction region. The reconstruction efficiency should be uniform in ϕ to within the systematic uncertainty coming from limited modelling of inhomogeneities in the detector material (assumed globally to be within 5%).

The new tracking detector must be able to have a good two-track separation resolution to measure tracks in the core of high-energy jets with high efficiency. The average track-reconstruction inefficiency for primary hadrons within jets should not increase by more than 1% from low jet p_T to jets with $p_T = 1$ TeV. The track-reconstruction efficiency within a jet should not decrease by more than 5 (10%) when moving from outer jet regions towards the jet axis for light (b-)jets [10]. Similar reconstruction efficiency must be achievable for hadrons from B-hadron decays within the innermost detection layer (assumed at 39 mm). It also should be possible to reconstruct electrons from photon conversions up to a radius of about 30 cm, which allows the study of the material distribution within the Pixel system.

Table 2.1: The target track finding efficiencies for different prompt particle types in limited ranges of pseudorapidity, even at the simulated worst case detector failures discussed in the text and p_T.

Particle	p_T **range**	**Required Efficiency**	
		$\|\eta\| \leq 1.0$	$1.0 < \|\eta\| < 2.7$
Muon	$p_T > 3$ GeV	$> 99\%$	$> 99\%$
Pion	$p_T > 1$ GeV	$> 90\%$	$> 85\%$
Electron	$p_T > 5$ GeV	$> 90\%$	$> 85\%$

With high pile-up, the rate of tracks which are poorly reconstructed due to one or more incorrectly associated hits needs to be controlled. The track selection (in particular increasing the requirement on the number of hits and rejecting candidates with too many missing hits in active sensors, so-called holes) has been shown to be the most effective handle for avoiding incorrectly or poorly reconstructed tracks. At the same time this needs to be balanced with the small inefficiency due to material interactions in the tracking layers and the impact of possible efficiency losses due to component failures after irradiation. To keep the additional number of tracks per generated stable particle below 1% on average and below 3% locally, the fake contribution has to be tightly controlled. This has to be achieved for all pile-up conditions, integrated over the pseudorapidity range of $|\eta| < 2.7$, while preserving the track reconstruction efficiencies specified in Table 2.1.

2.2.3 Track Resolution

In the following, the resolution of a track parameter X is expressed as a function of p_T using

$$\sigma_X(p_T) = \sigma_X(\infty)[1 \oplus \frac{P_X}{p_T}] \tag{2.1}$$

where P_X is a constant that represents the value of transverse momentum for which the intrinsic and multiple scattering terms are equal for the parameter X under consideration. A list of the performance requirements are given in Table 2.2 for the pseudorapidity range $|\eta| < 2.7$. In order to avoid contamination from falsely identified high momentum tracks, the fraction of tracks with an estimated transverse momentum $|p_T^{reco} - p_T^{true}|/p_T^{true} > 0.5$ should not exceed a rate of 1% over the entire detector coverage for particles following the p_T-spectrum of the underlying min bias events. The rate of charge misidentification should also be smaller than 0.5% for muons with $p_T = 500$ GeV and not exceed 10% at $p_T = 2$ TeV.

The track extrapolation to the calorimeter must have spatial resolution better than that of the fitted energy-deposit cluster centroid. The accuracy of the reconstructed centroid of electromagnetic calorimeter clusters depends on both their energy and the rapidity of the cluster. Table 2.3 shows the required track extrapolation accuracy at the entry point of the

Table 2.2: Required ITk track parameter resolutions (RMS) at a pile-up of 200. (See text for explanation of terms in the table.)

Track Parameter	**Units**	$\lvert\eta\rvert$ Range if reduced
Inverse transverse momentum		
$\sigma_(q/p_T)(\infty)$	TeV^{-1}	< 0.3 ($\lvert\eta\rvert < 2$)
$\sigma_(q/p_T)$ ($p_T = 10$ GeV)	TeV^{-1}	< 0.15 ($\lvert\eta\rvert < 2$)
$\sigma_(q/p_T)$ ($p_T = 1$ GeV)	TeV^{-1}	< 0.15 ($\lvert\eta\rvert < 2$)
Transverse impact parameter		
σ_{d_0} (∞)	μm	< 8 ($\lvert\eta\rvert < 0.5$)
σ_{d_0} ($p_T = 1$ GeV)	μm	< 100 ($\lvert\eta\rvert < 0.5$)
Longitudinal impact parameter		
σ_{z_0} (∞)	μm	< 50 ($\lvert\eta\rvert < 0.5$)
σ_{z_0} ($p_T = 1$ GeV)	μm	<100 ($\lvert\eta\rvert < 0.5$)

Table 2.3: The achievable precision for reconstructing the centroid of electromagnetic clusters using track extrapolation.

Accuracy of centroid position	$\lvert\eta\rvert = 0$	$\lvert\eta\rvert \sim 2.5$
$\sigma(\lvert\eta\rvert)$	0.2×10^{-3}	0.35×10^{-3}
$\sigma(\phi(\text{rad}))$	0.4×10^{-3}	0.7×10^{-3}

calorimeter for particles (electrons, muons and taus) to be able to match the calorimeter spatial resolution sufficiently for high efficiency in particle-flow algorithms.

2.2.4 Vertex Reconstruction, b-Tagging and Converted Photons

With 200 pile-up events, the mean separation of primary vertices is typically less than 1 mm. It is therefore not possible for all vertices in a triggered event to be reconstructed individually. However, it is important that high transverse momentum objects (muons, electrons and tracks in high transverse energy jets) coming from a common vertex can all be correctly associated to the same vertex with good efficiency. Vertex reconstruction in such an environment poses stringent requirements on the tracking resolution close to the interaction point and imposes the need to minimise the amount of material of the inner layers of the Pixel detector. This requirement corresponds, in the case of $t\bar{t}$ events, to the probability of the $t\bar{t}$ vertex being among the reconstructed vertices having to be greater than 0.95. In addition, the probability that the $t\bar{t}$ decay is associated to the correct reconstructed vertex should be greater than 0.90.

The $R\phi$ and z granularity of the innermost Pixel layers must be optimised for light-jet rejection in the jet p_T range around 150 GeV. The Strip layout should be optimised to minimise

the hit sharing in the core of dense jets. The performance of the b-tagging versus light-jet rejection in the presence of 200 pile-up events should be optimised for each layout and should match the performance of the current detector (including IBL) in the presence of 200 pile-up events.

Correctly identifying photon conversions is primarily of importance for maximising the acceptance for events with photons in the final state, particularly where, even at the HL-LHC, final data selections will be statistics limited (for example $HH \rightarrow b\bar{b}b\bar{b}$). It is also required for material distribution studies and helps to increase the measurement accuracy of e/γ objects when applying the correct photon, electron or conversion calibration. Electrons from photon conversions need to be reconstructable with good efficiency for radii below 30 cm.

2.2.5 Large Eta

A wide range of physics analyses of particular relevance to the HL-LHC physics programme, for example vector boson fusion (VBF), require track reconstruction beyond the $\eta = \pm 2.7$ of the current Inner Detector. Extending the coverage to either $\eta = \pm 3.2$ (the "Middle" scenario) or $\eta = \pm 4.0$ (the "Reference" scenario) was discussed in detail in the ATLAS Phase-II Upgrade Scoping Document [2]. The studies presented there show that apart from the increased physics acceptance, forward jet reconstruction, $E_{\mathrm{T}}^{\mathrm{miss}}$ resolution and pile-up jet rejection all benefit significantly from extending tracking coverage out to $\eta = \pm 4.0$.

The solenoid field diminishes along the z-axis, particularly at low radius, leading to poorer p_T resolution. Also the longitudinal impact parameter in the z-direction, needed to correctly assign tracks to vertices, worsens with respect to the ~ 50 μm typically required for high momentum at low $|\eta|$. However, even longitudinal resolution values of the order of the typical (mm) primary vertex separation at $< \mu >= 200$ out to $\eta = \pm 4$, provide significant discrimination in pile-up event jet rejection and $E_{\mathrm{T}}^{\mathrm{miss}}$ studies, as well as allowing very forward high p_T isolated tracks to be assigned with good confidence to correct primary vertices.

To achieve the performance discussed in Chapter 4 and in Ref. [2], a track efficiency of >80% for $t\bar{t}$ events is required over the full $|\eta|$ range, even with 200 pile-up events. With tracking extending to $|\eta| = 4$, the simulated pile-up jet rejection is 50 (with a hard scatter efficiency of 70%). Compared with tracking only to $|\eta| = 2$, this improves the acceptance for the VBF channel $H \rightarrow WW \rightarrow l\nu l\nu$ by a factor of two for a constant background [11]. This and other examples of the enhanced physics reach with coverage to $\eta = \pm 4$ are presented in Chapter 4.

Since this extended coverage is achieved through adding further Pixel rings (see Chapter 15), more details on how this will be technically realised will also be included in the Pixel TDR.

2.3 Further Strip Detector Specific Requirements

2.3.1 Assembly

The envelope of the ITk in its installation cradle is 2.4 m wide, 3.2 m high and 7.5 m long. On the outer side, the ITk radius takes into account the radius of the cryostat bore. On the inner side, the ITk must respect the beam-pipe envelope along its length including necessary clearances and the possible need for insulation during the bake-out.

The last strip layer is placed as close as possible to the ITk maximum radius as this maximizes the lever arm and thus the momentum resolution, and it reduces the extrapolation distance between the last measurement point in the tracking detector and the calorimeter shower for electrons.

The ITk with all its sub-systems will be assembled and commissioned on the surface and installed as a single unit into the LAr cryostat. It has to be completed with enough time to allow one full year of commissioning/testing in one of the surface buildings at Point-1 before the detector is scheduled for installation in the underground cavern. During commissioning/testing on the surface, disassembly to repair or replace any broken modules must be possible.

The fully assembled Inner Detector, with all the necessary services must be possible to lower and install during a "Large Opening" configuration passing between the end-cap calorimeter and central toroid system.

For the ITk Strip Detector, existing cables should be used wherever possible to reduce cost and installation time. Certainly the SCT "Type IV" cables bringing power to the Patch Panel 3 (PP3) should be reused, as well as possibly the "Type III" cables which run from PP3, through the muon spectrometer, to the PP2 region on the outside of the barrel calorimeter cryostat.

After installation and operation, the beam-pipe and the inner two pixel layers must be removable without disturbing the rest of the ITk. Circumstances could arise where removal of only one of these two components is desirable. Although not a requirement, designs enabling this are to be preferred. Designs must ensure that such operations can be completed, consistent with minimising radiation doses for workers, over the full duration of the experiment within a standard long shutdown period.

In certain fault conditions it is possible for the bi-phase CO_2 coolant temperature to drop as low as $-55°C$. Humidity within the ITk volume must therefore be regulated through flushing with dry N_2 gas to keep a dew point temperature at or below $-60°C$.

2.3.2 Performance

The integrated luminosity implies radiation requirements for all components at all radii to be compatible with the tracking performance listed above up to the end of HL-LHC running. From the total ionising dose (TID) and displacement damage to the bulk (measured in 1 MeV equivalent neutron fluence) using the expectations shown in Figure 3.9 a safety factor of 1.5 is applied to understand the strip and ASIC radiation hardness requirements. For the ITk Strip Detector this means adequate performance is required up to $1.5 \times 8.1 \times 10^{14}$ $n_{\text{eq}}\text{cm}^2$ ($= 12.2 \times 10^{14}$ $n_{\text{eq}}\text{cm}^2$) and a TID of 1.5×33.3 MRad($= 50$ MRad). For all materials used in the tracking detector volume which are not radiation qualified or well characterised, more stringent requirements are typically imposed. In the case of items where lot to lot variation in composition cannot be excluded, this safety factor should be multiplied by a further factor of 4 on top, resulting in the need to test to a factor 6 above the central value of the predicted dose. For the ITk Strip Detector, the high peak luminosity translates into requirements in terms of bandwidth that depend in detail on the trigger scheme. To avoid data losses, it is required for the Strip Detector that no link occupancy exceeds 90% for either a single-level trigger system with an average rate of 1 MHz or for a dual level system with up to 4 MHz L0 and 600 kHz L1. This assumes no more than 10% of the strip tracker is required for the regional read-out input to L1. Buffering is required for L0/single level for up to 6 μs while in the dual level scheme, the L0+L1 latency target is $\sim$25 μs. The electronics must be designed to be able to accommodate either trigger scheme.

In order to control the global and local fake rates, the levels of hit occupancy in the layers should be kept low. Any failures to reach these low levels require simulation validation to ensure that this does not significantly compromise the detector performance. Previous studies [1] indicate that a level of maximum 0.1% occupancy in the pixel layers and 1% occupancy in the strip layers leads to very efficient and stable pattern recognition. Noise occupancy of the ITk Pixel and Strip Detectors, even after exposure to lifetime irradiation, should be at least one and preferably two orders of magnitude less than the occupancy due to hits on tracks. This needs to be true at the thresholds required to retain the hit-finding efficiency per layer at 99%.

Tracking-reconstruction efficiency and minimisation of multiple scattering effects require a low material budget. For the ITk, generally it is required to be in total <1 X_0 up to $\eta = 2.7$, which is achieved with a target average strip material of below 2% of a radiation length per layer.

2.3.3 Alignment

The ITk Detector will use a track based alignment strategy that has been successful in the ATLAS Inner Detector [12]. The strategy is hierarchical in nature starting with the largest macro structures proceeding to local supports and finally modules. Constants for the macro

structures will eventually be determined on a daily basis. The constants for the modules will be determined less frequently and it is important to start with a good knowledge of their positions inside the local supports.

The support structure needs to provide stability on the time scale needed for a software alignment cycle. This drives the requirements for the performance of the support structures.

Even though the main alignment will be achieved using tracks from collisions, it is still required to have adequate metrology at the module and local support level as well as sufficient time to perform a cosmic-tracks-based alignment for the full ITk Detector after surface assembly. The latter will also allow checks of efficiencies and correct connectivity for all sub-components.

3 Overview of ITk Layout

The ITk Detector layout has been developed to meet the requirements discussed in Chapter 2 for pile-up values of up to an average of 200 interactions per bunch crossing. Several layouts were considered and studied in detail. The evolution of these layouts and the convergence to the layout option is presented in this document. As part of this process, the realism of the description of the detector in Geant4 has improved enormously, and the pattern recognition and track reconstruction have been optimised. Several of the necessary studies were carried out using fast simulation to estimate the consequences of the layout changes on tracking performance. Later, full simulation was used to cross-check the results by generating and simulating events with pile-up.

3.1 Evolution of the ITk Layout

The ITk layout as presented in the Letter of Intent (LoI) was guided by the requirement of at least 14 hits and a coverage of up to $|\eta| \sim$2.7 [1]. In Figure 3.1 the Pixel Detector is shown in red with four barrel layers in the central region and six disks in the forward region. The Strip Detector is shown in blue with five barrel layers and seven disks. Horizontal and vertical lines represent barrel and end-cap layers, respectively. The LoI layout featured a so-called "stub" layer, a short barrel layer between the fourth and fifth layer of the Strip Detector, to give robustness in the barrel to end-cap transition region around $|\eta|$=1.1.

The next important step in the evolution of the ITk layout was the LoI-Very Forward (LoI-VF) layout (see Figure 3.2) as presented in the Scoping Document [2]. In this context a layout with an extended tracking acceptance up to $|\eta| \sim 4$ was studied. The LoI-VF layout was not optimised in terms of mechanical construction and maximum performance for a given silicon area. This layout can be considered as the starting point to develop more realistic candidate layouts for the ITk Detector.

Since the Scoping Document, the layout of the ITk Detector has been optimised with a focus on tracking performance, cost effectiveness, ease of construction and installation, as well as the ability to operate the detector up to the end of the HL-LHC operation. Two options to extend the Pixel Detector coverage up to $\eta = 4$ have been implemented, named Inclined and Extended (see Section 3.1.5), replacing the LoI-VF layout concept as presented in [2].

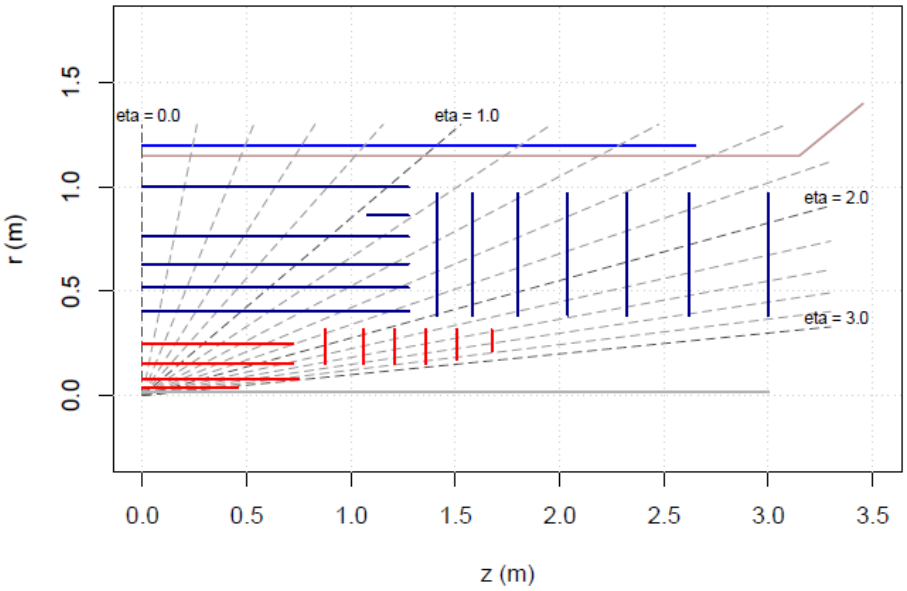


Figure 3.1: A cross-section of the ATLAS ITk tracker presented in the LoI showing the coverage of the Pixel Detector in red and Strip Detector in blue. The rapidity coverage extends up to $|\eta| = 2.7$ and is matched to the coverage of the Muon Spectrometer. The blue line outside the ITk volume represents the coil of the solenoid magnet.

3.1.1 Number of Pixel and Strip Layers

One of the most significant changes was the move from a layout with four pixel layers and five strip layers (4P 5S) to a layout with five pixel layers and four strip layers (5P 4S). This change was mainly driven by the overall tracking performance, optimising in particular the ability to resolve close-by tracks (double-track resolution).

Important physics goals for the HL-LHC involve processes with high-p_T jets or τs. Limits on the double-track resolution arising from channel size and sensor thickness result in significant rates of cluster merging that is observed in the innermost layers. A comparison of the τ reconstruction efficiency in the 3-prong decay channel as a function of the τ momentum is shown in Figure 3.3 for different cluster splitting scenarios. Cluster splitting is a technique to identify clusters created by multiple charged particles in the Pixel Detector, using neural networks which rely on analogue readout information. This has not yet been fully implemented in simulation for the new detector, therefore the study is made with a version of the ITk layout simulation that emulates the effect of the cluster splitting [13]. In Figure 3.3, the significant tracking efficiency improvements observed when increasing the number of pixel barrel layers in which cluster splitting technique is allowed from two (1,2) to four (1,2,3,4) imply a significant rate of cluster merging in the first four layers. The small additional improvement observed when applying this technique on five layers (1,2,3,4,5)

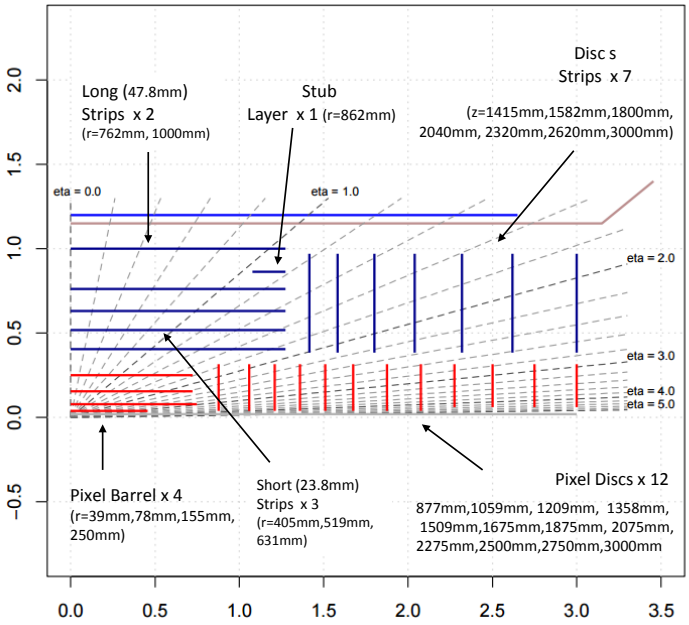


Figure 3.2: A cross-section of the LoI-VF layout from the Scoping Document. The pseudorapidity coverage extends up to $|\eta| = 4.0$. Blue and red lines represent strip and pixel layers, respectively. Horizontal and vertical lines represent barrel and end-cap layers, respectively. Lines of constant pseudorapidity are indicated. The blue line outside the ITk volume represents the coil of the solenoid magnet.

compared to four illustrates that with five layers there is sufficient redundancy in the Pixel Detector to correctly resolve these topologies in the presence of double-track resolution effects. The remaining efficiency losses at high-p_T illustrate double-track separation issues in the Strip Detector which become the limiting factor.

These studies demonstrate that the new layouts with five Pixel and four Strip layers allow for a better double-track separation in dense tracking environments and for lower fake rates at high object reconstruction efficiencies in the presence of pileup. With the new layer setup the overall hit count in the ITk barrel went from 14 to 13, replacing one strip layer (two hits) in favour of a high granularity pixel layer. The layout with five pixel layers also shows a much improved behaviour in the efficiency/fake balance at $\langle\mu\rangle$=200. The new layout preserves the redundancy necessary to ensure that the detector performance is not compromised in the presence of realistic detector defects.

3.1.2 Barrel – End-cap Transition Region of the Strip Detector

Most of the interesting physics measurements at the LHC involve s-channel processes that lead predominantly to high-p_T objects in the central part of the detector. The transition between the barrel and the end-cap is in this respect problematic, as in the transition region

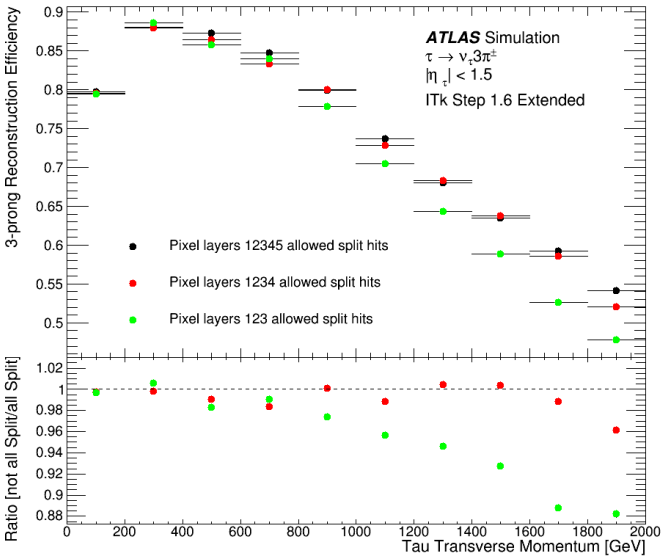


Figure 3.3: Tau reconstruction performance versus τ momentum in the 3-prong decay channel. Different cluster splitting scenarios are shown. L12 denotes cluster splitting in the two innermost layers, L123 in the inner three and so on.

one not only reduces the measured track length, resulting in a poorer momentum resolution, but one also has fewer hits and therefore less robustness for tracking. The LoI layout includes an additional stub layer to improve robustness in the barrel/end-cap transition region. As the ITk layout has evolved, the stub was removed from the layout to reduce the engineering complexity of the Strip Detector. Preference was given to maximally extending the central region, where the tracking performance is best and hence using the longer barrel staves. This moves the barrel/end-cap gap to 1.1 in $|\eta|$.

A further optimisation with respect to the LoI layout allowed the removal of one end-cap disk that would otherwise have been needed to maximise the track length in the end-cap region. The positions of the remaining six disks were adjusted accordingly to provide good momentum resolution over the complete η-range.

3.1.3 Barrel – End-cap Transition Region of the Pixel Detector

There are strong limitations on the momentum resolution above $|\eta| = 2.7$ due to the length of the solenoid coil and the shorter transverse lever arm at increasing pseudorapidity. However, as discussed in Chapter 2.2.5, recent studies have shown there is nevertheless a strong physics case (see Chapter 4.6) to expand the tracker coverage up to $|\eta| = 4$.

The overall physics performance of the ITk Detector requires that the extension to higher η must not harm the tracking performance in the central region, e.g. due to a more complex barrel/forward transition region in the Pixel Detector. Novel stave concepts are needed

to ensure both an excellent central performance as well an extended tracking η coverage. Designing the innermost barrel layer structure to cover the full η-range ensures the presence of a measurement as close as possible to the beam pipe. It also minimises the passive material crossed by particles before the first two measurements in the forward region of the detector, as well as optimises the extrapolation distance between these two measurements. In contrast, in a shorter inner barrel design with services routed along the barrel staves and then radially outward, a larger amount of material from services is crossed by forward particles at the end of stave before the first measurement or between the first two measurement. Moving the transition between the barrel and the end-cap to higher η optimises the tracking the tracking efficiency and the impact parameter resolution in the forward region of the detector.

3.1.4 Pixel End-cap Ring System

In the LoI-VF Layout the coverage up to $|\eta| = 4$ was provided by a forward pixel system comprising 12 disks. No detailed mechanical design or service routing considerations were taken into account in this 'proof of principle' implementation, which resulted in an average of 20 available hits at $|\eta| \sim 2$, a large silicon surface, and would imply a correspondingly large number of Pixel modules to instrument the disks. In order to mitigate such effects, a new end-cap concept based on rings of sensors in place of disks was developed. The sensor placement with the ring concept has much greater flexibility than with disks, allowing a more even distribution of hits on track, and a reduction of the required silicon area. The ring positions in z can also be easily adapted to the coverage needs of different barrel layouts. The ring system additionally offers advantages for pixel service routing, by allowing pixel service material to be routed out between the rings.

3.1.5 Choice of the Pixel Layout

Since the Scoping Document a number of different layouts for the Pixel Detector were studied, most of which are based on innovative pixel stave concepts to extend η coverage. The best results were achieved with two layout candidates named Inclined and Extended. Both layouts are based on long barrel staves to push the material of the end of barrel services and support region to large z. For both layouts the inner pixel barrel layer covers the full η range.

The main differences between the concepts is the inclination of the sensors in the forward part of the barrel layers for the Inclined layout. This allows the material transversed by particles at large η to be minimised and at the same time requires less silicon surface to cover the full η range. In addition, these inclined sensors provide two or more hits in the first layer, providing redundancy for the local track finding close to the interaction point even at large pseudorapidity. In the Extended layout, all barrel sensors are placed horizontally with respect to the beam line in a more classical arrangement that requires more

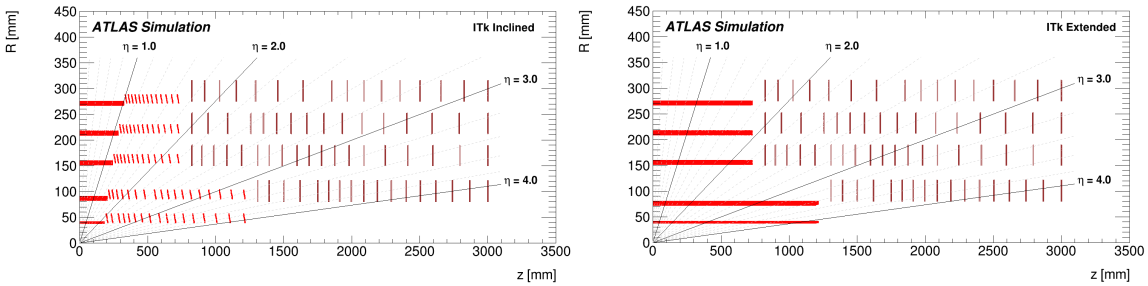


Figure 3.4: Diagrams showing simulated energy deposits in active layers for the two candidate layouts zoomed in on the Pixel barrel. **Left:** The Inclined layout. **Right:** The Extended layout.

silicon, but uses a simpler stave concept. In this case, more material is seen by particles traversing the layer at large η, while producing long clusters or mini-tracklets in the sensor. The properties of these long clusters can be used to determine their compatibility with the initial particle trajectory estimate. Based on the detailed studies done so far, the Inclined layout is chosen as baseline presented in this document. The main reasons for this choice are:

- In the Inclined stave concept the material transversed by particles close to the interaction region in the very forward region is minimised. This provides better impact parameter resolution for particles within the p_T-range relevant for jet vertex tagging.
- Multiple hits on a track in the first layer close to the interaction region facilitates robust track finding and thus improves the tracking efficiency for primaries and fake rates.
- With an Inclined inner pixel barrel system with more hits, it is possible to reduce the complexity of the Pixel Detector end-cap ring system, significantly reducing the amount of needed pixel surface to achieve the necessary hit coverage. At the same time, the inclining sensors on the barrel staves allows to cover the same η range as with Extended barrel staves with less silicon surface.

Furthermore, due the reduced total Pixel Detector surface the total service material for the ITk in front of the forward calorimeters is reduced. With the reduction in the total material in the Inclined stave layout, the effects due to secondaries from hadronic showers and conversion are reduced as well.

3.2 The ITk Layout

In the central region of the ITk Detector, sensors are arranged in cylinders around the beam axis, with (starting from inside) five pixel layers followed by two short-strip layers of paired stereo modules then two long-strip layers of paired stereo modules. The forward regions will be covered by six strip disks and a number of pixel rings leading to one or more hits

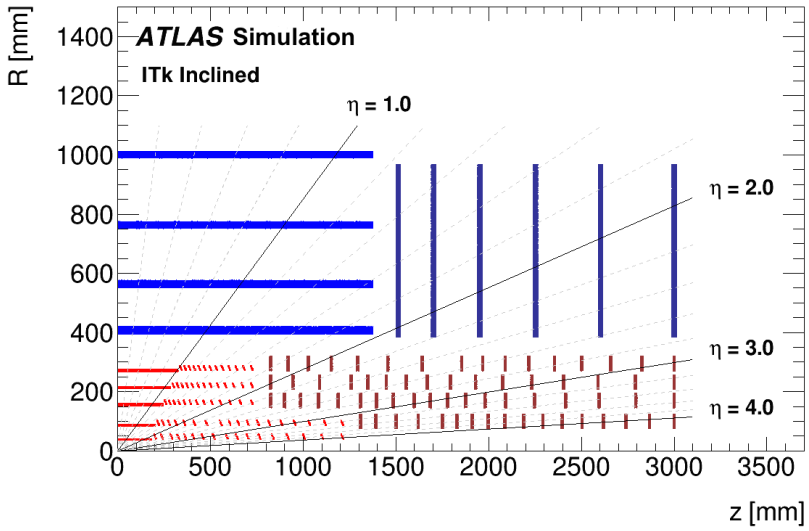


Figure 3.5: Schematic layout of the ITk for the HL-LHC phase of ATLAS. Here only one quadrant and only active detector elements are shown. The horizontal axis is the axis along the beam line with zero being the interaction point. The vertical axis is the radius measured from the IP. The outer radius is set by the bore of the solenoid.

depending on the ring layer and η position. The pixel layout will be presented in detail in Section 3.2.2.

The tracking detector is surrounded by a polyethylene moderator to moderate neutrons. This decreases the 1 MeV neutron equivalent silicon damage fluence arising from the flux of neutrons entering from the calorimeters. Gaps will be preserved between sub-detector parts to allow for supports, services, and insertion clearances.

3.2.1 Layout of the ITk Strip Detector

The ITk Strip Detector consists of a four-layer barrel section and one end-cap on each side with six disks each to provide good coverage to within 10° of the beam axis. The strip system covers $\pm$ 2.7 units of rapidity (see Figure 3.5). The strip barrel extends from -1400 mm to +1400 mm along the z-axis. The radii at which the barrel layers are located and the z-positions of the end-cap disks are chosen to optimise the number of hits on a track and the p_T-resolution. An overview of the geometry with the location of the sensing elements in the strip barrel section is given in Table 3.1. The two inner layers of the barrel are equipped with short strips of 24.1 mm length. The two outer layers have longer strips with 48.2 mm. All strips in the barrel section have a pitch of 75.5 μm.

The strips in the end-cap are radially distributed and pointing to the centre of the beam-axis. The strip lengths in the end-caps are optimised to keep the strip occupancy below 1%, resulting in varying strip lengths increasing from 19.0 mm in the region closest to the

Table 3.1: Layout parameters for the ITk Strip Detector barrel. Each strip barrel layer is 2.8 m long extending from -1400 mm to +1400 mm along the z-axis.

Layer	**Radius [mm]**	**Channels in ϕ**	**Strip Pitch [μm]**	**Strip Length [mm]**	**Tilt Angle [°]**
0	405	28×1280	75.5	24.1	11.5
1	562	40×1280	75.5	24.1	11.0
2	762	56×1280	75.5	48.2	10.0
3	1000	72×1280	75.5	48.2	10.0

beam axis to 60.1 mm in the outermost region. The exact locations of the end-cap disks and the strip details are summarised in Table 3.2. The "rows" are counted from the innermost position to larger radii. A number of rows is then grouped into "rings" as they are combined in sensors. The stated strip pitch is averaged over the strip length for the wedge shaped strip segments. The end-cap disks are located between 1512 mm and 3000 mm on each side of the detector.

Stereo angles are implemented in the barrel and end-cap systems giving the second coordinate measurement. In the barrel, the strips are rotated by 26 mrad on each side of a layer with respect to the beam axis to allow a total stereo angle of 52 mrad. In the end-cap a 40 mrad stereo angle is achieved by rotating the strips by 20 mrad with respect to the radial orientation in each disk. The stereo angles for the barrel section and the end-caps are different in value due to technical constraints which are optimised separately for those systems. In the barrel case the stereo angle is achieved by rotating the actual sensors with respect to each other while the stereo angle in the end-caps is directly implemented in the sensor design (see Chapter 6). In addition, the barrel sensors are tilted in the $R\phi$ plane to allow the overlap of neighbouring sensors to be hermetic for tracks down to 1 GeV. The grouping of strips in strip modules and the technical implementation are described in detail in the following chapters.

3.2.2 Layout of the ITk Pixel Detector

The pixel layouts consist of five barrel layers and four end-cap ring layers. Changes in the detailed design of the Pixel Detector are still expected and the final layout will be presented in detail in the Pixel TDR in 2017. The Pixel Detector provides hermetic tracking coverage up to $|\eta| = 4$. The two innermost barrel layers and the innermost end-cap ring layer are placed inside an Inner Support Tube, allowing for their potential replacement. In contrast, the three outer barrel layers and three outer end-cap ring layers are between the Inner Support Tube (IST) and the Pixel Support Tube (PST), and are, like the Strip Detector, designed to operate for the entire lifetime of the HL-LHC.

Table 3.2: Main layout parameters for the strip end-cap.

Ring/Row	**Inner Radius [mm]**	**Strip Length [mm]**	**Strip Pitch [μm]**
Ring 0 Row 0	384.5	19	75.0
Ring 0 Row 1	403.5	24	79.2
Ring 0 Row 2	427.5	29	74.9
Ring 0 Row 3	456.4	32	80.2
Ring 1 Row 0	489.8	18.1	69.9
Ring 1 Row 1	507.9	27.1	72.9
Ring 1 Row 2	535	24.1	75.6
Ring 1 Row 3	559.1	15.1	78.6
Ring 2 Row 0	575.6	30.8	75.7
Ring 2 Row 1	606.4	30.8	79.8
Ring 3 Row 0	638.6	32.2	71.1
Ring 3 Row 1	670.8	26.2	74.3
Ring 3 Row 2	697.1	26.2	77.5
Ring 3 Row 3	723.3	32.2	80.7
Ring 4 Row 0	756.9	54.6	75.0
Ring 4 Row 1	811.5	54.6	80.3
Ring 5 Row 0	867.5	40.2	76.2
Ring 5 Row 1	907.6	60.2	80.5

Table 3.3: Main layout parameters for the Pixel barrel as simulated. The numbers of sensors per half stave refer to the central part of the barrel where sensors are placed parallel to the beam axis.

Layer	**Sensor Size [mm^2]**	**Sensors per Half Stave**	**Half Stave Length [mm]**	**Staves**	**Radius [mm]**
0	40.2×16.8	4.5	1250	18	39
1	40.2×33.8	5	1250	18	85
2	40.2×33.8	6	780	32	155
3	40.2×33.8	7	780	44	213
4	40.2×33.8	8	780	54	271

In the barrel layer sensors in the central region are placed tangential to a circle of constant radius centred on the beam-line while sensors in the forward parts of all barrel layers are inclined at an angle of 56° with respect to the beam axis. Non-inclined sensors are tilted by 14 ° in the transverse plane. The main layout parameters are detailed in Tables 3.3 and Table 3.5. For this document, the simulated pixel size is nominally set to 50× 50 μm^2 with a sensor thickness of 100 μm for the two innermost pixel barrel layers and the innermost ring layer, and 150 μm elsewhere.

Table 3.4: Main layout parameters for the forward barrel in the Inclined layout as currently simulated. The forward barrel shares a common mechanical structure with the central barrel, with dimensions indicated in Table 3.3. There is a stagger of 4 mm in z positions between inclined sensors on neighbouring staves in ϕ, with sensors on half of the staves having positions 4 mm closer to the centre of the detector than indicated here.

Layer	**Sensor Size [mm^2]**	**Positions on Barrel Stave [mm]**
0	20.0 × 16.8	197.8 - 1206.9 (17 positions)
1	20.0 × 33.8	214.4 - 1206.5 (18 positions)
2	20.0 × 33.8	254.1 - 719.6 (13 positions)
3	20.0 × 33.8	295.7 - 719.5 (17 positions)
4	20.0 × 33.8	336.7 - 719.4 (13 positions)

In the end-cap ring system, the positions of the rings along the z-axis are optimised separately such that each ring layer provides hermetic coverage for tracks coming from the collision region. These positions and the number of sensors in each ring are detailed in Table 3.5. The number of rings (positions) in the end-cap have not yet been optimised and are considered to be conservative.

Table 3.5: Main layout parameters for the pixel end-cap rings as simulated.

Ring Layer	**Sensor Size [mm^2]**	**Sensors per Ring**	**Inner Radius [mm]**	**Ring Positions [mm]**
0	40.2 × 33.8	24	80	1308 - 3000 (18 positions)
1	40.2 × 33.8	36	150	823 - 3000 (19 positions)
2	40.2 × 33.8	48	212.5	823 - 3000 (16 positions)
3	40.2 × 33.8	60	275	823 - 3000 (16 positions)

3.3 Material Description within the Simulation

Due to the large impact of material within the detector volume on the tracking performance, electron and photon measurements, fluences, and total ionising doses, particular care was taken to describe the material to be implemented as accurately as possible. Both active and

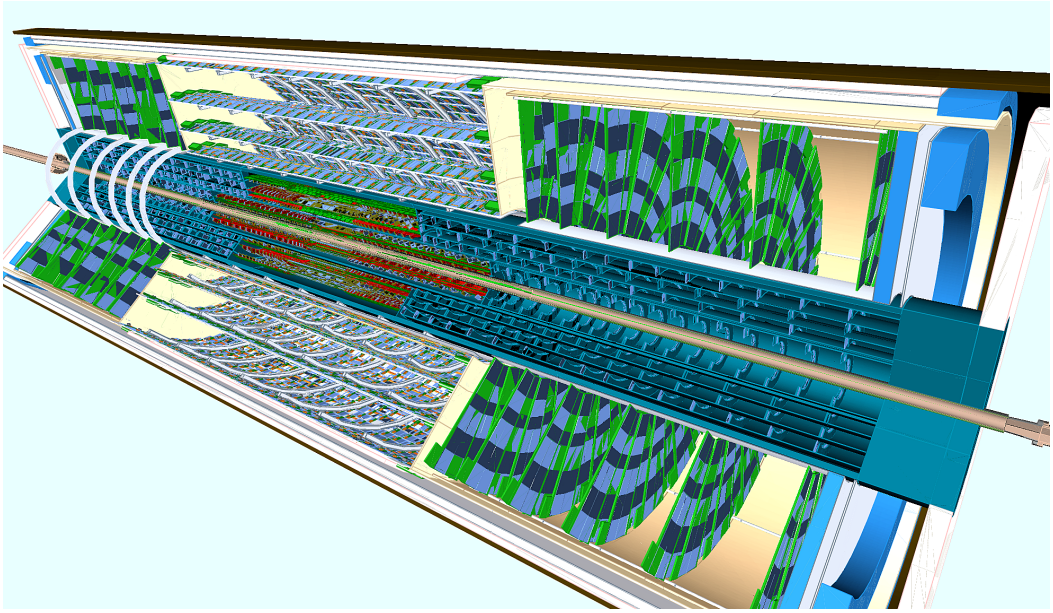


Figure 3.6: A visualisation of the ITk as implemented in the simulation framework

inactive elements of the detector were implemented in the simulation framework, which describes their size, position, and material composition. A visualisation of the simulated detector, including all material elements, is shown in Figure 3.6. The material description is based on the technical design of the detector as discussed in the following chapters.

For each pixel layout candidate simulation model, the relevant physical design was detailed by the ITk pixel mechanics groups. All pixel sensors are modelled as 100 μm thick silicon for the innermost two layers and as 150 μm elsewhere, and front-end chips are modelled as silicon with extra elements added as appropriate, corresponding to additional chip components such as metal layers. This approach provides a conservative estimate of the material. For pixel barrel services, the cable material included varies as a function of z to accurately reflect the number of cables that will be required for the modules at that position. For pixel end-caps, the masses and materials of both the support structure and services are modelled according to mechanical descriptions. For the Inclined design, the individual inclined-sensor supports are individually modelled as carbon foam wedges.

The strip barrel detector models each material contribution separately, with masses and material compositions reflecting the mechanical designs. For the strip end-caps some materials are merged: materials/objects that sit next to each other are not individually modelled, but instead one homogeneous block of material is included, adjusted to have the correct radiation length as calculated based on the engineering designs.

For the Strip Detector global supports, the barrel and end-caps are modelled in detail, including the stave cooling pipes, carbon-foam, face-sheets, cable bus, hybrids, and front-end ASICs. In the end-caps, the silicon sensors are described individually, but the remain-

ing components on the substructure are modelled as a single wedge-shaped object placed between the two silicon layers, and uniformly filled with a generic material. The density of this material is adjusted to give a radiation length of 2% per substructure, matching the mechanical design. Service volumes are modelled as annuli or cylinders, with the simulation including as many volumes as necessary to describe the local changes in service material, which is uniform over each volume. The material in each volume is calculated based on cable cross sections which give the mass per unit length, scaled by the necessary length and number of cables. A scaling factor of 1.3 is applied to account for e.g. indirect routing, clips, supports, and to provide a safety factor on the material estimate.

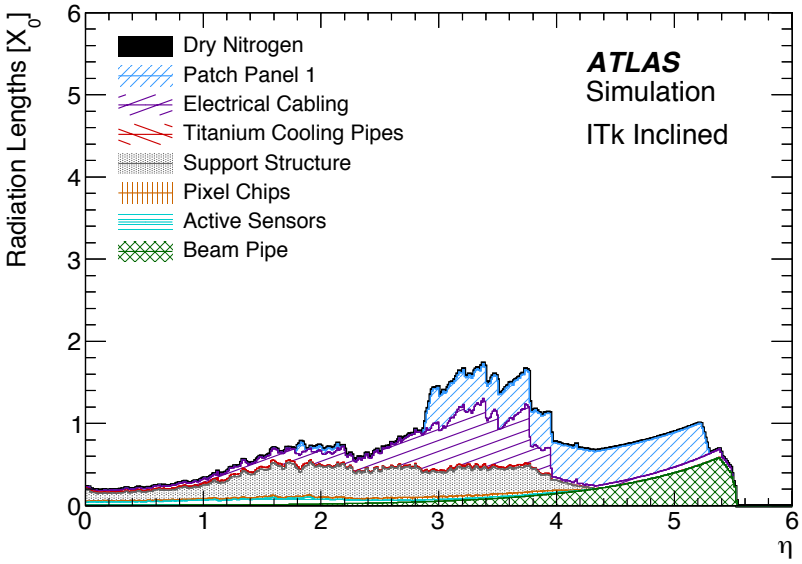


Figure 3.7: Radiation length X_0 versus η. The figure shows only positive η since the material distribution is symmetric about $\eta = 0$.

The pixel patch-panel 1 is modelled as a solid, homogeneous 40 kg cylinder at each end of the Pixel Detector. The material is a mixture of various metals typical for patch-panels. Patch-panel 1 for the Strip Detector is modelled as a 20 kg annulus for each barrel end and each end-cap end (two separate annuli at each end), filled with the same generic material as used for end-cap substructures. The poly-moderator is modelled as a 25 mm thick cylinder along the outer part of the cryostat bore. A second piece, 20 mm thick, is modelled inside the outer support cylinder, slightly shorter than the barrel staves. Disks with thickness 70 mm are placed at the extremes of the ITk volume.

The material distribution in X_0 versus η is shown in Figure 3.7 for the Inclined layout. The central region of η between 0 and 1 has very little material ($\sim$0.3% X_0 as foreseen by the light design of the sensor supports). At higher η the effect of the inclined services in the gap along the beam-pipe can be seen.

For comparison the same distribution is shown for the current ATLAS Inner Detector in Figure 3.8. Here the Run 2 configuration with the new innermost pixel layer (Insertable

B-Layer, IBL), which was installed in ATLAS during Long Shutdown 1, is shown. In comparison to the current ID, the ITk material budget is around 30% lower in the region $|\eta| < 4.0$. At the highest $|\eta|$, an even larger reduction is achieved.

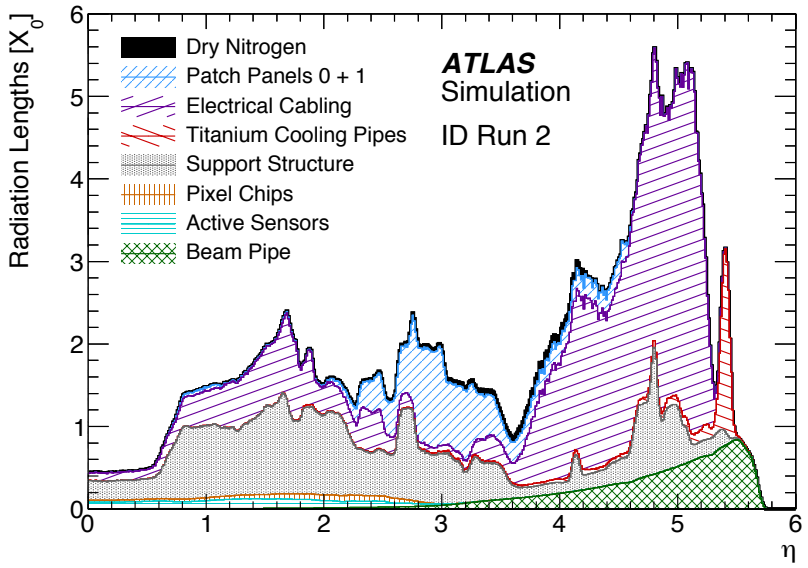


Figure 3.8: Radiation length X_0 versus the rapidity η for the current ATLAS Inner Detector (Pixel, SCT, TRT).

3.4 Radiation Environment Expectations for the ITk Detector

Due to the increased luminosity and the associated increase in the number of particles, the expected radiation levels in the ITk will increase by roughly an order of magnitude compared to the present ATLAS Inner Detector. The radiation background simulations are performed for the ATLAS ITk using the FLUKA particle transport code [14] and the PYTHIA8 event generator [15]. The predictions of particle fluences and ionising doses for the ITk layout assume an integrated luminosity of 3000 fb^{-1}, a proton-proton inelastic cross-section of 79.3 mb at a centre-of-mass $\sqrt{s}$ = 14 TeV [16]. In Figure 3.9 the fluence and dose distributions for the ITk layout are shown. It is important to emphasise that accurate fluence and dose predictions require accurate modelling of the entire ATLAS geometry in FLUKA [14]. In the ITk strip regions the fluences are dominated by particles coming from interactions in the calorimeter, beam-line and ITk service material. The ITk services are routed out radially away from the beam-line as soon as feasible, as this is beneficial in reducing radiation backgrounds, including the activation of detector components.

In summary, the maximum 1 MeV neutron equivalent fluences for the pixel, short-strip, long-strip barrel and strip end-cap detectors are predicted to be 1.5×10^{16} cm^{-2}, 5.4×10^{14} cm^{-2}, 2.8×10^{14} cm^{-2} and 8.2×10^{14} cm^{-2}, respectively. The corresponding values for the

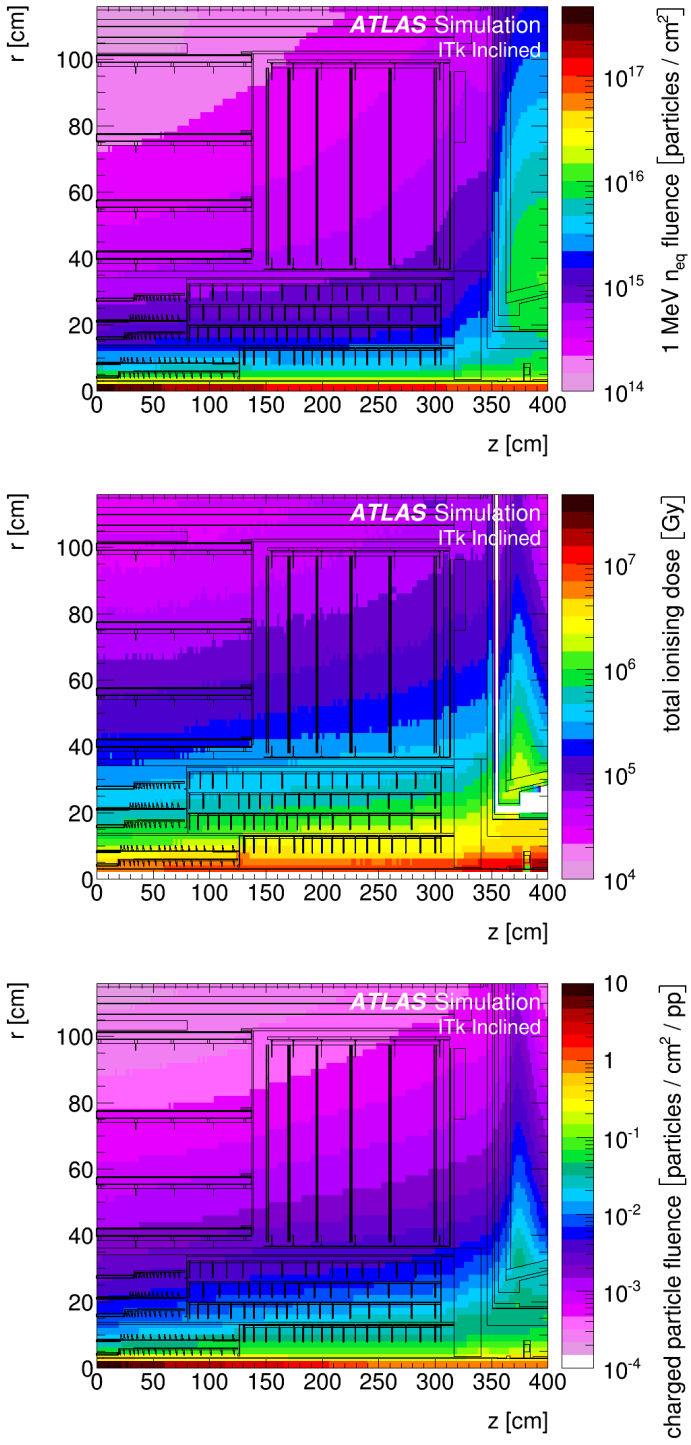


Figure 3.9: The fluence and dose distributions for the ITk layout. **Top**: The 1 MeV neutron equivalent flux. **Middle**: The total ionising dose. **Bottom**: The charged particle fluence.

ionising dose are 1140 MRad, 23.8 MRad, 7.1 MRad and 33.6 MRad. Hadron fluences for energies down to 20 MeV are also calculated to allow estimates of Single Event Upsets (SEU) as well as charged particle fluences for occupancy estimates.

3.4.1 Radiation Safety Factors

Table 3.6: Overview on maximal fluences and doses. The values including a safety factor of 1.5.

Layer	**Radius** [mm]	**Maximal Fluence** [n_{eq}/cm^2]	**Maximal Dose** [MRad]
Strips			
Long Strips	762	3.8×10^{14}	9.8
Short Strips	405	7.2×10^{14}	32.5
End-cap	385	1.2×10^{15}	50.4
Pixels			
Layer 0	39	1.87×10^{16}	1268
Layer 1	75	0.59×10^{16}	549
Layer 2	155	0.22×10^{16}	129
Layer 3	213	0.15×10^{16}	87
Layer 4	271	0.11×10^{16}	53
End-cap	80	0.62×10^{16}	477

Comparisons between fluence and dose predictions and measurements have been made during Run-1 at $\sqrt{s} = 7$ TeV and 8 TeV [17]. The typical agreement was better than 30% and a safety factor 1.5 has been used for the simulation component in the predictions. Although a safety factor of 1.5 is assumed, irradiation tests routinely evaluate components up to twice the expected fluences to check there is no sudden degradation just beyond the specified dose limit. All radiation tests presented in this document take the values in Table 3.6 as baseline (safety factor 1.5).

4 ITk Performance and Physics Benchmark Studies

The expected performance of the ITk detector is presented in this chapter for the layout presented in Section 3. The proposed tracker layout is based on the requirement for identifying charged particles with high efficiency and measuring their properties with high precision at the average pile-up values of ~ 200 expected at the HL-LHC.

Section 4.1 shows that the average occupancies are below the 1% level in all components and the maximum channel occupancy per module is consistent with the expected readout limitations. Section 4.2 explains the track reconstruction, and shows that the tracking efficiencies for individual particles are as high as in Run 2, and that fake rates are low, even at pile-up values of $\sim$200. It is also shown that for most track parameters the resolution is improved compared to the current ATLAS tracker, and it is demonstrated that the basic tracking performance is not strongly affected by typical failure modes which may be expected to occur during the LHC lifetime. Section 4.3 shows that the primary vertex position can be reconstructed accurately and with good efficiency, even in high pile-up environments, which is particularly important for the identification of b-jets. It is shown that the b-tagging performance is as good or better than Run 2 in the region $|\eta| < 2.5$, and that even at higher η values there is significant separation power between b- and light jets, albeit less than in the central region. Section 4.4 shows that for electrons, photons and τ-leptons the ITk performance is adequate, yielding results comparable to Run 2. The usage of tracking for the reconstruction of jets and the missing transverse energy, is also illustrated, in particular to suppress jets from pile-up interactions up to values of $\eta = 4.0$. Section 4.5 explains the challenges of reconstructing tracks in very dense environments as expected from jets or τ-leptons with $p_T > 1$ TeV produced in decays of multi-TeV mass objects (e.g. Z', W', axigluon, RS Graviton, ...). It is shown that the presence of five pixel layers provides the robustness needed to reconstruct tracks in such environments reliably.

All studies presented in this chapter are performed using MC events based on a full Geant4 simulation. For most studies, samples are used where an average of 200 pile-up interactions are overlaid to the hard-scattering event. The reconstruction software used is adapted from Run 2 to reflect the new geometry, and takes advantage of further improvements implemented e.g. to enhance the speed. While the reconstruction software is not yet fully optimal for the ITk (e.g. the pixel clustering can be further improved) it is sufficient to build confidence that the performance that can be achieved is adequate for the HL-LHC physics goals.

Finally, a discussion of the performance for selected physics channels is given to illustrate the capabilities of the upgraded ATLAS detector in Section 4.6. These make use of a parametric simulation, based on the performance determined using full simulation.

4.1 Occupancy Studies for the ITk Strip Detector

In this Section the hit densities are presented to give a global view of the particle fluxes through the various detector layers. The fraction of channels per module which register a hit and need to be read out, referred to as channel occupancy, is also presented. It is simply given by the hit occupancy divided by the number of channels in a module. Here the goal is an average value of at most 1% to ensure a robust and efficient pattern recognition, and a maximum value per event well below 90% to avoid saturation of the readout. For link occupancy values above 90% data losses can occur, see 2.

For the following it is assumed that the detector is read out in the so-called "01X" mode, as is currently the case for Run 2. This means that a hit (1) is only counted if there is no hit in that same channel in the previous bunch crossing (0), and regardless of whether or not there is a hit in the subsequent bunch crossing (X).

The average hit density is calculated using 200 overlaid minimum-bias events, and shown in Figure 4.1. In the barrel it is highest in the innermost layer at 0.005 hits / mm^2. It falls roughly quadratically with radius and is approximately independent of z. In the disks it also falls with increasing radius within each disk. It is about 15% higher in the disk closest to the end-cap calorimeter (disk 5), in part due to back-scattering of particles. A two-dimensional representation (R vs z) of the hit density is shown in Figure 4.2.

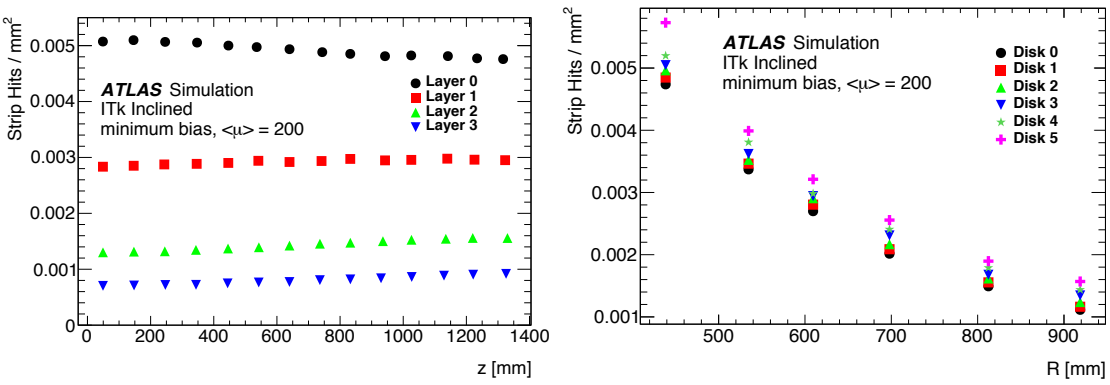


Figure 4.1: Average hit density, for the Strip Detector, in the barrel (left) and in the disks (right) for minimum bias events with $\langle\mu\rangle$=200.

The average channel occupancy, defined as the fraction of readout channels with a hit recorded above the threshold, for $\langle\mu\rangle = 200$ is presented in Figure 4.3 for the barrel and end-cap. It is seen that the occupancy is below 1% in all layers in the barrel. In the disk it is typically

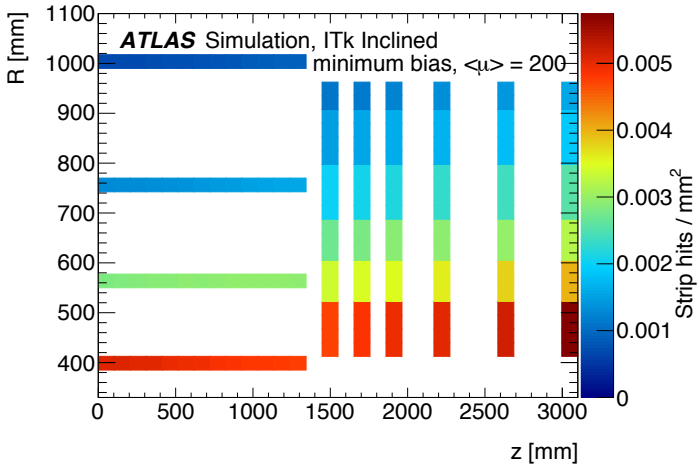


Figure 4.2: The average hit density calculated from minimum bias events with $\langle\mu\rangle = 200$ in the Strip Detector.

0.6-0.8% except for the innermost radius where it is up to 1.2%. This slight excess over the 1% requirement in the outermost disks does not compromise the pattern recognition quality. It is also seen that the occupancy is nearly independent of z in the barrel, and that it is very similar for layers 1 and 2. While the hit density is about a factor two lower for layer 2 due to its larger radius, as seen in Figure 4.1, the strip length is a factor two longer, thus yielding nearly the same occupancy. In the disks the occupancy is generally highest for the outermost disk (disk 5) due to back-scattering of particles from the end-cap calorimeter.

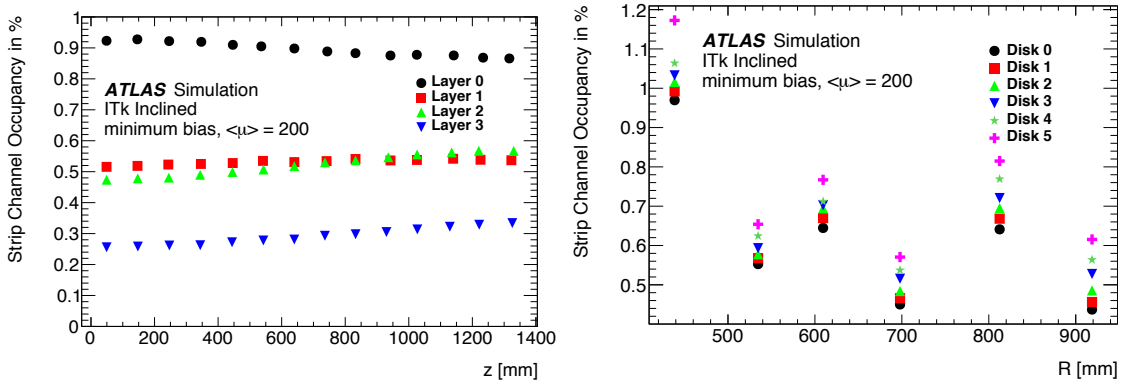


Figure 4.3: The channel occupancy, in the Strip Detector, for the barrel (left) and the disks (right) calculated from minimum bias, $\langle\mu\rangle$ = 200 events .

Two-dimensional views of the average occupancies in the strip detector and the entire ITk are provided in Figure 4.4. It is seen that the occupancy in the pixel detector is typically a factor 10 lower than in the strip detector.

The maximum channel occupancy seen in a sensor per barrel layer and ring of a disk per event in $t\bar{t}$, $\langle\mu\rangle$ = 200 events is shown in Figure 4.5. It is typically 5-10% and well below the

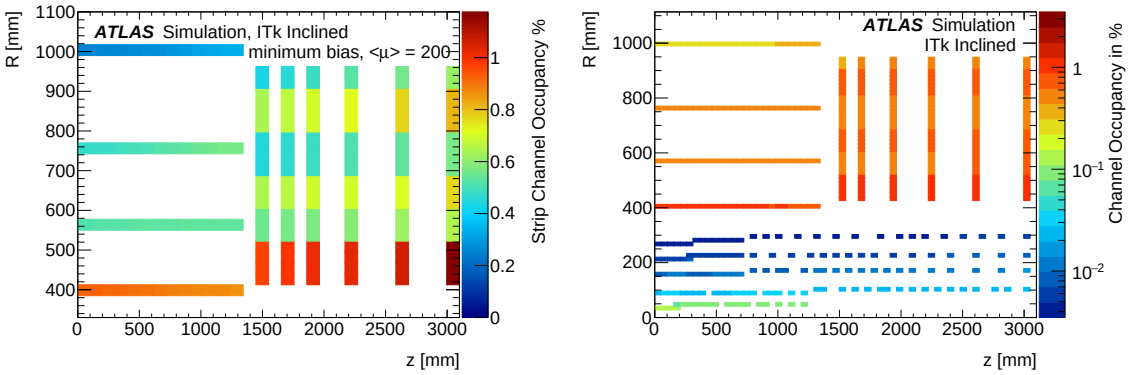


Figure 4.4: The average channel occupancy calculated from minimum bias events with $\langle\mu\rangle = 200$ in the Strip Detector.

90% readout constraint.

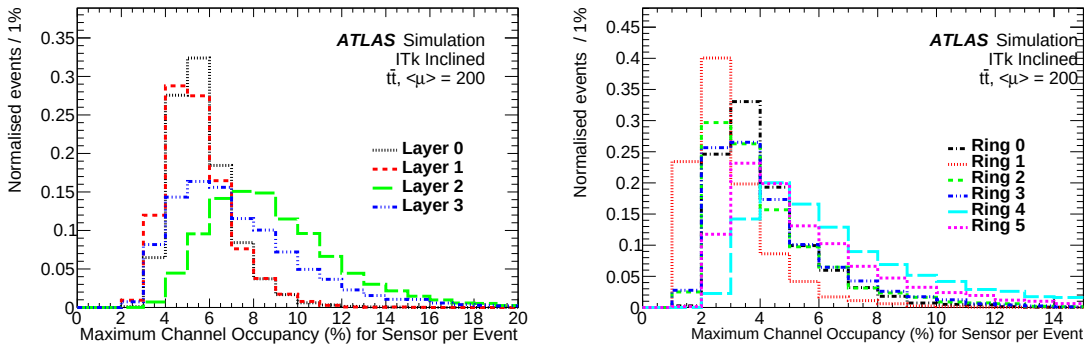


Figure 4.5: The maximum channel occupancy per strip sensor per event in $t\bar{t}$, $\langle\mu\rangle = 200$ events for each layer (left) and for each ring of the disks (right).

4.2 Tracking Performance

In this section a brief description of the track reconstruction is given, and then the performance is quantified in terms of efficiencies, fake rates and track parameter resolutions.

4.2.1 Track Reconstruction

A full description of the tracking used in ATLAS can be found in Ref. [18,19]. It is a complex procedure consisting of several steps, and highly optimised for CPU efficiency as tracking typically dominates the event reconstruction time, particularly at high pile-up. Here, only a brief description is provided. The algorithms used are the same as for Run 2 but have been

optimised to include tracking up to $|\eta| < 4.0$, to account properly for the different geometry (e.g. the inclined modules in the pixel system), and to reduce the CPU consumption.

Before the track reconstruction starts, the hits recorded with a charge above a set threshold are grouped into clusters of adjacent hits in both the pixel and strip detectors. For Run 2, the position in the pixel detector is determined using a neural network [13] which exploits the measured value of the charge of the energy deposit, yielding a 10-20% better resolution than the geometric mean of the hits. Since the details of the pixel detector readout, including the granularity of charge information, are not yet decided, no charge information is used for ITk pixels. Thus, for most of this document, the ITk pixel cluster position is determined as the geometric mean of the hits, and referred to as *digital clustering*. Only for Section 4.5, where resolving nearby tracks is critical, an emulation of the neural network is performed assuming that the ITk pixel detector will achieve a similar performance to IBL in terms of resolving merged clusters. For the ITk strip detector, no charge information is available and thus the geometric mean is always used.

Three-dimensional space points are formed from either a single pixel cluster or a pair of strip clusters on both sides of the same module. For the strip clusters, the z-position is determined using the stereo angle between the pair of strip clusters. Space-point triplet combinations – hereafter referred to as "seeds" – are formed and used to seed the combinatorial Kalman filter [20]. In the first iteration, these are required to all come from the ITk Strip Detector (SSS) as the purity of seeds is significantly higher [18, 21]. In a subsequent iteration, track seeds with all three space-points from the ITk Pixel Detector are used (PPP). At this point, a bookkeeping tool is used to reject combinations already used to find good track candidates. Based on these seeds, candidate track parameters are defined and then used to start the combinatorial filter [1)]

Figure 4.6 shows the number of SSS and PPP seeds per event versus η. It is seen that the number of SSS seeds is a factor 10 lower than that of PPP seeds as a result of the much higher purity of SSS seeds, already seen in Run 2 [18, 21] at $\mu \approx 40$. By first using the SSS seeds, and discarding any PPP seeds which appear to be duplicates, and then confirming the seeds by one additional layer before propagating the seed track to additional layers to attach clusters, a significant CPU improvement is achieved. The importance of SSS seeds in this initial tracking stage is one of the motivations to have at least four strip layers in the ITk; less would not provide enough redundancy for the seeding in case of module failures.

Following this stage of the track reconstruction, an ambiguity solving step is performed on the resulting track candidates, with the aim of rejecting incomplete and duplicate tracks, resolving situations with shared clusters between several tracks, and removing fake tracks. This is achieved by scoring the track candidates based on the presence or absence of hits when crossing the sensor layers. The procedure is repeated iteratively, attributing shared clusters to the higher scoring track candidate, and refitting all the candidates, to obtain

[1] This explanation is simplified. In reality there are further steps, particularly to improve the CPU performance.

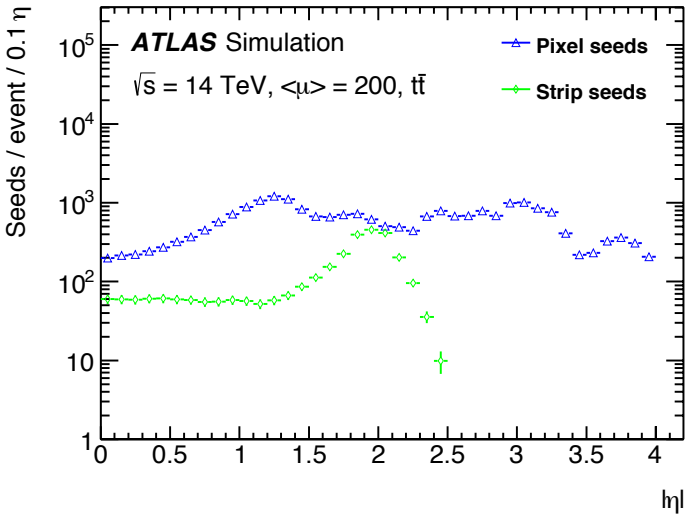


Figure 4.6: Number of track pixel (PPP) and strip (SSS) seeds versus η for $t\bar{t}$ events with 200 pile-up interactions for the ITk.

the final set of tracks. Both the pattern recognition and ambiguity solving steps have been adapted to take into account the effects of bremsstrahlung to improve electron track reconstruction.

Finally, the track candidates must satisfy a set of quality and kinematic cuts to be considered as tracks. These were optimised separately in three η ranges, and are listed in Table 4.1. There is a series of requirements on the presence of clusters and holes, which are the same in all three η ranges. Here, a hole is defined as an intersection of a track with a sensitive detector element where no cluster is present. Holes are indicators of fake tracks since the sensors are designed to be highly efficient ($>$ 99% for the entire lifetime) and thus for true particles holes are very rare. In addition, cuts on the track parameters are made. In the central region a p_T cut of 900 MeV is made to ensure full efficiency at 1 GeV. In the forward region ($|\eta| > 2.7$) this cut is relaxed to ensure a high efficiency for particles with p_T>1 GeV despite the significantly poorer p_T-resolution in this region. The d_0 requirement is also relaxed due to the inferior resolution at high η.

An important consideration for the design of both candidate layouts is the CPU time required to reconstruct HL-LHC events with up to 200 pile-up. Even though the track reconstruction has yet to be fully optimised, events with $\langle\mu\rangle = 200$ can be fully reconstructed within in about 2000 HS06 seconds. Further improvements are expected from further optimisation and multi-threading techniques.

Table 4.1: Set of requirements applied during the track reconstruction depending on the pseudorapidity interval for the ITk layout.

Requirement	**Pseudorapidity interval**	
	$\lvert\eta\rvert < 2.7$	$2.7 < \lvert\eta\rvert < 4.0$
Pixel+Strip clusters	≥ 9	≥ 9
Pixel clusters	≥ 1	≥ 1
Holes	< 3	< 3
Pixel holes	< 2	< 2
Strip holes	< 3	< 3
Double Strip holes	< 1	
p_T [MeV]	> 900	> 400
$\lvert d_0\rvert$	≤ 2 mm	≤ 10 mm
$\lvert z_0\rvert$	≤ 25 cm	≤ 25 cm

4.2.2 Number of Clusters on Tracks

The mean number of clusters per track is shown in Figure 4.7 as a function of η for single muons with $p_T = 10$ GeV and no pile-up for the pixel tracker, the strip tracker, and both together. The ITk provides at least 13 silicon hits up to $|\eta| = 4$. In the barrel region 8 strip clusters are expected on average, one for each strip module side, and 5 pixel clusters, one per pixel layer. In the end-cap regions, the number of clusters is kept the same, except for the transition region between the barrel and the end-cap near $|\eta| \approx 2$ where it is higher. This study shows the expectation for a detector with no defects. Thus any holes, i.e. missing measurements on a track where one would expect to have hit an active sensor, are due to pattern recognition mistakes and finite sensor inefficiencies [2)]. The average number of holes is below 0.1 per track for fully efficient modules in the simulation.

4.2.3 Tracking Efficiency and Fake Rate

Among the most important performance criteria for a tracking detector are tracking efficiency and the rate at which "fake" tracks are reconstructed. Fake tracks are constructed from random associations of genuine clusters from tracks and (to a much smaller extent) noise hits. Significant background contributions can arise due to such fake tracks, and so understanding and minimising the number of fake tracks is important when designing a tracking detector. The efficiencies and fake rates cannot be defined unambiguously and depend on track reconstruction algorithms. Here, two different approaches are used to study fake track rates.

[2] The hit efficiency is expected to be at least 99% for the lifetime of the Strip detector.

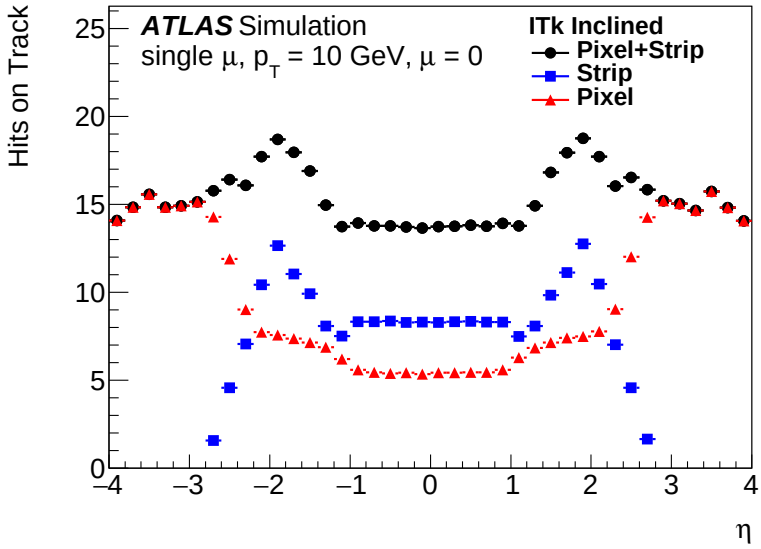


Figure 4.7: Mean number of hits per track as a function of η for single muons with $p_T = 10$ GeV for the ITk layout. The uncertainty on the mean values is too small to be visible.

The tracking efficiency is defined as the fraction of prompt particles which are associated with tracks passing a track quality selection. The particles considered must satisfy $|d_0^{\text{truth}}| < 1.0$ mm and $|z_0^{\text{truth}}| < 150$ mm, $p_T > 1$ GeV and $|\eta| < 4.0$, and be produced by the primary interactions. Secondary particles produced in the Geant4 simulation are excluded.

For the efficiency calculation, tracks are required to have a high probability of matching to a truth particle satisfying the above cuts. The matching probability, P_{match}, takes into account that a single track can have clusters that are generated by different particles, and is basically [3] defined as:

$$P_{\text{match}} = \frac{2N_{\text{common}}^{\text{pix}} + N_{\text{common}}^{\text{strip}}}{2N_{\text{track}}^{\text{pix}} + N_{\text{track}}^{\text{strip}}} \tag{4.1}$$

where $N_{\text{common}}^{\text{pix/strip}}$ is the number of Pixel/Strip-detector clusters common[4] to both the track and the particle to which it is being matched, and $N_{\text{track}}^{\text{pix/strip}}$ is the number of Pixel/Strip-detector hits assigned to the track. The factor of 2 included for N^{pix} arises due to the fact that each Pixel layer provides one 2D measurement of the track whereas a double sided silicon layer provides two 1D measurements. A probability value of 1.0 is found if all clusters of the reconstructed track are associated with the same truth particle, while a value of 50%

[3] For clusters without any truth information (noise hits and very low momentum particles from secondary interactions failing the truth cuts applied in Geant) the weight is reduced by a factor of two.

[4] i.e. the information in the simulation is used to ensure the hit is the same for the truth particle and the reconstructed track, i.e. the hit (truth) is common between truth and reconstruction.

implies that half the clusters are associated with a given truth particle while the others clusters are associated with one or more other truth particles.

The tracking efficiency, ϵ_{track}, is defined as the number of selected reconstructed tracks matched to a selected truth particle (satisfying the above cuts) with $P_{\text{match}} > 0.5$, divided by the number of selected truth particles:

$$\epsilon_{\text{track}} = \frac{N_{\text{reco}}(\text{selected, matched})}{N_{\text{truth}}(\text{selected})} \tag{4.2}$$

Figure 4.8 (top left) shows the inclusive efficiency to reconstruct tracks of charged particles, with $p_T > 1$ GeV, versus η in $t\bar{t}$ events with $\langle\mu\rangle$=200. A reconstruction efficiency of 85-93% is attained. At $\mu = 0$, the efficiency is compared to that in Run 2 (top right), showing that it is very similar. The inefficiencies observed are largely due to hadronic interactions with the detector material. For high-p_T muons, the efficiency is much higher as seen in Figure 4.8 (bottom left). It is typically 99% for both the ITk and Run 2.

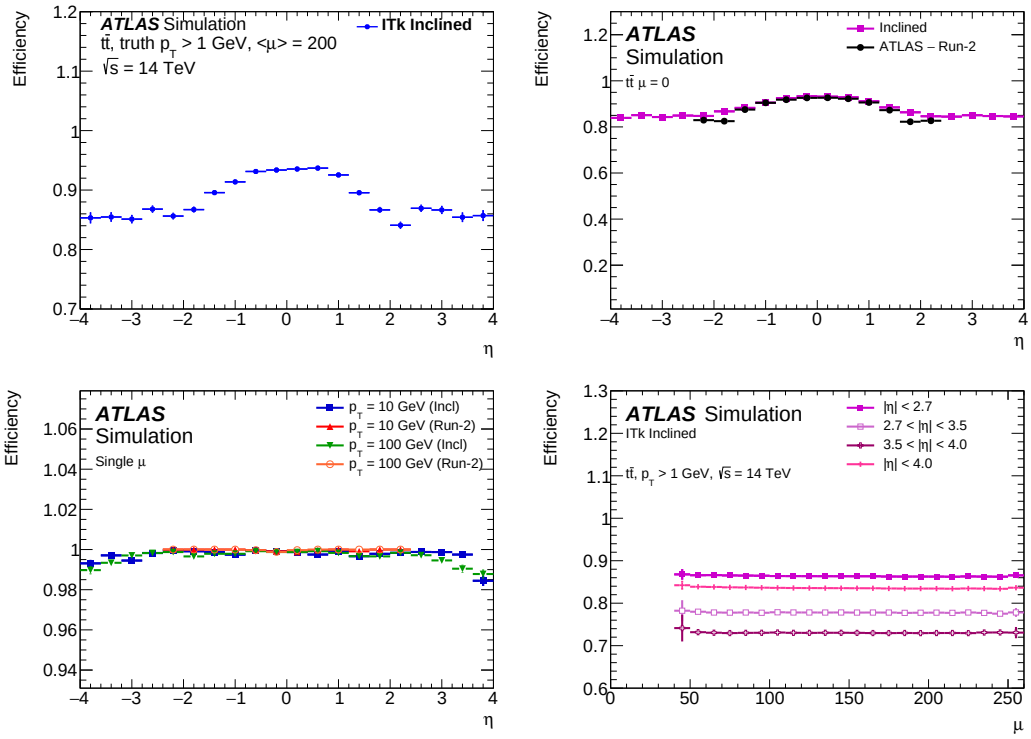


Figure 4.8: Track reconstruction efficiency for particles as function of η in $t\bar{t}$ events with $\mu = 200$ (top left), $t\bar{t}$ events with no pile-up (top right) and single muons at various p_T values with no pile-up (bottom left). For $\mu = 0$ the Run 2 efficiencies are also shown in the top right and bottom left figures. The dependence of the efficiency on μ is shown for different η-regions in the bottom right for particles in $t\bar{t}$ events.

Figure 4.8 also shows that the efficiency is independent of μ in the range 40-260 for all η-ranges, showing that the additional number of clusters produced by pile-up interactions does not disrupt the pattern recognition.

Defining a fake or mis-reconstructed track is ambiguous and difficult. Here two methods are used. In the first method, the ratio between the rate of reconstructed and the rate of generated tracks is evaluated. As the number of generated tracks increases (at increasing pile-up) more and more clusters are produced and this makes the track reconstruction vulnerable to finding more and more fake tracks, i.e. random combination of clusters. Figure 4.9 shows the ratio of the reconstructed to the generated number of tracks versus the number of pile-up interactions for four regions in η. It is seen that the ratio is flat versus μ for the tracking cuts used (given in Table 4.1) to within 1%. Based on such studies it was concluded that a minimum of 9 silicon hits is required to ensure the pattern recognition is robust against pile-up for a fully efficient detector (without any simulated defects or irradiation effects), and fake tracks are well controlled. This observation was one of the reasons for designing the detector such that at least 9 hits should be available even if after a decade of operation several modules in a given ϕ-region becomes compromised, and no longer provide useful data.

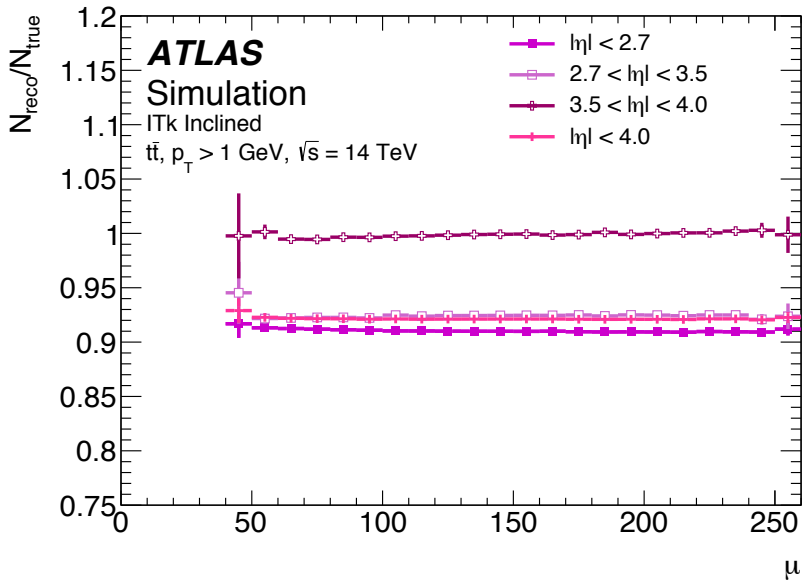


Figure 4.9: Ratio of the number of reconstructed tracks to the number of charged particles versus μ

A more direct way of assessing the fake rate is to consider the fraction of all reconstructed tracks that do not match to any truth particle, i.e. have a match probability below 50%. Studies using $t\bar{t}$ events indicate that the rate for fake tracks with respect to all tracks with $p_T > 1$ GeV is below 10^{-4} in the entire acceptance region.

4.2.4 Track Parameter Resolutions

ATLAS parameterises its tracks using the following five quantities to define the helical trajectory:

- the particle charge divided by the transverse momentum, q/p_T;
- longitudinal and transverse impact parameters, z_0 and d_0;
- polar and azimuthal angles, θ and ϕ.

The resolutions for these parameters are obtained from simulation by comparing their reconstructed values for a given particle with the truth value. The tracks used to calculate the resolution are required to pass the same selection as for the efficiency calculation. Tracks must be matched to a truth muon with $P_{\text{match}} > 0.5$.

The resolutions on the track parameters are obtained using an iterative procedure to define the RMS of a parameter without this being distorted by non-Gaussian tails. Initially this is determined with outliers beyond 3 σ of the mean being removed[5)], and the RMS then recalculated. This is repeated until a stable value for the RMS is found, which is assigned as the resolution.

Figure 4.10 shows the resolutions on the transverse and longitudinal impact parameters, $\sigma(d_0)$ and $\sigma(z_0)$, the resolutions on the azimuthal and polar angles, $\sigma(\phi)$ and $\sigma(\theta)$, as well as the relative resolution on the curvature, $p_T\,\sigma(1/p_T)$. These are shown for single muons with various p_T values.

For tracks with p_T of 100 GeV, the intrinsic d_0 resolution dominates over the multiple scattering, and a resolution below 10 μm is achieved for $|\eta| < 3.0$. It is 20-30% worse than the resolution in Run 2 due to the usage of digital clustering and the larger inner radius of the first pixel detector layer. For the lower p_T values, multiple scattering contributes significantly and the values for ITk are very comparable to Run 2 for the d_0 resolution for $|\eta| < 2.5$. Even at higher η the resolution remains rather good, indicating that useful information will be provided by these tracks for b-tagging purposes.

The z_0 resolution is better for ITk than Run 2 at all values of p_T , primarily due to the decreased pixel pitch in the z direction. In particular, in the central region, the current pitch of 250 μm in the inner pixel layer (IBL) results in there being no charge sharing, limiting the resolution to $\approx$ 250 μm, while the pitch of 50 μm of ITk results in charge sharing being present also for central tracks.

The momentum resolution is typically 50% better in the ITk than in Run 2, primarily due to the higher precision of the strip tracker compared to the TRT, and due to the reduced material. It degrades towards the forward region, mostly due to the fact that the particles traverse less of the magnetic field provided by the solenoid.

[5] For p_T=1 GeV muons, going from η=0 to η=4.0, 1.5% to 2.5% of the tracks are excluded as outliers. This percentage decreases as the p_T of the muon increases.

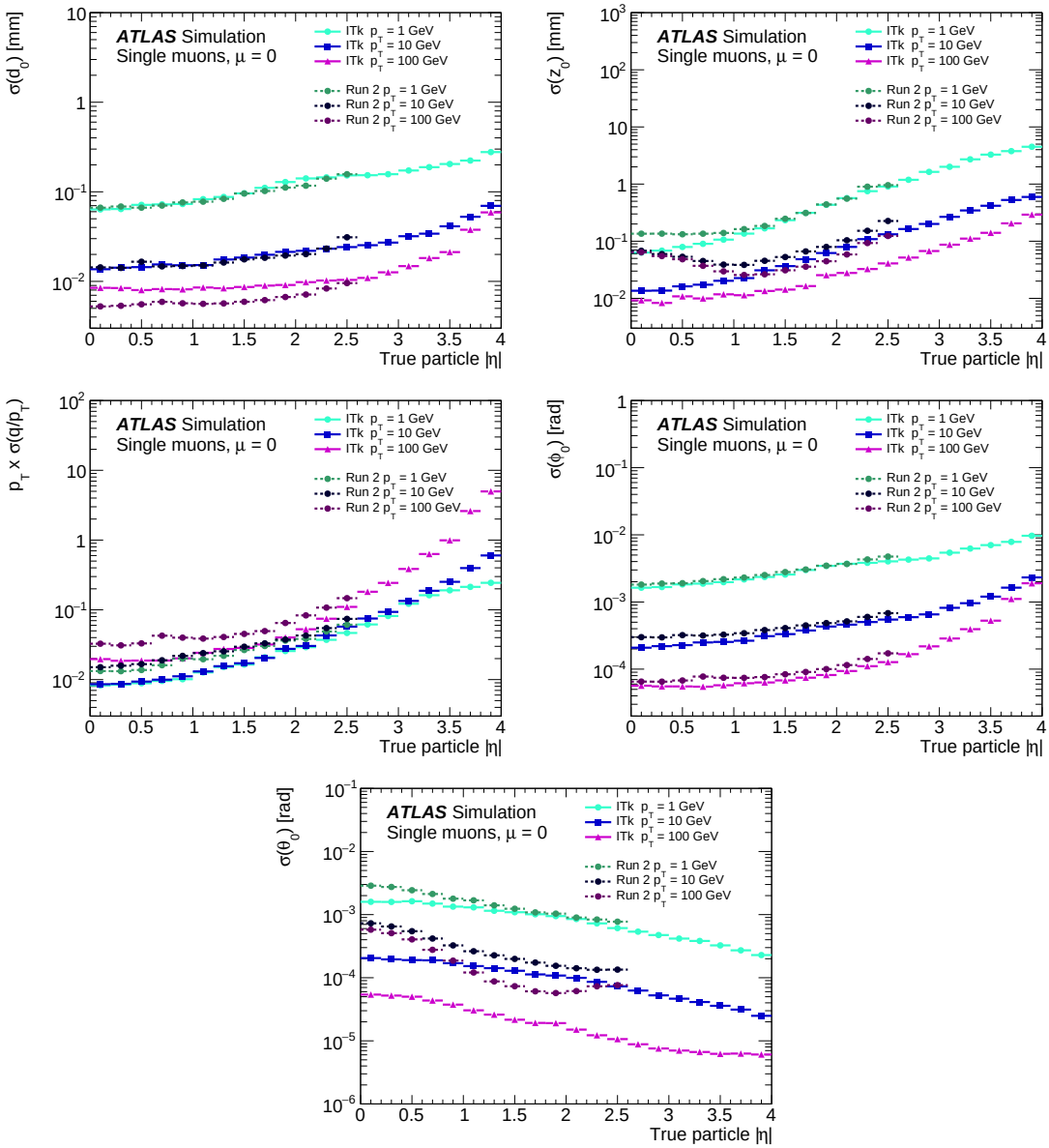


Figure 4.10: Resolutions on track parameters d_0, z_0, q/p_T, ϕ, and θ, as a function of true track η, for single muons with p_T of 1, 10, or 100 GeV, for $\langle\mu\rangle = 0$. Results for Run 2 are shown for comparison.

The angular resolutions are both improved compared to Run 2. While for the azimuthal angle, ϕ_0, the improvement is moderate, it is very significant for the polar angle, θ_0, particularly for p_T=100 GeV. The reason for this very large improvement is again the shorter pixel pitch in the longitudinal direction which results in a single track depositing hits in more than one pixel, allowing for a much more accurate position determination than is possible in Run 2 where all the charge is deposited in a single 250 μm long pixel in the z-direction. The θ resolution improves as tracks are more forward since the charge is shared among more pixels allowing an even more accurate determination of the polar track incidence angle.

4.2.5 System Redundancy

Based on experience from previous silicon detectors, it is expected that during the lifetime of the HL-LHC module failures will occur, despite all efforts made currently to design the detector as robustly as possible. As nine clusters are needed as a minimum to ensure that tracks can be measured well and fake rates are controlled, the available 13 cluster measurements provide the necessary robustness in case individual modules fail, or sensors develop inefficiencies. If a single strip module fails, the pattern recognition needs to find 9 out of 12 available clusters. This is still possible with high efficiency. And, even if an additional module fails there is still enough redundancy. However, any further reduction in layers would quickly lead to reduced efficiencies in case of module failures.

To determine the robustness of the ITk Strip Detector layout, different system failures were simulated using a $t\bar{t}$ sample with $<\mu>$ = 200:

- Known failures: the disabled modules are stored to the database and the information is used in the track reconstruction, so that missing hits in these modules are not considered "holes". As examples, one strip stave on the innermost Strip layer (positive η barrel side only corresponding to 28 modules) is turned off, and 10% random Strip modules (barrel and end-cap) are not being read out. Such failures would occur if there are problems with the electronics or cooling preventing data transmission or powering of components.
- Unknown failures: these are not known in the database and thus the missing hits do contribute as "holes". This can occur due to irradiation. Up to 5% inefficiencies are considered in this study, albeit the system is designed to have inefficiencies below 1% after the irradiation expected from HL-LHC.

Figure 4.11 shows the track reconstruction efficiency vs. η and p_{T}. It is seen that the track reconstruction efficiency is not reduced when one stave or 10% of the modules are known to be disabled for the tracking algorithm and requirements [6)] described in Section 4.2. The

[6] It was checked that if 10% of modules fail in a random, unknown way (e.g. due to irradiation) the tracking efficiency is reduced by 1% but this is not expected to occur during the HL-LHC lifetime.

impact of random failures in the Pixel detector of 1%, 3% and 5% on the tracking efficiency is also shown. For the central region the efficiency is unaffected while in the most forward region inefficiencies up to 5% are seen. Studies have shown that such failure modes have no significant impact on either the fake rate or the track parameter resolution with the proposed layout.

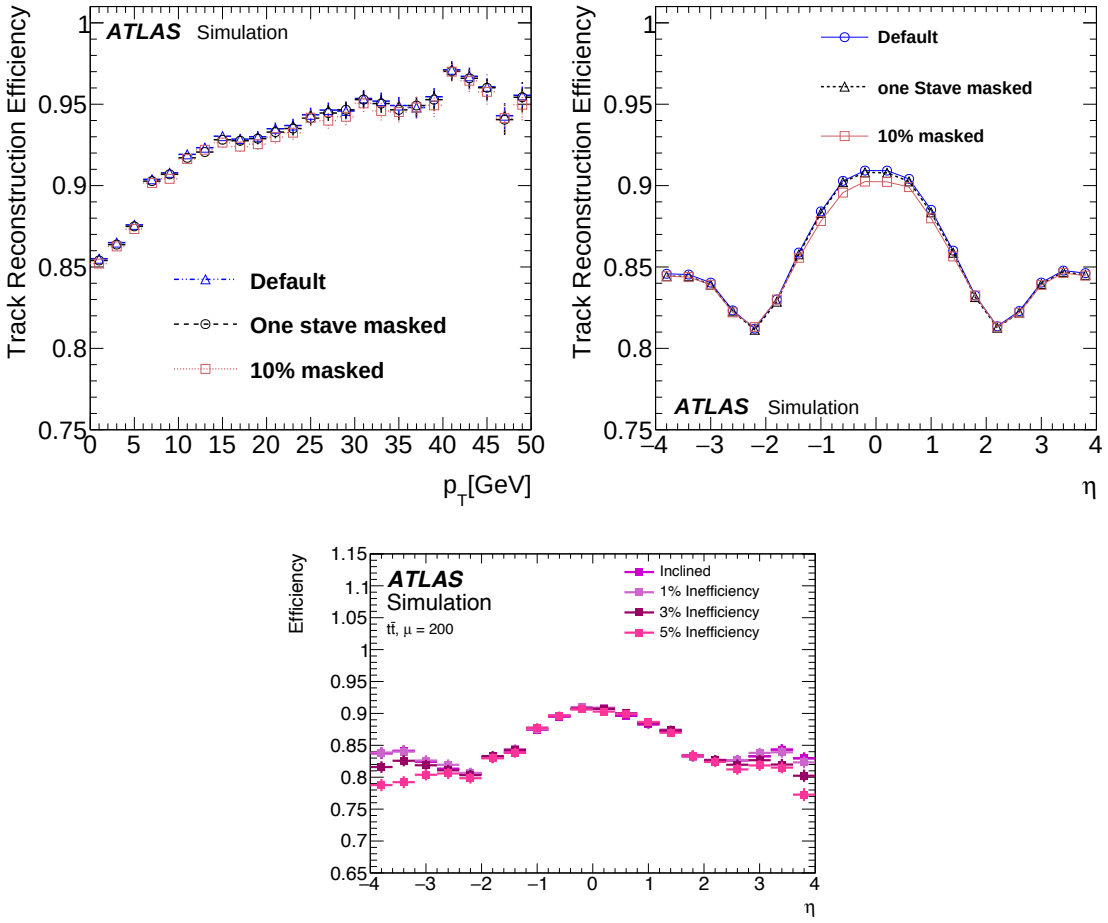


Figure 4.11: Top: Track reconstruction efficiency vs. p_{T} and η for $t\bar{t}$ events, $<\mu>$ = 200 events for no Strip modules masked and two different failure modes for SCT modules. Bottom: The track reconstruction efficiency for random inefficiencies in the Pixel detector of 1%, 3% and 5%.

Other considerations for the necessity of the present numbers of layers for the Pixel and Strip parts of the ITk were seeding discussed in Section 4.2.1 and the track triggering.

In summary, the ITk layout is adequate to achieve a basic tracking performance similar to that of Run 2. In particular, at pile-up values of 200 interactions per crossing it is imperative to require at least 9 clusters on a track to avoid suffering from significant amount of fake tracks. The layout presented here provides 13-14 hits assuming all modules are active and the sensors are 100% efficient. Even with an efficiency loss of 10% (which could occur

during the 10-year lifetime of the HL-LHC) this layout will provide sufficient redundancy to ensure that tracks can still be found with high efficiency, without creating fake tracks, and within reasonable CPU constraints. The importance of strip-based track seeds was also illustrated, and the four double-sided strip layers provide sufficient redundancy, so that strip-based track seeding can likely be used effectively throughout the HL-LHC data taking period. While this section described the generic tracking more detailed aspects such as vertexing and tracking in dense environments are described in the following sections.

4.3 Vertex Finding

4.3.1 Primary Vertex Reconstruction

Following the track reconstruction, primary vertex candidates are identified using a subset of the tracks with well-measured impact parameters and a close approach to the beam line. They are selected using the requirements in Table 4.2. The primary vertex reconstruction is performed using an iterative procedure [22]:

- Based on the tracks' longitudinal impact parameters relative to the beam spot, an initial seed vertex location is determined.
- An adaptive vertex fitting algorithm is run using all tracks, starting with the initial seed location. This algorithm iteratively reduces the weight of outlying tracks, and rejects all tracks not compatible with the vertex candidate. Tracks with higher p_T have more influence on the fit. After a fixed set of iterations, a vertex candidate is recorded if at least two compatible tracks remain.
- All tracks rejected in the previous fit are used to seed a new vertex candidate, and a new vertex fit is performed.
- This is repeated until no additional vertex can be found or no unassociated tracks remain.

Table 4.2: Requirements applied to tracks used in the vertex identification in addition to the track reconstruction requirements listed in Table 4.1.

Parameter	**Requirement**
Impact parameter w.r.t. IP	$\lvert d_0 \rvert \leq 1$ mm
Impact parameter uncertainty	$\sigma(d_0) \leq 0.35$ mm $\sigma(z_0) \leq 2.5$ mm
Impact parameter significance	$\lvert d_0 \rvert \leq 4 \cdot \sigma(d_0)$

Figure 4.12 shows the distribution of the number of vertices reconstructed per event. The simulated sample has an average pile-up value of 200, so roughly 35% of vertices are reconstructed, compared to about 50% in Run 2. In general, about 30% of the inelastic interactions are diffractive and have little activity in the central ATLAS detector. In addition, as the pile-up increases, more and more vertices are close together and get merged as is seen for Run 2 in Figure 4.12 (right), so that the number of reconstructed vertices does not increase linearly with μ. It is unclear how important it is to accurately determine the number of primary vertices since other measures can be used to determine the event-by-event pile-up. However, it is critical to reconstruct the vertex of the hard-scattering event with both high efficiency and with good resolution as this is input to the b-tagging and τ identification as well as for discriminating between prompt electrons and muons and those from to b-hadron decays.

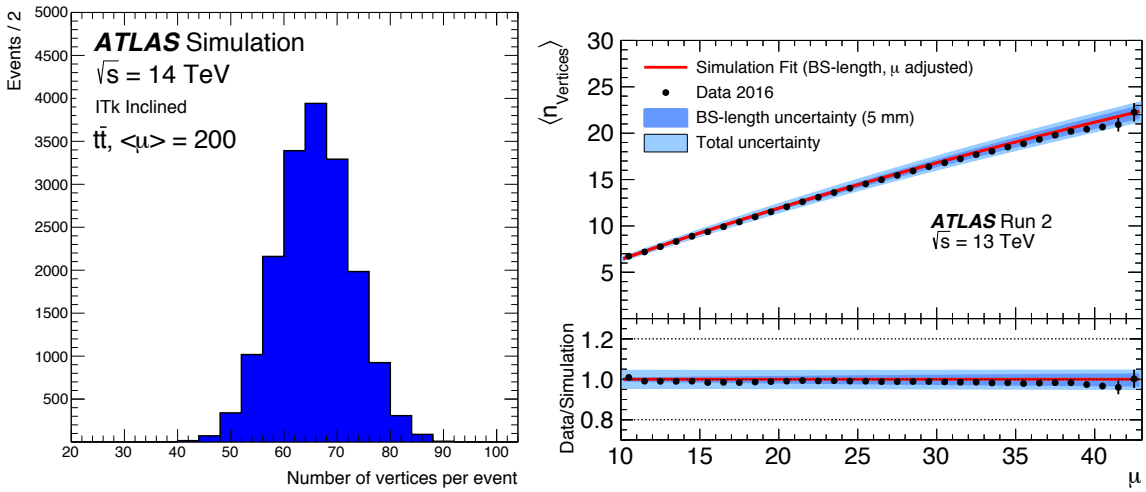


Figure 4.12: **Left:** The number of primary reconstructed vertices per event in a $t\bar{t}$ sample with average $\mu = 200$. **Right:** The number of reconstructed vertices versus μ for Run-2.

The hard-scatter $t\bar{t}$ vertex is reconstructed with an efficiency of nearly 100%. Figure 4.13 shows the transverse and longitudinal vertex position resolutions as a function of the pile-up density for the hard-scatter $t\bar{t}$ vertex. Pile-up density is defined as the number of generator-level events per mm along the z-axis. It is seen that the position resolution is independent of the local pile-up density and is just below 6 μm in the transverse and 8 μm in the longitudinal direction.

Figure 4.14 (left) shows the fraction of true hard-scatter track p_T which is correctly included in the reconstruction of the hard-scatter vertex, as a function of pile-up density. Approximately 10% of the true hard-scatter track p_T is missing from the reconstruction of the hard-scatter vertex (due partly to detector and tracking acceptance). There is no significant dependence on pile-up density. Figure 4.14 (right) shows the fraction of track p_T in the reconstructed hard-scatter vertex coming from pile-up tracks, as a function of pile-up density. As the pile-up density increases, pile-up tracks contribute relatively more of the p_T of

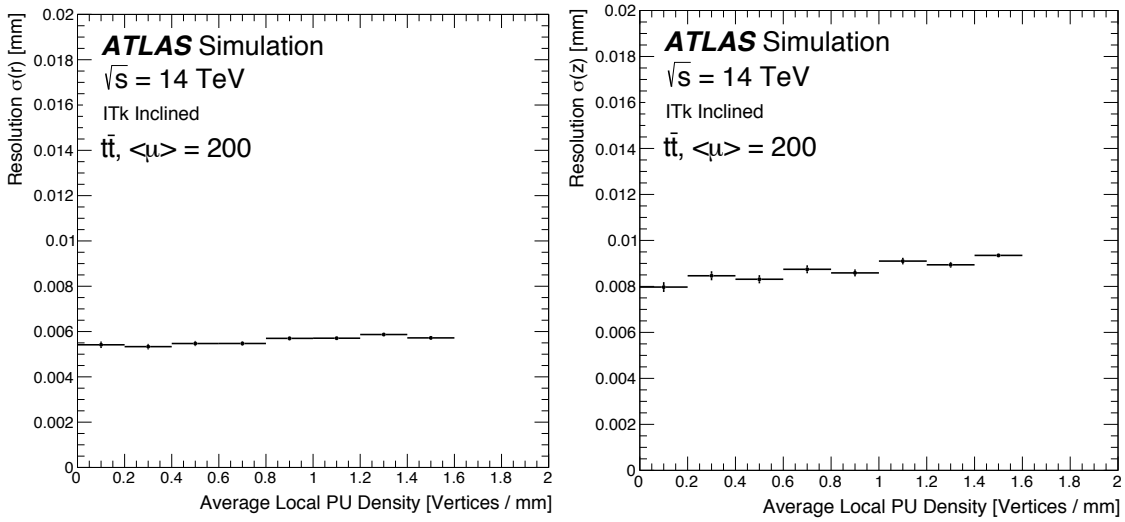


Figure 4.13: The transverse and longitudinal primary vertex resolution calculated as the difference between the reconstructed position coordinates (left) r and (right) z and their generator-level values, as a function of the pile-up density. The radial position co-ordinate is $r = \sqrt{x^2 + y^2}$, where the resolution for x and y are the same. Only hard-scatter vertices are considered.

the hard-scatter vertex, with 30% of total p_T coming from pile-up at the highest pile-up density. However, as was seen in Figure 4.13 this does not lead to a significance worsening of the resolution.

This robustness of the position against the presence of tracks from pile-up interactions is achieved since the algorithm is designed to reduce the weight for tracks that are less compatible with the primary vertex, and high-p_T tracks are weighted more than low-p_T tracks to enhance the hard scatter contributions. This is consistent with results from Runs 1 and 2.

The accurate assignment of tracks to the hard-scatter or pile-up vertices also plays an important role in the jet reconstruction, as discussed in Section 4.4.4.

4.3.2 *b*-tagging Performance

The performance of b-jet identification is characterised by the probability to identify a jet containing a b-hadron as a b-jet (b-jet efficiency) and by the inverse of the probability to identify a jet not containing a b- or c-hadron as a b-jet (light-jet rejection). The b-tagging algorithms used in ATLAS are based on multivariate techniques. For each jet, these algorithms provide a number (the b-tag weight) that is used to discriminate between b- and light-flavour jets. The values of b-jet efficiency and light-jet rejection corresponding to various minimum values of accepted b-tag weight give the b-tagging performance curve.

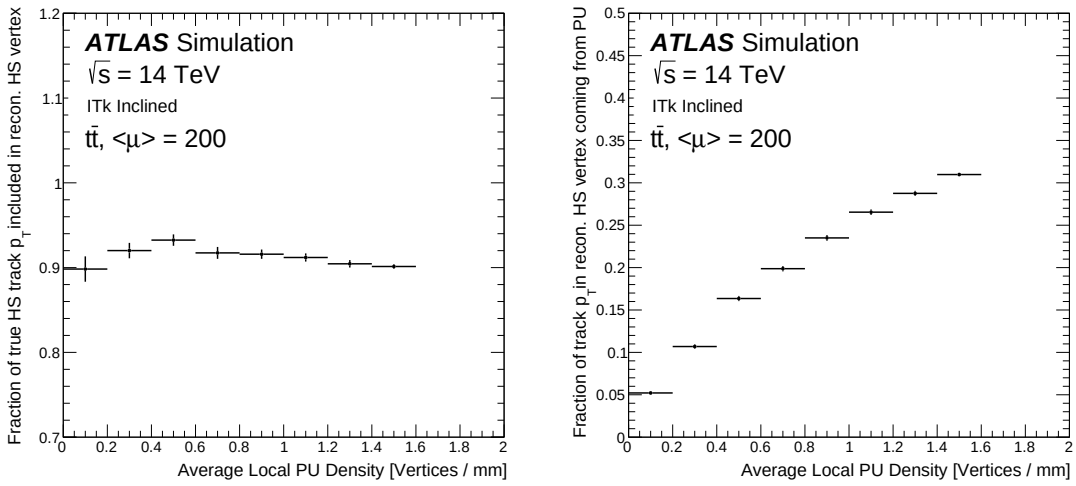


Figure 4.14: **Left:** The fraction of the total track p_T from the true hard-scatter interaction that is used in the reconstruction of the hard-scatter vertex; **Right:** the fraction of the track p_T used in the reconstruction of the hard-scatter vertex that comes from pile-up tracks.

For Run 2 three aspects of the b-tagging algorithm were tuned: 1) track selection and categorisation, 2) parameterisation of likelihoods for low-level algorithms (e.g. IP3D), and 3) training of high-level multivariate algorithms (e.g. MV1). For the ITk a re-tuning of any of these aspects was not performed but the algorithms were used as tuned for Run 2. Consequently, the performance is not optimal, in particular for $|\eta|$ >2.7 where the tracking resolution and environment is very different from the central region. However, it is still useful to understand what is expected for the minimum performance of the b-tagging with ITk.

The following results were obtained using $t\bar{t}$ events for jets matched to partons from the top quark decays. The jets are labelled b or light, based on the presence (absence) of b- (b- or c-) hadrons within a cone of $R = 0.3$ around the jet axis [23].

Figure 4.15 (top) shows the light-jet rejection versus the b-tagging efficiency obtained for two different b-tagging algorithms: IP3D and MV1 [24]. Both algorithms explore primarily the consistency of individual tracks with coming from the primary hard scatter vertex, and based on these inputs provide a single variable that can be selected on. MV1 uses IP3D as input in addition to an algorithm searching explicitly for secondary vertices. For an efficiency value of 70% for MV1, rejection factors are about 1000 and 10 are observed for $|\eta| < 2.7$ and $2.7 < |\eta| < 4$, respectively. For IP3D the values are lower as it uses less information. The Run 2 curve for rejection versus efficiency is also shown for MV1. For a 70% efficiency the rejection factor for ITk is about a factor two better than for Run 2.

It is interesting that even in the very forward region there is significant discrimination

power. This can be exploited e.g. to discriminate b-jets in $t\bar{t}$ events from jets in vector-boson-fusion processes (see Section 4.6).

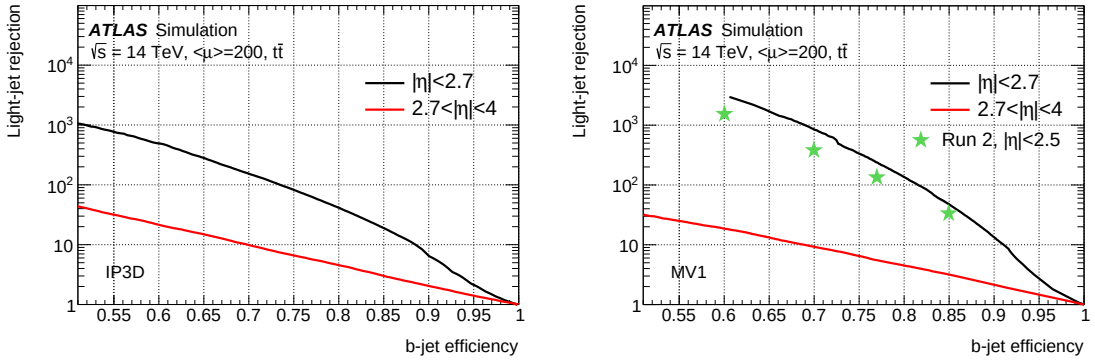


Figure 4.15: Performance of the IP3D (left) and MV1 (right) b-tagging algorithms for the ITk layout for two η ranges. For comparison purposes, the performance of the MV1 algorithm for ATLAS during Run 2 is shown as stars.

4.4 Tracking Performance for electrons, photons, taus, jets and missing transverse energy

Good tracking performance is essential for many higher level physics objects that are reconstructed within the ATLAS detector. In this section the performance of the reconstruction of electrons, photons, taus, jets and missing transverse energy is discussed.

4.4.1 Electron Performance

In comparison with the Run 2 configuration, the improved tracking, the absence of the transition radiation detector, and the increased pile-up require a new optimisation of the electron identification algorithm. A cut-based identification algorithm has been developed with three working points for the electron efficiency, referred to as Loose, Medium, Tight, with increasing rejection of backgrounds. The identification requirements vary according to the transverse energy and pseudorapidity of the electron candidate. The samples used for this analysis use the inclined ITk layout, and are evaluated for μ in the range 190-210. A $Z \rightarrow ee$ MC sample is used for the prompt electrons, and di-jet MC samples are used to study background electrons. For all studies, a p_T cut for reconstructed electrons of 7 GeV is applied, and all studies presented here only concern the region $|\eta| < 2.5$ as significant new optimisation is needed in the forward region to exploit the ITk for electron ID.

The efficiency of electron reconstruction, consisting of the electromagnetic cluster reconstruction, the track reconstruction, the cluster-track matching, and track-quality requirements, is evaluated using the $Z \rightarrow ee$ MC sample. The cluster reconstruction efficiency is (99.8±0.1)%; while the track matching efficiency is (97.7±0.1)%; and the efficiency of the track-quality requirements is (98.6±0.1)%. In addition to the tracking cuts in Table 4.1, the impact parameter significance, $d_0/\sigma(d_0)$ is required to be below 10 to ensure the electrons are consistent with coming from the primary hard scatter vertex.

The main backgrounds are evaluated using a di-jet sample, and are collectively referred to as "jet fakes". The main background sources are charged hadrons misidentified as electrons, photons converting in the detector material, and electrons from semi-leptonic decays of b- or c-hadrons. Photon conversions and electrons from b/c-hadrons are primarily rejected using track-based variables, while for charged pions, calorimeter-based variables are more effective as the shower shape is expected to be less compact and significant energy deposits in the hadronic part of the calorimeter are expected.

Table 4.3 shows the identification efficiency of the three identification working points for prompt electrons from Z boson decays and for the three background categories and their combined value. The total efficiencies are also shown, including both reconstruction and identification. It is seen that the jets are suppressed by a factor of 600-3000 for efficiencies between 89 and 63%, depending on the working point. This is similar to what was achieved with a cut-based approach in Run 1 [25].

In Run 2 a likelihood based electron identification is used, combining the many calorimeter and track variables into a single discriminant. This results in an improvement of about a factor of 2-5 in rejection of jets [25]. It is expected that such a development will also be carried out for the ITk and will result in similar performance gains.

In Figure 4.16 the overall efficiency to reconstruct and identify generator-level isolated electrons is given. Figure 4.17 shows the probability to misidentify generator-level jets as electrons, where generator-level jets are reconstructed from generator-level particles using the anti-k_t algorithm with an R parameter of 0.4 and requiring $p_T^{jet} > 5$ GeV.

The electron efficiency is relatively flat in both p_T and η except near $|\eta| = 1.5$ and $|\eta| = 2.5$ where there are boundaries between sub-detectors in the calorimeter system. The efficiency for jets is also rather independent of η but has a significant dependence on p_T and is highest near 50 GeV. The decrease of the fake rate towards low truth-jet p_T is due to the $p_T > 7$ GeV requirement: as the truth-jet p_T decreases it becomes less likely that an electron candidate with $p_T > 7$ GeV is reconstructed.

Finally, the charge misidentification rate for electrons identified at the medium working point is shown as a function of E_T and η in Figure 4.18. It is below 10^{-3} in the central region and increases to nearly 1% at high η. Compared to Run 2 it is significantly reduced particularly in the forward region due to the lower amount of material and the improved momentum resolution of the ITk.

Table 4.3: Efficiencies to successfully identify generator-level electrons and the probabilities to misidentify generator-level jets as electrons (jet fakes), for the Loose, Medium and Tight electron identification working points. Also shown are the efficiencies for electron fakes coming from hadrons, electrons from photon conversion, and electrons from heavy-flavour hadron decays. The bottom table gives the total efficiency, including both reconstruction and identification. The statistical errors on the efficiencies are also shown.

μ =190-210	Loose	Medium	Tight
	Identification Efficiency (%)		
Electrons	92.4±0.1	85.2±0.1	65.3±0.1
Jet Fakes	6.2±0.2	2.7±0.1	0.9±0.1
Hadrons	5.0±0.1	2.0±0.1	0.72±0.04
Conversions	10±2	4.4±1.5	0.6±0.5
Heavy Flavour	42±6	23±5	11±3
	Total Efficiency (%)		
Electrons	88.9±0.1	82.0±0.1	62.8±0.1
Jet Fakes	0.150±0.005	0.065±0.003	0.022±0.002

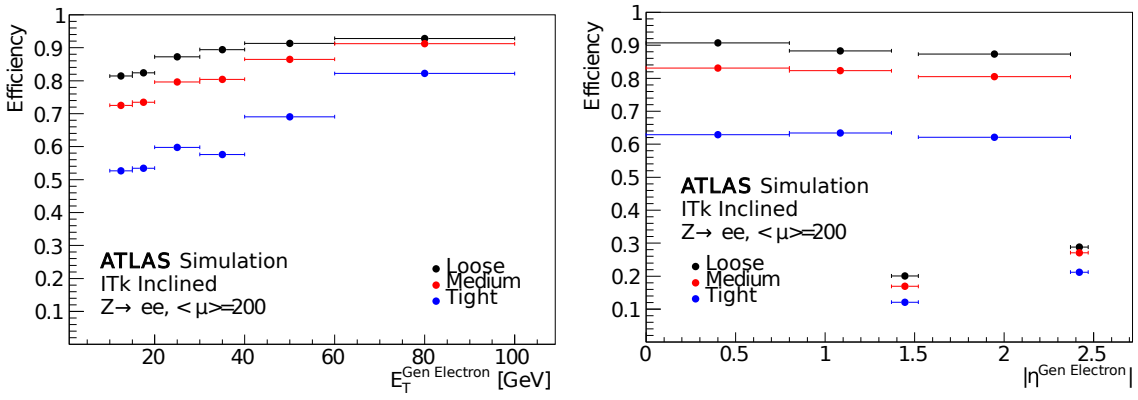


Figure 4.16: The electron selection efficiency (relative to generator-level and including both reconstruction and identification) as a function of E_T (left) and $|\eta|$ (right).

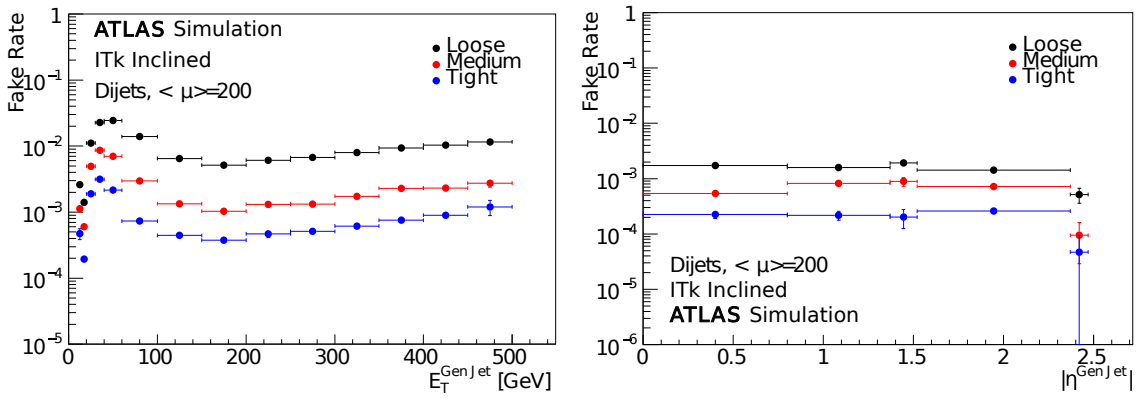


Figure 4.17: The efficiency (relative to generator-level) with which jets are reconstructed and identified as electrons as a function of E_T (left) and $|\eta|$ (right).

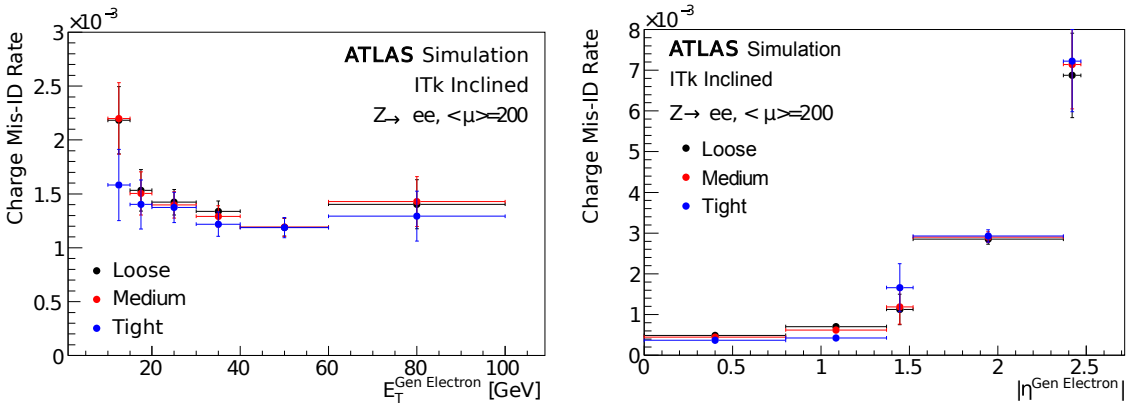


Figure 4.18: The charge misidentification rate for electrons as a function of E_T and $|\eta|$.

4.4.2 Photon Performance

Reconstructing converted photons is important for two reasons. Firstly, it increases the signal-to-background ratio for processes with photons as it provides additional means to reject prompt and heavy-flavour electrons. Secondly, it improves the photon energy resolution since converted photons require a larger energy correction. If a converted photon is treated as unconverted the energy resolution is 50% worse. In particular the $H \to \gamma\gamma$ process benefits from a dedicated photon conversion reconstruction and calibration.

For photons, the amount of material traversed increases the probability for a photon to convert into an electron–positron pair within the acceptance. In addition, the choice of the layout affects the efficiency to reconstruct the photons that have converted. A conversion track-finding algorithm has been developed for the ITk based on the Run 1 and Run 2 experience. This new algorithm runs after the default track-finding algorithm, and considers

any unused clusters to build tracks with loosened requirements. In particular, instead of 9, only 6 silicon clusters are required, the d_0 requirement is loosened, and tracks may begin at a larger radius than a standard track (see Table. 4.4). The reconstructed conversion candidates may involve either a single track or two tracks. This algorithm has only been developed for tracks with $|\eta| < 2.7$, and thus no results for the very forward region are presented.

Table 4.4: Set of requirements applied during the dedicated conversion track-finding reconstruction pass.

Variable	Requirement
Pixel+Strip clusters	≥ 6
Holes	$= 0$
p_T [MeV]	> 900
$\|\eta\|$	≤ 2.7
$\|d_0\|$	≤ 10 mm
$\|z_0\|$	≤ 12.5 cm

The cumulative probability for photon conversion as a function of radius obtained using a sample of VBF $H \to \gamma\gamma$ is shown in Figure 4.19. The probability for a photon in the central barrel region $|\eta| < 1.0$ (barrel–end-cap transition region $1.52 < |\eta| < 2.37$) to convert within a radius of 1.0 m from the interaction point is approximately 12% (36%) for the ITk layout, compared to 32% (62%) for Run 2 .

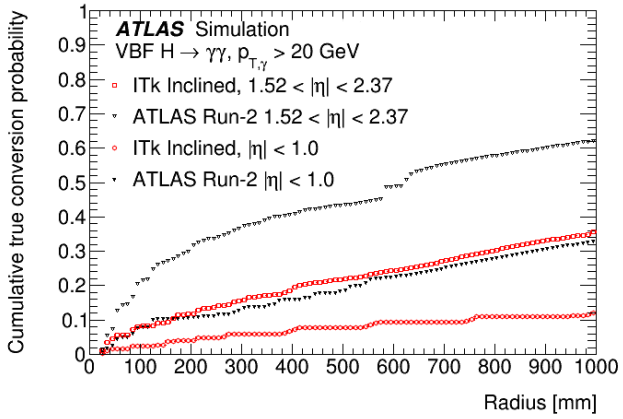


Figure 4.19: The cumulative probability of conversion, per photon, as a function of radius for the ITk and Run 2 layouts. It is shown separately for photons in the central barrel region $|\eta| < 1.0$ and the barrel–end-cap transition region $1.52 < |\eta| < 2.37$. The results are derived using VBF $H \to \gamma\gamma$ events.

The dedicated photon conversion reconstruction algorithm identifies a pair of tracks, consistent with coming from a massless particle, or a single track consistent with a photon

conversion. For two-track conversions, the radius is taken to be the fitted vertex of the two tracks, for single-track conversions, it is the most inner layer where a silicon cluster is assigned to the track candidate. If a cluster of cells in the electromagnetic calorimeter is matched to a track associated with a conversion vertex it is considered as a converted photon candidate. The distributions of the vertex radius for reconstructed and true photon conversions are shown in Figure 4.20. The spikes in the distribution correspond to the beampipe, the detector layers and support structures. The conversion reconstruction efficiency is also shown. It is defined as the ratio of reconstructed to true conversions. This efficiency is above 90% for photons that convert earlier in the detector, up to a radius of 40 cm, corresponding to the first layer of the silicon strip detector. At higher radii the efficiency falls rapidly, primarily due to the requirement of at least six silicon hits. The performance with no additional pile-up interactions is shown but studies demonstrate that the performance at $\langle\mu\rangle$= 200 is similar.

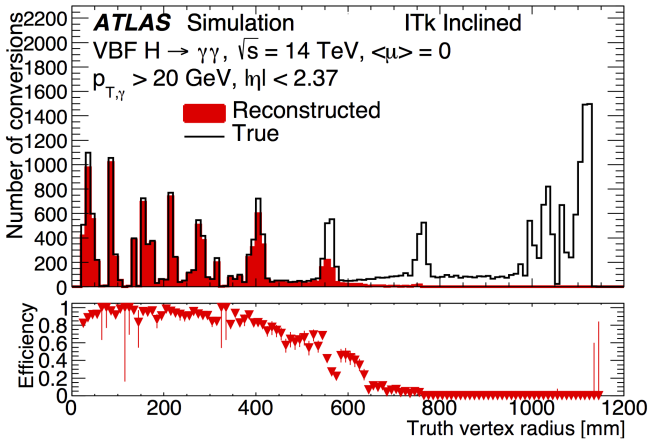


Figure 4.20: Distributions of true conversion radius for reconstructed (red) and true (black) converted photons with $|\eta|$ <2.37 (top panel). The bin-by-bin ratio gives the conversion reconstruction efficiency as a function of true radius (bottom panel). The results are derived using VBF $H \rightarrow \gamma\gamma$ events.

4.4.3 Tau Performance

An important part of the physics programme at the ATLAS experiment uses tau leptons for Standard Model measurements and searches for new phenomena. The τ-leptons decay hadronically (one or three charge pions plus neutral particles) 65% of the time and decay to electron or muon plus neutrinos 35% of the time. For leptonic decays of τ-leptons to muons or electrons, the efficiencies are discussed in Sections 4.2.3 or 4.4.1, respectively. In this section, the focus is on hadronic decays of τ-leptons.

The presence of one or three charged particles, together with a neutrino and possibly neutral pions, is characteristic of hadronic τ lepton decays. The visible decay products (here-

after denoted as $\tau_{\text{had-vis}}$) are reconstructed using an algorithm seeded by jets with $p_T > 10$ GeV. A $\tau_{\text{had-vis}}$ candidate must have $p_T > 20$ GeV, one or three associated tracks, an electric charge of ± 1, and depositions of energy greater than 10 GeV in the calorimeters in the range $|\eta| < 4.0$. The hadronic tau reconstruction efficiency is about 60%, in the region $|\eta|$ <2.5 for taus with p_T> 20 GeV. A Boosted Decision Tree (BDT) multivariate identification procedure is used for the discrimination of backgrounds from jets, exploiting the track properties, calorimetric shower shapes, and combined variables of the $\tau_{\text{had-vis}}$ candidates. Three different identification criteria are evaluated for one-prong (three-prong) $\tau_{\text{had-vis}}$ candidates, with efficiencies measured in $Z \to \tau^+\tau^-$ decays of approximately 85% (75%) for the Loose benchmark, 75% (60%) for the Medium benchmark and 60% (45%) for Tight. The BDT used is described in Ref. [26]. It was designed to provide efficiencies which are independent of p_T and μ. This algorithm has yet to be optimised for ITk.

The hadronic tau identification efficiency is defined as the number of reconstructed taus passing the BDT selection cut (Loose, Medium or Tight), divided by the total number of reconstructed tau candidates. The reconstructed taus (both in the numerator and the denominator) are matched to Monte Carlo truth. Figures 4.21 and 4.22 summarise the hadronic tau identification efficiencies for one-prong and three-prong taus with the ITk layout for each of the Loose, Medium and Tight efficiency selections. It is seen that the efficiency is stable as a function of p_T up to 2 TeV for both one- and three-prong τ-leptons. As a function of η it is rather flat for $|\eta| < 3$ for one-prong candidates and then falls rapidly. For three-prong candidates the efficiency starts to decrease at $\eta \approx 1.5$. At high p_T it is challenging to reconstruct τ-leptons as they are very collimated and the individual tracks often overlap for the three-prong case. A more detailed discussion of this challenge and how the chosen layout was optimised to ensure that nearby tracks can be resolved is presented in Section 4.5.

The fake rate is defined as the number of reconstructed jets with one (three) track(s) that pass the specified selection cut, divided by the total number of reconstructed jets with one (three) track(s). The fake rates are shown as a function of p_T in Figure 4.23, again for each of the three selection cuts and for both one-prong and three-prong taus, respectively. While the three-prong fake rate is rather flat there is a sudden increase at $p_T \approx$ 150 GeV for one-prong τ candidates. This increase is due to the imperfect training of the BDT in the high-p_T region, and can likely be further reduced when a dedicated training of the high-p_T regime is performed to address this.

A plot of the jet rejection (given by the inverse of the fake rate) versus the signal efficiency is shown in Figure 4.24. The hadronic tau identification efficiencies with the ITk are quite similar to those achieved in Run 2, but the ITk covers a broader η range. For an 80% efficiency, a rejection of a factor of 40 is achieved.

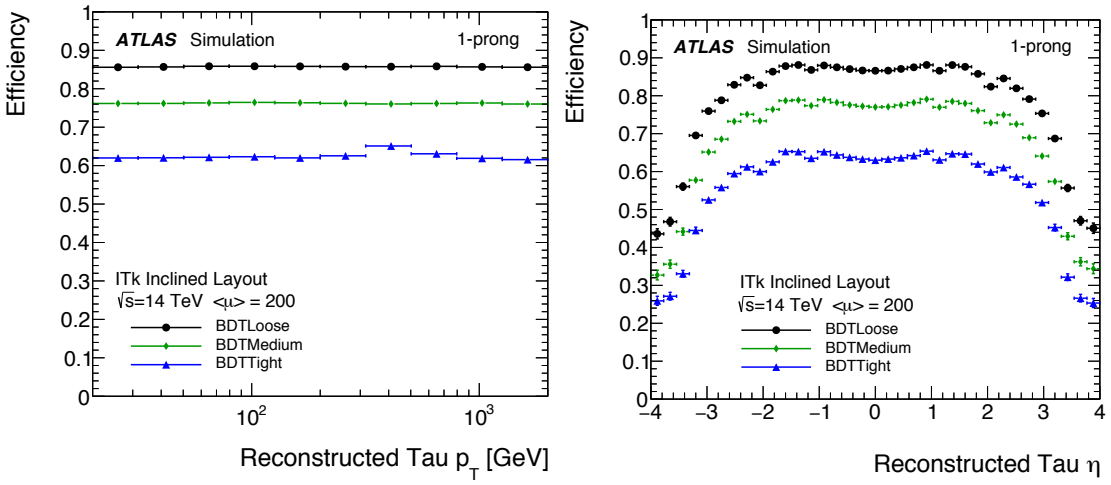


Figure 4.21: Hadronic tau identification efficiencies for 1-prong tau decays with the ITk layout, shown as a function of p_T and η. Results are shown for the Loose, Medium and Tight selections.

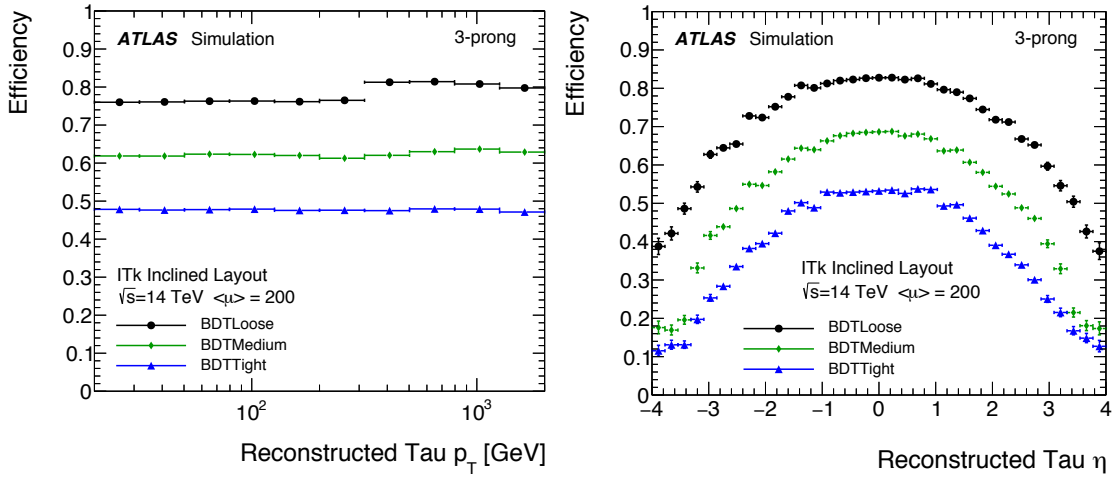


Figure 4.22: Hadronic tau identification efficiencies for 3-prong tau decays with the ITk layout, shown as a function of p_T and η. Results are shown for the Loose, Medium and Tight selections.

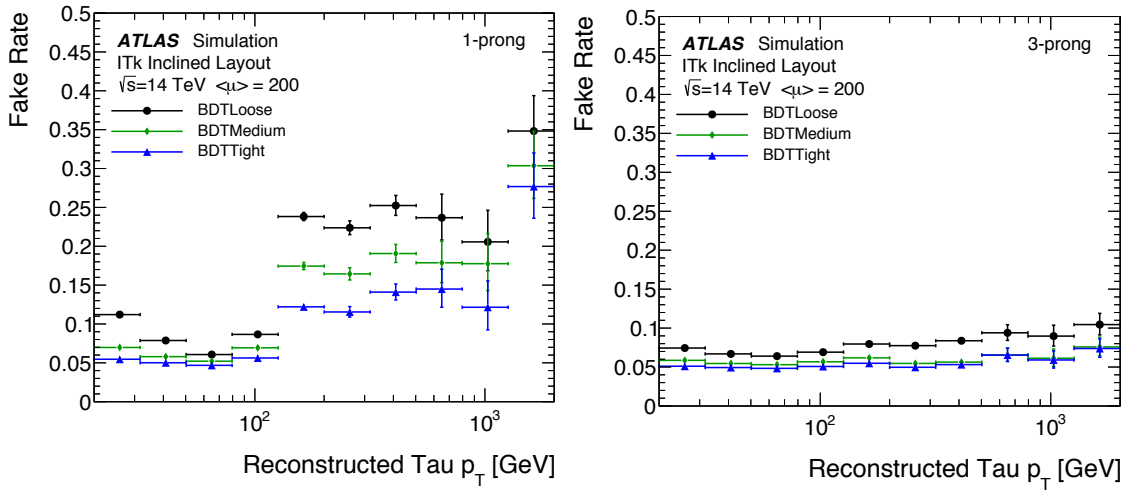


Figure 4.23: Tau fake rates for 1-prong and 3-prong tau decays, shown as a function of p_T. Results are shown for the Loose, Medium and Tight selections. A feature of the BDT is responsible for the increase in the fake-rate for hadronic tau candidates with a p_T greater than $\sim$ 100 GeV.

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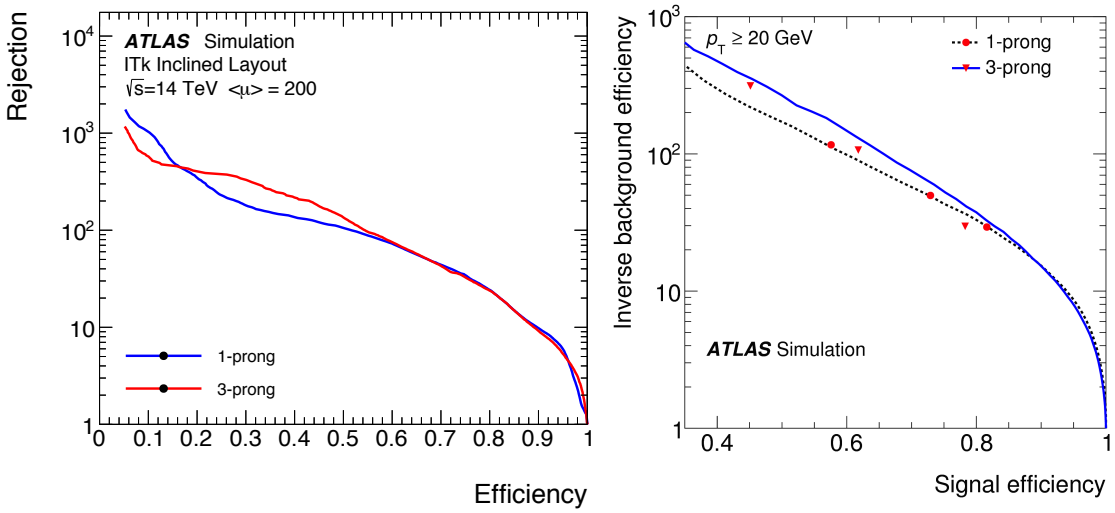


Figure 4.24: Rejection factor for fake taus as a function of the tau identification efficiency for the ITk layout (left) and at the beginning of Run 2 (right) [26]. Curves for one-prong and three-prong hadronic tau performance are shown separately. Reconstructed hadronic tau candidates with $p_T >$ 20 GeV in the region $|\eta| < 4.0$ are included for ITk. For Run 2 the η range is restricted to $|\eta| < 2.5$.

4.4.4 Jet and $E_{\mathrm{T}}^{\mathrm{miss}}$ Performance

Tracks, and their vertex association information, can be used to mitigate pile-up effects in the jet and $E_{\mathrm{T}}^{\mathrm{miss}}$ reconstruction. During Runs 1 and 2, ATLAS developed several jet vertex-tagging methods to identify and remove pile-up jets [27, 28]. A major limitation of the current track-based pile-up suppression methods for jets is that they are not applicable to jets outside the inner tracker detector acceptance. The extension from the current $|\eta| < 2.5$ tracker acceptances to $|\eta| < 4$ of the ITk will enable these techniques to be employed in the forward region to reject jets due to pile-up interactions.

This section considers the discriminant R_{pT}, defined as the scalar sum of the p_T values of all tracks that are inside the jet cone and originate from the hard-scatter vertex PV_0, divided by the fully calibrated jet p_T :

$$R_{\mathrm{pT}} = \frac{\Sigma_k p_{\mathrm{T}}^{\mathrm{trk}_k}(\mathrm{PV}_0)}{p_{\mathrm{T}}^{jet}} \tag{4.3}$$

The tracks used in the R_{pT} calculation fulfil the quality requirements defined in Ref. [29] and are required to have a $p_T >$ 1 GeV. The distance between the hard-scatter vertex and the z_0 impact parameter of the tracks used in the R_{pT} calculation is required to be within 1 mm and 4 mm, depending on the $|\eta|$ of the track. Small values of R_{pT} correspond to jets with a small charged particle p_T fraction originating from the hard scatter vertex PV_0 and therefore are likely to be pile-up jets.

The η distribution for jets from pile-up interactions is shown in Figure 4.25 before and after the pile-up suppression algorithm is applied. It is seen that the number of pile-up jets is reduced by about a factor of 50 for the rejection cut chosen. The efficiency for pile-up jets as a function of the efficiency for hard-scatter jets with $20 < p_T < 40$ GeV, in three different $|\eta|$ regions, using the R_{pT} discriminant in Pythia8 dijets events with $\langle\mu\rangle$ = 200, is shown in Figure 4.25. It is seen that even at high η, beyond the present tracker acceptance, a good discrimination is achieved. In the physics benchmark studies presented in Section 4.6, a pile-up jet efficiency of 2% (i.e. a rejection of 50) is assumed, corresponding to a jet selection efficiency of 86% for $|\eta| < 1.5$ and 80% for $|\eta| > 2.9$.

In ATLAS, $E_{\mathrm{T}}^{\mathrm{miss}}$ is computed as the vector momentum sum of high p_{T} physics objects in the event, plus a soft-term component, from particles which do not constitute high-p_{T} objects. The soft-term component is computed using tracks assigned to the hard-scatter vertex [30]. The disadvantage of using tracks is that the neutral particles are not accounted for, and that charged particles are only accounted for if they are within the tracker acceptance. However, the ATLAS LAr calorimeter has the disadvantage that it has a relatively slow response time of 600 ns, and thus the calorimeter signal is integrated over 24 bunch crossings. The pile-up interactions in the adjacent bunch-crossings to the hard scatter are referred to as out-of-time pile-up, and further degrade the $E_{\mathrm{T}}^{\mathrm{miss}}$ resolution, so that it is advantageous to use a track-based $E_{\mathrm{T}}^{\mathrm{miss}}$ calculation for the soft-term component [31].

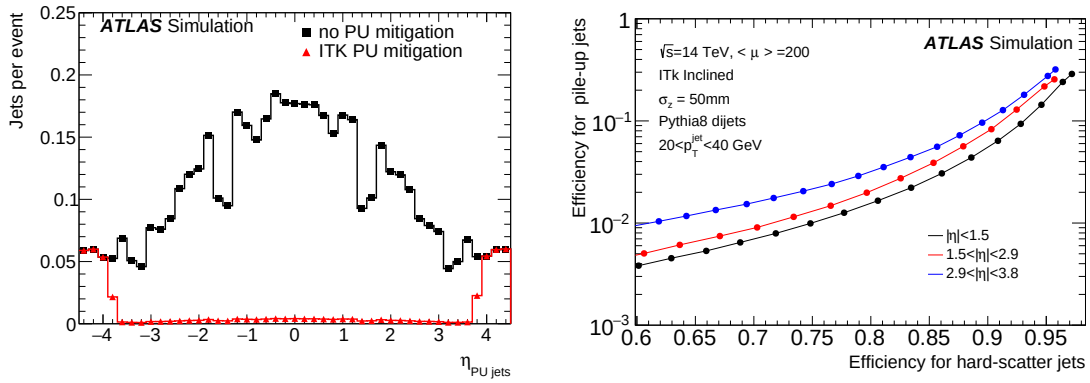


Figure 4.25: **Left:** The η-distribution of jets from pile-up interactions with and without the extended ITk coverage. **Right:** The efficiency for pile-up jets as a function of the efficiency for hard-scatter jets with $20 < p_{\mathrm{T}} < 40$ GeV.

In this analysis $E_{\mathrm{T}}^{\mathrm{miss}}$ is reconstructed using selected muons, with $p_{\mathrm{T}} > 2.5$ GeV or $p > 4$ GeV, electrons with $p_{\mathrm{T}} > 10$ GeV and jets with $p_{\mathrm{T}} > 20$ GeV, satisfying a requirement of $R_{\mathrm{pT}} > 0.1$ and hence compatible with originating from the hard-scatter vertex. Tracks coming from the hard-scatter vertex, with $p_{\mathrm{T}}^{\mathrm{trk}} > 1$ GeV and $|\eta^{\mathrm{trk}}| < 4$, not associated to muons, electrons and jets, are used to reconstruct the soft-term component of the $E_{\mathrm{T}}^{\mathrm{miss}}$. Figure 4.26 shows the resolution of the x- and y-components of the $E_{\mathrm{T}}^{\mathrm{miss}}$ as function of the number of primary vertices using track information for $|\eta|$ <2.7 (red) and using this information for $|\eta|$ <4.0 (black) for samples of Powheg+Pythia $t\bar{t}$ events with $\langle\mu\rangle$=200.

It is seen that the resolution is about 30% better when using tracks up to $\eta = 4.0$. This improvement is primarily explained by the removal of forward pile-up jets [7]. There is also a small improvement from extending the measurement of the soft-term component of the $E_{\mathrm{T}}^{\mathrm{miss}}$ out to $|\eta| < 4.0$.

4.5 Tracking in Dense Environments

The higher integrated luminosity of the HL-LHC allows higher p_T final states to be studied in more detail, increasing the sensitivity to higher mass particles. At high transverse momenta, the final states are very collimated and the separation between individual charged particles is approaching the resolution of the pixels in the Inner Detector. The physics objects affected are 3-prong decays of τ -leptons as well as quarks hadronising to form jets in the detector.

[7] For the tracker with $|\eta| < 2.5$ it happens that a central pile-up jet is removed but the corresponding other jet from that pile-up interaction is forward and not tagged, thus leading to $E_{\mathrm{T}}^{\mathrm{miss}}$. With the extended tracker acceptance this problem is much reduced.

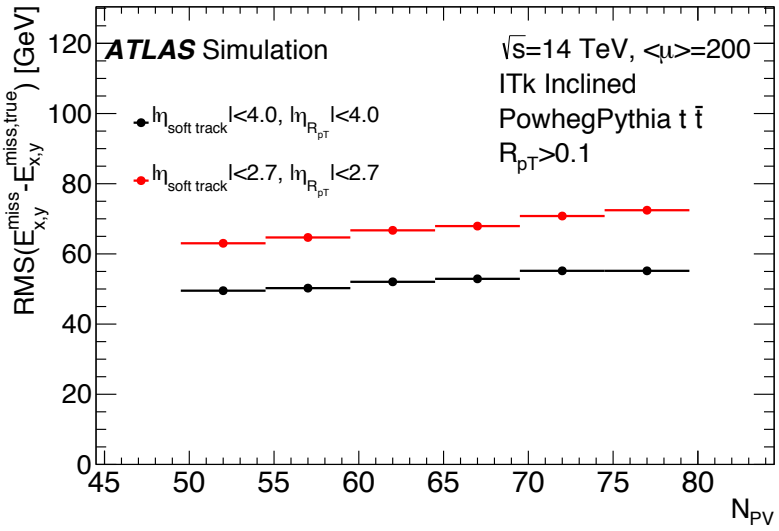


Figure 4.26: The resolutions of the x and y components of $E_{\mathrm{T}}^{\mathrm{miss}}$ for the $|\eta|$ <2.7 (red) and $|\eta|$ <4.0 (black) Inner Tracker acceptance ranges for samples of Powheg+Pythia $t\bar{t}$ events with $\langle\mu\rangle$=200, as a function of the number of reconstructed primary vertices.

Furthermore, the increased pile-up contributes to the event density, and compared to Run 2, it becomes more likely at HL-LHC that particles from the primary interaction deposit charge in the silicon sensors which is clustered together with that from particles produced in pile-up interactions. The ITk must be able to cope with these environments and reconstruct tracks from 3-prong τ's and jets at an acceptable rate such that the discovery potential for high-mass particles remains as high as possible.

For the tracking performance in dense environments the entire inner detector layout is of concern — many high-momentum decay products can have a separation smaller than a single detector element even at the large radius of the strips. Because of this, it is imperative to ensure the design of the entire detector is consistent with a tracking performance in dense environments that fits in with the physics goals of ATLAS at the HL-LHC. Since the hit information in the strip detector is digital, it is not possible to reliably resolve whether a cluster is made from hits due to the incidence of a single particle or of multiple particles. In the pixel detector the charge information can be used to resolve this, as done already in Runs 1 and 2. This is one of the primary motivations for favouring pixel layers to strip layers, as any additional layer provides additional separation. This is important, in particular when considering that during the HL-LHC lifetime individual modules may fail so that in a given ϕ region intersected by the track only 3-4 modules instead of the nominal 5 operate efficiently.

A set of dense environment goals were set out as recommendations for good performance in these conditions. The samples used for these studies were single τ-lepton decay to 3

charged pions, with a flat spectrum in transverse momentum, and a 5 TeV $Z' \rightarrow t\bar{t}$ sample. The single-τ sample is useful for judging the two and three-particle separation performance, and the heavy Z' is useful to evaluate the performance in highly collimated jets.

For this study the usage of analog charge information and an advanced algorithm to determine if a cluster might come from one or more particles is critical. Since no such algorithm for the ITk exists yet, it is assumed that the performance obtained with the Run 2 IBL can be achieved, and this is parameterised for the following studies.

4.5.1 Single tau

A single τ lepton decay to three charged pions is used for studying track reconstruction efficiency in dense environments. The track reconstruction efficiency is defined as the proportion of events where three tracks that are truth-matched (as described in Section 4.2.3) with the pions from the τ decay are accepted as good tracks. A good track is defined as one accepted in the ambiguity solver, with the implicit cuts this entails [32]. The ambiguity solver is a tool in track reconstruction which has been optimised in order to reject tracks which share too many hits with other tracks, as the number of shared hits, when multiple tracks share one cluster, is often an indication of a fake track. As such, the ambiguity solver acts as a first and effective selector of tracks after the seed finding process (see Section 4.2.1).

The efficiency for reconstructing all three tracks in a 3-prong τ-decay is shown in Figure 4.27 for the $\langle\mu\rangle = 200$ single τ lepton sample, for the ITk layout. A minimum cut on track p_T of 2 GeV is used, as well as a minimum cut on truth τ lepton p_T of 25 GeV. The tracks are also required to satisfy the criteria given in Table 4.1. It is seen that the efficiency stays relatively constant up to $p_T \approx$ 1 TeV for $\eta < 2.7$ and then falls significantly towards higher p_T. For the more forward region ($2.7 < |\eta| < 4.0$), it already starts to fall at $p_T \approx$ 600 GeV. The decrease is due to the increasing collimation of the τ-lepton decay products at high p_T and leads to the tracks sharing clusters, as discussed above. In addition, with increasing p_T, the τ-lepton's time-of-flight increases so that the impact parameter requirements in Table 4.1 are less efficient and no hits are present in the most inner layer, if the decay occurs at larger radius [8)] The efficiency is highest at lower $|\eta|$ showing good performance up to 2 TeV. Since τ-leptons from decays of high-mass particles are mostly central, this is the most important kinematic region.

In Section 3.1 it was discussed that the track reconstruction in 3-prong tau decays benefits from the presence of five pixel layers (see Figure 3.3), particularly when considering that individual modules can fail or layers can be affected by radiation damage towards the end of the HL-LHC period. At very high p_T, clusters are also merged in the strip detector and, since this detector is read out digitally, the information carried by the clusters is very ambiguous and cannot easily be used to resolve whether the cluster is merged or not.

[8] For instance for a τ with p_T=1 TeV 50% of the decays occur at a radius of 5 cm or beyond.

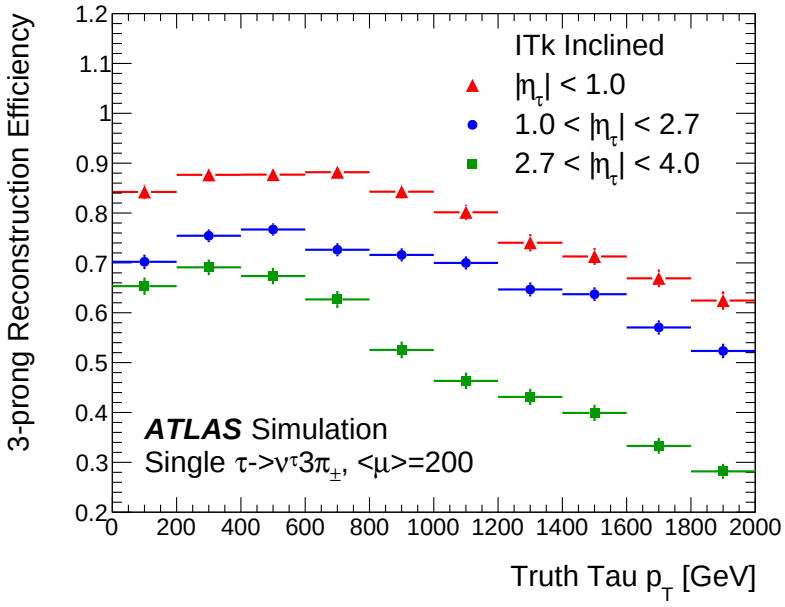


Figure 4.27: Efficiency to reconstruct tracks from all three charged pions in a 3-prong τ decay, as a function of the τ lepton p_T , in the central region $|\eta| < 1.0$, barrel–end-cap transition region $1.0 < |\eta| < 2.7$, and forward region $2.7 < |\eta| < 4.0$ for the ITk layout. Each truth pion of the τ lepton decay is required to be matched to a distinct reconstructed track with $P_{\text{match}} > 0.5$, based on the hits of the track. A minimum cut on track p_T of 2 GeV is used, as well as a minimum cut on truth τ lepton p_T of 25 GeV.

4.5.2 Jets in $Z' \rightarrow t\bar{t}$ Events

The two highly-boosted top quarks from the $Z' \rightarrow t\bar{t}$ samples will each produce a b-quark and W boson. Two thirds of the W-bosons decay to a $q\bar{q}$ pair, so that after parton showering and quark hadronisation, the final state consists of three jets (incl. one b-jet) related to each original top quark. As the top quark p_T increases, its boost increases and the three jets become more and more collimated. In addition the $c\tau$ of the b-hadron decay increases with increasing boost. For a 1 TeV b-hadron typically 50% decay at a radius of 10 cm or beyond, and thus miss the two inner layers of the pixel detector.

The reconstruction of charged particles inside these events, especially in the core of the jet, is an excellent performance indicator for dense environments in the ITk, and allows a study of both b-jets and light jets in dense environments.

For all subsequent studies, truth jets are found using a truth-based [9)] anti-k_t algorithm with an R parameter of 0.4. Jets are accepted up to $|\eta| < 4.0$, and from a p_T of 25 GeV up to 4 TeV. Truth particles are identified if they are charged, stable and primary hadrons, are within a cone of $\Delta R = 0.4$ around the jet-axis and have $p_T >$ 2 GeV.

[9] This includes all primary truth particles, except neutrinos and muons.

All good reconstructed tracks, using the selection cuts specified in Table 4.1, that are matched to truth particles within that jet, with a truth matching value of $P_{\text{match}} > 0.5$, and whose truth matched particles also meet the above criteria, are also selected. Then, the track reconstruction efficiency is found using the definition in Equation 4.2 in Section 4.2.3.

In the first study, the track reconstruction efficiency is found as a function of the truth jet p_T. This is shown in Figure 4.28. There is no decrease of efficiency observed in any of the η-ranges up to $p_T \approx$ 3 TeV. The efficiency for ATLAS Run 2 conditions is also included in Figure 4.28 (right) for the baseline reconstruction (Baseline) and the algorithm optimised for tracking in dense environments (TIDE). It is seen that in Run 2 the efficiency dropped significantly, starting already at 0.4 TeV, before the specific TIDE optimisation was performed.

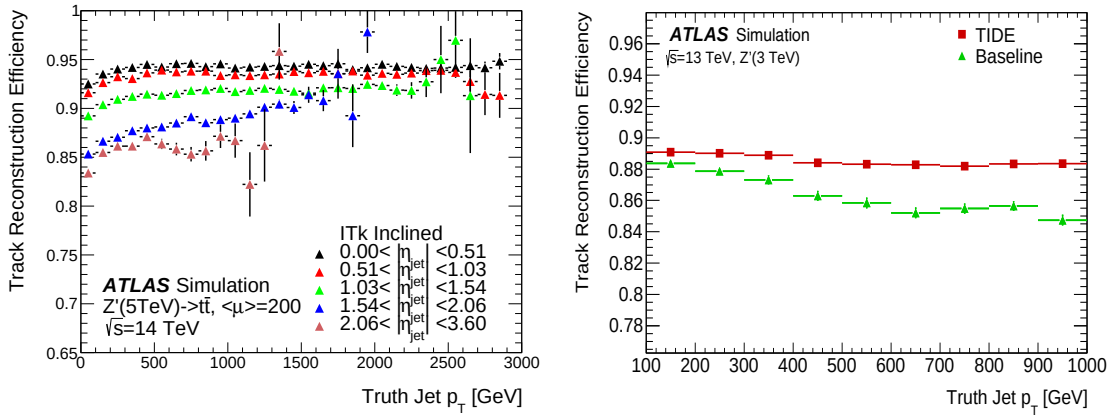


Figure 4.28: **Left:** The track reconstruction efficiency for tracks within $\Delta R < 0.4$ of jets, here shown as a function of jet truth transverse momentum in GeV for the ITk layout. The data is divided in slices of η to show the pseudorapidity dependence of the efficiency. **Right:** The corresponding plot for ATLAS Run 2 which is shown as a qualitative comparison, for a 3 TeV Z' sample [32]. In this right plot, the TIDE algorithm is compare to the baseline tracking performance.

In the second study, the track reconstruction efficiency is determined as a function of the ΔR of each truth particle from the jet axis, up to 0.4. In this case, the study is conducted separately for b-jets and light-jets. The jets are identified by matching the truth record of the particles inside the jet — if a stable truth particle containing a b-quark is found it is labelled as a b-jet; if none is found but a stable truth particle containing a c-quark is found it is labelled a c-jet, otherwise it is labelled a light-jet.

Figure 4.29 shows the track reconstruction efficiency as a function of ΔR for b-jets and light-jets. It is shown that no significant drop occurs inside the core of jets. Also included in Figure 4.29 is the corresponding plot for ATLAS Run 2 where even for the optimised TIDE algorithm there is a drop of about 10% for b-jets. Part of the reason for this drop is that for b-jets at high p_T often only 2-3 pixel detector layers are available since the b-hadron is so strongly boosted that it decays outside the inner pixel layers. The ITk design, with its 5 pixel layers, mitigates this problem considerably as the analog charge information can be

used to separate the tracks, and measure their properties, in this dense environment.

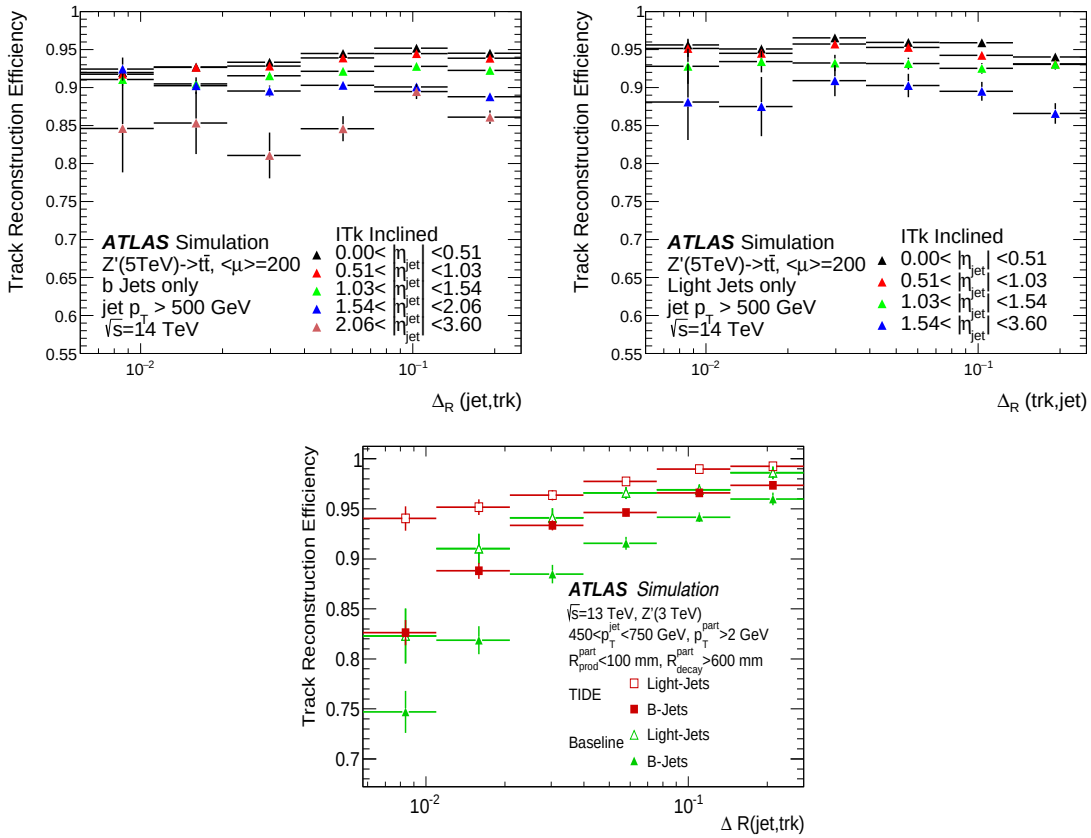


Figure 4.29: The track reconstruction efficiency for tracks in b-jets (top left) and light-jets (top right) with transverse momenta above 500 GeV as a function of the track's ΔR from the jet. The efficiency is shown for various η-ranges. The efficiency for b-jets and light-jets for ATLAS Run 2 is shown in the bottom plot [32] for a comparable p_T range, for a 3 TeV Z' sample. Here, the optimised Tracking In Dense Environment (TIDE) algorithm is compared to the baseline tracking performance.

4.5.3 Displaced Tracks

The $Z' \rightarrow t\bar{t}$ samples can be used to study displaced vertices, another critical signature for many ATLAS physics measurements and searches. Since displaced vertices often come from massive and/or boosted particles, they often appear in dense environments in their decays and as such are interesting to consider as part of the layout optimisation. For instance, charged particles associated to the decay of a b-hadron often miss the inner radius pixel detector layers as the decay of the b-hadron occurs at larger radii.

In this case, all truth particles in the event which are stable and come from a b-hadron are identified. Then, they are separated into leptons and hadrons, and the b-hadron decay

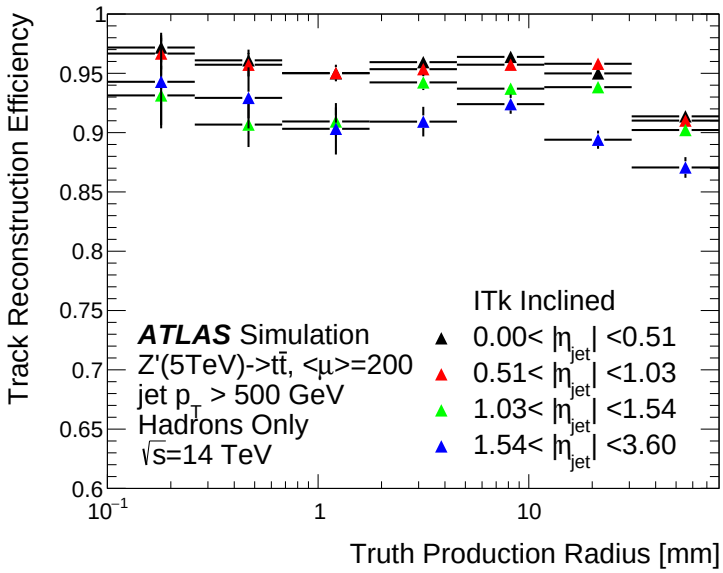


Figure 4.30: The track reconstruction efficiency for tracks matched to a truth hadron in jets with transverse momentum above 500 GeV which are a decay product of a b hadron, here shown as a function of the parent's decay radius in the detector, for the ITk layout. The results are shown in slices of η to show the pseudorapidity dependence of the efficiency.

radius is found. All the other requirements placed on truth particles and tracks from the previous subsection are also made, except for the ΔR requirement which is removed.

Figure 4.30 shows the track reconstruction efficiency for hadrons and leptons produced in a b-hadron decay as a function of the b-hadron's decay radius in the detector. In the central region ($|\eta| < 1.03$) the efficiency is about 95% up to a radius of 30 mm, and then falls by $\approx$7% as the b-hadron decays outside the innermost pixel layer. At high η the efficiency is generally a bit lower, but it is also constant up to $R = 3$ cm.

4.6 Physics Benchmark Studies

In this Section the impact of the new tracking system on physics analyses is demonstrated. The upgraded tracking detector plays a vital role in these analyses. They depend on it for b-tagging, for pile-up jet rejection, for track confirmation[10], for jets in the definition of missing transverse momentum, and for lepton and photon identification and isolation. Unless otherwise stated, jets used in the studies here are anti-k_t jets with radius parameter $R = 0.4$.

4.6.1 Production of Higgs-Bosons via Vector-Boson Fusion with Decay to $WW^{(*)}$

Production of Higgs bosons at the LHC proceeds mainly via the gluon-fusion (ggF) process. The next largest contribution to the production cross section is from the vector boson fusion (VBF) process. The Feynman diagrams for these processes are shown in Figure 4.31, together with the Feynman diagram for production of a Higgs Boson in association with a vector boson (VH production). The VBF process exhibits a striking signature: events are produced with jets in the forward/backward regions that have large dijet invariant mass. This signature can be exploited to distinguish VBF from many background processes. The forward jets are referred to as "tagging" jets, and by selecting events with large invariant mass of the two-tagging-jet system, a high signal-to-background ratio can be achieved. The expected precision of this measurement depends on the angular coverage and layout of the upgraded ATLAS tracker because it relies on the tracker to veto jets arising from pile-up interactions and to correctly identify jets containing b-hadrons.

The measurement prospects for VBF $H \to WW^{(*)} \to e\nu\mu\nu$ have recently been studied [11]. The study is based on a combination of electron and muon efficiencies from full simulation of the Run-1 ATLAS detector, and parametrisations of the expected reconstruction of other objects from the upgraded ATLAS detector. The b-tagging performance in Ref. [11] assumed a 70% b-jet efficiency working point with the light-jet "mistag" rate discussed in Ref. [2], however for this document the study has been updated to use the b-tagging 70% efficiency working point with the rejection of light quark and charm jets described in Section 4.3.2. Furthermore, for this document the jet selection has been modified slightly compared with that in Ref. [11].

The object and event selections closely follow the selections used for the *VBF cross-check analysis* in [33]. Electron and muon candidates are required to be isolated and have $p_{\mathrm{T}} > 15$ GeV. The electrons and muons are restricted to $|\eta| < 2.47$ and $|\eta| < 2.5$ respectively.

[10] Track confirmation uses the available tracking information to distinguish between jets coming from either the hard scatter or pile-up vertices, with a pile-up jet misidentification probability of 2%, as described in Section 4.4.4. For a given pile-up efficiency, the track confirmation function parameterises the hard scatter efficiency as a function of p_T and η.

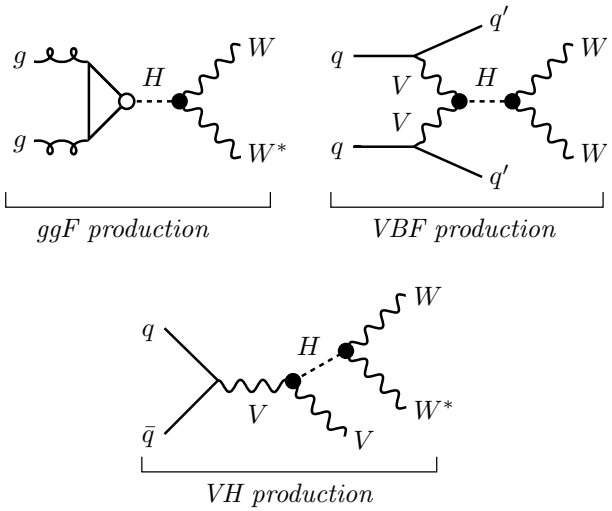


Figure 4.31: Leading order Feynman diagrams for Higgs boson production at the LHC.

All jets are required to have $p_{\mathrm{T}} > 30$ GeV and are restricted to $|\eta| < 3.8$. All jets are taken into account for the b-jet veto, which simply requires that no jets in the event are b-tagged, regardless of whether they pass track confirmation requirements.

The analysis uses an "OR" of single high-p_{T} electron or high-p_{T} muon triggers, and the efficiencies of these are emulated. The trigger p_{T} thresholds are 25 GeV for muon triggers and 25-28 GeV for electron triggers, depending on the detector scenario. Events with exactly two oppositely-charged different-flavour ($e\mu$) leptons are selected. The leading lepton must have $p_{\mathrm{T}} > 25$ GeV. The invariant mass of the lepton pair, $m_{\ell\ell}$ is required to be larger than 10 GeV. A requirement that the jet-corrected track $E_{\mathrm{T}}^{\mathrm{miss}}$ be greater than 20 GeV reduces the Drell-Yan and multi-jet backgrounds. The total transverse momentum $p_{\mathrm{T}}^{\mathrm{tot}}$ [11)] is used to further suppress backgrounds. Requiring small $p_{\mathrm{T}}^{\mathrm{tot}}$ removes mainly $t\bar{t}$ background events. To reduce the $Z/\gamma^* \to \tau\tau$ background, events with reconstructed ditau mass ($m_{\tau\tau}$) larger than 50 GeV, calculated from the visible leptons and the $E_{\mathrm{T}}^{\mathrm{miss}}$ via a collinear approximation [34], are removed.

The VBF topology is selected by requiring the leading two jets to have $|\eta| > 2$ in opposite hemispheres and the invariant mass of the two leading jets (m_{jj}) to be greater than 1250 GeV. VBF processes do not have colour flow between these jets, thus additional jet activity within the event is suppressed. Therefore events are removed if they have additional jets with $p_T >$ 30 GeV within the rapidity range spanned by the two leading jets. This selection is referred to as the central jet veto (CJV). Finally the leptons from Higgs-boson decay also tend to lie

[11] The $p_{\mathrm{T}}^{\mathrm{tot}}$ is defined as: $p_{\mathrm{T}}^{\mathrm{tot}} = |\mathbf{E}_{\mathrm{T}}^{\mathrm{miss}} + \mathbf{p}_{\mathrm{T}}^{\mathrm{lead}} + \mathbf{p}_{\mathrm{T}}^{\mathrm{sublead}} + \sum_{j}^{\mathrm{jets}} \mathbf{p}_{\mathrm{T}}^{j}|$, where $\mathbf{E}_{\mathrm{T}}^{\mathrm{miss}}$, $\mathbf{p}_{\mathrm{T}}^{\mathrm{lead}}$,and $\mathbf{p}_{\mathrm{T}}^{\mathrm{sublead}}$ are the transverse momentum vector for the $E_{\mathrm{T}}^{\mathrm{miss}}$, leading and sub-leading leptons respectively. The $\sum_{j}^{\mathrm{jets}} \mathbf{p}_{\mathrm{T}}^{j}$ is the vector sum over transverse momentum of the jets with $p_{\mathrm{T}} > 30$ GeV and passing the pile-up mitigation.

between the two leading jets in rapidity, so events with leptons outside the rapidity gap of the leading two jets are removed. Relative to [11] this selection has a lower p_{T} threshold on the leading two jets but requires them to be within the tracker acceptance, enabling an improved signal yield while reducing the background from pile-up jets.

The remaining selection criteria exploit the spin-0 nature of the Higgs Boson and the V-A decay of the W bosons. The invariant mass of the lepton pairs for signal events tends to be lower than for events from background processes, thus $m_{\ell\ell}$ is required to be less than 60 GeV. The two leptons also tend to point in the same direction in the transverse plane of the detector, hence a requirement is made that the azimuthal angle between the leptons ($\Delta\phi_{\ell\ell}$) be less than 1.8 radians. Finally, the invariant mass of the WW^* pair cannot be computed because of the two neutrinos in the final state; however the total $\mathbf{p}_{\mathrm{T}}$ of the neutrinos is known. It is thus possible to define the transverse mass as [35]:

$$m_{\mathrm{T}} = \sqrt{(E_{\mathrm{T}}^{\ell\ell} + E_{\mathrm{T}}^{\mathrm{miss}})^2 - |\mathbf{p}_{\mathrm{T}}^{\ell\ell} + \mathbf{E}_{\mathrm{T}}^{\mathrm{miss}}|^2}, \tag{4.4}$$

where $\mathbf{p}_{\mathrm{T}}^{\ell\ell}$ is the vector-summed transverse momentum of the two leptons and $E_{\mathrm{T}}^{\ell\ell}$ is defined as $(p_{\mathrm{T}}^{\ell\ell})^2 + m_{\ell\ell}^2$. This quantity has a kinematic endpoint at the Higgs-boson mass (m_H). Thus, allowing for resolution effects, the m_{T} is required to be less than $1.07 \times m_H$.

Distributions after the selection, including $\Delta\phi_{\ell\ell}$, m_{T}, the rapidity gap between the two leading jets ($|\Delta y_{jj}|$), and m_{jj} are shown in Figure 4.32. The background samples are stacked with the expected signal overlaid. The simulated $t\bar{t}$ sample is the largest background and statistical fluctuations are visible for some samples due to the limited number of Monte Carlo events and low selection efficiency.

The expected precision of the cross-section measurement for $H \to WW^*$ is 12% if one neglects theoretical uncertainties on VBF and ggF Higgs-boson production[12]. This expected precision depends on the tracker coverage up to $|\eta| = 4.0$, which allows the vetoing of pile-up jets via track confirmation to prevent signal events from being rejected by the CJV. The efficiency of the CJV requirement is 82% for $|\eta| < 4.0$ declining to 59% (26%) for a tracker with coverage up to $|\eta| < 3.2$ ($|\eta| < 2.7$). The resulting precision on the visible cross-section measurement for these different scenarios is shown in Table 4.5. The improvements from using the forward tracking are not as pronounced as in Ref. [11] due to the fact that in this updated study the same b-tagging performance is assumed for all tracking scenarios, whereas in Ref. [11] degraded performance was expected for the scenarios with reduced tracking coverage. It is expected that with a better optimised analysis this channel could provide measurement results competitive with those that would be expected at low pile-up with the run-2 detector and equivalent integrated luminosity.

This analysis shows a large sensitivity to the angular coverage of the upgraded tracker. This arises primarily through the use of the b-jet veto and track confirmation for jets. The

[12] Experimental systematic uncertainties such as those arising from the determination of the jet energy scale, jet energy resolution and b-tagging efficiencies are included in this study.

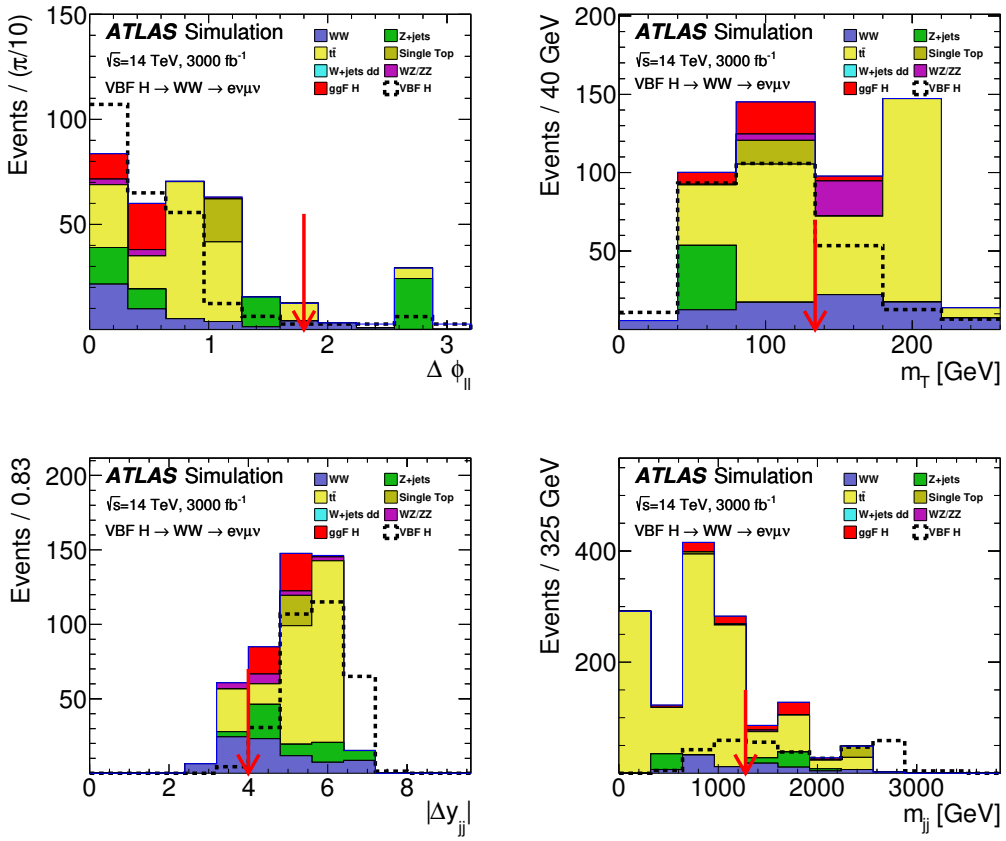


Figure 4.32: Kinematic distributions used in the measurement of VBF Higgs Boson production: (a) $\Delta\phi_{ll}$, (b) m_T, (c) $|\Delta y_{jj}|$, and (d) m_{jj}. Each distribution is shown for the full selection except for the requirement on the variable being displayed, arrows indicate the point at which the selection cut is set.

evaluation of their individual contribution has to take into account the strong correlation between them. If the track confirmation is dropped for jets in the pseudorapidity region $|\eta| > 2.4$, a degradation of the signal strength measurement by up to 60% is observed. On the other hand, the importance of b-tagging in the very forward region for physics processes where top-quark production is a significant background is demonstrated by removing the b-tagging requirement in the very forward region. In this case, the degradation in the signal strength measurement is 55%.

4.6.2 Same-Sign WW production

The measurement of same-sign $W^{\pm}W^{\pm}$ production offers one of the best opportunities to measure the cross section for vector-boson scattering (VBS). In the Standard Model, the Higgs boson prevents the longitudinal scattering amplitude of the $VV \to VV$ process from

Table 4.5: The expected precision of the VBF $H \rightarrow WW^*$ cross-section measurement for different tracking coverage scenarios, theoretical uncertainties on Higgs boson production are neglected.

Tracking coverage	**Expected precision**
$\|\eta\| < 4.0$	12%
$\|\eta\| < 3.2$	18%
$\|\eta\| < 2.7$	22%

continuously increasing as a function of the centre-of-mass energy of the diboson system, which would otherwise violate unitarity at energies above approximately 1 TeV. Thus, understanding VBS is a key part of studying the nature of the electroweak symmetry breaking (EWSB) mechanism. Furthermore, it is a powerful probe for physics beyond the Standard Model. It is still unknown whether the discovered Higgs Boson contributes fully to the EWSB, and preserves unitarity of the VV scattering amplitude at all energies, or whether other new physics processes are involved [36–38]. The expected precision of this measurement depends on the angular coverage and layout of the upgraded ATLAS tracker because it relies on the tracker to veto jets arising from pile-up interactions, and to veto additional leptons.

In the VBS topology two incoming partons radiate electroweak bosons, which subsequently scatter and decay into fermions. The two outgoing quarks are typically forward, leading to a final state with two bosons and two well separated jets. This final state can also be produced by other electroweak (EW) and QCD processes. Representative Feynman diagrams are shown in Figures 4.33–4.35: Figure 4.33 shows VBS processes; Figure 4.34 shows EW processes without VBS; and Figure 4.35 shows QCD processes.

A study of the impact of the Extended Inner Tracking Detector on the measurement of $W^{\pm}W^{\pm}$ scattering has been performed. In this study, a comparison is made between scenarios with the coverage of the Run-1 tracker ($|\eta| < 2.5$) and with the proposed forward tracking coverage ($|\eta| < 4.0$). This study incorporates several improvements relative to the ATLAS Phase-II upgrade scoping document study [2], the most important being the raising of jet p_{T} thresholds outside of the tracking acceptance, to suppress pile-up jets, and splitting the events into categories, to maximise the sensitivity of this channel when performing their statistical combination. The analysis proceeds on particle-level objects. Detector effects are taken into account with a procedure that relies on full simulation, and is based on a parameterised response of the upgraded ATLAS detector for the reconstruction of jets, leptons and missing transverse momentum.

The experimental signature studied is one with two leptons that have the same electric charge, two jets that are well separated in rapidity, and moderate $E_{\mathrm{T}}^{\mathrm{miss}}$. The dominant background process in this final state is WZ+jets production; other contributions include events with charge-misidentified leptons (most notably for Z+jets production), additional leptons from hadronic decays in jets, and photon conversions.

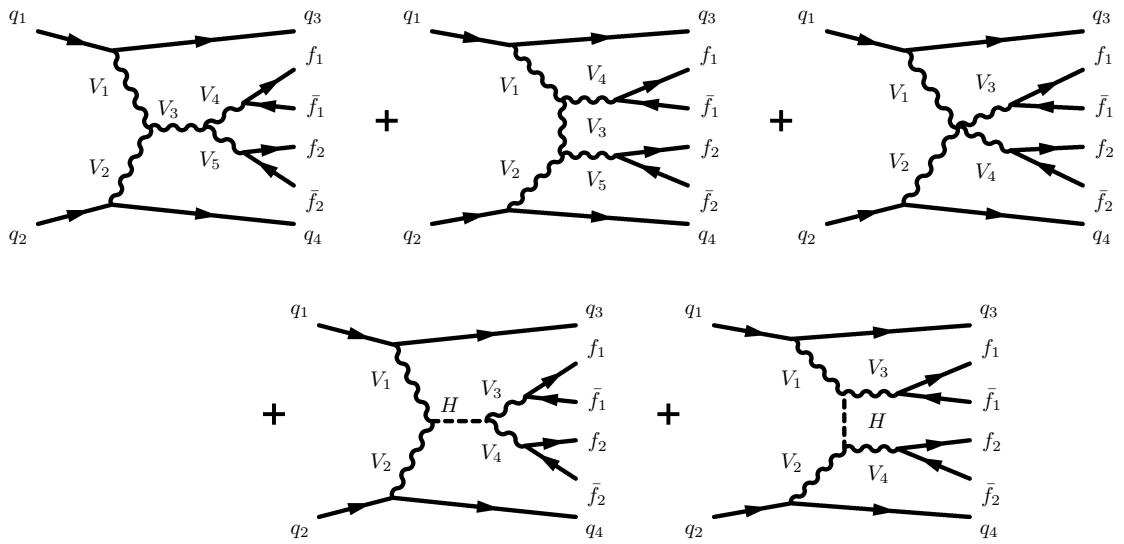


Figure 4.33: Representative Feynman diagrams for $VVjj$-EW production with a scattering topology including either a triple gauge boson vertex with production of a W/Z boson in the s-channel (top left diagram), the t-channel exchange (top middle diagram), quartic gauge boson vertex (top right diagram), or the exchange of a Higgs boson in the s-channel (bottom left diagram) and t-channel (bottom right diagram). The lines are labeled by quarks (q), vector bosons ($V = W, Z$), and fermions (f).

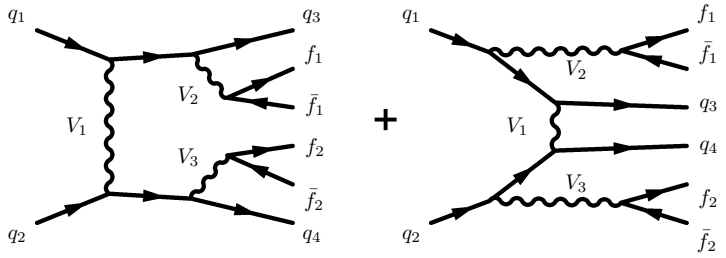


Figure 4.34: Representative Feynman diagrams for $VVjj$-EW production without vector-boson scattering topology. The lines are labeled by quarks (q), vector bosons ($V = W, Z$), and fermions (f).

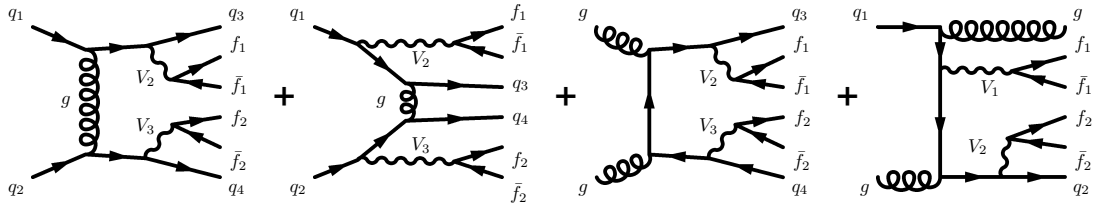


Figure 4.35: Representative Feynman diagrams for VVjj-QCD production with strong interaction vertices. The lines are labeled by quarks (q), vector bosons ($V = W, Z$), fermions (f), and gluons (g).

Events containing electrons and muons with transverse momenta $p_{\mathrm{T}} > 7$ GeV and 6 GeV, respectively, are preselected. The events must pass a single-muon or single-electron trigger requiring transverse momentum $p_{\mathrm{T}} > 20$ GeVand $p_{\mathrm{T}} > 25$ GeV respectively. The pseudorapidity range for the lepton selection depends on the tracking scenario being studied: with forward tracking, the leptons are required to be within $|\eta| < 4.0$, whereas without forward tracking the leptons are restricted to $|\eta| < 2.7$.

Jets with $p_{\mathrm{T}} > 30$ GeV are considered for the analysis. An overlap requirement is applied with the intention of excluding fake jets that are within a distance $\Delta R_{ej} < 0.2$ of a preselected electron. A track confirmation requirement is applied to all jets with $p_{\mathrm{T}} < 100$ GeV. In this study, the track confirmation is applied depending on the tracking scenario: for jets up to $|\eta| < 3.8$ with forward tracking available, and for jets up to $|\eta| < 2.5$ without forward tracking. To reduce the significant contamination from pile-up jets outside the tracking region, the p_T threshold for jets in this region ($|\eta| > 2.5$ or 3.8) is increased from 30 to 70 GeV. Jets passing the p_{T} threshold, track confirmation and overlap requirements are preselected, and the two highest p_{T} jets are defined as the leading and sub-leading tag jets in the event.

The event selection requires that there be exactly two leptons (electrons or muons) with $p_{\mathrm{T}} > 25$ GeV and no additional preselected leptons. The leptons are required to have the same charge and to be separated by $\Delta R_{\ell\ell} > 0.3$. Furthermore a mass requirement is applied to the dilepton system $m_{\ell\ell} > 20$ GeV. The large background to the dielectron channel from $Z \to ee$, in which the charge of one electron is mismeasured, is suppressed by vetoing events where the dielectron mass is close to the Z boson mass, $|m_{ee} - m_Z| < 10$ GeV. Moderate missing transverse momentum is required, $E_{\mathrm{T}}^{\mathrm{miss}} > 40$ GeV. The event must further have at least two jets that are required to be well separated from leptons ($\Delta R_{\ell j} > 0.3$) and to be very far from each other, $\Delta\eta_{jj} > 2.4$. The dijet mass, m_{jj} is required to be greater than 500 GeV. Finally the lepton centrality ζ[13] is required to be greater than zero.

The leading and sub-leading jet η distributions after the full event selection are shown in Figure 4.36 for the $W^{\pm}W^{\pm}$ signal and backgrounds. The solid filled histograms show the contribution when the selected jet originates from the hard scatter, while the hashed histograms show the contributions from pile-up jets. A step in the signal distribution in the $|\eta| > 2.5$ and $|\eta| > 3.8$ regions (for the scenarios without and with forward tracking, respectively) is noticeable in the sub-leading jet distributions, showing the effect of the raised p_{T} threshold for jets in these regions. The pile-up contribution is subdominant, but becomes more important beyond the tracker acceptance.

The expected precision of the cross-section measurement ($\frac{\Delta\sigma}{\sigma}$) is calculated separately for the four channels[14] $ee, \mu\mu, e\mu$, and μe, and then combined, giving the results shown in Table 4.6. Theoretical systematics are neglected, but an expected uncertainty of 15% on the

[13] The variable ζ is defined by $\zeta = \min[\min(\eta_{\ell 1}, \eta_{\ell 2}) - \min(\eta_{j1}, \eta_{j2}), \max(\eta_{j1}, \eta_{j2}) - \max(\eta_{\ell 1}, \eta_{\ell 2})]$.
[14] The channels are labelled $l_1 l_2$ where l_1 is the leading lepton and l_2 is the sub-leading lepton.

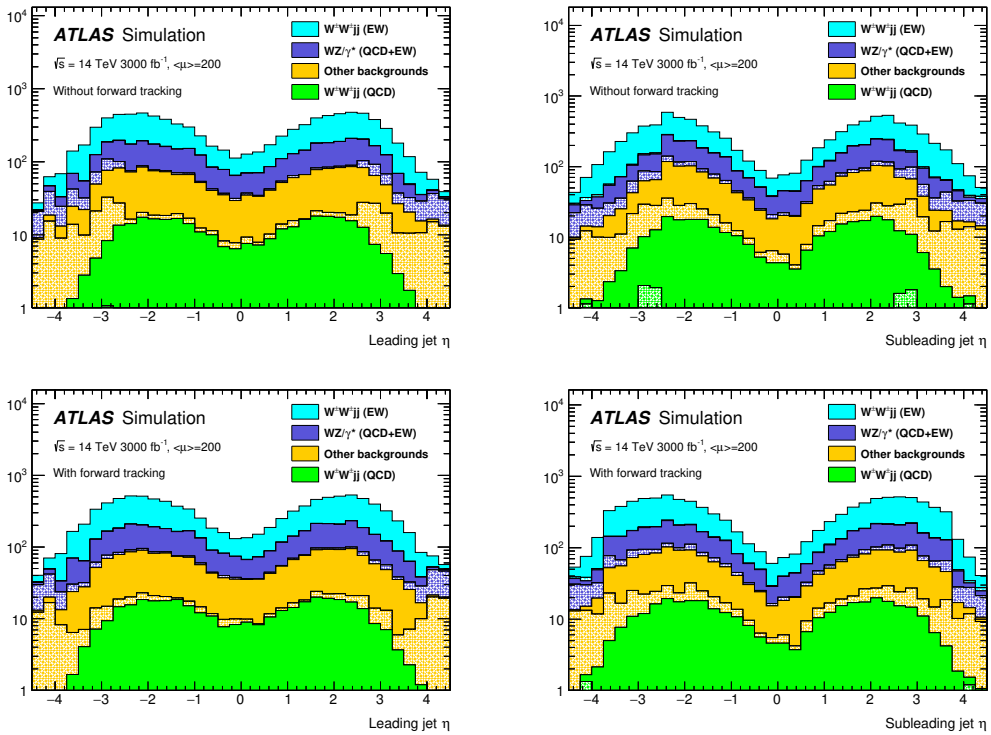


Figure 4.36: Leading (left) and sub-leading (right) jet $|\eta|$ distributions after all event selections, in the same-sign WW analysis, for the scenarios without (top) and with (bottom) forward tracking. The solid filled histograms show the contribution from selected hard scatter jets, while the hashed histograms show the contributions when the selected jet arises from pile-up.

background expectation from experimental sources is taken into account. This measurement provides a sensitive metric against which to evaluate the impact of a forward tracking detector in ATLAS for the HL-LHC run. The difference between the scenarios with and without forward tracking is less dramatic than in Ref. [2] due to the improvements in the analysis. With the large number of pile-up vertices expected, the forward tracker provides increased background rejection owing to both a stronger veto on additional leptons (helping to suppress the WZ background), as well as pile-up jet rejection across a larger phase space. The changes in the signal and background yields, and the effect on the measurement precision, are summarised in Table 4.7, where the separate and combined effects of allowing the pile-up jet rejection for forward jets, or the extending lepton η region are presented. The rejection of forward pile-up jets using the jet vertex requirement up to $|\eta| < 3.8$ increases the signal yield by 12%, since the jet p_T threshold remains at 30 GeV over a larger region. However, this comes at the cost of also increasing the total background yield, leading to a negligible change in the precision of the measurement. The $W^{\pm}W^{\pm}$ EW, $W^{\pm}W^{\pm}$ QCD, and WZ EW processes all contain two jets originating from the hard scatter vertex, and while the $W^{\pm}W^{\pm}$ QCD background can be reduced by the dijet rapidity separation requirement, the strongest reduction of the WZ backgrounds (both QCD and EW) comes from the veto

on additional leptons. Here, the ability to reconstruct forward leptons provides a stronger veto since the likelihood of detecting the third lepton is increased. The combination of the two thus provides the most optimal situation, with an increase in the signal yield of 14%, and an improvement of 13% on the measurement precision.

Table 4.6: Significance and precision of the $W^{\pm}W^{\pm}$ measurement for the scenarios without and with forward tracking.

	$\frac{\Delta\sigma}{\sigma}$
Without forward tracking	4.5%
With forward tracking	3.9%

Table 4.7: Effect on event yields and precision of the $W^{\pm}W^{\pm}$ measurement for the pile-up removal and additional lepton-veto from forward tracking.

	Signal variation	**Background variation**	$\frac{\Delta\sigma}{\sigma}$ **variation**
Pile-up rejection	+12%	+15%	+2.0%
Additional lepton veto	+2.8%	-8.5%	-13%
Combined	+14%	+7.3%	-13%

4.6.3 Higgs Boson to $\mu\mu$

To search for deviations from the SM predictions for the properties of the Higgs boson, it is important to study the coupling of the Higgs boson to different fermion families. The $H \rightarrow \mu^+\mu^-$ decay has a small branching ratio but produces a very narrow peak in the $\mu^+\mu^-$ invariant mass distribution. The sensitivity of the ATLAS experiment at the HL-LHC has been studied by using parameterisations of the expected detector resolutions and efficiencies for the ATLAS detector with an upgraded inner-detector tracker. A key aspect of this analysis is the precise reconstruction of the invariant mass of the $\mu^+\mu^-$ pair, which critically depends on the performance of the upgraded tracker. It has been shown in Section 4.2.4 that the track p_{T} resolution is significantly better in the central region than in the forward region. As a result of this, making use of the extended forward tracking of the ITk does not increase the significance of the final expected result.

The analysis is composed of an event selection aimed at keeping a high signal efficiency whilst suppressing the backgrounds as much as possible. Events are required to have exactly one pair of reconstructed opposite-sign muons with $p_{\mathrm{T}} > 15$ GeV and $|\eta| < 2.5$. One of these muons must cause the event to pass a single-muon trigger that has a p_{T} threshold of 25 GeV. Muons overlapping with good jets within a cone of radius of $\Delta R < 0.4$ are ignored, where good jets are defined as all jets with $p_{\mathrm{T}} > 30$ GeV passing a track-confirmation algorithm aimed at suppressing pile-up jets. The highest p_{T} muon should

have $p_T > 25$ GeV. Selected events are required to have dimuon invariant mass, $m_{\mu\mu}$, lying in the range $110 < m_{\mu\mu} < 160$ GeV; the distribution of this quantity is then used to extract the final results. The main backgrounds, in descending order of significance are: Drell-Yan events ($pp \to \gamma/Z^*X \to \mu^+\mu^-X$), leptonic $t\bar{t}$ decays ($pp \to t\bar{t}X \to \mu^+\mu^- b\bar{b}\nu\tilde{\nu}X$) and leptonic WW decays ($pp \to W^+W^-X \to \mu^+\mu^-\nu\tilde{\nu}X$).

An event classification is used to split the selected sample into subsets, each with different signal-to-background ratios (S/B) in order to increase the sensitivity of the search. Finally, a maximum likelihood fit is performed to the selected sample in order to estimate the signal yield and its uncertainty. Figure 4.37 shows the expected invariant mass distribution of selected signal and background candidates. The narrow signal peak has a maximum at approximately two orders of magnitude below the background. For such cases the resolution of the signal mass peak becomes paramount to improve the signal to background ratio within a mass window that yields high signal acceptance. In Figure 4.38 the resolution of the upgraded tracking detector (inclined layout) is compared to that of the existing layout as used in Run 2, the upgraded layout improves on the resolution of the Run 2 configuration by 25%.

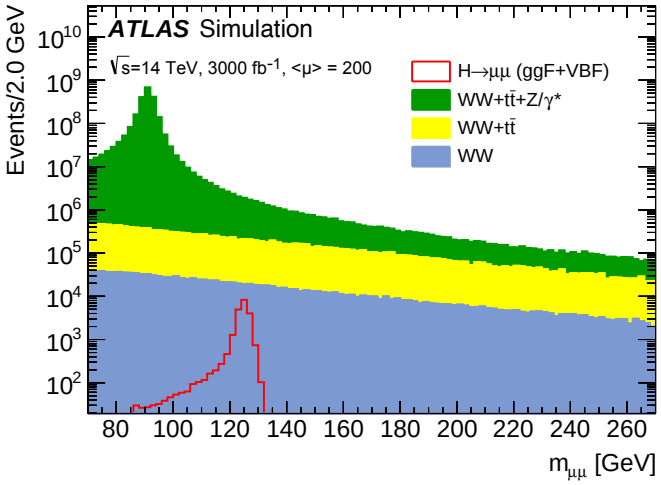


Figure 4.37: Invariant mass distribution of selected signal and background candidates, scaled to 3000 fb^{-1}, for the upgraded ATLAS detector with $\langle\mu\rangle$ =200.

4.6.4 *HH* Channels

In order to establish the Higgs mechanism as being responsible for electroweak symmetry breaking, the measurement of the Higgs boson self-couplings and subsequent reconstruction of the Higgs potential are crucial. A direct measurement of the Higgs boson trilinear self-coupling λ_{HHH} can be made via the study of Higgs boson pair production. At hadron colliders, the dominant production mechanism is gluon fusion, with the other production

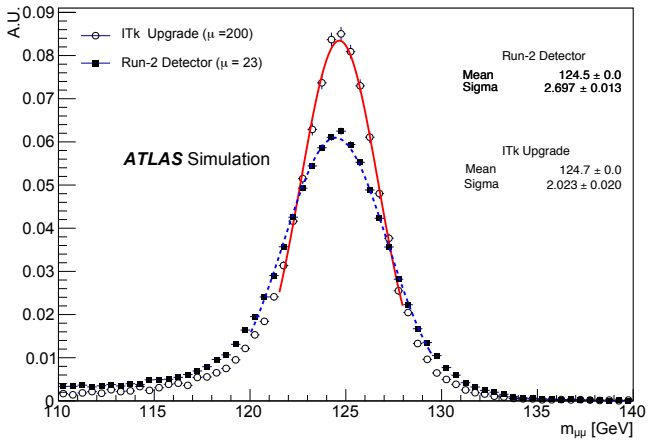


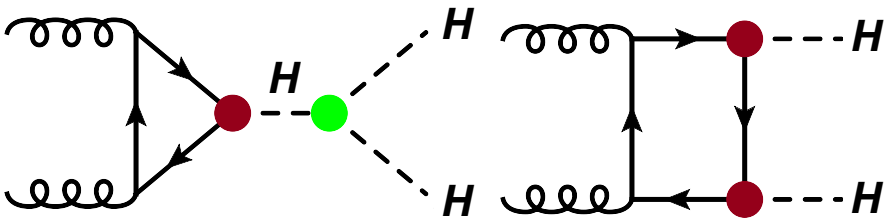
Figure 4.38: Signal resolution for $H \to \mu\mu$ signal events, the Run 2 resolution is compared to the HL-LHC with pile-up conditions corresponding to $\langle\mu\rangle$ =200.

mechanisms: Vector Boson Fusion, Higgs-strahlung, and associated production with $t\bar{t}$, being more than an order magnitude smaller [39, 40]. For centre-of-mass energies of 14 TeV, the production cross section of pairs of 125 GeV Higgs bosons is estimated to be 40.8 fb at next-to-next-to-leading order in QCD (with an uncertainty of $\pm$8.5% from QCD scale uncertainties, and $\pm$7% from PDF+α_S uncertainties) [41, 42]. Example Feynman diagrams of this process at leading order in Quantum Chromodynamics are shown in Figure 4.39. The diagram which exhibits λ_{HHH} dependence (Figure 4.39(a)) interferes destructively with the box diagram that is independent of λ_{HHH} (Figure 4.39(b)), thus a small increase in the value of λ_{HHH} decreases the expected HH production cross section, and modifies the distributions of event kinematics.

The low SM non-resonant HH production cross section means that it is necessary to consider final states where at least one of the two Higgs bosons decays into a final state with a large branching ratio. The decay channel with largest branching ratio is $H \to b\bar{b}$. Thus the high-performance b-tagging capability of the proposed upgraded tracker is of critical importance for these analyses. The SM non-resonant HH production process is dominated by gluon-gluon fusion, leading to centrally produced Higgs bosons, hence the extended forward tracking capability of the ITk is not expected to lead to large improvements in sensitivity.

$HH \to b\bar{b}b\bar{b}$

The HH decay channel with the largest branching ratio (33.3%) is $HH \to b\bar{b}b\bar{b}$. Projections for this channel have been made, extrapolating from the ATLAS Run 2 analysis [43], to estimate the sensitivity to Higgs-boson pair production with the full HL-LHC dataset of 3000 fb^{-1}. This extrapolation assumes similar detector performance to Run 2 for jet reconstruction and b-jet identification; as such it gives a pessimistic estimate of the sensitivity



(a) λ_{HHH} dependent (self-coupling) diagram. (b) λ_{HHH} independent (box) diagram.

Figure 4.39: Leading order Feynman diagrams for pair production of Higgs Bosons.

because, as shown in Section 4.3.2, the expected performance of the b-tagging is comparable to Run 2 before any optimisation of the b-tagging algorithms. Indeed, in the case of the MV1 algorithm, the expected performance is already better than that for Run 2 as shown in Figure 4.15.

Events were selected using a set of four triggers. These triggers require events to have either: one b-tagged jet with $p_{\mathrm{T}} > 275$ GeV, one b-tagged jet with $p_{\mathrm{T}} > 75$ GeV and three additional jets with $p_{\mathrm{T}} > 75$ GeV, two b-tagged jets with $p_{\mathrm{T}} > 55$ GeV and an additional jet with $p_{\mathrm{T}} > 100$ GeV, or two b-tagged jets with $p_{\mathrm{T}} > 35$ GeV and two additional jets with $p_{\mathrm{T}} > 35$ GeV. The event is required to contain at least four b-tagged jets with $p_{\mathrm{T}} > 30$ GeV and $|\eta| < 2.5$. The four jets with the highest b-tagging score are paired to construct two Higgs boson candidates as described in Ref. [44]. Higgs boson pairs are reconstructed over a wide range of masses, 200 GeV $< m_{4\mathrm{j}} <$ 1300 GeV. Event selection criteria that vary as a function of the reconstructed mass are used to enhance the analysis sensitivity across this range. Mass-dependent requirements are made on the leading Higgs boson candidate p_{T}, the sub-leading Higgs boson p_{T}, and the pseudorapidity difference between the two Higgs boson candidates. Following this mass-dependent selection, a further requirement is made that the two Higgs boson candidates must be well separated by demanding $\Delta R(H, H) >$ 1.5.

Finally, a requirement on the Higgs boson candidate masses is made:

$$X_{HH} = \sqrt{\left(\frac{m_{2\mathrm{j}}^{\mathrm{lead}} - 120\ \mathrm{GeV}}{0.1 m_{2\mathrm{j}}^{\mathrm{lead}}}\right)^2 + \left(\frac{m_{2\mathrm{j}}^{\mathrm{subl}} - 115\ \mathrm{GeV}}{0.1 m_{2\mathrm{j}}^{\mathrm{subl}}}\right)^2} < 1.6 \tag{4.5}$$

where the $0.1 m_{2\mathrm{j}}$ terms represent the widths of the leading and sub-leading Higgs boson candidate mass distributions. The final analysis discriminant, $m_{4\mathrm{j}}$, is simply the invariant mass of the selected four-jet system.

After the full event selection, $\sim$ 95% of the background consists of multijet events. It is difficult to model this background accurately using Monte Carlo simulation, partly due to the complexity of the large number of processes contributing to the background, but mainly due to the need for an extremely large number of events as a result of the large cross section

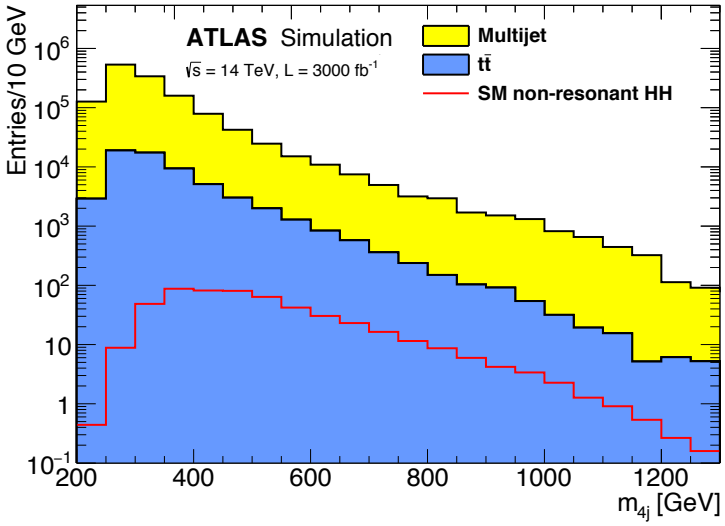


Figure 4.40: Stacked m_{4j} histograms of the $t\bar{t}$ and multijet backgrounds in the search for $HH \to b\bar{b}b\bar{b}$ extrapolated to $\int \mathcal{L}dt = 3000$ fb^{-1}. The predicted SM non-resonant Higgs boson pair production signal is shown as the line.

and high background rejection factor. As a result, the multijet background is modelled directly from data. Several high-purity, high-statistics control regions are defined using mass sidebands in the m_{2j}^{lead}–m_{2j}^{subl} plane. This allows the multijet background to be derived and tested using independent data samples that have background composition kinematics similar to the signal region. The remaining 5% is $t\bar{t}$ production, which is modelled using MC simulation. There is negligible background from all other sources – including processes involving Higgs bosons.

The m_{4j} distribution extrapolated to 3000 fb^{-1} is shown in Figure 4.40. This distribution is used in the statistical analysis, along with others corresponding to systematic uncertainty variations. The pseudo-data used in the extrapolation are taken to be the sum of the background distributions.

Variations in the Higgs boson self-coupling, λ_{HHH} , change both the total cross section of $pp \to HH$ and the shape of the m_{HH} distribution. To assess the sensitivity of the $HH \to b\bar{b}b\bar{b}$ analysis to λ_{HHH}, m_{HH} distributions were generated using the morphing technique documented in Ref. [45] for $-20 \leq \lambda_{HHH}/\lambda_{SM} \leq 20$. These distributions were then used to set 95% C.L. upper limit on the cross sections, as shown in Figure 4.41. If systematic uncertainties were negligible, the Higgs boson self-coupling would be constrained at 95% C.L. to $0.2 < \lambda_{HHH}/\lambda_{SM} < 7.0$. If the systematic uncertainties remain as they were for the 2016 analysis, the constraint would be $-3.5 < \lambda_{HHH}/\lambda_{SM} < 11$. The exclusion limits grow worse in the range $3 < \lambda_{HHH}/\lambda_{SM} < 5$ as the m_{HH} distribution skews to lower values of m_{HH} where the background is larger. Events produced via the process shown in Figure 4.39(a) have a softer m_{HH} distribution than those produced via the process shown in

Figure 4.39(b): as λ_{HHH} increases, the self-coupling diagram becomes dominant, leading to a shift to lower m_{HH}.

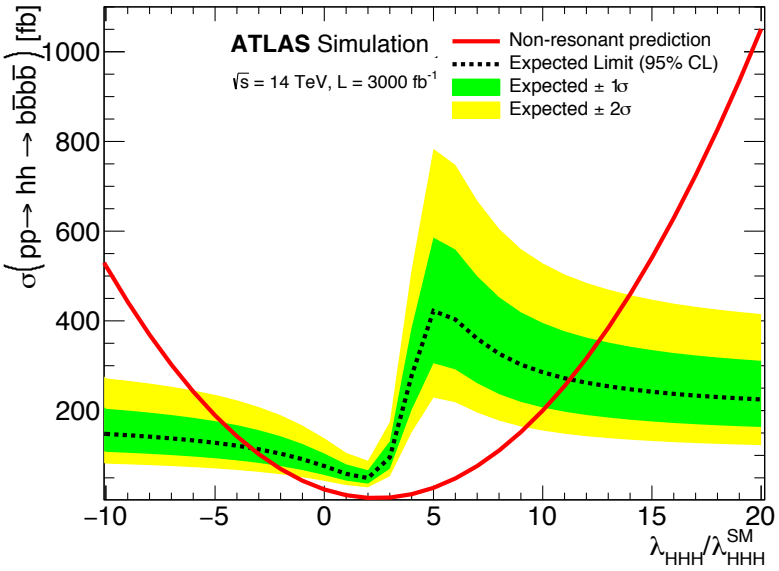


Figure 4.41: Upper 95% C.L. limit on HH production cross section versus the Higgs Boson self-coupling from the $HH \to b\bar{b}b\bar{b}$ analysis.

$HH \to b\bar{b}\gamma\gamma$

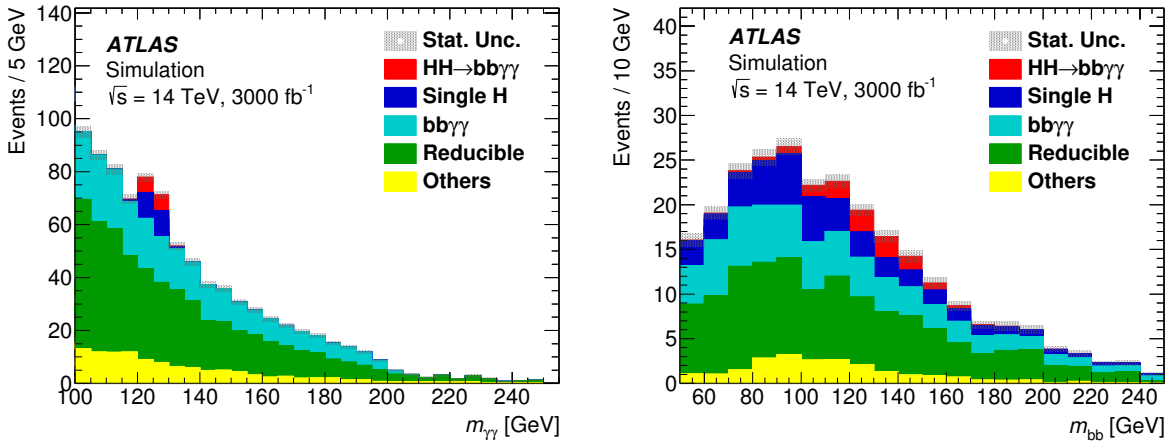
One of the most promising channels to measure the Higgs self-coupling is the $H(\to b\bar{b})H(\to \gamma\gamma)$ final state, which has recently been studied [46]. This channel profits from a clean HH signal extraction thanks to the narrow mass peak of the $H \to \gamma\gamma$ decay. The low branching ratio (0.26 %) for this decay mode leads to low expected signal rates. To emulate the detector response the final-state particles at truth level are smeared according to the expected detector resolutions assuming a pile-up scenario of $\langle\mu\rangle = 200$. In addition, the expected efficiencies and fake rates for identifying b-jets and photons are applied. Thus this analysis depends on the performance of the upgraded tracker for b-tagging described in Section 4.3.2, and photon identification described in Section 4.4.2.

The main backgrounds in this analysis can be separated into those with a single Higgs boson in the final state and the continuum background. The latter comprises contributions containing multiple jets and photons, such as $b\bar{b}\gamma\gamma$, $c\bar{c}\gamma\gamma$, $jj\gamma\gamma$, $b\bar{b}j\gamma$, $c\bar{c}j\gamma$, $b\bar{b}jj$ events. Other contributions arise from $Z(b\bar{b})\gamma\gamma$ and $t\bar{t}$ production.

To select the $H(b\bar{b})H(\gamma\gamma)$ events, the following event selection cuts are applied. Only events accepted by the diphoton trigger, which requires each photon to have a p_{T} greater than 25 GeV within $|\eta| < 2.5$ are considered. Two photons which should have $p_{\mathrm{T}} > 30$ GeV and be within the electromagnetic calorimeter acceptance ($|\eta| < 1.37$ or $1.52 < |\eta| < 2.37$)

are required. To ensure they are isolated, they are required to be separated by $\Delta R_{\gamma\gamma} > 0.4$ from other photons or jets found in the event. Furthermore, $\Delta R_{\gamma\gamma} < 2.0$ is also required as they come from the same decay. The two-photon system should fulfil $p_{\mathrm{T}} > 80$ GeV and the invariant mass must lie within $122 < m_{\gamma\gamma} < 128$ GeV. Events including isolated electrons and muons with $p_{\mathrm{T}} > 25$ GeV and $|\eta| < 2.5$ are rejected. These events are further required to contain at most five jets with $p_{\mathrm{T}} > 30$ GeV and $|\eta| < 2.5$, at least two of these jets must be tagged as b-jets. These b-jets have to lie within the pseudorapidity range $|\eta| < 2.4$, the leading b-jet is required to have $p_{\mathrm{T}} > 40$ GeV and the sub-leading jet p_{T} must be greater than 30 GeV. The $b\bar{b}$ system must have $p_{\mathrm{T}} > 80$ GeV, $100 < m_{b\bar{b}} < 150$ GeV and is required to fulfil $0.4 < \Delta R_{b\bar{b}} < 2.0$. The events passing the above selection criteria are split into two categories depending on the photon pseudorapidities. One category contains events where both photons are located in the barrel region of the electromagnetic calorimeter ($|\eta| < 1.37$), all other events are placed in the second category.

The selection efficiency for the signal is found to be $2.85 \pm 0.01\%$. The invariant mass distribution of the dijet and diphoton pairs is shown in Figure 4.42. Combining the two categories, the expected number of signal events is 9.54 ± 0.03 and 90.9 ± 2.0 for the background after selecting the $m(\gamma\gamma)$ and $m(b\bar{b})$ mass ranges described in the previous paragraph. The dominant backgrounds are from $b\bar{b}\gamma\gamma$ and $b\bar{b}j\gamma$ production. Systematic uncertainties are not considered in this study.



(a) diphoton mass

(b) dijet mass

Figure 4.42: Dijet and diphoton invariant mass distributions of expected signal and background components for $\langle\mu\rangle = 200$, assuming a b-tagging efficiency of 70%. All the selection cuts besides the cuts on the diphoton and b-jet invariant mass have been applied.

Having split the events into two categories improves the significance by 5% and leads to an expected statistical sensitivity of 1.05σ. The 95% C.L. upper limit on the cross sections is shown in Figure 4.43. The Higgs boson self-coupling would be constrained at 95% C.L. to $-0.9 < \lambda_{HHH}/\lambda_{SM} < 7.7$.

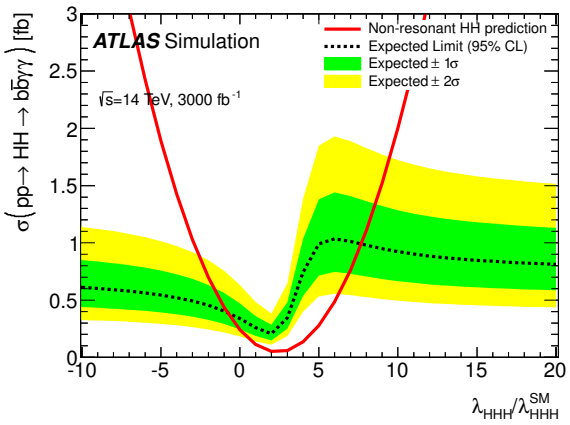


Figure 4.43: Upper 95% C.L. limit on HH production cross section versus the Higgs Boson self coupling from the $HH \to b\bar{b}\gamma\gamma$ analysis.

4.6.5 $Z' \to t\bar{t}$

Several theories of physics beyond the Standard Model predict new particles with masses at the TeV scale that decay primarily to a pair of top quarks. Thus, a $t\bar{t}$ resonance search is a benchmark analysis for evaluating BSM physics prospects at the HL-LHC. Furthermore, at higher masses of the new heavy particles, the produced top quarks will be highly boosted, leading to hadronic jets encompassing a very dense tracking environment. In particular, in this analysis the b-tagging of highly collimated jets (at high p_{T}) is very important. These searches will therefore depend on the performance of the upgraded tracker for tracking in dense environments described in Section 4.5.

A $t\bar{t}$ resonance would cause a local excess or deficit in the $t\bar{t}$ mass spectrum relative to that predicted by the Standard Model. A study of the prospects for a search for such a deviation has been performed [47] on $t\bar{t}$ pairs selected from events in MC simulations of proton-proton collisions with a centre-of-mass energy of 14 TeV, for a total integrated luminosity of 3000 fb^{-1}. The effects of an upgraded ATLAS detector are taken into account by applying energy smearing, object efficiencies and fake rates to truth level quantities, following parameterisations based on detector performance studies with full simulation and HL-LHC conditions. The study uses the expected upper limits on the production of $Z' \to t\bar{t}$ to benchmark the performance. Specifically a Leptophobic Z' arising from topcolour-assisted technicolour [48–51] is considered; such particles decay to $t\bar{t}$ with a large (33%) branching ratio and have a width that is much smaller than the experimental top-pair mass resolution. The most recent ATLAS search [52], using 3.2 fb^{-1} of data taken at $\sqrt{s} = 13$ TeV, excludes such Z' bosons for masses less than 2.0 TeV.

The search is performed in the single lepton plus jets decay channel ($t\bar{t} \to WbWb \to \ell\nu bqq'b$). It is carried out as follows. The invariant mass of selected $t\bar{t}$ pairs in Monte Carlo simulation for signal and background is reconstructed, and an expected mass spectrum

is prepared under the signal-plus-background hypothesis and under the background-only hypothesis. The limit setting procedure uses a likelihood model based on the binned mass spectrum to calculate the expected upper cross section limits for a benchmark signal model, for a range of resonance masses. The upper cross section limits are compared to the theoretical signal cross section to estimate the mass reach of the analysis. The search method is independent of the signal model, and can be adapted to test specific mass, resonance width, and cross section predictions of different theoretical models

Events are required to have exactly one lepton (electron or muon). The electron (muon) must have $p_{\mathrm{T}} > 30$ GeV (25 GeV), above single-lepton trigger thresholds. The lepton pseudorapidity must lie within $|\eta| < 1.37$ or $1.52 < |\eta| < 2.47$ for electrons and $|\eta| < 2.5$ for muons. There must be $E_{\mathrm{T}}^{\mathrm{miss}} > 20$ GeV and $E_{\mathrm{T}}^{\mathrm{miss}} + m_{\mathrm{T}}^{W} > 60$ GeV. Events must contain at least one b-tagged jet. These requirements, inherited from the Run-1 analysis [53], are imposed with the aim of suppressing the reducible backgrounds, the largest of which is W+jets. Events are separated into topological decay channels: boosted and resolved. In a boosted event, all the decay products of the hadronically decaying top quark, t_{had}, are detected inside one large-R jet (an anti-k_t jet with radius parameter $R = 1.0$). In a resolved event, the jet decay products of t_{had} and the leptonically decaying top, t_{lep}, are detected as well-separated small-R jets

Events passing the preselection are initially tested against the boosted selection. A boosted event must contain at least one small-R jet such that $\Delta R(\text{jet}, \text{lepton}) < 1.5$. If there is more than one jet that meets this criteria then the highest p_{T} jet is chosen as the candidate for the b-jet decaying from the leptonic top. This jet is referred to as the selected jet, j_{sel}. Additionally, boosted events must contain at least one large-R jet such that:

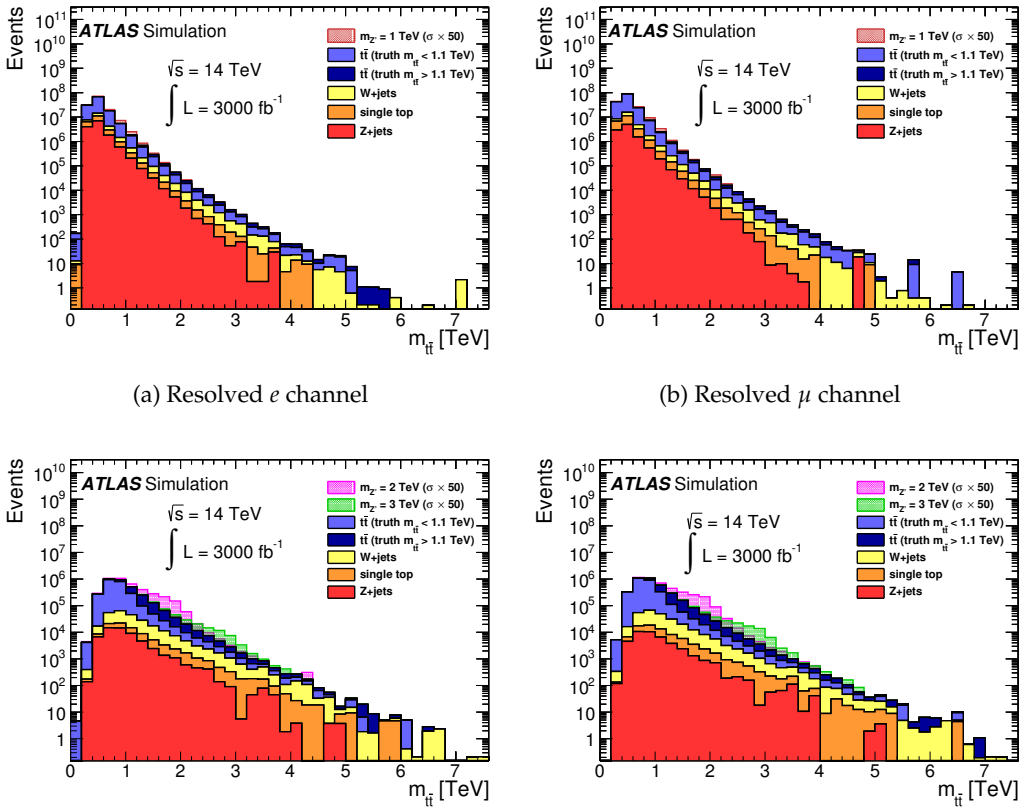
- $\Delta R(\text{large-}R\text{ jet}, j_{\mathrm{sel}}) > 1.5$
- $\Delta\phi(\text{large-}R\text{ jet}, \text{lepton}) > 2.3$

If more than one large jet satisfies these requirements, the highest p_{T} jet is chosen and is taken to comprise the decay products of the hadronically decaying top.

Preselected events failing the boosted selection that contain at least four small-R jets with $p_{\mathrm{T}} > 25$ GeV and $|\eta| < 2.8$ are classified as resolved events.

After this selection the remaining background is dominated by $t\bar{t}$ events. The invariant mass of $t\bar{t}$ pair candidate is then reconstructed for events selected as consistent with semi-leptonic $t\bar{t}$ decay. This is done by requiring hadronic jets and the reconstruction of a leptonically decaying W boson (W_{lep}) from the missing transverse momentum and lepton candidate[15)]. The events are classified into two categories:

[15] The missing p_x and p_y in an event is assumed to be due to the neutrino p_x and p_y. The neutrino p_z component is determined by imposing a W boson mass constraint on the mass of the neutrino-lepton system. This yields a quadratic equation that is solved for the neutrino p_z. If there is one complex solution, $|p_z|$ is taken to be the real part. In the case of two real solutions, $|p_z|$ is taken to be the smallest solution in a boosted event, while both solutions are tested by the χ^2 algorithm in a resolved event.



(a) Resolved e channel

(b) Resolved μ channel

(c) Boosted e channel

(d) Boosted μ channel

Figure 4.44: Mass spectra used in the search for $t\bar{t}$ resonances: (a) resolved e channel (b) resolved μ channel (c) boosted e channel , and (d) boosted μ channel.

Boosted events The leptonically decaying top quark, t_{lep}, is reconstructed from W_{lep} and j_{sel}, and the hadronically decaying top quark, t_{had}, from the large-R jet.

Resolved events A χ^2 algorithm [47] is used to iteratively test all combinations of four small-R jets in the event and identify the best candidates for the hadronic decay products. If there are two real solutions for $|p_z|$, each W_{lep} scenario is also tested in the algorithm. The combination with the lowest χ^2 is chosen, and a cut $\chi^2 < 10$ is applied to events, ensuring that the reconstructed top quarks and W_{had} in selected events have a mass close to the expected value.

A statistical analysis is performed to determine the expected upper limits that can be set on the signal cross section in the absence of signal. The $t\bar{t}$ invariant mass distribution is constructed for the background-only hypothesis, and for signal-plus-background hypotheses with varying signal strength μ, where $\mu = 0$ corresponds to the background only model and $\mu = 1$ is the prediction of the signal model. A likelihood function based on the binned $t\bar{t}$ mass spectrum is used to exclude values of μ with 95% confidence. The expected upper

limit set on the signal cross section is the largest value of μ that is not excluded with 95% confidence. This procedure is carried out for each signal mass. A luminosity uncertainty of $\pm 3\%$ is included. A systematic uncertainty on the number of events in each channel is applied: $\pm 8.8\%$ on resolved signal events, $\pm 18.0\%$ on the boosted signal events, $\pm 10.8\%$ on the resolved background events and $\pm 13.4\%$ on the boosted background events. These systematic uncertainties are extrapolated from the Run-1 analysis [53], the dominant experimental systematic uncertainties are those from b-tagging (for the boosted signal events), jet energy and mass scales (for resolved and boosted background events), and luminosity (for resolved signal events).

Stacked $t\bar{t}$ mass spectra for all included backgrounds and two signal points are shown for each channel in Figure 4.44. Most signal events fall into the boosted channels, where the excess of events is localised around the signal mass. Therefore the boosted channel dominates the limit setting. The expected upper limits set on the signal cross section $\times$ branching ratio as a function of the signal mass are shown in Figure 4.45. The mass reach of the search is estimated to be 4 TeV for the leptophobic topcolour-assisted technicolour Z' boson being used as a benchmark. At these masses the top candidates will tend to produce b-jets with $P_{\mathrm{T}} > 600\,\mathrm{GeV}$. Thus to be sensitive in this mass region, it is critical to maintain stable track reconstruction efficiency with increasing P_{T}, similar to the performance shown in Figure 4.28.

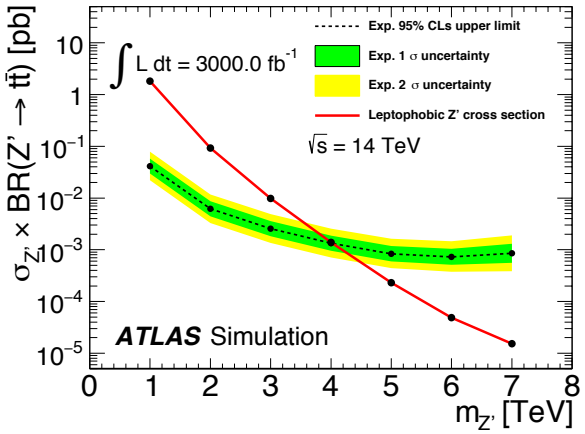


Figure 4.45: The expected upper limit on the cross section $\times$ branching ratio of a leptophobic topcolour-assisted technicolour Z' boson for masses in the range 1-7 TeV, assuming an integrated luminosity of 3000 fb^{-1} at $\sqrt{s} = 14$ TeV.

5 ITk Silicon Strip Detector Outline

The silicon-strip detector for the ITk is situated just outside of the pixel detector with a silicon area ∼165 m^2. It consists of a central barrel region between $z = \pm 1.4$ m and two end-caps that extend the length of the ITk Strip Detector to $z = \pm 3$ m. The strip barrel consists of four cylinders, each of length of 2.8 m, that surround the beam-line. The strip end-caps have six disks on each side (named end-cap A and end-cap C) to provide optimal coverage. The strip system covers $\pm$ 2.5 units of rapidity. In Figure 5.1 only the ITk Strip Detector barrel layers and end-cap disk are shown (see Chapter 3).

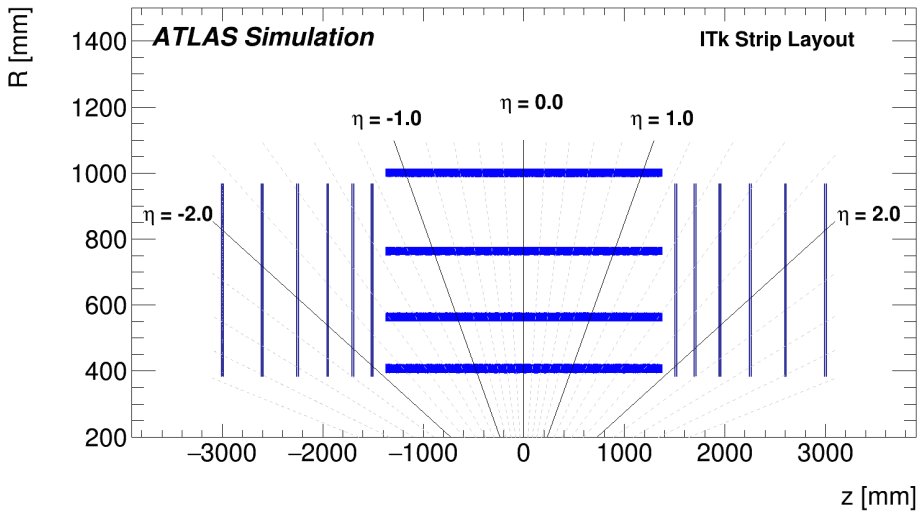


Figure 5.1: The Layout of the ITk Strip Detector. Here only the upper half of the Strip Detector is shown. The horizontal axis is the axis along the beam line with zero being the interaction point.

The basic mechanical building blocks of the barrel and the end-caps are the stave and petal, respectively. These units, also called local supports, consist of a low mass central stave/petal core that provides the mechanical rigidity, support for the modules and houses the common electrical, optical and cooling services. It also provides the accurate alignment and fixation points. All the power and data links are channeled through an end-of-substructure card, which forms the interface to the off-detector electronics. Chapter 9 provides technical details and an overview of the R&D for the stave and petal local supports, including the on-structure electronics.

The four barrel layers consist of 392 staves with modules on both sides (196 staves on each side of z = 0). Each barrel stave is populated with 28 modules (14 on each stave side). The

strips on the inner two cylinders are 24.1 mm long (short-strips) and those on the outer two cylinders are 48.2 mm long (long-strips). The strips (modules) on each side of the stave are rotated with respect to the beam line (z-axis) by a ± 26 mrad such that there is a total rotation between the strips on each side of the stave of 52 mrad.

In the end-caps each disk is populated with 32 identical petals. Each petal has nine modules on each side with six different sensor geometries to cover the wedge shaped petal surface. In the end-cap sensors a stereo angle of 20 mrad is directly implemented in the sensors to achieve a total stereo angle of 40 mrad. The staves and petals are loaded into global structures (see Chapter 10) within a common mechanics for the ATLAS ITk (see Chapter 18).

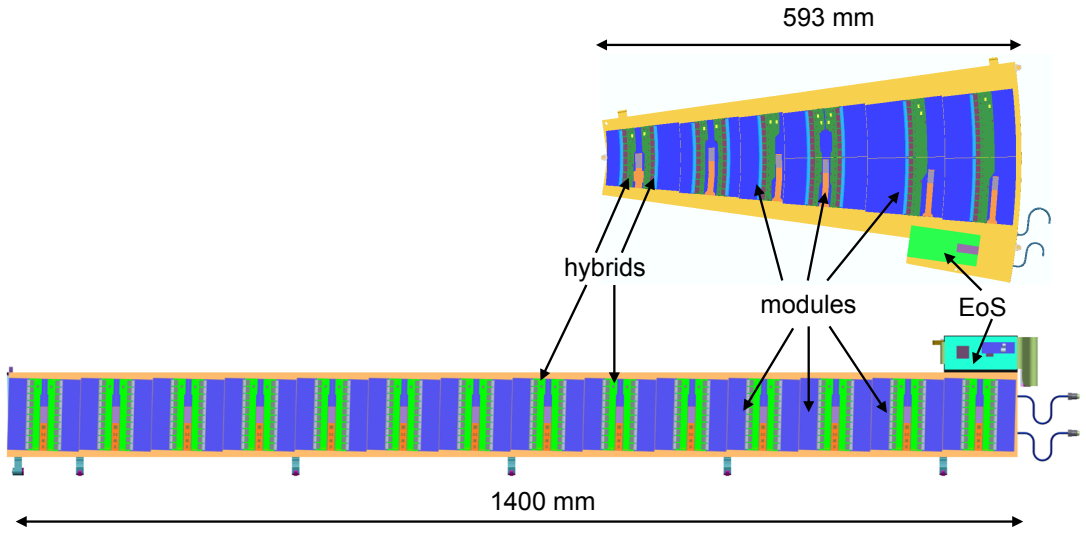


Figure 5.2: Local support components overview: End-cap petal (upper) and barrel stave (lower) components overview. In both cases modules are mounted directly onto a rigid carbon-fibre sandwich structure. The interface to the off-detector electronics is the End-of-Substructure card at one of the ends of the stave or petal. Titanium cooling pipes are directly embedded into the support structures.

5.1 System Concept

From the start of the design phase for the ITk Strip Detector an overall concept was developed which is applicable for the barrel layers and the end-cap disks. Based on the experiences during the construction of the current ATLAS SCT, simplicity in the design was pursued for improved producibility: Silicon modules glued directly onto cooled carbon fibre planks which are designed to reduce radiation length. Kapton service tapes are

directly co-cured onto carbon fibre skins. The advantage of this concept is that all components are independently testable prior to construction, thus allowing early systems-like testing. Additionally the concept allows for an insertion from the end of the barrel or from the side of the end-caps thus, during construction, enabling a possible replacement of misfunctioning elements. The choice of the petal geometry for the end-caps was driven by the decision to implement strips which are pointing to the centre of the beam pipe thus allowing a constant phi coordinate along the strip length. At the same time the concept of trapezoidal sensors opens the possibility to follow the same concept for the local supports as for the barrel. All material choices are the same for barrel and end-cap. The end-cap layout has evolved with time and with it the petal design, the sensor design, and the module designs.

The concept of radial strips has been successfully implemented in the current strip trackers of ATLAS and CMS. Lessons learned during the construction phase of the ATLAS strip end-caps have lead us to the concept with high integration of services and only a limited number of connections that is realised on the petals.

5.2 Numbers of Staves, Petals and other Components of the ITk Strip Detector

An overview of the overall number of staves, petals, modules, hybrids, front-end chips (ABCStar) and the silicon area is given in Table 5.1. These are the numbers of items to be installed in the ITk, e.g. the number of modules is 17,888. Spares are not included in this table. The number of parts to be produced during the production including yields and spares are summarised in Chapter 13.

5.3 Design of the Strip Modules

The basic unit of the ITk Strip Detector is the silicon-strip module. A module consists of one sensor and one or two low-mass PCB's, called hybrids, hosting the read-out ASICs (ABCStar and HCCStar). Due to the large number of modules required for the ITk Strip Detector, the modules have been designed with mass production and low cost in mind. The design is equally focused on material reduction with the elimination of a substrate between the hybrid and the sensor. This takes advantage of the heat path through the large cross-sectional area to the underlying mechanical support with an embedded cooling. An exploded view of a short-strip module as an example is shown in Figure 5.3.

The ITk Strip modules are constructed by directly gluing kapton flex hybrids to silicon sensors with electronics-grade epoxy. Various different strip lengths and geometries are foreseen, depending on the planned location of the module within the detector. For the

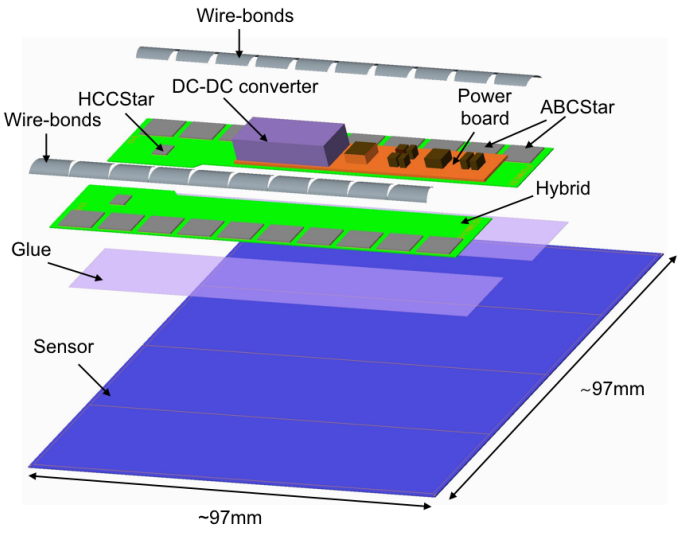


Figure 5.3: Exploded view of a short-strip barrel module with all relevant components. Long-strip modules and end-cap modules feature the same component groups.

barrel, two strip lengths are used: long strips are suitable in the lower occupancy region at larger radii (layers L2 and L3), whereas further subdivision with shorter strips is required at lower radii (layers L0 and L1). Therefore two different module types are required for the barrel section: the so-called short-strip and long-strip barrel modules where "short" and "long" refers to the strip length.

The short-strip barrel modules contain two hybrids, each with ten ABCStar read-out ASICs and long-strip modules contain one hybrid with ten ABCStar. Each petal has nine modules on each side organised in six subsegments referred to as rings (R0-R5) (see Figure 5.2); e.g. all R0 sensors of 32 petals in one disk will represent a ring around the beam axis in the $R\phi$ plane. The three inner rings (R0-R2) at the lowest radii from the beam axis have one module each with one or two hybrids, while the outer three rings (R3-R5) have two modules butted side-by-side, each with one hybrid spanning over the two neighbouring modules. Covering such a complex geometry over a large area requires six different sensor geometries and thirteen individual hybrids. The details of the modules for the barrel and the end-caps are described in the three following chapters: in Chapter 6 the various active components to form a silicon strip module including the silicon strip sensor and the ASICs are described. The layout of the hybrids and the power boards required for the modules and the production steps to build modules including the planned quality assurance measures are summarised in Chapter 7. The results of electrical characterisations and test beam studies of prototype modules are shown in Chapter 8.

As the final prototype chips ABCStar and HCCStar were not available at the prototype

Table 5.1: Number of components for the ITk Strip Detector in barrel (top half) and end-cap (bottom half). The numbers for the barrel are for the full barrel with 2.8 m length. The numbers for the end-caps (EC) are given both for one and both end-caps.

Barrel Layer:	**Radius [mm]**	**# of staves**	**# of modules**	**# of hybrids**	**# of of ABCStar**	**# of channels**	**Area [m^2]**
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABCStar**	**# of channels**	**Area [m^2]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

stage, all R&D studies presented in this TDR are based on the prototype chips ABC130 and HCC130.

5.4 Overall Electronics Architecture

Charged particles passing through the sensor create a signal charge within the silicon sensor diode. This signal is transmitted through a wire to the front-end chip, the ATLAS Binary Chip (ABCStar) containing 256 pre-amplifiers and discriminators together with the L0 buffer, event builder and cluster finder. With the front-end chip ABCStar the signal on each channel is amplified, shaped and then discriminated to provide a binary output. Details of the design of the ABCStar can be found in Chapter 6. Depending on the sensor type (short barrel strips, long barrel strips or one of the six shapes for the end-cap region) up to 12 ABCStar ASICs are grouped on to one hybrid. Each hybrid has a Hybrid Controller Chip (HCCStar) that interfaces the stave/petal service bus and the front-end ASICs on the

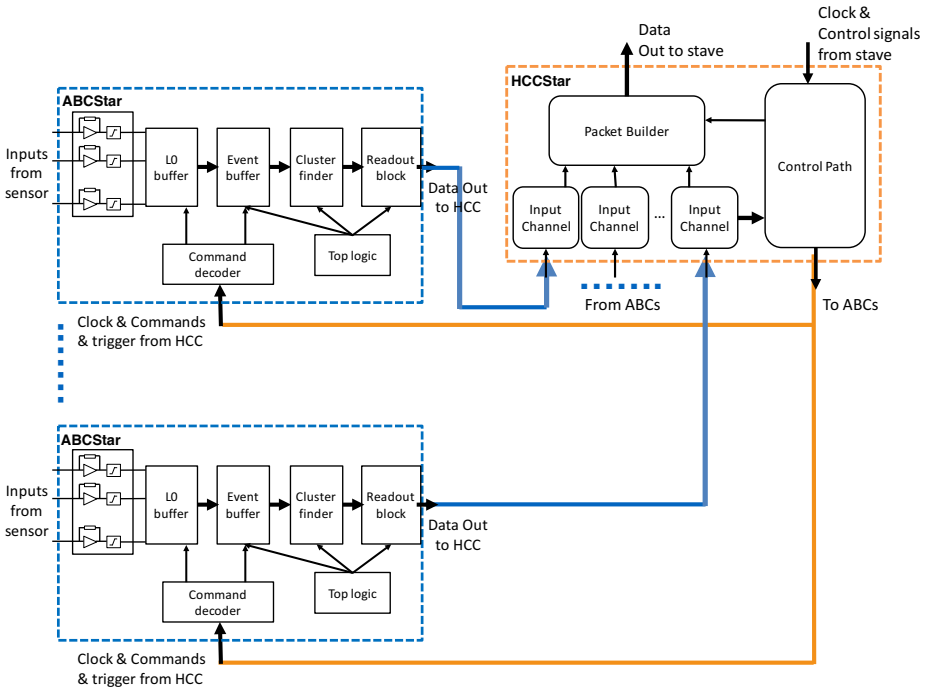


Figure 5.4: Simplistic schematic of a hybrid for the ITk strip modules.

Strip Detector hybrids. The HCCStar receives the signals from the ABCStar, builds packets and moves them on. It also receives the clock and control signals (TTC) and distributes those to the ABCStar. A simplified functionality diagram of the electronics on the hybrids is shown in Figure 5.4. The ABCStar and HCCStar are planned to be produced in a 130 nm technology[1)], which has the benefits of reduced power, improved radiation tolerance, and higher circuit density compared to larger feature size technologies (for example 250 nm technology), while having a reasonable price for both prototyping and production. It has been shown to be the optimal technology choice enabling a low-noise performance for the pre-amplifier. The risk of the 130 nm technology being discontinued in industry has been addressed, and access to this technology has been secured by frame contracts via CERN. Additionally, the availability of this technology is supported by the high demand from military industry and a number of commercial technologies dependent on it. Details of the ABCStar and the HCCStar including radiation tolerance studies with prototype chips are given in Chapter 6.

A low-voltage power converter and a high-voltage switching circuit are combined in one power board which is located on the sensor between the two hybrids. The power board also hosts the autonomous monitor and control (AMAC) chip, providing module level environmental measurements and control, including the module power up sequence. A number of system and chip design approaches, as well as QC procedures, guarantee a robust and

[1] Global Foundries, using a former IBM foundry

reliable module power service. Details are given in Chapter 6. The power board connects to the End of Substructure Card (EoS) and is distributed to each hybrid via a power bus. A power interface connects each hybrid to the power bus. The main electrical components on a short-strip stave are shown as an example in Figure 5.5 to give an overview of the main electrical components of the ITk Strip Detector.

Trigger, Timing, and Control (TTC) signals arriving from the off-detector systems are sent from the EoS to each HCCStar via the TTC bus on the bus-tape. The TTC consists of a 40 MHz system clock, a serial command/L0 trigger, and a R3/L1 trigger that are sent to each HCCStar (see Chapter 9). The TTC bus and data lines and power bus are integrated into a single copper/kapton bus tape that is co-cured onto the stave core. The EoS includes a low power GigaBit Transceiver (lpGBTx) that interfaces with the HCC130 ASICs and a Versatile link (VTRx+) fibre optic driver [54]. This is described in detail in Section 12.1.

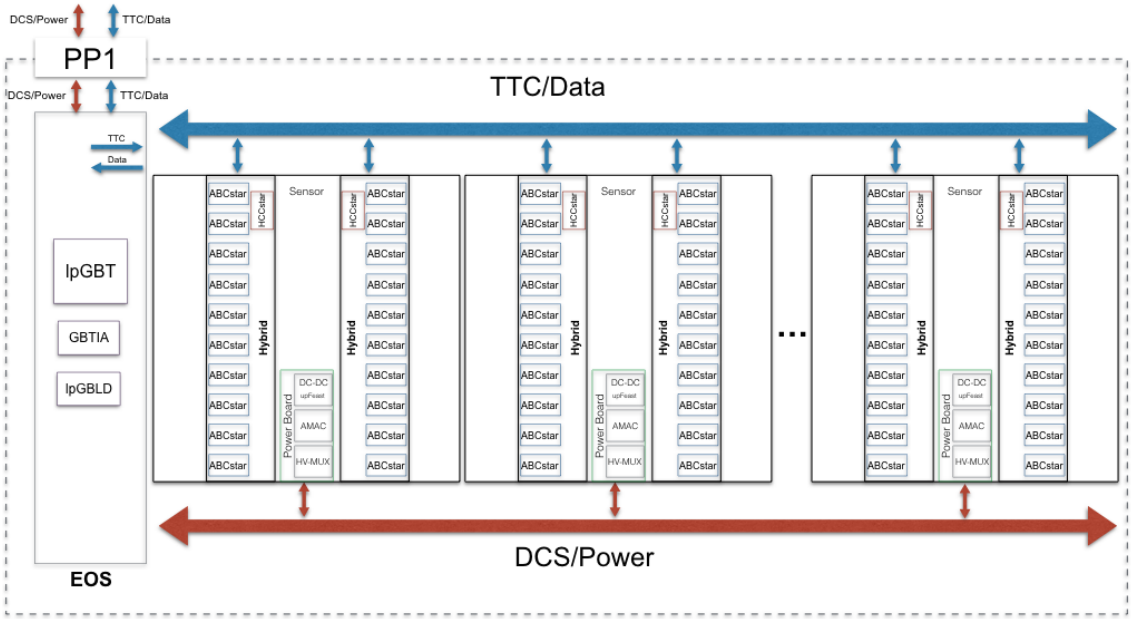


Figure 5.5: Overview of the electronics components of the ITk Strip Detector located within the active area of the detector. Timing, Triggering and Control (TTC), power and DCS are interfaced to the stave/petal at the EoS card.

5.4.1 Developments for 1 MHz/400 kHz Trigger Rates - the ABCStar and HCCStar

Since the design of the prototype ABC130, the ATLAS upgrade trigger requirement has been changed, increasing from L0/L1 rates of 500 kHz /200 kHz to 1 MHz/400 kHz. In addition, studies of trigger timing and latency have shown that a chain of at most three

ABC130 devices may be used in high occupancy regions of the ITk Strip Detector. Taken together, these issues have led the project to re-evaluate the architecture of the on-detector electronics and adopt a new approach: a so-called "star architecture" with point-to-point connections between each ABCStar and the HCCStar on the hybrid (see Figure 5.6).
In this "star" architecture the HCCStar builds and transmits module wide events, making more efficient use of the available bandwidth compared to what is possible with the ABC130. Taken together these changes permit full detector read-out at 1 MHz L0 rate and a significant simplification of the system architecture. However, to support this new topology, the hybrid will require one additional routing layer and, to maintain a safety factor of two on bandwidth, the Hybrid Controller Chip HCC will require 640 Mbit down-link bandwidth back to the End of Substructure card.

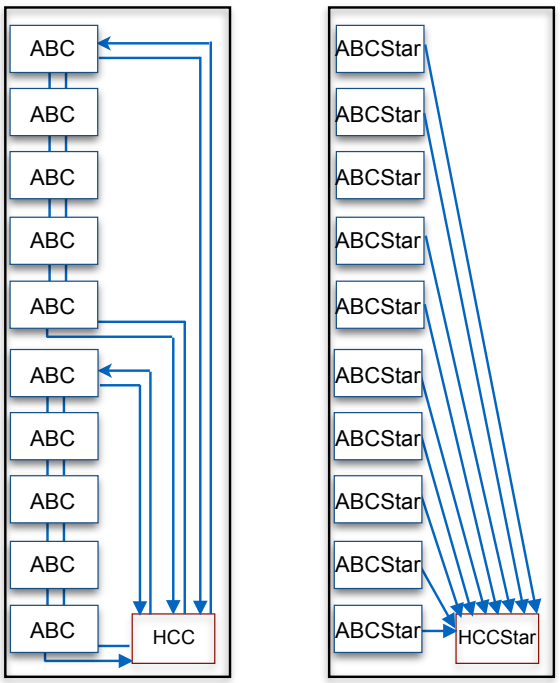


Figure 5.6: Sketch of the original daisy chain signal routing in comparison to the new star design for the ITk Strip Detector.

Serial transfer of data to the HCC130 was changed to direct communication from all the ABC130 ASICs to the HCC130 hence the new ABCStar and HCCStar. The "star" configuration removed a bottleneck in data transfer to the HCC, which had considerable bandwidth still available. While both ASICs required changes, the HCCStar required nearly a complete redesign as it must now build events in parallel from fragments coming from all the ABCStar ASICs. The specifications of the ABCStar and HCCStar are summarised in Chapter 6.2.2 and Chapter 6.2.5 respectively.

5.5 Powering Scheme for Low and High Voltage

With the increase in the total number of channels in the system compared to the current ATLAS Inner Detector, and despite a reduction in the power consumption per channel, more power is required for the ITk Strip Detector compared to the current SCT. In addition, there is no space for extra cables from the counting rooms to the cavern. Moreover, adding more cables would lead to extra material. Therefore, a more efficient way to provide power to the modules is required for the ITk. The baseline for the ITk Strip Detector is point-of-load DC to DC conversion (DC-DC), with off-detector power supplies at a higher voltage, reducing the current on the cables and the ohmic losses [55]. On-detector, buck DC-DC converters lower the voltage to that required by the on-detector electronics. This requires the design of radiation hard DC-DC converters. Details on the powering of the ITk Strip Detector are given in Chapter 17.

Similarly for high voltage distribution an upgraded and more efficient HV biasing of the sensors is needed. For instance, if existing ATLAS HV cables are re-used, groups of four sensors or more will need to be connected in parallel and this would lead to the loss of the other modules on the same bias line, should one sensor fail to high current. In order to avoid such potential losses, the approach for the ITk Strip Detector consists of having groups of modules on one side of the stave or petal powered by a single HV bias line. Each sensor can in turn be disconnected from the bias line with HV multiplexer switch (MUX) which is controlled through the detector control system (DCS) (for details see Chapter 6.4.1).

6 Components of the Silicon Strip Modules

In this chapter the components of modules for the ITk Strip Detector are described in detail. Performance studies that demonstrate the required functionality are described including, where appropriate, studies performed after irradiation.

6.1 The Silicon Strip Sensor

In the barrel region, the sensors are square, with nearly the maximum active size that can safely be used from the wafer area. In the end-cap, the sensors are roughly trapezoidal with two curved edges, which are concentric arcs of circles centred at the centre of the disk. The strips are AC-coupled with n-type implants in a p-type float-zone silicon bulk (n^+-in-p FZ). Bias resistors are implemented by poly-silicon implants. Inter-strip isolation will be achieved by p-stop implants, uniform p-spray, or a combination of both. This type of sensor collects electrons and has no radiation induced type inversion. The target thickness is between 300-320 μm. Radiation tolerance is a key requirement for the strip sensors; here the requirements are to withstand the expected maximum fluence of 8.1 $\times 10^{14}$ n_{eq}/cm^2 as well as an ionising dose of 33.3 MRad and to operate up to 700 V. In order to allow for uncertainties in fluence calculations, a safety factor of 1.5 is imposed for the fluence and ionising dose (see Chapter 3).

The main reason for choosing n^+-in-p technology over the p-in-n used in the current ATLAS SCT is the large difference in the amount of signal after irradiation [56]. In the range of 8-10$\times$ $10^{14} n_{eq}/cm^2$ n^+-in-p sensors deliver a factor of two more charge. A detailed list of specifications for the sensor before and after irradiation is given in Table 6.1. An n^+-in-n-technology is not considered for a number of reasons: n^+-in-n is significantly higher in costs relative to n^+-in-p as the required double-sided processing reduces yield and adds more complicated steps in the overall processing; depending on foundry the costs are 20-50% higher. There are fewer foundries producing n^+-in-n sensors compared to n^+-in-p sensors, and the foundries that do exist have lower volume capacity. The chosen n^+-in-p technology has comparable signal sizes as achieved with n^+-in-n sensors. The only significant benefit for n^+-in-n is that sensor edges are at ground whereas with n^+-in-p they are at the bias potential. However, this advantage of n^+-in-n is diminished after type inversion and further irradiation. There are multiple methods available to address the issues with the edge being at bias potential in n^+-in-p devices. ? The baseline design of the silicon sensor is based on 6-inch wafer technology. 8-inch was also considered, but not discussed in detail in

this document. The number of 8-inch production lines compatible with the sensor requirements is very limited. In addition, no large scale production of sensors has been attempted on a 8-inch production line. As such, cost, schedule and yield would be highly uncertain.

The design of the barrel sensors foresees an active area of 96.640 $\times$ 96.669 mm^2. There are 1280 read-out strips and a field-shaping strip at each side in parallel to the other strips, giving a strip pitch of 75.5 μm. The strips are parallel to the edge of the sensor. On a stave, the stereo angle is achieved by rotating the modules on both sides by 26 mrad. There are two types of barrel sensors: one has four rows of short strips in z-direction (24.10 mm) and the other has two rows of longer strips (48.20 mm) for the short-strip and long-strip modules, respectively.

The petal sensors require radial strips (i.e. pointing to the beam-axis) to give a measurement of the Rϕ coordinate. As a result, these sensors have a wedge shape with curved edges. The dimensions of the sensors have been chosen to use as few silicon wafers as possible with 32 petals per disk and fully covering the radial range required by the layout. The 40 mrad stereo angle between strips on opposite sides of a petal is achieved by rotating the strips 20 mrad within the sensors. The strip lengths are chosen to balance the strip occupancy with the shortest strips closest to the beam region. The segmentation was also determined by the maximum latency requirement of the read-out, which is closely related to the occupancy and channel count. The strip pitch was constrained to be as close as possible to the barrel pitch (75.5 μm) at the bond pad region to allow direct wire bonding between the read-out ASIC and the sensor. This results in three rings (R0, R1, and R3) with four strip rows and three rings (R2, R4 and R5) with two rows. In Table 6.2 the different sensor types with dimensions are summarised.

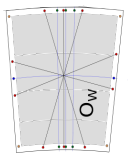
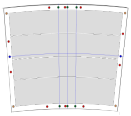
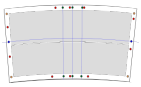
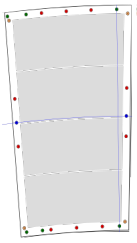
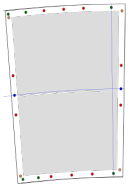
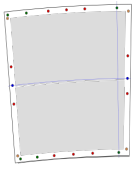
Two generations of barrel short-strip sensors have been fabricated: ATLAS07 [56–59] and ATLAS12 [60–64]. With ATLAS07, the performance of the baseline sensor technology (n^+-in-p FZ) with p-stop, p-spray and mixed isolation were shown to meet all specifications. The ATLAS12 series utilised p-stop isolation only and included a number of improvements. The ATLAS12 series have enhanced punch-through protection structures at the end of strips, a smaller inactive edge (450 μm in the longitudinal direction; 500 μm in the lateral direction), which reduces the dead region of the sensors and a modification to the bond pad layout to match the ABCStar read-out ASIC. The resistivity of the silicon is lower than specified for the ITk Strip Detector resulting in less collected charge than required for a good hit efficiency at the end-of-lifetime.

Miniature strip sensors (1 $\times$ 1 cm^2) have been included in the wafers of both series to enable an extensive irradiation and testing program [56, 58, 59, 61–64]; these studies include a full suite of surface and bulk properties evaluation before and after irradiations. A batch of 120 sensors with four rows of axial strips (ATLAS12A, see Figure 6.1) has been delivered for detailed studies of module, stave, and petal prototyping using the 130 nm ASIC set. In addition, a batch of 45 sensors with two rows of axial and two rows of "stereo (40 mrad

Table 6.1: Sensor specifications for the n^+-in-p-type sensor for the ITk Strip Detector.

Substrate Material	
Size	8-inch/200 mm or 6-inch/150 mm
Type	p-type FZ
Crystal orientation	<100>
Thickness (physical)	300-320 μm
Thickness (active)	>= 90% of physical thickness
Thickness tolerance	$\pm$ 5 %
Resistivity	$>$ 3 kΩcm
Oxygen concentration	1×10^{16} to 7×10^{17}cm^{-3}
Sensor specifications before irradiation	
Full depletion voltage	$<$ 330 V (preference for $<$ 150 V)
Maximum operating voltage	700 V
Poly-silicon bias resistors	1-2 MΩ
Inter-strip resistance	$>$ 10 $\times$ Rbias at 300 V at 23 °C
Inter-strip capacitance	$<$ 1 pF/cm at 300 V, measured at 100 kHz
Coupling capacitance	$>$ 20pF/cm at 1 kHz
Resistance of read-out Al strips	$<$ 15 Ω/cm
Resistance of n-implant strip	$<$ 20 kΩ/cm
Onset of micro-discharge at	$>$ 700 V
Total initial leakage current, including guard ring:	$<$ 0.1 μ A/cm^2 at 700 V at room temperature
Number of strip defects	$<$ 1% per strip and $<$ 1% per sensor
After irradiation (1.2×10^{15} n_{eq}/cm^2– 50 MRad)	
Onset of micro-discharge at	$>$ 700 V or $V_{fulldepletion}$+ 50 V after irradiation (if lower)
Inter-strip resistance:	> 10 $\times$ R_{bias} at 400 V and for T = $-$20 °C
Collected charge	$>$ 7500 electrons per MIP at 500V
Mechanical Specifications	
Dicing precision	$<$ $\pm$20μm or better
Sensor bow after process and dicing	$<$ 200 μm

Table 6.2: Overview of the number of silicon strip sensors per required shape with number of strip rows, channels and pitch for the ITk Strip Detector.

Sensor type	**Number of sensors**	**Shape**	**Number of rows**	**Channels per sensor**	**Min/max pitch** (μm)
Short-strips	3808	Square	4	5128	75.5
Long-strips	7168	Square	2	2564	75.5
EC Ring 0	768		4	4360	73.5/84
EC Ring 1	768		4	5640	69/81
EC Ring 2	768		2	3076	73.5/84
EC Ring 3	1536		4	3592	70.6/83.5
EC Ring 4	1536		2	2052	73.4/83.9
EC Ring 5	1536		2	2308	74.8/83.6

rotated)" strips (ATLAS12M) were delivered for prototyping a "stereo" sensor. In the following, the most relevant results are summarised.

6.1.1 Irradiation Facilities and Methodology

Irradiations were conducted at six different facilities:

- Neutrons at Ljubljana, Slovenia
- 23 MeV protons at Karlsruhe Institute of Technology, Germany
- 26 MeV protons at Birmingham, UK
- 800 MeV protons at Los Alamos, USA
- 70 MeV protons at Cyclotron and Radioisotope Centre (CYRIC), Japan
- 24 GeV protons at CERN

Since the annealing history is important for some of the studies, the sensor temperature is monitored if it cannot be controlled during irradiation. Facilities and setups that result in excursions significantly above the room temperature are not used. After irradiation the sensors are stored and shipped cold until a controlled annealing study is performed.

Given that the turn-around time is at least several weeks (sometimes months), repeated irradiations of the same sensor is impractical. Instead several devices of the same design are irradiated to different doses or fluences and compared after characterisation. To check for results reproducibility, several sensors are irradiated to the same dose or fluence. Additionally, some devices are cross-compared at different institutes. Typically miniature devices are used for such studies to facilitate the speed, cost, and ease of testing. They are about $\sim 1 \times 1\,\mathrm{cm}^2$ in size. They have the same design as the large sensors in production, but only one short row of short strips.

6.1.2 Charge Collection Efficiency after Irradiation

The charge collection from miniature p-bulk FZ sensors of 310-320 μm thickness using penetrating beta rays from ^{90}Sr sources was extensively studied. The charge measurements were performed using analogue read-out electronics running at LHC speeds and clustering techniques. Highly consistent results were obtained by the groups that participated in the measurements both prior to irradiation and after irradiations to the predicted fluences in the strip system. The collected signal charge versus the fluence at 500 V bias voltage is shown in Figure 6.2 and at 700 V in Figure 6.3. The charge collected depends on the particles used in the irradiation and the non-ionising energy loss (NIEL) fluence. Samples of ATLAS07 and ATLAS12 miniatures irradiated with beams with different proton energies and pions all show similar charge collection at a given NIEL fluence. After irradiation with

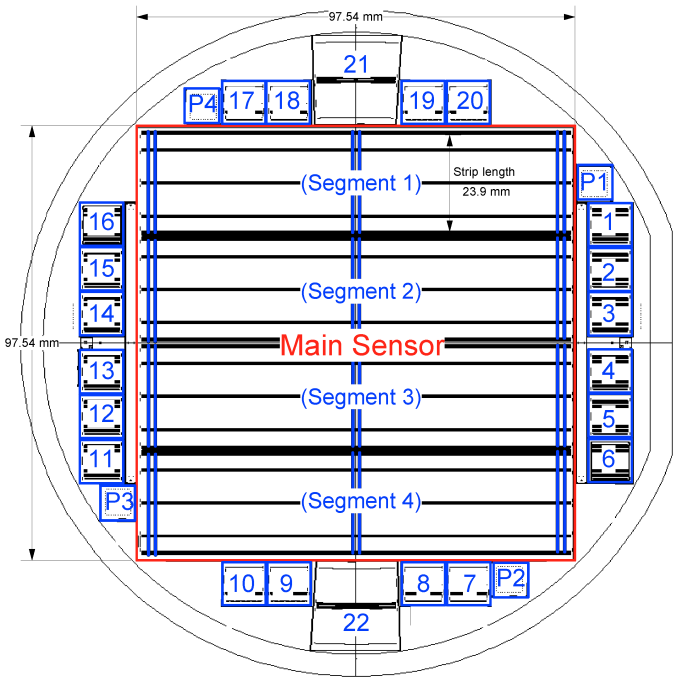


Figure 6.1: 6-inch wafer layout for the ATLAS12A prototype sensor. The main sensor in this prototype layout is 97.54 $\times$ 97.54 mm^2 with four rows of short strips.

reactor neutrons, the charge collected is lower relative to the charged particle irradiations as seen in previous studies [65]. ATLAS07 sensors have a larger collected charge than the ATLAS12 after neutron irradiation due to higher initial resistivity and therefore lower depletion voltages of the ATLAS12 sensors; this measured difference drives the sensor resistivity requirements in Table 6.1. All these charge collection differences diminish with increasing irradiation fluence and bias voltage. These results were also verified by independent measurements using an electron beam at the DESY-II Test Beam Facility.

The measured collected charge of the ATLAS07 sensors after neutron irradiation is used as a conservative estimate of the expected signal size (in electrons) at the end of lifetime for the strip system; the production sensors will have a larger charge as the resistivity will be at least as high as the ATLAS07 and the fluence would be from a mix of neutral and charged particles. The data is fit to interpolate between measurements [65]. Using a safety factor of 1.5 for the expected fluence, the estimated collected charge for a bias voltage of 500 V at the end of lifetime ranges from 11,500-17,300 e^- for the region of highest irradiation for the different module types. This can be increased to 14,000-19,500 e^- by increasing the bias voltage to 700 V.

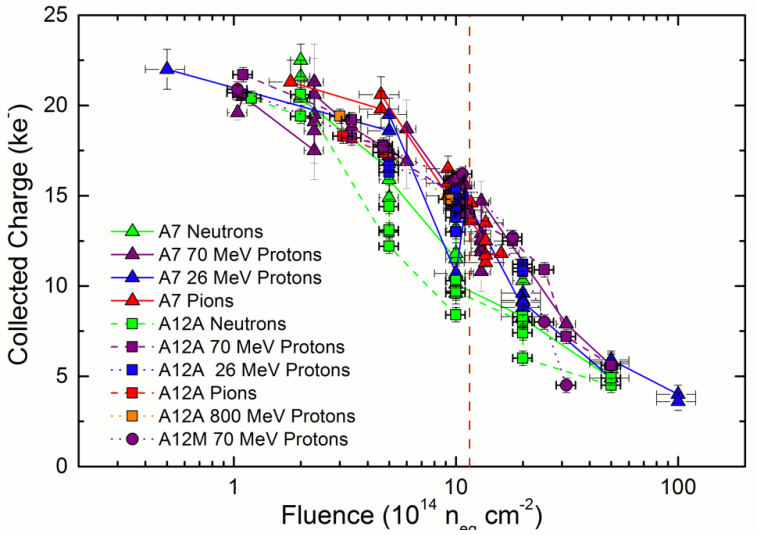


Figure 6.2: Collected signal charge at 500 V bias voltage for minimum ionising particles as a function of 1 MeV n_{eq}/cm^2 fluence for various types of particles [61]. The vertical dashed line indicates the maximal expected fluence within the ITk Strip Detector (incl. safety factor).

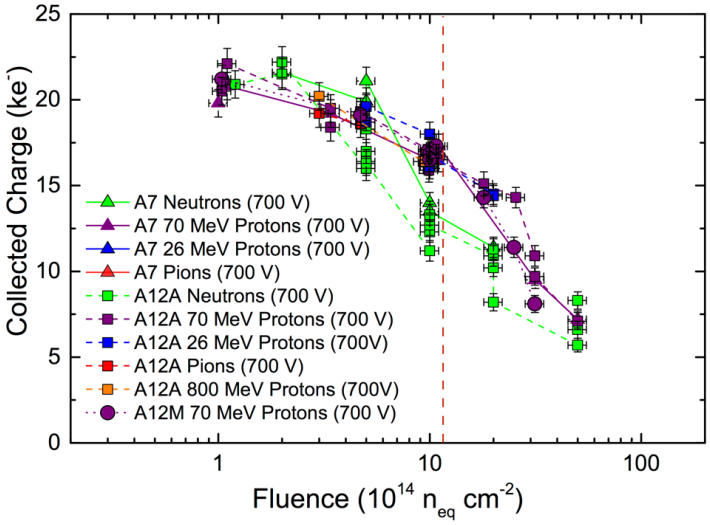


Figure 6.3: Collected signal charge at 700 V bias voltage for minimum ionising particles as a function of 1MeV n_{eq}/cm^2 fluence for various types of particles [61]. The vertical dashed line indicates the maximal expected fluence within the ITk Strip Detector (incl. safety factor).

6.1.3 Surface Properties after Irradiation

The changes in the surface properties of the baseline sensor technology (n^+-in-p FZ) have been studied after ionising and non-ionising irradiations. Non-ionising irradiation typically displaces silicon atoms which results in point and cluster defects in the bulk. Ionising irradiation results an accumulation of positive charges and traps in the SiO_2 and Si-SiO_2 interface which cause the majority of the changes in the surface properties of silicon sensors after irradiation. Sensor properties that could change are: the inter-strip resistance and capacitance, the coupling capacitance between the read-out strip's aluminium and implant, the strip's bias resistance and the punch-through protection (PTP) structure's performance, which protect against beam splash.

Miniature sensors were used to determine any changes with irradiation at multiple sites within the collaboration after irradiations by ^{60}Co gamma rays, 23 MeV and 70 MeV protons, and reactor neutrons. The inter-strip capacitance and coupling capacitance showed no measurable change over the full range of fluences expected for the strip system. The polysilicon bias resistance was shown to increase slightly with proton fluence and gamma dose (from 1.5 to 2.1 MΩ), but remains acceptable within the 2 MΩ specification up to the maximal expected fluence within the ITk Strip Detector (incl. the 1.5 safety factor). The PTP structures have been tested up to expected pixel fluences (1×10^{16} n_{eq}/cm^2) with the onset voltage of the protection increasing from 15 V to 30 V; as the coupling capacitors are specified to have a hold-off voltage of at least 100 V, these structures will work as designed for the lifetime of the ITk Strip Detector.

The inter-strip resistance showed the largest changes under irradiation as shown in Figure 6.4 and Figure 6.5. Neutron irradiated devices show smallest changes as expected as the majority of the damage is to the bulk sensor. The proton and gamma irradiations showed similar degradation; the inter-strip resistance reaches the specification at around 3×10^{15} n_{eq}/cm^2; it is 100 MΩ at the 2×10^{15} maximum strip fluence with the two times the safety factor, which is significantly above the 15 MΩ specification [62].

6.1.4 Lorentz Angle before and after Irradiation

Since the radiation damage in the silicon sensors changes the mobility of the charge carriers over time, the Lorentz angle will also change with increasing radiation damage. To study this effect, Lorentz angle measurements were performed on ATLAS12 test sensors before and after irradiation with neutrons at a range of fluences ($1.2, 2, 5, 10, 20$, and 50×10^{14} 1 MeV n_{eq}/cm^2 at Lublijana).

The measurements were carried out at the DESY-II test beam facility, using a 4.4 GeV electron beam for most measurements. Tracking was provided by the EUDET test beam telescope (see Chapter 8.3.1). Two ATLAS12 mini sensors at a time were placed between the two arms of the telescope. The minis were housed in a rotatable box and cooled to $-25°C$

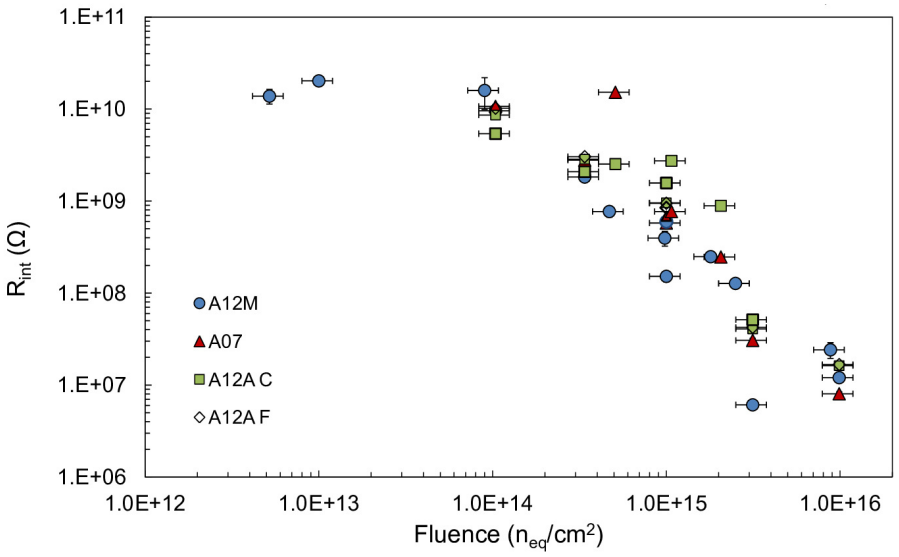


Figure 6.4: Inter-strip resistance vs. proton fluence for the prototype sensors ATLAS12A, 12 M and 07 barrel samples irradiated in the same irradiation campaign at CYRIC and measured by various laboratories at bias voltage of 400 V. The results are normalised to temperature of -20° C [62].

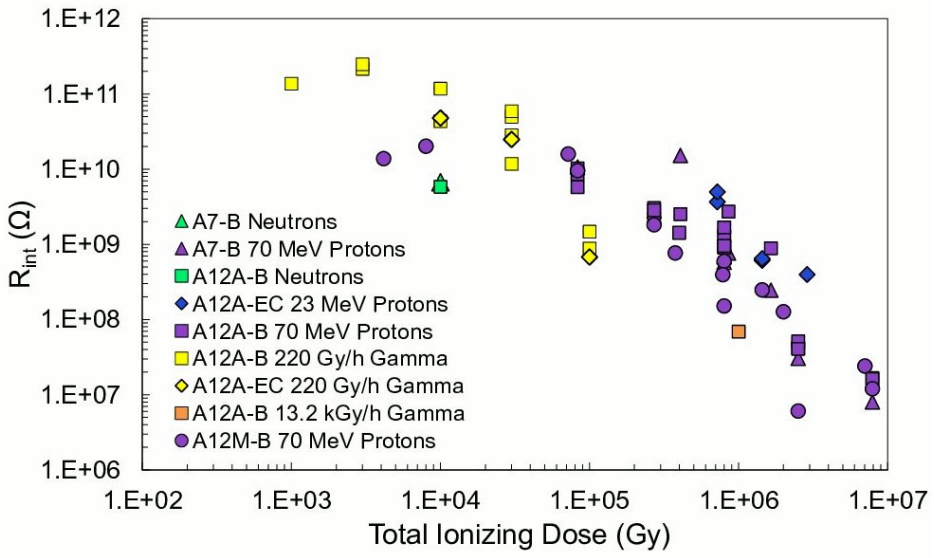


Figure 6.5: Inter-strip resistance vs. total ionising dose for the prototype sensor ATLAS12 irradiated by protons, neutrons and gammas at different irradiation sites. Results at bias voltage -400 V are presented. The results are normalised to temperature of -20 °C.

(with a precision of about 1°C). The solenoid provided a magnetic field of up to 1 T. The mini sensors were read out with an analogue ALiBaVa system. All measurements were carried out at a bias voltage of 500 V. At this bias voltage, only the non-irradiated test sensors and the test sensors irradiated at 1.2 and 2×10^{14} 1 MeV n_{eq}/cm^2 are fully depleted. At higher fluences, the measured Lorentz angle is affected by the fact that the sensors are not fully depleted (referred to as "effective Lorentz angle" in the following section).

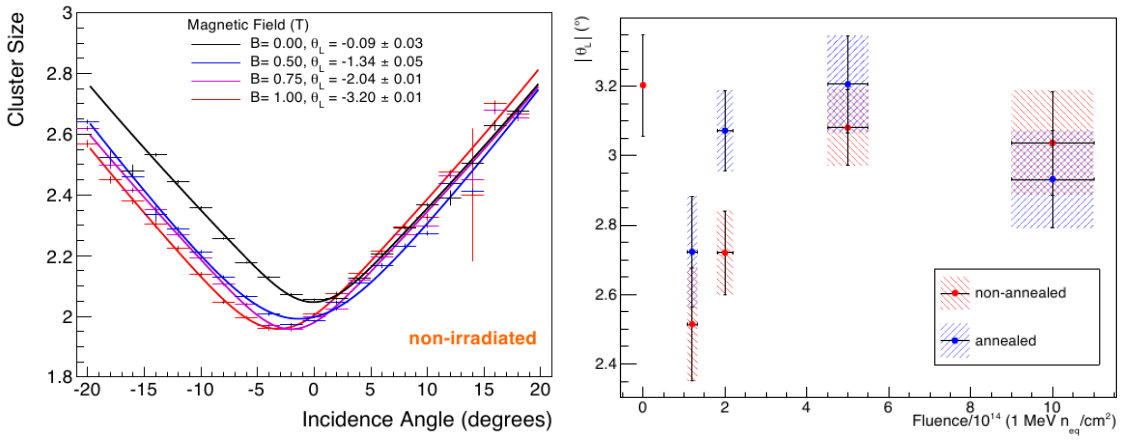


Figure 6.6: The cluster size vs. track incidence angle for several settings of the magnetic field strength measured for a non-irradiated ATLAS-12 test sensor (left) and the Lorentz angle at 1 T and a bias voltage of 500 V measured as a function of the fluence for ATLAS-12 test sensors irradiated with neutrons (right).

Figure 6.6 (left) shows the cluster size as a function of the incidence angle of the track for a non-irradiated test sensor. The measurements were performed at several values of the magnetic field strength for a robust extrapolation of the Lorentz angle measurement to a magnetic field strength of 2 T. The measurements were performed with low thresholds in the cluster reconstruction to allow for the measurement of the minimum of the cluster size vs. incidence angle distribution over a range of fluences. Figure 6.6 (right) shows the measured (effective) Lorentz angle for sensors operated at a bias voltage of 500 V in a magnetic field of 1 T up to a fluence of 10×10^{14} 1 MeV n_{eq}/cm^2 before and after annealing at 60°C for 80 min. The variation of the effective Lorentz angle over this range of fluences is 0.7° (extrapolated to 1.4° at 2 T), and the (effective) Lorentz angle is minimal in magnitude at 1.2×10^{14} 1 MeV n_{eq}/cm^2 (Ref. [66] reports a decrease up to 1×10^{15} 1 MeV n_{eq}/cm^2), and then increases again. At higher fluences, the collected charge was too small to allow for a reliable measurement of the effective Lorentz angle.

At the higher clustering threshold of 3000 e^- that will be used in the read-out of the silicon strip tracker, the effect of the Lorentz angle on the reconstructed cluster size will be smaller than indicated by Figure 6.6. At 5×10^{14} 1 MeV n_{eq}/cm^2 (10×10^{14} 1 MeV n_{eq}/cm^2), the cluster size is unchanged between track incidence angles of $\pm 5°$ ($\pm 10°$).

6.1.5 Tests of Non-irradiated Full Size Prototype Sensors

A sample of 100 of the 120 full-size (97.54 × 97.54 mm^2) ATLAS12A sensors produced at Hamamatsu have gone through the full quality control reception testing. The tests included the measurements of the shape of the sensor (bow), a visual inspection, measurements of global electrical parameters (leakage current, depletion voltage) and measurements of individual strip parameters (leakage current, bias resistance, coupling capacitance) through the use of a multi-channel probe card.

The devices were highly uniform with only one device outside of specification due to a section of ∼230 channels with a low coupling capacitance and a high bias resistance of up to 10 MΩ. The sensors are quite flat with an average bow of 51 μm corner-to-centre. Figure 6.7 shows the high quality of the full sensor leakage current, where all sensors pass the specification and most show no breakdown behaviour to the maximum tested voltage (1000 V). Only 132 faulty channels (excluding those from the faulty sensor) were found in over 0.5 million channels; the 99.97 % good strip fraction comfortably exceeds the 98 % requirement [63] (see Chapter 2).

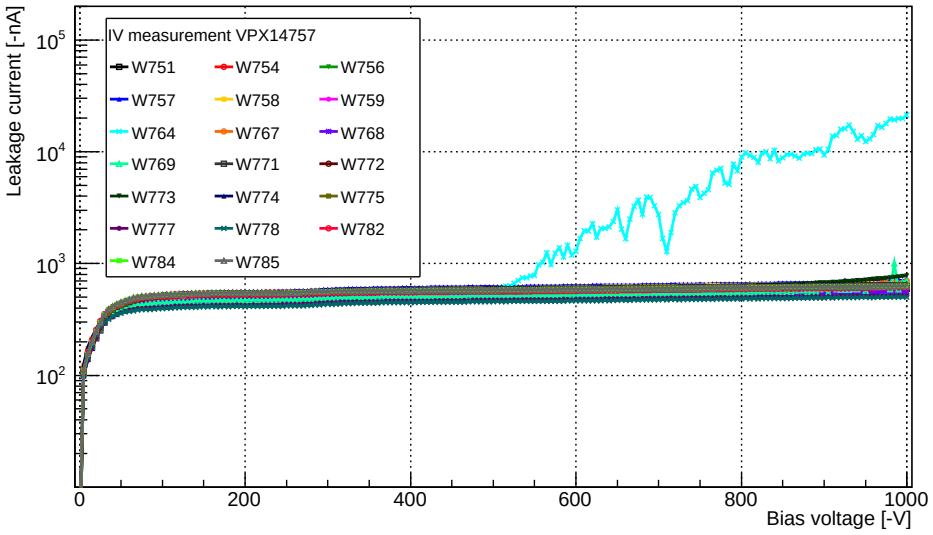


Figure 6.7: IV characteristics of large area ATLAS12 prototype sensors at 21 °C representatively for one batch [63].

6.1.6 End-Cap Specific Studies

Due to the complex geometry of the end-cap, six different sensor designs are needed to cover the petal surface. It was decided to implement the strips pointing to the beam axis

resulting in wedge shaped strips. Each face of a petal has nine sensors arranged in six rings named R0, R1, ... R5 from inner radius to outer. R0, R1, and R2 have one sensor per petal-face; the outer three have two identical sensors per face. The two faces are identical, so in total there are six sensor designs. The sensor sizes and shapes were optimised for 6-inch wafers. Different potential layout options which may be useful for the design of end-cap sensors have been explored.

The sensor layout is chosen to cover the petal with active strips, minimising the dead space such as guard regions and physical gaps between sensors. The stereo angle is built into the sensor – as opposed to making symmetric sensors, then rotating them by the stereo angle as implemented for the sensors on the barrel. Due to varying geometries of neighbouring sensors in the end-cap the physical rotation of sensors would be challenging to implement.

The chosen shape for all end-cap sensors is referred to as "Stereo Annulus": the inner and outer edges are concentric arcs of circles, centred at the centre of the disk, to cover part of an annulus. With circumferential edges[1)], all the strips are equal length and therefore the quality control is more simple. Additionally this is providing a more uniform capacitive load along the ASIC channels. The two sides are straight, but do not point to the centre of the wheel. Instead they are rotated away from the wheel centre by the stereo angle (ϕ_s = 20 mrad). Figure 6.8 shows how the sensor is designed to have the stereo angle built in. On the left side the principle geometry is explained. On the right hand side the sensor R0 for the innermost region of the end-caps is shown as an example for the end-cap sensors.

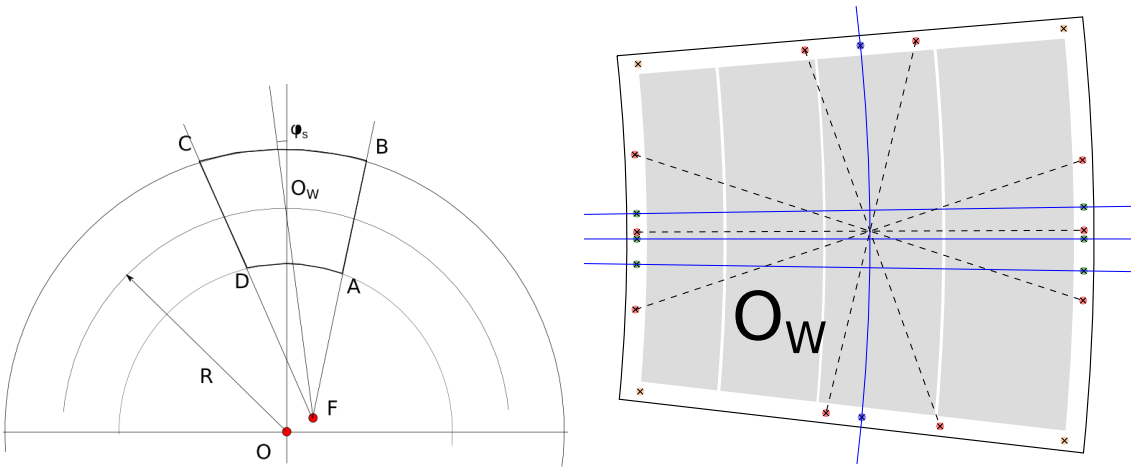


Figure 6.8: Left: Sketch showing how Stereo Annulus sensor geometry is made. The sensor is drawn connecting ABCD, the arcs CB and DA are centred at O which is the centre of the beam pipe. The strips are pointing to F which is slightly displaced from O due to the implemented stereo angle. Right: A drawing of the innermost sensor on a petal R0. Fiducials determine the centre of the sensor, the radius of the sensor in the global system and the corners of the sensitive area.

[1] The round edges are approximated during the wafer cutting process.

Further sensor layouts for the end-caps with implemented stereo angle and straight sensor edges were investigated. Straight edges are easier to produce and minimise the dead area between the sensors. Such a design could lead to strips at the edge of the sensor which do not directly connect to the read-out strip (orphan strips); if not corrected, this would result in inactive areas of the sensor for each row of channels. It was shown that this can be overcome by ganging the orphan strips to other strips that are connected to the read-out chips. With special ATLAS12A end-cap miniature sensors, two methods of ganging were explored: a metal strip which connects the implant of two strips (DC ganging) and a metal strip connecting the AC-coupling metal of two strips (AC ganging). It was shown that such a sensor can be designed and produced. Nevertheless, the skewed sensors were chosen as that layout does not require ganging of strips at all [64].

6.1.7 Market Surveys and Sensor Qualification

The strip sensor order is the single largest component cost for the ATLAS ITk Strip Detector. To survey possible vendors capable of producing large area strip sensors, a joint ATLAS and CMS Market Survey was organised, MS-4086. It started in May 2016. The survey has three distinct phases:

1. Survey of the vendors and compiling information on their technical capabilities.
2. Obtaining large enough samples from the vendors' prior fabrication rounds.
3. Test fabrication submission of sensors to particular ATLAS or CMS specifications to selected vendors and device evaluation.

The first step is common to both experiments, but the second and third step have different specifications and timelines. At the time of writing, the first two steps are completed for the ATLAS part of the survey. A total of six vendors expressed an interest in supplying strip sensors for ATLAS ITk strips. Based on their responses to the technical questionnaire of the survey, some companies were rejected at the first step of the survey. The key considerations in this decision were technical capability matching the strip sensor features, compliance with fabrication process rules, and feasibility of large sensor volume production. The companies that passed to the third survey step are Hamamatsu Photonics (HPK) and Infineon Technologies. ATLAS is in the process of designing the test sensors for the last step of the survey for these companies.

6.2 The ASIC Set for the ITk Strip Detector

A number of custom-made ASICs are being developed for the ITk strip system. In the following sections the design details and available test results including radiation damage studies are presented. In Table 6.3 the main functionalities of the ASICs are summarised.

The test results in the following chapters are mostly based on the prototype chips while the production chips are being specified and designed at the time of writing.

Table 6.3: Overview of the custom made ASICs for the ITk Strip Detector.

Acronym	Full Name	Basic functionality	Prototype	Production Chip
ABC	ATLAS Binary Chip	Converts incoming charge signal into hit information	ABC130	ABCStar
HCC	Hybrid Controller Chip	Interface between ABC130 and bus-tape	HCC130	HCCStar
AMAC	Autonomous Monitor and Control Chip	Provides monitoring and interrupt functionality	AMAC-I	AMAC-II
FEAST	FEAST	Synchronous Step-Down Buck DC/DC converter	FEAST	upFEAST

6.2.1 The ATLAS Binary Prototype Chip ABC130

A chip set has been designed in IBM 130 nm CMOS8RF technology: the ABC130 front-end [67] and the HCC130 (see Section 6.2.4). Both chips are currently under evaluation. The chip set is based on a daisy-chain read-out architecture, where data are serially transmitted through a group of front-end chips and then through the HCC130. These ASICs include capabilities aligned to the ATLAS upgrade trigger requirements. The specifications for the final ABCStar as required for the star architecture (see Chapter 5) will be described in Section 6.2.2.

The prototype analogue binary chip (ABC130) used for most of the studies presented in this TDR provides all functions required for processing the signals from 256 strips of a silicon strip detector employing the binary read-out architecture. The simplified block diagram of the configuration of the chip is shown in Figure 6.9. The main functional blocks are: front-end, input register, pipeline, derandomising buffer, data compression logic blocks, command decoder, read-out logic, threshold & calibration control, and power regulation.

The architecture chosen for the ABC130 allows a multi-trigger data flow control retaining the beam crossing synchronous pipeline transfer signal (L0), an asynchronous regional read-out request (R3) and a second level asynchronous data read-out intended for a global read-out (L1 here). The ABC130 contains 256 analogue preamplifier-shapers followed by discriminators with individual threshold trimming capabilities. The shaping time should allow 0.75 fC pulse detection separated by 75 ns. The binary outputs of the discriminators (data) are sampled at the bunch crossing clocking rate (BC) and stored for 6.4 μs in the "pipeline" or L0_Buffer memory bank. At the reception of a L0 signal, the data in the memory that were stored at some fixed latency time before the L0 signal are extracted from the pipeline and transferred to the de-randomising buffer (R3L1_Buffer) and stored. The data corresponding to three consecutive time slots are transferred for each L0 and form an event. There is enough room in the R3L1_Buffer for 86 events. After 86 events are stored,

new events overwrite the R3L1_Buffer content. At reception of a "R3" signal (R3s_L1 output from the HCC130, see below), which carries a L0 identifier, the event that has the same L0 number is extracted from the R3L1_Buffer and processed through the R3 Data Compression Logic block that performs zero suppression and cluster identification. The same happens at the reception of a "L1" signal (R3s_L1 output from the HCC), but the event with the correct L0 number is processed through the L1 data compression logic block.

The R3 and L1 data compression logic (DCL) differ in their algorithms to detect clusters and perform cluster identification; however, both algorithms will apply the same hit criteria as the present ATLAS-SCT chip, the ABCD. That is, a hit channel can be defined by the time sequence X1X, 01X, or XXX where 0 is no-hit, 1 is hit and X is "don't care" and the three bits are set for three consecutive beam crossings centred on the trigger BC. The criterion to use is set by the configuration register. The information extracted from the two DCLs is different; for example the R3 unit is limited to identify four clusters at maximum due to bandwidth limitations and produces one data packet. This limitation is not present in the star architecture. The L1 unit is not limited in the number of clusters and number of packets produced. The information extracted from the DCL contains a channel number to identify each cluster and bits that represent the cluster shape. The data are stored in local FIFOs to be transferred at the proper time to the read-out block.

The read-out block contains a packet builder and a fast serialiser. The packet builder gets the data from either:

- The adjacent chip (external)
- The R3_DCL (internal)
- The L1_DCL (internal)
- The internal registers (internal)

The priority of data transfer is set according to this order, i.e. for a given ABC130, it will first send any data from the adjacent chip, then from the R3_DCL, then from the L1_DCL, and then from a register read. The data from an adjacent chip is already formatted and is simply transferred to the serialiser.

The front-end is built with a trans-impedance amplifier with active feedback followed by additional shaper circuits and a differential discriminator. The shaping time is 20 ns with a quasi-Gaussian shape. The signal gain is simulated to 85 mV/fC, and the noise should be less than 700 e^- for a capacitance of 6.4 pF (simulated with p-on-n "positive" signal from the detector). A calibration signal distributed with one calibration line can be applied to a calibration capacitor (60 fF) connected to each front-end input with a CMOS switch, controlled with a configuration-bit per channel. The addresses of the channels connected to the calibration line, as well as the amplitude of the calibration signal and its phase versus the Bunch Crossing clock are set via the control-logic and programmable registers. The voltage applied to the calibration capacitors is determined by an internal 8-bit DAC with a range of

0 to 9 fC and a resolution of 0.035 fC. The discriminator threshold is adjusted per channel to compensate for the global threshold dispersion along the 256 channels, decreasing the dispersion from 15 mV down to below 2 mV (0.023 fC). The global threshold is set through an internal 8-bit DAC with a range of 0 to 6.5 fC and a resolution of 0.025 fC.

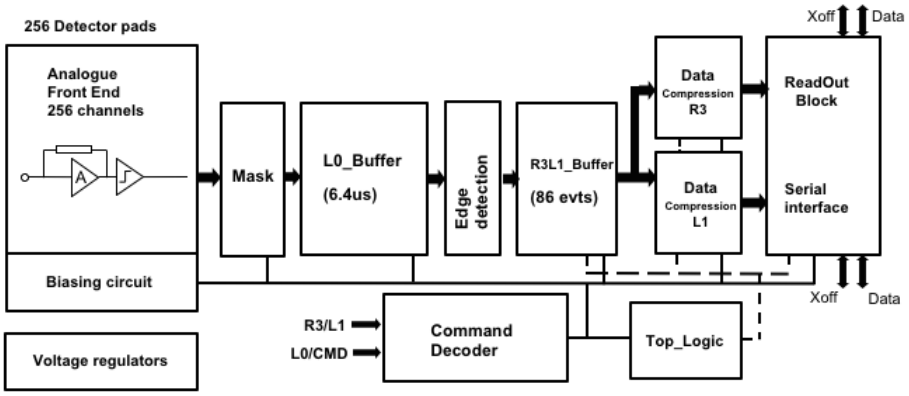


Figure 6.9: Block diagram of the ABC130 read-out part with the R3 capability. All the ABC130 chips receive L0A and extract the corresponding data from the pipeline (L0_Buffer). These data are stored together with a L0ID in the R3L1_Buffer. Only those in the region of interest receive R3 signal and send immediately the corresponding data. L1A comes later together with the L0ID to which it refers. This L0ID is used to select data in the R3L1_Buffer and send them. The TTC system requires 160 Mbit/s for the R3 Scheme as some additional information is to be sent together with L0A and L1A.

6.2.2 ABCStar Specifications

The ABCStar ASIC provides all functions required for processing of signals from 256 strips of a silicon strip detector in the ATLAS experiment employing a binary read-out. The architecture chosen for the ABCStar allows a multi-trigger data flow control retaining the beam crossing synchronous pipeline transfer (called L0 here) from previous versions, a first asynchronous read-out request (called PR trigger) with priority and low latency (this signal is distributed to a fraction of the detector to get the tracking data participating to the L1 trigger) and a second asynchronous read-out request (called LP trigger) intended for a global read-out. The design can be easily adapted to a single level read-out (L0 read-out mode) simply by not using the PR trigger and associating each L0 to a LP trigger. The simplified block diagram of the chip is shown in Figure 6.10. Additionally it contains improvements to mitigate the effects of total ionisation dose as well as an optimisation of the front-end stage.

The main functional blocks are: front-end including threshold and calibration controls, power regulation, command decoder, mask and edge detection, L0Buffer, EvtBuffer, cluster finder and read-out logic. The "Top_Logic" block controls the data path by interpreting the PR and LP trigger signals. The front-end is optimised for 2.5 cm strips with 25 ns shaping

time, and a noise level below 1000 electrons after full radiation effects. Resistive feedback and enclosed layout transistors are used to improve noise performance before and after irradiation. The discriminator level in operation should be lower than 1 fC, possibly reaching 0.5 fC. After discrimination, at each bunch crossing the binary outputs of the front-end channels are sampled and stored into the L0Buffer for a duration fixed by the (programmable) latency for receiving the L0 signal.

At each L0 reception the event with the correct latency is transferred to the EvtBuffer. It is maintained for an average duration corresponding to 128 L0 (128 μs at 1 MHz L0 rate) and tagged with an appropriate identification number (L0ID). If a PR or LP signal is received with the corresponding L0ID number, the event is processed through the cluster finder (CF). The CF block acts as a data reduction circuit, creating a "cluster" byte for channels found with hits. The expected average occupancy is of 2 [4 in case of 5 cm strips] clusters per event. The read-out block creates formatted packets with the event identification and the associated cluster bytes. The data are transmitted serially at 160Mb/s.

The command decoder block receives and distributes internally the trigger signals (L0, PR, LP). Through the same input the chip receives the configuration commands (including resets), the analogue bias settings, the mask and test and calibration settings, the register read-back instructions. The Top Logic block is the autonomous sequencer that controls the data flow path according to the arrival of the L0, PR, LP trigger signals.

At the time of the TDR this chip is being designed and will be submitted in the second quarter of 2017. The overall timeline of the project including the chip submission will be discussed in Chapter 24.

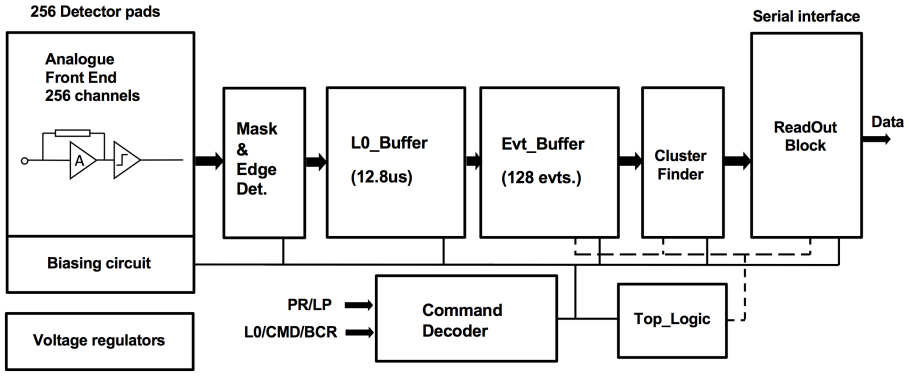


Figure 6.10: Block diagram of the ABCStar chip.

It will be fabricated at Global Foundries (using a former IBM foundry) in a 130 nm CMOS technology. The wafers are standard 8-inch wafers and will be thinned to 200-320 μm. The chip will be 7.9 mm wide to best fit the input pads to the sensor strip pitch, while keeping a reasonable gap between adjacent chips to allow the placement of decoupling capacitors. The maximum length is set to 6.8 mm.

6.2.3 ABC130 Characterisation: Results before and after Irradiation

Threshold Scan

The basis for the characterisation of the ABC130 is the threshold scan. This test allows the measurement of important figures of merit to evaluate the chip performance, such as input and output noise, and gain. The threshold scan is performed by injecting a constant charge and varying the threshold value of the discriminator from zero to its maximum. At each threshold level several charge injections are performed. Plotting the measured average hit rate versus threshold gives a plot known as an S-curve. The value with a 50% hit rate corresponds to the median of the injected charge and it is called "Vt50".

The S-curve is the integral of a Landau convoluted Gauss function. This curve is fitted with a skewed error function which determines the output noise in mV. Figure 6.11 depicts an example S-curve for a single ABC130 at 1.51 fC charge injection.

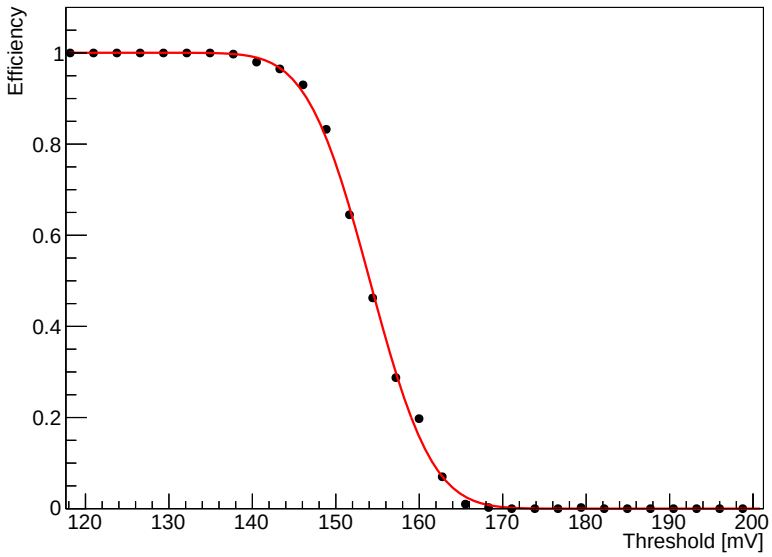


Figure 6.11: Average hit rate versus threshold for a ABC130 (S-curve) at 1.51 fC injected charge. The value with a 50% hit rate corresponds to the median of the injected charge and defines the threshold.

Gain and Noise

By measuring the Vt50 and sigma of the distribution for different input charges, the gain and input noise can be calculated and a safety factor of 20% added. The effect of this current increase is discussed in Chapter 17. The test consists of multiple threshold scans with

different charges. For each injected charge the Vt50 point is measured and plotted as a function of the charge. This curve is known as a response curve. By fitting the response curve the gain of the input stage is obtained. It is measured in [mV/fC]. Once the values of gain and sigma are known the Equivalent Noise Charge (e^- ENC) can be obtained. The ENC is the charge at the input that would create the same output level as obtained from the noise. It can be calculated as

$$\text{ENC} = \frac{\sigma[\text{mV}]}{\text{gain}[\text{mV/fC}]} \tag{6.1}$$

The ENC is in the following expressed in electrons [e^-] assuming 1 fC=6241 e^-. Typical noise values for a bare ABC130 chip are between 400 and 900 e^- depending on the capacitive load at the input. The same method is also used for the measurements of irradiated chips (see Section 6.2.3) and full modules (see Chapter 8).

Measurements of noise on an ABC130 single chip with capacitive load at the input are in agreement with results obtained on the front end prototype with negative input signals as shown in Figure 6.12. The noise results of module prototypes with the ABC130 connected to sensors is discussed in Chapter 8.

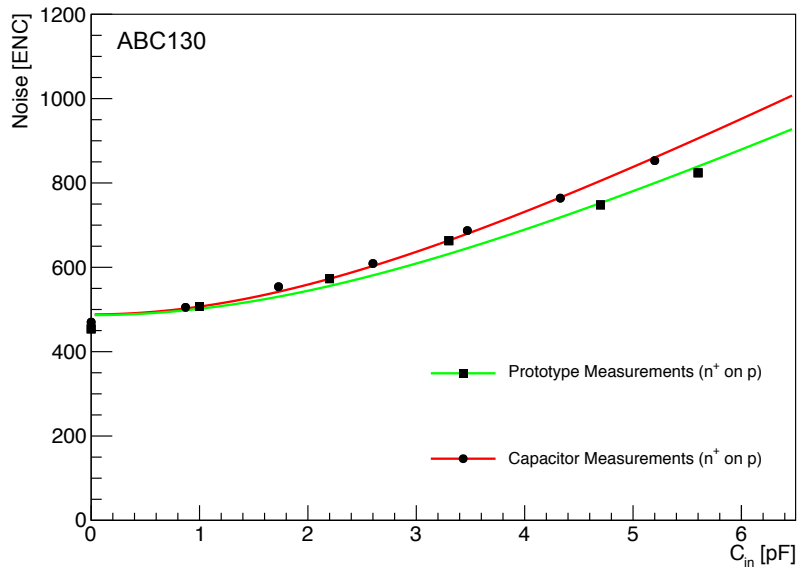


Figure 6.12: Noise measurement as a function of input capacitance for the ABC130 chip and the front-end prototype.

Current Increase induced by Total Ionising Dose

An irradiation campaign with X-rays at rates between 0.6 kRad and 2.25 MRad and at temperatures between -30 °C and +20 °C have shown a digital current increase, peaking around

1-2 MRad. As shown in Figure 6.13, the increase depends on the dose rate and temperature during irradiation. This effect is well understood and typical of the used 130 nm technology nodes [68, 69]. The increase of the low voltage current consumption of the front-end chip is tracked back to the generation of a leakage current in NMOS transistors induced by radiation. The radiation induces positive charge that are quickly trapped in the shallow-trench-on-insulator (STI) oxide at the edge of the transistor. Their accumulation builds up an electric field sufficient to open a channel source-drain where the leakage current flows through. While the build-up of positive charge is relatively fast, the formation of interface states is a slower process. The negative charge trapped in interface states start to compete with the oxide-trapped charge with a delay. This is the origin of the so called rebound effect. This effect was also observed in the ATLAS IBL detector, for which operating conditions to effectively mitigate the impact were applied successfully [70].

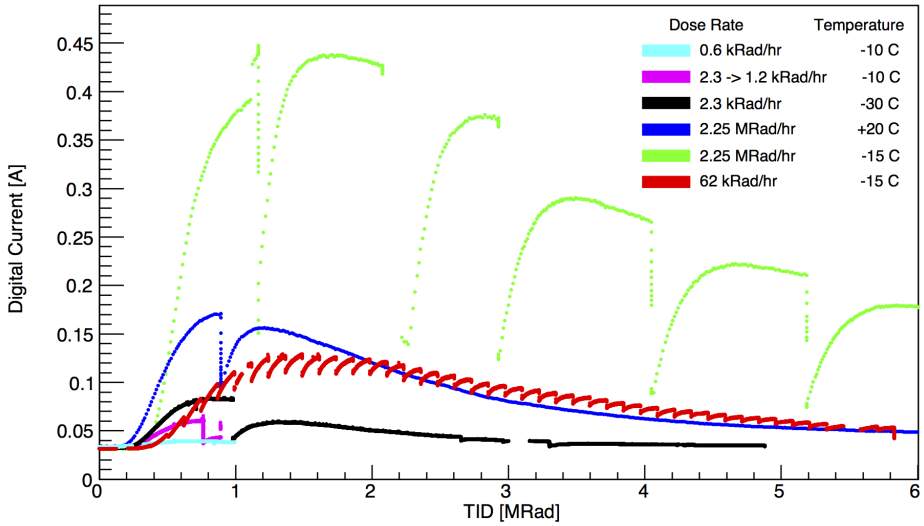


Figure 6.13: Digital current vs. TID for ABC130 chips during X-rays irradiations at different dose rates and temperatures.

No increase of the analogue current of the ABC130 chip is observed due to the large size of the transistors and the current bias controls.

A detailed low dose rate irradiation campaign was conducted at the ^{60}Co source at CERN to mimic the dose rates in the different parts of the detector during operation. A first campaign at -25 °C and 2 kRad/h (highest HL-LHC dose rate for ITk strips) gives a factor 2.5 increase in digital current. More irradiations followed at lower dose rates and different temperature, using updated results of both fluence and TID in the detector. Table 6.4 summarises the results of this campaign. Irradiations have also been performed with protons and results are shown in Figure 6.14.

The results give a current increase factor between 1.3 (T=-10 °C, low dose rate) and 2.5 (T=-25 °C, high dose rate) at the peak. The local dose rate and temperature will depend on

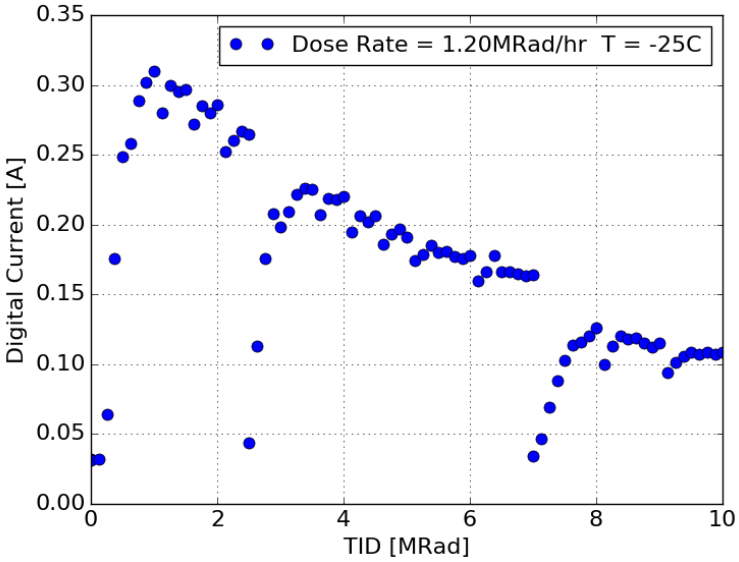


Figure 6.14: ABC130 digital current vs.TID for protons.

each component's location in the strips detector and the operating conditions. In Figure 6.15 the data points and a fit to the data is shown. Based on the fit functions the maximal current increase for each position in the Strip Detector can be calculated.

Table 6.4: Summary of the TID current increase factors for ABC130s using various irradiation facilities.

Source	**T (°C)**	**Current Increase**	**Dose Rate (MRad/h)**
^{60}Co CERN	−25	2.5	0.0023
^{60}Co CERN	−10	1.9	0.0023
^{60}Co CERN	−10	1.3	0.0006
Birmingham-p	−25	9.7	1.25
X-ray CERN	−15	3.9	0.062
(extrapolated)	−10	3.5	0.062
X-ray CERN	−15	13.6	2.25
X-ray CERN	+20	5.2	2.25

Noise versus TID

A noise increase is also observed after ionising radiation. As shown in Figure 6.16 the noise increases with TID to reach a plateau after 15-20 MRad. No recovery towards the pre-rad

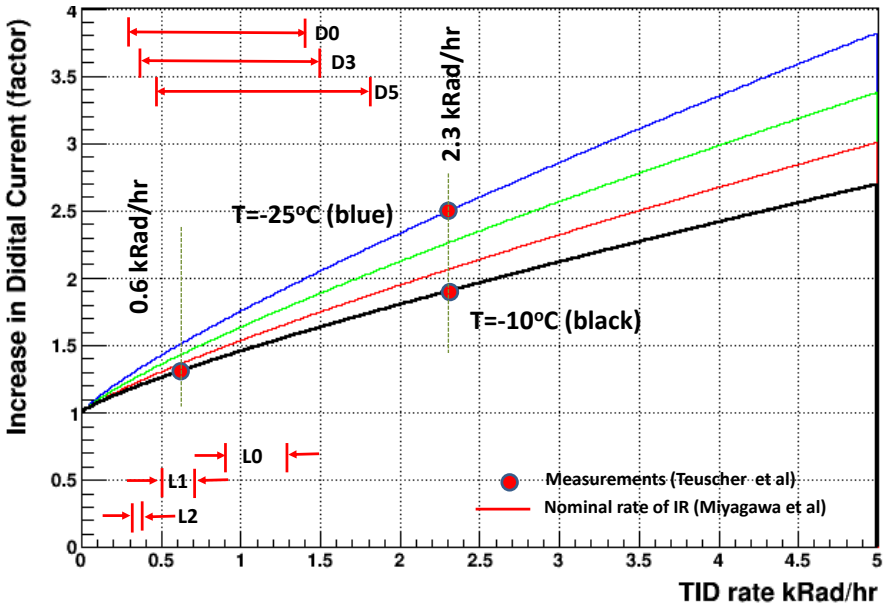


Figure 6.15: Current increase factor measured in ABC130s as a function of the dose rate for different temperatures.

value is observed. The most likely reason is 1/f noise. The simulated pre-rad contribution of the 1/f noise to ENC is at the level of 3%. Some reports for 130 nm technologies [71–73] show a substantial increase of the 1/f noise for regular NMOS devices and no change for the enclosed structures. For the ABCStar all critical (for noise) NMOS devices will be in an enclosed geometry.

Gain degradation with TID

The gain degradation with TID shows a peak followed by a rebound, similar to that observed for the current (see Figure 6.17). Depending on dose rate and temperature during irradiation, the gain can decrease by about ∼10 %, before recovering towards the pre-rad value. For realistic operating conditions the decrease is only around 2 %.

Single Event Effect Tests of the ABC130

Single Event Effect (SEE) tests of the ABC130 have been performed at CHARM with 24 GeV protons. Beam spills occurred every O(5s), delivered nearly 3×10^9 protons/cm^2 per spill and lasted for 300 ms. Over the course of one week a total dose of 6 MRad was reached. The test included two independent read-out systems. One of the read-out systems included an ABC130 located at the centre of the beam spill. The other read-out system included three

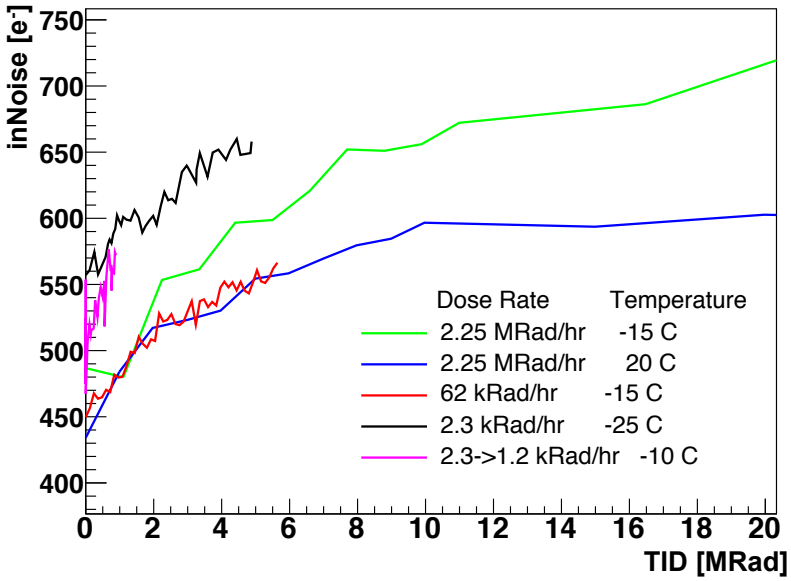


Figure 6.16: Increase of input noise in the ABC130 as a function of TID, for different dose rates and temperatures.

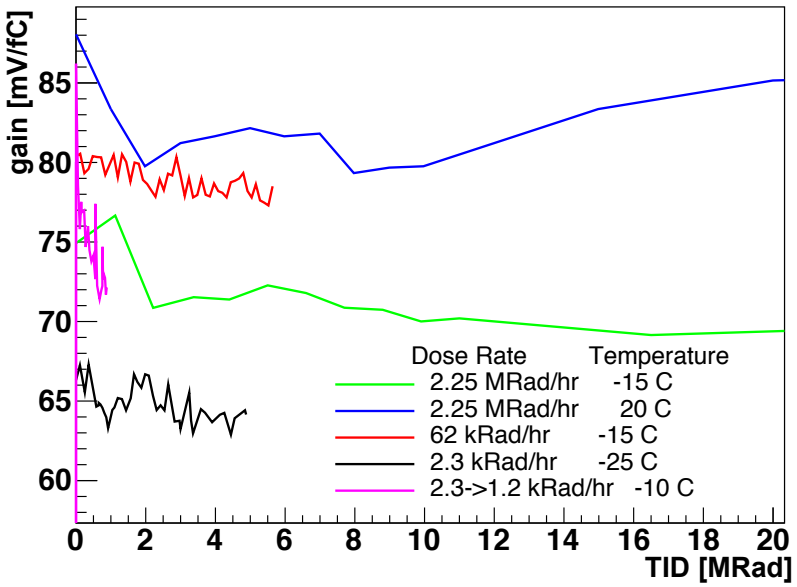


Figure 6.17: Gain change in the ABC130 as a function of TID, for different dose rates and temperatures.

neighbouring ABC130 chips on a hybrid read out by an HCC130 with the beam spot centred on the middle of the three ABC130s. The beam spot had a full width at half maximum of approximately 10 cm in the direction along the length of the hybrid and approximately 5 cm in the perpendicular direction.

To perform tests the chip was prepared in a configured state with known register values and known hit patterns loaded into the event buffer before the spill. During each spill no commands were sent to the chip. After each spill the chip registers and event buffer were read out then reset. The values read from the registers and event buffer were compared with the expected values and analysed for Single Event Upsets (SEUs) and functional interruptions.

Three types of Single Event Upsets (SEUs) were analysed. SEUs in the event buffer caused by a single bit flip were measured by a direct comparison to the expected hit pattern in the event buffer and the bit flip cross section was calculated. Flags set internally by the chip and stored on a read only register when one of the physical triplicated registers contains a different value than its two counterparts were also counted. Given the number of flags, the number of bits which each flag is monitoring and the assumption of independent bit flips a physical bit flip cross section was calculated in the registers. Logical bit flips in the triplicated registers were also counted and an effective logical bit flip cross section was calculated.

The calculations from the event buffer show bit flip cross sections around $1 \times 10^{-13}\text{cm}^2$ and are consistent across all chips (Figure 6.18 top). The cross section measurements based on internal flags are $\leq 9 \times 10^{-14}\text{cm}^2$ per bit (Figure 6.18 middle). The cross section for logical bit flips in the triplicated logic is measured to be around $2 \times 10^{-15}\text{cm}^2$ per logical bit for most registers, with a few exceptional registers showing cross sections up to $16 \times 10^{-15}\text{cm}^2$ (Figure 6.18 bottom). The increase in logical bit flips at higher register addresses is being investigated and will be addressed in the ABCStar.

Based on comparisons to similar measurements made of SEU cross sections in the ABCD3TA chip [74, 75], which is used in the current ATLAS SCT and the operational experience with the current ATLAS SCT during LHC Run-1 and Run-2 it is expected that the measured SEU cross sections will be acceptable for ITk operation. Misconfigurations of the chips are expected to be kept well under control with occasional reconfigurations as is done in the SCT. The rate of noise in the form of extra or missing hits introduced in the data pipeline due to SEUs has been calculated as one bit flip per 7.6 million data packets transmitted. The rate of misidentifying the event to which a data packet corresponds due to SEUs has been calculated as approximately one misidentification per 10^9 packets transmitted.

Analysis of functional interrupts where packets expected from the chip were never received, or where duplicates of packets were found, was also performed. Based on the rate of missing or duplicate packets in the CHARM tests from the ABC130 it is calculated that each ABC130 will send back a corrupted event no more than once for every 2×10^9 readout requests. Here a corrupted event is an event with at least one missing or duplicated

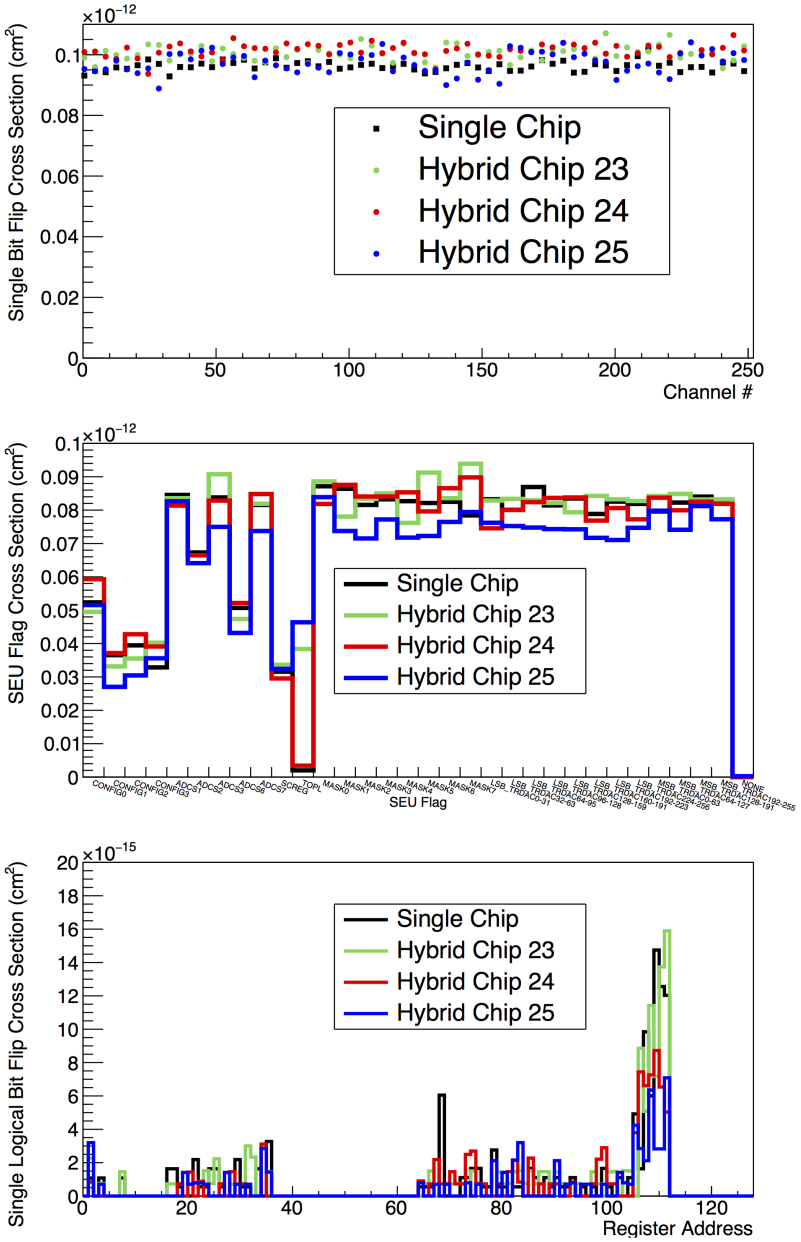


Figure 6.18: Single Event Upset cross sections for the ABC130 with 24 GeV protons measured for **Top**: data stored in the event buffer **Middle**: single physical bit flips in configuration registers as indicated by internal SEU flags stored on the chip. **Bottom**: logical bit flips in triplicated registers. These values assume that bit flips are uncorrelated and logical bit flips in triplicated registers are independent of the rate of particle flux.

packet. The rate of packets in an unexpected or unknown format being returned is found to be much smaller than the rate of duplicate or missing packets.

The ABCStar is expected to be more robust against single event effects as compared with the ABC130 due to improvements in the state machines and the triplication register auto correction. There was no evidence of a higher SEU cross section with TID.

Performance of the Modified Front-End Stage

The prototype front-end stage designed for the ABCStar ASIC was submitted in a multi-project wafer run. In the new front-end stage the resistive feedback was modified and a differential booster amplifier added. This was implemented to improve noise performance when operated with n^+-in-p sensors. Additionally enclosed transistors were implemented to remove the noise increase due to radiation damages as observed in the ABC130. The prototype consists of 32 channels of the preamplifier-shaper-discriminator chain with an input/output multiplexer for calibration injection and data readout. One channel is implemented with analogue outputs. During tests seven channels were connected to input pads for capacitor loading.

In Figure 6.19 the noise versus the input capacitance is shown for the previous prototype chips and the new prototype for the ABCStar. These measurements are in agreement with simulations and give confidence that the performance of the ABCStar will be improved compared to the ABC130.

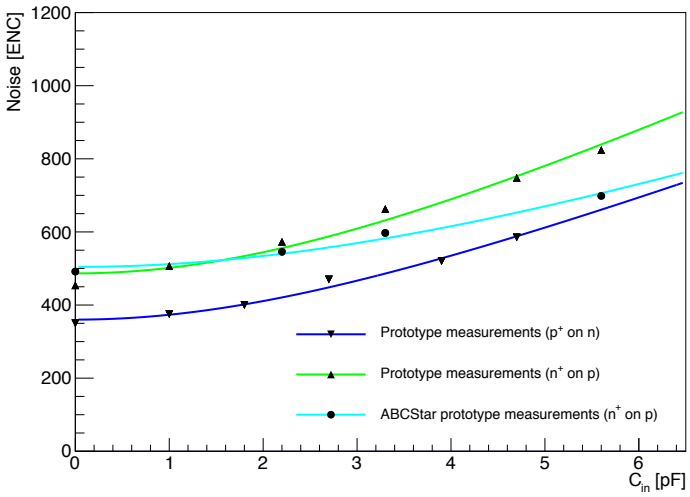


Figure 6.19: Noise measurement as a function of input capacitance for the front-end for the ABCStar chip and the front-end prototype.

Figure 6.20 shows the noise as a function of TID for the modified front-end stage. One of the channels is connected to a 4.7 pF capacitor to mimic operation with long strips. The irradiation was performed with x-rays at a dose rate of 0.87 Mrad/h at room temperature. The

noise increase is significantly lower than in the ABC130 prototype front-end, confirming that the use of ELTs improves the noise performance with TID.

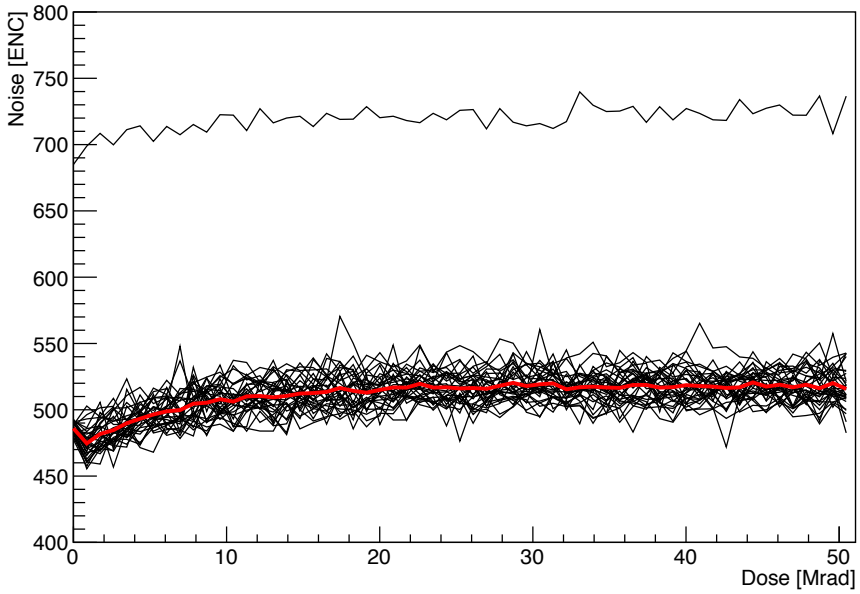


Figure 6.20: Noise measurement as a function of TID for the front-end for the ABCStar chip.

6.2.4 The Hybrid Controller Prototype Chip HCC130

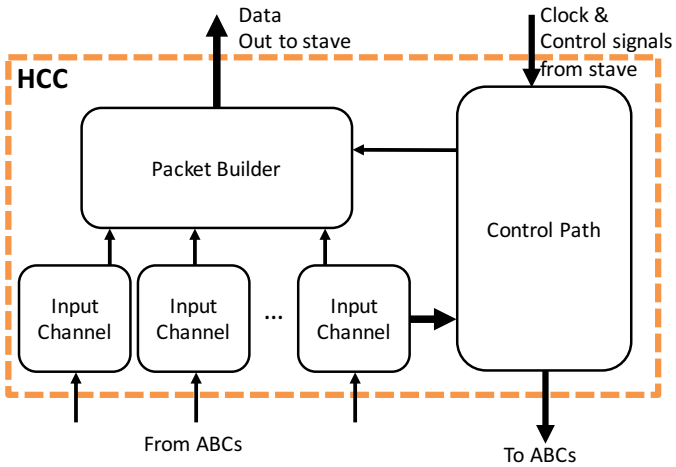


Figure 6.21: Block diagram of the HCCStar chip.

The Hybrid Controller Chip (HCC) is the interface ASIC between the signalling on the stave and the analogue front-end ASICs (the ABCs) on the hybrid. There is one HCC per hybrid. The chip has stave-side inputs for the bunch crossing clock and control signals. These

control signals include triggering and general commands. After processing in the HCC, the control signals are sent on a hybrid-side bus to the ABC130. Any data being returned from the ABC130 are sent through the HCC, where they are queued and sent out on the data line on the stave.

The prototype version of the HCC is the HCC130. The data connections from the ABCs are in the form of two bidirectional loops. In the barrel, each loop has five ABC130s. In the end-cap, the loops vary between seven and eleven ABC130s. The data handling in the HCC130 is very minimal: it adds a header to ABC130 data packets and sends them on to the End-of-Substructure Card (EoS).

The HCC130 has been fabricated in the Global Foundries 130 nm CMOS process. It has three LVDS inputs for its control lines: a 40 MHz clock, a 80 Mbit/s line shared by the L0 trigger and Commands, and a 80 Mbit/s line shared by the R3 and L1 triggers. The two 80 Mbit/s lines are configured so that one signal (CMD and L1) is sent with the high phase of the 40 MHz clock and the other signal (L0 and R3) are sent with the low phase of the clock. A detailed block diagramme is shown in Figure 6.21.

The 40 MHz clock is used as the reference for a phase locked loop (PLL) that generates several 160 and 320 MHz clocks that are used throughout the HCC130. The PLL also makes available a stabilised 40 MHz clock. One of the 160 MHz clocks is used to generate an 80 MHz clock, with deterministic phase with respect to the 40 MHz reference clock. Either the original 40 MHz clock or the PLL 40 MHz is distributed to the ABC130 chips on the hybrid side. The PLL contains several programmable internal parameters to optimise its performance under varying conditions. These parameters are a resistance, a capacitance and a current.

On entering the HCC130, the L0 and Command signals are de-multiplexed. The L0 signal is passed through the HCC130 with minimal fixed delay and is re-multiplexed with any Command stream being sent to the ABC130. Commands to the front-end are either global, with no addressing, or specific to a given ABC130 or HCC130. The specific commands have the hardware address of the HCC130 on the addressed hybrid. The HCC130 will filter out any ABC130 command that does not not have its hardware address. All global commands, and those ABC130 commands that are for ABC130s on this hybrid are re-multiplexed with the L0 signal and sent out on the hybrid bus.

The multiplexed R3-L1 line is treated similarly to the L0-CMD line. The L1 signals are passed through, while the R3 signals are processed. The R3 signal contains a 14-bit, unary encoded value, to indicate which modules are to respond to the R3 request. The HCC130 uses its hardware address to determine whether its module should respond to the R3. If it determines that it should respond, a shortened form of the R3, called R3s, is generated. The R3s and L1 signals are re-multiplexed and sent out on the hybrid bus. The HCC130 sends a clock on the hybrid bus that is used by the ABC130s to send data back to the HCC130. This clock can be selected to be either 80 or 160 MHz.

There are four inputs from the ABC130s to the HCC130. Two of these are the endpoints of one loop and the other two are the endpoints of the second loop. Depending on the configuration of the ABC130s in the read-out loops, data will arrive on any number of the four inputs. There are flow control signals from the HCC130 to the end ABC130s that indicate whether data can be sent to the HCC130.

Data from the ABC130 inputs have an HCC130 header added to them and are combined with a data flow from HCC130 register reads and the HCC high priority packet flow in a priority-based system. The HCC can output packets at 80, 160, or 320 Mbit/s. In one case, the data are taken from a single ABC130 loop, plus the HCC130 data and sent out. This supports output rates of 80 and 160 Mbit/s. In the other case, the data from the two loops are multiplexed bit by bit on the output. This mode supports output rates of 160 and 320 Mbit/s. In both cases, the lower output rate corresponds to an ABC130 to HCC130 data rate of 80 Mbit/s and the high rate corresponds to an ABC130 to HCC130 data rate of 160 Mbit/s. All of the hybrid side signals, both inputs and outputs, can be delayed over a range greater than one clock cycle with fine step size.

The HCC130 also contains blocks for monitoring the PLL and for making autonomous analogue measurements of various quantities including raw and regulated voltages, on- and off- chip temperatures, and high voltage current. This monitor also has the capability to individually interlock four separate output signals. This block is called the Autonomous Monitor (AM) and is the base for the development of the AMAC chip described in Section 6.2.8.

6.2.5 HCCStar Specifications

The HCCStar will be fabricated in the Global Foundries 130 nm process. A number of the analogue blocks with be reused from the HCC130, in particular the PLL and delay blocks. The drivers and receivers will be modified versions of ones in the HCC130. The HCCStar is divided into three major sections: the control path, the input channel and the packet builder/serialiser.

The control path takes the clock and control signals from the stave, decodes them, performs processing on them as needed and sends them on the hybrid bus to the ABCStar read-out chips. Many of the details are not yet known, including incoming data rates, data encoding, protocol etc. It is likely that the clock will be 40 MHz. There probably will be two control lines, at least one of which will run at 160 Mbit/s with the other running at a rate of at least 80 Mbit/s. An encoding such as 6b/8b is under discussion.

The L0 trigger decisions for some number of bunch crossings – likely four or five – will be collected and sent together, along with a tag composed of the low order bits of the L0ID. This tag will be interpreted as the L0ID of the first L0 trigger accept. Subsequent L0 accepts will have L0IDs incremented from the first. The input channel will decode the L0 trigger information for its own bookkeeping and will forward the command stream, unmodified, to

the ABCs, perhaps after multiplexing it and encoding it. The processing of the commands – register reads and writes, specific chip resets, etc. – is similar to the process in the HCC130, where only commands intended for an ABCStar on the hybrid where the HCCStar is located are forwarded intact to the hybrid bus. Because of the encoding and entanglement with the L0 trigger stream, it may be required to modify the command stream if it is not applicable rather than not forwarded at all.

The L1 read-out request stream is decoded by the HCCStar and enqueued as a Low Priority (LP) request in the control path. The R3 read-out request is processed as in the HCC130, and if applicable, the shortened request is enqueued as a PRiority (PR) request. The HCCStar will have an L0-only read-out mode. In this mode, an L0 accept will automatically generate an LP request and queue it to be sent to the ABCStar ASICS. Because there is no flow control on ABCStar data coming into the input channel of the HCCStar, the HCCStar must control read-out requests so that its input buffer does not overrun. This is achieved by a functional block in the HCCStar that takes the buffer occupancies of the input channels and implements a read-out request dispatch policy.

The HCCStar has 11 input channels that accept data packets from ABCStar chips, one input channel per ABCStar. These data packets can contain event data, from either an LP or PR request; or register data from a register read command. The input channel deserialises the data coming from the ABCStar, performs some validity checks on that data and separates it based on its type. Event data are stored in a 64 wide by 128 deep SRAM block that is divided in two. The lower half of the memory, with most significant bit of the address being zero, is used to store the data retrieved from a PR request, while the upper half, with the most significant bit of the address being one, is used to store the data retrieved form an LP request. Data from a register read command are stored in a small (4 deep) standard cell FIFO.

6.2.6 Irradiation Test of the HCC130

The HCC130 has been irradiated with X-rays and protons at similar dose rates and temperatures as the ABC130. Figure 6.22 shows the current increase factor as function of TID. With respect to the ABC130 the current increase is significantly lower. The HCC130 in fact contains less digital functionality, in particular fewer memory blocks. A higher current increase is expected for the next version of the chip, HCCStar, as the star architecture will imply significant changes to the chip, in particular added memory (see Section 6.2.5). This will have to be quantified with dedicated irradiations of the HCCStar.

6.2.7 Autonomous Monitor and Control Chip AMAC

The Autonomous Monitor and Control Chip provides both monitoring and interrupt functionality. A sketch of the chip architecture is shown in Figure 6.23. It will be programmed

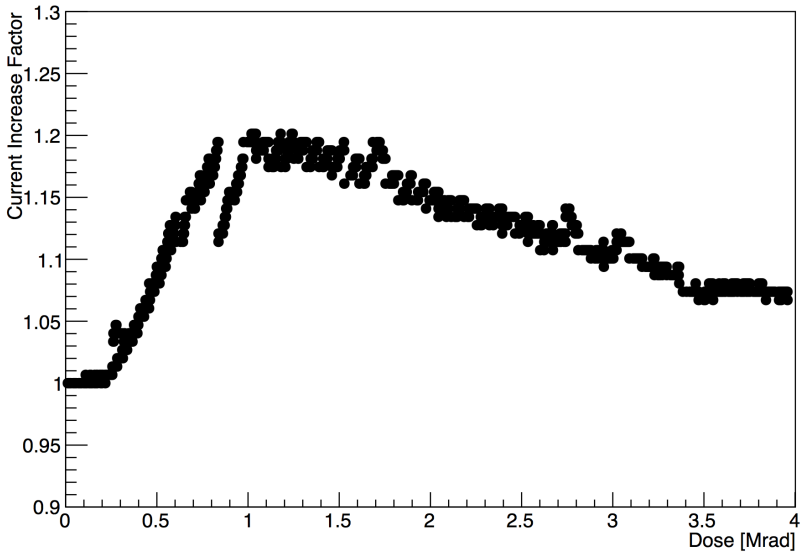


Figure 6.22: Current increase factor for an HCC130 as a function of TID during X-ray irradiation of an HCC130.

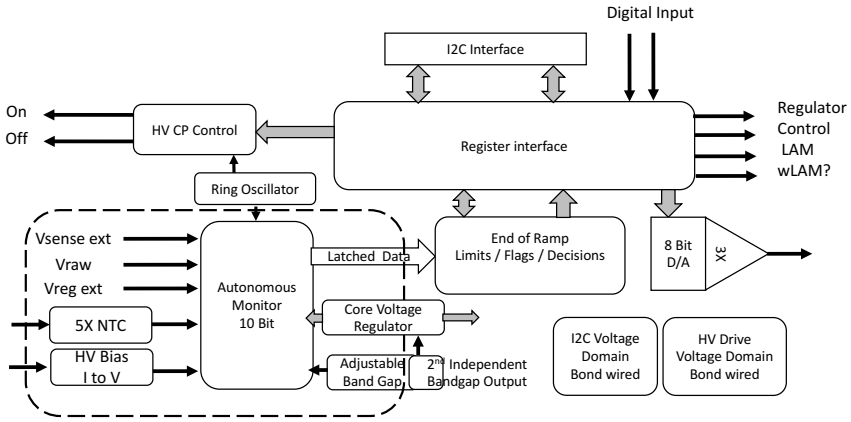


Figure 6.23: Simplified block diagram of the Autonomous Monitor and Control Chip – AMAC.

and read-out through the lpGBTx peripheral interface, planned to be a standard I^2C interface. A possible noise and offset mitigation will be discussed with the lpGBTx group that will provide for a two line uni-directional differential "LVDS like" interface using most of the I^2C protocol. The physical location of AMAC is on the power board which is located between the two hybrid strips on a sensor of a barrel strip module. Locations for AMAC on the end-cap module are yet to be determined. The AMAC allows the monitoring of voltages, temperatures and sensor bias current on strip modules at a rate of approximately one sample per millisecond. The monitoring is achieved through the use of the improved

analogue monitor (AM) block from the HCC130 chip (see Section 6.2.8). Whilst the total number of monitored quantities is yet to be determined, the monitored quantities in the current prototype are

- AMAC raw input voltage 3/5 mV /cnt
- AMAC band gap voltage 1 mV/cnt
- Sensor Bias current. Range for 4 gain settings 0.01 uA to 5 mA
- NTC thermistor Temperature Off chip Resolution 0.5°C or higher
- Internal diode based voltage $\sim$ 1.5 cnts/°C Relative to known value. This is not an absolute precise value without calibration.
- External Sense voltages (2-3) available

The basic components of the AMAC monitor are: a ring oscillator clock divided down and connected to both a counter and a reference voltage ramp generator, and a series of comparators (one for each sensed voltage) that send a write signal to record the counter value when the ramp voltage exceeds the sensed voltage. The internal ring oscillator drives the AMAC monitoring function. It has a frequency expected to vary between 35 and 40 MHz. This clock is divided by a factor of 48 to yield a counting rate for an integrating ramp ADC and counter of 0.75 MHz. An integrator provides the reference voltage ramp with nearly 1 mV steps for the comparators. The counter keeps track of the number of charge units dumped into the integrator. There is one comparator for each sensed voltage and one storage register to hold the counter value registered when the integrator ramp exceeds the monitored voltage for two successive counts. The recorded value is compared with the programmed upper and lower limits and a flag is set if the recorded number exceeds either of these values. If enabled by a mask bit this will result in an AMAC output voltage changing state. This provides a dedicated output that may be attached directly to a supply regulator enable bit or act as an interlock or it may be attached to an input of HCCStar. This approach offers a simple, low power technique to independently monitor an arbitrary number of voltages at a 1 ms sampling rate since each channel requires only a comparator, counter, two limit registers and a mask bit.

The AMAC also provides a clocked digital output to control the gate voltage on a high voltage FET intended to "switch" bias potential "on" and "off" the silicon sensor. Since the logic levels for this output may be set as high as 3 V AMAC will have a separate supply rail for this clocked HV output. A structure for interrupt servicing or direct interlock functionality is provided through dedicated outputs with CMOS (1.2 V) logic levels. These outputs may be programmed to change state when measured values exceed programmable upper and lower limits on mask enabled sensed values. The interrupt functionality offers the possibility to eliminate digital polling activity on the I^2C lines by providing a CMOS logic level on a dedicated Look At Me (LAM) line to the HCCStar. When enabled the LAM input to the

HCCStar could be used to raise a flag bit in the HCCStar output packet indicating to the upstream Detector Control system that the AMAC associated with the HCC130 with the flag bit high has a value out of range. With this module specific information, the I^2C associated with that module could be polled for out of range values on a particular module.

The default setting of the AMAC will be "DCDC LV off" with a likely power up sequence of first turning on the DCDC LV, and then subsequently each hybrid on a module by first turning on the HCC and then the ABC. Powering options on AMAC are being discussed to allow AMAC power to be derived from the DCDC LV power once enabled.

To provide a robust power service, a number of chip and system design strategies are being considered including:

- Dual I^2C busses to each AMAC chip in a string to allow either to control the chip.
- The HCCStar on the module can reset the I^2C block in the AMAC chip.
- Power boards chained along stave/petal provide the ability to turn off the upFEAST on adjacent modules power boards.
- The ABCStar and HCCStar regulator enable inputs will have internal pull up resistors so that open connections between AMAC and FE chips will leave FE chip Regulators enabled.
- The AMAC Interlock functions will power up disabled. They will require both a general "interlock enable" register bit and an unmasking of particular AM inputs to the interlock decision unit.

  Combinations of multiple channels (temperature and voltage out of range) may be required for interlock.

  Statistically significant error rates may be required to prevent single or short duration out of range readings from triggering an interlock: at least 'n' out of 'm' readings (1 ms/reading) may be programmed in to trigger an interlock action.
- Triplicated logic is implemented in the AMAC for SEU protection.

In addition, extensive simulations and measurements on prototypes are foreseen, including stress tests on the digital outputs to failure, radiations testing (TID and SEU), functional verification and state machine permanent lockup likelihood tests, as well as QC and burn-in on production chip.

6.2.8 Testing the Analogue Monitor (AM)

The HCC130 contains a voltage based analogue monitor (AM) with a 10 bit sensitivity for four internal and three external values. The AM uses a clock-driven integrating ramp generator to compare with the seven monitored quantities, and a counter is used to determine the point where the reference equals the sensed value. The value of the counter is compared to the high and low limits and is stored in monitor registers in the HCC130.

The Analogue Monitor needs to be calibrated in order to know which counter value corresponds to which voltage at the input. The input voltage pin V_{sense} is used for this purpose as it is the only channel that directly inputs a voltage into the HCC and can be swept over a large range. The result of the calibration is shown in Figure 6.24. After calibration, the input and output voltages match perfectly showing that the calibration is valid. The maximum value the AM can reach is 1023 counts (about 820 mV) and once a voltage exceeds that value, the AM was designed to keep reporting 1023; however, during testing, it was discovered that after the maximum count of 1023, the counter rolls over, appearing to start counting from 0 again. This was corrected for the Autonomous Monitor and Control Chip AMAC (see Section 6.2.7) and the next version of the HCC130. The AM needs to be calibrated as well as for each value of band-gap, DVDD, and VDD (Figure 6.25). The Analogue Monitor appears operational for a range of DVDD from 1.25 V to 1. 6V, and for a range of VDD between 1.125V to 1.35V.

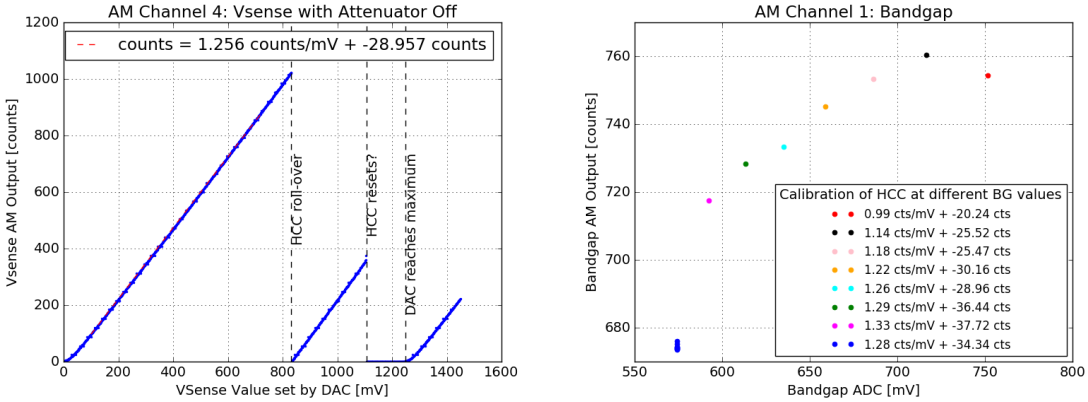


Figure 6.24: **Left**: The Analogue Monitor within the HCC130 is calibrated by varying the input voltage to V_{sense} and reading back the AM count value. **Right**: The AM is read for different band-gap values. For each band-gap value, a V_{sense} calibration ramp was taken and the slopes and intercepts are seen on each of the points.

The Analogue Monitor can be used to set up an interlock system. High and low limits can be programmed for any input channel of the AM and an interlock can be set on the General Purpose Outputs (GPO), Regulator Enable, or clock lines. The limits were set to 100 counts and 500 counts for the V_{sense} input line. The signal being monitored is GPO1 which changes

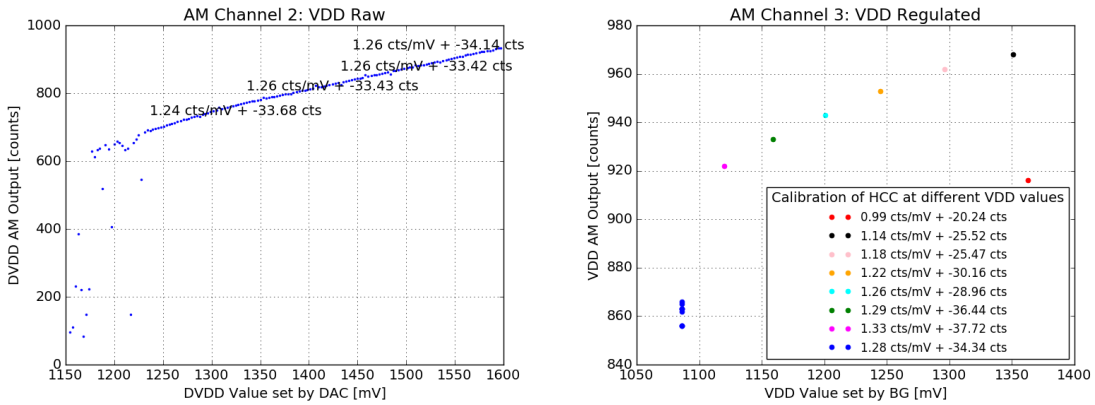


Figure 6.25: **Left**:This plot shows the DVDD Analogue Monitor output as a function of input voltage. For various values of DVDD, the Analogue Monitor was calibrated and the resulting slopes and intercepts are seen on this figure. **Right**: This plot shows the VDD Analogue Monitor output as a function of input voltage. For various values of VDD, the Analogue Monitor was calibrated and the resulting slopes and intercepts are seen on this figure.

from on to off once the interlock is triggered. For the low limit, the interlock was triggered when the low limit was reached. For the high limit, the interlock was triggered about 20 mV below the interlock limit. This is due to the fact that during the test, for each value of V_{sense}, the analogue monitor output was read out, perturbing the measurement. When the AM is not being read out during the test, the interlock is triggered only when V_{sense} reaches the limit. These results are shown in Figure 6.26.

6.2.9 FEAST and upFEAST

The chosen powering scheme for the ITk strip modules is based on the distribution of power through on-detector DC-DC converter modules [76]. The module is built around a buck converter ASIC, the FEAST chip, embedding both the power switches and the control circuitry. A number of ASIC prototype DC-DC converters have been developed to reach the required performance, with particular emphasis on radiation tolerance and efficiency. The latest version of the FEAST chip, the FEAST 2.1 provides output voltages in the range of 0.6 to 5 V from an input voltage between 5 and 12 V. The output current can be as high as 4 A. The switching frequency can be adjusted in the range 1-3 MHz. Operation at 1.8 MHz operation is the default configuration as it allows for reduced conductive noise. The chip proved to be radiation tolerant to TID up to greater than 200 MRad, and displacement damage up to $5x10^{14}$ n_{eq}/cm^2. Single Event Effect (SEE) tests showed continuous operation during exposure to heavy ions of Linear Energy Transfer (LET) up to 64 $MeVcm^2mg-1$ with short transients below 20 % of the nominal V_{out} (no destructive event, no output power interruption). The FEAST 2 design is being ported to a different 0.35 μm technology that can stand

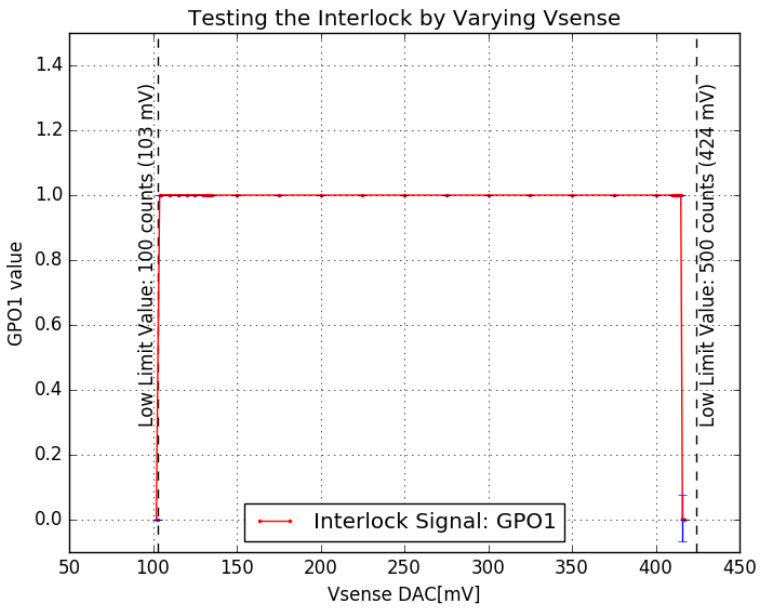


Figure 6.26: Only at the limits is the interlock triggered. For the high limit, the interlock is triggered 20 mV below the limit; however, when the test is conducted without reading the AM, the interlock is triggered only when the high limit is reached.

much higher fluence. The new chip upFEAST is expected to stand displacement damage up to 5x10^{15} n_{eq}/cm^2 The DC-DC converter modules features a custom toroidal air-core inductor needed to cope with the high magnetic field in the experiment. The layout of the module, as well as its surface mount device (SMD) components, have been chosen to minimise the emitted noise (conducted and radiated).

6.3 Hybrid Design and Prototypes

The prototype hybrid housing the ABC130s and the HCC130 is discussed in this section. The functionality of the hybrid is the same for barrel and end-cap modules, but due to the different number of channels to be addressed and different geometry designs various hybrids are required.

6.3.1 Barrel Hybrids

For the short barrel module, there is a requirement for either one or two hybrids to serve a single silicon sensor with ten ABC130s per hybrid. The electrical design of both hybrids is identical with the only differences being geometric. Electrically, the hybrid provides:

- A single power and ground domain for all ASICs on the hybrid.
- The connection of external clock and control to the Hybrid Controller Chip (HCC130).
- Distribution of on-board clock and control to the front-end read-out ASICs (ABC130).
- The return of multiplexed high speed (up to 640 Mbs) module data to the EoS.

Due to the large number of circuits required and to ensure maximal yield the design of the circuits has not pushed the boundaries regarding the design rules of the manufacturer; the track and gap geometry is $\sim$100 μm with laser drilled vias (plated-through-holes) of 150 μm hole diameter and lands of 350 μm, to maintain uniform plating and hence reliability of the via. The circuits are constructed using 50 μm polyimide dielectrics with copper conductor thicknesses of 18 μm The current prototype ABC130 barrel hybrids utilise three copper layers which results in a circuit build thickness of 300 μm. They are laser profiled with the width at 15.5 mm at the narrowest point and increasing to 17.0 mm at the widest (for approximately 20% of the overall length). The design and the layout of the hybrid has been optimised to meet the expected module noise performance whilst maintaining signal integrity of the high speed differential signals that propagate on the hybrid. Low noise performance has been achieved by the use of a single ground plane, partitioned into analogue and digital sections with no mixing of analogue and digital signals. The use of a low impedance ground plane ensures that the high frequency digital return currents will return directly underneath their signal traces and thus not corrupt the front-end analogue signals.

Furthermore, digital signals that do run close to the sensitive front-end of the read-out ASICs have been routed as differential strip lines (sandwiched between ground planes top and bottom) which has the benefit of shielding the digital signals and thus resulting in lower emissions and crosstalk. The ABC130 hybrid topology is based on a daisy-chain read-out with two groups of five ABC130s, with bi-directional data read-out, connecting up to a Hybrid Controller Chip (HCC130). This architecture results in up to four data paths into a HCC of which normally only two would be active to service the two groups of ABC130s. This topology is shown in Figure 6.27, showing both flavours of hybrid layout, referred to as Left-Handed and Right-Handed and pictorially their read-out topology.

Hybrids come equipped with two NTC thermistors of which one will be used during its operational life to allow monitoring of the hybrid temperature and a second sacrificial thermistor. The sacrificial thermistor is used to form part of a temperature interlock system during the construction phase of both hybrids and modules. Once installed onto a stave this thermistor becomes redundant and is no longer accessible.

Due to the nature of the module construction whereby there is no substrate between the hybrid and sensor and coupled with the large number of circuits required; a panellised hybrid solution has been adopted. This is made up of two parts with the flexible hybrid circuits being selectively attached to a rigid FR4[2)] former to provide mechanical support

[2] glass-reinforced epoxy laminate sheets

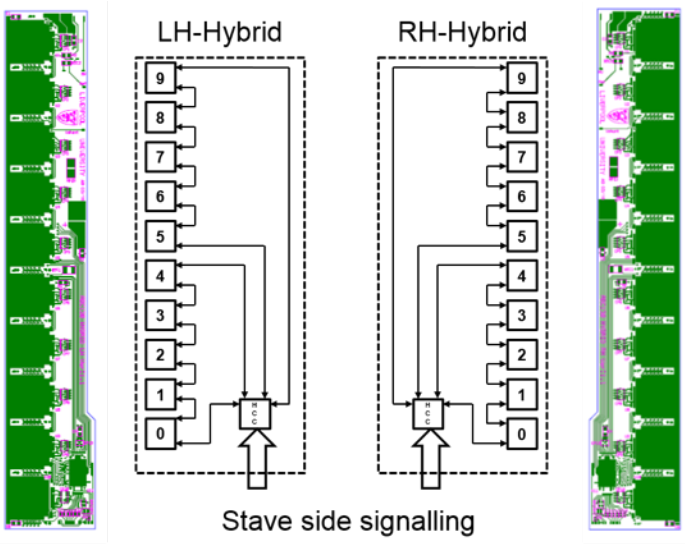


Figure 6.27: Barrel read-out topology in daisy chain architecture showing ten ABC130 connected to a Hybrid Controller Chip

during their build and testing phase. The panelisation provides for:

- Eight hybrids within a panel, four of each flavour (left-handed and right-handed).
- Hybrids are assembled in-situ with both SMDs and ASICs being attached to the circuits.
- The rigid former and vacuum holes, underneath the ASICs, providing suitable mechanical support for the Aluminium wedge wire-bonding of the bare die in-situ.
- Provision of trace routing, external to the hybrids, supplying both power and digital I/O. This enables the testing of the circuits whilst still resident on a panel. With the connections being brought to dedicated power and digital I/O connectors.

The panels also come equipped with two test coupons, one at each end of a panel. Their construction and attachment to the panel is identical to that of the hybrids, they will form an important part of the module quality control with embedded test structures which will allow for the:

- Testing of vias by the use of multiple via chains and low-Ohmic resistive testing.
- Checking of trace etching quality by the use of multiple "long" traces on differing layers of minimal width (100 μm), testing for their DC resistance.
- Addition of multiple bond pads, distributed longitudinally along the coupon. Providing for both visual and wire-bond pull strength evaluation.

Panel, hybrids and test coupons have provision for a Radio Frequency Identification (RFID) tag[3)] to be attached, this provides a 240-bit unique device ID and 512-bits of user accessible memory. The hybrids and test coupons are selectively attached to the panels, they are retained by "shaped" tabs which are required to ensure that there is no geometrical distortion encountered during the high temperature solder re-flow process of the SMD attachment. Once a hybrid has been through its full construction phase of having SMDs and ASICs attached followed by wire-bonding and testing they can then be released from the panel by the cutting of these retaining tabs.

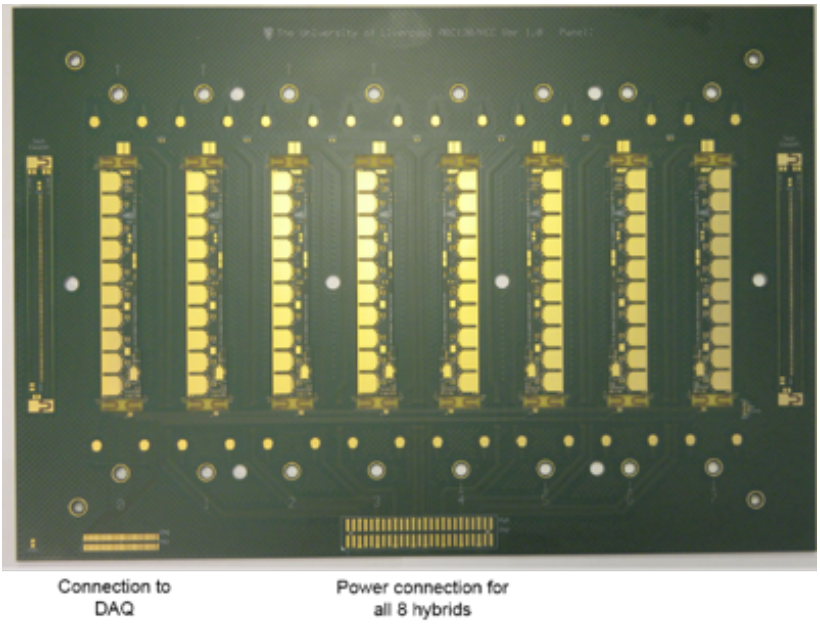


Figure 6.28: Panel for eight prototype barrel hybrids with the ABC130.

An example of a prototype ABC130 panel is shown in Figure 6.28. The eight hybrids of both types can be seen plus the two test coupons towards the ends of the panel.

6.3.2 End-Cap Hybrids

The end-cap read-out system is electrically identical to that of the barrel region, using the same front-end ASICs and infrastructures. Due to the higher multiplicity of the end-cap modules there are more flavours of the hybrids than in the barrel. The geometrical diversity of the end-cap sensors in the radial direction dictates the varying shapes and sizes of the end-cap hybrids. The number of ABC130 and HCC130 ASICs on each hybrid varies accordingly. The end-cap hybrids are four layer polyimide based flexible circuits designed and fabricated based on the industry standard High Density Interconnect (HDI) design

[3] MuRata LXMS31ACNA-010

rules similar to that of the barrel hybrids. These are laser cut to single pieces. Only filled and plugged laser drilled blind micro-vias are used in the design. Through-hole vias are implemented using staggered top-to-inner followed by inner-to-bottom layer vias, with a short offset on the inner layer. The vertically staggered via technique is to avoid problems in the lamination phase of the manufacturing process. The overall thickness of the hybrids is about 300 μm. Apart from tight real estate on hybrids in some regions of the end-cap, the routing goal has been primarily the signal and power integrity. Figure 6.29 sketches of the R0 to R5 hybrids mounted on their corresponding sensors. The red and yellow boxes in these sketches represents the ABC130 and the HCC130 ASICs respectively. Notice in the case of the R3 to R5 hybrids the segmentation across the sensor halves boundaries and the number of the HCC130 chips. Wire bond links provide electrical connection of the two hybrid segments. Each HCC130 is routed independently and reads out one half of the hybrid. The HCC130 is mounted close to the left edge of the hybrids in order to avoid long stubs on the data and TTC links to and from HCC130 not to degrade signal integrity. As in the case of the barrel, in order to speed up testing in the larger volume production phase, a panellised approach for future hybrid manufacturing is envisaged. A prototype R0 panel has been designed and produced.

6.3.3 Hybrid Designs for Star Architecture

For the next generation hybrids based on the Star architecture (see Section 5.4.1) new hybrids need to be designed. This new architecture requires the front-end ABCStar to send their data in a point-to-point configuration to the HCCStar. These many data paths will require an additional copper layer for the barrel short-strip hybrid to facilitate their routing. The geometry of the hybrid is not expected to change significantly as the placement of the front-end ASICs w.r.t. the sensor will remain as is and likewise the connections required for powering. Though there might be a requirement for a minor increase in real estate availability for the new HCCStar due to its increased size.

6.4 Power Board

The baseline powering scheme adopted for the ITk strip tracker modules is DC-DC. This powering scheme has to be both radiation tolerant and provide all the necessary power to the front-end read-out ASICs and auxiliary on-detector electronics used for monitoring, control and sensor HV biasing. Due to the geometrical constraints primarily associated with the barrel type modules, the power board is attached to the silicon strip sensor. This places severe limitations to the size of the board and the envelope it can accommodate whilst requiring its operation not to be detrimental to the module's expected noise performance.

The board provides the following functions:

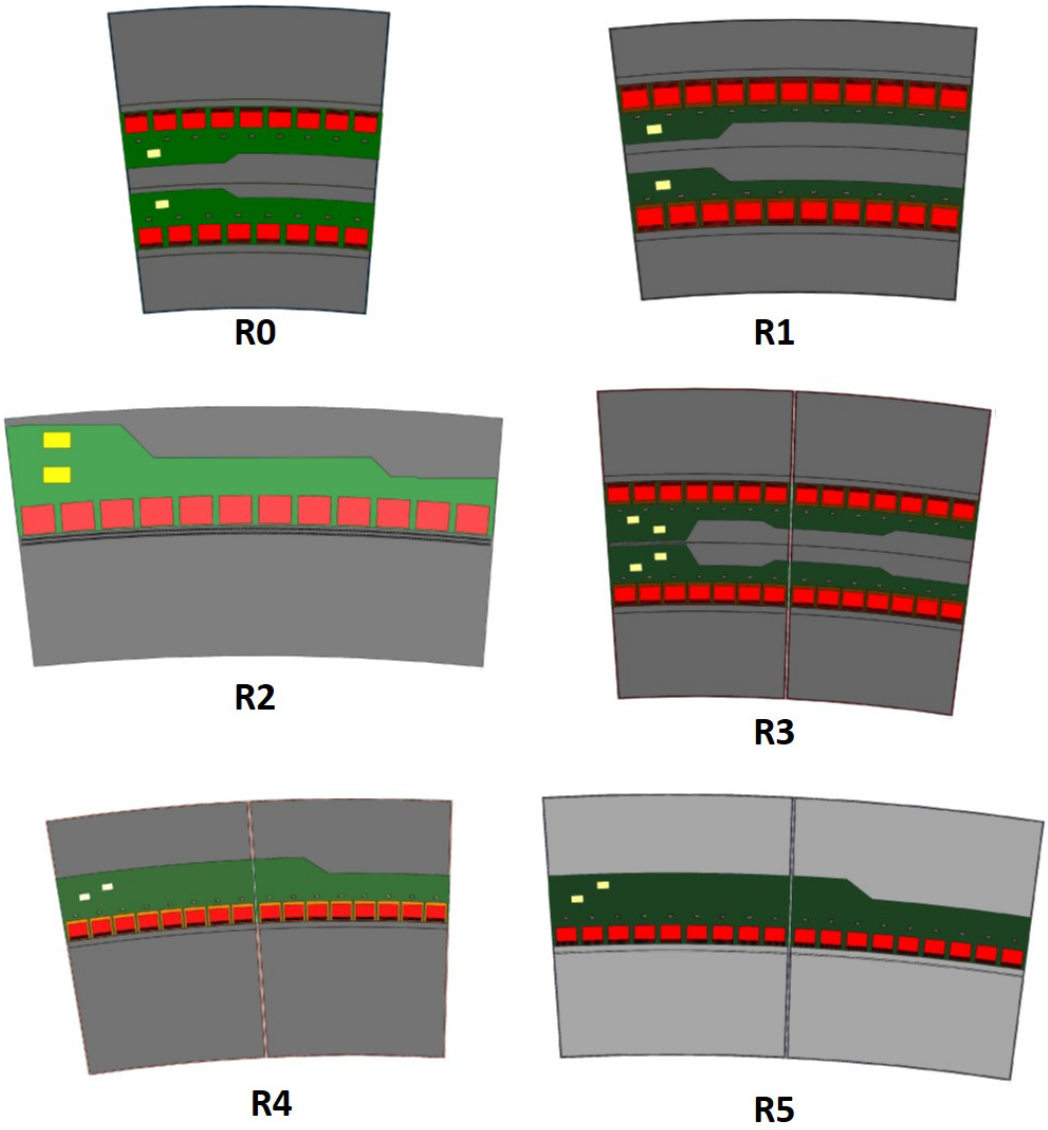


Figure 6.29: Overview of the different end-cap hybrids. The red and yellow boxes in these sketches represents the ABC130 and the HCC130 ASICs respectively.

- Power for the front-end read-out ASICs, nominally 1.5 V/4.0 A (max).
- The TID contribution could increase the current to 6.5A (max) for end-cap modules.
- Localised DCS, providing the monitoring of module front-end ASICs and DCDC converter voltages and currents and both hybrid and DC-DC converter temperatures.
- Switchable sensor HV bias and filtering with sensor current monitoring capability.
- The power board's control, configuration and DCS monitoring will be independent of the module data links, instead utilising a multi-drop I^2C link connected to lpGBTx.
- The DCS monitoring can operate in an autonomous mode providing a module level interlock in case of the risk of over temperature, voltage or current situations arising. This can operate independently of the user or can be over-ridden.
- Both DCS monitoring and sensor biasing are powered independently of the hybrid front-end ASICs. The decoupling of these powering domains allows the monitoring of both hybrid temperatures and the silicon sensor leakage currents prior to the module being fully powered. This feature allows the module to be placed into a low power mode with minimal power dissipation. When a module is configured in this mode, the hybrid temperatures will be representative of the cooling circuit embedded within the core and that of the silicon sensor. This is providing a more precise measurement of the sensor leakage current and thus enhancing the monitoring of radiation damage to the sensors.

The integration of module powering, HV sensor switching and monitoring has been realised in a "stand-alone" circuit board, currently manufactured in a "thin-build" FR4 of approximately 0.5 mm thickness. The future final circuit is being built in flexible copper-polyimide technology. A single board is able to provide power for all types of barrel and end-cap modules prior to irradiation. The design has been optimised for low noise and attenuation of EMI emissions to ensure the necessary required noise performance of the module.

Irrespective of the module type, be it barrel or end-cap, the core functionality of the power board is identical, the difference in the boards being geometrical to enable their matching up to the differing module and bus tape geometries. The topology of the board can be segmented into four groups:

- Silicon sensor HV bias filtering circuit.
- Sensor bias HV switch.
- Control and monitoring via the AMAC ASIC.
- DC-DC Power Block using the radiation tolerant buck converter, upFEAST ASIC.

A prototype barrel module type power board is shown in Figure 6.30 highlighting its functional blocks, also clearly shown are the coil, required for the DC-DC buck converter, and prototype shield box in the background.

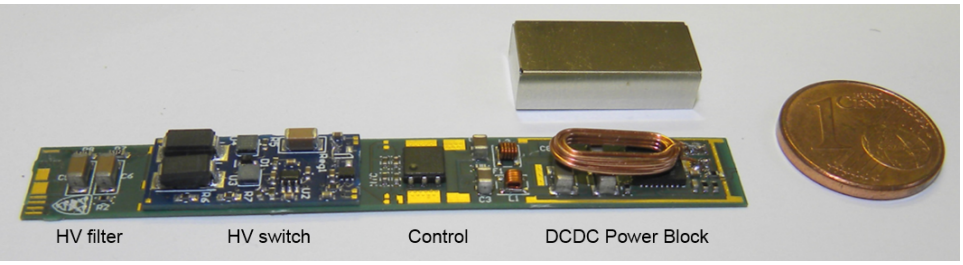


Figure 6.30: Prototype Barrel Power Board with coil and prototype shield box in the background

The use of a DC-DC buck converter and its associated EMI emissions and given its close proximity to both the silicon strip sensor and front-end read-out ASICs, makes it imperative for a shielding solution with low mass to be adopted. This is further complicated by constraints in both the height and width making it difficult to fit a toroidal coil of the nominal inductance, this type of coil would normally be the preferred choice due to its low electric and magnetic field emissions; instead a solenoidal "flat type" coil was chosen. The shielding of the high EMI part of the DC-DC power block has been achieved whilst maintaining low mass by using a mixed material solution of aluminium and copper to form a shield box. The combination of the shield box and shield layer on the power board, both referenced to local Ground, provide a Faraday cage enclosure thereby mitigating electric field emissions from the DC-DC power block. The shielding of the magnetic field is realised by eddy current cancellation; this exploits the solenoidal coil geometry whereby the time varying magnetic field, incident on the shield box, gives rise to an induced current in the shield box producing a magnetic field in opposition to the incident (aggressive) one. Although advantageous in the shielding of magnetic fields a disadvantage of this technique is that it attenuates the converter's coil inductance and thereby lowers both the efficiency of the converter and increases the conducted noise at the output (when compared to operation in free space). By maintaining a minimum coil-to-shield distance of >1.5 mm the impact on the coil inductance is at the level of 5% reduction. The combination of having to maintain shield box clearance and the physical height of the electronic components plus coil within the volume determines the actual height of the shield box; this is currently 4.8 mm. This has been shown to work very well in the attenuation of both electric and magnetic fields and thus minimising noise pick-up into the module whilst still maintaining a target efficiency of 75% at the nominal load of $\sim$2 A.

6.4.1 HV Multiplexer

The HV Multiplexer is a circuit than can connect or disconnect any malfunctioning sensor from the high voltage (or sensor bias) bus. The circuit consists of a high voltage multiplexer that controls the gate of a transistor that serves as a switch for the sensor bias. The transistor is the key component that is difficult to find or fabricate as it must switch greater than 500 V (700 V is the maximum sensor voltage), be radiation hard, and operate in a 2 T magnetic field. A variety of switches have been researched and two transistors are candidates for the ITk. The first is an enhancement-mode Gallium Nitride FET (GaNFET)[4] that can switch greater than 500 V. Radiation tests have been promising [77]. The second candidate is a depletion-mode 3D Trench Vertical JFET being developed[5]. It has the advantage, that there is already a deep understanding on how radiation will affect the device, and as a depletion-mode device it would not disable a working sensor should the transistor fail [78].

A series of irradiations on a large sample of devices (> 100) is ongoing for each candidate. Irradiations will be done with pions, neutrons, photons, and protons on devices powered either in the on-state or the off-state. Pending the results of these irradiations, a decision on which transistor will be used, or if neither will be used and therefore the HV Multplexing circuit will be abandoned. More extensive reliability testing will be done before committing to use the HV Multiplexer on production power boards.

In case the HV multiplexer option proves not to be working reliably at HL-LHC conditions, groups of modules (three or four) on one side of the stave or petal are powered by a single HV bias line. This is already implemented in the bus-tape designs for the staves and petals as presented in this document und is thus a backup solution easily to implement.

[4] Panasonic
[5] CNM in Barcelona

7 Silicon Strip Modules Assembly and Quality Control

In this chapter the different procedures used to build a strip module are described in detail. The chapter concludes with an overview of the quality control measures during the prototyping phase and subsequently during the production of the modules.

7.1 Module Assembly Steps

Since the start of the development phase of the ITk Strip Detector great attention has been paid to the ease of construction and handling of strip modules while reducing the risk of damaging sensors, ASICs or wire-bonds to a minimum. The assembly process for the modules strongly builds on the experience of building modules for the current ATLAS SCT. The number and complexity of steps to build a module in the combination of construction, bonding and quality control is optimised to guarantee sufficient throughput to meet the production targets while continuing to meet the required quality. Connections between ASICs, silicon sensors and electronics will be made through ultra-sonic wire bonding. The front edge of the ASIC is vertically aligned with the middle of the two strip rows on one sensor, with alternate channels of the ASIC bonded to different strip rows. The alignment of components on the module is determined by the requirements of the wire bonding process. The required alignment precision that is placed on the sensor elements (strips) is achieved when the modules are mounted to the local supports (see Chapter 9). This means ASICs and other components can be placed relative to their cut edges using custom vacuum tools. In addition this means that module assembly systems using dowel pins for location can be mass-produced for minimal cost. The assembly steps to construct a module are:

1. Pre-tested ASICs are glued onto hybrids[1)] and wire bonded.
2. Hybrids are tested electrically.
3. Hybrids and power boards are glued to the sensors.
4. ASICs are wire bonded onto sensors.
5. Full module is tested.

[1] SMD components are already populated.

The detailed assembly steps are discussed in the following sections using a short-strip barrel as example. Processes specific to the end-cap module are also summarised. Important to note is that all tools used for these steps are standardised for all module types at all institutes involved in the module production. The module concept is optimised to allow one production site to switch to a different module type in a very short time. The planned quality control during the production is detailed in Section 7.6.

7.1.1 ASIC to Hybrid Gluing

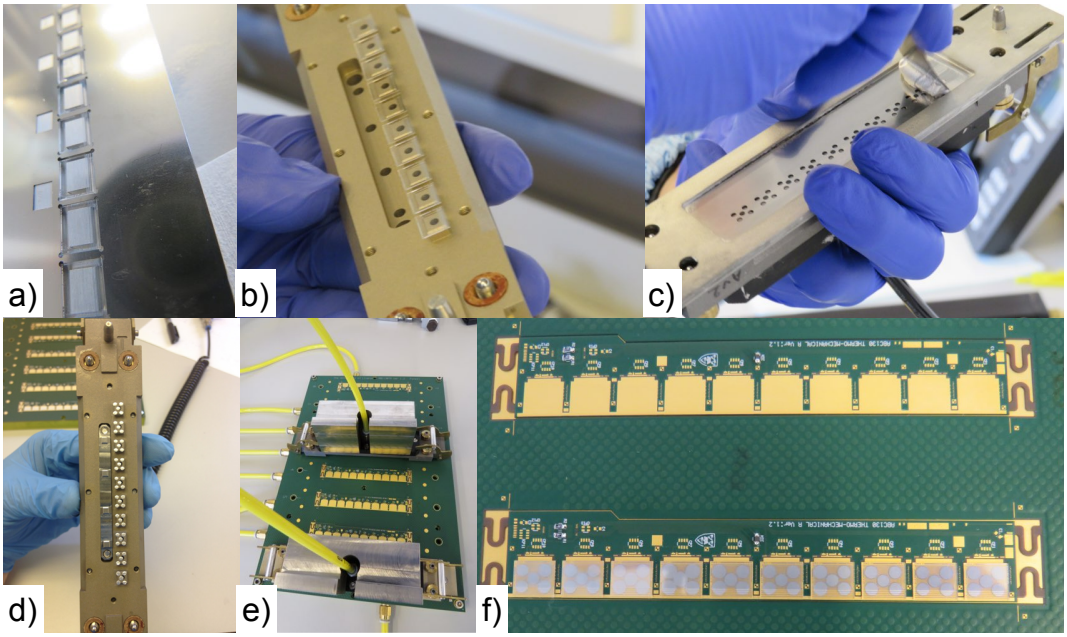


Figure 7.1: Six steps to glue ASICs to the hybrid carrier. Once wire bonded, the final hybrid is tested in the frame shown on the lower right.

The details of the ASIC to hybrid gluing process are depicted in Figure 7.1. Several tools are used for this process. Initially chips are aligned in a mask made up of a precision, laser-cut stencil and plastic tray, as shown in Figure 7.1 a. After being picked up with a vacuum pickup tool, as shown on Figure 7.1 b, the UV glue [2)] is distributed onto the ASIC pads with an automatic dispensing robot to dispense 2 μl of glue in a 5 dot pattern (Figure 7.1 c). Figure 7.1 d shows the resulting glue spots. As the last gluing step, the chips (in this figure glass dummies) are lowered onto the hybrid. The x-y alignment is set by precision holes in the hybrid panel and pins in the pickup tool. The glue thickness of 80 μm is set by four precision jacks in the pickup tool referenced to the ASIC locations by four landing pads on the panel. A brass weight is placed on top of the bridge tool to ensure the tool is held down securely. LEDs integrated on the upper side of the tool indicate when the

[2] Dymax 6-621 or Loctite 3525

touchdown is correct and UV LEDs within the tool are used to cure the glue. A curing time of 5 minutes is used. This procedure is repeated for each of the eight hybrids on one hybrid panel. Glue heights across the panel can be measured using a metrology system to check that the hybrids are within acceptable limits (see Section 7.6.4). The HCC130 for each hybrid is placed by hand and the full panel is cured overnight - to be re-evaluated with final panels. To yield acceptable temperature gradients in the vicinity of the HCC130, which has a higher power dissipation with respect to the ABC130, a silver-loaded epoxy adhesive [3)] with a good thermal conductivity is the chosen glue for connecting the chip to the hybrid. Possible radioactive activation of the glue is small and has no impact on the performance of the chip. After the glue has cured, the chips are wire bonded to the hybrid, followed by a set of electrical and thermal qualification tests of the final object (see Section 7.6.7).

7.1.2 Hybrids and Power Board to Sensors

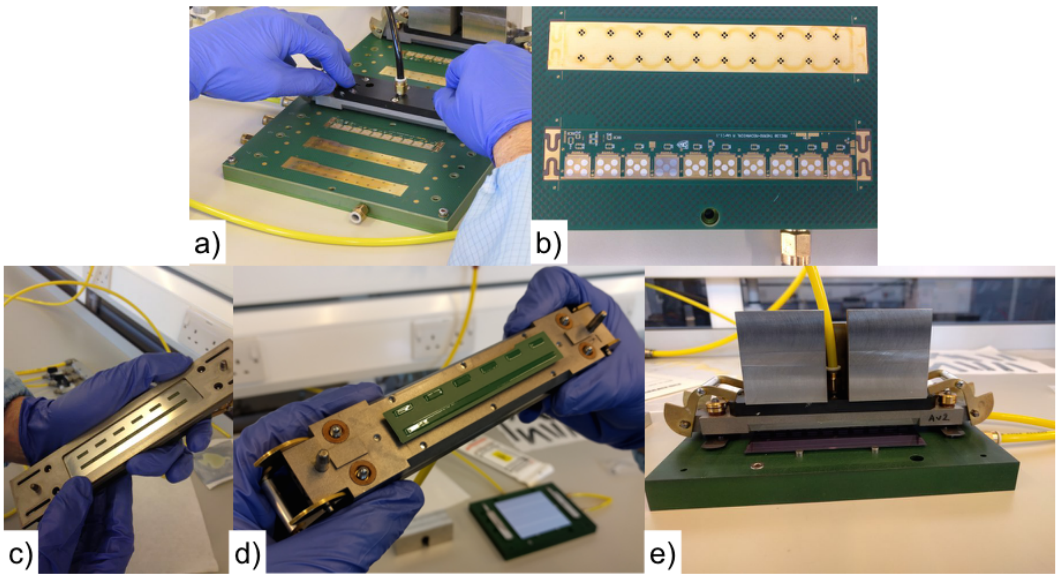


Figure 7.2: Gluing the hybrids to the sensors.

The hybrid to sensor gluing process is depicted in Figure 7.2. Tabs at either end of the hybrid are cut to release the hybrid from the panel. The hybrid pick up tool is placed on the hybrid and a vacuum is applied (Figure 7.2 a). The hybrid is picked up by the tool and removed from the panel (Figure 7.2 b). A second 200 μm thick, laser cut glue stencil mask is applied to the back on the hybrid (Figure 7.2 c), and an electronics grade epoxy [4)] is applied to the back side of the hybrid (Figure 7.2 d). The hybrid is then placed onto the sensor and weighted down to cure for another 6-12 hours (Figure 7.2 e).

[3] TRA-DUCT 2902, BIPAX
[4] fuller Epolite 5313

The hybrid placement in x-y is set by pins in the pickup tool locating into holes in the module assembly plate. The final 120 μm glue thickness is set by the four jacks in the pickup tool landing of ground pedestals on the assembly jig. The targeted glue coverage of $\sim$60% allows for any variation of the hybrids and applied glue layer's thicknesses and of the hybrid's flatness, while still supporting the relevant areas for wire bonding and ASIC cooling. An example of the resulting glue spots is shown (using a glass sensor dummy) in Figure 7.2b. After the glue has cured, the power board is glued[5)] directly to the sensor as well. The power board is currently glued by hand but similar tooling to the hybrid tools is envisioned once the final power board profile is defined. Afterwards the front-end pads of the ASICs are wire-bonded to the silicon strip pads and further electrical quality control steps are performed as detailed in Section 7.6.

7.1.3 Wire-bond Safety

The hybrids, modules and the necessary tooling are designed to minimise possible damages to wire-bonds during production and module handling. On each hybrid areas are implemented to control bond strength which is specified to be 9-12 grams. Additionally test tokens in the panels are foreseen to test critical features of the hybrids including metal layer interconnects (vias). The handling of the hybrids is eased by the use of panels containing up to eight hybrids. For the module assembly and loading, the tools are designed in a way to make damage of wire bonds close to impossible. The modules are tested directly in the transport frames and thus the handling of bare modules is minimal.

Devices are operated near constant current, therefore resonant damage in a magnetic field is unlikely. The encapsulation of wire-bonds is considered and studies are ongoing. However, the use of encapsulation adds other potential risks and possibly costs. During the R&D phase with the production and handling of more than 100 modules, no losses have been seen due to wire-bond breakage at a wide range of production sites.

7.1.4 HV Backplane Connection

The sensor is connected to the HV line through the backplane. The preferred option to provide a testable HV connection to the backplane of the sensor is using a small kapton aluminium tape. This tape is attached to the sensor backplane, either by wire bonding or by a very thin layer of silver epoxy, and traced below the sensor to a small connection on the bus tape. The bus tape connection is interfaced to the HV rail on the bus tape via the power board of the module, which will provide HV current monitoring. An alternative connection option connecting via the top metal layer with backplane connection through the conductive sensor edge, is under evaluation.

[5] also Epolite 5313

7.1.5 End-Cap Specific Details

The above steps apply generally to barrel and end-cap modules although all pictures shown are of the barrel module tools. In the case of the end-cap, the same procedure is used however tools and hybrids are arched to take into account the radial nature of the strips. The only complication in the end-cap is that the modules located at higher radius where the petal is wider (R3, R4 and R5) are pairs of modules made up of two sensors and two hybrids which are butted together by wire-bonds. In this case, the module with the HCC130 chips attached is tested first and if this is successful the second module is brought in and the stitch wire-bonds added before further testing of the completed module pair. The two modules will be only assembled together in the on-core-assembly process and before they are treated as separate modules (like R0-R2), and their testing will be done in specific frames.

7.2 Choice and Qualification of Glues

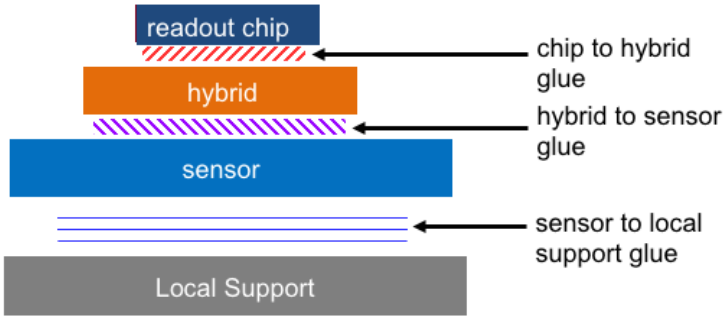


Figure 7.3: Sketch of the different glue layers for the module assembly and module loading process.

During the assembly and the loading of modules onto the local support (see Chapter 9) various adhesives or glues are used. A detailed qualification process is ongoing to qualify the selected glues and to identify alternatives where needed. The requirements for the adhesives are demanding; all glues have to be relatively short in curing time, cure with small volume shrinkage to maintain positioning precision and must provide enough mechanical stability to support wire bonding on all surfaces. The properties of the involved components should not be impaired and the glue properties, e.g. thermal conductivity, need to be stable with induced radiation. Here the most important criteria for the glues between AISCs and hybrids, and hybrids and sensors:

- Allows good electrical performance of attached components.
- Sufficient thermal conduction.
- Sufficiently strong mechanical connection.

- No corrosion, no detrimental influence on the functionality of sensors, ASICs or any other component.
- Low radiation length (i.e no metal filling).
- Working temperature range within operating temperatures of the ITk Strip Detector.
- Glass transition temperature outside of the expected operating temperature range.

All criteria have to be fulfilled both before and after irradiation up to the expected dose and thermal cycling matching the expected conditions in the ATLAS detector during ten years of operation. In Table 7.1 the additional requirements for each gluing step are summarised as well as the chosen glues and alternatives.

Table 7.1: Overview of glue requirements and chosen glues.

Glue step	**Special Requirements**	**Chosen glue**	Comment
ABCStar to hybrid	UV curable	Dymax 6-621 or Loctite 3525	fully qualified incl. radiation tolerance [79]
HCCStar to hybrid	higher thermal conductivity	silver-loaded epoxy adhesive TRA-DUCT 2902, BIPAX	fully qualified incl. radiation tolerance and activation
Hybrid to sensor		electronics grade epoxy Epolite FH-5313	fully qualified; availability unclear – alternative being investigated
Power board to sensor		electronics grade epoxy Epolite FH-5313	fully qualified; availability unclear – alternative being investigated
Module to Local Support	higher thermal conductivity to ensure low temperature of sensor	SE4445	qualified up to 2E15 n_{eq}/cm^2

7.2.1 ASICs to Hybrid Glue

Among several qualified glues the UV curable epoxy with highest viscosity was chosen as it is easy to dispense and UV curing improves the hybrid assembly flow. The ASIC-to-hybrid UV-type epoxies were obtained with the list of criteria to possible manufacturers, including the requirement to be available until end of production. None of the manufacturers could fulfil the list of requirements and manufacturers delivered options that were closest to the requirements. For the remaining three candidates for ASIC-to-hybrid UV glues, there is no guarantee that the epoxy will be available until end of production. However, the shelf life of each glue is very long so it would be sufficient to purchase a large order at the beginning of pre-production.

To yield acceptable temperature gradients in the vicinity of the HCCStar, which has a higher power dissipation with respect to the ABC130, a silver-loaded epoxy adhesive is foreseen for use. The silver loaded epoxy chosen for the HCCStar placement is more difficult to

dispense, and takes hours to cure. Detailed tests show that the chosen glues do not affect the electrical, mechanical or thermal performance of the modules.

7.2.2 Hybrid to Sensor Glue

The hybrid to sensor glue has to fulfil the same criteria as the ASICs to hybrid glue. In addition extensive glue studies have been performed using small-scale sensors, investigating the impact of different glues on the electrical characteristics of sensors before and after gluing, irradiation and temperature cycles. Performance studies in an electron beam were used to monitor adverse effects on the charge collection efficiencies of sensors glued with different glues.

7.2.3 Module to Local Support Glue

Fewer requirements had to be met for connections between sensor backplanes and local support structures. This adhesive connects materials with large discrepancies in coefficients of thermal expansion and is thus required to absorb the mechanical stress occurring during cooling, provide good thermal conductivity and maintain performance after irradiation and temperature cycles (see Chapter 9.7.6). Mechanical properties of the adhesive SE 4445 were studied and full scale prototypes were built and tested for thermal performance. Sufficient connectivity after irradiation was tested up to fluences of $2*10^{15}$neq/cm^2.

7.3 Module Material Calculation

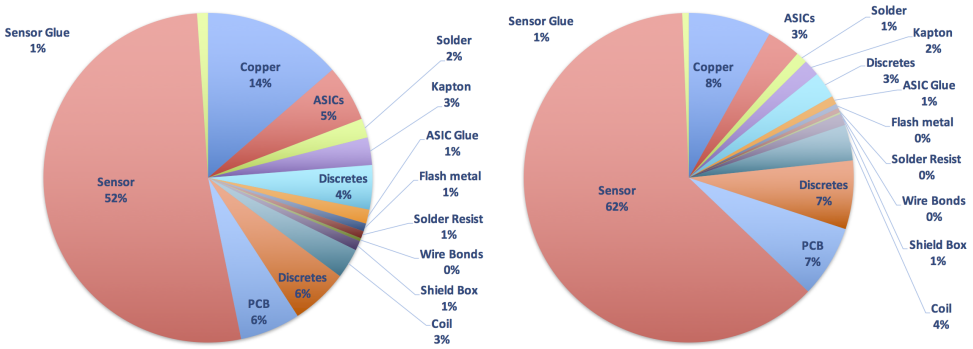


Figure 7.4: Fractional contributions for different materials to the radiation length of the barrel modules. Left: Short-strip barrel module. Right: Long-strip barrel module.

Based on the module design for the ABCStar, a material budget calculation has been made for the barrel strip modules. End-cap modules will be similar with the differences due to the fractional coverage of the sensors by the hybrids in the various rings. Assuming a 320 μm thick sensor, this yields a predicted average radiation length for short-strip barrel and long-strip barrel modules of 0.65% and 0.55%, respectively. Figure 7.4 shows the fractional contributions for the different materials to a module. As the sensor dominates the material, the modules have been well optimised to minimise material. Further reductions are unlikely as the second largest contributor to the radiation length is copper within the hybrid. Reducing the copper thickness could affect the hybrid yield.

7.4 Finalised Module

A fully assembled short-strip barrel module is shown in Figure 7.5. The green frame in which the module rests is used for connecting to power supplies and the read-out system for qualification tests.

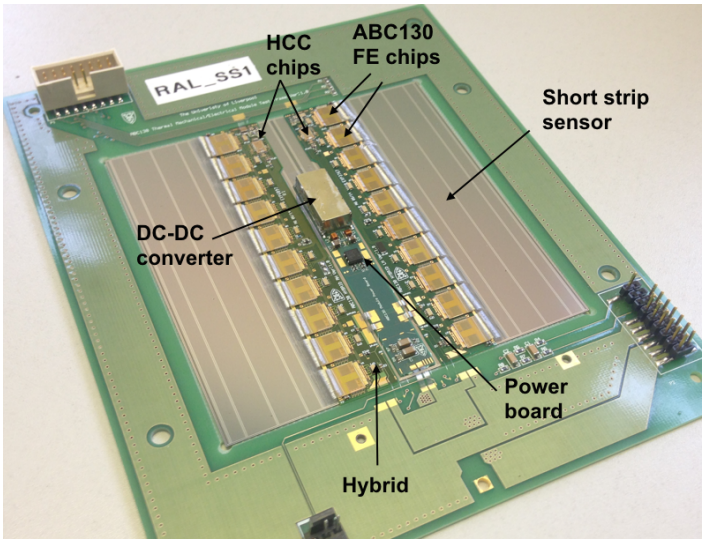


Figure 7.5: Fully assembled short-strip barrel module with ATLAS12 sensor and ABC130 chips including power board.

7.5 Prototype Thermo-Mechanical Modules

To aid the quality control program for hybrids and modules, numerous building institutes assembled and measured thermo-mechanical modules. The modules consisted of mechanical grade silicon sensors, thermo-mechanical hybrids and glass and blank silicon ASICs.

The glass ASICs were patterned with metal in the same configuration as the ABC130 bond-pads, so both back end and front end wire bonding could be trialled. The hybrids had integrated resistors under ASIC pads to simulate the predicted power output of the ABC130s, and the modules were powered by DC-DC power boards. A potentiometer was integrated into power boards which allowed the output voltage and therefore heat generation of the modules to be varied. The assembly of these modules were then used to trial the assembly tools, measuring techniques for glue heights and wire bonding programs. An example of a final thermo-mechanical module can be seen in Figure 7.6.

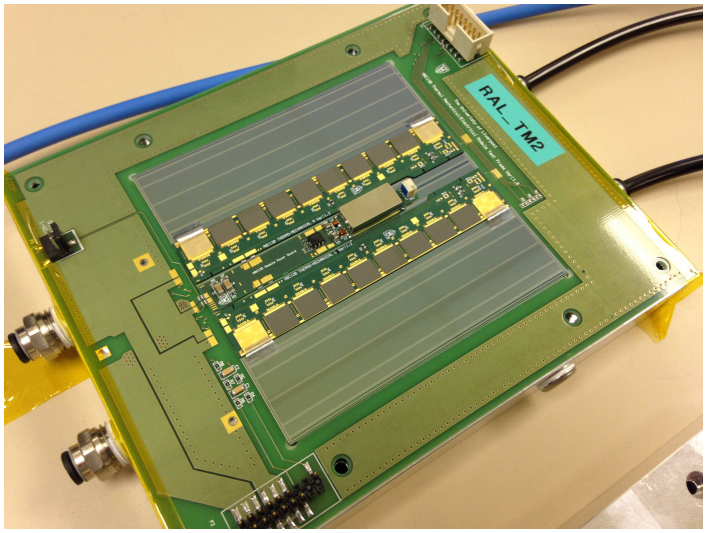


Figure 7.6: Fully assembled thermo-mechanical barrel module.

7.6 Planned Quality Control During Production

For hybrids and modules a series of tests are being designed to cover both quality assurance (see Chapter 14) and quality control (tests performed on every production item). These include a series of tests on their assembled structure (through metrology surveys), their electrical functionality and their thermo mechanical properties (including ASIC burn in, thermal cycling and long term cold tests). These tests are evolving through work from several R&D programs, and the current status of these tests are explained in the following section.

7.6.1 Silicon Sensor

The Quality Control testing protocol firstly describes a set of sensor acceptance criteria to ensure sensor minimum functionality for every sensor, and secondly more elaborate or time-consuming tests that are carried out on a sample basis to test for properties common

to a batch of sensors. Compromising between measurement time, infrastructure availability and number of faults found, sample testing should be carried out on 5 to 10% of the batch total.

Testing of each Individual Sensor:

The entire sensor surface is captured using digital imaging with high resolution, and dynamic range. The surface is inspected for uniformity. The sensor edge regions, spanning the cut edge to the bias rail, are inspected in more detail to spot scratches, blemishes, edge chips or cracks, and other irregularities. Subsequently, sensor bow is measured using a non-contact Coordinate Measurement Machine. For the barrel sensors, the minimum number of points required to cover the entire sensor surface uniformly form a grid of 11×11 points at 9.440 mm pitch. The maximum difference in z between any two points on the sensor is not to exceed 200 μm.

Electrical tests include leakage current (I–V), and sensor capacitance (C–V) against bias voltage, both ranging from $0 \ldots 750$ V in steps of 10 V with 10 sec pauses in between steps. The I–V is measured with nA precision. The current is not to exceed 0.1 $\mu A/cm^2$. For the C-V measurement, the bias voltage is increased in steps of -10 V over 5 sec, and an LCR meter with 100 pF and 100Ω resolution at $1 - 2$ kHz frequency is used to record the C-V curve. The extracted full depletion voltage should not exceed 330 V. The above tests should be carried out in a well controlled atmosphere, either clean-room atmosphere (ISO6), or dry air or nitrogen. Either custom-made jigs or a probe-station can be used for the measurements, as long as contact quality is guaranteed and light tightness is ensured.

Testing on a Sample Basis.

A leakage current stability test is used to check for the overall sensor quality, in particular the surface and edge processing. The leakage current is monitored over 24 hours at maximal bias voltage (700 V), in a dry nitrogen atmosphere maintained at 20°C. The total current variations should not exceed 3% over 24 hours. Multiple sensors will be tested simultaneously using suitable jigs. A full strip test comprises a test sequence to be carried out on each individual strip, with the sensor biased to 150 V to achieve full strip isolation. This test identifies shorts, pinholes to channels and measures the bias resistance and coupling capacitance between the metal (AC) strip and the strip implant. By using a multi-channel probe-card and associated multiplexers, a full strip test of a barrel sensor can be completed in three hours.

Additional testing on sample channels across each sensor segment includes measurements of the inter-strip capacitance (C_{is}), inter-strip resistance (R_{is}), and punch-through protection (PTP). The first is measured as a function of bias voltage from $0 \ldots 700$ V, and should not exceed 1 pF/cm beyond 300 V bias voltage. R_{is} is measured at nominal bias voltage of

700 V and should be in the GΩ range so that the foreseen deterioration due to radiation damage does not take it out of the specification of ten times the bias resistance. The PTP implant on sample channels is verified by measuring the sudden change in current when increasing the voltage across the bias resistor for a 200 V biased sensor. To avoid non-reversible effects due to excessive power dissipation in the bias resistor, the applied voltage change is limited to 50 V, with a current compliance of 100 μA.

Except for the current stability measurement, the above tests require the use of a probe-station, and are therefore carried out in standard clean-room conditions, with well defined boundary values which are consistently implemented across all test sites.

7.6.2 Hybrid Production Control

During the hybrid production the vendor will provide a full electrical test of the circuits checking for breaks, shorts and electrical continuity (comparing against the provided Gerber layout files). Only those circuits that pass will go on for SMD placement. The hybrid assembly sites will conduct further quality control: firstly by visual inspection, checking for correct component placement and no contamination of wire-bond pads (solder splash etc.). This will then be followed by metrology checking the flatness of the hybrids, the location of tooling holes etc. meets specification. Furthermore, an electrical test coupon, attached to the hybrid panel, will be checked for the quality of bond pads (wire bond pull strength), testing of trace resistance (checking for over-etching). Only upon satisfactory completion of these quality control steps will the hybrids be released for ASIC attachment. Once hybrids have had their ASICs attached and wire-bonded there will be a requirement for basic electrical testing to confirm electrical functionality followed by a burn-in step; this will require the hybrids to operate at an elevated temperature whilst being read out and clocked over a long period of time (to be defined). This burn-in step is being used to identify ASIC infant mortality (see Section 7.6.7).

7.6.3 Hybrid & Module Visual Inspection

After each assembly step, all hybrids and modules will be visually examined for any physical faults or defects. Such faults will include

- Missing or damaged SMD components
- Glue seepage covering wire bondpads or sensor guard rings
- Debris or physical contaminents on items
- Missing or dangling wire-bonds

All assembly sites will be equipped with appropriate optical microscopes to perform visual inspection throughout the course of all hybrid and module build steps.

7.6.4 Hybrid & Module Metrology

After the gluing of ASICs to the hybrid, and the gluing of hybrids and power board to the sensor, metrology (x, y and z) will be carried out for grading. A range of techniques exist amongst the hybrid and module institutes for such measurements. These include

- Optical Metrology - Uses a camera optics with small depth of field, with the focusing providing a measure of the z position
- Laser Focus Metrology - Uses a laser instead of an optical light source for a focus on the surface
- Laser Scan Metrology - Uses a laser to scan over the surface of the object, proving a visualisation of the flatness
- Touch Metrology - Uses a stylus with the object being measured after contact with the component surface

For all measurements in production, only optical and laser measurements will be used for module metrology in order to avoid potential damage to the silicon sensor by the use of a touch probe. However, because of the protective passivation layer of the ASICs, touch probe measurements could used for the hybrid metrology. Extensive calibration of equipment and measuring techniques have taken place since the IDR [80], to allow for both the comparison of data and for the qualification of the equipment for production.

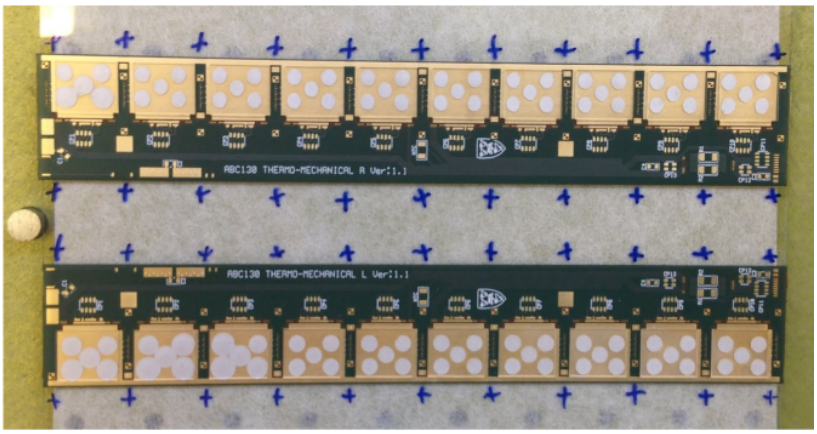


Figure 7.7: A dummy barrel module assembled using glass pieces for metrology calibration, with blue crosses indicating the positions of the optical focusing for measuring the surface of the glass sensor.

Figure (7.7) shows a dummy module assembled using the glass pieces for metrology calibration. The blue crosses indicate the positions of the optical focusing for measuring the surface of the glass sensor. Fiducial markers on the hybrid were used for focussing, giving the z height of the hybrid surface, and touch-down probe measurements are made on top

of the glass ASICs. Using glass ASICs also allows for optical focusing on the surface of the ASIC landing pads, facilitating an additional calibration measurement.

For metrology of hybrids and modules it is envisaged that the measurements will be fully automated, with pass/fail requirements introduced into custom written software. Such automation is aimed at reducing measurement times and improving the reproducibility of the measurement positions of the objects under test. The constraints that are needed for x, y and z measurements are explained in the following subsections. At present these constraints are based on extensive barrel and EC experience with 250 nm R&D items and 130 nm thermo-mechancial modules.

X-Y Hybrid Constraints

After ASIC-to-hybrid glueing, metrology will be carried out to investigate the positions of the ASICs relative to the hybrid. Any large displacement of the ASICs could cause issues for the wire-bonding, both in terms of the backend bonds to power the hybrid, and the front end bonds to the sensor strips. Nominally, 1.42 mm spacing between ASICs results in a bonding length of 400 μm. The X-Y rotation of the ASICs is constrained by the pickup chip tray, and measurements have shown the maximum variation in position using this method to be <100 μm. As groups, chips can be misaligned to the hybrid in large numbers but the maximal displacement allowed is set by the hybrid panel requirements, which is $\pm$ $\sim$100 μm in X and Y. Placement of ASICs will be measured relative to fiducial markers on the hybrid. (Figure 7.8 left)

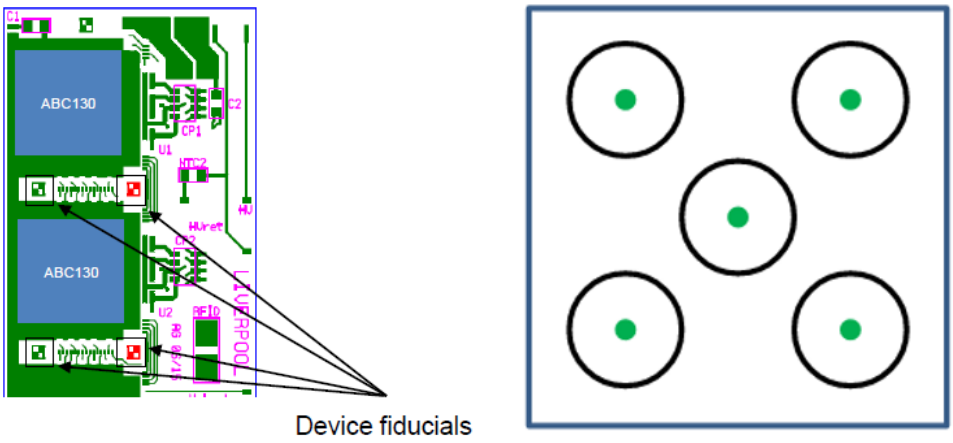


Figure 7.8: **Left**: Fiducial markers on hybrids for measuring X-Y positions of glued ASICs; **Right**: Five positions on each ASIC pad that are measured in z before and after ASIC attachment for calculation of glue heights

z Hybrid Constraints

The glue layer thickness between the ASICs and hybrid is designed to give a good coverage for thermal performance, mechanical stability and to take up any variability in the hybrid shape/thickness. The thermo-mechnical program was mostly executed using an Ag-Epoxy with a glue stencil designed to achieve a target glue thickness of 80 μm after compression. With ASIC-to-hybrid glueing defaulting to UV glue, the application process will likely use (semi-) automated dispensers, which has already been shown to be able to dispense such amounts accurately. If the separation between the hybrid and the ASIC is too large, then the glue coverage of the ASIC is reduced, the glue doesn't cure correctly and the chip will detach from the hybrid after thermal cycles. If the separation is too small then the glue will spread out of the edges of the ASIC and on to bond pads on the hybrid. Such seepage has been measured when the glue gap was reduced to 40 - 50 μm. Using hybrids made in the 250 nm program, a target glue thickness was found to be 80$\pm$ 20 μm.

Glue thicknesses can be measured using either optical metrology or a touch probe metrology. Before ASIC gluing, each ASIC placement pad is measured (in five locations) in z relative to the panel surface (Figure 7.8 right) and a z-plane is formed. After gluing, measurements are made on the same X-Y locations on the top of each ASIC. Glue heights are then calculated as the difference in z-planes after the ASIC thickness (300 μm) is subtracted.

Module co-ordinate system

For the purposes of module metrology, the following co-ordinate system is used (Figure 7.9):

- X: Perpendicular to strips
- Y: Parallel to strips
- Z: Out of module

Module Constraints in X–Y

As the module size is dictated by the sensor size there is no module X-Y constraints in relation to the stave or petal mounting. However constraints exist in relation to the hybrid's post gluing position on the module. Data and power bonds from the hybrid ends must be set from the bus tape, and there should be no part of the hybrid overhanging the sensor perimeter. Extreme (X-Y and angular) translations of hybrid positions on the modules will affect both the ability to wire-bond the front end channels and glue the power board to the sensor. Studies have shown that the requirements of the hybrid on sensor positions are constrained as follows

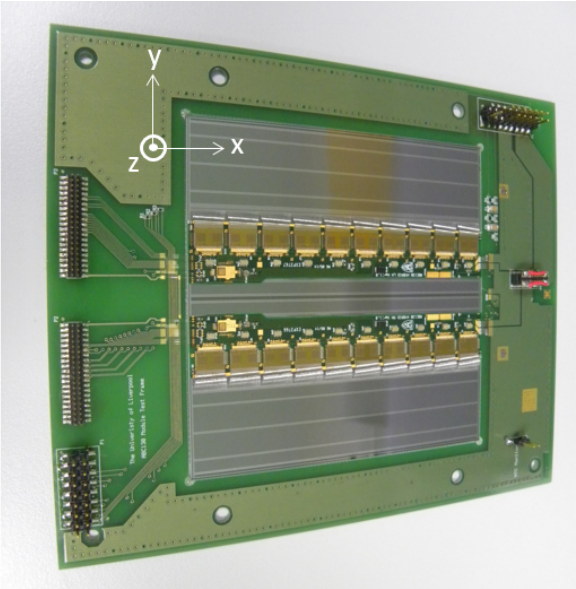


Figure 7.9: Adopted co-ordinate system for module metrology

- Δ X < 1 mm (Hybrid is positioned over front-end wire bondpads)
- Δ Y < 4 mm (Hybrid overhangs end of sensor and cannot be bonded to data, HV, or LV lines on the stave). Specially for EC modules R3-5 the requirement will likely be tightened to exclude hybrid-hybrid collisions at the sensor-sensor boundary of these split modules
- $\Delta\ \Theta$ < 0.7 Degrees Rotation (Power board cannot be glued to sensor in between two hybrids)

The positions of the hybrids on module will be measured using non contact (optical or laser) metrology techniques.

Module Constraints in z

The uniformity in z height of the finalised module is predominantly set by the hybrid-sensor gluing step. Therefore the z module constraints are dependant on the hybrid-sensor glue thickness. Experience from the 250 nm program showed that a glue thickness greater than 160-180 μm resulted in hybrids that did not stick to the sensors. It also showed that thin layers (<80 μm) resulted in glue seepage, either prohibiting the front-end wire bonding, or covering the sensor guard ring and consequently deteriorating the electrical performance of the module. A further optimisation criterion is the module noise which decreases with increasing gap size between the hybrid and the sensor. At the current gap of 120$\pm$40 μm the noise performance is found to be acceptable. Similarly to the technique for measuring glue height measurements of ASICs on hybrids, Hybrid-to-sensor glue heights are determined

by the subtracting the hybrid thickness (275 μm) from the difference in z between the hybrid surface and sensor surface.

It has been shown that the $>$ 95 % of hybrids glued by the different institutes adhere to 120$\pm$40 μm limit using the current generation of assembly tooling and they can all measure the glue height using the established metrology techniques.

To check for sensor bowing after module assembly, z envelope measurements of the entire assembled module will be made using non-contact metrology techniques. The current thermo-mechanical program will be used to set the tolerance for allowed module bow. However experience from the 250 nm electrical stave program showed modules with bow of up to $\sim$300 μm could be glued to the stave.

7.6.5 Hybrid & Module Wire-bonding QC

Quality control of wire-bonds is extremely crucial, as it has a direct correlation to the final electrical grading of all assembled hybrids and modules. For both hybrids and modules, connections between ASICs (ABCStar & HCCStar), Silicon sensors and electronics will be made with the use of wedge Aluminium (25 μm) wire bonds. Visual inspection (Section 7.6.3) of wire bonds will be made, to check for failed or missing bonds, as well as bond deformation size/shape. Pull bond tests will be made on a sample of bonds on a module, and using the test coupons on hybrid panels (Section 6.3). As well as confirming the required wire bond strengths, such pull-tests on sacrificial bonds will also check for possible failure modes such as bond lift off from pads, heel-cracks or neck-breaks [81]. As with the SCT build, wire bond strengths will be required that exceed standard mil spec requirements [81]. Wire-bond breakage due to varying currents in a magnetic field are not expected as all currents are static on short time scales and thus no resonances are expected.

Hybrid Bonding QC

The wire bonds form the electrical connections between the ASICs and the hybrid for data, communication, powering and grounding. Additional wire bonds form the connections from the hybrid to the hybrid panel to allow for electrical testing. Failed bonds should be detected either by post-bonding visual inspection or identified in electrical confirmation tests. The bond-pads on the hybrid and the ASIC bond-pads are sufficient to accommodate second bonding/re-works if required. This was achieved by modifying the bond-pad size to 95 um by 190 um for the digital and power (backend) ABC130 bond-pads. Previous studies for SCT module wire-bonding showed the average bond size footprint for 25 μm wire to be 40 μm by 70 μm [82]. Additionally, backend bonds are now only on two sides of the ASIC, reduced from three sides in the ABCn250 chipset, simplifying and accelerating

the hybrid bonding. For the ABCStar there will be a further reduction to only one side for backend bonds.

Module Bonding QC

Wire bonds are made from each front end (FE) ASIC channel to a silicon strips, resulting in 2560 front-end bonds for the long-strip modules and 5120 bonds for a short-strip module. Additional wire bonds are needed for powering and data connection to the module frame for electrical testing. Due to the four row bonding of the modules, visual inspection is required after each each full bond-row layer has been completed. This is due to the difficulty of removing failed bonds or re-bonding where this is an overlapping bond from a subsequent row.

An alternative method for wire-bond QC is also being investigated. This uses an electrical test setup integrated into the wire-bonding machine. Wire-bonds appear as channels in the software as the connections are made. This allows the bonding machine to check that all the front-end bonds are made between each row bonding stage.

7.6.6 Pass/Fail Grading for Wire-Bonded Hybrids & Modules

All bonds are required for a fully functioning hybrid. Lack of bonds will be detected though non responsive ASICs in later electrical tests. For modules, all data, communication and power bonds must be functional. The number of un-bonded or non-responsive front end channels will contribute towards the acceptance decision in the module QC checks. As an example, the allowed number of dead channels for end-cap SCT modules was <15 (2% of all channels) or <8 consecutive channels as absolute limit, but achieved 0.16 %. Similarly the allowed number of dead channels for the ITk Strip Detector should be absolutely better than 2% and are targeting 0.2% of bad channels.

7.6.7 Hybrid & Module Electrical Tests

All planned electrical testing of hybrids and modules must be scalable to match large production throughput at each build site, currently estimated to be up to three hybrid panels per day, and up to three modules per day. (see Chapter 13). All produced hybrids and modules will go though a series of electrical tests to validate their functionality and performance. All read-out hardware and DAQ will be designed to be usable for testing hybrid and modules, and for both the barrel and end-cap builds. It is envisaged that hybrids will be tested in multi-panel crates, and modules will be tested in batches of 4 or more.

Hybrid Testing

Hybrid testing checks for front-end chip functionality, including threshold, noise, occupancy and gain measurements on completed hybrids. Tests will be made using a single connector to panel of eight hybrids. or using a multi-panel crate system to allow parallel, high throughput testing. The testing procedure will be as follows:

1. Chip Communication:
    a) Putting the HCCStar in its startup mode, extracting the ID of the HCCStar
    b) Capturing Chip IDs to verify communication to all wire-bonded ABCStar.
2. Strobe delay - A scan that sets the timing (delay) of an injected calibration pulse with respect to the arrival time of the command to actually issue that pulse. This ensures that the discriminators, always firing at the clock frequency, will be synchronous with the calibration signal.
3. Three Point gain - Threshold scans are performed for three different injected charges (0.5 fC, 1 fC & 1.5 fC) . The resulting response curve is fitted linearly to obtain values for its estimated discriminator offset (mV at 0 fC) and the channel gain (slope, mV/fC). The three-point gain also determines input noise for each channel.
4. Noise Occupancy - A test that measures the noise occupancy as a function of threshold.

Module Testing

Module testing will check post assembly hybrid functionality as well as the final module performance. A test sequence will be run which will provide information on noise, threshold and gain for each channel. Noise values per channel will be used to indicate broken or missing wire-bonds, as well as noisy or dead ASIC channels. A test sequence would be compose of the following steps:

1. Chip Communication (as above)
2. Strobe delay (as above)
3. Tuning - The Trim Range is used to individually trim each channel in order to minimise the variation in the response. A threshold scan is performed for eight different trim ranges. For each Trim Range, a range of target thresholds is studied to determine the maximum number of channels that can be brought into line and the corresponding TrimDAC value is evaluated for each individual channel.
4. Response curve - A scan that extends the three point gain scan to ten points. This test is done after the channels have been trimmed. Injected charges are 0.5, 0.75, 1.0, 1.25, 1.5, 2.0, 3.0, 4.0, 6.0 & 8.0 fC.

5. Noise occupancy (as above).
6. Scans of the leakage current versus bias voltage.

In addition I-V characteristics will be performed on each completed module to the final operational voltage, which is going to be maximal 700 V.

Hybrid & Module Thermal Tests

It is planned that ASIC burn-in, thermal cycling and long term cooling tests will be closely based on SCT production experience, with the relevant changes made to the upper and lower temperature regimes.

Thermal finite element analyses (FEAs) indicate the lowest temperature the modules and its components expect to experience during operation at the HL-LHC. The temperature of the components is strongly correlated to the expected evaporation temperature, and whether or not the pixel and strips systems share a common cooling loop. This affects the lower temperature of any long term or thermal cycling testing. Consequently thermal tests are being designed to operate down to -40°C.

Hybrid Temperature Tests

A key quality control test for hybrids is the ASIC burn-in tests to check for any early ASIC death. Based on SCT experiences, long term (> 90 h) tests will be carried out on hybrids at $\sim$37°C. For testing the thermo-mechanical properties of the assembled hybrids, thermal cycling will be performed ten times through lower and upper temperatures ranges informed via further FEA studies.

Thermal Cycling and Low Temperature Testing of Modules

Test setups are being designed to allow for both thermal cycling and long term cold tests of modules including environment and dew point control. Preliminary studies have been performed on thermo-mechanical modules. A cold test jig (see Figure 7.10 a) consisting of a cold box with an external coolant chiller/heater has been used. With a vacuum chuck (see Figure 7.10 b) compatible with the barrel strip module test frame, modules are connected to the chill block but electrically isolated.

The cold test jig has demonstrated that it can maintain its coolant temperature at -30°C with 25W of heating load applied on to 2 vacuum chucks (50W total cooling power tested), which exceeds cooling power needed for testing four barrel strip modules simultaneously.

Thermo-mechanical modules with hybrids dissipating up to 8 W of heat have been cycled between 24.4°C and -37°C, with no evidence of mechanical damage. This process will help

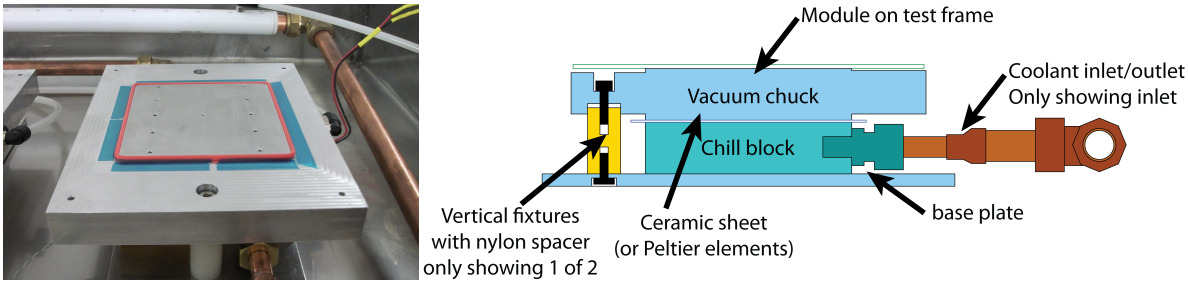


Figure 7.10: A cooling stack for one silicon strip module. **Left**: Assembled cooling stack in the cold box, showing the vacuum chuck on top. **Right**: A drawing of the cooling stack build up.

to define the necessary number of cycles to burn-in modules and will highlight pathological failure modes for modules under thermal-cycling.

8 Strip Module Test Results

During the extensive R&D programme for the ATLAS ITk Strip Detector, a number of module prototypes have undergone a thorough electrical characterisation both before and after irradiation. The modules have been measured in both bench-top setups in collaborating institutes and at test beams. The most critical parameters under study are the Equivalent Noise Charge (ENC) in electrons, the gain, the collected charge, the hit efficiency, and the noise occupancy. The ENC and gain are determined using standard threshold scans for binary read-out systems. The same threshold scan technique is used for single-chip boards, hybrids and modules (see Chapter 6.2.3). Most results presented in this chapter are based on the prototype ASICs: ABC130 and HCC130.

8.1 Overview of Tested Prototypes

Multiple prototype ABC130 modules were assembled for detailed testing. To improve the understanding of modules operating under a series of different conditions, barrel short-strip sensors were first connected to a fully populated barrel hybrid. In order to compare results for long and short strips under the same conditions, long-strip modules were approximated by connecting adjacent short-strip columns with wire-bonds to form long (4.8 cm) strips. In all of the assembled long-strip modules, sections of the module were connected to only one column to allow direct comparisons between the two lengths on the same sensor connected to the same front-end ASIC. In Figure 8.1 pictures of a fully constructed ABC130 short-strip module with power board (left), and a long-strip module (centre) are shown. The sensors used for these prototype modules are from the ATLAS12 series with a lower resistivity substrate than is required in the final sensor specification. The lower resistivity substrate results in a lower signal after irradiation than expected with the final sensor specification. The ABC130 read-out noise increases with fluence and this issue has since been addressed in the design of the production chip ABCStar and is discussed in Chapter 6.

For these reasons the modules under test are not entirely representative of a production ITk strip module. However, the modules behave as anticipated based on earlier measurements and if appropriate corrections are made for the increase in signal height that will be realised with increased substrate resistivity, the module is expected to meet the requirements for the lifetime of the HL-LHC. This will be confirmed as part of the pre-production qualification of the production process.

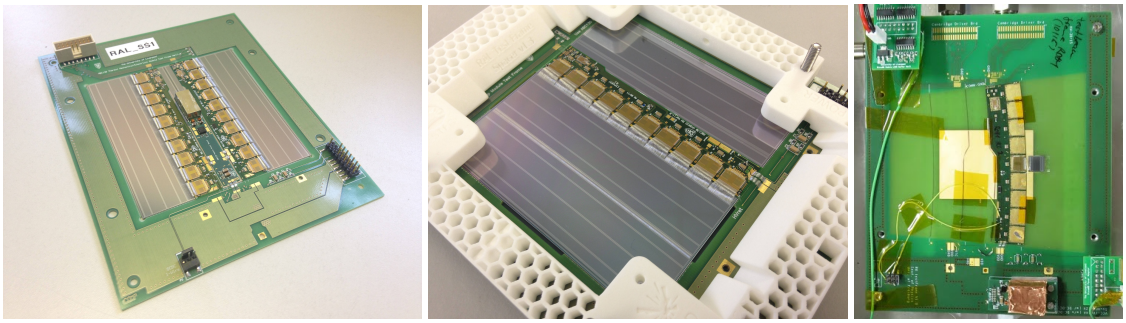


Figure 8.1: Pictures of **Left:** a fully assembled ABC130 Short-Strip Barrel Module, **Centre:** a Long-Strip Barrel Module and **Right:** an end-cap DAQload.

In addition, mini-assemblies (called "DAQload") (Figure 8.1 right) consisting of a partially-populated end-cap hybrid with a single HCC130 and up to three ABC130s and one or two ATLAS12 mini-sensors (see Chapter 6.1) have been assembled. These assemblies allow rapid testing without using large number of ABC130s or full size sensors. Table 8.1 summarises the tested prototypes discussed in this chapter.

Table 8.1: Summary of prototypes of DAQloads and full modules tested.

Module	Description	Test Beam	Comment
DAQload10	Barrel hybrid with three ABC130s, two wire bonded to mini-sensors.	May-15 DESY	
DAQload13	Two ABC130 and two ATLAS12-mini sensors.	May-16 DESY	Sensors neutron irradiated ($2x10^{15} n_{eq}/cm^2$), ABC130-1 non-irradiated, ABC130-2 X-ray irradiated (4 MRad with 0.85 MRad/hr at RAL at -5°C).
SS1	Full barrel module with ten ABC130, short strips.		
LS2	Full barrel module with ten ABC130, short and long strips.	Nov-15 DESY	
LS3	Full barrel module with ten ABC130, short and long strips.	Jul-16 CERN	Irradiated at PS with protons ($8.0x10^{14} n_{eq}/cm^2$ and TID=37.2 MRad)
LS4	Full barrel module with ten ABC130, short and long strips.	May-16 DESY	

8.2 Irradiation of Module Prototypes

It is critical to study the performance of strip modules after being irradiated to accumulated fluences expected at the end of HL-LHC operation. As well as measuring any degradation in sensor performance, it is important to study any changes in the performance of a mod-

ule's electronic components, such as ASICs and hybrids. The maximal expected fluence for the Strip detectors is $1.2\text{x}10^{15}\text{n}_{\text{eq}}/\text{cm}^2$ including a safety factor of 1.5 (see Chapter 3). As described in Chapter 6, irradiation programmes have been carried out on individual components such as ABC130, HCC130 and silicon sensors. In addition, an irradiation was performed on a full electrical module. The irradiation performed and subsequent tests are explained in the following sections. The module and DAQloads were tested to study both the effects of the total ionising dose (TID) and the bulk damage (NIEL) via proton and neutron irradiations.

8.2.1 Proton Irradiation

A single 130 nm long-strip barrel module (LS3) was irradiated at the CERN Proton Synchrotron with 24 GeV protons resulting in both ionising (TID) and non-ionising energy loss (NIEL) damage. The hybrids and their read-out ASICs suffer damage from ionising radiation. The sensors suffer bulk damage due to non-ionising energy losses (as presebted in Chapter 6.1.2) and surface damage from ionising radiation (as presented in Chapter 6.1.3). The irradiated module is used to confirm the model of how the performance of the key parameters evolves with increasing radiation. This model is based on measurements made on individual components.

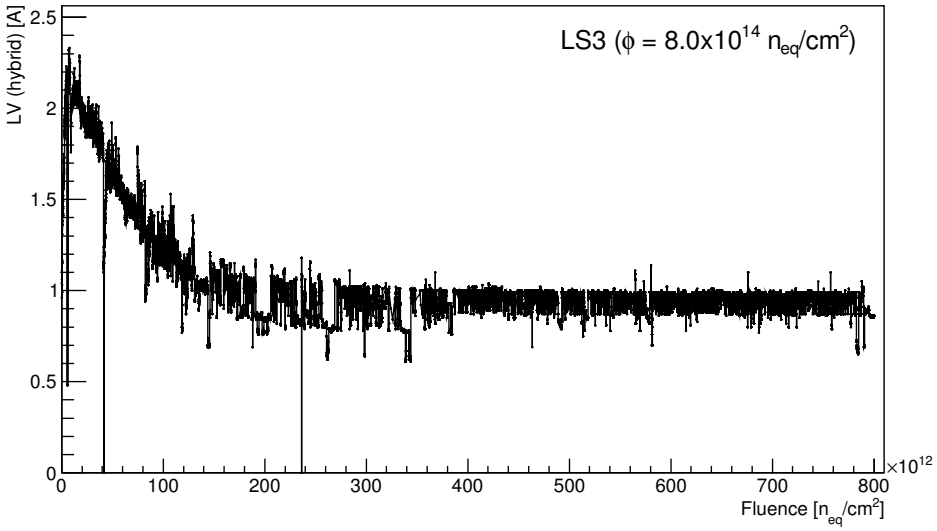


Figure 8.2: Low voltage current of the hybrid as a function of irradiation dose in $\text{n}_{\text{eq}}/\text{cm}^2$ for module LS3 during the irradiation at the PS.

During irradiation, module LS3 was mounted in a box, oriented at a small angle relative to the beam axis to allow for a time-efficient irradiation. A movable stage allowed scanning of the sample to uniformly irradiate the full sensor area (scanning window 100×100 mm^2). Aluminium strips were placed on the front and back of the module to measure the applied fluence using the Aluminium activation. The device was cooled to -20°C, the sensor

was not biased, the chips were powered, configured and clocked, and current monitored throughout the irradiation period of 19 days (Figure 8.2). For seven days and for additional short periods the beam was not available. Large changes in current are observed in the beam off periods.

At a given rate of ionising radiation and operational temperature the change in the front-end digital current was consistent with changes observed in the digital current seen in the irradiations of the individual ABC130 and HCC130 chips. The total NIEL dose received by the module was calculated to be 8×10^{14} n_{eq}/cm^2 and the total ionising dose was 37.2 MRad. The level of irradiation matches the maximum expected in the strip system without the safety factor of 1.5. The standard annealing cycle (80 minutes at 60 °C) to migrate radiation defects was not performed after the test beam measurement and therefore the signal from the silicon sensor is smaller than expected after the applied radiation level.

8.3 Test Beams

A series of tests have been performed at the DESY-II and CERN SPS test beam facilities to investigate the detailed performance of the strip module before and after irradiation. The DESY tests used electrons with an energy of 4 to 4.8 GeV, while those at CERN used 120 GeV pions. A range of devices were studied, including end-cap and barrel modules, with miniature, short-strip and long-strip sensors. The tests included irradiated devices to measure any possible degradation in performance. Two of the tested prototypes are pictured in Figure 8.3.

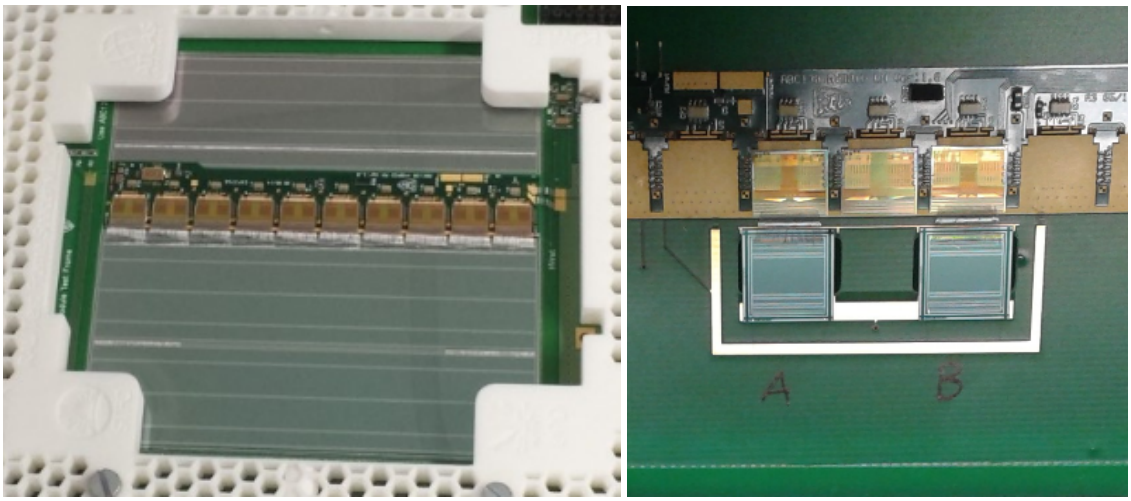


Figure 8.3: **Left**: LS2 module, tested at DESY in November 2015. **Right**: DAQload 10, tested at DESY in May 2015.

8.3.1 Test Beam Setup

For both the DESY and CERN test beams, tracking was performed using the EUDET-style telescopes, which consist of six MIMOSA26 pixel sensors with a pitch of 18.4 μm. An additional pixel layer with an FE-I4 read-out was used to improve the timing of the telescope, allowing individual tracks to be matched to hits on the strip module under test. Tracks were reconstructed using the General Broken Lines algorithm [83], resulting in a pointing resolution of 1.5 μm (2 μm) at CERN (DESY) [84].

The strip modules were mounted between the third and fourth telescope planes. For irradiated devices, custom cold boxes were used to maintain a temperature of -35 °C resulting in a sensor temperature of ∼-25 °C and an ASIC temperature of ∼-20 °C. All devices were read out using the current test hardware[1)] and software (ITSDAQ), integrated with the telescope data acquisition software (EUDAQ). An example of the test setup is shown in Figure 8.4.

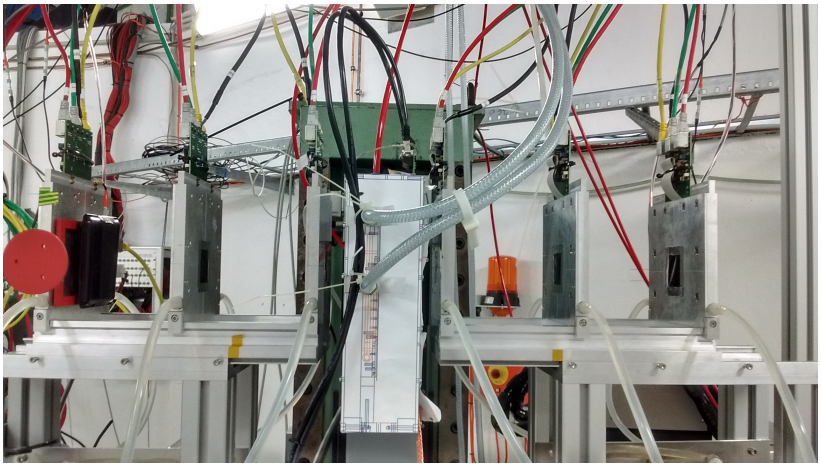


Figure 8.4: The DURANTA Telescope at DESY with a barrel mini module under test.

The size of the beam spot was chosen to be ∼1 cm^2, allowing for hits on strips wire-bonded to individual ABC130s. For each strip device, threshold scans were performed with a minimum of 200,000 events taken for each threshold setting (∼2k events/strip). The scans were repeated for each bias voltage being studied, and then for the different positions when testing the full size sensors on LS2, LS3 and LS4, or on each mini-sensor for a DAQ Load. Additionally, scans were performed without beam to determine the pedestal and noise levels.

[1] ATLYS FPGA development board

8.4 Results of Electrical Tests and Test Beam

8.4.1 Noise Measurements

Figure 8.5 summarises the noise measurements as a function of input load capacitance for a range of prototype devices including the ABC130 front-end prototype, ABC130 single-chip test cards and full barrel hybrids with front-ends connected to both discrete capacitors and sensors. The input capacitance in the case of sensors is taken from the capacitance measurements performed on ATLAS12 full and mini sensors. Good agreement is observed for the prototype and capacitive loading of hybrids and single chips. This is true both for capacitors connected between front-ends and ground (simulating capacitance to the back-plane) and for capacitors connected between front-end channels (simulating inter-strip capacitance).

When sensors are attached to single-chip cards or full hybrids, it is observed that there is an increase in noise over the passive capacitor measurements. The increase in noise due to strip resistance is 5.3 % (14.2 %) for short (long) strips in agreement with simulations.

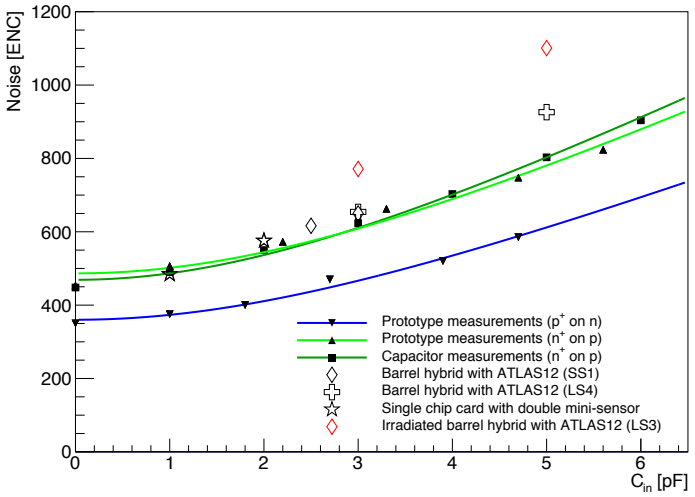


Figure 8.5: Measured noise as a function of input capacitance for a range of prototype devices. All results are taken from threshold scans using an injected charge of 1.5 fC whilst the input capacitance when sensors are attached is taken from direct measurements of the sensors.

Also shown in Figure 8.5 are the results for LS3 after irradiation (see Section 8.2.1). The increase of 25-30 % of the measured noise, observed for both short and long strips, is expected due to the lack of enclosed transistors in critical regions of the ABC130 front-end, which have already been addressed in the ABCstar front-end. An additional decrease of noise is expected for the production chip arising from the change to resistive rather than active feedback (see Chapter 6); this decrease in noise is expected to be more pronounced for the longest strip lengths.

8.4.2 Electrical Characterisation of ABC130 Barrel Modules

All devices were read out using the ITSDAQ software with an ATLYS FPGA read-out board. Modules were biased to 400 V (non-irradiated) or 500 V (irradiated), and electrically characterised as described in Chapter 7. Shown in Figure 8.6 and 8.7 are the gain and noise performance of a short-strip module (SS1) and long-strip module (LS4). In the case of LS4, Stream 1 is connected to long strips whilst Stream 0 is connected to short strips. Stream 0 comprises the 128 front-end channels closest to the chip edge whilst Stream 1 comprises the channels furthest from the chip edge. As expected the gain is independent of the load on the front-end channel. The chip-by-chip gain variation seen here is corroborated by the results taken when the wafers are probed.

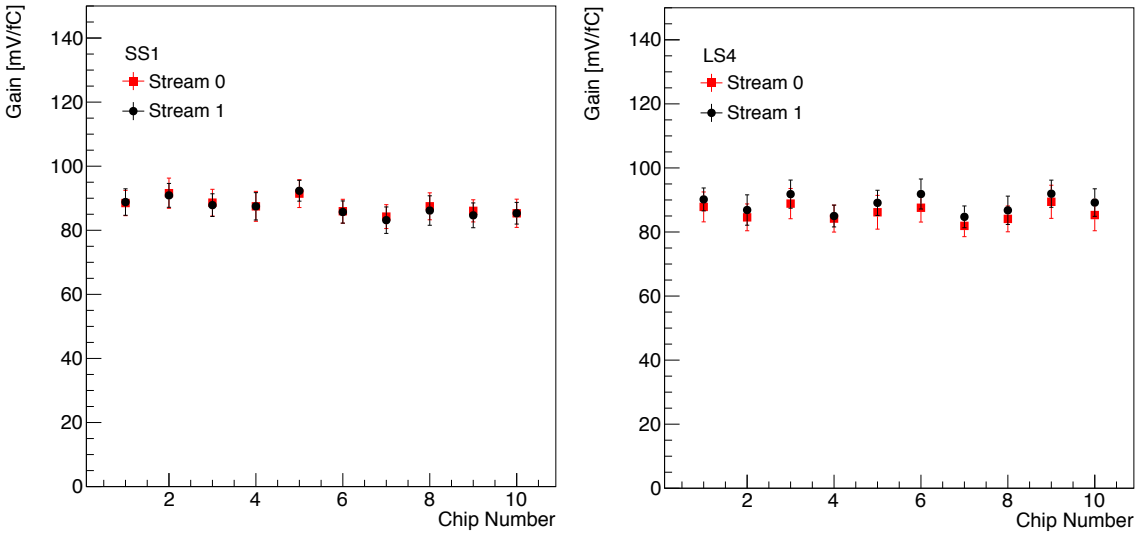


Figure 8.6: Gain averaged per ABC130 read-out chip for **Left**: the short-strip module SS1 and **Right**: for the long-strip module LS4.

The average noise per read-out chip is summarised in Figure 8.7. In the left figure the short-strip module is shown. The small differences in Stream 0 and Stream 1 for chips 6 and 7 are due to the presence of the DC-DC converter close to those chips and are within expectations. In the right plot of Figure 8.7 the results of LS4 are shown. Due to the increased capacitive and resistive load to each channel in case of the long strips, the noise is higher. The noise difference on LS4 between Stream 0 and 1 is consistent with expectation.

For binary read-out systems, the noise occupancy is a critical parameter. The requirement for the ITk Strip Detector is less than 1×10^{-3} channel noise occupancy at a threshold resulting in detection efficiency greater than 99%. If the noise is well understood with a single-Gaussian spectrum, the noise occupancy is simply related to the single-channel noise. In order to investigate the noise, large statistics noise occupancy runs have been performed on module LS4. The results are shown in Figure 8.8.

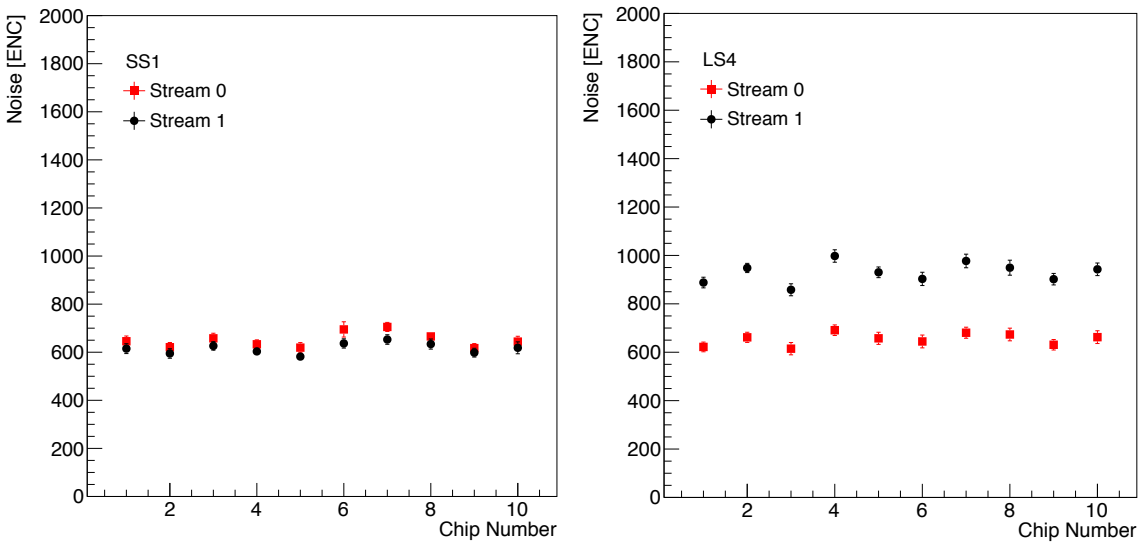


Figure 8.7: Input nose in e^- ENC and averaged per read-out chip for **Left**: short-strip module SS1 and **Right**: long-strip module LS4 utilising ABC130 chips. In LS4 the long strips are read out in Stream 1 and short strips in Stream 0.

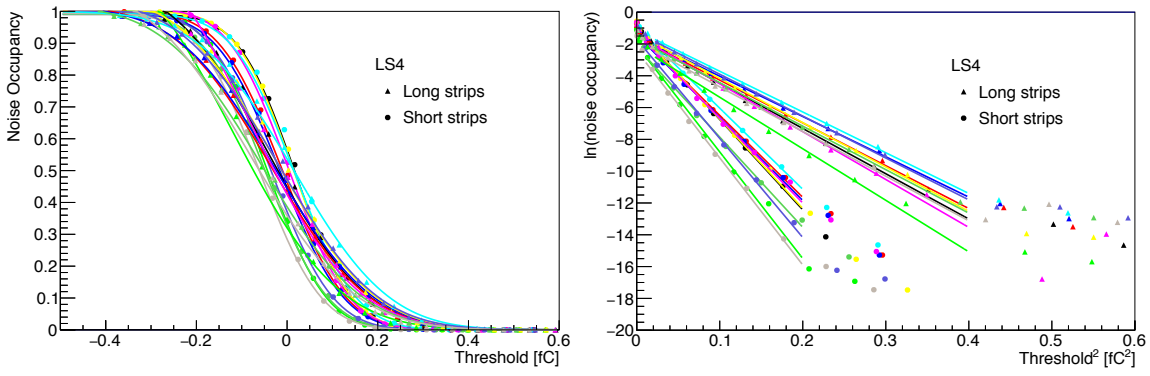


Figure 8.8: **Left:** Fit of the noise occupancy vs. threshold distributions for LS4 with an error function (ERFC). **Right:** Fit of the natural log of the noise occupancy (ln(occ)) as a function of the $Threshold^2$ for LS4.

The noise occupancy as a function of the threshold is fit with an error function; the shape describes the distribution well with a minimal non-Gaussian tail in the noise spectrum. The single-channel noise can also be extracted from a linear fit of the distribution of the $Threshold^2$ as a function of the natural log of the noise occupancy [85]. The spectrum is linear over the range of$Threshold^2$ that is expected in standard operation. Figure 8.9 summarises the three methods for extracting the single-channel equivalent noise charge. All three agree well indicating the noise and channel noise occupancy are within expectations.

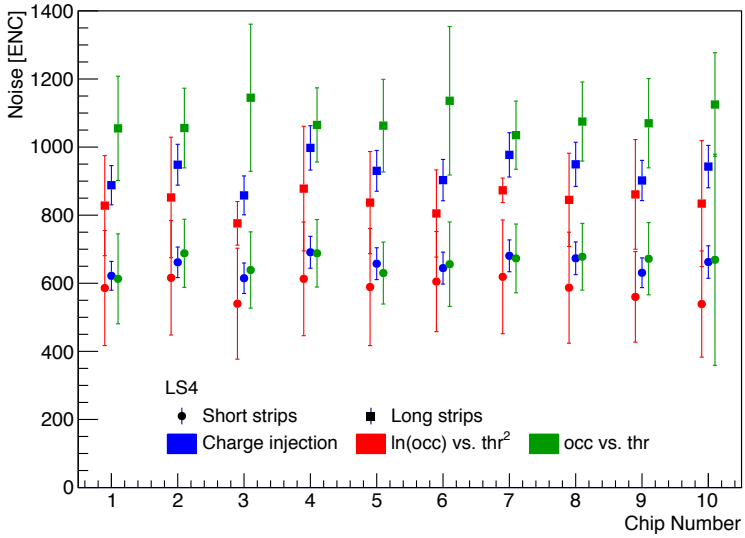


Figure 8.9: Equivalent noise charge estimates from response curves (RC) and derived from noise occupancy fits with error functions (ERFC) and using $ln(occ)$ vs $threshold^2$ fit.

8.4.3 Electrical Performance after Irradiation

Current vs. voltage (I-V) characteristics were taken for the sensor of the irradiated LS3 module at a range of temperatures (Figure 8.10) whilst the module was unpowered. The leakage current before irradiation is much smaller and off the scale. The sensor behaves as expected within the uncertainties due to the lack of annealing of the module after irradiation. The sensor's leakage current evolves as expected with temperature over the full bias and temperature ranges studied.

In addition, measurements of noise and gain were performed using the internal calibration circuit. In Figure 8.11 the noise is shown for module LS3. Both strip types exhibit an increased noise which is consistent with expectations from ABC130 single chip irradiations.

After the irradiation to the aforementioned levels, the module is still fully functional. All components of the module are operational after the irradiation, allowing for full electrical characterisation and test beam measurements to be performed on the module.

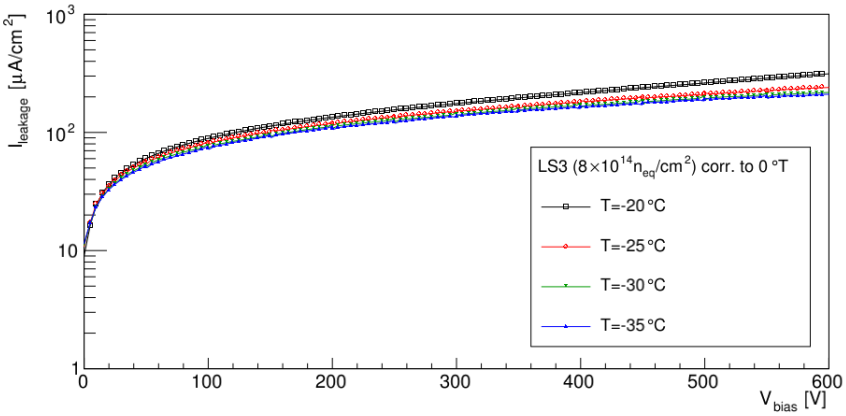


Figure 8.10: I-V characteristics of the proton irradiated LS3 module with chips unpowered for a range of low temperatures recalculated to 0 °C. The leakage current before irradiation is much smaller and off the scale.

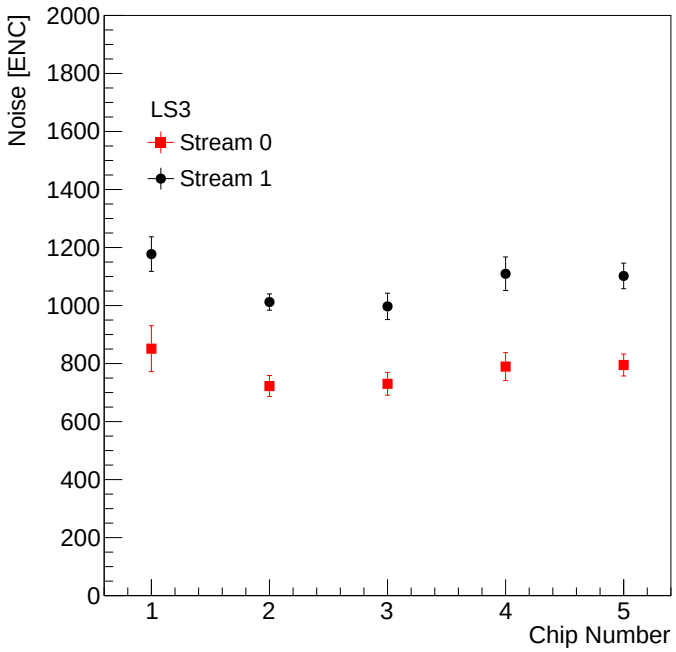


Figure 8.11: Input noise in e^- ENC and averaged per read-out chip for five ABC130 of the irradiated LS3 module at a bias voltage of 600 V.

8.4.4 Test Beam Results

DAQloads

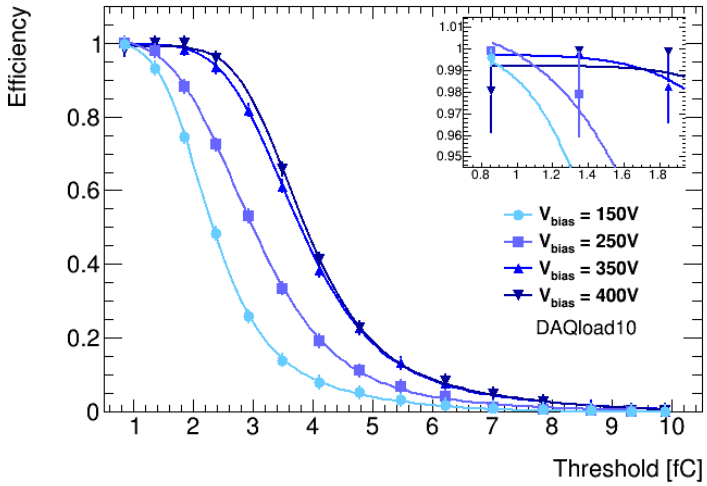


Figure 8.12: Efficiency versus threshold for one sensor on DAQload10, at four different bias voltages.

In all test beam measurements, threshold scans were performed and the tracks reconstructed with telescope data were used to determine the efficiency at each threshold. The efficiency is defined as the fraction of events in which a cluster is recorded whose centre is within 200 μm from the track position as it passes the device under test. The threshold scans can be used to infer the distribution of the collected charge, as the difference between two points corresponds to the fraction of electrons or pions producing a signal between those two threshold values. The threshold scans are then fit to a skewed error function, allowing for a determination of the most probable value (MPV) for the collected charge.

Figure 8.12 shows the threshold scan for four bias voltage settings of one of the sensors on DAQload10. For measurements with a bias voltage below the depletion voltage of 350 V the efficiency is observed to be lower as the collected charge is reduced, resulting in lower measured values for the MPV.

The excellent pointing resolution from the telescope allows for investigation of the behaviour within and between the strips. Figure 8.13 shows the hit likelihood as a function of the distance a track passes from the centre of a strip. This is defined as the probability that a hit will be recorded in a given strip. The curves show a flat efficiency in the central region of the strips, and a width consistent with the strip pitch of 74.5 μm. Similar results are seen for all devices. There is a drop in the efficiency near the strip edges which is attributable to the effect of charge sharing between strips. This can also be seen by looking at the average cluster size for lower thresholds, as shown in Figure 8.14. The likelihood of two-strip

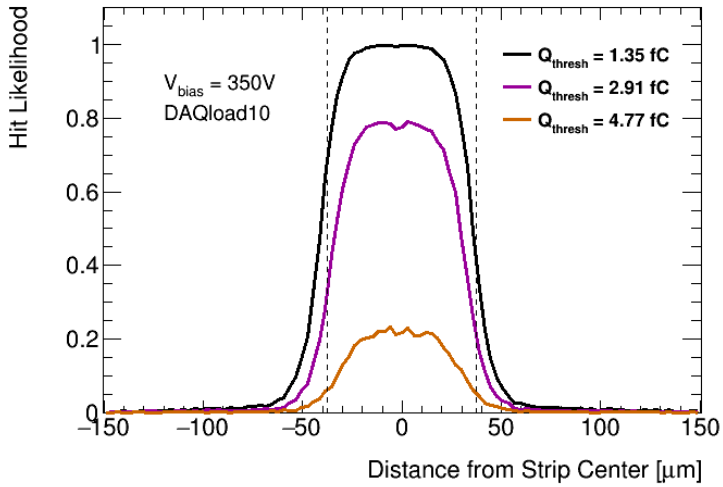


Figure 8.13: Hit occupancy, as a function of the residual from the track to the centre of the strip as measured with DAQload10. The strip width is indicated with dashed lines.

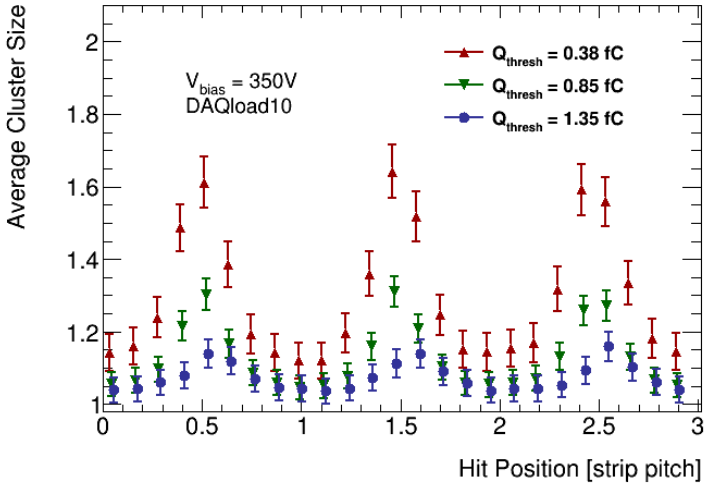


Figure 8.14: Average cluster size versus hit position, along three strips for DAQload10. The integer position values correspond to the centre of the strips.

clusters increases for electrons passing in between two strips, where charge sharing is the highest.

Non-irradiated & Irradiated Long-Strip Modules

The efficiency curves were evaluated at the DESY test beam for the long-strip and short-strip regions of a non-irradiated module (LS2) at two different bias voltages, shown in Figure 8.15. The discrepancies in the curves arise from different ABC130s attached to the short and long strips.

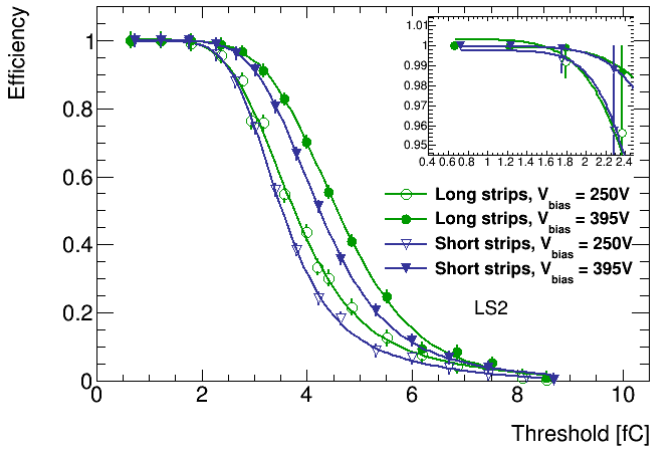


Figure 8.15: The efficiency versus the threshold for two bias voltages and two positions on the long-strip module LS2.

A testbeam at CERN allowed a comparison to be made between the performance of modules before and after irradiation to 8×10^{14} n_{eq}/cm^2. Figure 8.16 shows the efficiency curves for long-strip regions of seven ASICs of the non-irradiation module (LS4) and for the irradiated module (LS3). As expected, the charge collection is reduced significantly after irradiation.

As a cross-check of the collected charge, the CERN test beam efficiency curves are compared to the sensor charge collection studies described in Section 6.1.2. As a ^{90}Sr source is used in those sensor studies, the average clusters are much wider than from test beam due to multiple scattering. To make a meaningful comparison, the full charge of the cluster should be taken from each device. For the test beam analysis, this cluster charge is approximated by requiring the tracks intersection is within 15 μm from the centre of the strip; this requirement removes most of the charge sharing to the neighbouring strips. For the sensor studies, the cluster charge is fit to a Landau convoluted with a Gaussian; the fraction of the fit function above the threshold is defined to be the efficiency. Figure 8.17 shows the comparison of the source-based sensor studies to both the non-irradiated and irradiated module test beam results. For comparison the results from DAQLoad13 (measured at DESY) are presented on

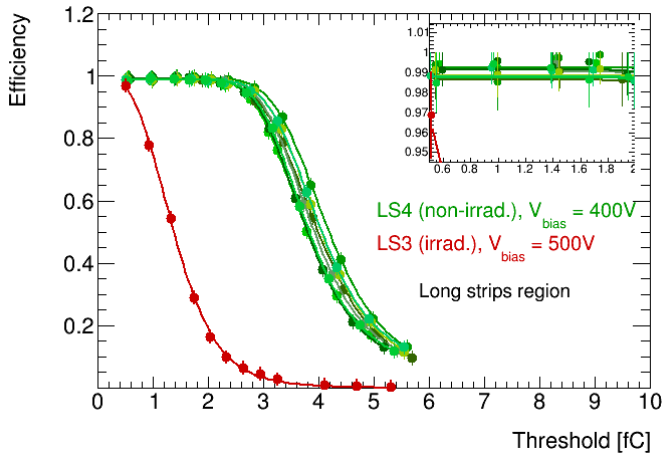


Figure 8.16: The efficiency versus the threshold for four ASICs on the non-irradiated long-strip module LS4 (shown in green), and one ASIC on the irradiated module LS3 (shown in red).

the same plot. DAQload13 was irradiated with neutrons at Ljubljana, and received 60% more radiation than the expected highest radiation level in the ITk Strip Detector including a 1.5 safety factor. In both cases, LS3 and DAQload13, the test beam data is consistent with source data, giving confidence in the normalisation for the signal and efficiencies measured in test beam.

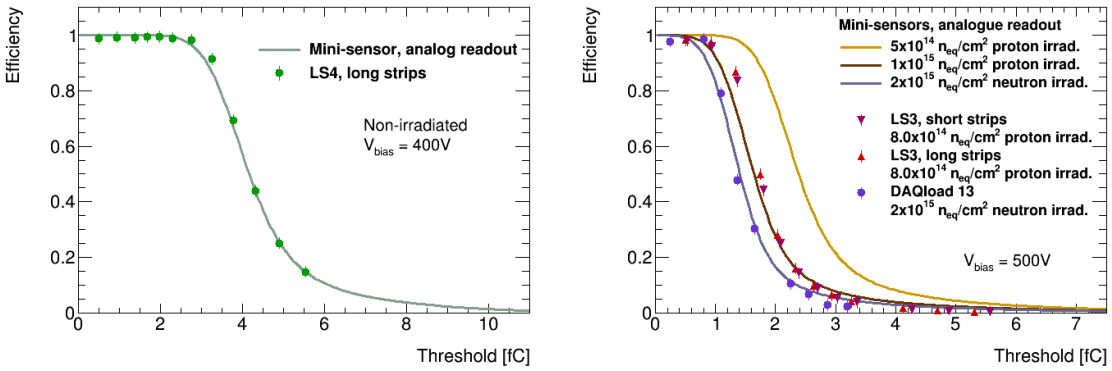


Figure 8.17: Comparison of the efficiency versus the threshold between test beam and source-based sensor studies. **Left:** Non-irradiated. **Right:** Irradiated.

Figure 8.18 shows the signal efficiency compared to the noise occupancy for modules (non-irradiated and irradiated) studied at the CERN test beam. As noted earlier, the combination of the lower substrate resistance of the ATLAS12 sensor and the lack of annealing after irradiation mean that the signal measured at test beam is lower than expected at the end-of-life with production grade sensors. The noise in the prototype chips ABC130 is larger than expected in the final design of the production chip ABCStar. Prior to irradiation a wide range of thresholds (0.5 - 2.0 fC) meet both the noise occupancy of better than 1×10^{-3} and hit

efficiency requirements of greater than 99%. With irradiation the range of thresholds which will simultaneously meet the efficiency and noise occupancy requirements is reduced. Even with all of these limitations discussed above there is still a narrow range of thresholds near 0.5 fC that will simultaneously meet both efficiency and noise requirements for LS3 with short and long strips at 500 V sensor bias. The range of threshold is widened with a sensor bias voltage of 600 V; this behaviour motivates the requirement on the HV system to be capable of delivering up to 700 V to increase the safety margin to operate efficiently at end-of-lifetime. For the long strips at 600V the signal-to-noise was calculated to be 10.9:1

In Figure 8.18 the noise occupancy data for the new front-end stage for the ABCStar (see Chapter 6) is added for comparison; the noise occupancy is extrapolated from the equivalent noise charge measurements. With the reduced noise in the production chip the range of thresholds which meet the specifications on noise occupancy and efficiency will be much wider.

8.5 Expected End-of-Lifetime Performance

At the end-of-lifetime, modules are required to have greater than 99% detection efficiency at thresholds that allow for operation with less than 1×10^{-3} channel noise occupancy. It has been shown that requiring a signal-to-noise ratio of 10:1 will simultaneously satisfy these efficiency and noise occupancy requirements. For this signal-to-noise ratio calculation, the signal is defined to be the sum over a number of strips using a cluster algorithm and analogue read-out electronics operating at HL-LHC speeds and the noise is the average single-channel noise. Previous sections in this chapter have shown the signal, the hit efficiency, noise and noise occupancy of the systems are well understood before and after irradiation, so the 10:1 requirements should effectively represent the efficiency and noise occupancy requirements. This was demonstrated for the long strips on LS3 which exhibited a working region satisfying both the hit efficiency and noise occupancy, and had a signal-to-noise of 10.9:1. The remainder of this section outlines the inputs required for the signal-to-noise estimate at the end-of-life of the module. The technique is valid for all module types. The expected signal after the highest expected fluences is determined using the charge collection efficiency studies from Section 6.1.2. A fit of the collected charge vs. neutron fluence is used as a conservative estimate of the expected signal. The measurements are made on neutron irradiated ATLAS07 miniature sensors. The expected signal for both the nominal (500 V) and maximal (700 V) bias voltages have been calculated.

The noise after irradiation is modelled as the sum of two components: the noise before irradiation and the shot noise expected at the end-of-lifetime. The two are added in quadrature. The noise before irradiation is estimated to be the same as that measured with the ABCStar front-end protoype, described in Section 6.2.2, scaled by the simulated increase in noise with sensors relative to the passive capacitor due to the sensor's strip resistance. This estimate assumes that the noise increase after irradiation seen in the prototype chip

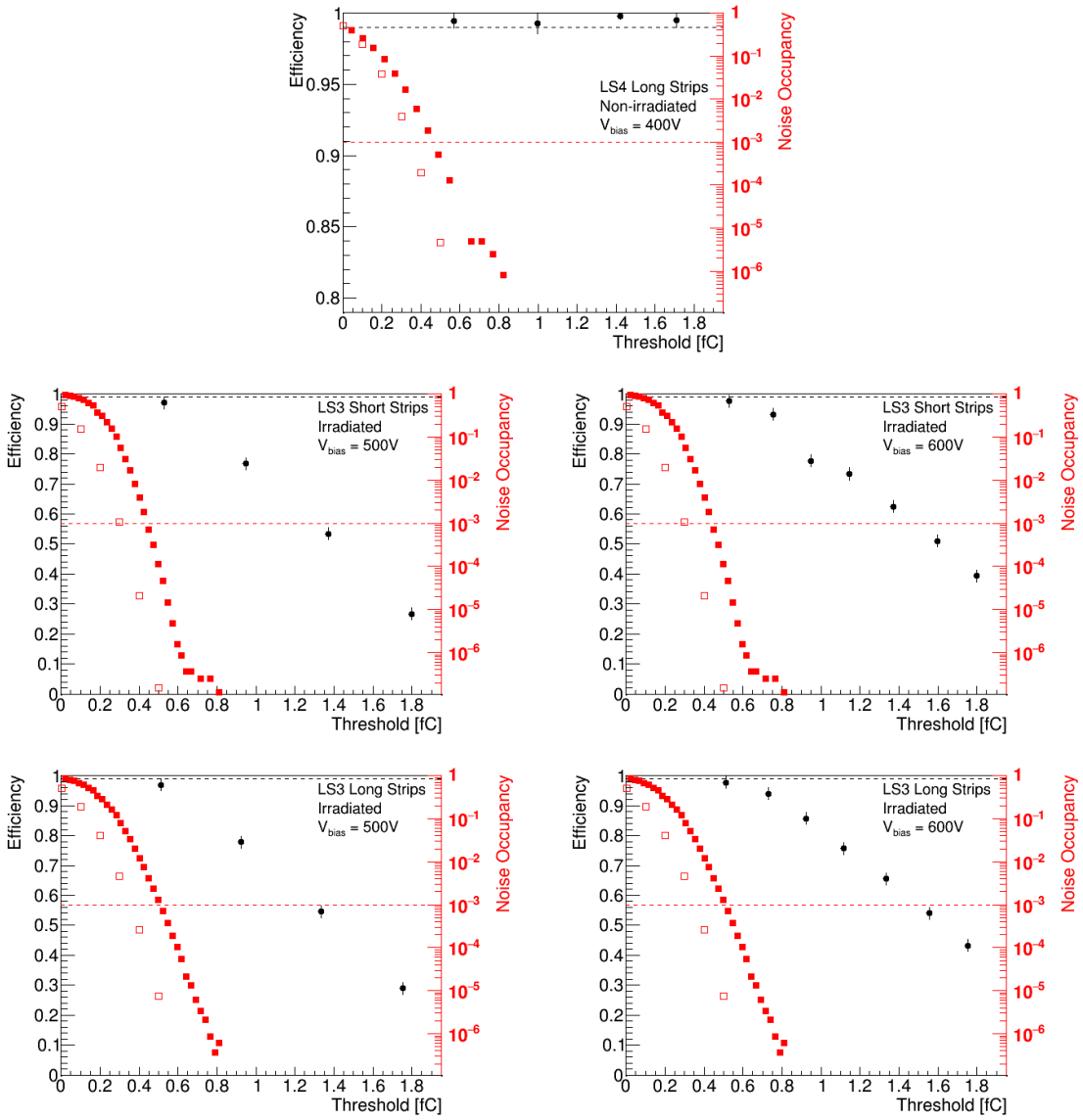


Figure 8.18: The signal efficiency (black dots) compared to the noise occupancy at different thresholds for the ABC130 (red squares) and the new front-end (open squares). The top plot shows the non-irradiated LS4 module, while the middle and bottom rows are for the short- and long-strip regions of the irradiated LS3 module and the new prototype front-end chip. The results are shown with a bias voltage of 400 V (top), 500 V (left), and 600 V (right). The combination of the lower substrate resistance of the ATLAS12 sensor and the lack of annealing after irradiation mean that the signal measured at test beam is lower than can be expected at the end-of-life with production grade sensors.

Table 8.2: Estimated signal-to-noise at the end-of-lifetime for all module types of the ITk Strip Detector. Maximal values of the Fluence include a safety factor of 1.5

Module Type	Fluence $10^{14}n_{eq}cm^{-2}$	Charge ke^- 500 V	Charge ke^- 700 V	Noise e^-	S/N 500 V	S/N 700 V
SS	8.1	13.7	16.1	630	21.8	25.6
LS	4.1	17.3	19.5	750	23.1	26.0
R0	12.3	11.5	14.0	650	17.7	21.5
R1	10.1	12.5	15.0	640	19.6	23.4
R2	8.7	13.3	15.7	660	20.3	23.9
R3	8.0	13.8	16.2	640	21.4	25.1
R4	6.8	14.6	17.0	800	18.4	21.3
R5	6.0	15.3	17.6	840	18.3	21.1

ABC130 will be eliminated in the production chip ABCStar through the use of enclosed layout transistors in the critical regions of the front-end. The shot noise is estimated using the measured increase in sensor leakage current with fluence [56], the predicted operating temperatures of the petals and staves (Section 9.4) and the simulations of the ABC130 and ABCStar's front-end pre-amplifier and shaper.

The resulting signal-to-noise estimates for the various modules types are summarised in Table 8.2. For the nominal 500 V bias operation, all modules meet the 10:1 signal-to-noise requirements, with end-cap modules R0, R4 and R5 having the lowest signal-to-noise. Increasing the bias voltage to 700 V results in an increase of the signal-to-noise of 15-20% compared to the 500 V case. This gives additional head room over the standard signal-to-noise requirement and that could useful at the end of life.

8.6 Comparison of ABC130 Results between various Testing Sites

An important metric for assembled modules is quantifying the reproducibility of test scans, as well as confidence that measurements can be compared between different testing institutes with variable test setups (power supplies, cabling, DAQ firmware etc). For this reason a DAQload was assembled using an end-cap hybrid, populated with an HCC130 and one ABC130 wire-bonded to an ATLAS12 mini-sensor (see Chapter 6.1). Of the 256 front-end channels of the ABC130, 104 were bonded to sensor strips, and the remaining 152 were left un-bonded, allowing for noise comparisons. The hybrid was mounted in a R0 test frame with a DC-DC bridge for direct powering of the hybrid. Held in a dark box (Figure 8.19), the DAQload was shipped and electrically tested between 14 international institutes. At

each site, threshold and noise scans were performed, as well as 100 three-point gain scans for increased statistics.

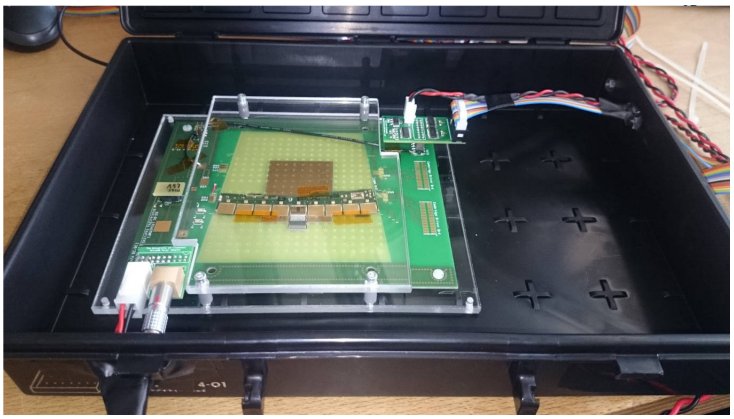


Figure 8.19: End-cap ABC130 DAQload in dark box.

Figure 8.20 shows the gain and noise for bonded channels for multiple testing institutes. It can be seen that the results are extremely similar between institutes, with small offsets caused by humidity and temperature variations (which were logged at time of testing).

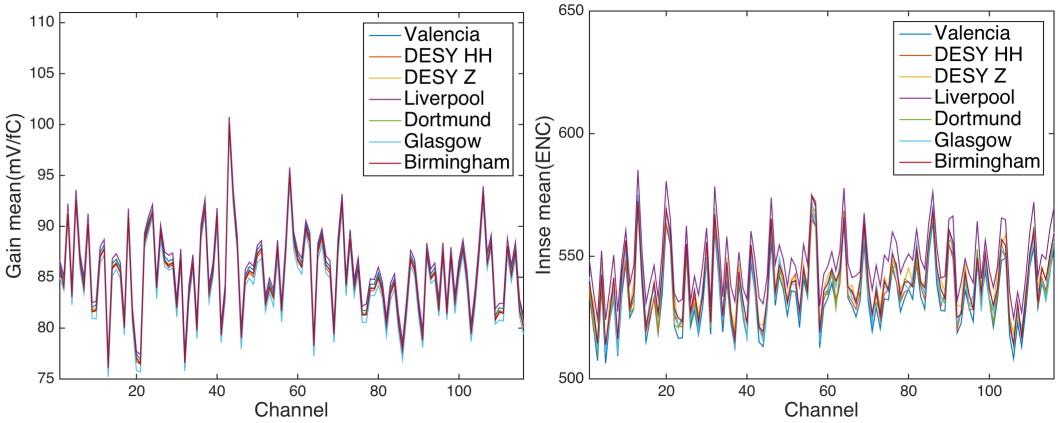


Figure 8.20: **Left**: Gain and **Right**: equivalent noise charge (e^- ENC) for the 104 bonded strips in the end-cap ABC130 DAQload, compared between different institutes.

9 Local Supports: Staves and Petals

In this chapter the engineering design of the stave cores (for the barrel) and petal cores (for the end-cap) is described. Stave cores and petal cores are simply different flavours, necessitated by geometrical considerations, of the same basic conceptual unit; a local support. Local supports combine the mechanical support with all the required services for a completely autonomous multi-module system. The barrel and end-cap sub-detector arrays are then formed of multiple copies of the same (or at least very similar) staves and petals mounted into the barrel and two end-cap global support systems.

The general performance requirements for staves and petals concern geometric stability, cooling performance and the supply of electrical connections to and from the modules and are therefore essentially identical. Similarly they share common interfaces; mechanical (to their respective global support structures), electro-optical (via an End-of-Substructure (EoS) card to the services interconnects) and their connections to the cooling system.

Given the similarities in the requirements and interfaces, the engineering designs of staves and petals are conceptually identical.

9.1 Requirements and Overview

The local support must encompass geometric, mechanical, electrical and thermal aspects in its design (see Table 5.1). The main functional requirements are: that it supplies all the services which modules need to function and transmit the data off the detector, that it is capable of maintaining the operating temperature of all modules within acceptable limits given the constraints imposed by the cooling system, and finally, that it ensures the position of each module is maintained within acceptable limits as defined by the ability to determine the module positions using track-based alignment procedures during data-taking. The mechanical and cooling performance of the local support is determined by employing high-stiffness, high thermal conductivity carbon-fibre for the face-sheets and the sandwich geometry, which gives high rigidity and allows the cooling structures to be buried within the core such that heat generated by the modules is removed directly.

Mechanically, local supports interface to their global support structures through a series of position locators and locking points, which together define the position of each local support. The electrical services needed to power and control modules are connected to the off-stave services via an end-of-substructure (EoS) card (see Section 12.1) and distributed to

each module along electrical connections on the surfaces of the local support core. Similarly, the EoS card receives the data from each module, processes it and then transmits it via optical links to the data acquisition systems. The embedded cooling loop is connected to the off-stave cooling services via orbital welding to eliminate the need for mechanical connections within the ITk volume.

The local support requirements can be summarised in three groups covering the operation of modules within ATLAS, the integration of the strip tracker, and the attachment and servicing of modules.

9.1.1 Requirements for the Operation of Modules in ATLAS

For the most part of their life-cycle, local supports will be in operation within the ATLAS experiment. During this period, local supports will play a critical role in ensuring the proper functioning of the ATLAS strip tracker. Local supports must be compatible with the environmental conditions within the tracker volume and maintain the positions of modules with sufficient stability to enable track-based alignment procedures to converge. The required electrical power and control signals for module operation need to be distributed and the data must be gathered and condensed before being transferred off. Finally, the heat generated by the modules must be absorbed into the CO_2 cooling system whilst maintaining a safe module operating temperature.

Operating Environment

The thermal conditions within the ITk are dictated by the evaporation temperature of the CO_2 cooling system. During detector shut-down, local supports will reach stable equilibrium with the environmental temperature within the ITk volume. Initially, this might be as warm as 20°C but, as the sensors become more radiation damaged, a lower temperature will be used. During operation it is envisaged that the CO_2 evaporation temperature at the exit of the local support will be -35°C. However, in certain fault conditions it is possible for the temperature to plummet to -55°C (worst case scenario).

Humidity within the ITk volume will be regulated by flushing it with dry N_2 gas at a rate required to keep the dew point safely below the minimum possible CO_2 evaporation temperature in any operational scenario, including system faults and catastrophic leaks. Assuming the minimum CO_2 temperature is -55°C, a dew point temperature of -60°C is a reasonable requirement. The materials used to construct local supports are to some extent hygroscopic. Assembly will take place in an environment where the relative humidity is in the region of 50%, where as operation will happen in a dry nitrogen atmosphere. Immediately after the ITk is sealed and the dry nitrogen gas flow is started, the hygroscopic structural materials (polymers, resins & adhesives) will begin to lose moisture by diffusion

towards surfaces in contact with the N_2 gas. Thus, dimensional changes may occur as a result of the materials having a non-zero coefficient of moisture expansion (CME).

Operational Stability

The requirements for geometric stability come from the limits on deviations for track-based alignment algorithms to be able to track potential displacements. The global stability requirements are summarised in Ref. [80]. In the measurement direction $R\phi$, the requirement is for displacements to be less than 2 μm over timescales of one day and 5 μm over one month. The stability requirements in less sensitive directions are ten times less stringent.

These stability requirements are global numbers and as yet there is no agreed sharing between the requirements for the local and global support. Geometric instability may result from environmental changes (temperature, moisture desorption or radiation damage), or mechanical deformation (gravitational sag, external loads, vibration or material effects).

When mounted on its support structure, the geometric position of a local support can be affected by gravity, dynamic inputs from vibration sources or transients, and material effects as well as deformations of the global support. Gravitational effects induce a static deformation and there is a requirement that any such deformation must be less than the amount which would cause gaps in hit-coverage to open up.

There are two types of dynamic instability which need to be considered: transient phenomena and vibration. Transient phenomena, such as movements in the external services, pressure cycling of the CO_2 in the cooling tubes, and thermal cycling can cause changes in the load conditions on an local support and can therefore lead to significant changes in position. It is envisaged that such thermal cycles will be relatively rare and the intervals between such transients will be considered as forming a block of data with each unique block having its own alignment constants derived from the data.

Power and Data Transmission

The electrical power, control signals, and data transfer services required by the modules are carried by a copper/polyimide "bus-tape" mounted on both faces of the local support sandwich. The design of the copper track-work is constrained by the need to achieve the correct operating voltages for the front-end ASICs, to allow the transmission of signals to and from the modules with high reliability, and to respect the geometrical constraints necessary for the up to 700 V sensor back-plane bias connections.

The low-voltage power will be brought to the modules at 10 V and DC-DC converters will be used to generate the required 3.3 V and 1.5 V for each module (see Section 5.5). The current drawn will vary during the operation, therefore the requirements are specified in terms of the worst case current (see Table 9.1). In order not to compromise the data

Table 9.1: Stave and petal bus-tape power requirements. The estimate of the maximum current required is based on our current understanding of the Total Ionising Dose (TID) induced current increase.

Supply	Minimum voltage (V)	Maximum voltage (V)	Maximum current (A)
Stave			
Low voltage	10	11	8.2
High voltage	-	750	0.1
Petal			
Low voltage	10	11	3.6
High voltage	-	750	0.07

transmission, the voltage drop along the low-voltage return line will be limited to 200 mV. The voltage drop along the positive low-voltage line should be less than 800 mV to ensure that the last module on the stave or petal is correctly powered. The widths of the power lines have been adjusted to satisfy these requirements for the worst case currents.

The high voltage requirements are based on an assumed maximum sensor high-voltage of 700 V, but this will require 750 V on the bus-tape to allow for the voltage drop in the bias resistor. The High Voltage Insulation Resistance (HVIR) for both HV lines to neighbouring lines should be greater than 1 GΩ. This should be tested at twice the voltage planned for normal operation.

The Timing, Trigger and Control (TTC) data are sent from the EoS to the HCC130 ASICS using multi-drop lines. The maximum data rate required is 160 Mbit/s. In order to satisfy the requirement for full read-out of the detector at an L1 trigger rate of 1 MHz, the module data is transferred from the HCCs to the EoS at a rate of 640 Mbit/s. The data links are all point-to-point. The barrel staves (end-cap petals) require 28 (14) such data links. In addition slow control (monitoring data) is sent to (from) the AMAC chip using I^2C communication at a maximum rate of 400 kHz.

Thermal Performance

Thermal runaway will occur if the sensor-generated heat is not balanced by its removal by the coolant. Stable operation depends on a combination of the coolant temperature, thermal path resistance and sensor power (which grows with radiation damage).

Detailed finite element analysis (FEA) models of the local support have been developed to predict temperature distributions and safety margins (headroom), given the power consumption of modules and EoS as given in Chapter 5. Table 9.2 summarises these numbers as thermal requirements for the local supports. This table already assumes maximal power consumption at TID induced current peak (see Chapter 6), where it estimated the digital

circuitry to consume 1.5/1.7 times more current than before irradiation for stave/petal respectively.

Table 9.2: Local support thermal requirements.

	Stave	**Petal**	**Comment**
Max. module power	10 W	12 W	For module R3
EoS power	12 W	6 W	
Local suport total power	300 W	130 W	

9.1.2 Requirements for the Integration of the Strip Tracker

During integration, local supports are inserted into the global support structures, where they are located on their position reference features and locked in place. Following insertion, the connections from the local support to the cooling system, electrical power and optical data transmission systems will be made. The local support design must allow for the varying load conditions during the process of local support insertion whilst obeying all the geometric clearances and positional tolerances required.

Local Support Flatness

Local supports will be positioned in the global support structures via a number of position locations and locking points. Local supports need to be flat enough to allow proper engagement of all mechanical interfaces without putting too much stress on the fixation points on the global support and the local support.

Local Support Envelope During Insertion

During local support insertion, its envelope needs to be such that there is no risk to the local support being installed nor those already mounted. This places limitations on the heights of components and the trajectory of the local support during insertion.

9.1.3 Requirements for the Mounting of Modules

Following the construction of a local support core, modules will be adhesively attached to the two faces and electrical connections between the read-out hybrids and the bus-tape will be made via wire-bonding.

It is assumed that during this phase, the local support is retained in an assembly frame, which references the position of the locking points. The locking points mimic those employed on the global support structures. Modules are then positioned in the plane of the local support with reference to the nominal position of the global support structure locators. The out-of-plane position of the modules is not governed by this coordinate system and is therefore a free parameter.

Co-cured Bus Tape Geometry

The precise geometry of the bus-tape is defined during the co-curing[1)] of the tape to the carbon-fibre reinforced polymer (CFRP) pre-impregnated with the resin ("prepreg"). With the prepreg systems being used, the cure temperature is about 120°C. Typically the bus-tape expands during heating until the temperature at which the prepreg starts to cure is reached. Experience from prototyping indicates that the bus-tape for the stave expands by 0.5 mm along its length due to co-curing. The cumulative positional shift of wire-bond fields must be small enough to allow the wire-bonding of any module. The design of the hybrid and bus-tape wire-bonding fields is such that wire-bonding is possible up to relative shifts of 0.3 mm. Provided the part-to-part variation in the expansion is small, then a correction to the bus-tape art-work can be made to minimise the overall expansion and optimise the co-cured tape geometry for wire-bonding.

Local Support Surface Geometry

The local support design and assembly processes have been developed with the intention of producing cores which are smooth (have minimal surface roughness) and flat (have minimal large-scale departures from a plane).

Modules will be positioned relative to the local support using a system with precision optical metrology and a set of vacuum pick-up tools. The pick-up tools incorporate adjustment mechanisms which allow the in-plane position of a module to be adjusted to bring it into the correct location relative to the local support coordinate system. The modules are attached to the support via an adhesive layer. This layer has to guarantee the positional stability of modules for the lifetime of the tracker and to conduct the heat generated in the module through to the face-sheet. With respect to the latter, both the area of contact and the thickness affect the efficiency of heat transfer. In terms of thermal performance, the area of the layer should be maximised while the thickness should be minimal.

[1] The process of curing a composite laminate and simultaneously bonding it to some other material

9.1.4 Local Support Requirements Summary

Table 9.3 with quantitative mechanical requirements. Some of those values will be explained in the text appearing later in this chapter.

Table 9.3: Local support mechanical requirements summary. Only quantitative requirements are listed. For related requirements see text (e.g. bending stiffness with respect to insertion tightness and insertion model).

Requirement	**Stave**	**Petal**	**Comment**
Module Placement Accuracy, with respect to local coordinate system			
R·φ	<50 μm		max. absolute deviation
z	<50 μm		max. absolute deviation
Module glue thickness	<150 μm		
Out-of-plane Sag	<1 mm	-	To prevent collision
Overlapp R·φ / φ	0.9 mm	1.5 mrad	~12 strips
Surface flatness	<100 μm		In a 10x10 cm^2 region

9.2 Details of the Design

In this section, the details of the engineering design of both barrel staves and end-cap petals (see Figure 5.2) is presented. Using the common set of requirements, system-level architecture and materials leads to a single conceptual design for both barrel and end-cap local supports from which the two geometrically different implementations are derived.

9.2.1 Local Support Cores

All local supports are formed from two face-sheets, which sandwich a core that is made from cooling components and low-density carbon-fibre honeycomb. The core is sealed by close-outs with the addition of ancillary components which allow mechanical mounting on the corresponding global support.

Figure 9.1 shows a cross section of the internal structure of the stave core as an example, identifying the face-sheets, cooling structure and low-density carbon-fibre honeycomb, as well as the bus-tapes and modules on the outside of the structure. Close-outs and ancillary components are specific to the type of local support and will be explained in the corresponding subsections.

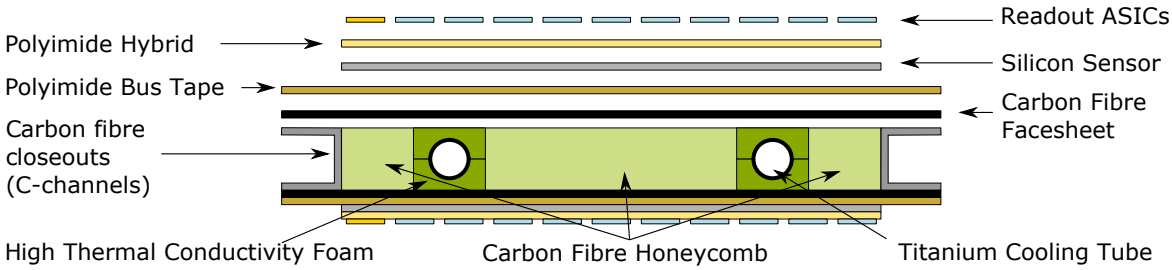


Figure 9.1: Schematic of the internal structure of the stave core, with the silicon sensors and ASICs added. Glue layers are not shown. Not to scale.

Face-Sheets

Face-sheets are formed from layers of high-modulus unidirectional carbon-fibre material with pre-impregnated radiation tolerant and low-CME cyanate ester resins (prepreg) together with a copper/polyimide bus-tape. The carbon-fibre material properties are dictated by the overall stiffness requirements for the local support and the thermal requirements for supporting the conduction of heat generated in the modules to the cooling structures embedded in the core. The copper/polyimide bus-tapes are laminated together with three layers of K13C2U/EX1515 (45 gsm, 40% resin content) prepreg in a [0,90,0] lay-up (where "0 degrees" is along the stave/petal centre axis) in an autoclave at high pressure and temperature (7 bar, 120°C). Due to the high coefficient for thermal expansion (CTE) of the bus-tape relative to the carbon-fibre, co-curing at high temperature stretches the tape and induces stresses in the final face-sheet at temperatures below the cure temperature. These stresses can lead to curved face-sheets which can cause problems during local support core assembly. The degree to which the co-cured face-sheet deforms is reduced by performing the co-cure on a custom designed curved tool which produces a curved face-sheet at 120°C which then becomes flat at room temperature.

Cooling Structure

As local supports have all their service connections at one end (staves at z ~1.4 m, petals at R ~1 m), the cooling tubes pass along the full length of the local support and return via a U-bend (either close to $z = 0$ m or $R \approx 0.4$ m). Using both the flow and return arms maximises the area available for heat transfer into the fluid and hence the tubes are located at a symmetric distance around the centre-line of the local support such that heat flow from the module is divided into four sections of equal length and heat flux. In order to ensure that the structure is balanced with respect to thermally induced stresses, the cooling tubes are located in the mid-plane of the local support. The interface between the tube and the face-sheet is formed using a thermally conducting carbon-foam (Allcomp K9, 130 ppi[2)],

[2] pores per square inch

$\rho = 0.23\ \mathrm{g\,cm^{-3}}$, $K \approx 30\ \mathrm{W/mK}$). The glue joints are made using an adhesive[3)] loaded with thermally conducting carbon particulates. To ensure electrical isolation between the structure and the external cooling services, the cooling loop incorporates two ceramic insulating breaks which are located close to the connectors inside or outside the core at the connection end. The example of a stave is given in Figure 9.2.

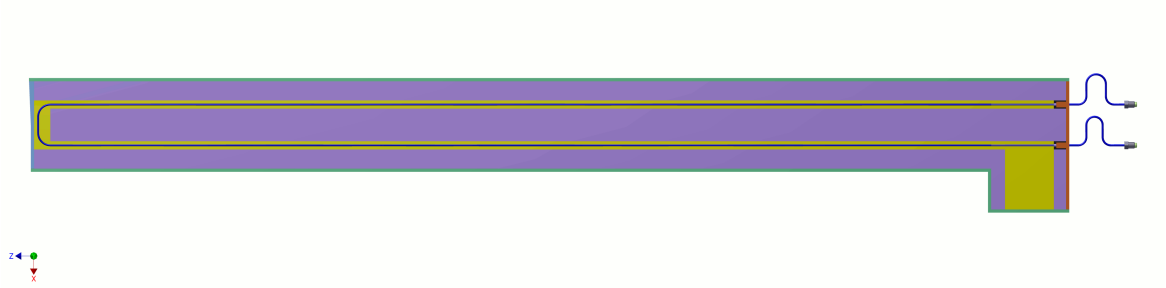


Figure 9.2: A stave core as seen from the top side. Violet colour indicates carbon-fibre honeycomb material and yellow indicates carbon-foam used in the assembly.

Cooling loops are manufactured from three basic components: the internal cooling loop and two composite inlet/outlet sub-assemblies. The joints between the three parts are all made through orbital welding. The inlet and outlet sub-assemblies each comprise a short section of the internal cooling tube, an insulating break and an interface tube of 2.5 mm outer diameter and wall thickness of 0.2 mm. The interface tubes follow the routing required after insertion into the global support structures but are extended by a few cm, as shown in Figure 9.2. The extension is terminated in a connector[4)] for all subsequent testing. Following the local support acceptance test, the extension piece is cut off and the end of the tube cleaned up ready for service connections after integration into the global support structure.

Low-density Core Material

Apart from the cooling structures and the close-outs, the remainder of the central portion of the local support core is filled with a low-density honeycomb core material which is glued to the two face-sheets using a conducting glue. The honeycomb maintains the separation of the face-sheets for good bending stiffness and ensures the support has a sufficiently flat and robust surface to allow adhesive attachment of the modules without the need for excessively thick glue layers. Although the choice of honeycomb material is not critical, a high-performance carbon-fibre based honeycomb with a cell size of about 6.4 mm has been selected.

[3] Hysol EA9396
[4] Swagelok VCR

9.2.2 Stave Specifics

Close-outs

The stave edges are enclosed by end and side close-outs. End close-outs, made of engineering plastics, are used to mitigate against possible de-lamination of the core during handling in general and, in particular, against the effects of extraneous forces applied to the cooling tubes. Meanwhile, pultruded carbon-fibre C-shaped channel (C-channel) close-outs are used for the long edges of the core. The side close-outs are important in mitigating against the peel forces generated by the co-cured face-sheets when the stave is cooled, form part of the mechanical interface to the global support structures and function as guide rails during stave insertion and support points during module mounting, increasing the stiffness to reduce bowing. The C-channel, into which the stave locking points are glued, has apertures cut into the vertical wall to allow the mounting bracket sockets to be installed during stave core assembly.

Stave Locators and Locking Points

Staves are attached to the support cylinders via a minimal set of precision location features and a number of locking points (Figure 9.3). The position of a stave core on its support cylinder is defined in $R\varphi$, R and z at the $z = 0$ m end through a ball-and-cone arrangement. A restraint is provided in z by a fastener which is secured using a long rod immediately after stave insertion. The angle of the stave relative to the radial direction is defined at $z = 0$ m via a precision hole in a plastic (PEEK[5)] or LCP[6)]) locator glued into the free-edge of the stave core. The stave core slides over a tapered pin located in a bracket which is glued to the support cylinder. At $z = 1.4$ m, the free edge of the stave is located close to the EoS card to mitigate against any possible deformation of the stave as a result of stresses caused by movements of the services. Finally, the stave is held along the edge closer to the support cylinder in $R\varphi$ and R through five locking points. These bind the stave to the support cylinder and exploit the stiffness of the cylinder in maintaining the stave in a stable position. The locking points are formed from a bracket, which is mounted into the stave core, and a housing which is mounted onto the support cylinder.

The position of the stave is defined by the V-shaped features in the locking point. Bracket and housing are brought together through a side-ways force generated by rotation of a cam mechanism using a long circular rod terminated in a hexagonal shaft. The rod is inserted from the $z = 1.4$ m end and passes through the hexagonal holes in the five locking points. The rod is then withdrawn until the hexagonal rod sits in the corresponding hole in the cam mechanism and rotated to activate the cam. The rod is then pulled back a little further to actuate the next cam and so on.

[5] PolyEther Ether Ketone
[6] Liquid Crystal Polymer

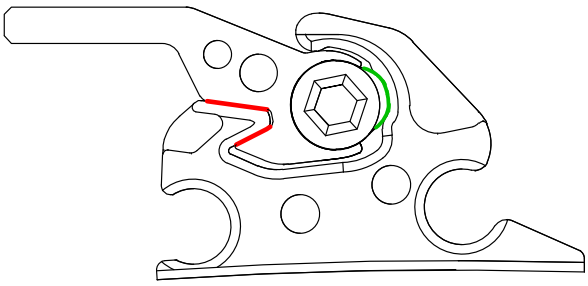


Figure 9.3: Cut view of a Stave locking point, showing both the stave-side component (towards top left) as well as the cylinder mounted bracket (bottom part) and indicating their mating precision faces (red) and the tensioning cam face (green).

9.2.3 Petal Core Design

The petal core is the equivalent to the barrel stave core. It uses mostly the same materials as stave cores. Here, the main differences are outlined.

The petal core is wedge-shaped with the routing of the cooling tube approximately V-shaped as shown in Figure 9.4. Each module in the outer three rings is cooled by a single length of tube, while the inner three modules – which have higher power densities – are cooled by two lengths of tube, similar to a stave. The cooling parameters are quite different between staves and petals. A petal has fewer modules than a stave (18 versus 28) and of these, ten have a single hybrid. This reduces the power load and servicing needs compared to a stave. Furthermore the wide-end of a petal is much wider than a stave. The outer modules have lower power density than short-strip barrel modules, but since there is only one tube-section for cooling, the heat path-length is roughly doubled. A maximum separation of ~110 mm between the input flow and return arms of the cooling pipes is reached at the second highest module row (R4). The innermost modules have higher power-density than the short-strip barrel-modules, but have two lengths of cooling pipe giving more area and shorter heat-path. There is also one EoS per side, connected to the bus-tapes.

The locking mechanism and locators for the petals are different from the stave ones. In this case, the petal locators are at the top and bottom closeouts (on the short edges of the petal), as shown in Figure 9.5. The locators are constructed from thermoplastic material (PEEK, Torlon, or LCP), with precision holes and slots at $R \sim 375$ mm and $R \sim 968$ mm, glued onto the petal core closeouts. They come in three different flavours: a 4 mm diameter hole at $R \sim 375$ mm, and a 4 mm diameter slot and a 6 mm diameter hole at $R \sim 968$ mm. They constrain the movement of the petal in XYZ, $z\phi$, and z, respectively. The kinematic mount of the petal locators and the locking points on the global disk structure are described in Chapter 10.4.

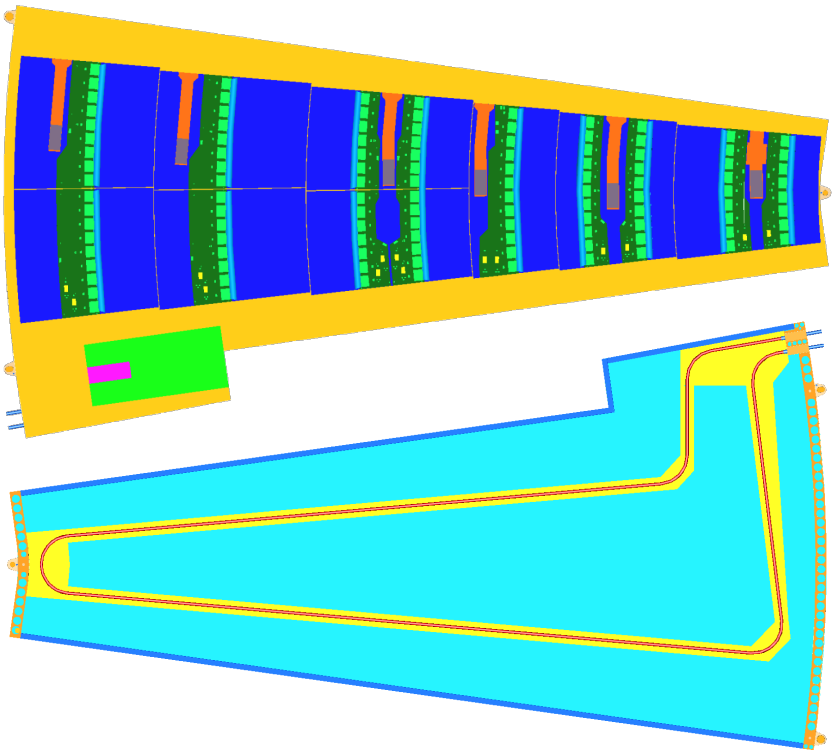


Figure 9.4: Schematic view of a petal. (Top) Full petal sketch showing petal core and silicon modules. The blue sensors are glued directly on the co-cured facing, here indicated in light brown. (Bottom) Internal structure of a petal core showing the cooling pipe routing. The red lines indicate the titanium pipe; the yellow region shows the carbon-foam enclosing the pipes. The light blue area is filled with the honeycomb filling material.

9.2.4 Estimated Radiation Length

Table 9.4 shows estimates for the radiation length of a single short-strip barrel stave as well as for a petal. These numbers represent best estimates based upon stave and petal prototyping and extrapolation to the use of expected lower-mass components (e.g. ABC130 hybrids and titanium cooling pipes). For comparison, the current SCT radiation length excluding barrel or disk support is 2.48% for the barrels and 3.28% for the end-caps [86]. The lower expected radiation lengths can be achieved as a result of the high degree of sharing of support, power and services in the upgrade designs.

9.3 Electrical Concept

In this section, the details of the system-level components common to both stave and petal local supports are described. The detailed designs of these components differ only through

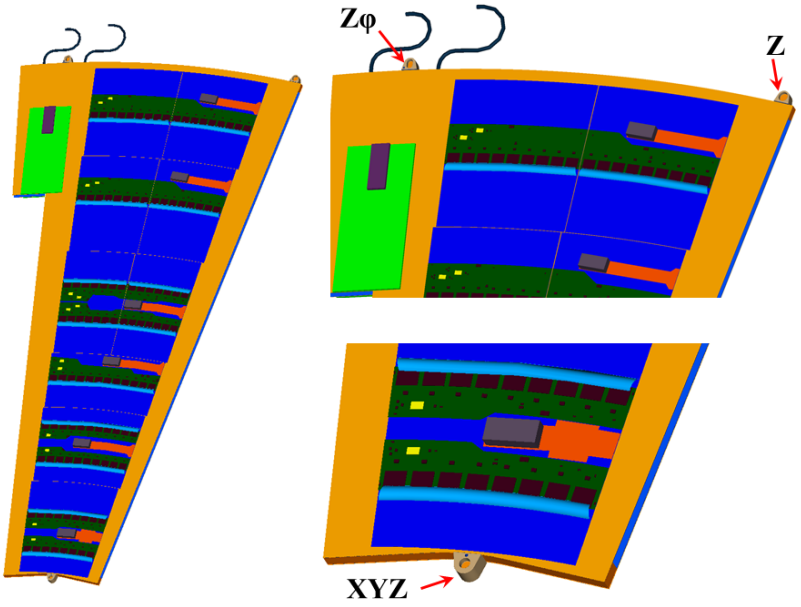


Figure 9.5: CAD sketch of a petal showing the petal locators.

Table 9.4: Radiation length estimates for the barrel stave and end-cap petal. Power ASICs and the EoS are not included. These numbers need to be confirmed with full stave and petal designs.

Barrel		**End-Cap**	
Component	% Radiation Length	Component	% Radiation Length
Stave Core	0.48	Petal Core	0.46
Bus Cable	0.18	Bus cables	0.23
Short-Strip Modules	1.08	Modules	1.04
Module Adhesive	0.06	Module adhesive	0.05
Total	1.80	Total	1.78

geometric necessity when applied to staves and petals. The general electronics concept has already been outlined in Section 5.4. Details of the optical read-out will be given later in Chapter 12.

9.3.1 Bus-tape

The bus-tapes provide to the modules all the low-voltage and high-voltage power from an EoS card at the end of the stave or petal. The bus-tape also provides all the high-speed data links between the modules and the EoS, as well as I^2C communication between the EoS and the AMAC chips on the power boards. The modules are glued directly onto the bus-tapes.

Tape Design

Identical technologies will be used for the barrel stave and petal bus-tapes and the differences between the two types of bus-tapes will only be those dictated by the different geometry.

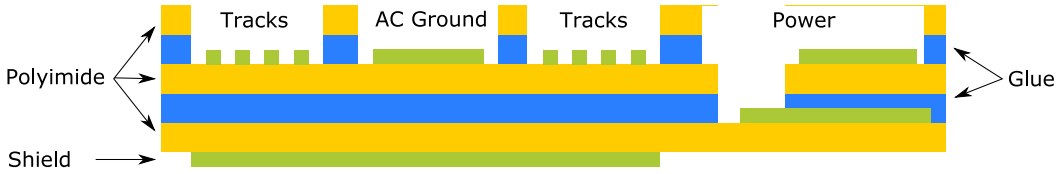
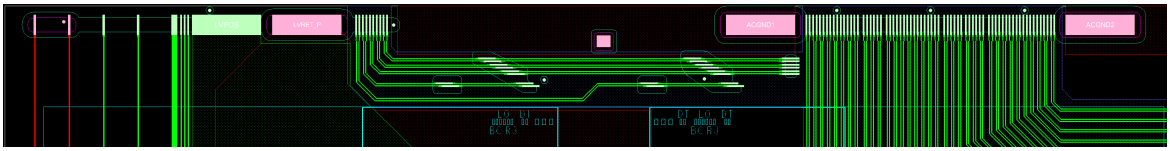


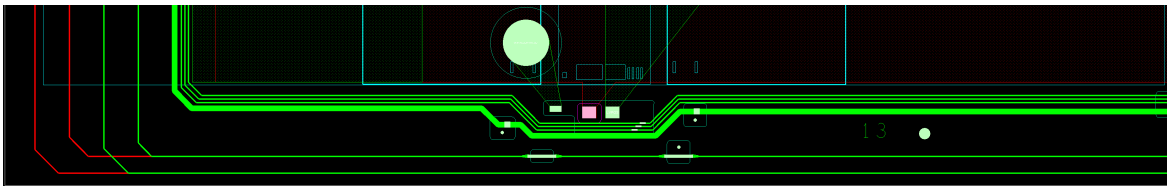
Figure 9.6: Sketch (not to scale) to illustrate the stackup of the bus-tape, showing the three copper layers (green), three polyimide layers (yellow) and the glue sheets holding them together (blue).

The bus-tapes are laminated from two layers of adhesiveless copper/polyimide, see the stackup in Figure 9.6. The tapes are designed to have very high reliability and minimum material. Therefore they use adhesiveless copper/polyimide tapes and all connections to the modules and the EoS are made using standard aluminium wire bonding. The copper thickness used is 17 μm and the polyimide and glue layers are both 25 μm thick. Openings are cut out around pads to allow standard nickel-gold plating for the exposed pads (but not the full length of the tracks). The separation between exposed HV pads and neighbouring pads is greater than 2.5 mm (0.8 mm if the tracks are underneath a cover layer). This satisfies the IPC specifications [87] for 500 V. If operation at a higher voltage is required, the safety of the design will be validated by HVIR testing at twice the required voltage.

As the same copper layer is used for high-speed tracks and for power, the minimum thickness was selected in order to meet the voltage drop requirements without exceeding the available width. The voltage drop requirements for the low-voltage return for the stave bus-tapes is satisfied by the use of a wide trace. In order for the I^2C communication to work, the voltage drop on the return lines should be less than 200 mV. To allow efficient



(a) EOS region and data connection to the first module



(b) Module power connection area

Figure 9.7: Details of the different bonding areas on the bus-tape.

operation of the DC-DC converters, the round-trip voltage drop for the low-voltages line on the bus-tape should be less than 1 V. The width of these lines will be adjusted to meet these requirements.

The critical issue in the tape design is to provide good-quality data transmission over the full 1.4 m length of the tape, without adding too much material. A differential micro-strip configuration was selected for these lines. A standard design would use wide tracks to lower the resistive loss and a thick polyimide layer to ensure the required 100 Ω differential impedance of the lines. There is insufficient space for wide lines, and the use of thin layers of polyimide is required to minimise the material and the thermal impedance. The widths of the tracks is set to 100 μm and the gap between the two lines of each differential pair is also set to 100 μm. In order to minimise cross-talk, the gap between neighbouring pairs is set to 250 μm. These dimensions are close to the largest that are compatible with the stave width.

In order to achieve acceptable resistive losses without adding any extra polyimide layers, the stack-up shown in Figure 9.6 will be used.

The layout of a *prototype* bus-tape for a 13-module[7)] stave is illustrated with two images of the design: Figure 9.7(a) is for the EoS region showing the bond pads to connect from the tape to the EoS, as well as the data bond pads for the first module, and Figure 9.7(b) shows a region at the end of a module and the bond pads for the power connections.

The bottom copper layer will be in good contact with the carbon-fibre skin. Copper strips will be used in the EoS region to allow the carbon-fibre to be connected to the low-voltage return, thus allowing the copper strip to act as the ground for the high-speed transmission lines. There will also be data and clock lines for the I^2C communication between the EoS

[7] The prototypes for the bus-tapes were based on a previous layout of the ITk with only 13 modules per stave side

and the AMAC chips. All the high-speed signals use differential pairs above a ground plane. The slow speed I^2C (speed < 1 MHz) use single-ended signals.

9.3.2 Grounding and Screening

The ground reference for the local supports is defined by the first and common electrical interface, which is the EoS.

Within the bus-tape, the lowest copper layer in the stack acts as the ground layer for the data transmission lines. To satisfy the overall grounding and screening requirement and have all conducting surfaces grounded, the carbon-fibre skins of the local support, including the EoS region, will be put in contact with copper layers carrying the local ground into the stave. All of these contacts are co-cured, which should provide a good contact over the large copper area.

Module ground will be transported in two ways: a DC connection with significant currents will be given by the low voltage return on the bus-tape. In addition a clean AC-ground will be available for wire bonding to the module in case it is required to minimise the noise in the ABCStar ASICs.

9.3.3 Slow Control

Slow Control will be implemented through at least three digital I/O signals running as a bus to all modules on the local support. In terms of logical cable units, per EoS, there will be one LV and one HV cable, as well as the high-speed fibre link plus the external detector control system (DCS) information.

Two NTCs on the outlet pipe of every stave and petal will provide direct measurement of the stave temperature. Being wired individually, these are used to define a hardware fail-safe interlock so as to ensure that the cooling is operational before any power can be applied.

Much more granular DCS data will be read out from each module HCC130. The HCC130 will merge DCS data with the physics data. This will allow the reading of voltages, currents and one NTC per hybrid.

9.4 Thermal Finite Element Analysis

Detailed three dimensional thermal Finite Element Analysis (FEA) models have been developed [88] that predict the temperature distributions across the sensor, read-out chips and local support structures. These address major concerns during normal operation such as thermal runaway headroom (see Section 9.1.1 above), sensor leakage current (hence

shot noise) and cooling requirements, that depend in turn on radiation damage to both the sensor and read-out chips. They also allow temperature estimates outside normal operation, for instance during "beam off" conditions and initial detector commissioning at elevated temperature. The models concentrate on evaluating the conductive thermal paths to the cooling pipes and heat removal by the evaporating CO_2. Ambient heat exchange (by convection and radiation) has been considered, but in most situations is a negligibly small effect. The FEA predictions will be verified by comparison with stave and petal "thermo-mechanical" structures currently under construction.

FEA models of the barrel stave and end-cap petal differ mainly due to their geometry and read-out chip arrangements (Figure 9.8).

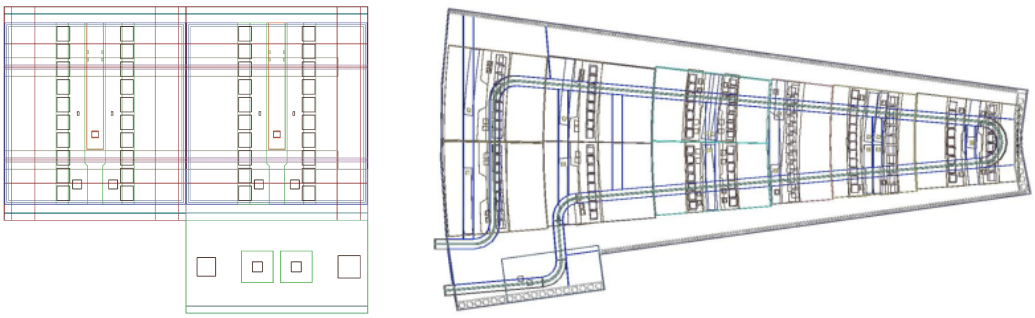


Figure 9.8: Top view of the FEA simulation models: The stave behaviour is very uniform along its length and can therefore be estimated using just two modules, one along the stave length, and a second one being the module closest to the EoS region, estimated to be the worst-case scenario (simulation model on the left). However, the petal is a non-uniform structure and needs to be fully simulated.

Since the stave has a predominantly periodic structure, it is sufficient to model a short segment at its end, where there is a coincidence of the slightly higher radiation level, the thermal load from the EoS chips and reduced cooling efficiency (due to the insulating break). Separate models are required for the inner radius (short strip) and outer radius (long strip) barrels. By contrast, the end-cap petal spans the radial extent of the strip tracker with an irregular module geometry. Hence the FEA model is constructed to describe the full petal. All petals are of the same design, and the FEA is usually run for conditions expected at the end of the tracker, where the predicted radiation level is highest.

Thermal Conductivities

Thermal properties used as input to the FEA are summarised in Table 9.5. Apart from minor variations, they are the same for the stave and the petal, in particular along the conduction path between sensor and coolant. Evaporative CO_2 cooling is simulated as a convective film between the pipe wall and fluid, at its evaporation temperature. The convective heat

transfer coefficient (htc) varies around the cooling loop and is computed using the stand-alone package CoBra [89], for the appropriate stave or petal thermal loads. The cooling pipe inner diameter is currently assumed to be 2 mm, although calculations are in hand to optimise this.

Table 9.5: Thermal properties used as input to the FEA.

Part or Interface	**Material**	$K_x/K_y/K_z$ **[W/(m×K)]**	**Thickness [mm]**	**Comment**
ASIC	Silicon	191 (250K) - 148 (300K)	0.30	
ABC130 to Hybrid	UV cure glue	0.5	0.08	50% coverage
HCC130 to Hybrid	UV cure glue or silver epoxy	0.5 or 3.0	0.08	75% coverage
Hybrid PCB	Cu/polyimide	72/ 0.23 (0.54)* / 72	0.2	*in via region
Power PCB	Cu/polyimide	see text	0.3	
PCB to sensor	FH5313 Epolite	0.23	0.12	75% coverage
Sensor	Silicon	191(250K) - 148(300K)	0.3	
Sensor to Bus	DC SE4445	2.0	0.1 - 0.2	100% coverage
Bus tape	Polyimide/ Cu/Al	0.17 / 0.24 / 0.17	0.17	
Bus to facing	-	(idealised)	-	co-cured
CFRP Facing	0-90-0 CFRP	90 / 1/ 180	0.15	K13C2U fibre, 45 g/m^2
Facing to Foam	Hysol 9396 + graphite powder	1.0	0.1	
Graphite Foam	Allcomp, 2g.cm-3	30	5 mm (core)	
Foam to Pipe	Hysol 9396 + graphite powder	1.0	0.1	
Cooling Pipe	Titanium (grade 2)	16.4	0.14-0.15 (wall)	2 mm inner dia.
Fluid film	Bi-phase CO_2	htc 4.5 - 17 [kW/m^{2}K]		

Conductivity values for the foam and co-cured facing have been measured by ATLAS institutes and are so far consistent with manufacturers' specifications. Thermal conductance through the various layers, of which the most crucial is the interface between the graphitised foam and cooling pipe, have also been measured. Where thermal performance is sensitive to these individual conductivities, components will be monitored as part of the

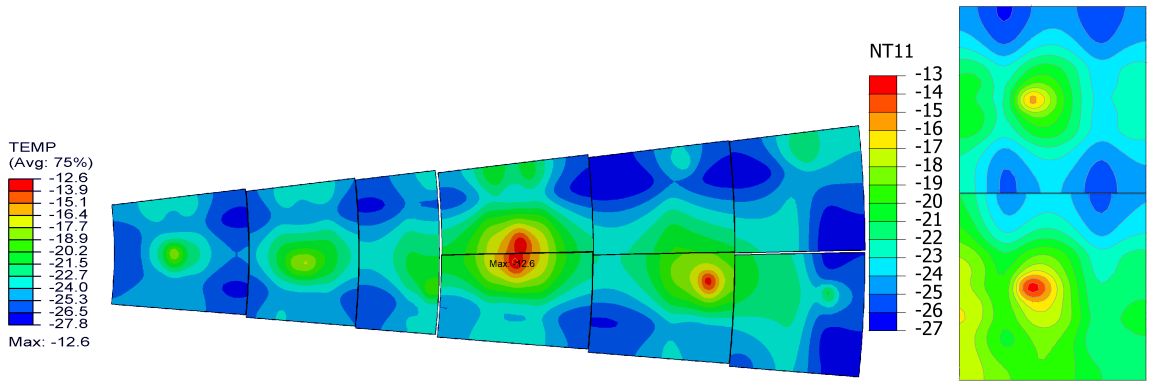
QC process. Read-out chip temperatures depend on the thermal path through the printed circuit boards. In particular, the DC-DC converter (that steps down the input voltage to power the ABC130 and HCC130 chips) is a localised source of power dissipation that is particularly important at the TID peak. Care is being taken to model the structure of the PCB (and compare with measurements) so as to correctly predict the DC-DC chip temperature. Certain material and design variants are under study and their effect is simulated in the FEA models; these include a possible reduction of the glue area between sensor and bus-tape in order to reduce its mass.

Thermal Loads - Performance at the TID induced Current Peak

Thermal loads are simulated for power dissipation by the read-out electronics, which is relatively independent of temperature, and for the sensor leakage power, that increases exponentially with temperature, as described in Section 9.1.1. Sensor power dissipation is simulated as Joule heating, by assigning an electric potential difference across the sensor thickness together with a specific electrical conductivity. The conductivity is input as a table (for interpolation) that describes the expected leakage power dissipation with temperature. Hence the FEA correctly accounts for temperature and power variation across the sensor area (albeit not through its thickness). At locations where radiation levels are highest, ionisation damage to the CMOS read-out electronics is expected to peak early in the life of the detector, when the sensors are relatively un-damaged and leakage currents are consequently low. However, the read-out heat itself is predicted to result in large temperature gradients and elevated chip temperatures, particularly in the regions of the DC-DC converters. Figure 9.9 shows predicted temperature distributions based on the present, limited understanding of the ionising dose effect and assuming a factor of 1.5/1.7 in peak digital LV power consumption with respect to initial digital LV power for stave/petal respectively. Detailed studies are in progress, to quantify the irradiation damage more precisely and to understand convective corrections and design strategies that will reduce its impact.

End of Life: Thermal Runaway

The danger of thermal runaway is greatest at the end of operation where both the leakage current and required bias voltage are a maximum. By that stage, at the locations most vulnerable to runaway, the excess read-out power due to ionisation damage will have reduced to a negligible level. At the maximum expected sensor power (allowing a factor of two on predicted fluence), the FEA finds stable temperature solutions for both the stave and the petal sensors (Figure 9.10). Temperature variations are smaller here than at the TID peak and, although localised peaks are evident, runaway will occur only if the temperature dependence of heat generated over an area comparable to the sensor exceeds the thermal conductance of the local support. FEA results for the evaporation temperature critical for



(a) Petal temperature distribution

(b) Stave temperature distribution

Figure 9.9: Temperature distribution within the FEA model, given the estimated power consumption at the TID peak, which is higher due to a 1.5/1.7 times larger (than initial) digital current consumption.

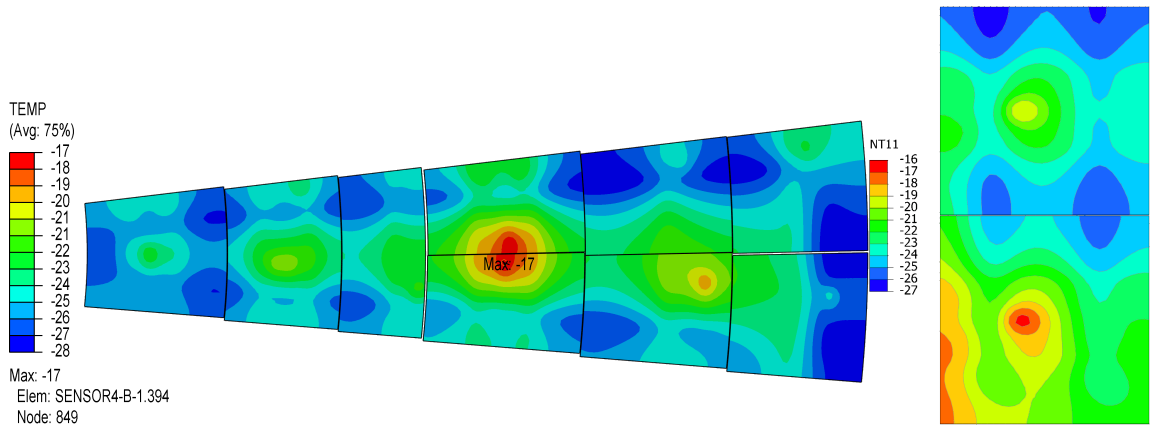
runaway are given in Table 9.6, and can be directly compared to the cooling system specification. The behaviour of the average temperature of a sensor can be estimated quite accurately from an analytic model in terms of just two thermal resistance parameters derived from the FEA [90]. This allows a simple prediction of quantities of interest, such as runaway headroom, shot noise and required cooling power. It will be further used to understand the combined effects of ionising dose and fluence, as these vary with integrated luminosity and location on the detector.

Table 9.6: Performance numbers from FEA simulation.

	Inner radius Barrel stave	End-cap petal (at highest z)
Maximum temperature variation across any sensor at TID peak	12°C	14°C
CO2 evaporation temperature that will induce runaway at end-of-life	-16°C	-16°C

9.5 Local Support Core Assembly

This section will outline core production tooling and assembly steps for the example of a barrel stave. As outlined in the design description in Section 9.2, most of these tools and assembly steps easily transfer to the petal geometry.



(a) Petal temperature distribution

(b) Stave temperature distribution

Figure 9.10: Temperature distribution within the FEA model, given the estimated power consumption after 3000 fb^{-1}.

9.5.1 Cooling-Loop Production

The components used for the cooling-tube assembly are:

1. VCR parts: fitting, nut and sealing gasket. These parts allow easy testing during assembly but will be removed during the final integration stage.
2. Titanium tube with 2.275 mm outer diameter.
3. Electrical isolator parts: ceramic, cap and braze alloy.

All these components will be pre-qualified by the manufacturers. The straight tube titanium pipe will be tested to 300 bar pressure. The tubes will be cleaned to remove oxide on the outer surface. Visual inspection and dimensional accuracy etc. will be performed before assembly. The electrical isolator assembly will be pre-qualified by the manufacturer using a leak test with a limit of 10^{-9} mbar l s^{-1}. The cooling tubes will be bent using a former to control the internal radii. Those radii range from 0.7 to 2.0 mm, depending on the structure (stave or petal). A filler will be used to prevent the pipes from collapsing while being bent. Different bend radii are used for the inlet and outlet tubes. After bending, the tubes will be dimensionally checked using a jig. The U-bends are cut to the exact length. The titanium caps are vacuum brazed to the ceramic isolators and leaked tested to 10^{-9} mbar l s^{-1} by the manufacturer. The titanium caps have a Titanium Inert Gas (TIG) [91] weld socket joint machined in. The VCR fittings are TIG orbital welded to the U-bends of the electrical isolator "wiggle". The U-bends of this assembly are then welded to ceramic caps of the isolator assemblies. The connecting nuts for the VCR fittings are placed in position. The cooling loop is placed into a tooling jig and excess length determined and cut-off using a diamond wheel to ensure a clean 90° face without burrs. The loop is then checked for debris

and cleaned. It is then placed into a tooling jig and purge gas pressure applied to the tube. A check is made that the argon gas is at the correct pressure for welding. The orbital weld head is locked onto the tooling jig, an argon purge of the weld head is made and then the weld is performed.

The electrical data from the welding process is logged as large voltage spikes are indicative of weld failures. The post-purge gas is retained for 30 s after the weld head is removed and a visual inspection is then made. The procedure is repeated for the second weld. Each weld has a unique number and the cooling loops are labelled with printable heat shrink.

Cooling loops that pass all the QC tests will be sent to the stave/petal core assembly sites for integration into the CFRP stave/petal structure.

During integration at CERN, the temporary VCR fittings will be removed. A visual inspection will be performed and then a filler ring will be inserted between the stave/petal loop and the service module interlink. The alignment and purge gas pressure for welding will be checked and then the identical TIG welding procedure to that used in the cooling pipe assembly will be used to connect the stave/petal loop to the service module interlink. A final visual inspection will be performed to detect gross failures and then vacuum and pressure leak tests will be performed. Studies of the TIG welding have demonstrated that this procedure is not dangerous for the nearby electronics.

9.5.2 Co-Curing Assembly

To avoid the need for a separate glue layer between the carbon-fibre face-sheet and the electrical tapes, the tape and the carbon-fibre are co-cured. Copper pads are co-cured at the same time into the end-of-stave area of the face-sheet for good electrical ground connection throughout the stave core. Prototypes for such co-cured assemblies have been produced.

For the co-cure and the subsequent stave core production the tape is cut with a 10 mm sacrificial rim, which prevents resin from creeping around the edge of the tape and onto sensitive areas (bond pads). The tape does not extend onto the end-of-stave area, and this area is covered by an equivalent thickness of flash-breaker tape.

The surface finish of the co-cured assemblies is excellent as they are cured with the tape against the smooth jig surface. There is evidence for contamination of the tape during the co-cure process and now this is avoided by the use of a protective polyethylene film on the tape during this process.

9.5.3 Core Assembly Tooling

The core assembly tooling provides the means of building the layer sandwich of carbon-fibre/polyimide facings, honeycomb and carbon-foam, cooling tubes, and closeouts, where

the accuracy of the product is defined by the tooling. The tooling consists of the following pieces:

- Main vacuum jig: The main vacuum jig is built from a carbon-fibre sandwich structure making it easy to handle whilst keeping it dimensionally accurate. It comes with a series of positional references (dowel holes) for locating face-sheets as well as additional tooling used during the assembly process.
- Masking ruler: This ruler allows application of glue to the facesheet in locations where carbon-foam is to be glued down. The ruler locates to the jig using dowel pins.
- Carbon-foam block alignment jig: To align the carbon-foam blocks to the facesheet, this jig holds the carbon blocks, aligning them with a half-circle representing the cooling pipe that will be inserted later. The alignment jig can then be placed on the main jig and pressed down onto the facesheet using weights. Currently it is adjusted for a glue layer thickness of 0, i.e. glue penetrating into the carbon-foam, but this can easily be adjusted by re-defining the carbon block height.
- Cooling pipe glue applicator: This is a small tool made from two parts that can be mounted around a cooling pipe straight section. It allows glue to be injected into the channel in which the cooling pipe sits, depositing a well defined thin film of glue as one slides the tool along the pipe.
- CF C-channel closeout placement jig: This jig allows the definition of the lateral placement of the C-channel closeouts, and also the definition of its vertical placement. This is particularly important to guarantee a full surface contact between the glued faces. To achieve that alignment, the jig touches on all straight inside faces of the C-channel, allowing for torsion and bend along its full length.
- In-core housing location jig: This jig aligns the in-core housings that will later be used to insert the locking points into the stave.
- $z = 0$ mid-end support locator: This locates the mid-end support (slides onto a support pin at $z = 0$)
- Glue bath jig: This jig is used to provide the outer glue faces for the top side of the assembly. While the carbon-foam glue face can be applied to the last face sheet brought down on the main assembly jig, the outside glue is applied using this bath, filling it in all areas except the carbon-foam contact faces and lowering the remaining assembly topside down into the bath.
- Locking point gluing ruler: The last tool to be used aligns the locking points with their inserts inside the stave. The tool uses counterparts of the locking points to hold these, simulating the final assembly and therefore placing the locking points in their corresponding place as per CAD design. Any inaccuracies within the locking points themselves must be caught by the glue layer applied to the outside of the locking point insertion part.

All of the above tools have been produced and are already in use to provide prototypes.

9.5.4 Core Assembly Steps

The core assembly process takes several days altogether, to allow for appropriate curing times.

To start producing a stave core, a co-cured facesheet is brought down onto the main jig, located using dowel pins and held down using vacuum. Using a masking ruler, tapes then get applied, to allow a selective application of glue to the backside of the facesheet. After the masking tape is removed, pre-machined foam blocks and the two end-closeouts are brought down into the glue using the cooling pipe alignment jig, and pressed down using weights. The whole assembly then rests over night for the glue to cure.

The second day is used to insert the cooling pipe into the groove of the (already glued in) lower foam blocks and then close off the cooling pipe assembly with the upper foam blocks. Whilst the joint between upper and lower foam blocks is created by dipping the upper foam blocks into a glue bath, the glue joint with the cooling pipe is created by applying glue directly to the cooling pipe. Once the assembly is stacked up, it gets compressed again using weights and is left to cure overnight.

C-channels are placed on the third day, closing the core off on the remaining two sides. Before applying glue to the lower side of the C-channel sections, they get attached to their placement ruler. After applying the glue, those rulers locate into the main jig, are again held down with weights and left to cure overnight.

On the fourth day, in-core locking point housings are glued into the stave using a location jig. Once those are placed, the rest of the in-core volume is filled using sections of honeycomb, no larger than 20 cm in any direction. In addition the z=0 endpoint is glued in place. All of this is left to cure overnight, before being machined to height.

After machining, the core gets sealed off by a top-facesheet. To allow for application of different types of glue (filled and unfilled), the filled glue is applied to the new facesheet (now sitting on the main jig), while the unfilled glue is filled into a masked bath, allowing the rest of the pre-assembled stave core to be dipped in. With both glues in place, the core gets lowered down onto the new facesheet, pressed down with weights and is left to cure again.

In a final step, locking points are then inserted into the core, using a location jig.

9.6 Module Loading

The module loading approach will be described along the lines of the existing module loading setup for staves. Section 9.6.7 will then go into the differences applicable when operating a petal module loading setup.

9.6.1 Requirements

The required outcome of the module loading is an accurate placement of modules, with particular focus on the axis perpendicular to the long stave axis (in plane). The basic requirements also include electrical functionality, in particular thinking of high-voltage connection on the backside of the sensor, as well as thermal contact for removing the heat generated in the modules. The requirements on module alignment are derived from a requirement on hermeticity for measuring 1 GeV tracks. The software-based alignment corrects most misplacements, as long as enough overlap is given between modules from the same barrel radius, allowing the constraint of the complete circumference. This overlap criterion is less stringent than the aforementioned hermeticity, hence automatically fulfilled. Placement precision should be to within 100 μm (both axes) of where a module is meant to be. Post-placement, a survey measurement is to take place, that will give a better knowledge of the modules relative position to the stave, allowing to seed the alignment. With current sensor dimensions and a centre-to-centre spacing of modules of 98 mm, that leaves a gap of 427 um, which will shrink slightly with final sensor dimensions.

One of the main goals of the module loading is to provide a good cooling connection by creating close contact between the module backside and the surface of the support structure. The glue used for this process should not only withstand radiation, but also be thermally conductive. Current prototyping uses SE4445[8)], technically speaking a two component thermal compound, based on a large Alumina filler fraction. Earlier use within the ATLAS Pixel and IBL detectors puts equivalent requirements on radiation hardness of the compound, but mechanical properties are currently being qualified for use with the much-larger strip sensors.

Part of the module loading procedure is the electrical connection of the stave bus-tape to modules and the End-of-Substructure card by means of wirebonding. The mounting has to provide an assembly that is not too flexible, allowing the application of appropriate pressure to the wirebonds for attachment.

9.6.2 Module Loading Tooling

The setup for module loading is comprised of two major components:

[8] Dow Corning®, SE4445 CV Gel, 2-part thermally conductive silicone gel

- An optical table with a moving microscope that can locate precisely coordinates on the table.
- Module loading bridges, which can be mounted on the table in given locations and enable a module to be put down onto a stave core in an adjustable location.

Figure 9.11 shows the stage system on its granite table.

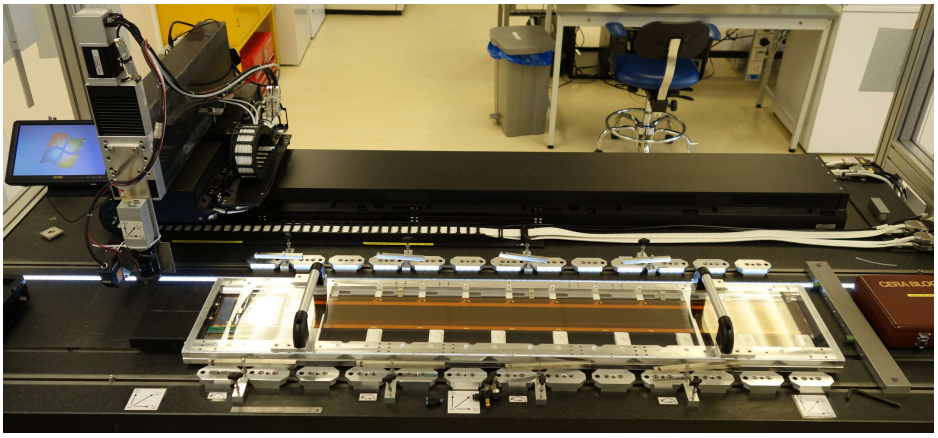


Figure 9.11: The current barrel module mounting system, including the thermo-mechanical test stave in its assembly frame.

9.6.3 Optical Table

The microscope is currently set up to show a 2.7×2 [mm] sized area through a camera projecting 2×2 [μm] fields onto each pixel of the camera. The field of view had initially been chosen to be smaller, but caused trouble in locating items on the table. A larger field of view allows for a much quicker approach and shrinks the apparatus significantly.

The microscope is mounted to a granite table, using x, y and z stages, allowing any point to be located within a region of 1500×300×150 [mm] to O(10) um accuracy. To deliver that accuracy in all axes, a monitoring system is needed to compensate for possible out-of-axis movements on the longest (X-) axis. As requirements are currently well below that achievable accuracy, the option of a straight line reference is forseen but not yet implemented in the existing module loading machinery.

9.6.4 Module Loading Bridges

The module loading bridges are designed to move a module on the stave surface. They allow translation and rotation of the module to adjust its final position on the stave. The current design employs three fine-threaded screws to do three translations, two along the stave's z-axis (if screwed in opposite directions allowing an angular adjustment), one along

the Rϕ direction. An iteration is planned, where rotation and translation are fully decoupled, but this requires testing. Each bridge is fitted with a pickup tool that serves to hold a module underneath a bridge. The pickup tool allows for a soft touchdown on the module (with silicone vacuum suction caps), rotational and lateral placement, whilst picking up any vertical non-conformities.

Method of Module Loading

Modules are glued to their corresponding stave by applying a pattern of glue. A mask of film adhesive is used to apply a known thickness (~150 μm). While the glue is at least partially cured, the modules are held in position using the module loading bridges. The pickup tools on these bridges touch down on the stave surface, next to the sensor of a module, in doing so they define the glue thickness.

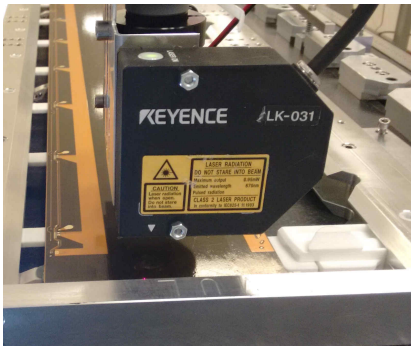
9.6.5 Post-Mounting Survey

To allow for a quick alignment, a survey of module locations and geometry is conducted after they have been loaded to the stave. This will incorporate re-measuring all module fiducial positions with respect to the stave/petal coordinate system. Once these are established, the out-of-plane geometry of all loaded modules is measured. This will allow the offline alignment to treat a stave or petal as a single, well-defined object, at least for the first pass, and hence quickly produce alignment constraints for complete staves or petals.

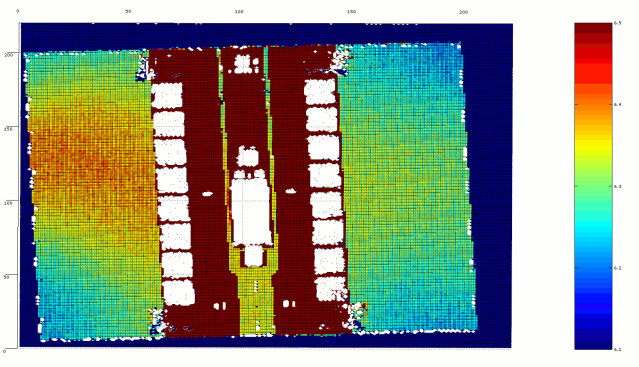
Repeatability of the stages used for module mounting will provide a global location accuracy (within the stave) of <20 μm in all directions. This is well below the sensors' resolution and therefore should suffice for the initial alignment. The out-of-plane coordinate will be measured using a laser range finder (or confocal probe, depending on availability) and should be precise to <10 μm.

9.6.6 Transport for Integration

After assembly is finalised, staves will be mounted into a transport frame. These frames are relatively cheap components which serve as a protective enclosure for handling and shipping. They also provide interfaces for various test systems. Immediately before insertion into the support frame, these dummy interfaces are disconnected and removed from the transport frame and the cooling tubes are trimmed back to their final length. The transport frame is mounted onto a system of tooling which supports the frame and manipulates it into the correct position and attitude for the insertion of the local support into the correct position in the global support sub-assembly.



(a) Laser range finder above a prototype stave. The red measurement dot is visible.



(b) Height of a module. The colour scale is in mm with an arbitrary offset. The module shows a sensor bow of about 350 μm out of plane.

Figure 9.12: Measurement system and a representative example of a measurement above a module.

9.6.7 Differences in Petal Geometries

As mentioned earlier, the general approach to module mounting using a moving microscope and module loading bridges is followed for both, stave and petal geometries. With the first setup existing for stave module mounting, certain adaptions are needed to perform the same task for the petal module mounting. At the same time, conclusions from stave module mounting have been drawn and have led to suggested changes in the way module mounting setups are to operate in a petal-style version.

Loading Split-sensor Modules

An adaptation of the tools is required for the endcap modules located at high petal radii, that is, modules R3, R4, and R5. In those regions, the modules are split into two sensors, stitched together via wire-bonds across their respective hybrids. It is suggested to load one sensor at a time for the split-sensor modules, using the same pickup tool under either a variable bridge or two different bridge versions.

Bridge Support Structure

Whilst for the stave module loading, bridges are supported by blocks mounted firmly into the granite table, it is suggested to locate the bridges of the petal module mounting with respect to the assembly frame, allowing fully flexible location on the module mounting table.

9.7 Test Results

The following subsections present results for many prototypes. Some of these are very close to the final objects proposed, some are early prototypes, measurements of which have led to significant design changes and are presented for completeness.

9.7.1 Stave Core Mechanical Performance

Multiple stave cores have been produced in the course of R&D, and have been checked for their geometrical and mechanical properties. An initial check of vibrational frequency response showed that stave cores are sufficiently well built to be tested by means of 3-point bend tests, as their vibration properties can be predicted well enough from a model. Most recently, the latest prototype stave to hold first electrical 130 nm chipset modules on it was checked with such a test: It shows that, given a known load (due to modules and glue) of about 500 g[9)], the stave will deflect by up to 5 mm (given a spacing of 1.4 m as shown in Figure 9.13). This "softness" of the staves allows them to be inserted even if the stave itself is not perfectly flat and therefore drastically reduces constraints on the global flatness of the local support cores.

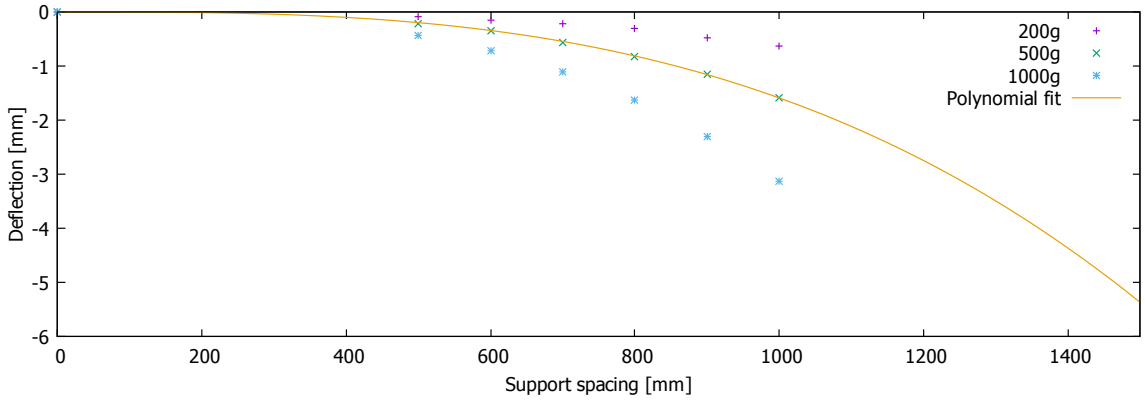


Figure 9.13: Results of a 3-point bend test with different spacings between the supports and three different loads. A 3rd order polynomial fit is shown, extrapolating to about 1.4 m length for the final stave design, loaded with 500 g.

[9] The stave core weight itself is 340-360 g in prototypes, depending on the amount of glue used during assembly

9.7.2 Petal Core Flatness

A number of mechanical tests were performed on preliminary petal core prototypes. These measurements were performed in order to asses the feasibility of the existing test setups. Global flatness measurements following ISO Geometrical Product Specifications (GPS) standards were performed on completed petal cores. Measurements were performed with a 3D microscope (SmartScope). Given the final position of the petals in the endcaps, the petals were laid down on the measurement table unsupported. Global flatness results obtained for one of the finished cores are shown in Figure 9.14. The core exhibits a global flatness over its full surface of ~ 250 μm.

9.7.3 Stave Core Prototype Flatness

The stave core must be sufficiently flat over the area of a module (100×100 mm^2) to achieve reliable module glue attachment. Laser scans of surface height have shown that height variations over this area are typically well below 100 μm (Figure 9.15), therefore allowing a 150 μm thick glue layer to compensate for that un-evenness when glueing down modules.

The detailed shape of the unconstrained stave core has also been measured using a CMM and was found to be well within a 300 μm envelope, but due to findings about the stability of the stave (see Section 9.7.1 above) there is no hard requirement on the global flatness.

9.7.4 Long-Term Stability

Stave core prototypes in particular have been looked at in the context of long-term stability. To accomplish a measure of stability, a prototype was installed the same way it is to be installed in the experiment and loaded with an appropriate out-of-plane load. This allowed to establish whether time or thermal events cause displacement of the stave core with respect to its installation position. The initial test gave two major results:

- Long-term stability: Initial prototypes showed a long-term relaxation behaviour around the edge-mounted locking points. The design was changed according to these findings, extending the locking points into the stave cores. A new stave core section has then been mounted and loaded, and shown that the improved locking point now rotates around the locking point features, rather than around the glue joint, which was the intended improvement. Given that this was only a section of a stave core, no quantitative measure of displacement can be given, but relating to the initial full prototype the "gravitational sag" can be estimated to be well below 130 μm. With clearances (depending on the barrel layer) of more than 1 mm this does not impose any problems for the construction or operation.

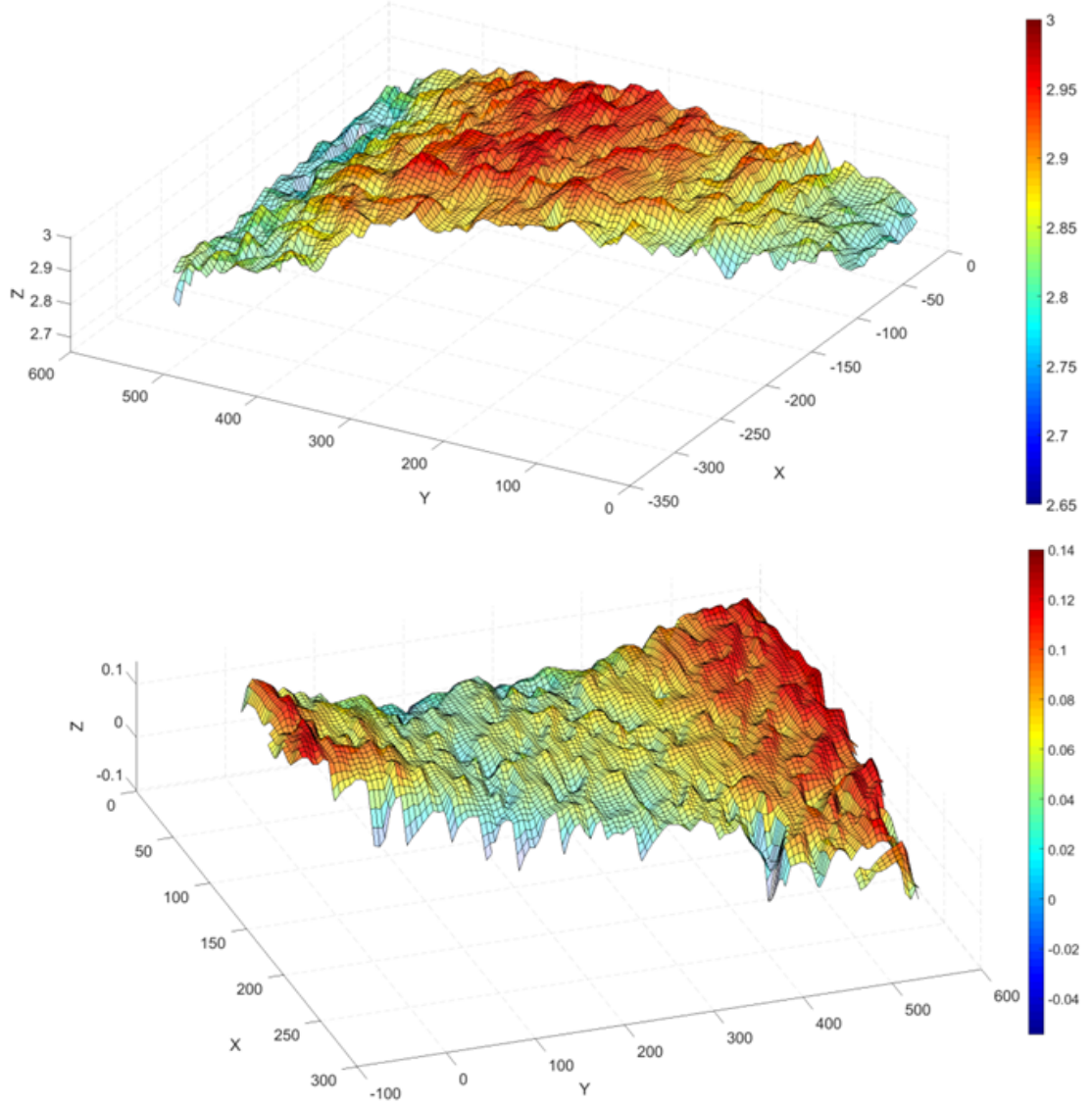


Figure 9.14: Flatness measurement of the sides of a representative petal core. **Top**: front side and **Bottom**: back side.

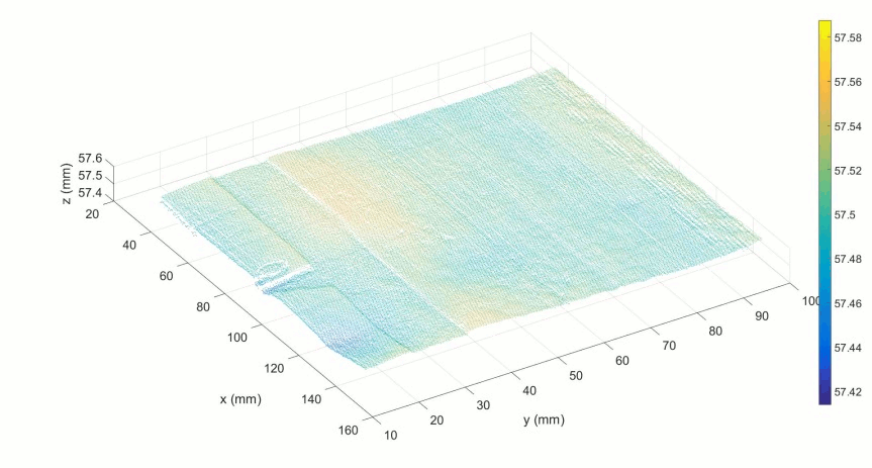


Figure 9.15: Surface height data over a typical 100 $\times$ 100 mm^2 area of stave core surface. The maximum out-of-plane deviation fits within a 100 μm envelope.

- Thermal changes: Thermal cycles of the initial prototype (exhibiting a long-term relaxation feature) have shown that the prototype deforms slightly under drastic temperature changes, but will return to its previous shape given a stable temperature.

9.7.5 Thermo-Mechanical Prototypes

Module loading as described in Section 9.6 has gone through a few years of prototyping in a barrel-type system, not only allowing the evaluation of the assembly process, but also feeding back into the core design, in particular for the stave core. The technology of aligning both the local support and the modules has been used for assembly of five stave prototypes of different length and with different numbers of modules, iterating also on the alignment operation. First results from a modules with ABC130 chips with close-to final dimensions (13 modules instead of planned 14 modules) are now available. Additionally, thermo-mechanical prototypes of petals and staves are being constructed, which use sensor equivalents, both thermal and mechanical, and special hybrids with integrated resistive heaters to simulate the heat load of a realistic local support assembly.

250 nm Stave Prototype measurements One of the early prototypes built is a "250nm stave" with thermo-mechanical modules, that was used to test the concept of a local support, integrating cooling through carbon-fibre heat conduction. This also helped to verify that FEA modelling is possible and delivers realistic results. Equipped with 12 thermo-mechanical loads per side, this structure was cooled with a blow off CO_2 cooling system and run at different input powers. Measuring the temperature of a thermistor on the heat loads, a thermal resistance was established, as shown in Figure 9.16. The extracted value

is only 5% above what was extracted from an FEA model of the same structure and gave confidence, that the FEA simulations give a reasonable estimate of what can be achieved.

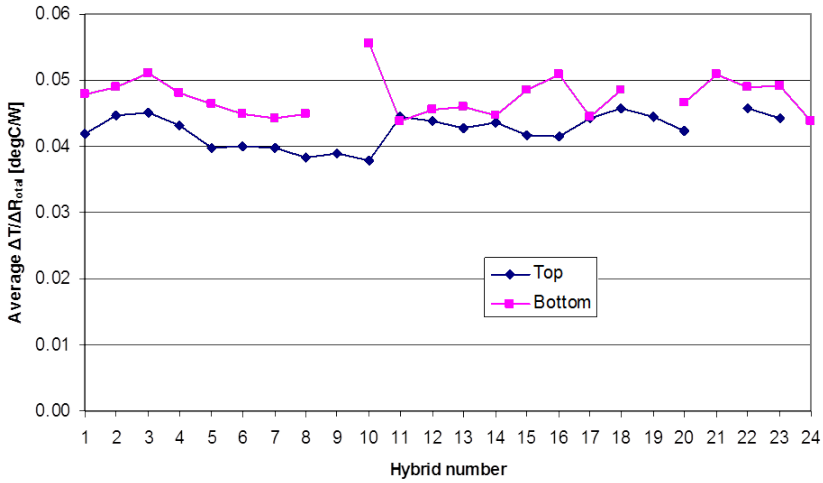


Figure 9.16: Thermal resistance measured at each location of the 250nm thermo-mechanical stave.

130nm thermo-mechanical stave prototype The 130 nm stave prototype is in production using the module loading mechanism and system described earlier, allowing evaluation of its performance under realistic conditions. The stave is aligned on the table, and module fiducial locations are repeatedly recorded to observe drift throughout the assembly process. An example of two module fiducials is shown in Figure 9.17. This shows how the fiducials move in the various stages. The visible range within these images is 400 $\times$ 400 μm and a movement due to curing and releasing the vacuum is visible in y, limited to less than $\pm$10 μm, thereby falling well within the requirements. The fiducial marker size is 70 μm in both the vertical and the horizontal direction. Therefore, given a 100 μm requirement on location, a movement not meeting this requirement would be indicated by the fiducial marker moving fully onto one side of the red markers locating the centre of the image.

Assembly of the 130nm thermo-mechanical stave prototype has already passed the mounting of all modules and currently undergoes wire-bonding. The prototype will provide essential cross-checks with respect to FEA simulations of the current core layout.

Thermo-mechanical petal prototype In order to validate the petal geometry and core structure, a fully equipped thermo-mechanical petal was built and measured, see Figure 9.18.

The core construction is based on preliminary petal designs, and built with the real materials, including 2.275 mm outer diameter CP2 titanium pipes, K9 Allcomp foam around them, carbon-fibre honeycomb, and K13C2U carbon-fibre face-sheets, co-cured together with a thermo-mechanical bus-tape designed for that purpose. In that tape, dummy data lines

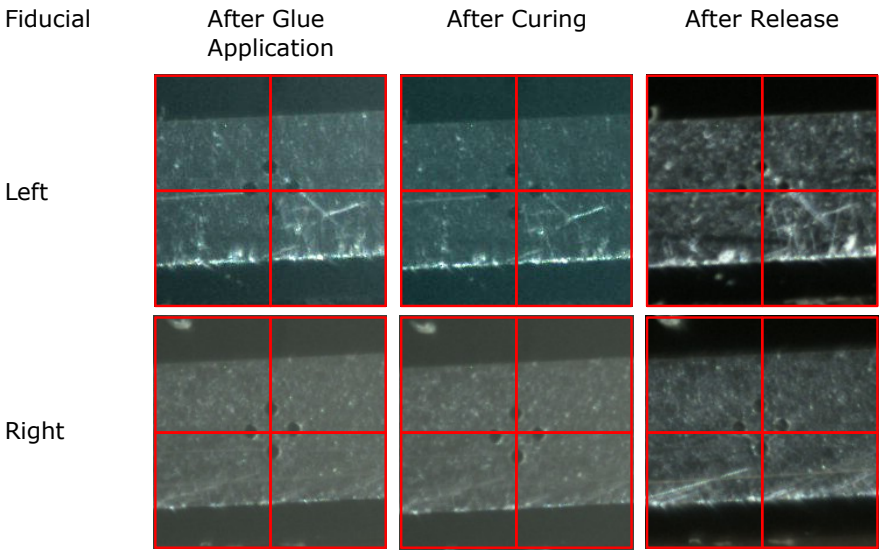


Figure 9.17: Fiducial markers through the process of module mounting (from left to right) for two different locations on a module. In particular, the lower row shows a down and up movement in the range of ± 10 μm. The total fiducial marker size reflects the requirements (70×70 μm), hence a movement out of spec would definitively be indicated by fiducial points crossing the line that was originally between two opposing points (e.g. both vertical fiducial points being above the horizontal line).

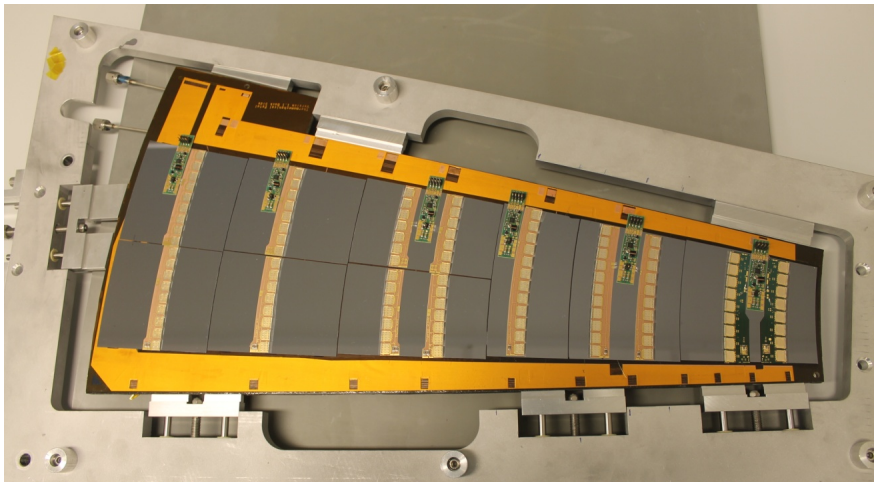


Figure 9.18: Photo of the thermo-mechanical petal prototype.

and shield layers are included, as well as real copper power traces. The thermo-mechanical modules consist of blank silicon crystals laser-cut to shape (320 μm thick), FR4 hybrids (200 μm thick) directly glued to them via UV-cured glue, and glass patterned ASICs with a heat pattern (350 μm thick), directly glued to the hybrids with UV-cured glue. The patterns in the ASICs and the gold traces in the hybrids allow for direct wire-bonding between ASICs and hybrids. Wire bonds were made also between the ASICs and the blank silicon. The HCC ASICs are emulated with SMD resistors of the appropriate value in the HCC locations of the hybrid. Finally, the DC-DC converters consist of a commercial buck converter (LTC360 ASIC) and inductor coil mounted on a custom FR4 board of the appropriate size. The converter provides the required power for each module, and the converters are powered via standard power supplies through the bus-tape power traces. As in the real case, the heat is mostly dissipated in the converter, the glass ASICs, and the SMD resistors emulating the HCC ASICs. The modules were directly glued on the petal bus-tape surface with SE4445 adhesive. The target glue thickness was 140 μm. The assembly of the modules into the petal was performed manually, with the help of templates, glue masks, and stencils for proper positioning of the petal. The glue thickness was controlled using fishing-line wires 140 μm diameter) below all sensors.

Optical metrology measurements were performed on the thermo-mechanical petal with a 3D microscope (SmartScope), making use of the Grid Projector feature, which allows the reliable measurement of highly reflective (silicon sensors) and transparent (Polyimide bus-tape surface) surfaces. The high accuracy of these measurements and the ease of obtaining them provided important input for the development of QC methods for petals and cores during production stages. The location of the silicon crystals within the petal was determined with measurements at the periphery of the sensors. The glue thickness for each module was obtained with pairs of measurements on the sensors and on the bus tape surface, at the periphery of the silicon crystals. Figure 9.19 shows the measurement map within the petal, and the glue thickness measurements for the silicon modules of the back side of the petal.

Infra-red thermal tests of the thermo-mechanical were performed at a custom thermal chamber. The infra-red camera (VarioCam 640 HR from Infratec) was inside the chamber, flushed with dry air. Temperature and humidity inside the chamber was monitored with SHT70 sensors, as close as possible to the petal. The thermo-mechanical petal was cooled down to $+5^{\circ}$C (measured at input cooling pipe) with a water-glycol chiller in a dry-air atmosphere (chiller temperature -20°C). Humidity values equal to 2% RH were measured at the vicinity of the petal during the tests. Both petal sides were powered at the same time, dissipating 24.8 W per side. No EoS structures are included in the thermo-mechanical petal, as observed in Figure 9.18. Figure 9.20 shows the infra-red image of the thermo-mechanical petal under these conditions. Reference regions were established on the silicon surface using black tape (faintly visible at the left corners of the R0 module), providing input for emissivity correction. The image was then corrected offline for the appropriate IR emissivity values of silicon based on the results measured at the reference regions and

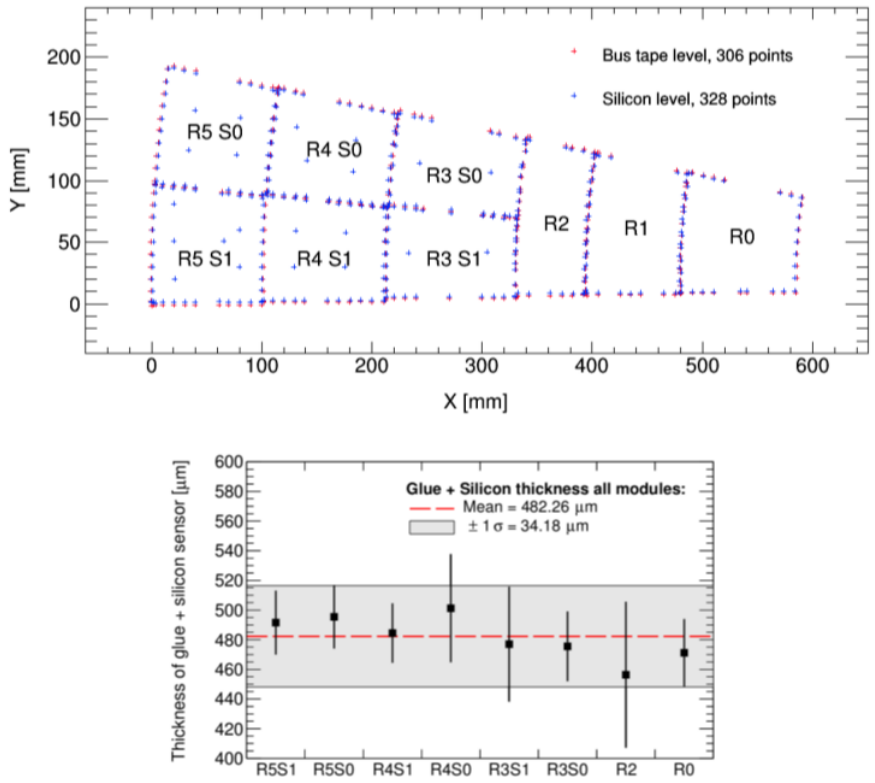


Figure 9.19: Optical metrology measurements of the thermo-mechanical petal. **Top:** Map of measurements on the thermo-mechanical petal, showing the location of the silicon sensors. **Bottom:** Glue thickness measurements for the silicon sensors. Sensor thickness is 320 μm. Average glue thickness is 162 $\pm$ 34 μm.

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their vicinity at a known emissivity value, and on the Stefan-Boltzmann law for black body radiation. The final value for the corrected emissivity at that temperature was established as $\epsilon_{corr} = 0.68$. Significant deviations with respect to real temperatures should be expected in Figure 9.20, for the regions which are not silicon (everything but the sensors on this prototype). However temperatures in the silicon sensors surface are reliable. The image show a good qualitative agreement with simulations. The main hot spots are observed at the DC-DC converters and at the HCCs. More systematic test are under way, which shall allow for a quantitative comparison with simulation. This will, in particular, require use of a high pressure CO_2 cooling system, so as to deliver the correct heat transfer coefficient inside the cooling pipe.

9.7.6 Module-Mounting Glue Studies

Although SE4445 has previously been used in pixel detector assemblies (ATLAS Pixel and Insertable B-Layer), its use for the much larger strip sensors was re-evaluated.

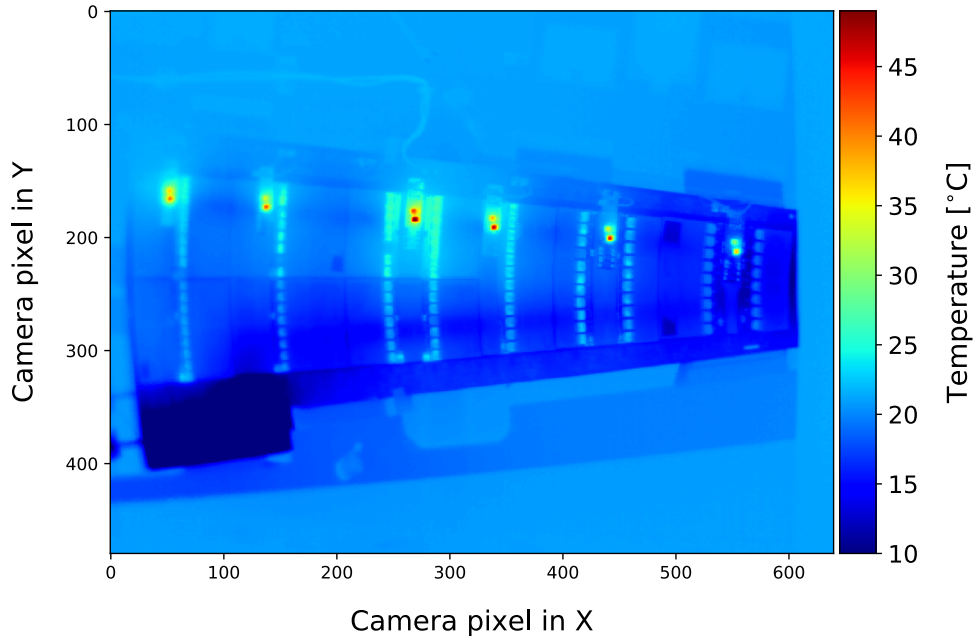


Figure 9.20: Infra-red image of the front side of the thermo-mechanical petal. Emissivity was corrected for the silicon surfaces ($\epsilon_{corr} = 0.68$).

In a bottom-up approach, tensile stress tests have been performed to deliver numbers for Young's modulus (∼3.5 MPa) and peak stress (∼0.35 MPa). Furthermore, the tests observed that the glue can survive a strain of ∼2-3 times past strain at peak stress. Tests were carried out by applying strain at different rates, and the glue turns out to have an increased peak stress with decreasing strain rate.

Since the glue changes properties with temperatures, getting harder at lower temperatures, these tensile tests were also repeated at low temperature (-50°C) and showed an increase in Young's modulus by a factor of 2-4, whilst the peak stress increased by a factor of 5-10.

Given the above results, test samples with module equivalent structures glued to local support equivalent carbon-fibre sandwiches using SE4445 were produced and successfully thermo-cycled 100 times between +30°C and -50°C. After cycling, the glue layer was still intact and no mechanical failure was observed.

9.7.7 Data Transmission Tests

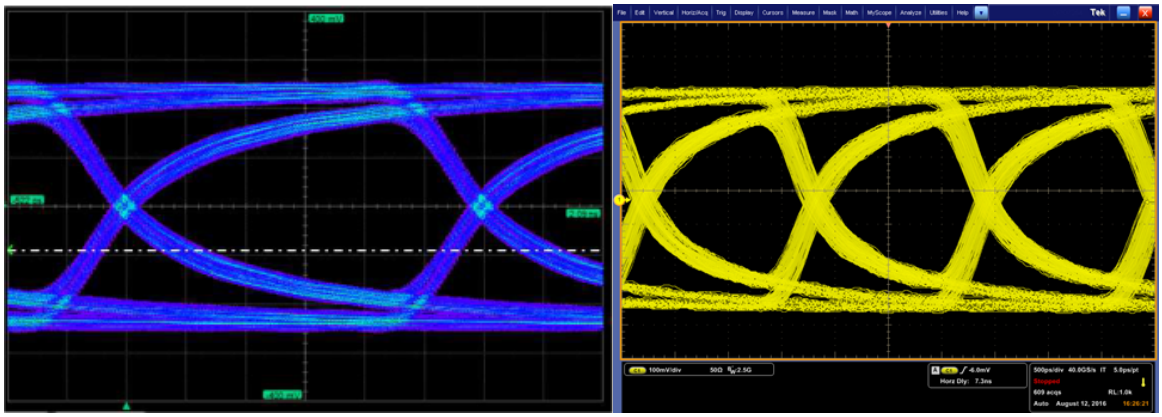
The quality of the data transmission was studied using FEA calculations and experimental measurements of S-parameters. The losses for the transmission lines in the relevant fre-

quency range are dominated by the resistive loss in the lines

$$f = \exp\left(-R/2Z_0\right) \tag{9.1}$$

where R is the line resistance (taking into account the skin depth) at a given frequency and Z_0 is the characteristic impedance. A differential impedance of close to 100 Ω is required both to minimise reflections and lower the resistive losses.

The expected performance of the data transmission on the bus-tapes [10] was studied with FEA calculations [11]. The calculated S-parameters were used to simulate 'eye-diagrams' to assess the signal integrity. This indicated that clean eye-diagrams could be obtained for the point-to-point data links operating at 640 Mbit/s. Experimental measurements of S-parameters were made on a 1.4 m long test tape using a network analyser. The measured S-parameters were then used to simulate eye-diagrams for Pseudo Random Bit Stream (PRBS) data. The resulting eye-diagram for the location at the furthest end from the source (which has the maximum attenuation and dispersion) is shown in Figure 9.21.



(a) Data eye diagram (b) TTC eye diagram

Figure 9.21: Eye diagrams resulting from a simulation based on measured S-parameters, for 640 Mbit/s (Data) and for direct measurements on a test tape.

Direct measurements of the signal integrity were performed on a test tape with test chips containing drivers and receivers of the type expected in the HCC130 ASIC. The eye-diagram for the longest line for 640 Mbit/s point-to-point data transmission is shown in Figure 9.21. This clearly shows the effects of dispersion but confirms that a reasonably clean eye-opening can be achieved. Bit Error Ratio (BER) measurements confirmed that the BER was lower than the required maximum value of 10^{-12} and this could be achieved at higher frequencies. Improvements in data quality were also demonstrated using 8b10b encoding which

[10] The studies used barrel bus-tapes as they are significantly longer than for the end-caps.
[11] Using HFSS from ANSYS.

removes the effects of the slow tail of the rise time [92] and by using pre-emphasis. The HCC130 will allow for the option of using 8b10 if required and for pre-emphasis.

The TTC transmission uses a 40 MHz clock and 160 Mbit/s data lines. The critical issue here is that each HCC130 chip on a bus tape represents a capacitive load and therefore generates unwanted reflections. This causes the transmission to fall away rapidly above a frequency of $\sim$ 500 MHz and the reflections to increase. Using a design with one TTC bus for all 28 HCC130 chips on a barrel bus-tape showed significant signal integrity problems. The worst signal integrity was for the location near the middle of the line due to the combined effect of reflections, dispersion and attenuation. Therefore the TTC bus for the barrel was split into four sections, serving 2, 10, 8 and 8 HCC130 chips [12)]. The signal integrity was studied on a test tape with ten capacitive loads to simulate the HCC. The signal integrity was greatly improved compared to the original design with 28 loads because the dispersion in the line, reduced the speed of the edges and therefore decreased the magnitude of the reflections. The worst signal integrity was for the first load because of the effect of reflections, however a relatively clean eye diagram was obtained at the required transmission speed of 160 Mbit/s (see Figure 9.22). The BER was measured to be less than the required value of 10^{-12}. The safety margin was studied by doubling the magnitude of the capacitive loads and increasing the data rates until errors were observed. This showed that there is a very large safety margin.

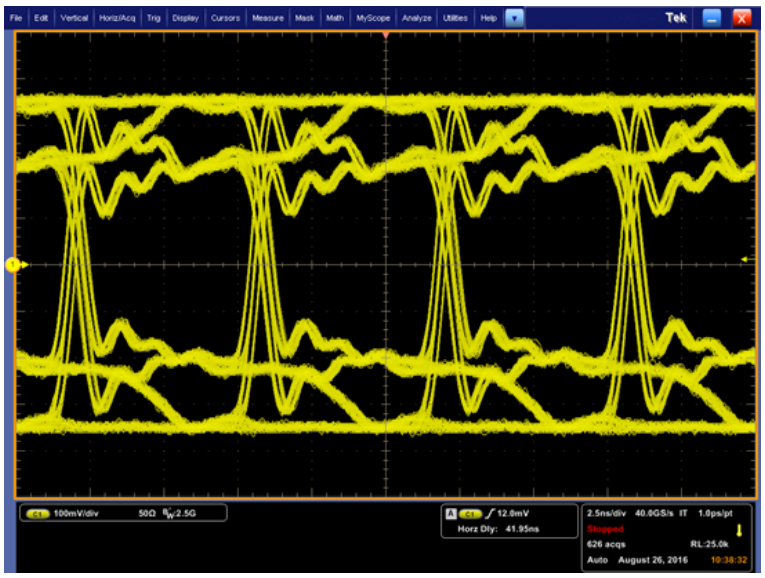


Figure 9.22: Eye diagram for PSRB data at 160 Mbit/s for the first load of 10 (location closest to EoS).

[12] This change was requested by the TDAQ group to allow finer grained TTC data to be sent to the modules.

9.8 Quality Control in Production

The stave or petal core will be assembled from the components listed in Table 9.7 along with initial tests to control their quality before they are used to assemble a stave/petal core. With the exception of the graphite/epoxy, all components will also be weighed and visually inspected.

Table 9.7: List of suggested Quality Control (QC) tests on local support core components during production.

Component	**Tests**
Co-cured facing	Thickness. Tape measurements identical to those described for a bus-tape. Modulus tests on facing coupons. Resistance measurements on co-cured copper strips.
Carbon-fibre honeycomb	Thickness. Crush strength. Density.
Pipes	Pressure tests 200 bar. Helium leak tests.
Carbon-foam	Density. Electrical conductivity. Thermal conductivity.
C-channels	Thickness and dimensional measurements.
Peek closeouts	Thickness.
Graphite/epoxy	Two molded dog bone sample coupons per stave/petal. Full electrical and thermal testing of one sample for a fraction of the cores (1 in 5 cores or 1 in 10 cores). Other sample will remain a traveler with stave/petal for later testing if needed.

During construction of the stave core the partially assembled core will be weighed after each glue step. This allows the amount of epoxy used at each step to be ascertained and is a check on the consistency of the construction techniques. The determination of the amount of epoxy that is used is necessary to calculate the final radiation length of the stave core.

Before attachment of the second facing, electrical measurements of resistances between various components, such as the foam to the EoS copper strips, will be made and recorded. This will determine the consistency of the assembly

Each stave/petal core will first be thermal cycled between 25 °C and -40 °C for 24 hours before the measurements are made so that thermal or mechanical defects introduced by the cycling will be detected.

The following measurements will be made either on each assembled cooling loop or full stave/petal core. The purpose of each quality control measure is also listed below.

9.8.1 Cooling Loop QC

A series of QC tests will be performed on the complete cooling loop assembly:

1. Visual inspection for dents, defects, pin holes, rippling of the bent tube, dimensional tolerance of components, discolouration of joints to indicate above normal temperatures (indicate potential metallurgical issues).

2. Hydraulic pressure testing to 200 bar.

3. Vacuum leak checking to 10^{-11} mbar l s^{-1}. This leak rate should be maintained for several hours and should be carried out in parallel with the pressure testing.

The last two tests will be performed on a system that holds multiple cooling loops. The system will cycle the cooling loops under working pressure to $-60°C$ for a defined number of cycles. After a defined number of repeated welds or the start of any welding operation from cold, the TIG electrode will be changed, a new tube-tube test piece produced and cross sectioned to visually check for root weld penetration and weld faults in the tube bore.

A fraction of the assembled cooling loops will be subject to further QA tests as described in Section 14.1.7.

9.8.2 Bending Stiffness

The stave/petal core is simply supported at each end and different weights are placed on the centre of the core. From this simple measurement, the bending stiffness of the stave is determined. The bending stiffness should be within acceptable limits and its determination is a check on the overall quality and consistency of the core construction. From the bending stiffness, the effective tensile modulus of the facings are determined and this is a final check on their fabrication of the facings. The bending stiffness also serves to provide the fundamental vibrational frequencies of the stave/petal core.

9.8.3 Thermal Imaging

This technique involves chilling the core via coolant flowing through its pipes down to $-30°$C. The stave is chilled in dry air or nitrogen. An infrared thermal imaging camera takes an image of the complete core. From this technique, the thermal impedance of each point on the surface of the core can be determined. Stave/petal cores with anomalously high thermal impedances will be rejected.

9.8.4 Delamination

This technique is still under development but has been demonstrated on a short stave prototype. The purpose of this technique is to ensure good bonding of the facing material to the carbon-fibre honeycomb and foam. The core is constructed to be virtually air tight but has two ports on the pipe side closeout that are used to vent the core. These ports can be used to apply an interior pressure as well. Approximately 5 psi of pressure will be applied to the interior of the core and a scanning technique will be used to look for deformations in the facings. Deformations indicate a lack of a good glue joint at that location. Deformations above a certain height will be used to reject a stave/petal core. This technique will serve to assess the overall quality of the fabrication process. It is expected that with good fabrication techniques very few cores should will show any deformations.

9.8.5 Flatness

A similar or identical scanning technique will be used to assess the flatness of the core. As the final shape of the core in the experiment will be determined by its mounting brackets and its orientation on the barrel, this test serves to provide an approximate check on the consistency of the core construction. Cores that exhibit large deviations from flatness will be rejected. The same measurements will assess local flatness, which is flatness of the stave/petal core over dimensions of a silicon module (~10 cm). Nominally a core should have a local flatness not exceeding 100 μm to permit good application of the 150 μm thick module-to-core glue.

9.8.6 Stave Core Electrical Measurements

This test measures the resistances between all the co-cured copper strips on both sides of the stave/petal core. They should all be connected to each other with a low resistance via the conductive graphite/epoxy used to construct the core.

9.8.7 Bus Tape Measurements

The electrical continuity of all tracks will be measured with a robotic tape tester. The system is comprised of two heads on a gantry system. Each head contains a camera which can take photographs of fiducials on the tape. Image analysis software then determines the fiducial centres and, after the system is calibrated, this allows the tester to move to any required pad. Each head also contains a probe to allow the open and short circuit testing to be performed. A photograph of the prototype tape tester is shown in Figure 9.23.

After checking for continuity, the tape tester will check for short circuits between all neighbouring networks. In order to confirm the reliability for high- voltage operation, the tape

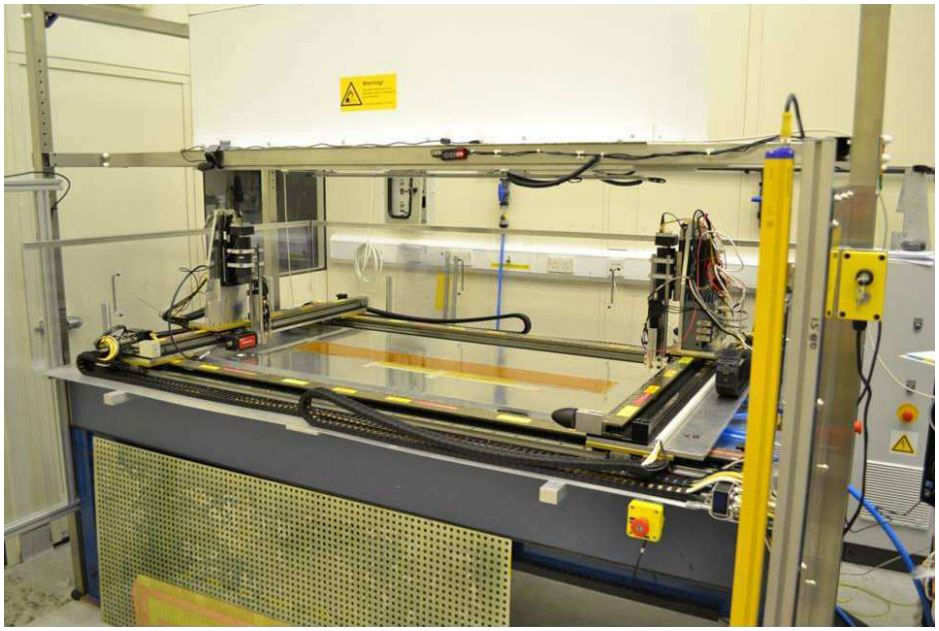


Figure 9.23: Photograph of the prototype robotic tape tester.

tester will also measure high-voltage insulation resistance (HVIR) at a voltage equal to twice the maximum voltage required in operation. The tape tester will perform simple length measurements to check that the module-to-module length is as expected before and after the co-cure process. A prototype robotic tape tester has been built and used to test prototype tapes built in industry and by Oxford University. The tester was able to successfully measure the electrical continuity, short circuits and HVIR for these tapes. The tester also measured the location of fiducials to determine the length expansion. In production, an optimised version of this tape tester will be used for the Quality Control (QC) for all tapes. This QC step will be carried out at three stages of production:

1. On receipt of bus-tape from industry.
2. After co-cure of tape to carbon-fibre skin.
3. After the co-cured tapes are assembled into a full mechanical stave.

10 Strip Detector Global Support

In this chapter, the global structures that have the primary role to locate robustly the sub-structures carrying the strip modules are discussed: staves and petals in the barrel and end-cap structures respectively. The structures will be largely made of carbon-fibre in order to cope with large temperature variations up to 60°C. Whenever possible, interfaces are glued, rather than bolted, with adhesives that are qualified for the expected radiation level including safety factors.

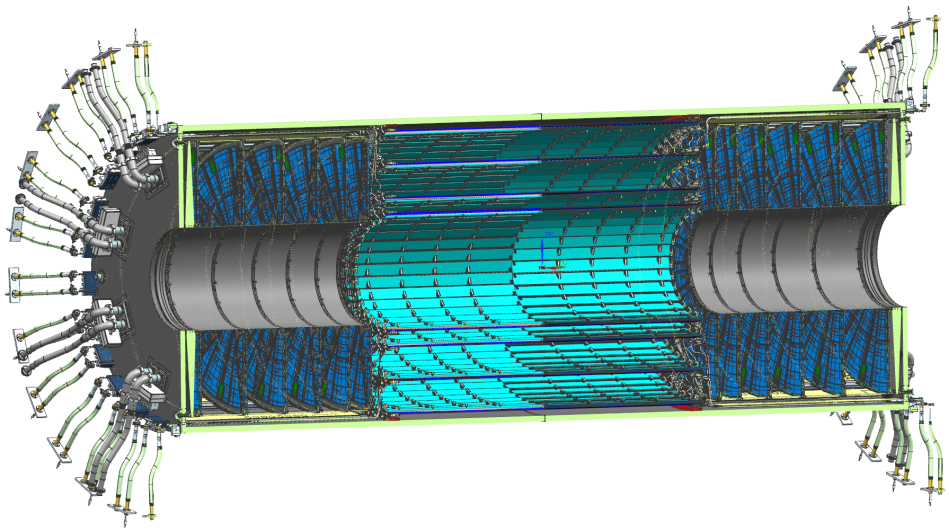


Figure 10.1: Cross section of the outer cylinder that accommodates the strip barrel and end-cap structures. The Pixel system (not shown) is placed in the inner tubes of these structures. The outer cylinder is closed by structural end-plates (bulkheads).

Figure 10.1 illustrates the large structures that constitute the ITk Detector. These structures are independently constructed and assembled at different institutes and later combined at CERN. The strip structures, a barrel and two end-caps, are housed inside the outer cylinder (OC) (7 m long by 2 m diameter) made with carbon fibre skins over a honeycomb core, see Chapter 18 for a detailed description. The outer cylinder supports the strip barrel layers through interlinks at its outer ends and the strip end-caps through a semi-kinematic rail system. The elements of the interfaces directly attached to the strip structures are discussed in the following.

The inner strip barrel holds the Pixel system, which is connected at its outer ends to the end-plates or bulkheads of the outer cylinder. The bulkheads maintain the circularity of the outer cylinder and initially support the end-cap strip structures during installation, see also Chapter 21.

The outer cylinder, since it is attached to the ATLAS cryostat, picks up external vibrations produced directly by the whole ATLAS apparatus itself or caused by seismic movements. Below, the expected magnitude of these vibrations and the requirements they impose to the structures are discussed.

10.1 Requirements and Targets

The structural requirements summarised here are derived from the ATLAS ITk stability requirements. The accurate in-situ track alignment requires a modest initial accuracy of 100 μm, to guarantee mechanical clearance and/or overlap between active elements. However, stability considerations impose more stringent requirements. These are quantitatively obtained from actual vibration measurements in the ATLAS cavern using accelerometers.

The stability requirements are listed in Table 10.1. The modal structural performance requirements were derived by considering the maximum detector resolution in R, ϕ and z. These resolutions are then used as maximum allowable motions during running to not reduce the detector performance (see Column A of Table 10.1). These motions are converted to modal requirements using the Miles equation. The Miles equation assumes a flat Acceleration Spectral Density (ASD) and indicates at what frequency the structure will move a certain distance. For this study ASD profiles from several similar experiments have been used. As the Miles equation is based on a simple one-dimension model which does not allow for many real world characteristics, it was decided to add a safety factor to the requirements by requiring one order of magnitude more on the assumed ASD. Based on past experiences this was found to be a healthy margin. This is then shown in Column B of Table 10.1.

As the tracker is designed with quite different resolutions in the three principal directions, a different requirement is placed on the independent degrees of freedom. The safety factor are large due to two main reasons. The Miles approach does not take into account superposition of responses and there is a tendency in FEA to overestimate modal responses.

These are significantly different as it is recognised that many parts of a modal system are difficult to simulate well and, to ensure the performance is not degraded and the final requirements met. Most challenging in the design of the global structure is the need to avoid vibration modes in the ϕ direction with resonances below 31.6 Hz.

Table 10.1: Stability requirements more modes in the R and ϕ direction. Column A shows the frequency above which motions will be smaller than the displacement requirements for the assumed ASD. Column A (B) lists the performance (design) requirement based on the corresponding Acceleration Spectral Density (ASD) as listed.

System	Direction	Stability requirement	1st mode (A) ASD=$10^{-7}g^2$/Hz	1st mode (B) ASD=$10^{-8}g^2$/Hz
Strip barrel	z	20 μm	3.2 Hz	6.7 Hz
	R	20 μm	3.2 Hz	6.7 Hz
	ϕ	2 μm	14.4 Hz	31.6 Hz
Strip end-cap	z	20 μm	3.2 Hz	6.7 Hz
	R	20 μm	3.2 Hz	6.7 Hz
	ϕ	2 μm	14.4 Hz	31.6 Hz

10.2 Interactions between Sub-Systems

The support hierarchy minimises the interactions between the sub-systems. After installation, the subsystems are largely kinematically supported by the outer cylinder and its bulkheads. One exception is the connection of the Pixel system and the barrel structure. The Pixel system has its own support tube, which is supported by the outer end of the barrel structure and the two bulkheads. Moreover, the bulkheads support the end-cap structure during petal installation and transport to CERN, allowing the pre-installation of all end-cap services up to integrated patch-panels (PP1).

The support of the barrel and end-cap structures is described in more detail in the following sections.

10.3 Barrel Structures

The barrel consists of four concentric cylinders connected together at the ends of the cylinders by interlinks. The interlinks are "one per stave" (i.e. 120 interlinks per end − connecting each cylinder to its neighbouring cylinders).

The ITk common mechanics group has explored how the barrels interface to the outer cylinder. The preference is to use another ring of interlinks to make this connection, forming a quasi continuous interface between the barrel structure and the outer cylinder. Should this prove problematic, a backup solution of structural independence is maintained, where the barrel structure interfaces to the outer cylinder kinematic mounts at four points (3 and 9 o'clock at either end of the barrel).

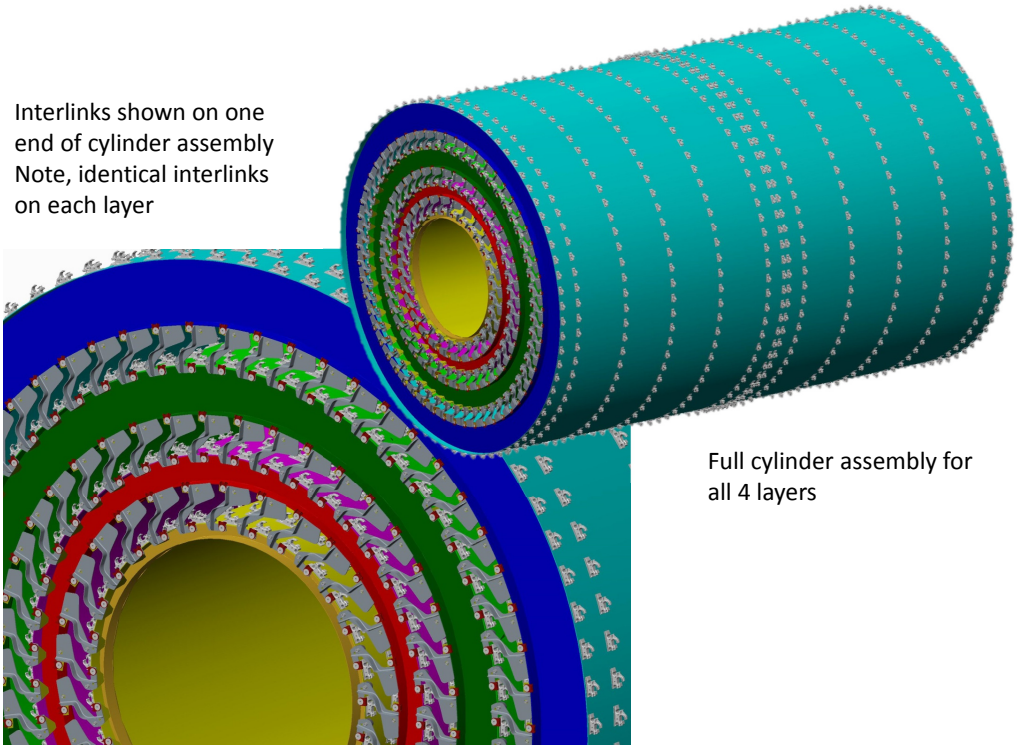


Figure 10.2: Drawing of the barrel structure.

As the detailed design of the cylinders and interlinks is incomplete at this time, the present developments and uncertainties are described along with probable mitigations. The design consists of single skin cylinders with reinforcement rings along the length in specific locations (up to eleven rings and two end flanges). The experiences and costs of the Pixel and SCT structure barrels in the present tracker have led to this concept.

The expected performance of the proposed cylinder and interlink designs was studied in detail. Additionally, vendors have been contacted to investigate the possibilities to refine the design and minimise the cost of the structure without compromising its performance (see Figure 10.2).

10.3.1 Cylinders

The optimisation is based around a single skin of K13C2U pitch-based carbon reinforced fibre polymer (CRFP) in a cyanate-ester matrix. The skins of the following thicknesses would be appropriate for the four cylinders:

These skins are adequately stiff to have the first mode above the required frequencies. However, the toughness of such thin skins has to be further investigated. This may lead to the

Table 10.2: Layups of conceptual barrel support cylinders. All fibres are K13C2U in a EX1515 matrix.

Layup detail	**Cylinder 0**	**Cylinder 1**	**Cylinder 2**	**Cylinder 3**
Ply 1	0°	0°	0°	0 °
	t=0.36mm	t=0.36mm	t=0.42mm	t=0.45mm
Ply 2	90°	90°	90°	90°
	t=0.36mm	t=0.36mm	t=0.42mm	t=0.45mm
Ply 3	0°	0°	0°	0°
	t=0.36mm	t=0.36mm	t=0.42mm	t=0.45mm
Ply 4	90°	90°	90°	90°
	t=0.36mm	t=0.36mm	t=0.42mm	t=0.45mm
Total thickness	1.44mm	1.44mm	1.68mm	1.8mm

choice of a less-brittle lower-modulus fibre which increases the thickness and thus radiation length, but reduces the risk of handling damage during assembly and integration. At either end of the cylinder is a flange to allow attachment of the interlinks. The design of these flanges is dominated by the need to interface to the interlinks. The flanges are also required to maintain the hoop structure of the cylinders and need to maintain a specific hoop stiffness and a longitudinal shear stiffness.

The flanges are bonded to the cylinders with a room-temperature cure epoxy[1)]. The tooling for this operation is yet to be developed, but is required to set the two flanges perpendicular to the cylinder axis, and parallel to one another. These perpendicularity and parallelism requirements are driven by the needs of the interlinks, as the interlinks need to bridge the tolerances of the two cylinders they link. The flanges and cylinder shells also have attached the stave lock points. There are five identical lock points along a stave every three modules (see Figure 10.3) and then a unique lock point at $z = 0$. This means that every stave position has a row of 11 lock points along the cylinder. All lock points are injection moulded Liquid Crystal Polymer (LCP) parts, and need to be attached accurately (within 50 μm) of their nominal locations. This process has been completed for a test sector, also shown in Figure 10.3.

All four cylinders have stave locking points installed upon them prior to their integration. These take the form of injection moulded LCP parts and are held in a row in a fixture that is then positioned accurately above the cylinder and the row of lock points is glued in place. Figure 10.3a shows a typical locking point and Figure 10.3b shows a prototype of the fixture gluing prototype locking points in place.

All four cylinders have a broadly similar design and are assembled in the same way with the only variations being allowances for the relative sizes of the cylinders. Once they are all built they need to be jigged together in their correct locations, ensuring their correct form

[1] Hysol EA9396

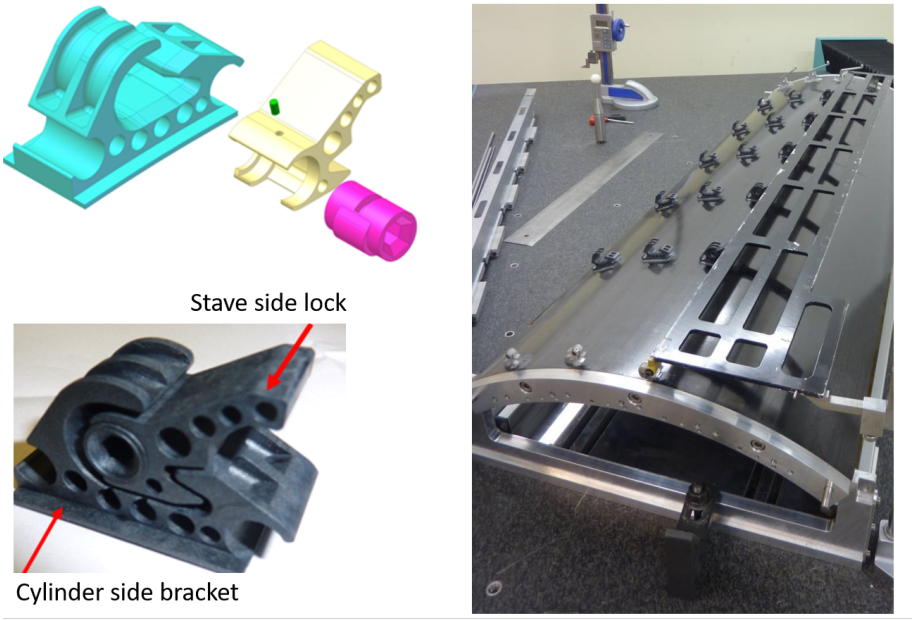


Figure 10.3: **Left:** CAD rendering and photograph of a barrel locking point. **Right:** Row of locking points on sector prototype.

(roundness) is maintained and that their correct positions (coaxiality) are set, allowing the interlinks to be assembled into place.

10.3.2 Barrel Cylinder Interlinks

The key properties of the interlink design are:

1. Demountable
2. One interlink per stave with a geometry where only one link need be removed to install or remove the stave behind it.
3. Interlink interfaces with no “droppable” fittings.
4. The interlink interfaces into the depth of the flange allowing a well-constrained interface to a flange made of moderately thin parts.

A drawing of the interlink is shown in Figure 10.4

The principal requirement on the interlink is that it has adequate stiffness to prevent the overall structure resonating at less than 7 Hz. This mode is not constrained by any structure other than the interlinks, so the interlink design is critical to achieving performance in this area. The function and operation of the interlink design is illustrated in Figure 10.5

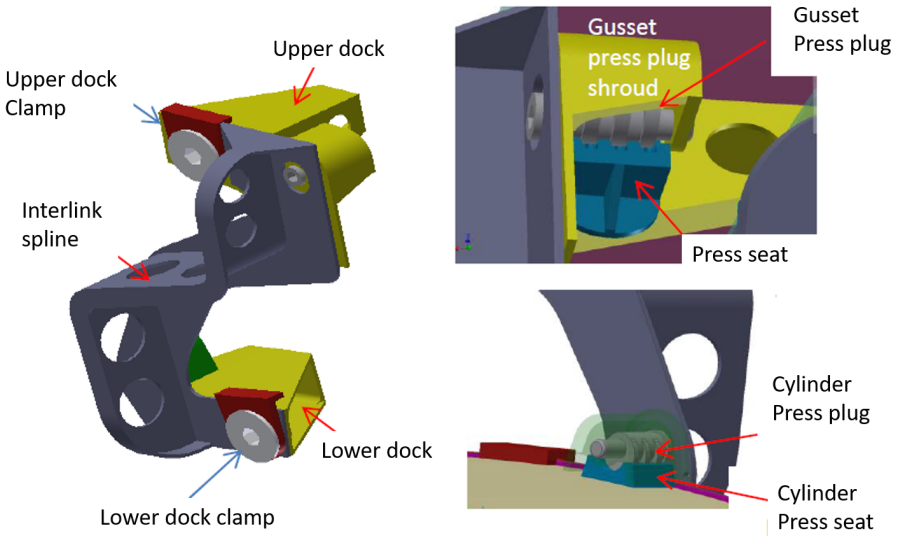


Figure 10.4: The parts of the barrel cylinder interlink.

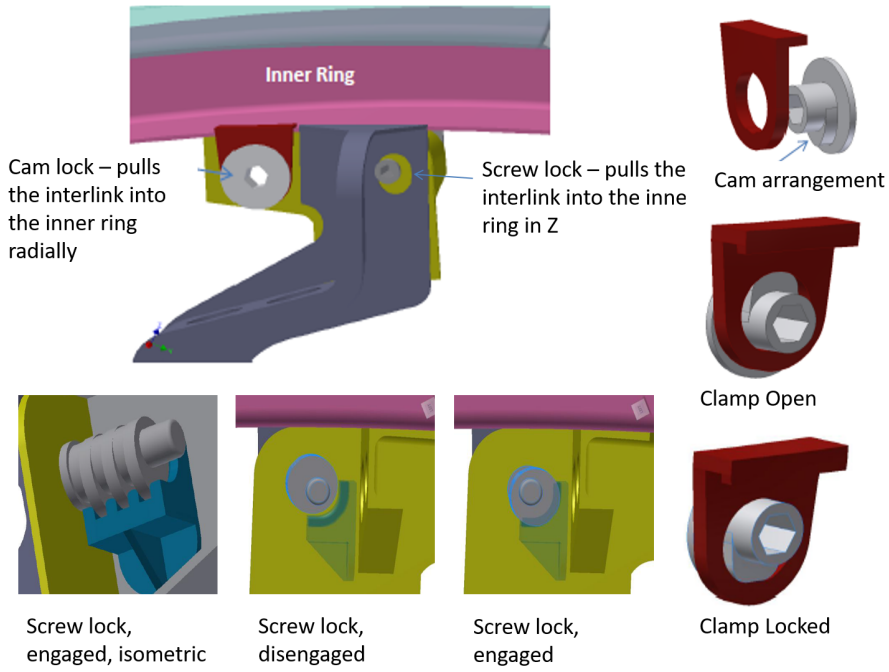


Figure 10.5: The interlink locking mechanism. Clockwise from top left: the "screw lock" used to pull the interlink into the flange ("Cam lock"); on the right had side: the Cam arrangement, in the disengaged position, half a turn later in the engaged position; lower left: in situ with support shroud; the radial retainer that pulls the interlink up onto the flange; two cylinders with flanges and gussets. The gussets stiffen the flanges and provide a ϕ location reference.

The biggest challenge is to ensure sufficiently rigid interfaces between the interlinks and the flanges. Assuming a single interlink per stave, they require a bending stiffness in the z direction of 203 N/mm over a 100 mm span. If they are rigidly enough connected to the flanges, then the first z mode of the barrel system meets the requirements.

The performance of the demountable flange-interlink mechanical interfaces dominates the overall interlink performance. To understand this better, a prototype has been built and is being explored by being loaded in various configurations and measuring its compliance.



Figure 10.6: Interlink prototype on CMM machine, Z compliance is measured by supporting the outermost “cylinder” and loading the innermost “cylinder”.

Figure 10.6 shows a picture of the setup. It should be noted that this prototype is made from lower-grade materials and thus never achieved the required stiffness and is instead intended to inform the next prototype. However, the results have already shown that the interface maintains a constant stiffness throughout its motion suggesting there is no slack in the mechanism.

10.3.3 FEA Design of Barrel Structure

The cost of the barrel structure is dominated by manufacturing considerations. Therefore the cylinder is designed as a series of components that work together to provide adequate performance. This allows working with vendors to iterate each components’ design without having to explore the full system FEA to look at the impact of every change.

The overall barrel system is modelled as four nested single-skin cylinders joined at either end by helical interlinks (see Figure 10.7). These have an "L" cross section (L beam) and map 1:1 onto the stave locations. A weight of 97 kg for the Pixel Detectors is located on either end of cylinder 0. It is assumed that all the Pixel Detector mass sits on the strip barrel and the Pixel Support Tube (PST) have zero bending stiffness. This is a conservative assumption. The barrel structure (and the Pixel Detector that it carries) are presently modelled to interface to the outer cylinder on four points only. This is assumed to be the worst case,

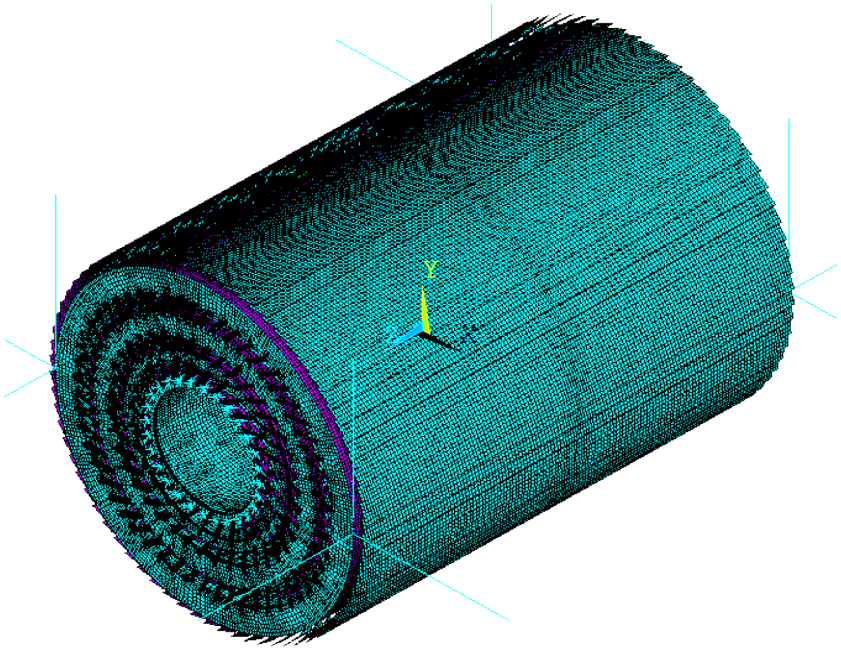


Figure 10.7: Barrel FEA model, shown with simple L beam interlinks and deep flanges.

and this interface is being explored. A continuous interface around the circumference of the outer cylinder (OC) is favoured.

System Performance:

The overall modes of the system can be seen in Figure 10.8. The results indicate that the stability requirements of 20 μm and 2 μm in the z direction and ϕ direction respectively are achieved (see Section 10.1).

It should be noted that the z motion and the $R\phi$ motion of the barrel structure are dependent on very different aspects of the structure and can be optimised independently. The z motion is controlled by the interlinks, the interlink coupling to the flange, the rigidity of the interface to the outer cylinder and the mass supported. The $R\phi$ motion is a function of the cylinder skin performance. The lowest $R\phi$ modes can be changed by either thickening the skins, or by adding stiffening rings. For the moment, the design is based around a single skin and further discussions with vendors to see whether the same performance can be achieved for no additional material and at lower cost with stiffening rings. The Pixel support tube in the present tracker is stiffened with stiffening rings.

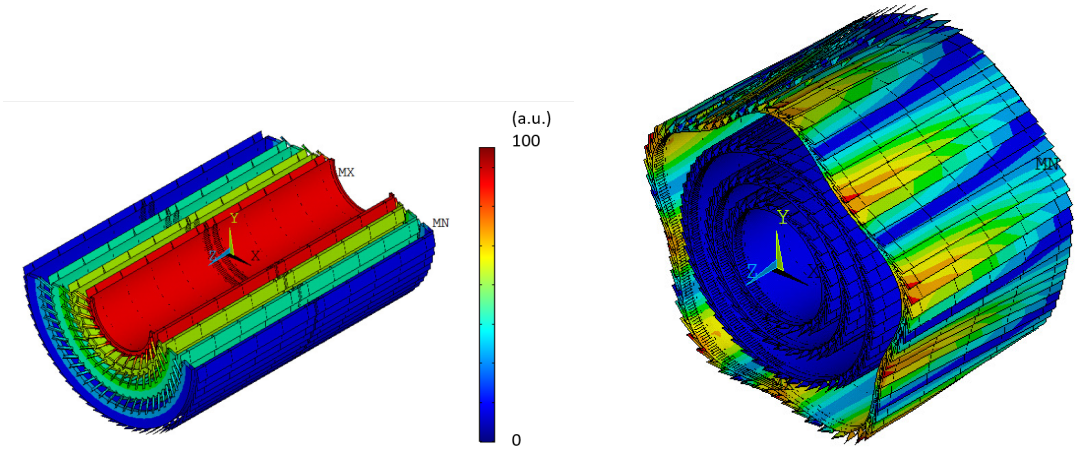


Figure 10.8: FEA model analysis of the barrel structure. The colour scales represent the relative movements of the 1st z mode with frequency of $\sim$7 Hz and the $R\phi$ mode with a frequency of $\sim$30 Hz.

10.3.4 Subsystem Performance

The performance of the modelled cylinders with the flanges is obtained for the two load scenarios shown in Figure 10.9. The results for all four cylinders are listed in Table 10.3. The performance obtained for this model provides the guideline for the final design and notably the fibre layup of the cylinders.

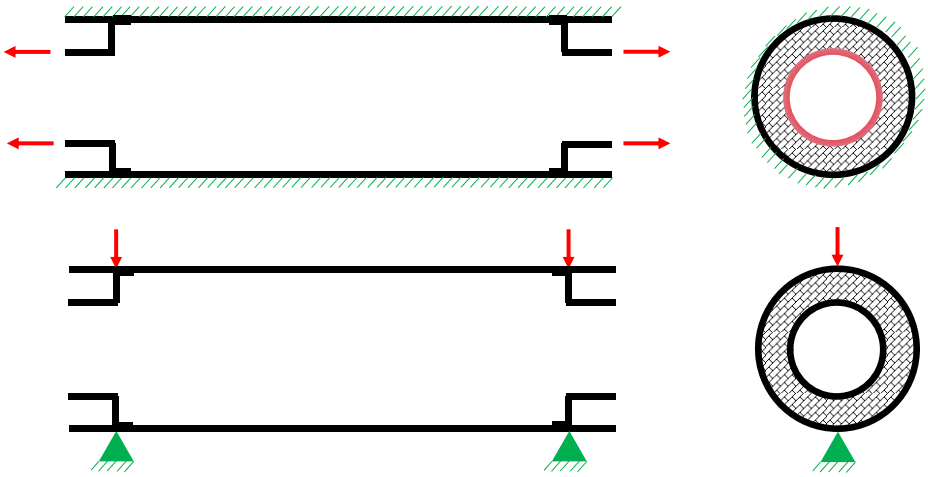


Figure 10.9: Diagrams describing the detailed load conditions in Table 10.3. Top image is axial stiffness load condition with cylinder skin constrained and flange inner wall pulled outward. Lower image is circular stiffness with full cylinder supported on two points and load placed diametrically opposite.

The interlink geometry as detailed in Section 10.3.2 is complex and under study using pro-

totypes. As the details of the interface dominates the performance, FEA results are not presented.

Table 10.3: Required flange stiffness in longitudinal and circumferential directions.

Cylinder and Flange Assembly	Axial Stiffness (Nmm^{-1})	Circular stiffness (Nmm^{-1})
Cylinder 0	16, 945	703
Cylinder 1	8, 420	587
Cylinder 2	875	2 175
Cylinder 3	725	1 527

10.4 End-Cap Structure

Once finished the end-cap structure consists of six disks on which the petals are mounted with the required initial accuracy of 100 μm. A drawing of the design is shown in Figure 10.10. The six disks are supported by an inner tube which provides the space for the ITk Pixel Detector. At the outer radii of the structure, the disks are connected with rods and service elements in the z direction and also attached to a so-called stiffening disk, to provide stiffness in the z direction. The stiffening disk is placed just outside the active tracking volume and the material budget of the other structural elements is kept low, while the structure's design avoids low-frequency vibration modes as required. The full end-cap structure is carried by the outer cylinder.

In this section, the elements of the end-cap structure are described in detail, followed by the assembly strategy and necessary set-up. The petal integration into the structure is discussed in Chapter 11.

10.4.1 End-Cap Disks

The petals for an end-cap disk are kinematically mounted onto carbon-fibre wheel structures. Figure 10.11 shows a drawing of a wheel consisting of two rings connected with eigth blade like structures. The wheels hold the petals in accurate positions, and they absorb mechanical stresses that may affect the petals in the in-plane direction, since the petals are attached kinematically to the structure. These stresses come from external vibrations during operation, from variations in temperature and humidity and, additionally, when the end-cap structure is transported, during the tracker integration, when the strip-detector end-cap is inserted in the outer cylinder and, finally, when the Pixel system is inserted.

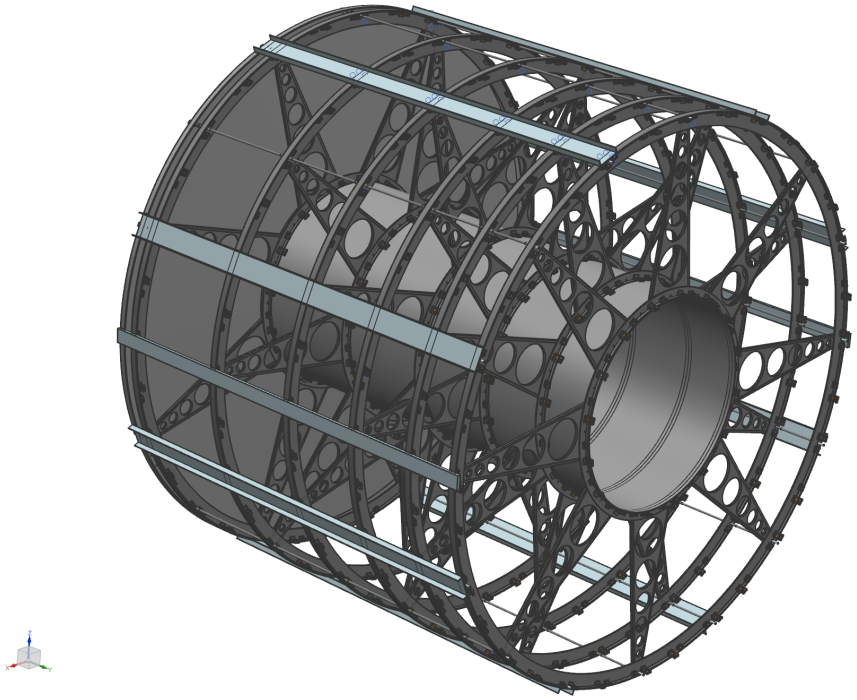


Figure 10.10: Drawing of the global structure of the end-cap, seen from the interaction point. The drawing contains the six disks of the end-cap. The stiffening disk can be seen behind the last disk.

Six wheels for each end-cap are prepared as individual structural elements that are combined into a larger mechanical super-structure at a later stage (see Chapter 18). Special attention has been given to ease the production without the need of an autoclave to accommodate this structure with a diameter larger than two meter. In addition, no thermal stresses are induced into the mechanical structure in this way. In this section, the constituents of a wheel are described. A wheel has an inner (outer) ring with a "T"-shaped profile. The flange has a radius of 37.1 cm (98.9 cm) and consists of carbon-fibre (Sigrafil c t50) with a long pot-life adhesive (Poxy-systems epoxy L harder W300) that matches the processing time of a few hours. To produce the rings, the carbon-fibre is wrapped around aluminium moulds that are designed such that both the base and the flange have the weave in the same direction, and are fabricated in one continuous process. A picture of the assembly of an outer ring is shown in Figure 10.12. Measurements on prototyped inner rings have shown that the roundness of the rings is within 30 μm, comfortably below our target of 100 μm.

The blades provide the rigidity to the wheel with the minimum possible mass. They have been conceived with two square profile tubes along the sides made of unidirectional carbon-fibre. The volume is filled with a sandwich of carbon-fibre honeycomb or carbon foam and covered with a carbon-fibre skin. A number of holes, of increasing size with the blade width, are cut-out in the sandwich to stay below our target of 0.2% X_0. The blade concept is

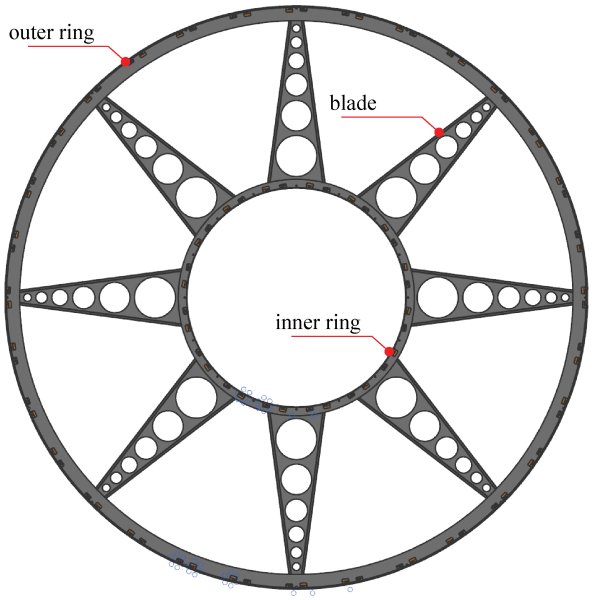


Figure 10.11: Drawing of an end-cap disk (without petals) consisting of two carbon-fibre rings with flanges that are connected with blades. Together, the blades form a star-shaped structure. The rings are equipped with precision locking points to which the petals are eventually mounted.

shown in Figure 10.13 where for clarity, the upper carbon-fibre skin and the core have been removed. The details of the carbon-fibre skins and size of the cut-outs are further optimised to reduce the amount of material without compromising the mechanical rigidity.

The blades are joined to the rims of the wheels using an adhesive[2)]. Since the blades have only a structural role, tolerances are not tight and the static and dynamic mechanical performance of the structure are inside specifications without using exotic carbon-fibres or cores. Blades are relatively easy and cheap to manufacture

The interface between the petals and the end-cap structure are the so called locking-points, which are part of the end-cap structure and define the initial precision of the tracker (see Figure 10.14). The locking-points consist of small pillars with a slider mechanism that hold the (on-petal) petal-locators described in Chapter 9. Note that a petal has three petal locators, each shaped differently to allow kinematic movement that avoids stress on the petal.

The main part of the locking-point is machined from Torlon[3)] as a small pillar with a relatively large base, 313 mm^2, to ensure a robust joint. Figure 10.14 (right) shows a locking-point that holds the petal-locator locked by a slider (PEEK machined), which is fixed with a small M3 bolt in addition.

[2] Heysel AE9396 Aero
[3] high performance thermoplastic material



Figure 10.12: Picture of the assembly of an outer ring. The picture shows a nearly finished ring in its mould.

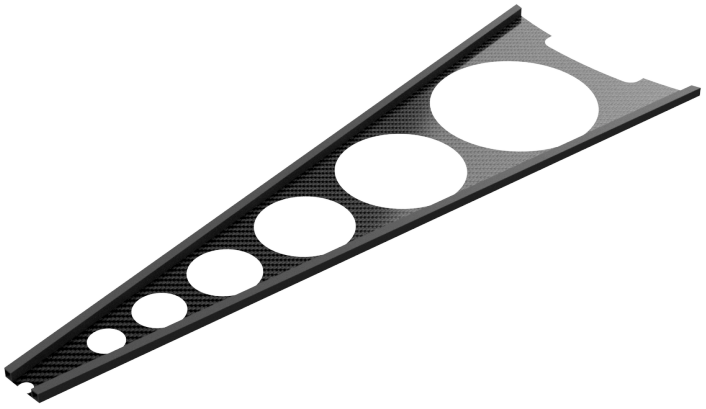


Figure 10.13: An end-cap blade with the top carbon-fibre skin removed for clarity. The picture shows the two rectangular beams and the sides and the carbon-fibre skin at the bottom.

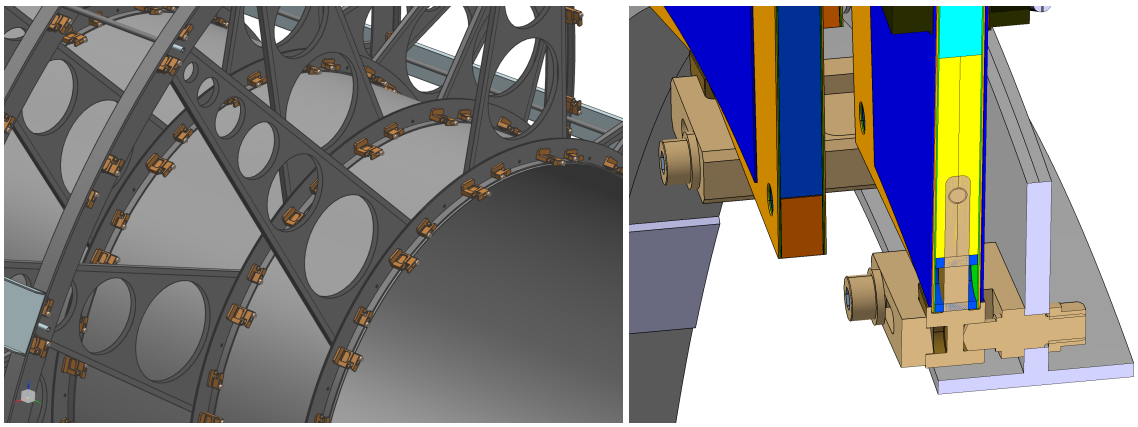


Figure 10.14: **Left**: The drawing shows the kinematic locking points on the inner and outer rims of the wheels. **Right**: Cut away view of the petal-locator and their connections to the locking-points at the inner rim of the wheel.

The locking-points are glued and bolted to the rims of the rings using a template to reach a high precision in $r\phi$ of 20 μm (expected), well below the required 100 μm. However, in the z direction, the base of the rings are not precise. Therefore, after the disk assembly, all the pillars of the locking-points are machined to their final "height and position" with an expected local precision of 20 μm. Note that the pillars in one disk are arranged on two z planes offset from one another by 15 mm to create the necessary overlaps of the petals.

A prototype disk structure is assembled to test the assembly strategy. The blades are glued to the bases of the rings with adhesive[4)]. A picture of this structure is shown in Figure 10.15.

10.4.2 End-Cap Inner Tube and Stiffening Disk

The inner tube of the end-cap constrains all disks and provides a gas barrier between the end-cap volume and the ITk Pixel Detector. It is designed to suppress rotations of the wheels around the z-axis and it defines the z locations of all the wheels. Since the inner-tube is located in front of the silicon sensors, it is essential to minimise its thickness. The current baseline design consists of three layers of carbon-fibre windings at -60, 0, and +60 degrees with a cyanate ester resin, resulting in a zero temperature expansion coefficient and a skin with isotropic mechanical behaviour. It is foreseen to produce the cylinder in industry.

The stiffening disk is attached to the inner tube, just outside the active detector volume as shown in Figure 10.16, close to the bulkhead. This disk provides stiffness in z to the end-cap and acts as a thermal barrier. Its thickness at the inner radius is 8 cm, decreasing to 2 cm

[4] Heysol AE9396 Aero

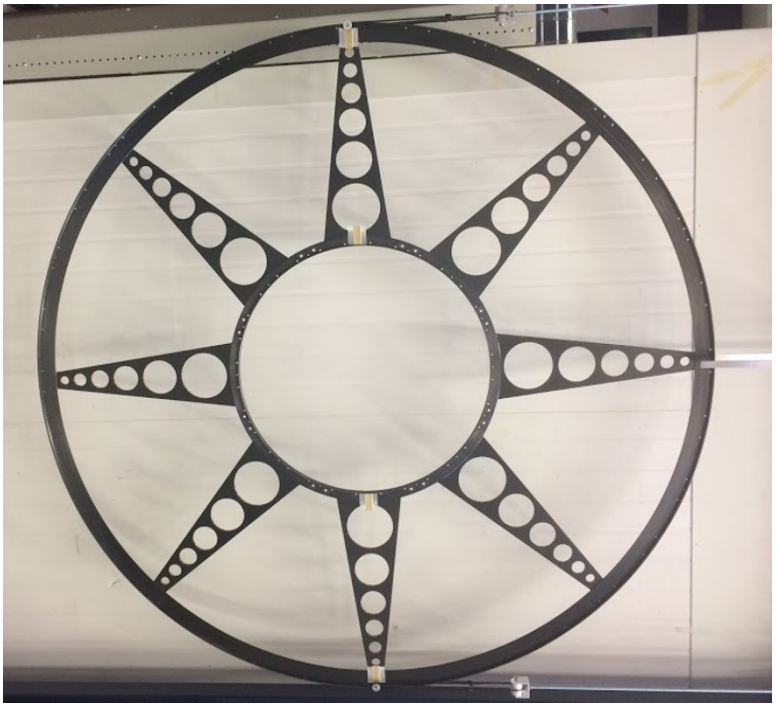


Figure 10.15: Picture of the first prototype disk structure.

at large radii, allowing for space for the routing of services. The design of the disk foresees making the skin of commercially available carbon-fibre sheets filled with a foam[5)].

10.4.3 End-Cap Rail System

The end-cap is supported inside the outer cylinder with a kinematic mounted rail system, which has a dual function: it is required to insert the system in the outer cylinder, and, during operation to enable some long-term mechanical deformations, typically less than 1 mm. Figure 10.17 shows a drawing of the end-cap rail system, which comprises stainless steel rollers attached to the end-cap that run over a profile, attached to the outer cylinder. The four rollers are attached toward the outer ends of two beams at 3 o'clock and 9 o'clock of the end-cap. The two rollers near the stiffening-disk are fixed in z after insertion of the end-cap. The rollers on the left side (negative x) run over a flat strip, which is part of the outer-cylinder. Additional movement in the y direction, especially during insertion, is required. The baseline solution features a spring-loaded suspension of one of the rollers that is fixed after installation, but has not been worked out yet. The present idea for the rollers, or set of rollers, is a commercial solution with mechanical adjustments. The materials of available systems have to be carefully checked to ensure the absence of magnetic components.

[5] Rohacell 110A

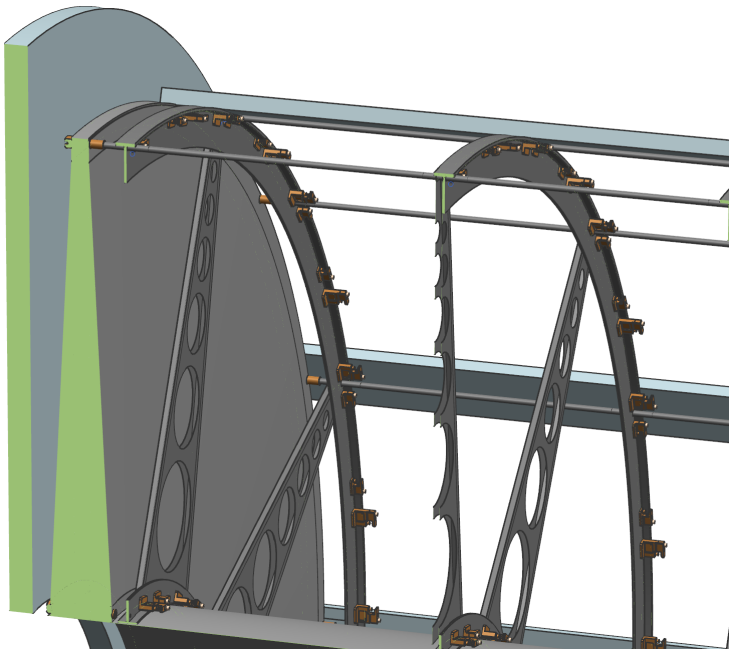


Figure 10.16: Drawing of the stiffening disk, located between the bulkhead and the sixth wheel. After transport, all the connections to the bulkhead are loosened, except the kinematically mounted services. In this situation, the disk provides the z-stiffness of the end-cap and acts as a thermal barrier. Near its connection with the inner cylinder, the disk has maximal thickness and becomes thinner, going radially outward.

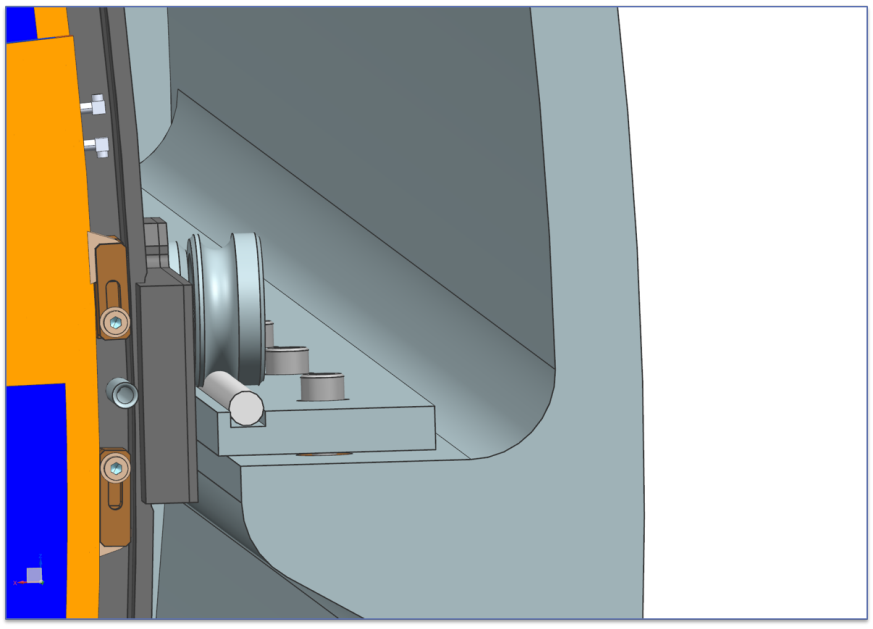


Figure 10.17: End-cap rail system at the side that constrains the x direction.

10.4.4 Results of FEA for the End-Cap Structure

For the initial structural analysis of the end-cap, a modelling software[6)] has been utilised. To model the structure, several simplifications have to be made, notably:

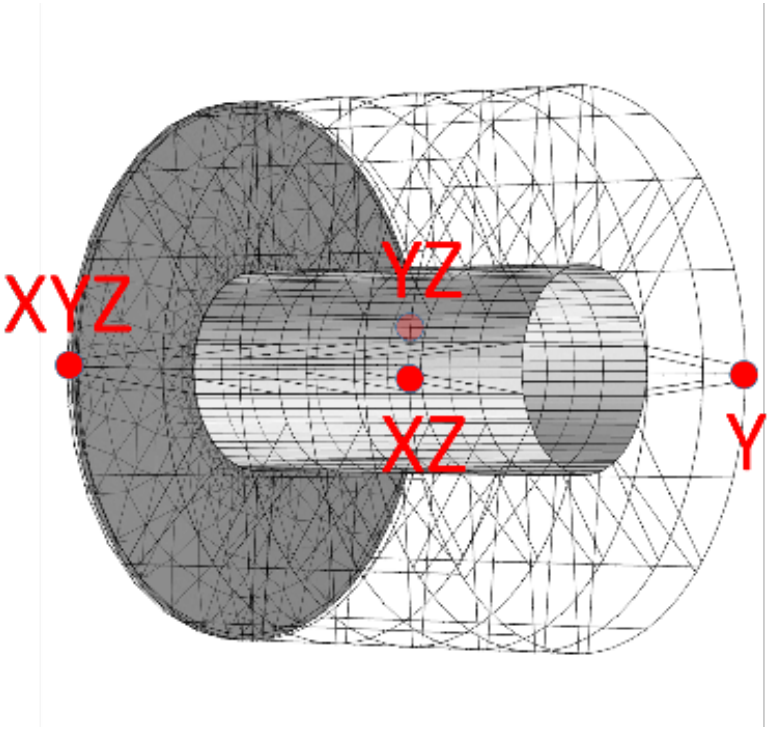


Figure 10.18: The used mesh for the FEA on one end-cap with the bulkhead on the left side.

1. All elementary connections within the system are simulated as fully fixed nodal connections;
2. The petals are simulated as added mass on the locations of their respective locking points;
3. The piping and cabling of the system is simulated purely as added mass;
4. The stiffness of the "outer world" supporting the end-cap is modelled as infinitely stiff.

The modelled system is slightly over constrained, with two constraints mounted on the stiffening disk, and two constraints on the front petal supporting wheel as shown in Figure 10.18 together with the mesh which is used. The mesh is obtained after additional refinements became insignificant for the results presented here. Figure 10.19 shows the expected gravitational sag which is up to 70 μm- this is comfortably small.

[6] Comsol Multiphysics

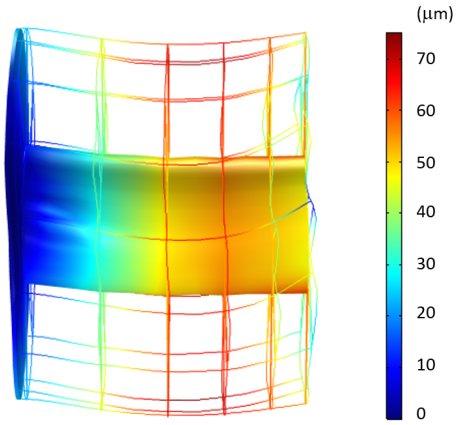


Figure 10.19: Results of the gravitational sag analysis. The colour scale also shown.

The vibration modes are studied in detail. Figure 10.20 shows the vibration mode in the x direction, the x-sway. This mode affects the important ϕ direction, but has an eigenfrequency of 42 Hz, sufficiently above the required 32 Hz. This corresponds to a stability in the ϕ direction of 2 μm (see Table 10.1). Other modes have all higher eigenfrequencies, such as the z-telescoping and ϕ-twist, which have frequencies of 49 Hz and 50 Hz respectively.

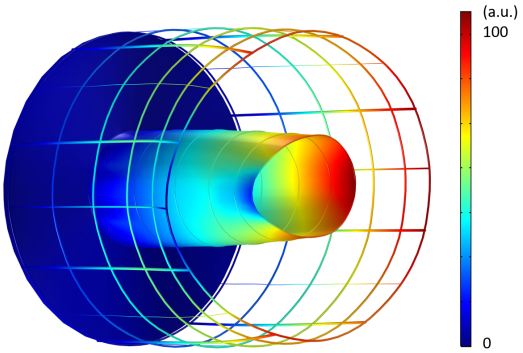


Figure 10.20: Results of the modal analysis for the specific vibration in the x direction. The blue colour indicate zero movement, while the red coloured lines represent the maximal movement with an arbitrary magnitude. This mode has an eigenfrequency of 42 Hz.

10.4.5 End-Cap Assembly Procedure

The mechanical super-structure for the assembly of the ITk end-cap contains the stiffener disk together with the inner cylinder and the carbon-fibre wheels that hold the petals. This structure will be pre-assembled and ready together with all the services in order to avoid delicate operations near sensing elements. The super-structure is designed such that the precision locking points for the petals are referenced during the assembly procedure,

thereby eliminating cumulative systematic uncertainties in the positioning of the petals that are otherwise introduced by sequential stacking of the wheels.

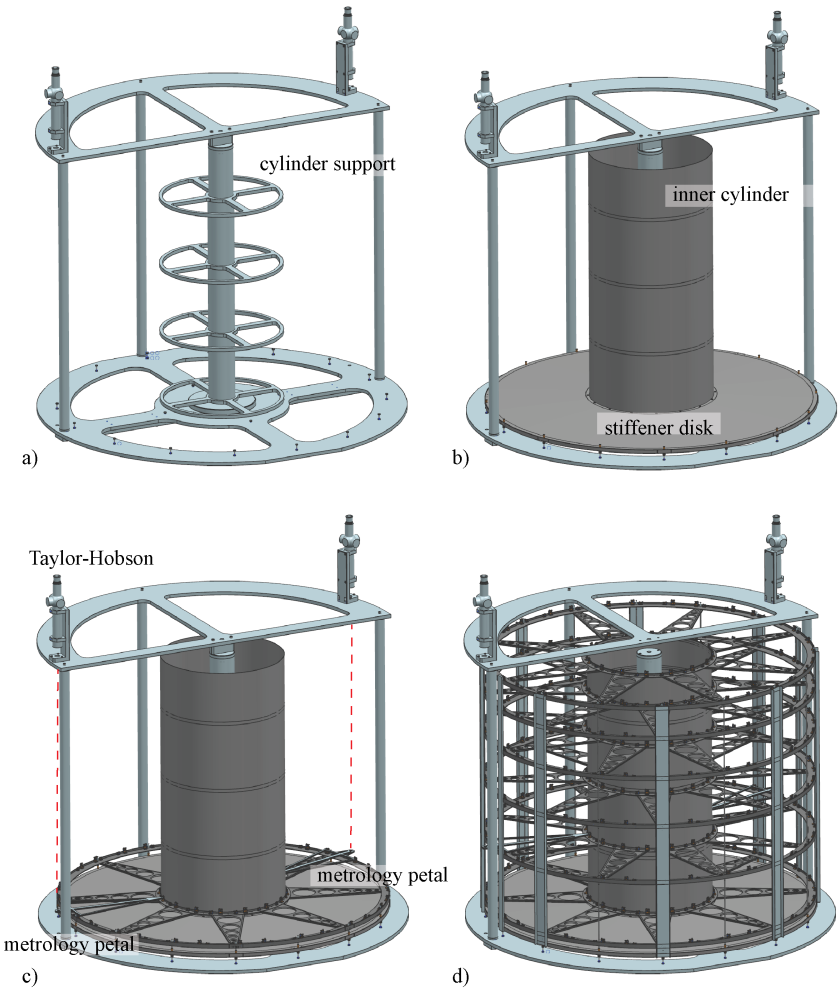


Figure 10.21: a) End-Cap assembly tool. b) First step is to install the stiffening disk together with the inner cylinder. c) Mounting of the first wheel and alignment with the Taylor-Hobson metrology system. d) The finished mechanical super-structure with six wheels and the service trays and carbon-fibre mounting bars installed.

In Figure 10.21 a, the main assembly tool for the super-structure assembly procedure is shown. As a first step, the stiffening-disk and the inner cylinder are connected with the inner cylinder in the vertical position held by the aluminium cylinder support rings. The key step is to align the axis of the inner cylinder to the z-axis of the coordinate system with a tolerance of 0.5 mm, which is necessary to allow the wheels to be inserted without interfering with the cylinder. The stiffening disk is mounted to the inner cylinder and once it is attached it defines the $R - \phi$ positioning of all wheels, as shown in Figure 10.21 b. Then carbon-fibre reinforced polymer (CFRP) spacing tubes are attached to the stiffening

disk as well at defined locations in $R-\phi$. With an alignment system, the height of the spacers is measured, and afterwards the spacers are trimmed with 50 μm precision in order to form one single plane in z that can hold the first wheel, a strategy that is similar to the one adopted for the disks made for SCT end-cap.

The wheel is slid over the cylinder onto the spacing tubes with two specially designed metrology-petals which are connected to two of the real petal insert locations as is shown in Figure 10.21 c. On these metrology-petals, alignment markers are visible with a well-defined position with respect to the petal mounting points. Our baseline strategy for positioning the wheels is to use a Taylor-Hobson metrology system for precise positioning in $R-\phi$, while more expensive alternatives such as laser alignment systems have to be used if the required precision can not be achieved in this way. With the wheel in the correct location both in z and $R-\phi$, the glue already on the spacers is allowed to cure, while epoxy wetted shims are inserted between the inner cylinder and the wheel to make a solid connection at low radius. During the full disk insertion procedure, the position of the wheel in $R-\phi$ is continuously monitored allowing for fine-adjustment during the assembly.

The mounting procedure is repeated for the other wheels. Each time the spacers for the z-position are trimmed after metrology, and the $R-\phi$ alignment is achieved each time with the Taylor-Hobson system. Once all six wheels are mounted in the structure, carbon-fibre trays are attached to the structure that holds the petal services. Besides holding the services, the trays are a structural element of the super-structure, providing z-stiffness. At this stage two carbon-fibre bars are attached at $\phi = 0^\circ$ and $\phi = 180^\circ$ along the full length of the structure. These connect the wheel-based kinematic mounting system to the ITk outer cylinder (see Figure 10.21 d).

As a final step, the bulkhead is attached to the super-structure. The finished product is then ready for mounting of the petal services, before the actual petal mounting and transportation to CERN.

The end-caps will be assembled at external sites in frames which will also serve as transportation frames when being transported to CERN. Those frames need to be placed in shock-absorbing transport boxes and then be transported with a special transport to CERN. The design of the transport box is ongoing and will benefit from the experience of the SCT transport, which also used a truck with air suspension. It is also foreseen to use the same frame during the testing at CERN and possibly during the installation of the end-caps in the ITk volume.

11 Integration of the ITk Strips

This chapter describes the process of assembling the ITk Strip subsystem from the constituent parts. Generally the process is independent of the location of the activities, but the intent is that the barrel is integrated at CERN and the end-caps at end-cap assembly sites outside of CERN. This section covers both the process of assembly and describes the design and function of the service modules. The thermo-mechanical performance of the service module is also described.

11.1 Barrel Integration

The barrel has all the staves end inserted once the barrel structure is fully assembled in the outer cylinder (OC). The OC is assumed to be sitting in a cradle and it is assumed that access into the bore of the OC for two at once is possible. Furthermore, it is presumed that the population of the barrel region from both ends simultaneously is possible.

Assembly of Structures

The barrel structure is based around four carbon-fibre reinforced polymer (CFRP) cylinders linked together at either end by many interlinks (Figure 11.1). The interlinks provide multiple functions as described in Chapter 10, but for the assembly the critical function is supporting and maintaining the separation of the barrel cylinders. To assemble the barrel structure the outermost of the four cylinders is held in a cradle, the penultimate cylinder is then positioned within this on a spindle, and the outermost layer of interlinks is installed, these are mechanically locked in place to the two cylinders. When all the interlinks are connected the spindle support can be removed. This process can then be repeated with the other two layers.

Once the four-layer barrel is assembled and inspected it can be inserted into and attached to the outer cylinder. When the barrel structure is installed within the outer cylinder the staves can be installed and connected.

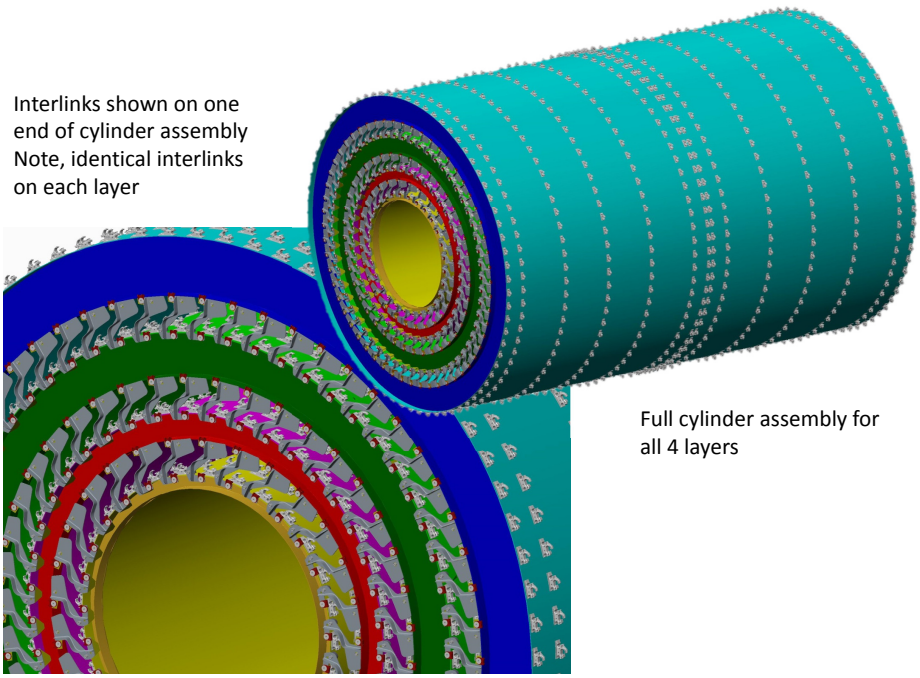


Figure 11.1: Barrel structure, all interlinks are shown in place. This configuration would exist just before the barrel structure is slid inside the outer cylinder.

Insertion of Staves into Barrel Structures

The staves are inserted into the fully assembled cylinder structure from the ends. This is done by the removal of an individual interlink, the insertion of temporary rails, fitting of an insertion frame, and then the sliding of the stave along the temporary rails. This work is detailed in Ref. [93] and the insertion process is summarised in Figure 11.2. Once the stave is inserted it is locked, the frame removed, the rails removed and the interlink reinstated. The insertion can then progress to the next stave.

Figure 11.2 shows the process of inserting staves on to the cylinders. The images are all taken from a series of prototypes and the lessons learned through this process have resulted in minor geometry changes. The insertion uses a dedicated fixture that can be used in the outer cylinder to support the stave in its transport frame to facilitate the insertion, an early demonstrator of this is shown on the bottom right. Figure 11.3 shows the prototype transport frame. The transport frame is designed to be low cost (one per stave) and to allow the stave to be slid in and out from the Z=0 end of the transport frame. This allows the stave to be slid from the transport frame into the tracker.

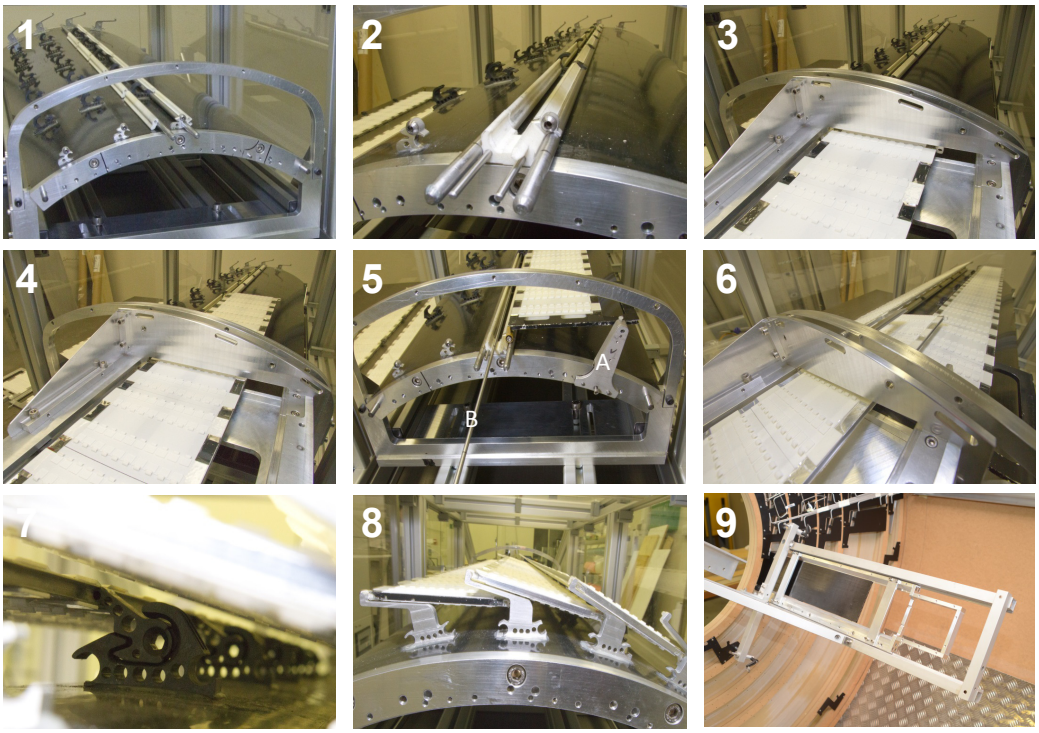


Figure 11.2: Assembling staves to cylinders - from top left; 1) rails in place ready for stave insertion; 2) rails locked; 3) offer up stave frame (prototype shown); 4) slide in stave; 5) add interlink (A, non representative piece shown), lock (B); 6) insert multiple staves; 7) engaged and locked lock point; 8) Z=0 lock point; 9) very early prototype frame shown in situ.

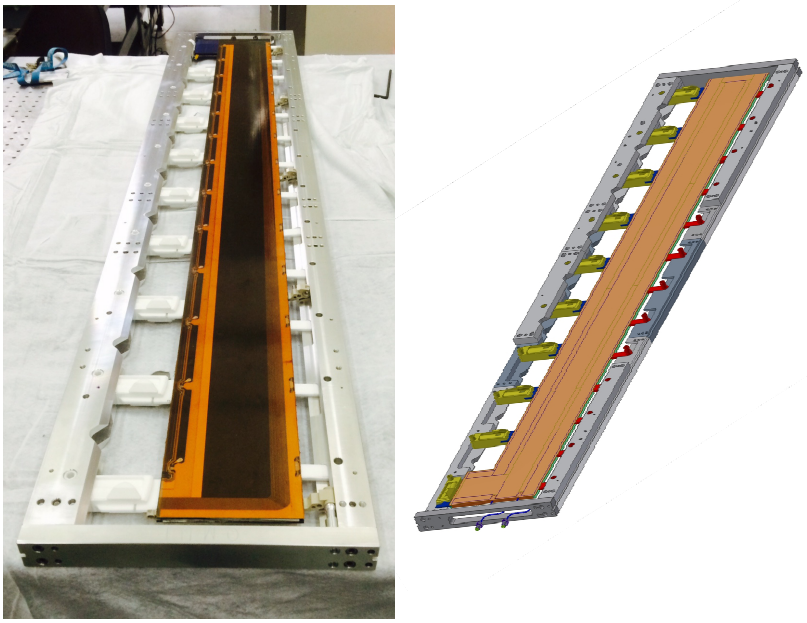


Figure 11.3: Stave transport frame.

Servicing of Barrel Staves

Once the staves are installed in the outer cylinder they need to be connected to the services. The services are pre-fabricated in Service Module (SM) units that serve eight staves (see Section 11.4). The Service Module is offered up to the outer cylinder wall and attached in place (it is attached in two places z ≈3.5 m and ≈1.5 m) with gas, thermal, and ESD seals being made where services penetrate the tracker volume. The services can now be connected to the staves they serve.

Three connections have to be made to every stave as shown in Figure 11.4. These will be made in the following order:

1. Cooling: each stave needs one inlet and one coolant exhaust, these are manifolded together with pipes from other staves reducing the number of inlet and exhaust lines that penetrate the tracker volume. Naturally this increases the impact in the case of problems. Each pair of inlet and exhaust lines needs two welds to attach the stave to the prefabricated SM.
   The order and process of stave connection is complex, with a clear need to back gas [1)] the welds with Argon throughout the welding. This is compounded by the fact that as more connections are made joining staves to manifolds the network of interconnected pipes grows, and the system becomes harder to purge with argon this makes it harder to ensure the purity of the gas inside a weld, and thus the risk of weld failure due to oxygen contaminated argon.

2. Electrical: this connection is done with a single mixed type D click connector that plugs into a mating connector supported on the corresponding interlink. The connector carries the high and low voltages and the DSC lines. The "D Click" connector is a tool and screw free positive lock connector.

3. Optical: the optical fibres are connected last as they are fragile. Each stave side needs data in and out (minimum of four fibres per stave), and the short-strip staves need an additional two data out fibres to cope with the data throughput. If the final stave has four fibres per stave these will probably be individual standard telecom fibre connectors (MTP), but should the stave have six then the ribboned approach will be used. Connection of either individual fibres or six-way ribbons will be done using standard telecommunications connector technologies with proven track records of robustness and reliability.

[1] TIG welding on the thin wall Titanium pipes requires the arc to be struck in an inert atmosphere, for this to be possible the pipe needs to be filled with inert gas (here Argon), as well as the electrode to be shrouded in Argon.

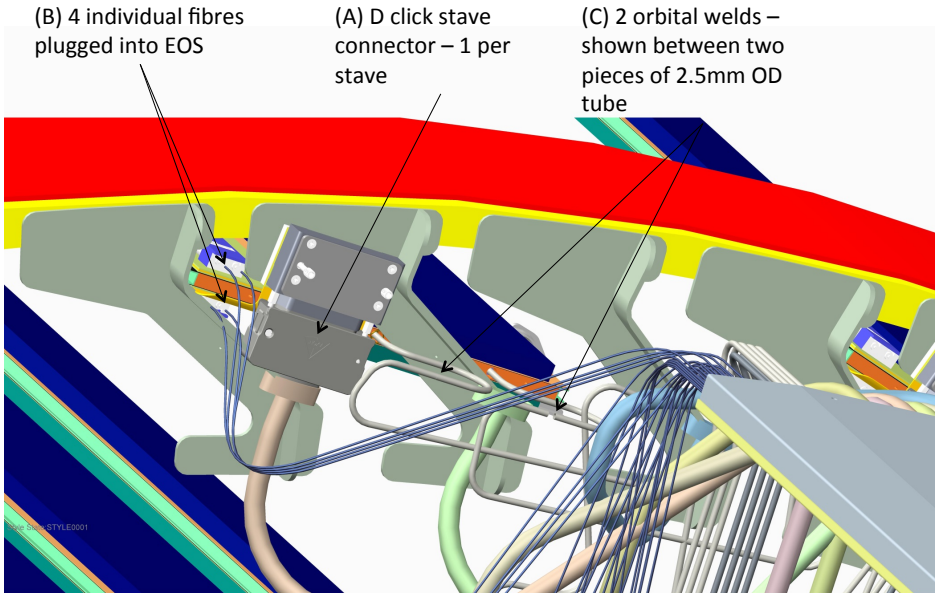


Figure 11.4: Making the SM connections, C) 2 welds made in situ; A) D click electrical connection - 1 per stave; B) connection of optical services - shown as 4 fibres, but may be done as single ribbon. Note, for clarity no cylinders, and the neighbouring staves are also not shown.

11.2 End-Cap Integration

The end-cap integration and servicing has a lot in common with the barrel. Hence, in areas where the two sub detectors use the same methodology this is stated and cross referenced. By contrast, where the sub detectors are different the end-cap solution is fully described.

The (empty) end-cap structure is placed in a support frame with the beam axis pointing up as shown in 11.5. This position is regarded as most practical and safe for the delicate petal mounting, but has the drawback that connections to the patch-panels at the Bulkhead are difficult to reach. The petals are installed disk by disk and connected to the corresponding cooling manifolds. The petals are also connected to the pre-installed service modules to enable tests of each full disk during the insertion process.

Insertion of Petals in to End-Cap Structures

The end-cap petals are to be inserted radially into the end-cap structure. Partial rotations of the petal over its length axis are necessary during insertion as well as a final translation in ϕ to reach behind service trays. Tooling is required to support the petals during installation, as they by contrast to the barrel they do not have rails to guide them in to place. Figure 11.5 illustrates the insertion of a petal. The petal is handled with a temporary protective cover and placed into its locking points, described in Section 10.4.1 . For the inner radius a tool is required to fix the locking point. It should be noted that the baseline handling strategy

relies mainly on craftsmanship. However, a mock-up of the end-cap set-up will be made. Whenever the risk of damaging a petal can not be excluded, additional automated handling tools need to be designed.

Servicing of End-Cap Petals

Once the petals are inserted they need to be connected to the service modules. As with the staves three connections are needed (cooling, electrical and optical). These are made in a similar way to the barrel. The strategy for connecting the cooling services is optimised for the end-cap structure. Figure 11.5 shows the routing of the cooling pipes and their connections to the petals. The main differences with barrel are:

1. Cooling pipes have formable ends. To allow for the small amount of radial space available the cooling pipes attached to the petal have formable ends which avoid the need for the cooling pipes to exit the petal within the active volume and then to be connected to services in front of the silicon sensors. This is done with helical grooved pipes attached at the ends of the petal cooling loop. These ends are manipulated once the petal has been installed so the pipes are co-axial to the end-cap and abutted to the pre-installed cooling tubes with an orbital weld preparation.

2. Capillaries. The capillaries are going to be coiled in close vicinity to the wheels. Unlike the barrel there is no long straight section of service module available for all the inlet pipes/capillaries. To allow a constant approach all the capillaries will be coiled near the wheels allowing their flexibility to be used to make easy connections to the disks.

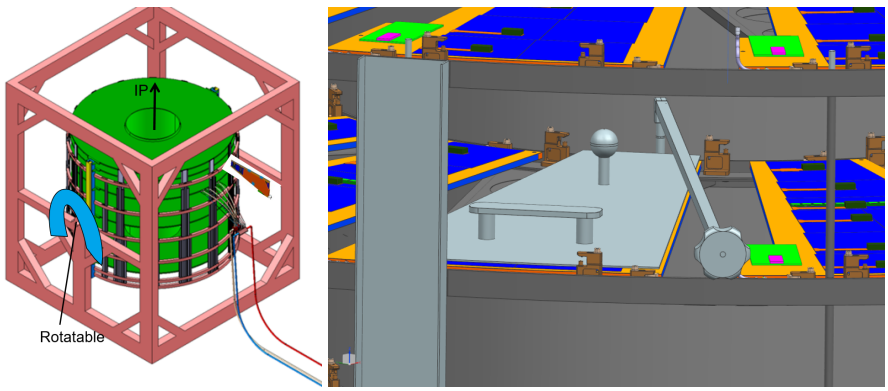


Figure 11.5: **Left:** Drawing of the support frame for integration of the petals. The frame holds the Bulkhead to which the end-cap structure is connected. The end-cap axis is pointing up and the petals are inserted radially. **Right:** Illustration of an end-cap petal insertion. Shown is the petal covered with a protective handling shield to put the petal into its locking points. A special tool that is required to fix the lock at the inner radius, is also shown.

11.3 Testing during Integration

As the ITk is assembled the parts of the system installed first become progressively harder to access. This means that any remedial work becomes more difficult and slower. To minimise the risk of such problems the strip barrel integration sequence intends to "close" the tracker volume periodically to do partial testing of the installed system. The expectation is that the outer cylinder will have both ends closed either with a dummy gas tight structural bulkhead, or a gas tight membrane. The tracker volume would then be purged with dry Nitrogen and the dew point driven down to allow safe running of the cooling system without the risk of condensation. The specific testing plan is still under development as the optimal testing regime has to carefully balance the schedule impact of testing against the risks of damage to the system from the testing, the risk of not finding faults and the resources available. It is planned to test in increasing steps, following installation of 1,2,4,8,16, and then all 48 service modules. This test pattern is provisional and based on the idea that the connection process will be optimised reducing the need for rework over time. Should the early stage testing reveal problems this process will be refined reducing the number of additions between testing.

11.3.1 Barrel Test at Surface Building SR1

Full system tests of the Strip tracker barrel will take place at CERN in the SR1 facility (see Chapter 21). An extension of this facility is being prepared for these tests in order to accommodate the complete Strip barrel, which is about three metres long. In addition, services are installed, including a cooling plant, powering of the staves, read-out and detector control systems.

The electrical system tests are aimed at characterising the noise performance of the modules. The conditions in which these tests are carried out should be as close as possible to the tracker in the cavern. These include the cooling fluid and temperature, humidity, environmental noise, data rates and read-out hardware, firmware and software. Also, grounding and shielding should be as close as possible to the final system configuration. The tests include:

- Equivalent Noise Charge (ENC) measurements, recording the input noise in electrons. Bias voltage scans at operation temperature are performed for comparison with the installed detector, and to study the evolution as it is operated in the radiation environment.
- Noise Occupancy (NO) tests.
- Double Trigger Noise (DTN) tests to measure the susceptibility of the setup to electrical noise pickup. The addition of modules to larger structures and multiple layers may increase noise.

- Cosmic data taking. With these tests, the triggering and the read-out can be tested in the intended operation mode when the tracker is installed. The trigger is taken from scintillators and photo-multipliers in coincidence, also allowing for an initial alignment and efficiency measurement. The barrel can be tested with a selected area in the way it was done for the SCT and TRT [94]. In addition, the whole tracker can be tested using sufficiently large scintillators.

All testing in SR1 for which grounding and cross talk are important is done within the outer cylinder and to do these tests the outer cylinder needs to be closed, and in this closure the Faraday gauge must be closed to represent the complete ITk.

When the tracker is closed for testing it is expected that the staves have their full functionality tested. This is not a long term or a burn in test, which at that time would have happened already. Instead, the aim is to demonstrate that nothing unexpected has happened to a specific stave during its installation that could inhibit its long term use. As each of these tests is in an active work area it is possible that damage could happen after the stave is initially tested in situ. It is believed the risk of this is low, but, that once the tracker is fully assembled a final test of all staves should be performed. This final test will be technically challenging as there will be inadequate infrastructure available to do it all at once, requiring a large number of service connections and disconnection and a great deal of care in the mapping. It is planned to provide enough infrastructure to test at least three service modules simultaneously requiring up to 16 service connection and disconnection operations.

11.3.2 End-Cap Test

Each of the two end-caps will be assembled at two external sites, where they will also undergo tests. The electrical tests are the same as those for the barrel, with the only additional consideration of a different power and read-out architecture. In the petals, the power and read-out lines run along the same side, which means the influence of nearby petals has to be assessed. This test is prior to the full end-cap test, which will serve to assess the performance of the system when multiple disks are operated simultaneously.

Trigger tests and data taking with cosmic tracks for both end-caps are a possibility since both are assembled and tested at two different sites:

- Electrical Interference
- Trigger tests
- Grounding & shielding
- Operation

11.3.3 End-Cap Tests during Integration

The strip end-cap integration takes place mostly at the macro-assembly sites and is therefore fundamentally different from the barrel system. The first step is the reception testing of all components that arrive at the macro-assembly sites. All cables are tested for continuity and for shorts, the optical fibres are tested for continuity and the cooling tubes are tested for leaks. In addition it is envisaged to immediately test the petals when arriving at the macro-assembly sites. The key objectives are first to ensure good quality components enter the assembly line, and secondly to have a short turn around for errors in the supply line.

Before the petal mounting we intend to mount all the services to the end-cap mechanical support, followed by an extensive testing programme. The same tests as for the component reception are repeated, and in addition it is foreseen to do a few thermal cycles per wheel. During such test our plan is to operate a realistic CO2 cooling system, and to dress the petal mounts with dummy heat-loads petals. These dummy petals should verify the working of all the services to a petal, including the optical fibres.

Once the services have been installed and tested on each of the wheels, the system is ready to start with the petal mounting. The petals are mounted in a staggered structure to ensure overlap between neighbouring petals, and it is safest to start the mounting with the low-lying petals on a wheel. Once the low-lying petals are mounted, a full functionality test will be done on each single petal. The same testing procedure will be executed once the high-lying petals are mounted.

A completely finished wheel undergoes a system test in which large sections of one wheel are tested simultaneously. At the time of writing this report it is not yet known what segmentation will be chosen for such a test. In principle it would be best to test one wheel as one unit, but given the amount of infrastructure needed (power supplies, DAQ, cooling) it is likely that testing will be limited to one quadrant at a time. Special attention will be paid at this stage of the integration to common mode noise, and other sources of interference between petals. In addition to the segment tests, simultaneous tests are planned for a small number of petals on adjacent disks to investigate cross-talk between wheels.

The final step of the integration will be the installation of the strip end-caps inside the support tube. This will happen only once the barrel and end-caps are fully tested and will result in the tracker volume being permanently closed. The step will be much less complicated than the integration of the barrel detector as each end-cap is installed as a single unit. There will be no disconnection and reconnection of any cables, optical fibres or cooling pipes inside the active volume of the detector the end-caps have all connections fixed to the end-cap endplate which is already attached to the mechanical superstructure before petal mounting takes place. The installation and closure of the ITk volume is the very last part of the ITk Strip Detector construction and should be followed by the pixel insertion and then the surface characterisation of the detector.

11.3.4 Test of Cooling Pipes

Each individual part of the pipe work needs to be tested as it is assembled. The Pressure Equipment Directive (PED) [95] is used as a guideline to determine test pressure and procedures, resulting in a test pressure of 186 bar. As the system is assembled each service module and the associated staves are pressure and leak tested. The pressure test aims at detecting gross failures, and the leak test ensures that the system has a high enough integrity that a minimal amount of working fluid is lost during operation. The leak test requirement is that a service module should not show a helium leak under vacuum leak test conditions of more than 10^{-6} mbar l/s. It should be noted that a leak rate at this level is far stricter than any sensible working fluid loss limit. It is instead defined by the experience that shows that leak rates above this level tend to occur due to inadequate care being taken in the preparation and build process.

11.3.5 Laboratory Requirements for the System Tests

All system tests from single stave or petal tests at the production sites to the full system tests at CERN it is desirable that power supplies, sensor bias sources, read-out hardware and the overall grounding and shielding should be common with that used during the earlier assembly stages. In all sites, clean rooms classified as ISO 7[2)] or better with temperature stability of $0.5°C$ and humidity control of $\pm 10\%$ should be part of the basic infrastructure. For the data taking with cosmic rays, the sites shall implement a large enough system with scintillators and photo-multipliers, together with the whole DAQ system. In all cases, control systems monitoring the power supplies, sensor leakage currents, humidity and temperature are required. Interlocks are needed in order to operate the systems safely both for personnel and modules. Test sites also require an adequate cooling system to operate the larger items under test at the design temperature.

The ITk will be integrated in the surface building at Point-1. This building was used for the integration of the ATLAS Inner Detector (ID) in 2003-2005. For the ID a limited amount of space for maintenance and development of test structures is required up to the end of Run 3 in 2023. The remained building will be refurbished before 2018 for the ITk integration extending the footprint from 408 m^2 to 508 m^2. In addition there is a large controlled radiation area of 200 m^2.

11.3.6 Cold Testing during Integration

During HL-LHC running the ITk Strip Detector will be operated at cold temperatures (in the range between -20 and $-35°C$) by means of evaporative dual-phase CO_2 cooling. Therefore it is important to test assemblies during pre-production and production at low

[2] Class 10000 equivalent

temperatures. The development of the methods is under way; here the preliminary plans are presented.

The staves and petals assembled during pre-production will be cold qualified at around $-20°C$. This does not necessarily need to be performed with evaporative CO_2. Other alternatives are being investigated, such as the use of chillers and pumps circulating HFE7100 (Methoxyperfluorobutane) fluid. Apart from understanding the thermal behaviour of the structures, this qualification will also make it possible to obtain benchmark noise values for the staves and petals at operating temperatures. Development of the method for this qualification has already started. During production, every single stave and petal will be tested at $-35°C$ at the stave and petal assembly sites and/or at the end-cap integration sites. The later test is foreseen to assure that the cooling pipes are not damaged during assembly and will not necessarily be done at very low temperatures. At some point during assembly or integration, petals and staves will all be tested cold, but the exact timing will vary from object to object. The integration structures will not specifically be cold tested at any point apart from inadvertently when the electronics might be cold tested. It is reasonable to expect that the structures will not reach their operating conditions until the ITk is running underground.

System Cold Test

The ITk Strip barrel and end-caps will be tested at low temperatures before the installation in ATLAS. They will have different build testing regimes as the barrel is integrated directly at CERN while the end-caps are integrated at the assembly sites. For these tests, cold boxes are mandatory to control the temperature and humidity. Either separate cold boxes or, for the barrel, the outer cylinder, can be used for this. In order to test the barrel at low temperatures, the outer cylinder will need to be closed. That will stop all work in the outer cylinder on both ends and thus needs to minimise the number of cold tests to be scheduled. Two dedicated closures are foreseen.

The full end-caps will be tested at low temperature only after arrival at CERN, due to the limited availability of adequate CO_2 plants and extreme high costs for such a big structure. The end-caps will arrive at CERN having been cold tested service sector by service sector. The barrel will be cold tested sector by sector at the end of the build process at CERN. As closing the gas volume to do a cold test is a substantial overhead the CO_2 plant will be run warm (20-25°C) for most tests. This means that the noise results obtained will not be representative of the real scenario. However the tests will allow the understanding of the thermo-mechanical behaviour of the structures. Despite performing warm tests, this is not at zero risk. For example, an unplanned vent could cause icing. Work is needed to mitigate this risk. The barrel is planning cold tests after one service module worth of staves is installed on layer 3 (eight staves), four service modules worth of staves are installed on layer 3 and layer 2 (32 staves, 16 per end) and after all the staves are installed (48 service modules, 384 staves). This cold test will be staged looking at a few tens of staves at a

time. The end-cap community has not yet finalised when cold tests will happen during its builds as the cold box has yet to be designed. It is expected that a similar pattern will be followed.

11.4 Service Modules Design

The service design for the strip tracker has been motivated by experience from the service installation for the ATLAS SCT. There, all services (optical fibres, cooling pipes and electrical cables) were installed individually either into service channels on the calorimeter wall or onto the OD of the end-cap support structure. This design lead to a sequential service installation due to the limited accessibility and the large number of individual services, which in turn resulted in a lengthy installation procedure. When problems were encountered ad-hoc modifications of the original service design were performed. The exit of the services from the SCT barrel and end-cap thermal enclosures were badly designed and resulted in a large leak rate from the ID. In consequence, no overpressure has ever been possible on the SCT volume. It is clear that the experience from the SCT points towards higher integration of services. For the Tracker upgrade we are pursuing a model where pre-fabricated units of services (service modules) are presented to the structures. These units carry all the services for a number of staves or petals, and are intended to be pre-tested with no facility included to allow in-situ rework. The decision to interface one stave or petal as the smallest detector unit has dramatically reduced the service count compared to that in the SCT. While this has been essential to reduce the service cross section, there is still a very considerable amount of services to manage.

11.4.1 Sealing the End of the Service Module

The tracker environment is enclosed by a chamber made from the support cylinder, two structural bulkheads, and two ID endplates. It is penetrated through the centre by the beam-pipe, which is expected to be sealed as part of the pixel detector build, and is traversed at the two z ends by the patch-panels of the strip and pixel systems. Where the service modules enter the tracker volume they need to maintain the integrity of the volume. Although the barrel and end-cap provide different implementations of the seals, the principles are the same and the challenges and proposed implementations will be described here:

1. Gas seal: The SCT was unable to ever achieve gas over pressure as the penetration of its services through its thermal enclosure were not sufficiently sealed. This was principally due to the gas seal that had been made in situ with RTV[3)] around the individual services. In the ITk the services are installed in service modules. A service

[3] room temperature vulcanising

module has all its services sealed to the service module duct during fabrication. This will happen both part way along the multi core cables, and at the patch-panel. The quality of these seals are to be tested before installation. The service module and patch-panel need to be sealed into the relevant structure. In the case of the end-cap, this will be the patch-panel into the structural bulkhead. For the barrel, the patch-panel and the service module body will be sealed to the OC, and the gaps between the service modules will be bridged to present a single face to seal the structural bulkhead to. All these gas seals are shown in Figure 11.6.

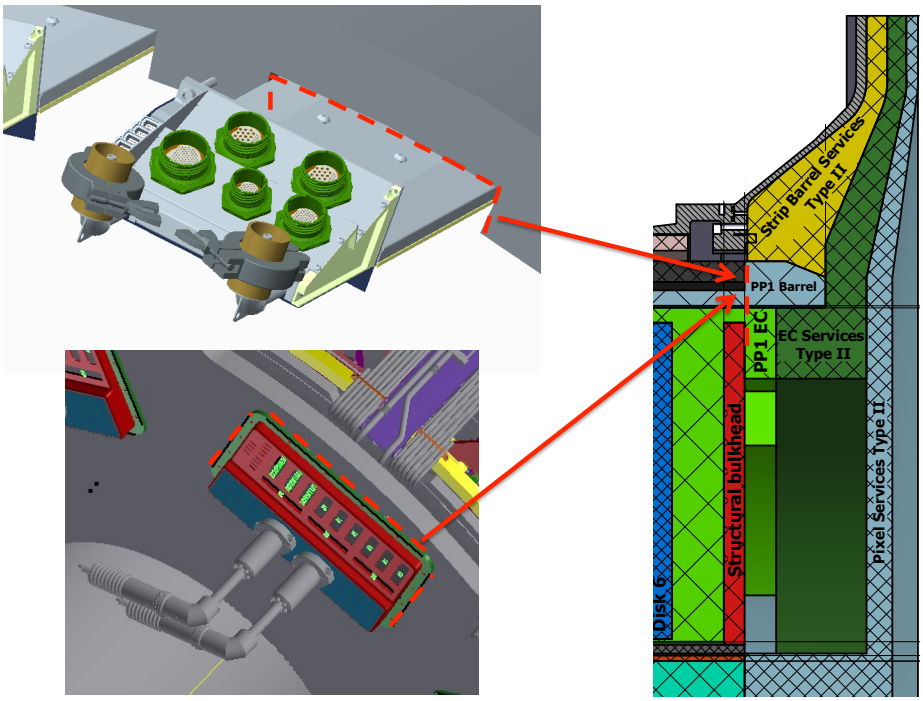


Figure 11.6: Location of the gas seals around the services at the end of the outer cylinder - on the envelope drawing the dashed line shows the approximate location.

2. Grounding and shielding: The general philosophy of grounding and shielding as described in Chapter 17 defines the requirement that the cables and pipes all share a common ground at the patch-panel. This common ground links to the Faraday cage provided by the tracker OC and structural bulkhead. This requires that both the barrel and end-cap strip systems make these connections within their service modules. Also the service modules and patch-panel PP1 then need to be connected back to the structure with an appropriate connection. Neither barrel nor end-cap have yet final implementations of these grounding connections.

3. Thermal barrier: The successful closing of the gas volume, described below in detail, is a critical part of the thermal management of the system. Once the closing is complete only conductive heat exchanges will occur. The thermal management of the ITk is discussed in Chapter 18. The outside faces of the OC will run at cavern temperature

and humidity. If the control of this fails no condensation problems are expected as the cryostat bore will be dry gas flushed within the ID end-plates.

11.4.2 Barrel Service Modules

For the ITk strip tracker pre-fabricated, standardised and removable service modules were developed. Each of these is installed as one unit containing all services for a set fraction, e.g. $1/24^{th}$ of one end of the barrel (see Figure 11.7). The services comprise cooling pipes and associated manifolds, electrical cables and optical fibres. The service module would also contain well-defined internal electrical ground connections for all metallic surfaces, in particular cooling pipes, and a common ground connection to the thermal enclosure. The off-detector end of the service module is part of the thermal enclosure and contains all necessary feed-throughs. Performance of the gas and thermal seals is fully qualified before installation. The most challenging area of the Service Module to implement reliably is at the detector end because of the complexity of weaving the services from a rotational to mirror symmetric arrangement.

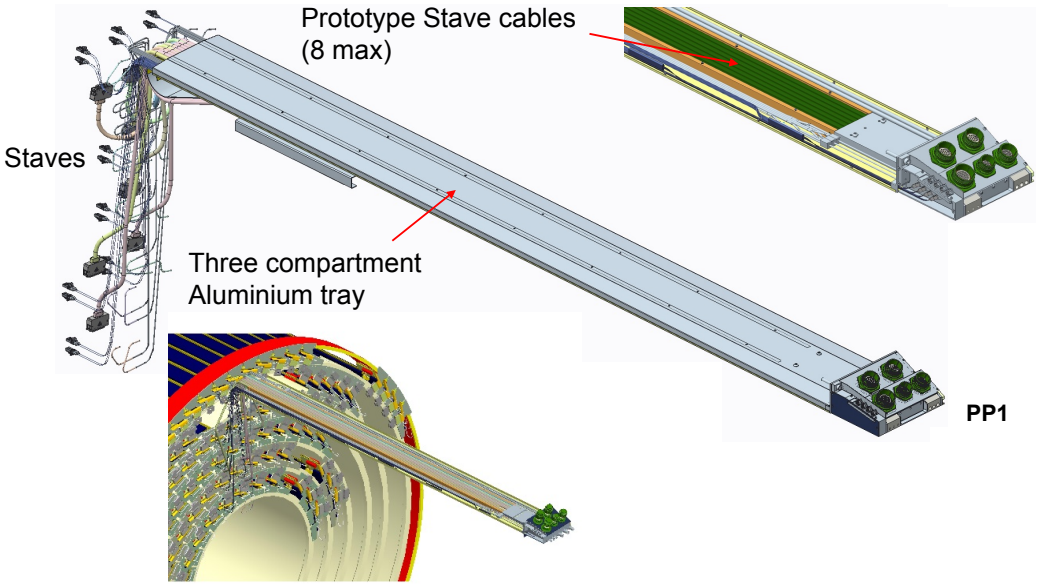


Figure 11.7: Barrel service module; each service module supplies eight staves with LV power and sense lines (EoS & Hybrid), HV power, interlock signal, optical fibres, and cooling.

Service Module Body

The service modules are self-supporting and hook up to the outer cylinder with just two fasteners to facilitate installation. At the same time, structural elements of the service module are small enough to not significantly reduce the volume available for services. The

service module body is proposed to be made from folded Aluminium with a thickness of 0.5 mm. If the geometry would need to be more complex the option is retained to fabricate from CFRP. To install a service module it is lifted into place, the z = 0 end hooks in to features pre-installed on the outer cylinder and the patch-panel end is bolted to the outer cylinder onto of a silicone rubber gas seal.

Off-detector patch-panels

Patch-panels at the end of the ITk allow electrical connectors to exit radially in the region of the cryostat chamber. Optical links exit longitudinally, and cooling radially in a higher z position than the electrical services. The whole patch-panel is kept outside the end-cap radii to ensure no reforming of any services is needed to install the strip end-cap. All connectors are sealed into the patch-panel, with the seal qualified as part of service module production, so that just the duct needs to be sealed into the ID during ID integration.

Cooling services

The preferred joining technique for all joints inside the thermal enclosure is welding to achieve low-mass, reliable connections. All connections within the service modules are made before integration into the outer cylinder. Within the service module there are also vacuum brazed assemblies which are welded onto the rest of the tubes. It is presently expected that the electrical insulated breaks are vacuum brazed, and also transition pipe diameter. The termination of the capillaries may also use a vacuum braze process. Service module welds could use any welding technique, but the preferred option is orbital Tungsten Inert Gas (TIG) welding, where an electrical arc is formed and maintained by a tungsten electrode in a insert gas (argon) atmosphere. The electrode is mechanically driven to orbit the pipe. At the detector-end pipes from the service module terminate close to the local supports. The connection from the detector to the service modules is made by a short patch pipe, which is cut to length and shaped to the actual end positions during the barrel integration. This short patch pipe is connected using orbital TIG welding. The routing of the patch pipe, and the adjacent sections of the pipes on the service module and the local support, prevent stress transmitted onto the staves and allow access for the orbital weld head. The probability of a successful joint at this stage is improved if pipes of similar parameters are joined. Therefore it is proposed that the transition from the on-detector pipe parameters to the service module pipe parameters shall be part of the on-detector cooling pipe assembly, and be qualified there. At the off-detector end of the service modules the pipe termination is not yet finalised as it depends on the type-2 (end of the cryostat) service design that is not yet finalised. The preference is either a bare pipe to be orbitally welded or something similar to a VCR bulk-head connector.

The manifolds reduce the number of cooling connections before the ID ends by about a factor 1:4 to 1:8, which is a good compromise between the space needed for connectors

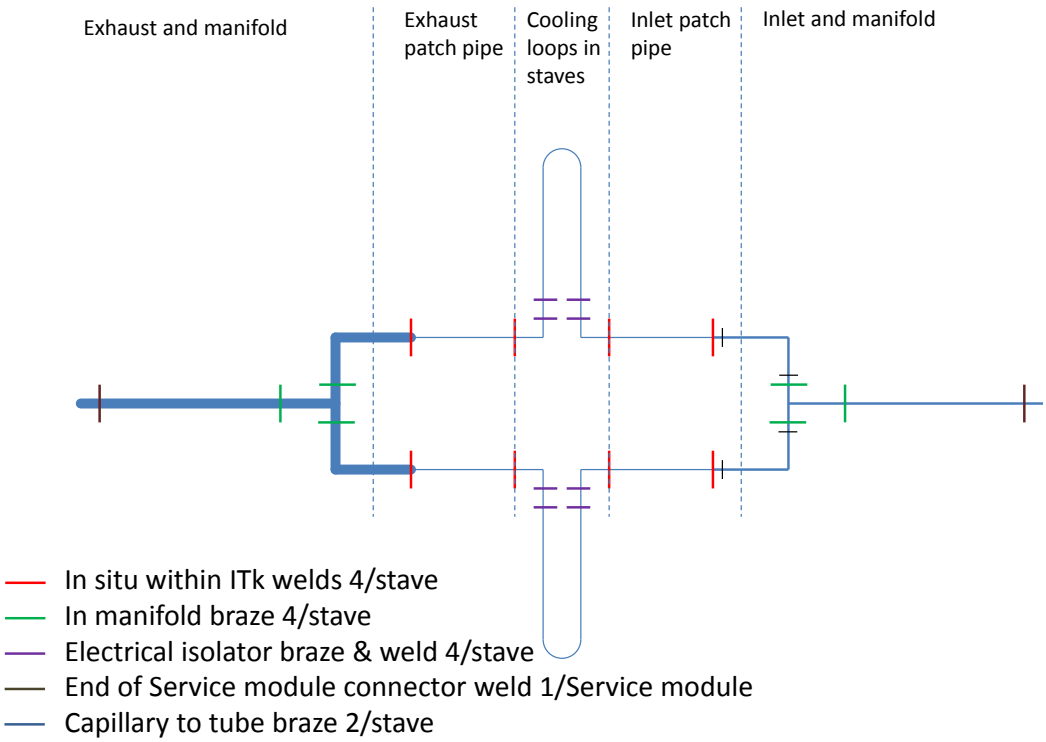


Figure 11.8: Sketch showing the locations of the welds and cooling connections within a cooling loop on the barrel.

and pipes from there to PP2, and the risk of damage that may incapacitate many modules. A 1:4 manifolding scheme would result in the loss of 8 staves (112 modules) from a fault in one cooling circuit. These manifolds are part of the service modules. For the barrel Strip Detector each service module connects on average to three short-strip and five long-strip local supports (1/24th segmentation). It is believed that the difference in power load on these different arms of a manifold does not cause any issues as the pressure drop is dominated by the capillary. A diagram of the cooling pipe connections within a barrel strip service module is given in Figure 11.8.

Power and DCS cables

Cables are standardised and slightly over length at the detector end of the service modules with the surplus being lost in routing. The cables have a decoupling capacitor between each line and the system ground at PP1.

Optical Services

The optical conversion of the modules's data signals happens on the local support (staves or petals), namely on the end-of-substructure card. At the detector end single fibres with overlength will connect to the local supports. These fibres need appropriate protection during installation and in-situ. The single fibres will get ribbonised within the service module and terminate at standardised MT8 or MT12 ribbon connectors at the ITk end.

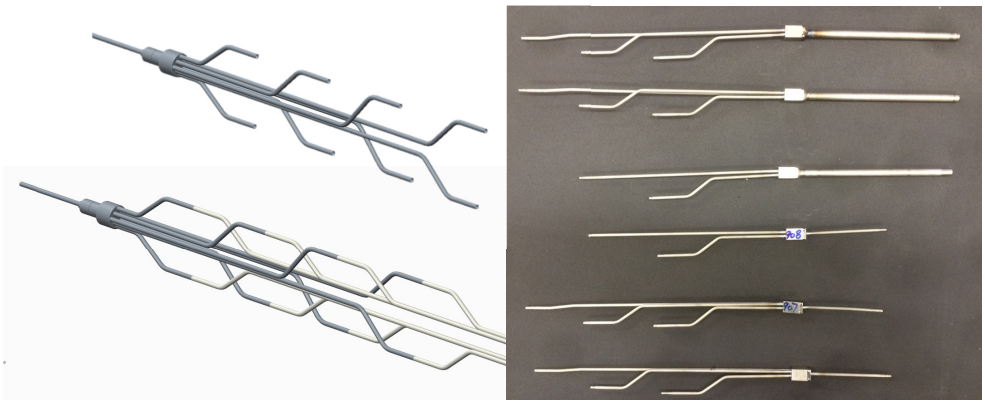


Figure 11.9: Barrel service module cooling manifolds. The photograph shows the inlet manifolds and a 2:3:3 configuration. As the flow is better understood the granularity of manifolds may change, and we would like to go to an 8 way manifold as shown in the renderings.

11.4.3 End-Cap Service Module

The service modules in the end-cap are based on the same concept as in the barrel. They are pre-fabricated, standardised and removable objects or units, each containing all services for a number of petals. In addition, the end-cap service modules play a very important structural role in the end-cap global support structure. They run on the outside and all along the end-cap structure. Contrary to the case of the barrel, the service modules will be already installed when the petals are inserted and that limits the number of service units. The end-cap design has eight of those service modules equally distributed in ϕ. The electrical services carried by the module serve a section in ϕ comprising four petals in each disk. The cooling services, however, will serve half disks rather than the corresponding ϕ section. The idea behind this is to avoid losing more than one point in the tracks in the event of a failure in the cooling circuit on the service module. As a consequence, four of the service modules serve the cooling for 32 petals, while the other four only contain the cooling services for 16 petals. Figure 11.10 shows a service module servicing a phi sector with four petals in each disk.

The end-cap service modules are part of the structure while the patch-panels are attached to the structural bulkhead by inserting them from the inside. This closes both the thermal

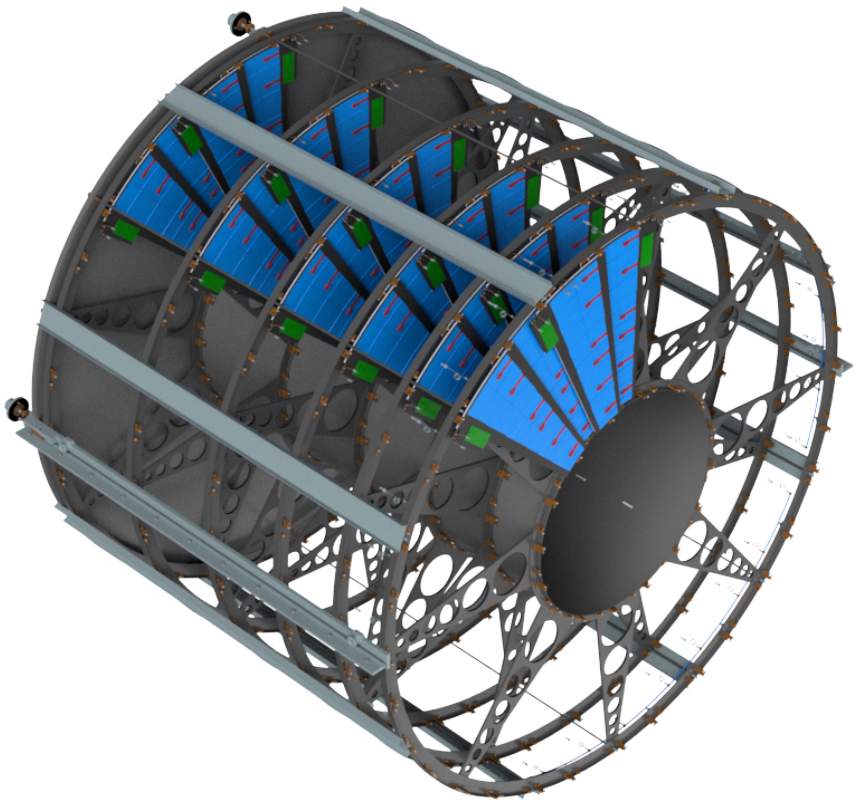


Figure 11.10: An end-cap service module serving. Each service module electrically serve a section in ϕ comprising four petals in each disk

and electrical enclosures. It is assumed that the bulkhead, even if not part of the end-cap, travels with an end-cap so that the patch-panels do not need to be placed in temporary structures while the end-cap is assembled. Figure 11.11 shows one service module with the patch-panel at the left. Services leave the service duct close to the patch-panel and fly from the service module to the patch-panel.

The service module consists of a carbon-fibre tray that contains the pipes inside. The electrical services run along the tray on the outside and are held by a perforated panel close to the point where the petal is connected to its services. At this point, the cooling inlet and outlet corresponding to that half disk leave the tray though holes at the bottom where they connect to the circumferential pipe from where the capillaries connect to the petals. The capillaries will be coiled before connecting to the petal to absorb tensions

The service module tray provides a well-defined internal electrical ground connection for the pipes and a common ground connection. The electrical services are already shielded and connect to the common ground in the patch-panel (Figure 11.11).

The petals are arranged on the disk in pairs such that the end of substructure boards are al-

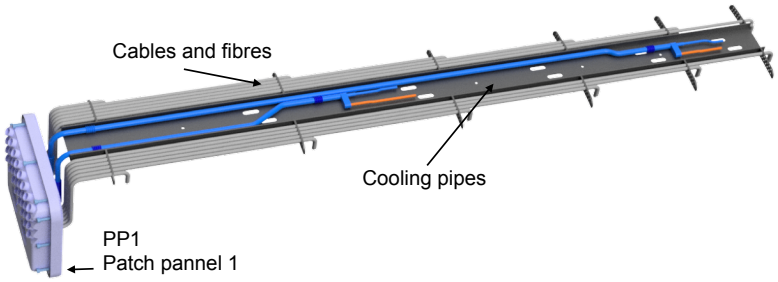


Figure 11.11: An end-cap service module: The patch-panel, at the left, is inserted in the structural bulkhead, while the service module tray is part of the structure. This requires that services "fly" from the patch-panel to the service tray.

most facing placing to connectors close to each other. The two inner petals in the ϕ segment have the end of petal substructure right under the service tray where the connection will be made as show in Figure 11.12 (left). For the outermost petals the cables will exit the service tray and run over the disk ring until the end of substructure boards of the corresponding petals where the connection will be made (Figure 11.12, right). The cooling pipes protruding the petals are only bent during installation to avoid the need for two petal flavours. Figure 11.13 shows the pipes before the welding of the cooling pipes. To allow for bending with relative ease annealed copper tubing is used.

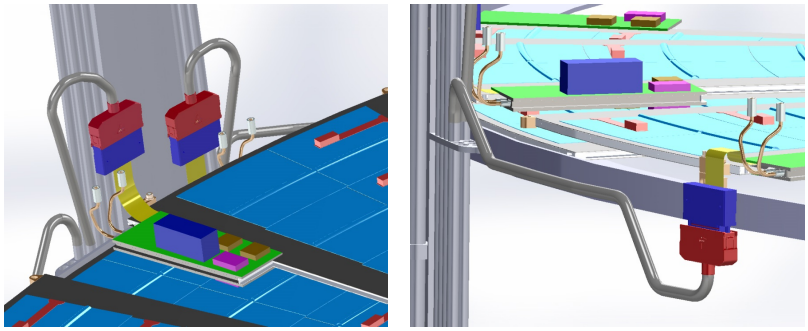


Figure 11.12: The petals are either connected under the service modules in case of an inner petal (left) or over the disk ring (right).

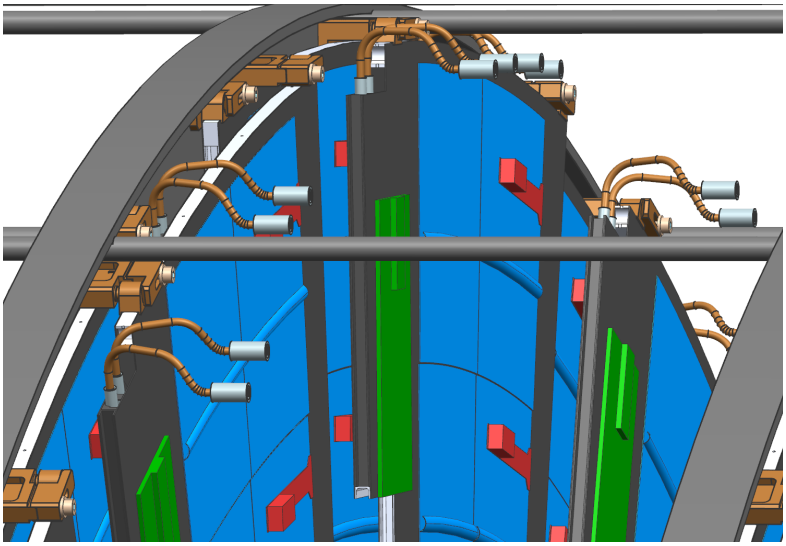


Figure 11.13: All cooling pipes protruding the petals are bent into the same direction to ease the welding process. The bending of the pipes is foreseen during the petal loading.

12 On-Detector Control and Read-Out Electronics

This chapter describes the on-detector control (situated outside of the modules) and read-out architecture. These electronics are responsible for communication between the on-detector modules and control components, and the off-detector electronics, the ATLAS Trigger and Data-Acquisition (TDAQ) and Detector Control System (DCS). This includes all control signals, the entire data stream and the DCS data to a large extent. All front-end data and controls flow through the End-Of-Substructure Card (EoS) (see Section 12.1), the optical links (see Section 12.1.2) via the ATLAS-wide FELIX system to and from the ATLAS TDAQ (see Chapter 16).

The Detector Control System is split into three parts: the hardware-based DCS, which is common for the the entire ITk (see Section 12.2), the the local interlock functionality for the power board provided by the AMAC (see Chapter 6.2.7), and the DCS data coming from the ITk Strip Detector, which is included into the data stream. Details of the off-detector components including the FELIX system are described in Chapter 16.

12.1 The End-of-Substructure Card (EoS)

The End-Of-Substructure (EoS) Card is the interface between the stave and petals with the off-detector electronics. In both cases the EoS is situated on an "ear" at one end of the substructure (see Chapter 9). The EoS handles all the communication between the stave/petal and the off-detector electronics and additionally also link both LV/HV from the power supplies to the stave/petal. There is always one EoS per side, so each stave or petal will actually host two EoS cards.

The EoS hosts up to two lpGBTx (low power GigaBit Transceivers) high-speed serial communication ASICs (see Section 12.1.1) and an optical transceiver module (see Section 12.1.2) VTRx+ (Versatile Transceiver). The lpGBTx and VTRx+ are common developments for the PhaseII upgrades of all LHC experiments and thus not developments of the ITk community and here summarised for completeness.

The EoS electrical schematics for both barrel and end-cap are common with only minor differences in the number of supported data channels and the number of necessary lpGBTx ASICs. The layout will be different due to different geometrical requirements in the barrel

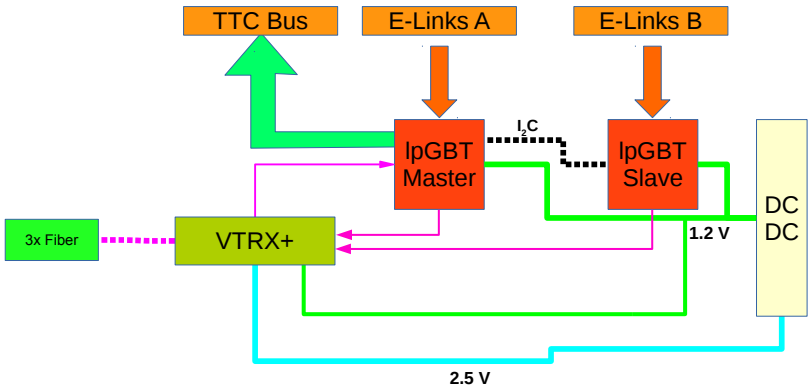


Figure 12.1: A block diagram of the short-strip Barrel EoS card, showing the VTRx+ optical package, the two lpGBTx in master-slave mode and the data stream going to (TTC) and coming from the stave/petal (E-Link A / E-Link B) and the DC-DC converter block

staves and the end-cap petals. In the case of the short-strip barrel EoS, the two lpGBTx on the EoS are operated in a master-slave configuration There is only one downlink (RX) link to the master lpGBTx, but two independent uplink (TX) links (see Figure 12.1). In this case the master lpGBTx passes the configuration data to the Slave lpGBTx via the I^2C bus. For both the end-cap and long-strip barrel modules, only one lpGBTx is required per side and the master-slave mode is not required.

For the timing, triggering and control (TTC) bus, the incoming optical signal runs at 2.56 Gbit/s. The forward error correction (FEC) can correct for an error burst of up to 16 bits and provides 1.28 Gbit/s user data. This allows for the detection and correction of the expected error bursts in the p-i-n diodes [96]. Different TTC data will be sent to four different groups of modules on the stave/petal at 160 Mbit/s.

The lpGBTx uplink operates at 10.24 Gbit/s providing, after headers and FEC, 8.96 Gbit/s for user data. The HCCStar ASICs on the modules (see Section 5.1) will send data at 640 Mbit/s to the lpGBTx. Therefore two lpGBTx ASICs are required per stave/petal side to accommodate the 28 (short-strip barrel) and one lpGBTx to accommodate the 14 (end-cap/long-strip barrel) HCCStar chips respectively (see Table 5.1). The data are scrambled by the lpGBTx to remove any DC bias.

The EoS card itself requires two input voltages, 2.5 V for the VTRx+ with the VCSEL(Vertical Cavity Surface Emitting Laser diode) in particular and 1.2 V for both the VTRx+ and all the other components including the lpGBTx ASICs. The input voltage from PP1 (11 V) will be converted to 2.5 V using the upFEAST converter (see Section 6.2.9) and then converted down to 1.2 V using the DC-DC2s chip [97]. The DC-DC2s chip has an input voltage of 2.0-2.7 V and an output voltage of 0.6 to 1.5 V and a maximal output current of 3 A. It is designed using a 130 nm process. This process makes it possible to withstand a total ionising dose of 100 MRad and a total displacement damage up to $4x10^{15}$ n_{eq}/cm. The total power

consumption per side is 3 W for the two lpGBTx variant including the DC-DC conversion efficiencies.

Each stave/petal has only one power connector including the high voltage and low voltage for both sides of the stave/petal, so the two EoS cards needs to be linked using a high-density connector at the edge in order to route the power to the second EoS. There will be a connector for the NTCs for the DCS system (see Section 12.2).

12.1.1 The lpGBTx ASIC

The low power GigaBit Transceiver (lpGBTx) is a high-speed, radiation-hard multiplexing chip, that can de-multiplex a serial input link into many different channels (the so-called E-Links) and multiplex many E-Links back into a common uplink. The number of E-links varies with the required data rate and level of error correction, e.g. one can use either eight 160 Mbit/s E-links or two 640 Mbit/s E-links. The lpGBTx also adds FEC code to its link. The lpGBTx also includes a slow-control interface with an I^2C bus, a 10 Bit ADC with eight input channels an internal temperature sensors and a current source to drive an external sensor.

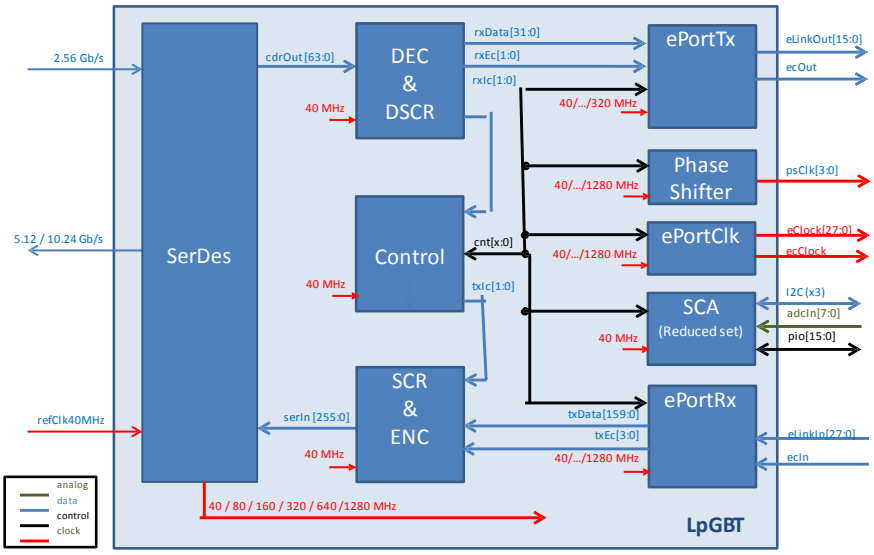


Figure 12.2: A block diagram of the lpGBTx chip with serializer/deserializer block(SerDES), the Decoding (DEC & DSCR)and Encoding Units (ENC & SCR), the Controller (Control), the input and out E-Links (eportRX/TX), the programmable clocks and the Slow-control interface (SCA).

The lpGBTx is a development of the existing GBTx chip [98] to work at higher data rates and survive the radiation doses for the Phase-II upgrades. The lpGBTx is therefore being designed in 65 nm technology. The lpGBTx will come in a Ball Grid Array (BGA) package requiring minimal external components.

12.1.2 High-Speed Optical Driver VTRx+

The opto-electronics for the data transmission between the EoS and the off-detector DAQ will use the components developed by the *Versatile Link* + group (see Figure 12.3), the main ASICS being the GBTIA (Gigabit Transimpedance Amplifier) for the receiving part and the GBLD10 (Gigabit Trans-impedance Amplifier) chip to drive the optical transmitter.The optical links will use Vertical Cavity Surface Emitting Laser diodes (VCSELs) and photodiodes operating at a wavelength of 850 nm and multimode fibres.

For the downlink RX on the EoS, the optical to electrical conversion will be performed by a photodiode (PD). The converted signal is then amplified and discriminated by the GBTIA and fed into the master lpGBTx

The multiplexed data from each of the two lpGBTx chips is then sent on the uplink to the low-power laser driver ASIC lpGBLD10, which drives the optical TX Link using a VCSEL. The lpGBLD10 ASIC is under development but existing prototypes have achieved the required speeds [99]. Array drivers are being developed in 65 nm technology which will result in lower power consumption.

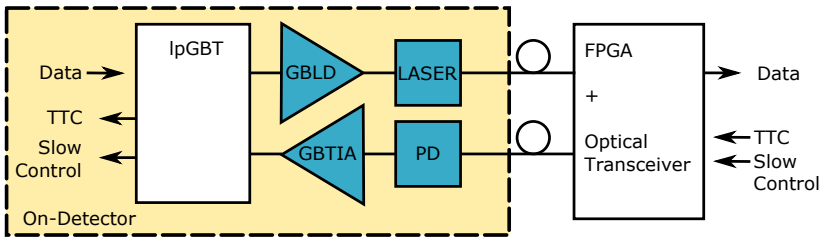


Figure 12.3: The opto-electronics read-out chain. The on-detector items are inside the dashed yellow box. PD=photodiode. The functionality of the radiation tolerant ASICs is described in the text. The off-detector opto-electronics will use commercial off-the-shelf components.

The links power budget is being evaluated by the VL+ group but is expected to be very similar to that of the Versatile Link [100]. The maximum insertion loss for fibre connectors is 1.5 dB. Therefore assuming that there are three fibre connections in the chain, the loss per connector should be less than 0.5 dB.

The power consumption for all ASICS is summarised in Table 12.1.

Table 12.1: Power consumption for the opto-electronic ASICs

ASIC	Power consumption (mW)
lpGBTx	750
GBTIA	129
GBLD10	56

Opto-Electronic Packaging

The GBLD10, the GBTIA and the corresponding lasers and photodiode will be packaged in one transceiver module (VTRx+) by the Versatile Link+ group. The VCSELs and photodiodes will be of the same type as used in the existing VTRx modules since these have been demonstrated to be sufficiently radiation tolerant [101]. Different options for the packaging are being developed but they are all very much smaller than the existing VTRx and are very low profile. The number of RX and TX channels can be adjusted to match the user requirements and it is currently foreseen to use two TX and one RX channel in a package.

The VTRx+ will contain electrical connections for power and for the high-speed electrical I/O. It will contain a "pig-tailed" optical package (a short fibre cable which is directly connected to the optical package) with small form factor optical connectors at the end of the fibres (such as the LC connector). The fibres will be connected to adaptors at the end of the EoS card to simplify making fibre connections during the final installation.

12.2 Detector Control System

To ensure safety, reliable control and information for debugging the ITk Pixel Detector control system (DCS) foresees three independent paths. These paths differ in granularity, availability, and reliability. Each has its own signal paths.

The safety path is built by a hardwired interlock system, which acts directly on power supplies or other equipment, if the safe operation of the detector cannot be guaranteed any more. This system must have the highest reliability, however, due to the required low material budget, the lowest granularity. It is always in operation.

The ITk Strip Detector DCS comprises three main components: a Common Interlock system, shared with the Pixel Detector; a Common Monitoring System, also shared with the Pixel Detector; a Strip specific interlock and monitoring system provided by the AMAC chip (see Section 6.2.7).

12.2.1 Common Interlock

The ITk Common Interlock System is a safety system which protects both the detector and personnel against any risks which may arise. It is a completely hardwired system which acts as last line of defense for the detector safety. It must be running at all times, but has a coarse granularity and relatively low precision. In the case of the ITk Strip Detector, the common interlock system operates in support of sub-detector specific interlock circuits, described below, which would normally be expected to operate first before the detector is switched on.

As overheating is one of the main risks to all silicon detectors, temperature sensors are located at crucial points of the ITk. In the ITk Strip Detector, each cooling pipe outlet is equipped with dual (redundant) 10 kOhm Negative Temperature Coefficient (NTC) thermistors. These are chosen due to their high radiation hardness and their large signals (δR/δT) which permit the use of two-wire read-out and routing of signals back to the counting rooms.

All signal processing takes place in the Interlock Matrix Crates (IMCs) located in the counting rooms. This location is chosen such that radiation hardness is not required and that the equipment is accessible at all times. The voltage across each temperature sensor is converted to a binary signal by means of a discriminator with a predefined threshold. These interlock signals are then fed into a Complex Programmable Logic Device (CPLD) programmed with an action matrix, mapping interlock signals onto the associated power supply channels.

In addition to temperature information, signals from the ATLAS Detector Safety System (DSS) providing information such as the status of the accelerator or the ITk cooling plant are also fed into the CPLD: certain events may require action upon a large number of channels to help protect ITk detector hardware against major external failures. For safety reasons a negative logic is foreseen, such that the system fails safely if any cables are removed. Also note that all temperatures are digitised and fed into the Detector Control System for purposes of detector monitoring.

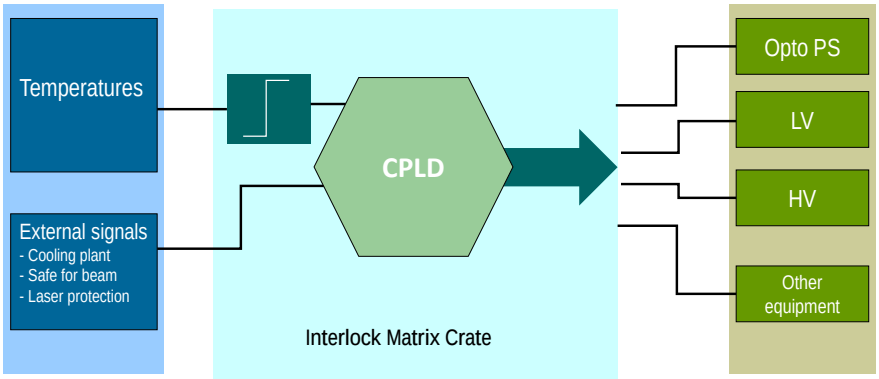


Figure 12.4: The conceptual form of the ITk Interlock Matrix Crate (IMC).

12.2.2 Common Monitoring

The Common Environmental Monitoring system provides temperature and humidity monitoring within the ITk detector volume. In the case of the ITk Strip Detector, all sensors which do not directly form part of the staves or petals are supervised by this system, for example the temperatures of air volumes or cable bundles. In order to keep the services

which must be routed out of the detector volume to a minimum, some local data processing is foreseen.

CERN is developing a successor to the Embedded Local Monitor Board (ELMB) presently used in the LHC experiments [102]. The proposal for ELMB++ aims to use components developed for high bandwidth optical links (GBTx, GBT-SCA, VTRx etc.) to realise a radiation hard monitoring system which may be deployed in the experimental caverns. As the GBTx and VTRx are relatively expensive items, it is proposed that these are integrated into "HUB-ELMB++" units, each of which may then utilise electrical links to up to 19 "Satellite-ELMB++" boards. In this way the data for up to 1240 inputs with digitised data may be routed back to the counting room over a single, cost effective VL optical link. Whilst this scheme remains under development, it is most likely that this is going to be used for the ITk common monitoring.

12.2.3 ITk Strip Detector Interlock and Monitoring

Within each stave or petal, a local interlock system is provided by means of the Autonomous Monitor And Control (AMAC) chip located on the on-module power board (see Chapter 6. This forms our first line of defense against temperature excursions of the powered detector modules. The AMAC chip monitors several on-module parameters such as the temperature of each hybrid and the sensor bias current. It must also be powered and configured in order to enable the two key components of the on-module power board, the DC-DC converter and the HV Multiplexer switch. Each analogue input is digitised autonomously, results being transmitted off-detector for purposes of supervision upon request (through lpGBTx by means of an I^2C link). In addition AMAC compares the digitised signals against programmable upper and lower limits: any excursion beyond these limits will, in extreme cases, result in the DC-DC converter and HV switch being disabled directly.

12.3 The Optical Links

The components of the on-detector optical links are described in Section 12.1. The on-detector optical transceiver, the VTRx+ contain a “pig-tailed” optical package (see Section 12.1.2) and for each VTRx+ there will be a short length of fibre break out cable, terminated with a small form factor optical connector such as an LC connector. For the barrel, this will allow a connection to the ribbon fibres in service modules (see Figure 11.7).

The fibres in the service modules will be in ribbon form and be terminated with MT/MPO (Multiple-Fibre Push-On/Pull-off) connectors at patch-panel 1 (PP1). The ribbons will be split into single fibres with standard LC connectors at the EoS end. All the fibres will be multi-mode and operated at a wavelength close to 850 nm. The fibres inside the high dose

region of the detector will be qualified radiation tolerant fibres. It was verified that the radiation induced attenuation (RIA) for these fibres operating at -25 °C is acceptable [103]. Furthermore it was demonstrated that the mechanical reliability of these fibres is maintained with increasing radiation [104] as well as that there is no significant deterioration of bandwidth with radiation [105]. As a final test the radiation hardness of the LC and MT/MPO fibre connectors [106] was verified. In order to satisfy the bandwidth requirement, an OM3 (multi-mode) fibre needs to be used. OM3 (OM4) fibre, as defined in ISO/IEC 11801 has a minimal modal bandwidth of 1500 (3500) MHz.km. However the cost of long lengths of qualified radiation tolerant OM3 fibre is prohibitive, a shorter length of such fibre will be used and spliced to a longer length of a commercially available (COTS) fibre which would still be sufficiently radiation tolerant.

In the counting room, commercial opto-electronics packages will be used to convert optical signals to/from electrical signals. Ongoing VTRx+ research has shown that several components are commercially available that operate at the required data rates. As this is a rapidly evolving market, new components are being continuously tested. In the counting room, the functionality of the lpGBTx will be implemented in FELIX FPGAs.

12.4 Quality Control

12.4.1 EoS Card

The PCBs will be manufactured and populated in industry and a thorough quality control of the board will be performed by the manufacturer. This includes boundary and X-ray scans of each BGA package to check for connectivity of the solder balls. It is also foreseen to have a dedicated set of vias on each board to probe the via quality. All EoS card will then be put under a thorough burn-in test and an extensive Bit error rate test, which each card has to pass.

12.4.2 Opto-electronics Quality Control

The opto-electronic ASICs will be tested at the wafer level and only known good die will be packaged. The VCSELs and photodiodes will be packaged into the VTRx+ and then tests will be performed on the VTRx+. The critical parameters for the VCSEL that will be measured are laser threshold and slope efficiency, rise and fall times. The minimum receiver responsivity will be measured for the photodiode. This is defined as the incoming optical power for which the Bit Error Ratio is less than a specified value. The exact tests to be performed will be defined by the VL+ group at the end of the development stage.

13 Production Model for the ITk Strip Detector

The production of the ITk Strip Detector involves both a range and quantity of objects that far exceed the production of the current ATLAS strip tracker (SCT). For example, the number of silicon strip modules for the barrel has increased from 2,112 to 10,976, and for the end-cap from 1,976 to 6,912. This is equivalent to a 388% increase in the number of modules required during the production phase of the project. Such a significant increase in the number of modules (and their associated components) has led to improving in every way the ease of construction and affordability during the production phase.

This effort to streamline the assembly process has driven the development of the local support concept. In the current SCT, large numbers of modules were mounted serially on a relatively small number of large-scale structures (four in the barrel and 18 for the end-caps). For the ITk Strip Detector, groups of 28 barrel modules will be mounted onto the stave and groups of 18 modules onto each end-cap petal. These local support structures form independent and functional sub-systems which can be fully tested before being installed in the global structure. This ensures working highly parallel and that the time between the start of the assembly of a particular module to a test in its final operational environment is as small as possible. To achieve the best possible outcome, it is important to define a production model in which the rates of module assembly and local support manufacture are well matched.

The production model for the strip modules will be heavily based on both SCT experience and R&D developments. Many production steps, quality assurance and quality control processes are planned to be scalable and modular, and production and testing rates have been estimated (and measured where possible) for all objects. Monitoring of the production process will be carried out via the ITk production database.

13.1 Production Model Infrastructure

The following section will detail the existing plans for the infrastructure necessary for production, including the work breakdown structure (WBS), the organising of build sites into assembly clusters, and the layout of the division of responsibilities and reporting lines.

13.1.1 Work Breakdown Structure

The work breakdown structure (WBS) defined for the ITk Strip Detector is a hierarchical decomposition of tasks and deliverables needed to complete the project. It breaks the tasks and deliverables down into manageable work packages that can be scheduled and have costs and resources assigned to them. The WBS for the ITk Strip Detector is shown in Table 13.1. The highest level shown in the table (level-3: e.g. 2.2.1 for sensors) defines all deliverables or major construction milestones during the production.

13.1.2 Assembly Clusters

The construction of the barrel and two end-caps will be the responsibility of two assembly clusters of institutes; one cluster for the barrel and one for the two end-cap. It is anticipated that some sub-components may be procured or manufactured by a single cluster or even a single funding agency. Such items may include AMAC ASICs, HV multiplexers and EoS cards.

One cluster will be responsible for the delivery of the barrel to CERN. For the end-caps, the cluster will be responsible for assembling complete end-cap sub-systems and delivering them to CERN. They will then be jointly responsible for the integration of the end-caps with the barrel section. All involved institutes will share the work relating to the final testing of the ITk Detector on the surface and the subsequent commissioning once the ITk Detector is installed in ATLAS.

13.1.3 Division of Responsibilities and Reporting Lines

During production, a Production Coordinator coordinates the overall production flow of the ITk Strip Detector in strong collaboration with the Strip Project Leader and the Project Office (see Chapter 23). The Production Coordinator will oversee the overall production and ensure the interfaces between the various WBS activities. Each WBS level-3 deliverable (e.g. a 2.2.1 Sensors, 2.2.3 Module, etc) will be the responsibility of a WBS level-3 manager, responsible for the WBS planning, following the progress at all production sites involved in the respective WBS, ensure the QA process, and reporting. Each WBS level-3 manager oversees the progress in both clusters, for the barrel and the end-caps.

The Project Leader together with the Production Coordinator will organise regular meetings of the project management team who will review progress, discuss technical issues, monitor the quality control data and supply information to the clusters as required. The Strip PL will report progress to the ITk PL, ATLAS management and LHCC as required, as well as report to the institute board.

2.2	**Strip Detector WBS**	
2.2.1	Sensors	
	2.2.1.1	Sensor wafers
	2.2.1.2	Sensor masks
	2.2.1.3	Sensor probing
2.2.2	Read-out Chips	
	2.2.2.1 - 3	ABCStar masks, wafer production/dicing, testing
	2.2.2.4 - 6	HCCStar/AMAC masks, wafer production/dicing, testing
2.2.3	Modules	
	2.2.3.1	Hybrid procurement
	2.2.3.2	Hybrid assembly and testing
	2.2.3.3	Power board procurement/production/testing
	2.2.3.4	Module assembly and testing
2.2.4	Local Support Electronics	
	2.2.4.1 & 2	Barrel & end-cap bus-tape procurement/production/testing
	2.2.4.3 & 4	Barrel & end-cap EoS including optical interface and testing
2.2.5	Fully Assembled Local Support	
	2.2.5.1 & 2	Stave & petal facing co-curing
	2.2.5.3 & 4	Stave & petal cooling loop build and test
	2.2.5.5 & 6	Stave & petal core production
	2.2.5.7 & 8	Stave & petal loading with modules
2.2.6	Global Mechanics	
	2.2.6.1	Inner layers support tube
	2.2.6.2 & 3	Barrel & end-cap mechanical structures
	2.2.6.4	Insertion tooling
2.2.7	Services	
	2.2.7.1 & 2	Barrel & end-cap service modules
	2.2.7.3	Type-2 and 3 services
2.2.8	Integration	
	2.2.8.1	Barrel stave loading
	2.2.8.2	End-cap petal loading
	2.2.8.3	End-cap transport to CERN
	2.2.8.4	Integration testing
2.2.9	Off-detector Electronics	
	2.2.9.1	Detector Control System
	2.2.9.2	LV power supplies
	2.2.9.3	HV power supplies
2.2.10	Component Evaluation and System Tests	
	2.2.10.1	Module irradiation
	2.2.10.2	Further component irradiation
	2.2.10.3	System test at test beam
	2.2.10.4	Barrel stave system testing
	2.2.10.5	End-cap petal system testing

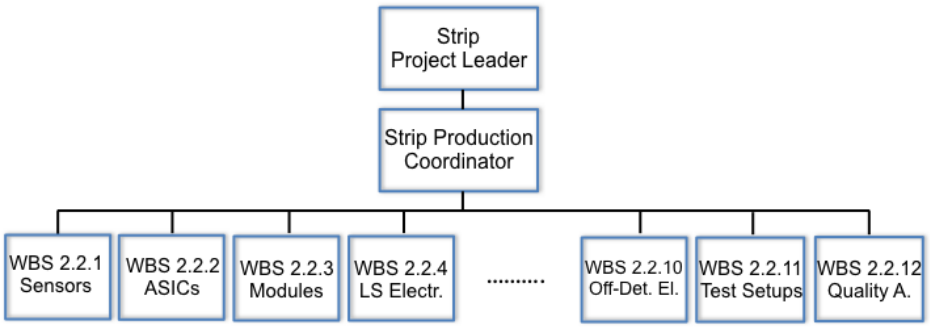


Figure 13.1: Organisation of the production team during the build of the ITk Strip Detector.

13.2 Global Production Plan

The production of the ITk Strip Detector will involve the building, assembly and testing of multiple items, shared by over twenty different sites in a 3.5 year period. Consequently much of the item production will be done in parallel, emphasising the importance of item flow (Section 13.2.2), build rates (Section 13.3), and scheduling (Chapter 24).

13.2.1 Product Flowchart

Figure 13.2 shows the parts flow involved in the manufacture of a completed stave. One short-strip barrel stave will involve the assembly of 28 modules consisting of 56 hybrids and 560 ASICs purchased from industry and their mounting on a stave core. The core is made from two bus-tapes, two EoS cards and a number of small components procured from industry plus raw materials such as carbon-fibre material, honeycomb, carbon-foam and titanium tube which have to be processed into sub-components and then assembled into a stave core (see Chapter 9 for details).

The production of modules requires the reception testing of vast numbers of sub-components, high-speed assembly and an efficient quality control regime whilst the assembly of a stave core requires relatively few parts but a large effort in processing, assembly and quality control.

13.2.2 Item Flow between Production Sites

Figure 13.3 is a schematic outlining the relationship between different production sites for the building of staves and petals, from sensors and read-out ASIC acceptance, to module on core (MC) assembly, and ending with integration. Each box represents the role of the building site, with lines indicating the necessary links between the site types, and consequently the production flow.

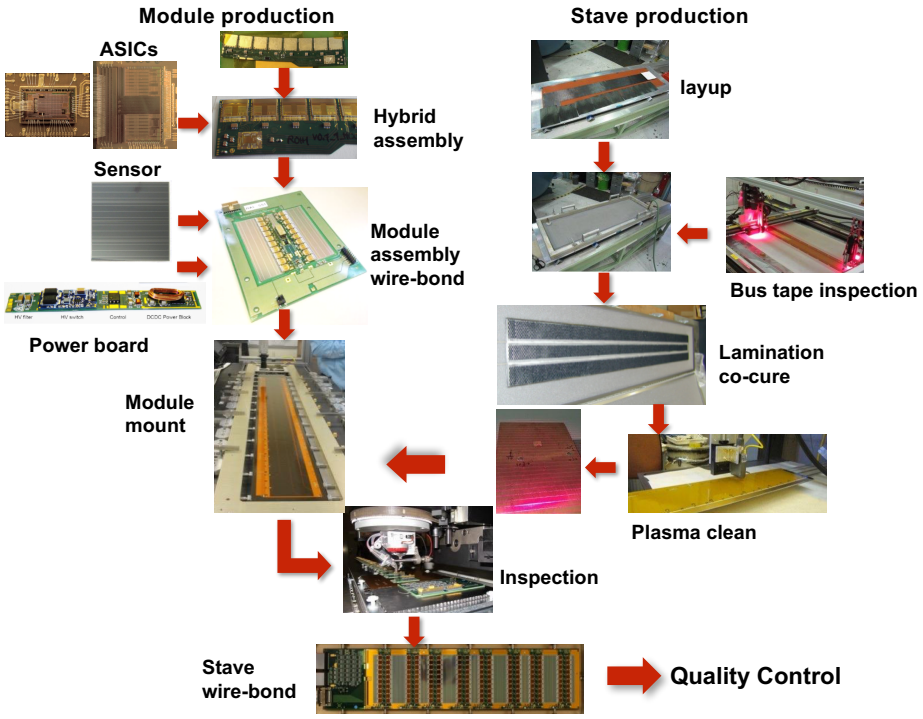


Figure 13.2: Product flow chart for a full stave or petal. The various processes are in parallel. The detailed testing between production tests are not shown.

The links between build sites will be established through the assembly clusters, accounting for transport distances and any variability (or downtime) in build rates at each site. Details of the high throughput rate necessary for certain items of the build are covered in Section 13.3

13.2.3 Production Sites

Table 13.2 shows the number of build, test or assembly sites involved in the ITk Strip Detector. In some cases sites will perform more than one step (for example, sites may build cores as well as the module on core assembly).

The number of sites for each part of the production has been determined based on the possible production sites as well as to allow for redundancy to cope with potential site downtime.

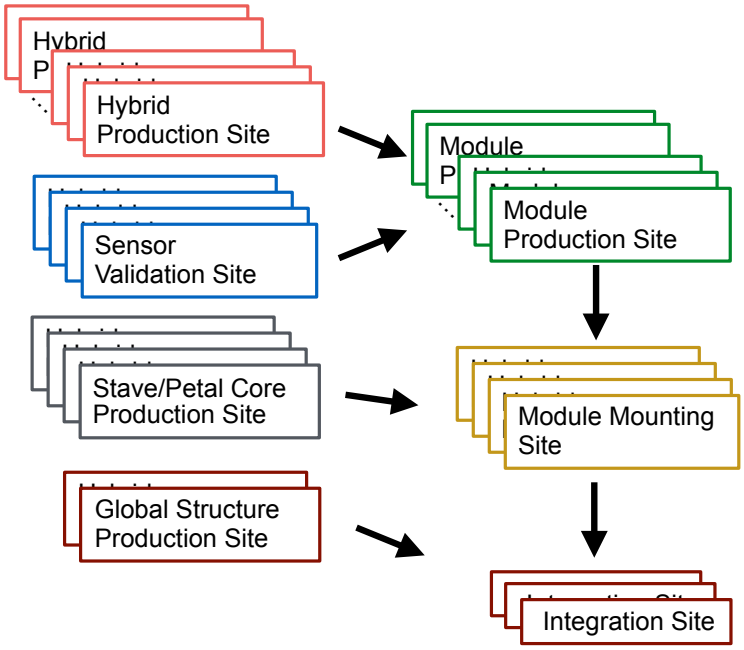


Figure 13.3: Schematic outlining the interdependency of production sites for the building of assembled staves and petals

Table 13.2: Intended Number of Production Build Sites for the ITk Strip Detector

Item	**Sites**
Sensor Testing	4
ABCStar Wafer Probing	2
HCCStar Wafer Probing	2
Power Board Assembly	2
Barrel Hybrid Assembly	2
End-cap Hybrid Assembly	2
Barrel Module Assembly	8
End-cap Module Assembly	7
EoS Card Assembly	2
Barrel Bus Tape Testing	2
End-cap Bus Tape Testing	2
Barrel Core Production	2
End-cap Core Production	2
Barrel Module on Core Assembly	2
End-cap Module on Core Assembly	2

13.3 Production Rates of High Volume Items

There are several steps of the production - sensor probing, hybrid and module assembly - that require a high number of parts, and consequently necessitate high production rates. For this reason an effort has been made to maximise the industrialisation and parallelisation of all steps. Examples include the manufacture of multi-hybrid panels (Section 6.3), the use of UV cured glue to minimise assembly time (Section 7.2) and multi-module testing crates (Section 7.6.7). For each component, production yield is taken into account, i.e. the scope of delivery depends on the yield for that part together with the yield of all subsequent assembly steps which might result in a good part not making it into the final detector. An example would be a hybrid glued onto a silicon sensor. If the sensor gets damaged during wire bonding, module testing, module mounting, Local Support testing or integration that hybrid (possibly two) is lost. Production rates have been calculated for those tasks of the build that will demand high production throughput and taking into account the component-to-ATLAS yields. The data is presented in term of work days, where it has been agreed to take one production year as 200 days (40 weeks). Data are shown for the production length of three and a half years, with the number of required parts including yield estimates. Furthermore the ramp up of the production rates for certain items was modelled, with 50% of full rates for year 1, reducing the equivalent work days by 100.

Table 13.3: Required production rates per equivalent site per day for various high number items

Item	**Number**	**Equivalent Sites**	**Ramp up**	**Assumed Days**	**Rate / Eq. Site/ Day**
Sensors IV/CV	20665	4	no	650	7.9
Sensors Full Probing	2067	4	no	650	0.8
ABCStar (wafers)	670	1	In pre production	450	1.5
Barrel Hybrids (panel)	2284	2	year 1 @50%	550	2.1
End-cap Hybrids (panel)	1542	1	year 1 @50%	550	2.8
Barrel Modules	12688	8	year 1 @50%	550	2.9
End-cap Modules	7976	7	year 1 @50%	550	2.1
Barrel Cores	412	2	year 1 @50%	550	0.4
End-cap Cores	403	2	year 1 @50%	550	0.4

Table (13.3) shows the required build rates (per equivalent site per day) for the various high volume items in the build. These are average rates taking into account that the infrastructure at each site may vary. Compared to the experiences with the prototype production, all rates are conservative.

13.3.1 Item Rate Estimations

The following section will detail the recent work done with prototypes, as well outline production mode plans to show the necessary build rates for high throughput items are achievable within the 3.5 year production time.

Sensors

A range of sensors will have to be probed for characterisation studies before use for module production (two variants for the barrel and six for the end-cap). Custom probe cards used in semi-automatic probe stations will allow for high throughput of probing. Full sensor probing after reception is planned initially for 10% of all sensors. This will be reduced at a later time if appropriate. Current testing rates for prototype sensors indicate one sensor/day is achievable for such full scale measurements.

ASICs

ABCStar wafers will be probed using semi-automatic wafer probing machines, with an expected 470 ASICs per wafer. For the AMAC and HCCStar ASICs, full wafer productions are assumed. With less than twenty wafers for each, these are not considered as high throughput items. Studies from the wafer probing of ABC130 chips showed about 8 h/wafer in semi automatic mode is achievable.

Hybrids

Production will be divided into hybrid reception from companies, and then hybrid metrology, passive component stuffing, ASIC population, wire-bonding and testing at sites. The panelisation of the hybrids allows for parallelisation (up to eight hybrids/panel) of the wire bonding and testing steps. In addition, the envisaged use of UV curing glue reduces the assembly time, as well as the necessary jigging, vacuum lines and tooling for such high throughput rates. With wire bonding being the limiting factor, it is believed that a rate of three panels/day/site is achievable.

Modules

The module production is driving the overall production schedule due to the time required for wire bonding steps, the curing time of the hybrid to sensor epoxy, and the long-term testing. The time to produce a module is reduced due to the optimisation of the multi-module assembly, including the use of UV-cure adhesive, multi-module wire bonding jigs, the electrical testing of front-end bond failures whilst wire bonding, and the automation of module metrology. With these techniques it is envisaged that a build rate of 3.5 modules a day per site can be achieved.

Cores

For the ITk Strip Detector detector 392 staves and 348 petals are needed. The staves will require four different flavours of bus tapes (left/right and short/long strips). These bus tapes will be made in industry and the production time will be a few months. The tapes will be tested at all stages of production with a customised tape testing robot and identical systems will be used in both clusters. After testing the tape, it will be co-cured to a carbon-fibre skin. The straight cooling pipes will be produced in industry and all the finished cooling pipe assemblies will be produced in one institute. The production times for the cooling pipes will be determined at the end of the development phase but will not create a bottle-neck for production as the required time is expected to be much shorter that for the other items. The co-cured carbon-fibre skins and cooling loops will be assembled into staves. Preliminary studies indicate that a stave will take two weeks to assemble after the process has been optimised. Therefore each cluster will have parallel assembly of four staves, to allow an overall production rate of two staves/week.

Limited thermal cycling will be performed on all cores during production. Prior to production, extended thermal cycling will be performed to validate the design and manufacturing procedures. A small subset of cores (1%) will be used for QA studies, undergoing extensive thermal cycling. Consequently these cores will not be installed in the ITK. In addition, continuity tests on a subset of bus tapes will be performed during such QA thermal cycling.

Only two flavours of bus tapes are required for the petal (front and back side), since all the petals are identical in the end-caps, irrespective of their location. The bus tapes are also manufactured in industry. An identical tape testing robot as that used for the staves will be used for the petal bus tapes, before and after the co-curing with the carbon-fibre skins. Simplified tests will be also carried out on the completed petal cores. Cooling pipes will be also manufactured in industry, and cut and bent to shape at the core assembly sites. The lateral close-outs will be machined from pultruded carbon-fibre rods manufactured in industry. The remaining petal components will be manufactured in-house from commercial components (carbon-fibre honeycomb, high thermal conductivity carbon-foam, adhesives, and thermoplastic material for the petal locators). Studies suggest that a parallelised production will allow for a rate of two petals/week. In case that an increased production rate

can be achieved, the petal core production will take place in the initial phases of the production in order to avoid a bottleneck during the production. Similarly as for the barrel staves, infra-red thermal quality control testing is envisioned for the completed petals.

Power Boards and HV switches

The power board production consists of three steps: PCB manufacturing, loading and testing. A vendor will be identified and qualified during prototype assembly and will execute all three steps.The institutes will receive only fully tested power boards and will perform extended QA and stress tests on random samples. During pre-production 10% will be produced. The power board production depends on the following custom items: UpFeast2 DCDC regulator, AMAC2 chip, air coil, shield box and HV multiplexer switch. All parts should be tested before they are loaded onto the power board. Power boards will be produced and tested in panels of 25. Testing is performed at the vendor with a bed-of-nails structure and test system as well as quality control data will be supplied by the institutes. The vendor will perform heat driven accelerated life-time testing on random samples throughout the production. All panels will be burned-in at the vendor. Prototyping will use an FR4 base material, while pre-production and production will use kapton based flexible stickup.

Two candidates for the HV multiplexer switch are under consideration; a commercial GaNFET and a custom 3D Vertical JFET. The production time needed to fabricate and test approximately 18,000 switches for the barrel and end-cap will likely depend upon which candidate is selected. A two year production for the GaNFET and a two and a half year production for the 3D VJFET is assumed. Initial testing of the devices will be done by the manufacturer. Further testing of the devices will occur before and after they are mounted on the power boards and will be part of the final power board quality control by the ITk community.

EoS Electronics

In total 1552 end-of-substructure (EoS) cards are required.

Each card requires one VTRx+ hence 1552 VTRx+ altogether. The petals (384) and the long-strip staves (256) require one lpGBTx per side, while the short-strip staves (136) require two per side, so 1824 lpGBTx are required in total. All the components will already be tested at the manufacturer. The PCB manufacturing and assembly will be performed in industry and the total production time for the entire batch will be a few weeks. The main effort will be the testing of the assembled card. It is planned to have two test sites with several test set-ups each, which will allow testing the entire production including the burn-in and bit error rate tests in less than five months.

13.3.2 Re-Works

A very good reliability and high assembly yield will be validated for all components before launching production. The specifications will be validated against requirements and the necessary quality control procedures will be developed to allow pass/fail tests. The known assembly yield will then be used to fine-tune the appropriate number of parts to produce sufficient working components. Many components will be produced by industry and it will therefore be the industry's responsibility to produce the required number of working parts. For components assembled in collaborating institutes, stringent QC and QA criteria developed during the R&D phase will ensure that the production yields for most items will be high enough that failed objects can be put aside and will not need to be repaired, except in very exceptional circumstances.

For any repairs, there will be a hierarchy of scenarios which are linked to practicality and value. The yields will be closely monitored during the production phase, such that any unexpected problems will be detected and resolved. For instance it is envisaged that items such as bus tapes, power boards, sensors, HV multiplexers and stave/petal cores that are damaged will be rejected. For loaded hybrids, failed ASICs (ABCStar or HCCStar) will be replaced rather than rejecting the full hybrid. Only very simple minor repairs would be attempted on modules. For example any modules with failed ASICs would be rejected, but any module requiring replacement wire-bonds would be repaired. A possible scenario is that such repairs would happen during the end of the build phase, minimising any effect on production rates. For fully loaded staves and petals, failed assemblies would be put aside until the end of production. Only in the event that at the end of production, the yield was significantly lower than anticipated would repairs then be attempted. A possible repair mode would be the replacement of a bad module. Module replacement was envisioned during R&D and was a main driver on the adhesive choice. Such a repair would require expertise at the local site. It is expected from previous studies that it would take one day to remove and replace a module.

In general, repairs should be carried out by the same site that performed the assembly of part, where there is knowledge on the exact processes and methods needed for the repair, as well as attempting to limit wherever achievable additional shipments.

13.4 Production Readiness

The following section details the existing plans for production readiness, including, documentation, transport boxes, site qualification, build rates, and re-working.

13.4.1 Documentation

The documentation used for the ITk Strip Detector build is based on the previous SCT experience. It is planned that all production sites will have their own webpages, and this information will be aggregated into the corresponding central cluster site/database. This allows for greater control of parts and component stocks, and faster reporting of yield rates and possible build issues. Every part will have a unique identifier to follow the parts around. Travel sheets will be used for movement of objects throughout the build, and documentation will also be written outlining in detail the assembly and testing procedures needed for production sites. As an example, it is envisaged for module production sites the following documents shall exist and store in the ATLAS internal EDMS system;

- Module Assembly: operator's guide
- Module wire bonding guide
- Mechanical survey procedures
- Electrical testing procedures
- ESD and testing specifications
- Quality assurance document
- Qualification criteria for sites

13.4.2 Storage, Transport and Tracking

During production, there will be a large number of parts being transported between institutes. It is essential that all component parts are tracked, transported and then stored in an agreed way. Where possible all components (ASICS, hybrid panels, sensors etc) will be stored in line with the IPC/JEDEC J-STD-033B.1 standard [107] for storage of components. This requires

- < 5% Room humidity sustained
- Recovery to normal conditions < 1 h
- The use of dry air, N_2 and active desiccant

Consequently, many items will be stored in N_2 flow cabinets contained within clean rooms. To counter any electrostatic discharge (ESD) damage to components, electrostatic discharge protected areas (EPA) [108] will be established at all relevant build sites. All users and conductive objects nearby the EDS sensitive parts must be grounded, and no highly charging materials will be allowed in this area. After handling, completed objects will be returned to the low humidity environment, awaiting shipping and transportation to the next building site.

Transport and Shipping

During production there will be considerable movement of high value items between sites. Consequently shipping and transport strategies have been outlined for many areas of the production. Invaluable experience has been gained from shipping large quantities for the SCT, where there were no recorded losses or damages of shipped items.

Transport boxes are currently being evaluated and the goal is to keep a box below 10%rHum resp the dew point for 14 days at standard shipping conditions. Furthermore solutions are evaluated to keep accelerations of the modules in transport boxes below 16 g at all times. Figure 13.4 a shows the transport box designed for the barrel modules, which has successfully been used for shipping thermo-mechanical modules between the US, the UK and Germany.

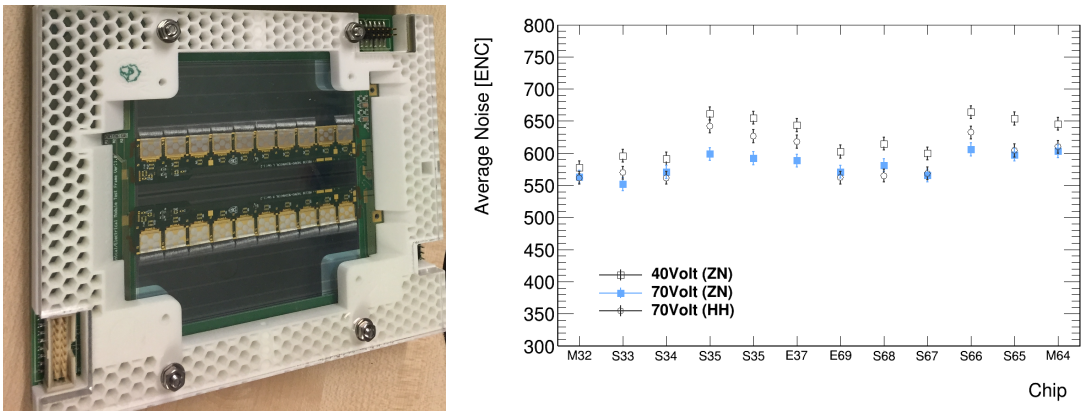


Figure 13.4: **Left**: Example of the transport frame for barrel strip modules; **Right**: Average noise per read-out chip as measured at voltages of 40 V and 70 V before and at 70 V after shipping between two production sites (HH=Hamburg, ZN = Zeuthen).

Testing before and after transportation of an end-cap module with 250 nm ASICS between two sites showed no degradation in electrical performance (see Figure 13.4 b) as would be expected from transport damage such as damaged sensors, broken or shorted wire bonds. Custom transport boxes also exist for hybrid panels, along with commercially available systems for ASIC wafers and sensors. Specifications exist for the shipment of local support cores along with the methodology for transportation of fully assembled stave and petals.

Expected Number of Transport Boxes

Work is progressing on the estimated necessary number of the reusable transport boxes for modules. The final figure will be strongly related to the build rate at clusters and frequency of shipping. If all barrel module sites sent all five day's worth of produced modules once a week it would require $\approx$ 130 boxes. With each production site having two spares per shipment it would then require $\approx$ 500 barrel module boxes and $\approx$ 240 end-cap module boxes.

The boxes are reusable and downtime for shipment is taken into account for the estimate of the required boxes. An additional number of boxes will be produced as contingency against any delays to module mounting or integration rates

Tracking

To assist with tracking, all hybrids will be mounted with a Radio-frequency identification (RFID) chip[1)]. It incorporates industry standards IC, and supports a frequency range of 865-955 MHz, allowing to cover all globally relevant UHF frequency bands.

This allows for a hybrid (or subsequently assembled module) to be coded with information such a serial numbers, test results or institute history. Information contained on each hybrid will then be written or read out out with a RFID reader at the relevant institute. For larger items (such as staves & petals), barcodes will be used for item identification. For both barcodes and RFID, item identification will use serial number codes, which are outlined in the next section.

13.4.3 Site Qualification

Before production starts, every construction site that is expected to build or test components will have to pass a site qualification validation. This is designed to demonstrate that the particular site has the ability to build their deliverables and measure the uniformity of test results across several clusters/sites to understand assembly yields. Guidelines for the infrastructure including details for the required equipment and parameter ranges are provided to all sites. The key points of site qualification will include:

- All the necessary equipment, infrastructure and personnel to execute the task exists
- All documentation, operating instructions and component build sheet check lists exists
- Procedures for tracking components, uploading test results and evaluating yield statistics exist
- A demonstration of the ability to assemble a number of pre-production pieces that conform to the documented specifications
- A demonstration of the ability to manufacture components which give test results compatible with other sites and that conform to the documented specifications
- Verification that all results are in the production database and visible to all sites.

[1] LXMS31ACNA-010

- Site requirements, including climate control, ESD precautions, clean room specifications and storage facilities

For site qualification, it is envisaged that a small number of items shall be produced by each assembly cluster/institute before production begins.

As an example, a module assembly site will have to produce approximately five modules, satisfying every aspect of the electrical and mechanical specifications before commencing as a production site. The specifications for the modules are defined and documented in a reviewed ATLAS note.

13.5 Production Database

An important step for the success of the project will be the production database, which will be used to track the geographic location and utilisation of all parts during construction, as well as serve a vital function during operation for potential fault finding. However unlike for the current inner detector, there will be only 1 central database for the entire ITk, covering not only strip barrel and end-cap components, but also all Pixel and Common Mechanics parts.

13.5.1 Methodology

The ITk Production Database (PD) has been designed to be a centralised web application with an universal application programming interface (API). The ITk Production Database will be accessible from the web application or API (see Figure 13.5) All business logic, rules and configuration will be centralised in the ITk PD. The API will be fully documented and will be accessible to the 3rd parties.

Significant products (entities) of the ITk PD and their relations are depicted in Fig 13.6. The ITk PD will mainly store information about the components and assemblies (Staves, Petals, Modules, Hybrids, etc.). The component is represented by an item (e.g. ASIC chip) or batch (e.g. tape). Components or other assemblies can be combined into a new assembly. The database will facilitate tracking of iterations of a component/assembly during a production phase.

The ITk PD will allow to store test results and related information (attachments), as well as shipments of components and/or assembly status. The database will be designed both for the ITk Strip and Pixel Detector needs.

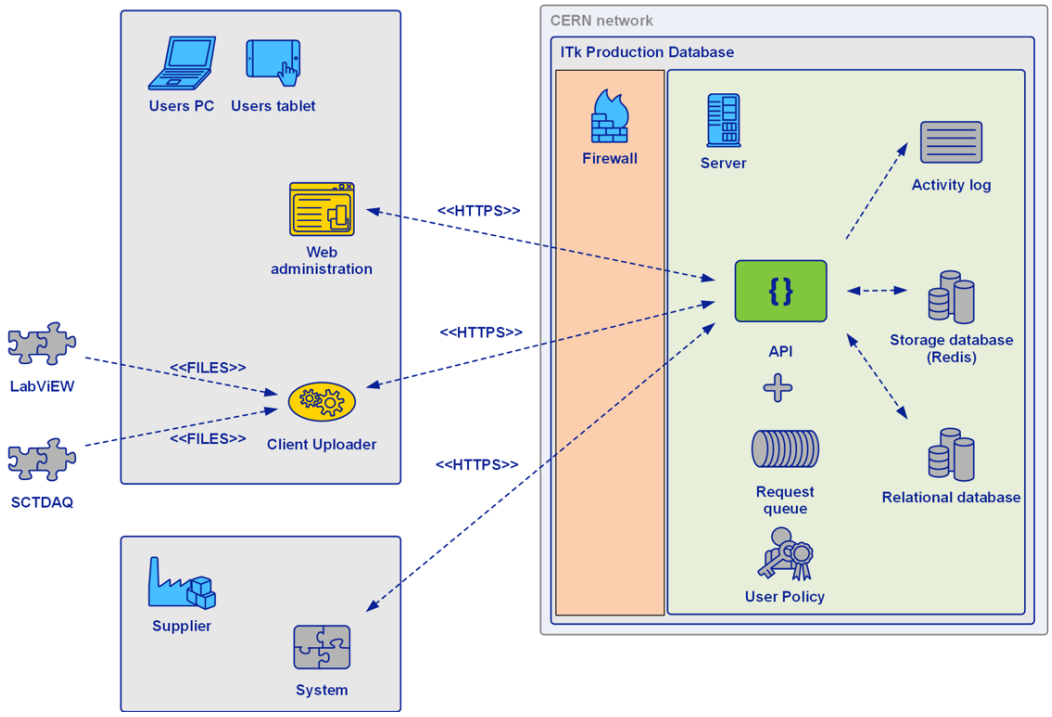


Figure 13.5: Suggested deployment diagram of the modified ITk PD

13.5.2 Key Features of the ITk Production Database

The main features of the ITk production database will

- have a centralised business logic,
- support tracking of shipments,
- allow management of access rights and user permissions.

13.5.3 Serial Numbers

The purpose of the serial number is to identify an item and relate it to a record in the construction database. Where possible the items should be labelled by a graphical code (bar, QR or similar code), which will be used to retrieve the corresponding record from the database. A serial number readable to humans is not required, although it might be convenient in some cases. Labelling by numbers will only be done where the space is easily available.

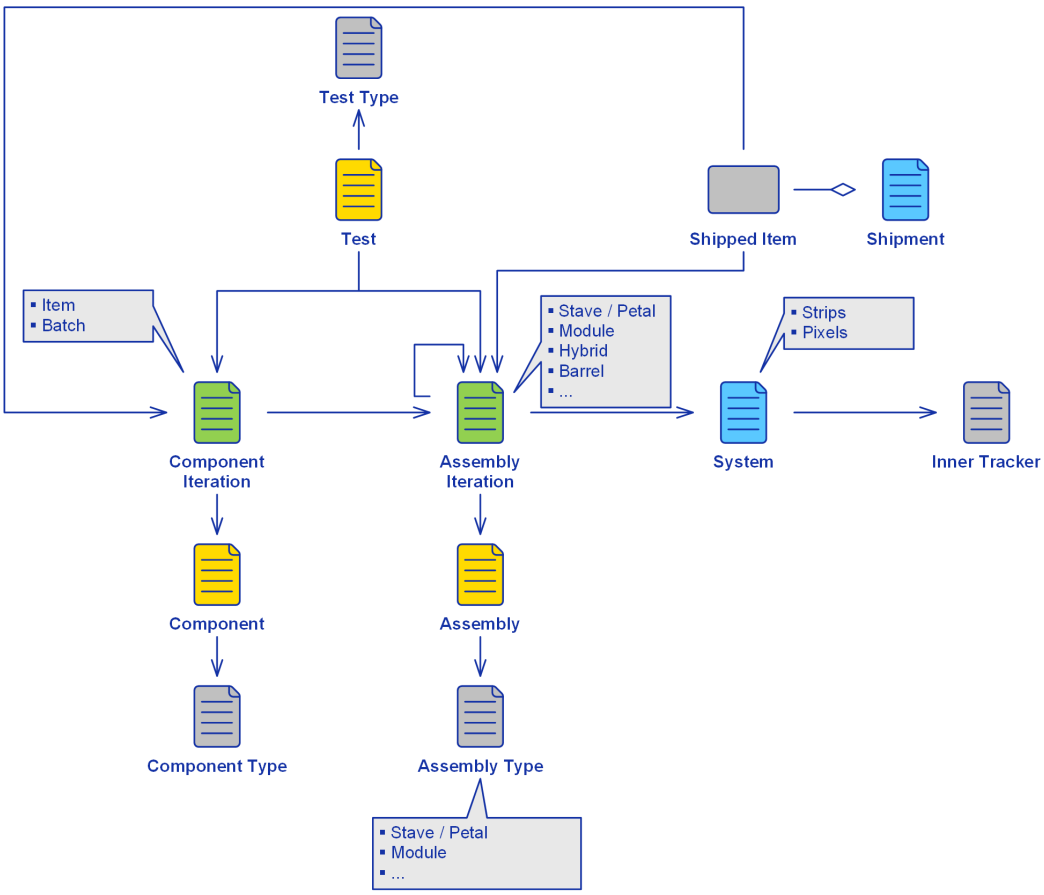


Figure 13.6: Suggested product view of the ITk PD

Expected Number of Parts

As has been discussed earlier in this chapter, the count of numbered items in the ITk will be less than 10^7. Note that the intention is that all items in the ITk will be traceable, which entails that more serial numbers will be needed than in the ATLAS ID, where many integration items were not numbered. In principle the numbering convention currently used in ATLAS with seven digits allocated for serial numbers appears sufficient for this.

Block Booking vs Randomly Allocated Serial Numbers

In the past serial numbers have been allocated by block booking. The disadvantage of block booking serial numbers is that it results in inefficient usage of number space, because serial numbers are typically chosen to allow for easy human identification, and even if this is not the case, paddings need to be included to allow for an overflow of part numbers (prototypes, spares, reworks, etc.).

Random allocation of serial numbers requires a central serial number allocation server, which is reliably accessible from all construction sites at any time. In practice this would be the construction database. However, as this database is still under development and not yet used by all aspects of the project, it seems that this service will not be available within the near future. While it would be beneficial to train users to use the database already from early on (also for prototypes) and the need to register items with the database for a serial numbers would provide such an incentive it is likely that without a real infrastructure in the database for certain items, users will not use this feature and rather rely on private, more or less organised ways to keep track of items. Therefore the current plan is to use block booking as detailed below. As a consequence a number space of 10^7 is expected, exceeding the number space in the old serial number scheme.

Alphanumeric vs Numeric Characters

The original ATLAS numbering scheme does in principle allow for the use of non-numeric characters in the serial numbers. In practice this has been avoided in the ID (even system, sub-systems and institute codes have been converted into numbers). However, the third digit for the 20 (ATLAS detector) serial numbers has been used in current ATLAS for the numbers 1-9. It seems therefore reasonable to start using alphanumeric characters in the more global designations of the item. However, for the actual serial number alphanumeric numbering schemes are likely to be not intuitive and could lead to misunderstandings.

Institute Identifiers

The ATLAS identifier used in current ATLAS detector uses institute identifiers. It has proven to be very useful for assemblies, which are taking place at one institute out of a larger group of possible production sites (typically for modules). However, for the ITk production it is planned to trace more levels of assembly and integration (modules, staves, barrels/disks, etc.), which can be spread over many different sites for one assembly. It is also planned to store data for assemblies which will only be produced at one site,even if there are only a small number of this assemblies being produced. In all these cases the reasoning for an institute code appears weaker. However, for assemblies where a human-readable institute identifier is deemed beneficial, the use of such an identifier as part of the serial number is going to be provided for.

Numbering Scheme

The following serial number scheme will be used: "20 U xx yy nnnnnnn" with details of the alphanumerics needed described in Table 13.4.

Table 13.4: Proposed Serial numbers for ITk.

20	Code ATLAS detector
U	Phase-II ATLAS upgrade
xx	project/subproject code PI - inner pixels PB - outer pixel barrel PE - pixel end-caps PC - pixel common SB - strip barrel SE - strip end-caps SC - strip common CM - common mechanics CE - common electronics
yy	sub-project specific block identifiers (could be MS for short-strip modules LA for A-side local supports etc.)
nnnnnnn	7-digit numerical serial number, A subset of these digits (TBD) can be used for an institute identifier (format and position to be defined)

13.6 Test Beam Studies at Pre- and Production Phase

The efficiency and functionality of modules have been studied in detail during the prototyping phase at test beam at DESY and CERN (see Chapter 8). During both the planned pre-production and production phase of the ITk strip system, test-beam measurements are also foreseen to be made. They will be conducted as part of the quality control procedures for small batches of assembled modules, as well as for system tests of larger objects. During pre-production the focus is more on understanding the devices and measuring their performance (such as the ABCStar), while during production test beams are a tool of quality control and testing of full segments of detectors.

13.6.1 Test Beam of Pre-production Components

During pre production it is envisaged that a test beam of both non-irradiated and irradiated end-cap and barrel modules, using ABCStar & HCCStar components will take place. In addition, test beam data is planned to be taken in a combined test beam with Pixel and Strip modules. Several modules of both detector components will allow testing of the common read-out and tracking performance, as well investigate any possible electrical interference between both detector types.

At a later stage in pre production it is planned for test beam campaigns for both a non-irradiated stave and a non-irradiated petal. They will not only probe the electrical performance but also test efficiency, charge collection and noise occupancy levels. In addition the resolution of the double-sided device with two sensor layers in final spacing can be obtained. Important tests like tuning the operating modes of the front-end electronics can be performed. Moreover, essential tests of shielding and grounding and read-out with external triggering can be achieved. It will also be possible to prove that no performance degradation of the modules due to the core structures can be measured.

13.6.2 Cosmic Ray Test Stand for Petals and Staves

In addition to particle test beam work, a cosmic ray test stand is planned to be set up. A stand allowing the mounting of several petals or staves will be constructed, and equipped it with scintillators on top and bottom for triggering and a TLU via read-out system. It will allow for the full reconstruction tracks through several detector layers. The test stand can be run continuously and measure not only efficiency showing functionality of the devices, but also giving an indication of the long-term performance of the objects under test. It is presently undecided where the set up will be. However, both CERN for stave tests and DESY for petal tests are possible sites.

13.6.3 Tests of a Detector Segment

Test of a detector segment which include several petals and several staves are important to develop common read-out and unveil interference effects. A test stand for segment tests needs to be set up and several electrical tests performed. The tests will include:

- Operation and read-out of several devices and optimisation of operating mode
- Cooling tests at different temperatures and the operation with CO_2
- Electrical interference of several petal/staves and electrical tests like noise occupancy, response curves
- Long-term tests to probe high voltage, temperature and performance stability
- Noise injection tests from the power line and from cooling pipes

13.6.4 Test Beams during Production

Test beam measurements of a small number of modules per annum are foreseen during production to check their continued performance characteristics. Data will be taken with non-irradiated and irradiated modules to monitor and guarantee the production quality. This will allow to conduct control studies on a small batch basis.

14 ITk Strip Detector Reliability Testing

All on-detector components will have to operate reliably for ten to fifteen years with little or no maintenance. Therefore ensuring high reliability of all these components is an essential part of our programme. This section gives an overview of our approach to reliability engineering and the resulting Quality Assurance programme. Brief descriptions of some of the proposed procedures are given.

14.1 Quality Assurance and Reliability

It is important to make a distinction between Quality Assurance (QA) and Quality Control (QC) tests that will be carried out during both pre-production and production. Quality control (QC) tests are performed on every production item, validating their performance compared to agreed specifications. The tests should include stress tests to eliminate or at best reduce infant mortality (eg ASICs). The QC for each component is described in the section in which the parts are described and this chapter focusses on QA. The definitions of Quality Assurance and Quality Control as used in this document are based on ISO 9000:2015 [109].

Quality Assurance (QA) tests are statistical studies of quality during R&D and on a batch basis in production. They are aimed at improving product reliability during R&D and monitoring consistency during production. This generally involves "destructive" testing which implies more extreme stresses for devices than will be experienced during normal ATLAS operation. The functionality of the devices will be measured before and after the stress tests. These will generally involve running the QC tests. The types of stresses used are typically, elevated or reduced temperature, rapid thermal cycling (sometimes called "thermal shock") and elevated operating voltages. The use of vibration testing to study mechanical reliability is also investigated. All on-detector components require radiation testing to validate the radiation tolerance. However the nature of the radiation testing is very device dependent and therefore these tests are described in the relevant sections of the TDR.

The specifications review (see Chapter 23) will include the strategy for Quality Assurance. Definite plans for numbers of devices to use for QA should be given in the Production Readiness Review, and similarly the Final Design Report will specify the number to be tested during the production.

Table 14.1: Examples of planned QA and QC tests for the Module components during the build phase.

Test	Sensor	ASICs	Hybrid	Module
QC	Probe testing	Probe testing	Electrical functionality Burn in	IV electrical functionality Thermal cycling
QA	Mechanical stress	Extended temperature and voltage	Thermal cycling	Thermal cycling

The tests are therefore considered destructive in the sense that these parts will not be used in the final detector, even if they are fully functional after the stress tests. The tests will be used on a statistical basis to validate the quality of the parts. Excessive QA failures during R&D will allow to optimise the design appropriately or look for alternative more reliable components. Tables 14.1 and 14.2 show examples of planned QA and QC tests for parts during the build.

Table 14.2: Examples of planned QA and QC tests for the stave/petal components during the build phase. HVIR = High Voltage Insulation Resistance, BER = Bit Error Ratio.

Test	Bus Tape	Cooling Tubes	Local Support	Optoelectronics
QC	Open / shorts HVIR Geometry	Pressure test Leak test	Geometry Bending stiffness Thermal performance	Power and responsivity BER and eye-diagrams
QA	Thermal cycling	Elevated pressure at -120°C	Thermal cycling	Elevated temperature and humidity

14.1.1 Common Voltage and Temperature Tests for all Objects

Since the ITk IDR, there has been a focus to standardise the voltage and temperature ranges used for all component testing across different components. This is done to guarantee all components are tested to the required limits, to avoid unnecessary testing as a component goes through the relevant assembly stages and allow sites to plan and purchase the necessary equipment.

Voltage Ranges

The sensor bias voltage is set to maximal 700 V. All silicon sensors will be tested up to this maximal voltage as part of the quality control. All cables and bus tapes providing the high voltage will be tested during the quality control to double the expected maximum operation value (i.e. at 1500 V assuming 700 V sensor bias and a 50V drop in the bias resistor). The factor two is a standard safety margin for HV testing.

Temperature Ranges

The coolant temperature is foreseen to be -35°C during normal operation. However the detector will be operated warm during integration and commissioning in order to be above the dew point. The increase in temperature from the cooling fluid to the active components is known from FEA calculations and thermal measurements. When switching the cooling on or off, the ramp rate is expected to be $\sim 1°C/s$. Therefore the rapid thermal cycling required for meaningful stress tests will involve significantly faster ramp rates. The temperature changes will cause dimensional changes in the structures and the effects of the resulting stresses will need to be studied.

14.1.2 QA for the Strip Sensors

The QA for the sensors is designed to study radiation damage, long term stability issues and the effects of mechanical stress.

- On a batch basis, sensors will be irradiated to 30% greater than the expected fluence to ensure that there is no deterioration in the radiation tolerance.
- The stability can be degraded by contamination or if the top metal layer is too thin. On a batch basis, sensors will be operated at high voltage beyond the maximal operation voltage for much longer periods of time than is practical for the QC tests of every sensor and the leakage current will be monitored for possible breakdown. In addition, humidity variation will be used in these studies.
- Mechanical stresses can cause increased leakage current because of micro-cracking and will be studied on a batch basis. The effects of handling and assembly will be simulated by repeatedly vacuum-attaching sensors to jigs/chucks and monitoring the IV behaviour to detect micro-cracking etc. The number of cycles used will simulate a multiple of the number of times sensors will be stressed in production.
- Stresses can be induced in the sensor when a hybrid is glued to the sensor and when the sensor is glued to the stave/petal. Some studies will be performed on a batch basis of sensors after they have been glued to hybrids. Repeated thermal cycles will be used to stress the sensors while monitoring the leakage currents. In a similar way studies will be performed of sensors glued to staves/petals.
- On a batch basis a thermo-mechanical module will be glued to a stave/petal. This will use staves/petals which were assigned for QA testing (see Section 14.1.7). The stave/petal will be subject to repeated rapid temperature cycling to stress the sensor and the leakage current will be monitored. The effects of temperature gradients will be monitored by measuring IV performance or the noise for sensors mounted on a module.

14.1.3 QA for the ASICs

The reliability of ASICs has not been a major concern for the current generation of experiments. However the reliability of newer deep sub-micron technologies might be worse because of the increased current density and the use of thinner gate oxides. The reliability of the current generation of GBTx will be studied using the standardised process as defined in Ref. [110].

The mean time to failure (MTTF) will be measured for batches of ASICs operating at different temperatures and elevated voltages. Different failure mechanisms have very different dependencies on temperature and voltage. For example hot carrier injection (HCI) is more severe at lower temperatures, while electro-migration is worse at high temperature. Therefore statistical fits will be performed on the MTTF data taken at different conditions to fit the relevant model parameters. These fits will then be used to predict the MTTF for the expected operating conditions. If these studies are successful, this methodology will be used for the production ASICs.

14.1.4 QA for the Hybrids

Hybrids will be produced in panels allowing for test structures to be laid out in the sacrificial area of each panel. Long lengths of narrow tracks will be used and the measurement of the resistance will monitor the quality of the etching. A daisy chain of a large number of vias will be included. The continuity of this chain will be measured before and after rapid thermal cycling in order to validate the reliability of the vias. Wire bond pull strengths will be measured on a batch basis.

14.1.5 QA for the Modules

The possible failure modes for a module that have not been already addressed by the hybrid and the sensor QA are the adhesion quality of the glue interface and the potential strain induced by the glue layer. The QA programme for modules will therefore involve peel tests of the glue as a measure of the adhesion. On a batch basis, modules will be subject to fast thermal cycling using a CO_2 cooling system. The electrical functionality after thermal cycling will be checked using the module QC tests. Modules which failed some of the electrical QC but were mechanically correct, will then be used for peel tests. The differences in the peel tests of modules that have undergone thermal cycling will be compared to modules that have not been thermally cycled.

On a batch basis, the bow of bare modules will be measured on a Smartscope before and after thermal cycling. Finally, it is considered to use liquid nitrogen insertion for a sample of modules that failed the electrical QC. Post-mortem analysis would be performed on modules that failed mechanically.

14.1.6 QA for the Bus Tapes

The radiation tolerance of the acrylic epoxy used to laminate the layers was studied by irradiating short length samples of laminated tapes. Peel tests were performed on samples with and without exposure to an ionising dose of 500 kGy(Si). A decrease in peel strength was observed after radiation but the peel strengths were still above the specification. In addition the robustness of the irradiated laminated tapes was checked by repeated insertion in liquid Nitrogen which did not create any delamination.

The bus tapes contain a sacrificial area which is removed at the end of the stave mechanical assembly. Long narrow lines will be laid out in this area for QA trials. The continuity of the long lines will be measured before and after rapid thermal cycling. A large area pad will also be included that can be used for wire bond pull strength trails. The first such tests on prototype tests gave excellent results with a mean pull strength of 10.0 g and an RMS of 0.88 g. These tests will be performed on a small fraction of the production tapes.

The reliability of prototype tapes is being assessed with rapid thermal cycling. A blow-off CO_2 cooling system is being used to rapidly thermally cycle a thermo-mechanical stave while the electrical resistance of all narrow lines are measured. The ramp rate is $\sim 3^{\circ}C/\mathrm{s}$. If this is successful, liquid nitrogen tests will also be used to achieve much higher ramp rates.

14.1.7 QA for the Local Supports

QA tests will be performed on completed cooling loops on a batch basis, probably using one assembly from each batch. A TRACI (recirculating) CO_2 system will be used for cooling cycles and thermal imaging of the cooling pipe assembly will be performed. This test would detect any blockages or flow restrictions in the tubes which would not have been detected by the pressure or leak tests performed during the QC. The cooling tube assemblies are designed to operate up to the limit of the rupture disks (186 bar). The tubes will be tested at 300 bar by the manufacturers before bending the tubes. However the bending is expected to slightly reduce the maximum pressure the tubes can survive, therefore a QA test will be performed on a batch basis using an intermediate value of the pressure. The actual value will be based on experience during the R&D stage. A post-mortem analysis would be carried out on any assemblies failing this test to determine the root cause. In addition an analysis of data from the individual components will be performed to see if the QC criteria should be tightened. For example this would allow examination of detailed IV data from the welding process, which could be used to optimise the process. The tube will be cut and polished to allow for a measurement of the diameter and out of roundness measurements. A visual inspection will be made to look for the effects of rippling.

The mechanical reliability of the local supports will be studied on a batch basis using rapid thermal cycling. This will be performed using a blow-off CO_2 cooling system, combined

with N_2 for warming cycles. The number of thermal cycles will be of the order of 100. The thermal performance before and after thermal cycling will be measured using the infra-red imaging used for the stave QC tests (see Section 9.8). We are also investigating the use of infra-red imaging during the thermal cycling. Pass/fail criteria will be based on the difference in temperature between the stave surface and the cooling fluid. The criteria will guarantee that the degradation in thermal performance is small and will not lead to thermal runaway. The actual value to be used will be determined based on trials with prototype staves. Visual inspection will also be performed to look for evidence of delamination.

14.1.8 QA for Optoelectronics

The reliability of VCSELs will be studied using accelerated ageing tests at 85°C and 85% relative humidity (RH)on a sample basis. The tests will measure the LIV (optical power, current and voltage) thorough the test. LIV scans will be performed periodically. Optical spectra will be taken before and after the test. Small changes in the widths of the spectra are sensitive to the loss of higher order modes, which has been demonstrated to be a very sensitive measure of VCSEL degradation. The tests will be run for at least 1000 hours which is sufficient to give high confidence in the long term operation.

First tests were performed with hermeticity packaged VCSELs[1)] in TO cans. 19 VCSEL channels were studied and they all survived 1300 hours of the 85°C and 85% RH test. There were no significant changes in the widths of the optical spectra after the test. In order to study the mechanical reliability, thermal cycling is being used. The temperature range was -35°C to +45°C, however the ramp rate was very low and therefore it is considered to use an air-jet system that could have a ramp rate of greater than 10°C/s. These tests are now being performed on a candidate small form-factor package which is not hermetically packaged.

The same tests will be used to validate new VCSEL packages being developed by the VL+ group. The reliability of transceivers will also be studied. A test system to allow 11 channels of VTRx to be tested simultaneously in an environmental chamber is used. The performance of the VTRx under test will be determined by a loop back system. Psuedo-random Bit Sequence (PSRB) data is sent from a VTRx outside the chamber, via an optical switch to a VTRx inside the environmental chamber. An electrical loop back is used for each transceiver so that the data is then returned to the VTRx outside the chamber, such that the Bit Error Ratio (BER) can be measured. The switch allows the one VTRx outside the chamber to monitor the performance of all eleven channels under test. This system will be used to study the reliability of the VTRx+ prototypes as they are developed. It will also be used to study the reliability of production items on a batch basis.

[1] Finisar HFE6x92-761

14.2 Radiation Testing during Production

All on-detector components which are susceptible to radiation damage will be studied in the appropriate radiation environment during the development phase. However it will also be essential to perform batch testing of components during production to validate the quality in terms of radiation tolerance. In general this will involve testing a small number of parts from each batch during production. The tests will be the same as those used during the development. This procedure will allow to interrupt production, in the unlikely event that the tests indicate that the parts fail the appropriate radiation QA. This is particularly relevant for parts which are not specified as radiation-hard by the manufacturer. The precise number of parts required and the definition of "batches" will depend on the nature of the part. However, in general the testing should be frequent enough to avoid building up deep pipelines of parts which might have to be scrapped. The detailed plans will be worked out during the remaining development phase but some indicative examples will be given to show how this strategy will be turned into practice.

- **Fibres.** If the fibres are COTs components as envisaged for the part of the fibre beyond PP2, a fibre sample from each preform will be irradiated to the maximum expected dose at this location including safety factor and the radiation induced attenuation (RIA) will be measured during the irradiation. The measured RIA versus dose will then be used to calculate the total RIA expected in ATLAS operation for the given fibre routing and a selection cut will be placed on this value.
- **Silicon sensors**. Each silicon sensor wafer will contain a miniature detector with a size of 1 cm $\times$ 1 cm. From each batch of sensors delivered a small number of these miniature detectors will be irradiated to the required fluence. The sensors will be read out with an analogue read-out system to check that their performance is as expected. In addition to this test, some sensors will be irradiated and regular IV measurements will be performed to check for evidence of early breakdown. The exact number of sensors to be used in this programme will depend on the available effort.
- **Glues**. Batch information of glues will be stored in the production data base in order to ensure full traceability. A glue sample from each batch will be tested for radiation, using the appropriate ionising dose.

15 Overview and Status of the ITk Silicon Pixel Detector

The Pixel Detector for the new ITk is situated inside of the Strip Detector (see Chapter 3). It consists of a central five-layer barrel region with four layers of rings composing the end-cap region. Although the final radial position of the pixel layers is still to be optimised, the innermost layers will be located very close to the interaction point and will be exposed to very large radiation levels as discussed in Section 3.4. In order to prevent early loss of physics performance due to radiation damage in the silicon sensors and to anticipate a possible extension of the operations beyond the current schedule, the two innermost barrel layers and the innermost ring layer will be removable and decoupled from the rest of the pixel system. To allow operation in such a harsh radiation environment new front-end electronics are under development within ATLAS and the RD53 collaboration [111].

The final layout of the ITk Pixel Detector is pending two important decisions which are being addressed (see Section 3.2.2): use of flat or inclined modules in the barrel layers, and angle coverage up to $|\eta| = 4.0$. In the inclined layout option tracks originating from the interaction point cross the modules at an angle close to normal. The extension at high $|\eta|$ is motivated by better tracking and physics performance using physics objects reconstructed in the very forward region. Based on the detailed studies done so far the "inclined" layout is chosen as baseline for the presentation of the tracking performance in this document (see Chapter 4). For completeness the technical details of both options are discussed in the following.

Intense detector R&D is still under way. Since the ATLAS Phase-II Upgrade was initially proposed in the Letter of Intent [1], major progress has been achieved in several areas and key technological options have been finalised. They are summarised in the following sections. The final detector design will be described in the ITk Pixel Technical Design Report that is due by the end of 2017.

15.1 Modules

15.1.1 Introduction and Requirements

The basic electrical unit of the ITk Pixel Detector is a module. The baseline module concept for the ITk Pixel Detector is the well proven hybrid pixel detector in which modules are composed of a sensor and the read-out chip (ROIC) bump bonded to each other on a pixel level. In addition other concepts are also investigated such as monolithic CMOS pixel detectors especially for the outer layers, see Section 15.1.7.

There will be two main types of modules: dual-modules (two chips bump bonded to a sensor, around 4×2 cm^2) for the innermost layer to accommodate the limited space, quad-modules (four chips bump bonded to a sensor, around 4×4 cm^2) for the outer layers and in the rings[1)]. 3D and planar sensors are considered for the innermost layers. For quad-modules in the outer barrel layers and outer end-cap rings the standard planar sensor technology is foreseen. The read-out chip is presently under development within the RD53 collaboration, which will produce an RD53 prototype chip. Following this chip an ATLAS ITk pixel chip will be developed using the basic blocks designed by RD53 while integrating additional functionality to meet ATLAS specifications. Figure 15.1 shows a sketch of a quad-module based on the previous ATLAS pixel read-out chip FE-I4 with 50×250 μm^2 pixel size. Due to ongoing development of the new pixel read-out chip its final size is not yet defined. For the time being, the same active size as for the FE-I4 pixel chip (16.8×20 mm^2) and a similar periphery region of 2×20 mm^2 are assumed. All connections (clock and command input, data output, low voltage and high voltage power) to the modules are done via a flexible printed circuit (flex-hybrid) which is glued to the backside of the sensor. The connections to the front-end chips and the sensor are done with standard wire bonds and passive components like decoupling capacitors and termination resistors are mounted on this printed circuit.

The relevant parameters for barrel and ring modules are listed in Table 15.1 assuming 50×50 μm^2 sensor pixel size for all layers[2)]. The fractions of inactive regions are kept low by having larger pixels at the edge and in the regions between chips, and by minimising the edge region while still preventing voltage breakdown. Sensor and ROIC thicknesses are a compromise between material reduction and radiation tolerance improvements (which favour thinner sensors) for the inner barrel and ring layers and increased production yield and handling (which favour thicker sensors and thicker ROICs) for the outer layers.

[1] Some layout or sensor options will in addition require single-chip modules (one chip bump bonded to a sensor, around 2×2 cm^2).

[2] The sensor pixel sizes given for each layer are for illustrative purposes. The actual sensor pixel size is still being optimised based on simulation studies, considering also 25×100 μm^2. Note that the read-out chip pixels are sized 50×50 μm^2 independent of the sensor pixel size choice.

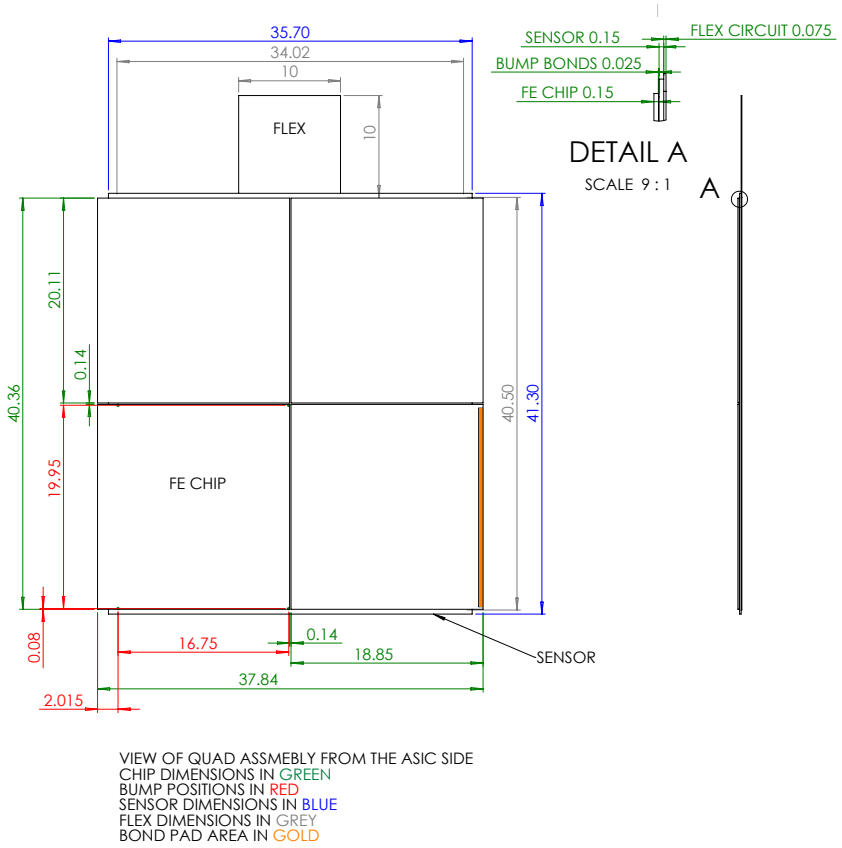


Figure 15.1: Drawing of a quad-module with four FE-I4 chips

Modules will be serially powered[3)], see Section 15.4, with the chips in each module controlled in parallel (shared clock and command inputs), but the module may have one or several dedicated data outputs. The multi-chip output data multiplexing functionality may be incorporated into the next generation pixel chips being developed or it could be implemented with a separate chip on the module as is done in current detectors.

Apart from the sensor (Sections 15.1.2 and 15.1.3) and the front-end electronics (Section 15.1.4) the key step in the classical hybrid pixel module integration is the fine pitch flip-chip bump bonding process which connects each pixel sensor with the corresponding front-end readout cell. Bump bonding requirements for the Phase-II layout will be similar to those of the IBL modules, but experience with the present Pixel detector and the IBL production showed the importance of multiple qualified bump vendors, see Section 15.1.5 for more details.

[3] The power specified in Table 15.1 refers to serial powering with the difference in power between inner and outer layers being caused by higher activity of the digital part and the consumption of the drivers for the high speed data links needed only for innermost layers. Power numbers are given as used for the design phase but will be better understood after the RD53-A prototypes are produced which are designed for less than 1 Wcm^{-2}.

Table 15.1: Basic parameters of the pixel modules for the ITk pixel system.

Parameter	**Layer 0**	**Layer 1**	**Layers 2 - 4**	**Rings**
Chips ($\phi \times z$)	RD53-FE 2x1	RD53-FE 2x2	RD53-FE 2x2	RD53-FE 2x2
Pixel size (μm^2)	50 x 50	50 x 50	50 x 50	50 x 50
N_{pixels} in ϕ	336	672 + 6 ganged	672 + 6 ganged	672 + 6 ganged
$N_{\text{doublecolumns}}$ in z	400	400	400	400
Sensor length at gap (μm)	300	300	450	450
Distance to module edge (μm)	150	150	500	500
Distance active to cut edge (μm)	100	100	100	100
Active size (mm^2)	16.8 x 40.3	33.9 x 40.3	33.9 x 40.5	33.9 x 40.5
Physical size (mm^2)	18.8 x 40.5	38.0 x 40.5	38.0 x 41.5	38.0 x 41.5
Sensor thickness (μm)	100 - 150	100 - 150	200 - 250	100 - 250
ROIC thickness (μm)	100 - 150	100 - 150	200	200
FE Power (W)	5.5	11.0	7.8	7.8

Depending on the final layout decision of the ITk Pixel Detector, about 10,000 hybrid pixel modules are needed. High throughput and efficient assembly processes are mandatory. Therefore the ATLAS groups are pursuing an extensive prototype programme on quad-modules [112], as well as high volume bump bonding using FE-I4B wafers with several vendors. More than 100 wafers had been added to the IBL production order for such R&D efforts world-wide (the production order of 96 FE-I4B wafers contained more pixels than the present ATLAS and CMS detectors combined), as discussed further in Section 15.1.6.

In many areas of the module development alternative approaches are being investigated. Among these are four side buttable dual- and quad-modules with Through-Silicon-Vias (when micro holes are produced after transistors and in a different factory). Such modules will relax the constraints on the mounting of the modules on the stave and potentially reduce the material budget. ATLAS pixel institutes evaluate alternative hybridisation methods like capacitive coupling and industrial 3D integration processes as well as direct laser soldering to replace standard wire-bonding technology between module and flex-hybrid.

15.1.2 Planar Pixel Sensor Technologies

A new generation of planar pixel sensors are under development for the ATLAS ITk pixel system. The main differences with respect to the planar sensors implemented in the present detector are the different electrode arrangement (n-in-p versus the traditional n-in-n) and the reduced thickness in the range of 100-150 μm with respect to the 200 μm for the sensors used in IBL and 250 μm in the three outer ATLAS pixel layers. This work builds in part on the research performed within the RD50 collaboration [113].

The n-in-p technology allows for cost reduction given the single side processing and the reduced complexity in handling and testing. The guard ring structure is implemented on the front side, leaving the edges of the sensor at a potential close to the one of the backside. This arrangement potentially induces the risk of electrical sparks between the sensor periphery and the chip. Isolation techniques, like the deposition of a layer of Benzocyclobutene (BCB) on the sensor surface at wafer level or of parylene after module assembly have been successfully employed to prevent this problem [114, 115].

Several studies have been performed to optimise the pixel cell structure in view of the smaller pitch of the read-out chip developed by the RD53 Collaboration (see Section 15.1.4). Two pixel cell structures are being investigated, 25×100 or 50×50 μm^2 cell size, the latter being the baseline option. New designs of planar sensors with 25×100 or 50×50 μm^2 cell size, (see Figure 15.2), based on beam test results obtained with the FE-I4 chip, have been implemented in prototyping productions already under process or completed.

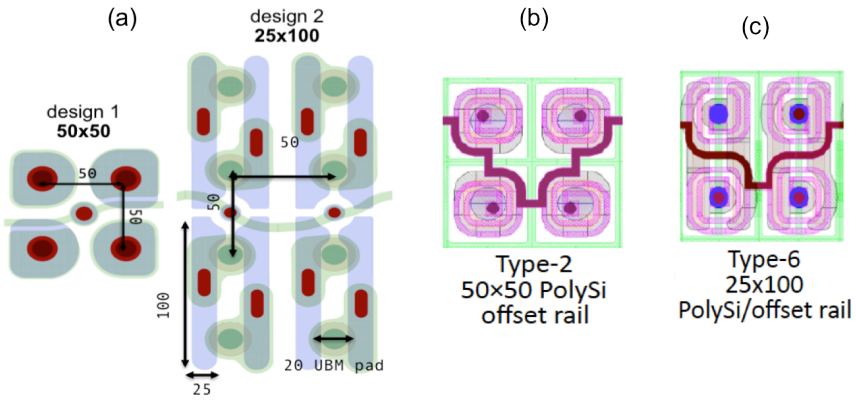


Figure 15.2: Design of 50×50 μm^2 and 25×100 μm^2 pixel cells implemented in (a) a sensor production with a common punch-through for four pixels, and (b, c) in a productions with Poly-Silicon resistor biasing, among other variants. In (a) the n^+ implant is shown in light blue, aluminium in green, and contacts through the silicon oxide and nitride layers in red. In (b, c) the n^+ implant is shown in light grey, the p-stop in green and the poly-silicon in pink.

Preliminary results of the electrical characterisation of these devices can be found in Ref. [116]. The cell optimisation has been particularly focused on the biasing structures that induce a

reduction of the efficiency after irradiation, for pixels where a punch-through dot or a poly-silicon resistor were implemented. Better performances have been demonstrated with a punch-through structure common to four cells or with a displaced bias rail in the case of the poly-silicon resistors [116–118].

Thin planar sensors have been irradiated up to a fluence of 10^{16} n_{eq}/cm^2 to investigate the feasibility of employing them in the innermost pixel layers [119]. A hit efficiency up to 97 % with FE-I4 modules has been reached in test beam measurements by 100 μm thin sensors at a bias voltage of 350 V for a fluence of 5×10^{15} n_{eq}/cm^2. Comparing this performance with

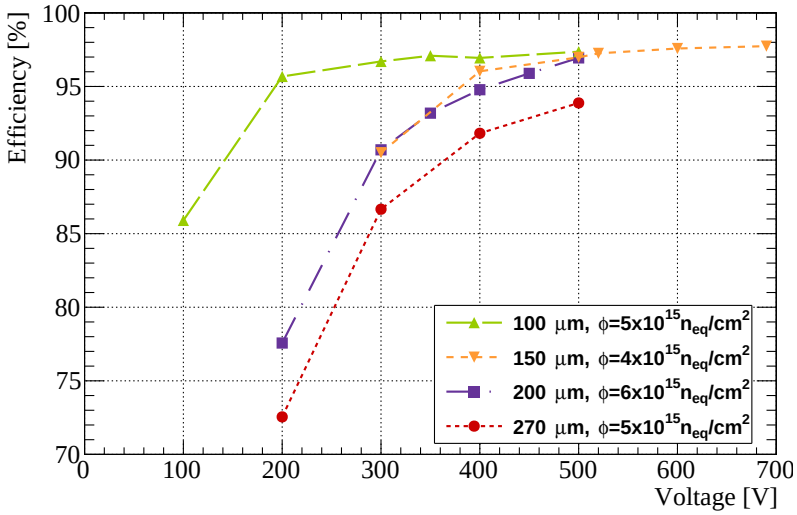


Figure 15.3: Comparison of hit efficiencies obtained with planar pixel sensors of different thickness interconnected to FE-I4 chips after a fluence of approximately 5×10^{15} n_{eq}/cm^2.

those of thicker sensors, as shown in Figure 15.3, it is evident that 100 μm thin sensors can provide the same tracking efficiency at lower bias voltages. At a fluence of 10^{16} n_{eq}/cm^2 500 V are needed to reach a hit efficiency of 97% in test beam measurements. Based on this result, the power dissipation has been estimated to be in the range of 25-45 $mWcm^{-2}$ at a temperature of -25°C for a sensor after 11 days of annealing (see Figure 15.4).

Pixel sensors with implanted sides to extend the depleted volume to the physical edges are also investigated for the innermost layer, where the maximisation of active module area is particularly relevant [114, 120].

Layers 1 to 4 in the new pixel system will be instrumented with quad-modules with a single sensor interconnected to four chips. Quad sensors compatible with FE-I4 chips have been produced at different vendors and good yields have been obtained also with these large area (around 4×4 cm^2) devices. Various inter-chip distances, in the range of 180-280 μm, have been used in the design of the sensors by implementing different number of ganged

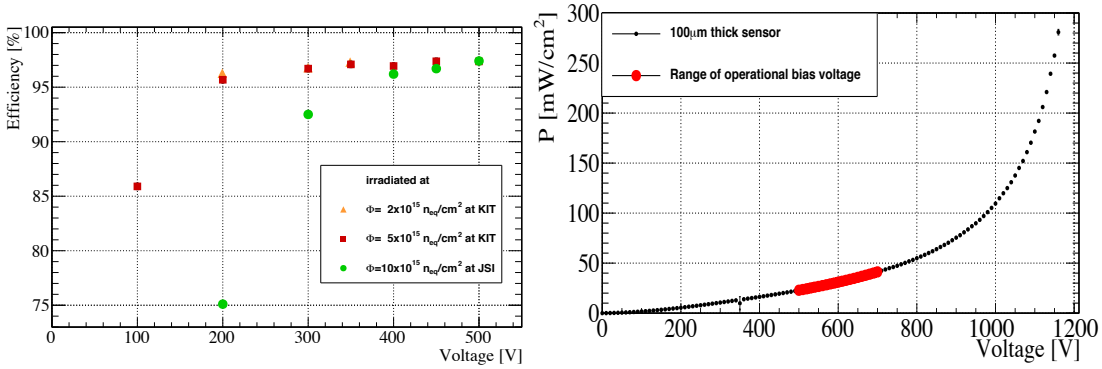


Figure 15.4: **Left:** Comparison of hit efficiencies of FE-I4 modules with 100 μm thin planar sensors irradiated from a fluence of 2×10^{15} n_{eq}/cm^2 to 10^{16} n_{eq}/cm^2. **Right:** Power dissipation estimated for 100 μm thin sensors at a temperature of -25°C irradiated to a fluence of 10^{16} n_{eq}/cm^2, where the range of possible operational bias voltages is based on the results shown in (left). The values of the leakage currents used in the calculation are for a sensor after eleven days of annealing at room temperature.

pixel rows in the sensor central area. The design of the inter-chip region will then have to be adapted to the finer pitch of the RD53 chip.

15.1.3 3D Pixel Sensor Technologies

3D silicon detectors are candidates to be used for the inner most layer(s) of the barrel pixel system and some of the inner end-cap rings due to their excellent radiation hardness at low operational voltages and moderate temperatures with low power dissipation compared to planar sensors. 3D silicon detectors have recently undergone a rapid development from R&D to industrialisation with their first operation in the IBL.

IBL-generation 3D pixel detectors coupled to FE-I4 pixel electronics have been found to have hit efficiencies in test beam measurements larger than 97% at 170 V after irradiation to 10^{16} n_{eq}/cm^2 for normally incident minimum ionizing particles with a power dissipation of 15 $mWcm^{-2}$ at a temperature of -25°C [121], see Figure 15.5.

The 3D design under development for the ITk detector builds on the successful IBL 3D sensor. Columns of 5 to 10 μm diameter are alternately n- and p-type doped into the high resistivity p-type silicon bulk, defining the pixel configuration. In the IBL 3D sensors, the columns were etched from both sides of the wafer (double sided process), which allows production of sensors with thicknesses down to 200 μm. Moreover, the single sided approach on a support wafer is also well established at several 3D fabrication facilities, which allows for thinner sensors. Active thicknesses of 50-200 μm are currently being investigated at various production sites. The 3D sensor technology inherently allows for slim edges of 15-150 μm [122], or even active edges sensitive up to the physical sensor edge [123].

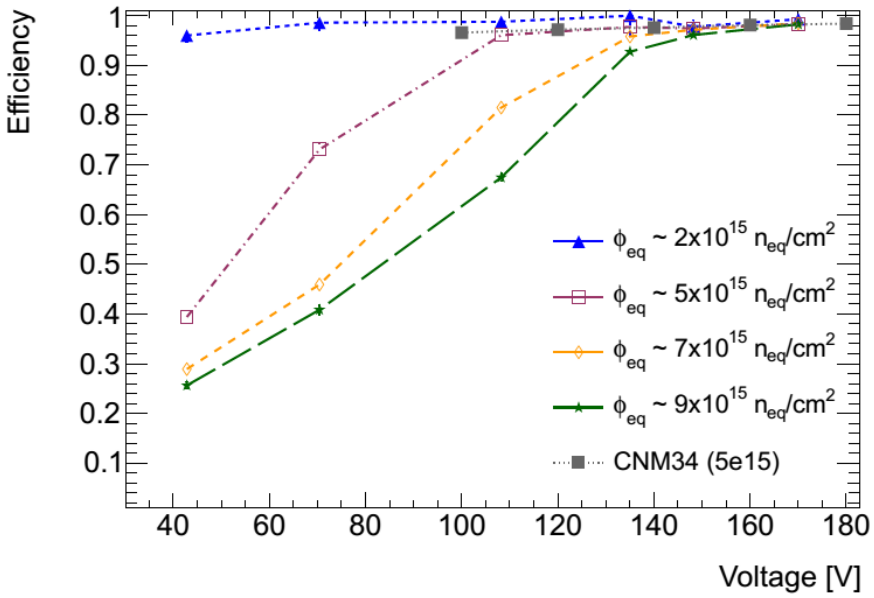


Figure 15.5: Hit efficiency as a function of bias voltage for different fluence regions on a non-uniformly irradiated 3D FE-I4 detector. For reference, the efficiency of an IBL 3D device from the qualification phase (CNM34), irradiated with protons to 5×10^{15} n_{eq}/cm^2, is also shown.

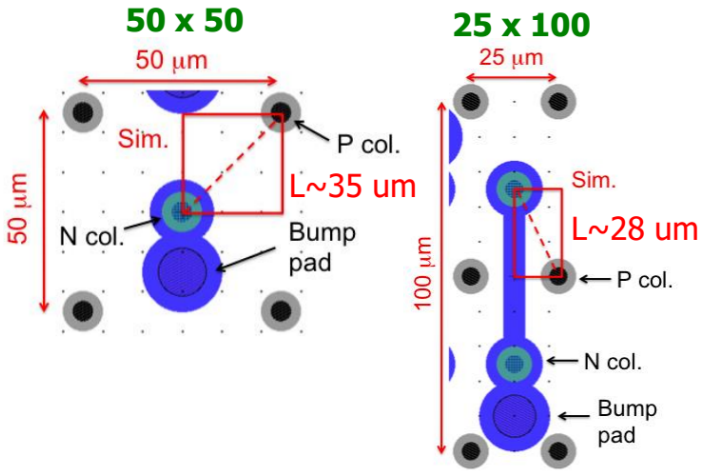


Figure 15.6: Design of 3D pixel cells with 50 × 50 and 25 ×100 μm^2 size.

Productions of 3D devices with smaller pixel sizes of 25×100 and 50×50 μm^2 compatible with the FE-I4 chip have already been carried out and the prototypes are currently being tested [121, 124, 125]. Furthermore, specific productions of 3D sensors compatible with the RD53 chip, design shown in Figure 15.6, have also been completed.

Though performance is the decisive factor for the relatively small size of the innermost pixel layers, the 3D technology is reducing its cost and production time, while improving the yield, by optimising the 4″ production line and establishing new 6″ lines [124, 125].

15.1.4 Pixel Front-End Electronics

The RD53 Collaboration [111] is developing the pixel read-out chip technology for both ATLAS and CMS usage at the HL-LHC. This is a critical path item for both experiments. A first large format chip to demonstrate the results and allow the experiments to test sensors meeting HL-LHC requirements, called RD53-A, is planned to be submitted at the end of March 2017 and delivered by the end of June 2017. Detailed specifications for the RD53-A were approved by both experiments and released as a public document in 2015 [126]. The RD53-A chip embodies the main deliverable of the RD53 collaboration. RD53-A will be produced in wafer form, allowing development of wafer testing on 300 mm diameter wafers. Significant testing of the RD53-A chip and hybrid modules built with RD53-A chips will take place in 2017/18. Even though many important tests will be possible with RD53-A modules, this will not be sufficient to fully qualify the new pixel module design, as the chip will be too small and missing a number of crucial read-out features. The ATLAS design team will directly proceed to the design of the final chip relying heavily on RD53-A, successively incorporating test results, and using the tools, basic blocks, and design environment provided by RD53. It is assumed that the design phase will start mid-2017 and will take 18 months; as a consequence, the ATLAS Pixel read-out chip will be submitted by the end of 2019. The schedule foresees two ATLAS ITk pixel chip submissions, with the second being the production chip. After initial on-wafer testing, the pre-production of modules using the final components will start in the second half of 2020. The pre-production phase (between 10% and 15% of the modules needed) will last one year, so the production of modules to be used in the ITk will start in the second half of 2021.

While the plan is to use the same read-out chip in the entire detector, the most critical performance requirements are driven by the innermost layer. Compared to the FE-I4 chip [127] used in the present inner layer (IBL [128]), the HL-LHC requires large improvements in several parameters at once. The new pixel size must be 20% that of FE-I4, essentially due to the 5-fold increase in particle flux (by comparison, the FE-I4 chip pixel size is only 63% that of the original Pixel detector). Yet at the same time, the hit threshold must be drastically reduced to 600 electrons instead of 2000 electrons (in response to thinner sensors and heavy sensor radiation damage), all without a significant power increase. Additionally, the trigger rate will be increased by an order of magnitude. Therefore, while the read-out bandwidth of one FE-I4 chip in the IBL is 160 Mb/s, the new inner layer will require an estimated 5 Gb/s

per chip (not only is the trigger rate increasing from 100 kHz to 1 MHz, but the events are also busier, while the chip size is assumed to the the same as FE-I4). The magnitude of these challenges was recognised early on, and the RD53 collaboration was formed to attack them. A 65 nm feature size CMOS technology (through a CERN frame contract) was selected to address them. Several alternative candidate platforms were also investigated, including 3D silicon integration with 130 nm feature size as a candidate solution.

High radiation tolerance is of course a critical requirement. Following the initial studies of the chosen 65 nm feature size process, more detailed and extensive studies by RD53 and the CERN Microelectronics group revealed some unexpected issues, including a previously unknown effect now called Radiation Induced Short Channel Effect or RISCE [129]. Like the already known Radiation Induced Narrow Channel Effect (RINCE [130]), this is a fundamental CMOS damage mechanism, not peculiar to any vendor or foundry. These two effects together mean that the thing that is necessary for high logic density, namely small transistors, is bad for radiation tolerance. High logic density is mandatory to have small pixels with high hit rate and long trigger latency. Fortunately, with only modest compromises on logic density (still much higher density than could be achieved in FE-I4), the RD53-A design meets the specifications after 500 MRad dose. This value stems from the fact that RD53 has developed simulation models for transistors up to this dose. Simulation beyond 500 MRad is much more difficult because degradation becomes highly dependent on voltage and temperature conditions and history. Of course, the RD53-A chip will be tested beyond 500 MRad. Nevertheless, a design with removable inner layers is prudent at this time, since performance beyond 500 MRad is uncertain. At the same time, work on radiation damage continues. A particular focus is understanding low dose rate damage and annealing effects. For the CERN frame contract 65 nm CMOS process, annealing under power (after initial irradiation) causes additional degradation. This is not an issue for low temperature operation, but it does appear to be a vendor-specific effect, demanding further scrutiny. It is interesting that sensor radiation damage also becomes uncertain after 10^{16} n_{eq}/cm^2 (same luminosity as 500 MRad), and mitigation also requires cold operation, in spite of completely different damage mechanisms.

While the RD53-A chip is the main prototype that the production read-out chip will be based on, a small scale demonstrator called FE65-P2 [131] was produced in a multi-project run in late 2015, with miniature first sensors bump bonded in mid 2016. FE65-P2 has the same pixel size and same CMOS process as RD53-A, and was intended to demonstrate the layout approach where digital logic completely surrounds 4-pixel amplifier blocks called "analogue islands in a digital sea", which allows to synthesise the digital logic as one flat block. FE65-P2 also demonstrates the performance of the analogue front-end to be used in RD53-A and validates the superb analogue-digital isolation needed for 600 electron threshold stable operation. It contains several front-end variants to allow comparative measurements and optimisation. The per-pixel threshold was found by injecting charge of varying magnitude through a built-in calibration circuit. Charge injection was repeated 50 times at each value and the response (number of hits) of each pixel was registered. The

result is a sigmoid curve for each pixel showing firing rate vs. injected charge. These data were fit to an error function (s-curve), with the mean being the threshold and the width the noise (sigma). The discriminator threshold of a bare FE65-P2 was tuned to values below 600 electrons with a dispersion of 30 electrons, see Figure 15.7. The average extracted equivalent noise charge is 35 electrons, given in Figure 15.8, which will increase when a sensor is attached by an amount depending on the sensor capacitance.

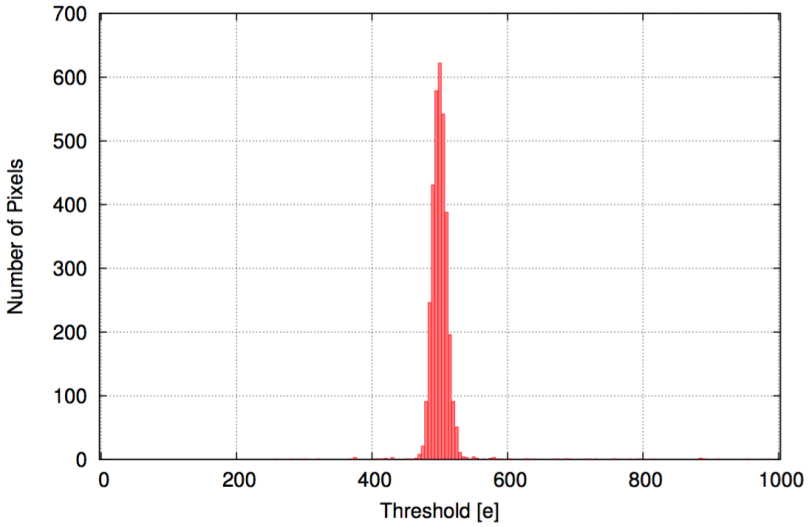


Figure 15.7: Threshold distribution of a bare FE65-P2 chip.

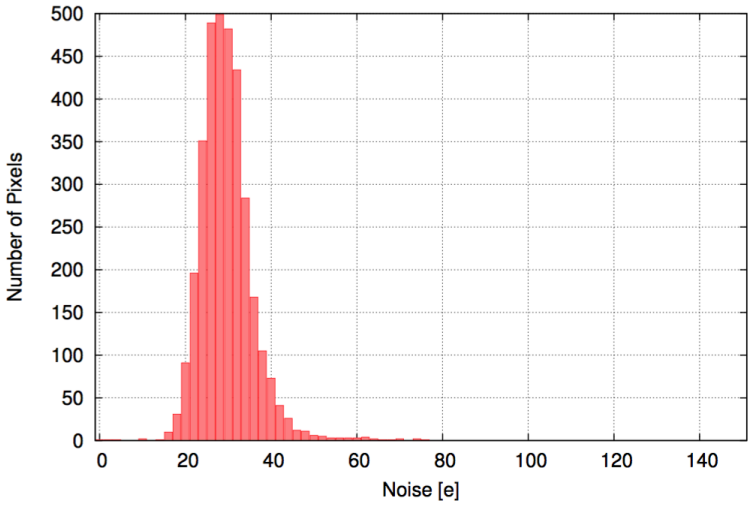


Figure 15.8: Equivalent noise charge of a bare FE65-P2 chip.

While a significant temperature variation of the threshold is observed on irradiated chips, pixels with a "radiation hard" front-end variant show the smallest effect, at a level accept-

able for operation. Threshold shift (and dispersion increase) during irradiation is initially 100 to 200 electrons per MRad at a high dose rate (10 times HL-LHC), but lower at lower dose rate, and that is considered acceptable. Figure 15.9 shows the shift in threshold mean as a function of absorbed dose. The chip was retuned after 1 MRad and then further irradi-

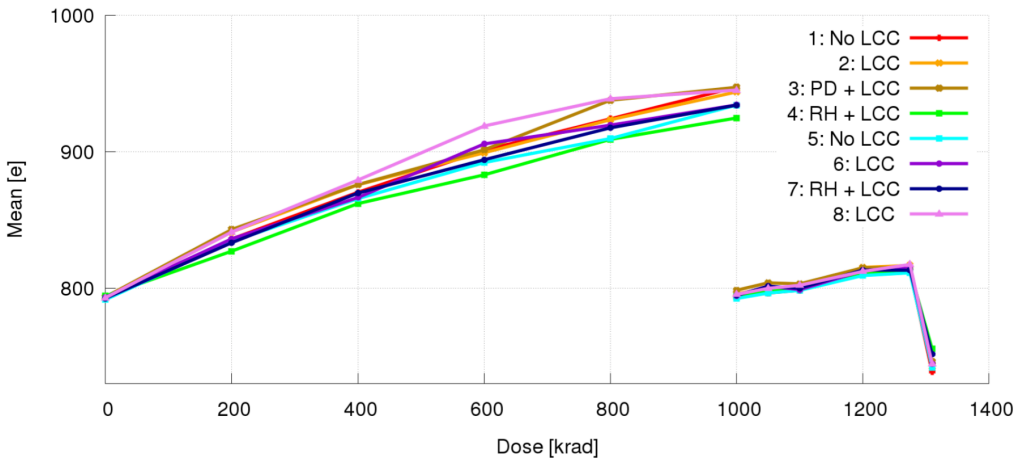


Figure 15.9: Threshold mean per radiation dose for a non-irradiated chip. At 1 MRad the chip was retuned and dose rate decreased. At 1.3 MRad the temperature increased to 20 °C.

ated at half the original dose rate. The effect of the lower dose rate can be seen in the smaller slope from 1 to 1.3 MRad. The sharp decrease at 1300 krad is due to a temperature increase to 20 °C as the device was removed from the setup, serval curves are shown for different Pixel designs. Furthermore, as accumulated dose increases, the radiation threshold shift decreases: it was found to be negligible on chips previously irradiated to 150 MRad and 350 MRad. Generally, performance is still good after 500 MRad. The threshold to detect a charge pulse within 25 ns was measured to be below 500 electrons for a discriminator threshold of 300 electrons.

A number of FE65-P2 chips have been bump bonded at SLAC to planar sensors from Hamamatsu photonics. The modules show a small increase in noise with nominal noise achieved at a bias voltage of -10 V (full depletion expected at -300 V) which confirms expectations that the noise performance is most sensitive to the inter-pixel capacitance. Data were successfully taken with a 50 MeV proton beam which shows pixel hit clusters the size of which matches the expected depletion depth. These excellent results with FE65-P2 give significant confidence in the RD53-A design.

15.1.5 Interconnection Technologies

A key step in the fabrication of the hybrid pixel assembly is the flip-chip bump bonding process. There are two major challenges facing the flip-chip bonding of the ATLAS pixel system. The first is the technical challenge posed by the requirement to produce very thin pixel assemblies targeting 100 - 150 μm for the inner layers. The second challenge is the production rate and volume required for the substantially enlarged pixel system.

The specifications for the bump deposition and flip-chip process are under development based on those successfully used for the IBL production [132]. Additional requirements include increased wafer sizes: 300 mm diameter read-out chip wafers (increased from 200 mm), sensor wafers up to 200 mm diameter (increased from 100 mm). Furthermore the read-out chip and sensor thicknesses are reduced to 100 - 150 μm, and the bump density is five-fold increased due to the bump contact pad pitch of the read-out chip of 50 μm in both directions. These additional requirements will impact on both the bump realization and the flip-chip processes. However, the bump failure rate is expected to remain the same as for the IBL for which on average approximately 0.56% of pixels on accepted planar modules failed during QA tests.

The details of the manufacturing process are being developed in collaboration with the vendors that the pixel groups are working with during the R&D phase. The pixel specifications will not place a requirement on the detailed technology used but will assess the quality of the product via a qualification process. The qualification process will be based on that used for the IBL, but will additionally include a HALT (Highly Accelerated Life Test) and HASS (Highly Accelerated Stress Screen) programme and will take into account the lower operational temperature of the modules. A development programme based on the FE-I4 wafers is being used for the first stage of vendor engagement. A bump test structure is under development on 300 mm diameter wafers to allow process development at the final wafer diameter before the delivery of a significant number of RD53 chips in mid-2017.

As with the present ATLAS detector both Indium and solder bumps are under development. The flip-chip bump bond process is broken into five stages.

- The first is the deposition at wafer level of a solder wettable metal layer (under bump metal UBM) on the pixel pads for both the sensor and read-out chip. To reduce cost, development is taking place to allow the sensor UBM to be deposited by the sensor vendors.

- The second stage is the bump deposition on the wafers. For solder the bumps are electroplated on the read-out chip wafer only. The indium process requires indium bumps to be evaporated onto both the sensor and the read-out wafers.

- Wafers are thinned to the desired thickness, before or after bump formation depending on technology, and diced after bump formation.

- For the front-end chip thickness below 400 μm require vendor specific techniques to handle chip bow during the flip-chip process to prevent disconnected pixels and these may be applied at wafer level depending on technology.
- Finally, the parts are attached via the flip-chip process. The flip-chip process requires the alignment of the two die and the application of heat and pressure to make the bond. For solder a reflow at 230 °C is required, while indium uses temperature from 30 to 100 °C during the flip-chip process.

One of the most significant technical challenges is the handling of thin read-out wafers. The chip bow increases with reducing thickness, increasing die size and increasing temperature. The use of elevated temperatures causes the read-out chip to bow still further, due to the coefficient of thermal expansion (CTE) mismatch between the chip thick front-end metal and dielectric stack and the silicon substrate, resulting in disconnected bumps.

Four different processes have been investigated to enable thin chip flip-chip by the prospective ATLAS flip-chip vendors that show the challenge has been successfully met.

The first is a low temperature flip-chip processing using indium bumps; either free standing or as a cap on a nickel pillar (Selex, RAL and HPK). The chip is held flat on the vacuum tool of the flip-chip machine while the bond is performed at modest elevated temperature. The die is released only after the chip has returned close to room temperature. This process has been shown to work well, but has the disadvantage of reduced flip-chip throughput. To mitigate against this, flip-chip at various laboratories is being investigated using bumps deposited in industry. An example of a high yield bump-bonded thin-chip FE-I4 based quad module is shown in Figure 15.10. The module is made with 150 μm thick FE-I4 read-out chips and a single 150 μm thick quad sensor. The response to a uniform Am-251 gamma illumination is shown. The module shows a lack of any low count regions, which illustrates the high bump-bond yield.

The second process developed at IZM, and successfully used for the IBL, employs a temporary glass carrier wafer bonded to the backside of the thinned read-out chip wafer. The wafer including carrier is diced and the chip-carrier packages are used for flip chip to prevent the chips from bowing during the solder reflow process. The glass carrier are removed from chip backside after the flip-chip process by laser exposure. Again the flip-chip process is the bottle neck of this method and development to increase throughput is taking place.

The third method uses a reducing atmosphere during a solder reflow stage immediately before flip-chip on the flip-chip machine (HPK), where the chip is held flat during reflow and allowed to cool before removing from the machine. The final method uses a dielectric and metal layer deposited on the backside of the read-out chip wafer to balance the bow induced from the front-side stack (CEA Leti/Advacam [133]). This layer is not removed after flip-chip. These two processes have produced a number of high yield assemblies on thin die and are under-going further development. The last two processes aim to produce solder based flip-chip without the use of a carrier wafer to increase throughput.

Table 15.2: Flip-chip bump bond vendor candidates for the ITk pixel system.

Vendor	**Technology**	**Bonding Technology**	**Thin Chip Bonding Demonstrated**	**Thin Chip Handling Option**	**Experience in Particle Physics**
IZM	SnAg solder	Solder reflow at 230 °C	150 μm FE-I4 chip demonstrated	Temporary handling wafer	High built the present ATLAS pixel and IBL
Selex	Indium	Thermal compression 100 °C	100 μm FE-I4 chip demonstrated	Bonding on vacuum jig of flip-chip machine	High built the present ATLAS pixel
HPK	Indium on Nickel pillar	Low temperature thermal compression	150 μm FE-I4 chip demonstrated	Bonding on vacuum jig of flip-chip machine	New to particle physics
HPK	SnAg	Solder reflow on flip-chip machine	150 μm FE-I4 chip demonstrated	Reducing-reflow on flip-chip machine	New to particle physics
CEA LETI and Advacam	SnAg solder on copper pillar	Solder reflow at 230 °C	100 μm FE-I4 chip under development	Developing chip backside process to compensate bow	New to particle physics. Advacam used with ALICE pixels
RTI	SnAg solder	Solder reflow at 230 °C	250 μm FE-I4 chip demonstrated. Thinner under development	Under development	Used for CMS pixels
RAL	Indium	Room temperature compression	Thin chip not demonstrated	Bonding on vacuum jig of flip-chip machine	New to flip-chip bump bonding

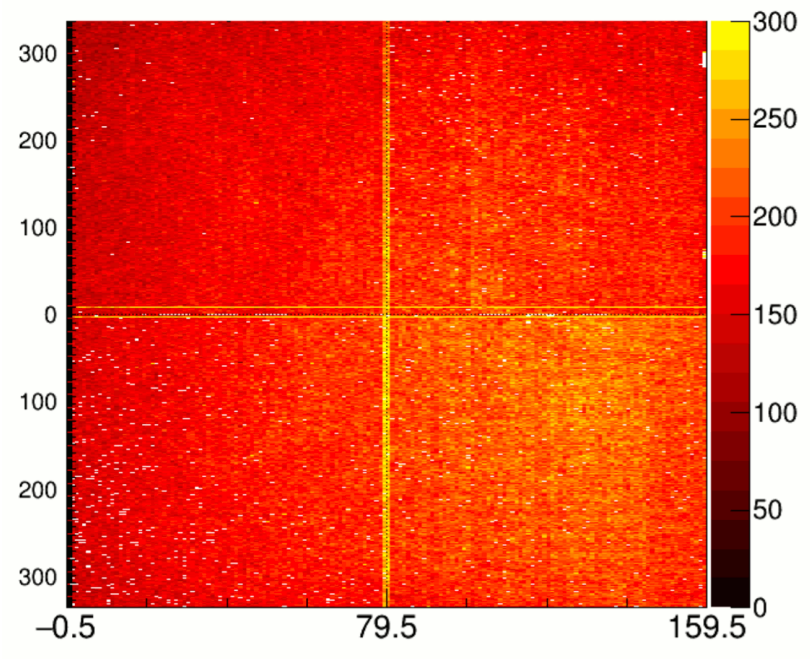


Figure 15.10: The response to ^{241}Am gamma radiation of a thin chip FE-I4 based Quad module produced at HPK (150 μm thick sensor and read-out chip). The plot shows the number of hits recorded per pixel. The high hit pixels are due to their larger size in the inter-chip region.

The ATLAS pixel community is actively working with six suppliers of flip-chip bump bonding technology. The large number of suppliers has been chosen so that the likelihood is increased of solving the challenges imposed for volume production of thin chip assemblies as well as allowing a meaningful choice of supplier at the tender stage. The vendors are given in Table 15.2 with their bump technology, thin chip handling option and their level of maturity in the ATLAS pixel project.

The technology at the various vendors is at different levels of development. The FE-I4 chip has been used to develop the technology to date. There are many more 200 mm diameter FE-I4 wafers available to enable further process development over the coming year to allow all the identified vendors to fully demonstrate thin module processing. In addition, a bump bond test wafer processed on a 300 mm diameter wafer in being produced. This will allow the vendors to demonstrate the process with the final wafer diameter, bump density and die size. The RD53-A chip will be available in the middle of 2017 by which time the vendors will be ready to produce pixel assemblies based on the new generation front-end chip prototype. Some vendors will require the RD53 wafers for further optimisation of thin chip processing in the second half of 2017 and early 2018. Thanks to this qualification process, no significant flip-chip bump bonding development is expected to be needed for the final ATLAS front-end chip.

The HL-LHC pixel system will have of the order of 10,000 pixel assemblies mainly consisting of 4-chip modules. This represents an increase of over five times the number of modules and approximately three times the number of front-end chips compared to the present ATLAS pixel system. The start date for module production is driven by the front-end chip development, while the completion date is dictated by the HL-LHC turn on date.These constrains limit the total module production duration to at most 30 months. The rate limiting steps for module production is flip-chip bump bonding and pixel module characterisation. The bump deposition will have to be completed approximately six months before module production is finished to allow time for flip-chip and module characterisation. The 300 mm diameter wafers, produced at a high throughput fab, are estimated to produce 88 good chips per wafer. The use of larger wafers reduces the pressure on the bump deposition facility (reducing wafer count by 2.4 times compared with that required with 200 mm wafers) but reduces the number of facilities that can handle the larger wafers. Therefore, approximately 500 wafers will be required to be processed with bumps in 24 months, or an average of 20 wafers per month. A typical wafer lot is twenty wafers and takes about three months from start to finish to process. If three vendors with equal capacity are chosen they will process eight wafer lots each over two years, which is very manageable for all the vendors under investigation. The rate limiting flip-chip step may require more than three vendors. Various laboratories (e.g. RAL and Barcelona) are able to supplement commercial flip-chip vendors and this option is being investigated to guarantee supply.

A test of such a sustained high production rate is not possible during the R&D phase of the project. Several small production runs have been launched with 400 μm thick FE-I4 wafer to give some evidence of a robust bump deposition process and fast flip-chip production. Lessons have been learnt from these runs and processes have been made more reliable. Further larger runs will continue throughout 2016 with the FE-I4 wafers and 300 mm diameter bump bond test wafers at several vendors.

15.1.6 Module Assembly and Prototyping

An example of a first prototype quad-module with the FE-I4B chip is shown in Figure 15.11. Several flex PCB circuits have been developed for quad pixel modules exploiting the experience with the two chip IBL flex. The quad module flex is designed for serial powering and AC coupled communication. The flex has a single clock and command bus for the four chips but individual data outputs per chip. Presently it is assumed that the data links from the four chips of one module will be multiplexed together and transmitted electrically to PP1 (Section 15.6). The concept of multiplexed data from the four FE-I4 chips has been demonstrated with a module hosting a commercial CMOS multiplexing chip. The final data multiplexing chip will be designed using IP blocks from the RD53 collaboration and mounted on the module flex or directly integrated in the ROIC. The flex also supports a PSPP chip (Section 15.4) to enable the DCS functionality including module power bypassing required in the case of module failure. A redesign of the quad flex to adapt it to the

particular geometry of the barrel I-beam design is underway.

The FE-I4 chip serial data LVDS output runs at 160 Mb/s while the new ATLAS chip will have fast serial output with a maximum speed of 5 Gb/s. While the output data rate per chip for all but the inner layer will be less than the maximum, data multiplexing of chip data results in Gb/s data links on all modules. The next designs of the module flex will be produced in the coming year to handle these fast data rates. They will initially be tested in a similar fashion employed for the data links (see Section 15.6) before being used to make RD53-A chip based modules at the end of 2017. Many modules will be made to allow module construction and testing techniques to be developed ahead of the Pixel TDR as well as to produce a stock of modules for system tests.

The flex PCB will be produced in industry and the vendor will be responsible for guaranteeing the quality of the product, including cleanliness. The development of flex to pixel assembly techniques is starting. Presently several techniques are under investigation at different laboratories and these will be reviewed and qualified in due course. The rate limiting step for module production is module characterisation.

The module testing process will be based on that used for the IBL and is presently under review. It will include a HALT and HASS programme for quality assurance as well as standard tests for quality control. The development of the characterisation process is based on the FE-I4 modules being produced for the bump bonding development. During the next six months more than 100 modules will be made and used to develop the module characterisation process. Parallel test facilities will be used to allow batch testing of modules such that the production schedule will be met. DAQ developments allow for the testing of many FE-I4 chips in parallel at reasonable cost. Present DAQ systems include inexpensive FPGA cards, connected to a PC via USB3, (e.g USBpix3) capable of characterising a quad module and more advanced DAQ cards such as HSIO-II capable of characterising 18 front-ends (equal to 4.5 quad modules) in parallel or PCIe-based cards used for parallel communication to several front-ends.

15.1.7 CMOS Pixel Detectors

Recent developments of CMOS pixel detectors, originally designed for charge collection in an epitaxial layer (10-20 μm thick) [134–136], use new approaches to cope with the rate and radiation environment expected at the HL-LHC [137–141] based on the following enabling technology features:

- HV add-ons that allow to use high depletion voltages (HV-MAPS).
- High resistivity wafers for large depletion depths (HR-MAPS).
- Radiation hard processed with multiple nested wells to allow CMOS electronics embedded with sufficient shielding into the sensor substrate.

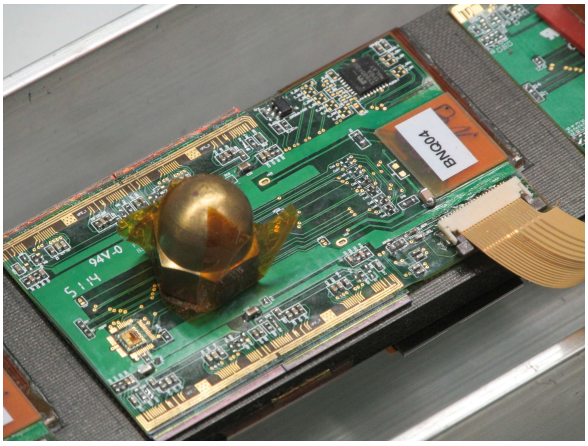


Figure 15.11: Prototype of the quad-module with four FE-I4 chips.

- Backside processing and thinning for material minimisation and backside voltage application.

A typical CMOS sensor pixel cell with sensing substrate and a CMOS electronics layer embedded in multiple cells is shown in Figure 15.12.

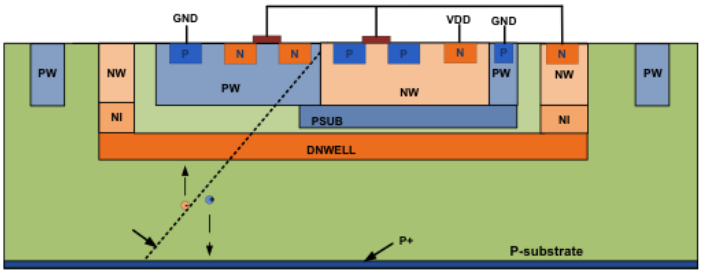


Figure 15.12: DMAPS schematic showing fully or partially depleted bulk, multiple nested wells for CMOS electronics and charge collection node.

R&D within ATLAS started about 2010 with an ATLAS Demonstrator programme (sensor design and characterisations) being pursued since 2014. The first goal of this programme was to demonstrate that depleted (monolithic) CMOS pixels (DMAPS) are suited for high rate and high radiation operation at LHC. For this a number of technologies have been explored and characterised: AMS 350 nm and 180 nm, Global Foundry 130 nm, ESPROS 150 nm, LFoundry 130nm, TowerJazz 180nm, Toshiba 130 nm, XFAB 130 nm (SOI), ST-M 160 nm. The designs have been characterised as stand-alone sensors as well as bonded to the FE-I4 pixel chip (as a 'hybrid') either via bump bonds or via glue bonding (capacitively coupled pixel detector, CCPD).

The results within the demonstrator programme can be summarised as follows:

- Technologies complying with the above list of enabling technology are principally suited to fabricate depleted monolithic sensors that can cope with the HL-LHC running condition, at least at distances larger than 20-25 cm away from the interaction point (outer layers).

- DMAPS pixel sensors detect mips with integrated efficiencies[4)] above 98% and with spatial resolutions similar to those as hybrid pixels ($50 \times 100 - 200$ μm^2, possibly 50×50 μm^2).

- DMAPS pixel sensors can stand radiation fluences of more than 10^{15} n_{eq}/cm^2 when properly designed. This is demonstrated in Figure 15.13 showing the collection width obtained after irradiation to a neutron fluence of 5×10^{15} n_{eq}/cm^2 determined using edge TCT measurements.

- Test beam measurements have shown high rate capability as detectors bonded to the FE-I4.

- Fully monolithic DMAPS pixel sensors have been designed incorporating read-out architectures suitable to cope with the expected rates at the HL-LHC (such as column-drain architectures and direct hit transfer architectures). Such designs have been submitted for fabrication in 2016 and are currently being evaluated.

15.2 Local Supports

15.2.1 Introduction

The design of the mechanics is deeply related to the detector layout. In general, the active elements should first be distributed in the detector volume, the mechanical structures can then be developed around them. The layout is the input to the mechanical design.

However, as explained previously and in Section 3.2.2 the layout has not been finalised and two options are being evaluated for the barrel section. Different mechanic concepts have been developed so far providing solutions for both layouts. Prototypes have been produced and they are under test to verify their performances against the relevant requirements.

It is therefore mandatory to specify the requirements for the local supports and in particular those which are relevant for the current phase of the development process. The complete description of the Pixel local support specifications are described in the following.

[4] In-time effects were not considered and may have an impact on the number given.

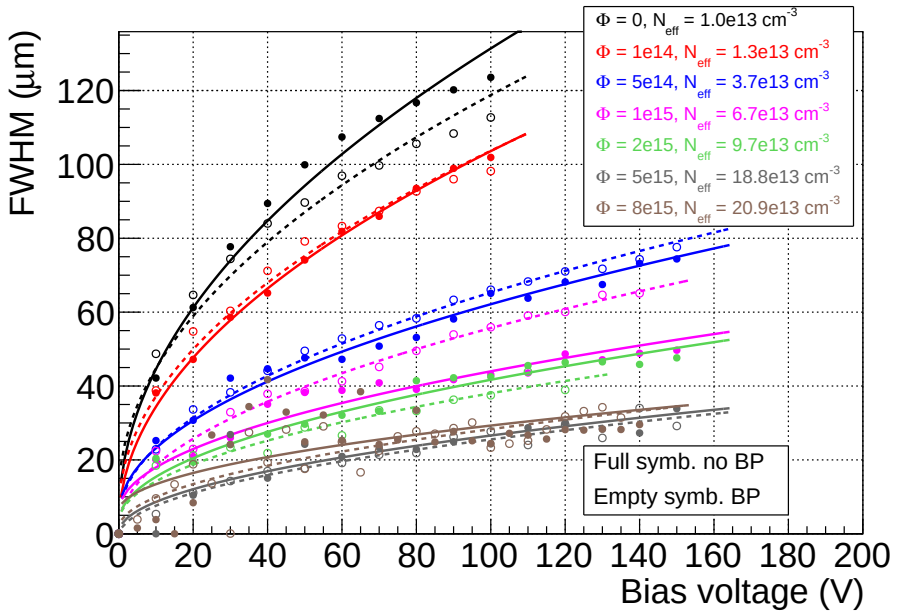


Figure 15.13: CMOS Pixel sensor (LFoundry) after irradiation to fluences of up tp 8×10^{15} n_{eq}/cm^2 demonstrating that collection widths (measured as full width at half maximum, FWHM) in the order of several 10 μm can still be achieved after high fluence irradiation. Full symbols show results from a device without back plane metallisation (no BP) in which case the substrate bias was applied from top, open symbols show results from a device with back plane metallisation (BP) used for biasing.

15.2.2 Requirements and Specifications

Requirements are a set of functions that a design must guarantee. The specifications define the metric and the performance values that are needed to meet the requirements. They are numerical values that the qualification process evaluates on prototypes or via calculations. Stability and thermal performance are the most relevant requirements in the current state of the detector development.

Thermal Performance Specification:

The thermal performance requirement ensures that the modules will not suffer the so called thermal run-away at the end of the detector life. The metric for the requirements is given by the parameter Thermal Figure of Merit (TFM) and it is typical of any local support design.

TFM is defined as the ratio of the temperature difference (ΔT) between the evaporation fluid and the hottest spot on the sensor to the module power per unit of area Φ_{mod}.

The unit is °C cm^2W^{-1} and it can be considered as the thermal impedance of the structure cross-section. A low TFM corresponds to low temperature on the sensor. The total TFM

(Γ_{TOT}) is made from several contributions: the Heat Transfer Coefficient (HTC) in the pipe, the interfaces in the local support cross-section and the heat conduction in the materials. The total TFM can be split into two contributions: the convective part (Γ_{HTC}) since it is related to the HTC of the boiling CO_2 and the conductive part (Γ_K) that depends on the thermal conductivity coefficient of the materials and interfaces in the local support structure.

$$\Gamma_{TOT} = \Gamma_{HTC} + \Gamma_K \tag{15.1}$$

Γ_{TOT} can be measured experimentally on prototypes imposing a heat flux generated by silicon heaters and a boiling CO_2 flow in the cooling pipe. The temperature on the sensor is given by:

$$T_{sensor} = \Gamma_{TOT} \cdot \Phi_{mod} + T_{evap} \tag{15.2}$$

Where Φ_{mod} is the heat flux from the module (Wcm^{-2}). The heat flux from the module Φ_{mod} is the sum of two contributions: the front-end chip (FE), and the sensor power dissipation caused by its leakage current.

While the first contribution is constant and depends on the hit rate only, the sensor power depends on the radiation dose. The dependency is exponential and since the ΔT increase is, in first approximation, linear with the power, this may trigger a thermal runaway as the radiation dose increases.

Assuming a design evaporation temperature T_{evap}, Γ_{TOT} can be set as a specification for the local support such that, at the end of the detector life, there will still be a margin against the thermal runaway. The required Γ_{TOT} depends on assumptions on several detector operational parameters and on the safety factors used in the calculations to estimate some unknown parameters. Some of the assumptions and the most relevant safety factors are listed in Table 15.3:

- Max Pixel Current: the maximum single pixel current the front-end chip can handle. Depending on the sensor technology this current can be a limiting factor even though the runaway limit is not reached.
- σ_{TFM} and TFM acceptance range: There will be variation of the TFM value both along the length of the local support and between local supports. The standard deviation of the TFM distribution is estimated to be 16.7%. The acceptance criteria is set to $3\sigma_{TFM}$, meaning that a variation of 50% of the specified TFM value is accepted.

The TFM is determined using an analytical approach solved via perturbative techniques. The calculation is done separately for each barrel layer given that the radiation fluence depends on the layer radius as shown in Table 3.6. Moreover, the requirements depend also on the type of sensors. The planar sensors dissipate more power than the 3D sensors

Table 15.3: Parameters and Safety factors of the Pixel Detector.

Parameters and Safety Factors	**Nominal**	**SF / Margin**	**Design**
Sensors			
Pixel size along z			50 μm
Pixel size along ϕ			50 μm
Max Pixel Current			10 nA
Inner pipe ID			2.4 mm
Evaporation Temperature	-35°C	Margin = 5.0 °C	-30°C
CO_2 Heat Transfer Coefficient	8000 W $K^{-1}m^{-2}$	SF = 1.3	6150 W $K^{-1}m^{-2}$
σ_{TFM}			16.7%
TFM acceptance range			$3\sigma_{\text{TFM}}$

due to the higher depletion voltage, see Sections 15.1.2 and 15.1.3. Figure 15.14 shows the conductive TFM Γ_K as function of layer radius. The values for Γ_k were determined with $\Phi_{3D} = 10$ mW/cm^2 and $\Phi_{\text{planar}} = 92$ mW/cm^2 both at -25°C and 10^{16} n_{eq}/cm^2 and with FE and sensor thickness of 150 μm. The power consumption of each sensor type is scaled to radius according to the full fluence expected for each layer and added to the power from the front-end (see Section 15.1)[5]. The greyed area below 10°C cm^{2}W^{-1} is considered off-limits in the sense that the actual technology does not allow such a low thermal impedance to be reached. Developments are under way to lower the CO_2 operating temperature.

Operational Temperature Range (OTR):

The estimate of the OTR is based on the minimum evaporation temperature on the low side and on the interlock system on the high side. The interlock system will switch off the power on modules if the temperature rises above +40°C. The nominal temperature range can be therefore be set at $-35°\text{C} < T < +40°\text{C}$. However, a safety margin of 20°C has been added to the range specifying the OTR to be $-55°\text{C} < T < +60°\text{C}$.

Humidity Range (RH):

The ITk Pixel Detector will be operated in a dry nitrogen environment at a constant dew-point. However, the temperature variation of a constant dew point gas produces variation of its relative humidity RH. Composite structures react to it with medium long timescale affecting the geometrical stability of the detector. For this reason, the range $0\% < \text{RH} < 80\%$ has been set for the detector volume.

[5] The plot is for illustration only: power consumption and device thickness need to be adjusted to values discussed in Section 15.1 once these were finalised.

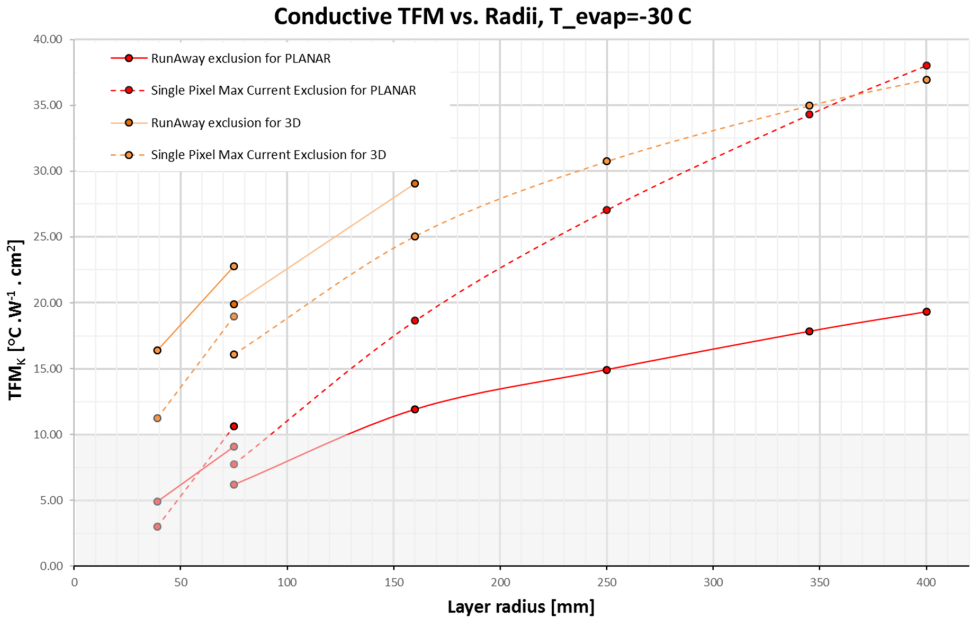


Figure 15.14: Conductive TFM Γ_k obtained from an analytical approach solved via perturbative techniques. The solid lines give the conductive TFM limit required to cope with the thermal runaway in orange for the 3D and red for planar sensors. The dotted lines show the limit for the maximum pixel current with the same colour coding. The jump from layer 0 to layer 1 is caused by the change from double- to quad-chip modules illustrated by the two data points given for layer 1, the upper one showing the result for double- the lower point showing the result for quad-chip modules.

Radiation Hardness:

Radiation deteriorates the mechanics characteristic of the material generally causing embrittlement and stiffness change. The strictest requirement is given by the dose, including a safety factor, expected for the innermost barrel layer as described in Section 3.4.

Material Budget:

The goal is to minimise the total structure mass per layer in terms of radiation length. The target value is, for the structures only with no modules, 0.5% and 0.6% X_0 for the innermost and outermost layers respectively.

Stiffness:

The stiffness requirement is given in terms of maximum gravity sag (Max 100 μm) and/or in terms of minimum resonance frequency. The two parameters are not independent from

each other and they can be applied separately. The specifications assume that the local supports are loaded with modules and services.

Layer Hermiticity:

The hermeticity specification is twofold:

- The first one sets the minimum number of pixel of overlap in the ϕ axis once all the loads described above are applied. The goal is to guarantee at least five pixel overlaps in any operational condition.
- The minimum hermeticity per layer in the $r - z$ plane is set to 98.5% per layer due to the unavoidable longitudinal dead gap between modules sharing the same Local Support.

Maximum Design Pressure (MDP):

The local supports house the cooling pipe in which the CO_2 evaporates to evacuate the heat generated in the services and in the modules. In general, the cooling pipe is embedded in the structure and is subjected to high pressure. The specification on the MDP of the cooling line is driven by the safety release systems that will be implemented in the cooling plant. Those are either release valves or rupture disks. In particular, the CO_2 transfer lines, running from the cooling plant to the detector, will be equipped with rupture disk at 130 bar. Therefore, the pipes in the detector could experience such a pressure and the MDP for the on-detector piping necessarily needs to be set to 130 bar. So far ITk has defined the pressure code to be used for the design. The Pressure Equipment Directive (PED)[6)] defines, among other parameters, the safety factor to be applied for the pressure test qualifying the pressurised sections of the cooling system. According to the code the pressure test must be 1.43xMDP leading to a test pressure of 186 bar.

Geometrical Stability:

One of the most relevant specification refers to the position stability of the modules in the detector volume. Stability requirements are given for two time ranges over which a set of load variations have been defined: Short is a timescale of 1 day, Medium in a timescale of 1 month. The loads variation be considered in order to address the stability requirement over the two time intervals are as follows:

[6] See the European Parliament and the Council Directive 97/23/EC, http://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:01997L0023-20130101&locale=en for details on the PED.

- Short: 10% power dissipation in the front-end chip and in the services; $\pm 1^{\circ}$C evaporation temperature variation.
- Medium: Relative Humidity variation of the detector environmental gas from 10% to 50%; $\pm 3^{\circ}$C evaporation temperature variation.

Given the loads variation above, the specifications for the geometrical stability are listed for both timescales in Table 15.4.

Table 15.4: Specifications of geometrical stability. Values are given by means of absolute maximum stroke in μm on each axis

	Nominal (μm)	**Safety factor**	**Design (μm)**
Short - 1 day stability period			
δR	7	1	7
$\delta \phi$	7	1	7
δZ	14	1	14
Medium - 1 month stability period			
δR	17.4	1	17.4
$\delta \phi$	17.4	1	17.4
δZ	34.8	1	34.8

15.2.3 Qualification Process for the Barrel Local Supports

The final Layout will be selected on the basis of the Physics performance. However the barrel local support candidates will go through a preliminary qualification process in order to ensure that one option will meet the specifications. The qualification process will be carried out on a limited but relevant subset of the requirements. The complete thermal and mechanical qualification will be performed later (by the Pixel TDR, scheduled late in 2017) and it will only apply to the candidates of the selected layout.

Preliminary qualification

- Validation of the nominal TFM: The measurement of the conductive and convective TFM requires dedicated equipment based on a CO_2 evaporative cooling system. The local support is loaded with 300 μm thick silicon heater mimicking the front-end chip and the sensor (both assumed to have 150 μm thickness). At least three silicon heaters are loaded on each structure. The prototype pipe is connected to the CO_2 cooling system and a current is run through the heaters. A number of thermal sensors are

placed on the structure in order to measure the evaporation temperatures in the boiling channel and the ΔT increase profile in a few places up to the hottest point on the silicon heater.

Figure 15.15 shows the measured TFM as a function of the heat flux. The black curve gives the TFM as measured close to the pipe inlet, the purple curve gives the TFM as measured close the pipe outlet. The other curves refer to other thermal sensors placed in intermediate positions. The TFM decreases with increasing heat flux from the silicon heater due to reduced influence of convection. The asymptotic value is therefore to be compared to the specifications listed in Table 15.5. Those specification were derived as for Figure 15.14 from the given evaporative temperature, the pipe size, the HTC and the heat flux, to cope with the thermal runaway and the max pixel current.

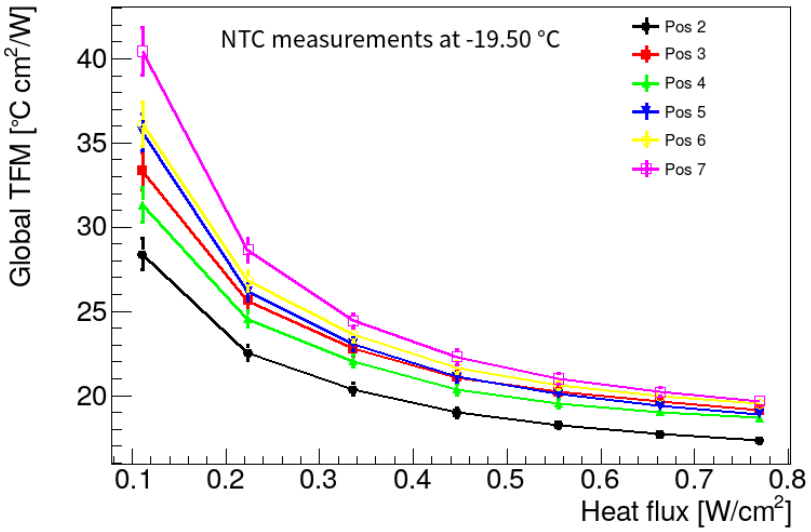


Figure 15.15: TFM as a function of the heat flux. The black curve gives the TFM as measured close to the pipe inlet, the purple curve gives the TFM as measured close the pipe outlet. The other curves refer to other thermal sensors placed in intermediate positions.

- Consistency of the estimated TFM production performance: It is difficult to qualify a design against such a specification. It requires a large number of samples produced with the final assembly procedure. For the preliminary qualification process only, the statistical distribution of the production performance on the TFM is verified over three samples.

- Robustness test: The robustness test applies to the effect of the pressure and thermal cycling on the TFM. Once the nominal TFM has been measured, the sample undergoes 100 pressure cycles (from 0 to MDP=130 bar) and 100 thermal cycles covering the

Table 15.5: Specifications for the Thermal Figures of Merit Γ in °C cm^{2}W^{-1}.

Barrel Layer	Γ_K	Γ_{HTC}	Γ_{TOT}
0 (3D)	11.22	4.31	15.53
0 (Planar)	2.99	4.31	7.30
1 (3D)	16.08	8.62	24.70
1 (Planar)	6.20	8.62	14.82
2 (Planar)	11.91	8.62	20.53
3 (Planar)	14.92	8.62	23.54
4 (Planar)	17.83	8.62	26.45

whole OTR (Operational Thermal Range from -55 to +60°C). TFM is measured again and it should not show any appreciable degradation.

- Mechanics performance test: The preliminary qualification of the mechanic performance is estimated via FEA (Finite Elements Analysis). However, the FEA needs to be validated by experimental tests on prototypes. These specifications define the maximum gravity sag (or minimum resonance frequency) of the local support design. The stability requirement is set over a period of one day by means of displacement caused by a defined load case that takes into account the expected maximum variation of the environmental loads like power and evaporation temperature.

Final Qualification

The full qualification of the local support will take place only after the layout is chosen. The qualification process will therefore only apply to the relevant designs. The details of the qualification are still under development mainly for what concerns the population of the sample to test for qualifying the design against the specifications. A short description of the main aspects of the qualification is given below:

- Radiation effects: The TFM will be measured on samples irradiated to doses expected in Layer 0 as described in Section 3.4 in order to exclude degradation of the thermal compounds. Radiation could degrade the thermal coupling at the interfaces.
- TFM production performance: It is essential to verify the variation of the TFM measured on a preproduction samples at different module locations and from different assembly sites. The qualification will be carried out once the final design is selected on a significant number of assemblies in order to verify the production performance estimate which is equal to 1.5 times the design value.
- Ageing effects: Ageing tests will be performed through temperature, humidity and pressure cycles. A number of pre-production samples will be cycled over the OTR

(operational temperature range), the MDP (max. design pressure) and humidity variation 100 times. The design number of cycles is defined to be less than ten per year over the detector lifetime of ten years.

- Mechanical and stability performance The local support design must be qualified against the gravity sag (or minimum resonance frequency) on a final prototype. The stability performance within a one day and a one month period must also be verified on a final prototype. The verification of the overlap in ϕ between local supports is of great importance. However this measurement can only be done once the detector is taking data. Therefore the qualification is performed simulating the displacement of the modules in a layer using as input the measured displacement of the local support under the thermal, pressure and humidity cycle.

15.3 Design of the Local Supports

Several different design options of the barrel local supports are under development. For the end-caps, a single design is under study. The design is optimised to reduce the material budget in each layer. This is achieved by using low density and low Z material for high thermal performance. The required stiffness is achieved with the use of ultra-high modulus fibres. Cooling lines are embedded in the local support to bring the biphasic CO_2, operated at low temperature, close to the heat producers (sensor and front-end electronic). Most designs use titanium tubes with a diameter of a few millimetres and a wall thickness of few hundreds of μm.

15.3.1 Barrel Candidates for the Extented Layout

In the extended layout all the sensors are positioned on cylindrical surfaces and are parallel to the beam axis, see Figure 3.5(left). Two designs are under development: I-Beam and Carbon Stave.

I-Beam

This design achieves the low-mass requisite by coupling two layers in a single discrete structure with an I-Beam-like cross-section. Modules are placed on both flanges of the I-Beam, see Figure 15.16.

The heat generated by the modules is collected by the flange whose core is low-mass thermal conductive carbon-foam. The heat reaches a titanium pipe directly bonded to the carbon-foam in which the boiling CO_2 removes the heat at low temperature. The laminates of the entire structure are bonded together by means of a process called co-curing. This process does not require extra adhesive to bond the parts together. It is the matrix of the

plies itself that provides it. The uncured layups are wrapped in a mould and they are cured in one pass. The resin of the pre-preg provides the adhesive.

The first thermal test conducted on a non-optimised design showed good TFM values almost meeting the specs listed in Table 15.5 for the most demanding innermost layer. Recent estimate of the radiation length shows values around 1.62% X_0 for the sum of the two layers. Considering the two innermost layers, approximately 1/3 of this is contributed by layer 0 with 2/3 being contributed by layer 1.

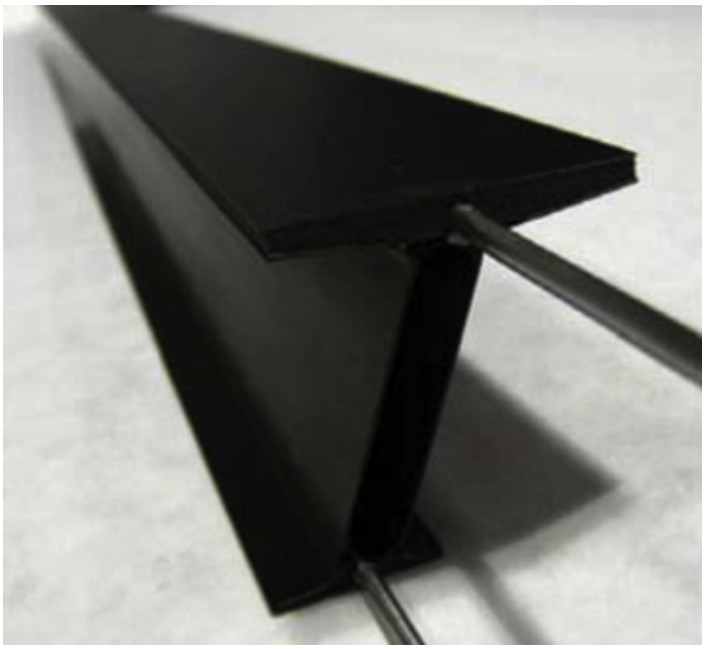


Figure 15.16: I-Beam stave. Modules are loaded on both sides (top and bottom).

Carbon Stave

Although the wall thickness of the pipe is slightly larger than 100 μm, the titanium density is significantly higher than for the carbon. The contribution to the radiation length from the titanium pipe is not negligible. As a consequence, the replacement of titanium with another material has recently been considered. Aluminium has been used in past detectors but it is sensitive to galvanic corrosion and it tends to be the sacrificial anode of the galvanic pair Al-C. Severe events of galvanic corrosion have been experienced on Aluminium pipes in carbon structures that led, in the past, to loss of the integrity of several cooling lines. Moreover, a metal pipe in a quasi-zero CTE carbon structure might lead to undesired deformation during cool down or transient conduction. From this point of view, a pipe made of carbon-fibre is the best option in terms of mass and CTE matching.

The carbon stave is an attempt to implement the concept. The metal pipe is replaced by a carbon pipe braided dry on a mandrel and passed through an impregnating dye. Several carbon pipes have been produced already. They have been proven to stand the testing pressure and fulfil the tightness requirement. However, a full carbon stave has not been tested for TFM yet. The thermal performance could be extremely good since the lightness of the carbon pipe allows the usage of several pipes in the same structure without increasing its radiation length.

FEA calculations show a surprisingly good value of TFM with a lot of room to reduce considerably the mass but simulations need to be validated by measurements.

Figure 15.17 shows a photo of a carbon stave prototype.



Figure 15.17: Carbon stave prototype. The carbon pipe (in front) has been impregnated with a diamond-loaded resin in order to increase significantly the through-thickness thermal coefficient that, for the laminate, it is dominated by the resin.

15.3.2 Barrel Candidates for the Inclined Layout

In the inclined layout concept, the pixel sensors are tilted in the longitudinal plane in order to align them orthogonally to the particle trajectory, see Figure 3.5(right). One of the main advantages is the reduction of the pixel surface to be fully hermetic. The main consequence

of a reduction of the number of required pixel modules is a reduction of the amount of associated services, and therefore less associated material in the detector, as well as a decrease of the costs of the detector.

In order to simplify the design and production of the local support which positions the sensors, it was decided to fix the tilt angle. Since the module orientation is no more parallel to the cooling lines, it has been necessary to demonstrate the capability to cool down efficiently the modules without introducing too much material. Two local support designs have been developed: SLIM and ALPINE of which large size prototypes have been produced and tested. The two teams are now aiming at a single design combining the advantages of both approaches.

SLIM

This design groups four rows of modules supported on a longeron-like structure. Within $|\eta| < 1.2$ quad chips modules are arranged flat. For $|\eta| > 1.2$ modules are two chips size and inclined around ϕ forming an angle between the sensor plane and the z-axis. Four titanium pipes run along the longeron corners each one cooling one row of modules (see Figure 15.18).

A recent development foresees the replacement of the longeron laminate with a filament winding truss structure significantly lighter but with an equivalent stiffness. Prototypes of SLIM have been deployed and thermal testing is ongoing in order to measure the TFM.

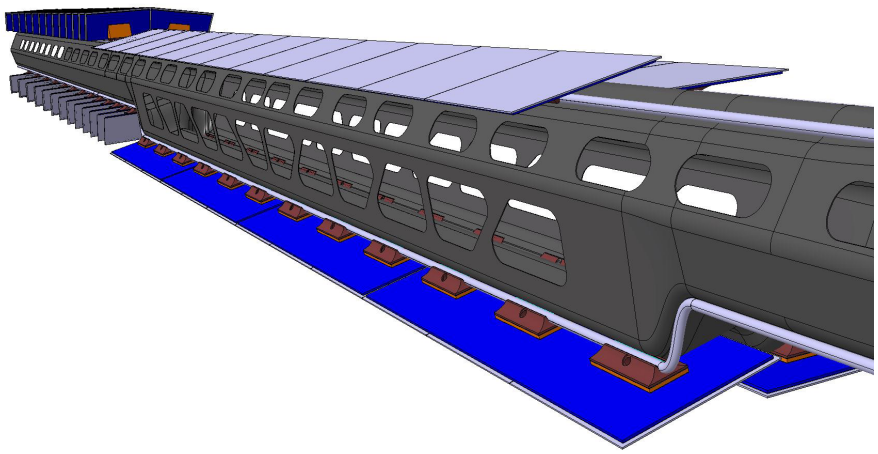


Figure 15.18: SLIM design for the inclined layout.

ALPINE

The ALPINE local support structure is an extension of the IBL approach with inclined sensors. The general shape of a stave is defined by the carbon-foam (typical density of 0.6 mg cm^{-3}). In the inclined sensor area ($|\eta| > 1$), a mountain-shaped wedge of foam, as large as the sensor itself, defines the sensor position. In addition to the geometry definition, the carbon-foam transfers the heat from the sensor modules to the cooling tubes. In order to better spread the heat load, both sides of mountains are covered by a thin sheet of graphite (approx. 100 μm). The flat part of the staves is covered by a carbon-fibre skirt to reinforce their mechanical properties (stiffness, handling). Two titanium tubes are embedded along the stave. These three components are assembled together with glue. A full size prototype (1.2 m long) produced in 2014 is shown in Figure 15.19. Measurements have demonstrated that this first prototype fitted within the design tolerances of the stave. In agreement with thermal simulation, first measured thermal performances for the mountains fit with the ATLAS measurements.

The sensor modules are located on the stave face closer to the interaction point so that incoming particles are detected by a pixel sensor before crossing the inactive material (local support structure, cooling tubes and electrical services). This is critical for the two first layers which mainly contribute to vertex reconstruction. The radiation length estimated for this layout is 0.5% X_0 per stave.

To reach sufficient rigidity (vibration frequency and gravitational sagging), the staves from the same and nearby layers are assembled together through carbon-fibre flanges. The stave and flange geometries have been designed so that a single stave can be dismounted without moving the other staves. The inner/outer flanges holding the (two inner)/(three outer) layers are attached to the IST / PST.

The electrical services run along the stave in the face opposite to the mountains. Module flex linking the sensor module to the electrical service collector along the same have been designed to show a first approach.

15.3.3 Local Support Design for the End-Cap

The end-cap local support is developed through a novel approach. Usually the forward region is covered by disk-like structures on which the sensors are arranged in petals. This solution is somehow rigid to any layout change. If the radius or the z position of a disk needs to be modified, the petal geometry as well as the module size are impacted. In fact, both inner and outer radial coverage can only be matched discreetly by adding or removing one or more active elements.

This sets undesired constraints on the layout definition that benefits from flexibility in its attempt to maximise the physics performance. A ring is an elegant solution to this problem. Instead of a disk stack arranged along Z, modules are placed over a narrow round stave.

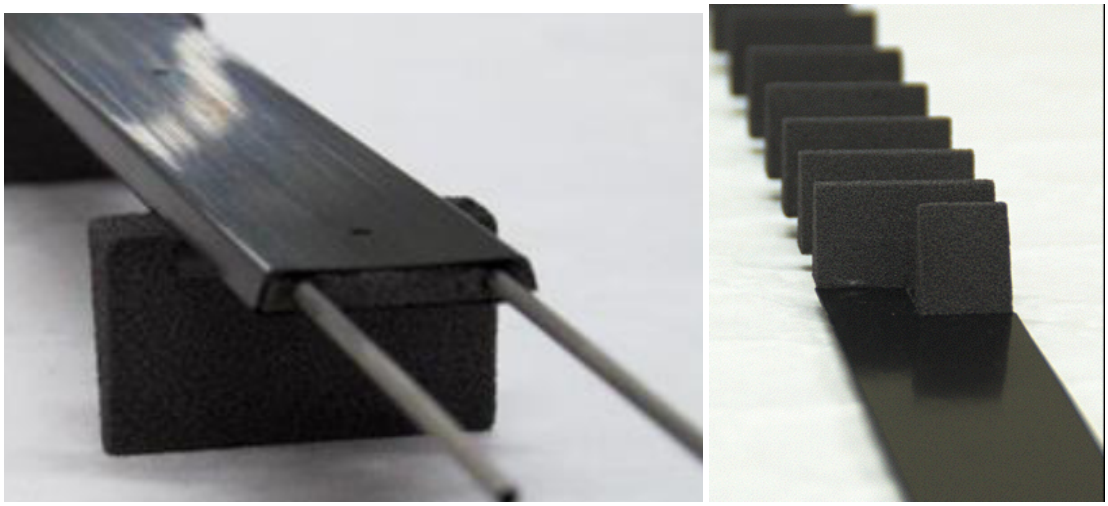


Figure 15.19: ALPINE design for the inclined layout.

Four layers of half-cylindrical shells support the modules providing coverage up to $\eta = 4$. Each ring in a shell can be placed independently from the sensors z position loaded in the other shells.

Figure 15.20 shows the ring concept. Rings in different shells line up to provide a tight disk like coverage.

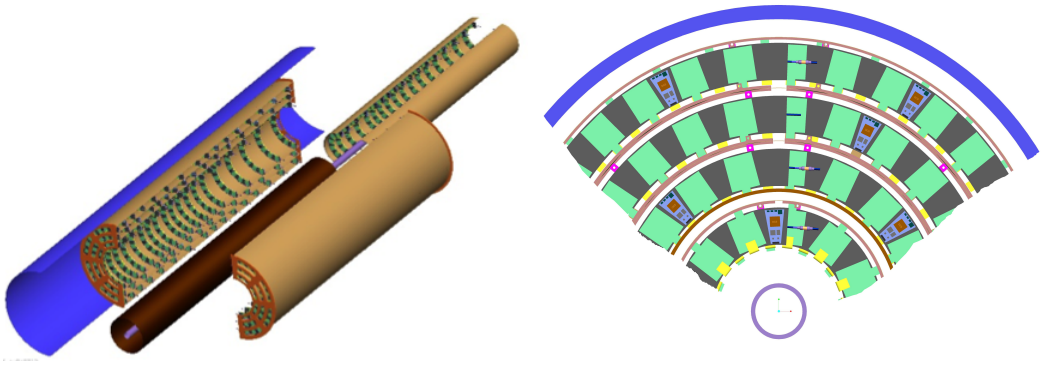


Figure 15.20: **Left**: Ring concept. The composite half-cylindrical shells supporting the half rings carrying the modules are shown in light brown. **Right**: layers lining up to provide coverage.

The half-ring is a sandwich of carbon laminates where the core is carbon-foam. In its neutral plane a titanium cooling pipe and the service bus tape are placed. The heat generated by the modules is taken away by the CO_2 boiling system. The bus tape distributes the electrical services to the modules and are alternatively bonded to the two carbon face-plates allowing the adequate sensor overlap.

Figure 15.21 shows an exploded view of the assembly which is symmetric in its cross-

section to manage the CTE mismatch between different materials. Several prototypes have been already built but design optimisation is still ongoing. Particular attention is placed to reduce the mass of the Rings system in order to minimise the particle background reaching the forward calorimeter and improve tracking performance at high η. To address this issue, it has been foreseen to implement in the assembly procedure (co-curing). Similar to what was successfully tested on the I-Beam, the sandwich skins are bonded to the foam without adding extra adhesive.

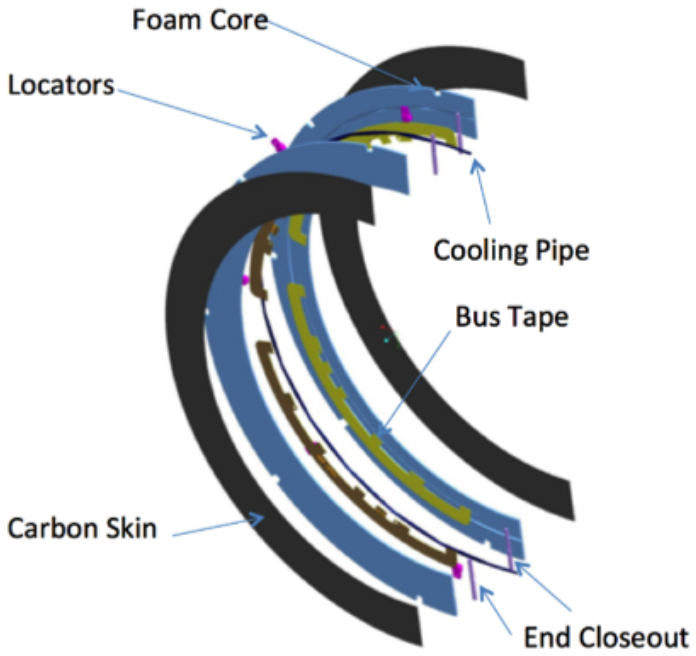


Figure 15.21: Exploded view of the ring mechanical assembly.

Type-I End-cap Services

The Type-I cooling and electrical services for each end-cap-ring layer will be routed along the inside of the half-cylindrical support shell of each layer, exiting the end-cap at the high-z end before joining PP1. Care will be taken to distribute the services as uniformly as possible in ϕ, both to make efficient use of the limited space available and to ensure that services material is not allowed to build up at any given location.

The currently-planned distribution of services is illustrated in Figure 15.22(left). The coolant for a layer of rings will be delivered via a main feed pipe (shown in red) and removed by a main exhaust pipe (shown in blue); smaller-diameter branches lead from these main pipes to each ring as shown in Figure 15.22(right). The main pipes necessarily have a somewhat larger diameter than the pipes leading to the individual rings, but the total material budget

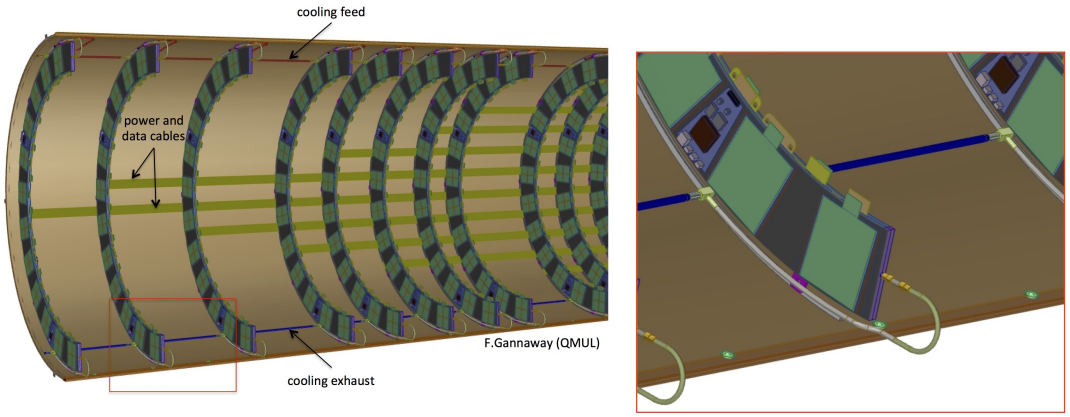


Figure 15.22: End-cap services routing. Left: full view of the routing in a half-shell; right: a detail view of the routing in the inset red box in the left figure.

and occupied space is smaller in this scheme than if each ring's cooling pipe were to run the entire length of the cylinder.

To guard against potential cross-talk between adjacent rings, it may be necessary to keep the electrical services of a half-ring spatially isolated from one another. A way to do this is shown in Figure 15.22; the cables of each half-ring are routed in ϕ, along the edge of the ring, before being bundled together and exiting the end-cap along z. The cable bundle of each half-ring exits at a different ϕ location. If cross-talk between rings is not expected, an overall lower-material solution would be to simply route cables directly to the high-z end of the end-cap, without the ϕ-wise routing along the edge of a half-ring. System tests are planned to determine if the ϕ routing is necessary.

15.3.4 Electrical Services

The cooling services are described in Chapter 19. Electrical services can be grouped under five categories: DATA to bring the data from the modules to the counting room, CLK/CMD to bring the clock and the data to configure and monitor the front-end chips, LV to power the modules, HV to bias the sensors and DCS for detector control system. Table 15.6 shows the current understanding[7)] of the modularity of the services in each layer. Each type of services is detailed in the following.

Data

Data links connect the module to the opto-board that converts the electrical signal into an optical signal. Opto-boards will be located outside the detector volume to reduce the

[7] Subject to detailed design.

Table 15.6: Summary of services modularity of the ITk Pixel Detector layers.

Layer	FE's per Module	Data Modularity		CMD & CLK Modularity		HV Modularity		DCS Modularity		LV Modularity	
		# Links per FE	# Links per Mod.	# Links per FE	# Links per Mod.	# Links per FE	# Links per Mod.	# Links per FE	# Links per Mod.	# Links per FE	# Links per Mod.
Barrel											
0	2	1/1	2	1/2	1	-	1/10	1/20	1/10	1/20	1/10
1	4	1/2	2	1/4	1	-	1/5	1/20	1/5	1/20	1/5
2	4	1/2	2	1/4	1	-	1/6	1/24	1/6	1/24	1/6
3	4	1/4	1	1/4	1	-	1/6	1/24	1/6	1/24	1/6
4	4	1/4	1	1/4	1	-	1/6	1/24	1/6	1/24	1/6
End-cap											
0	4	1/2	2	1/2	1	-	1/5	1/20	1/5	1/20	1/5
1	4	1/4	1	1/4	1	-	1/5	1/20	1/5	1/20	1/5
2	4	1/4	1	1/4	1	-	1/6	1/24	1/6	1/24	1/6
3	4	1/4	1	1/4	1	-	1/5	1/20	1/5	1/20	1/5

radiation level the optical components are exposed to, see Section 15.7.3. This implies long data links of up to 8 m.

The data rate varies with the layer. This is partially taken into account with the modularity. The data links for the innermost layers are still the most demanding in terms of rate specification. Developments are under way to extend the link length while keeping the cable mass as low as possible. The optimisation might require locating the opto-boards inside the detector volume which would mean they would not be accessible. The most promising solution under study is based on a micro-coaxial cable terminated with a short section of twisted pair conductors to reduce even more the cable mass in the proximity of the modules.

Clock and Command

Clock and command lines provide the configuration and timing to the front-end chips. The required data rate is significantly lower than the data links. However, the total number of links is non-negligible and contributes considerably to the overall mass of services.

Low Voltage

Serial powering was adopted to power the front-end chip, mainly due to the large number of modules. Several modules (therefore several front-end chips) are ganged in series and powered with a single line.

High Voltage

High Voltage services provide the bias voltage for the silicon sensor. The maximum depletion voltage depends on the sensor type (3D or Planar) and by the integrated end of life fluence. The maximum high voltage is 1200 V that corresponds to the depletion voltage required by the planar sensors loaded on the innermost Layer. The distribution among sensors is done in parallel and the modularity ranges from 10 to 5.

Detector Control System

The goal of the DCS system is to ensure conditions for stable data taking and to ensure the safety of the detector at all times. The main task of the pixel DCS system is to monitor the module functionality and to provide automatic actions in the case of risk to the detector integrity as described in Section 15.5. DCS links carry the temperature information of the modules previously digitised. If one module fails, the DCS needs to automatically bypass the affected module, see Section 15.4. The continuity of the low voltage serial line can be reestablished and the other modules on the same chain can remain powered. This is one of the most important functions of the DCS system.

15.4 Powering

The ITk Pixel Detector will have around 10,000 detector modules (depending on the final layout decision), which hold either two or four front-end chips. These modules need to be powered with low and high voltage. Furthermore, the finer granularity of the ITk Pixel Detector sensors and its connected front-end chips together with smaller feature size technology of the electronics (65 nm instead of 130 resp. 250 nm) lead to an increased current consumption inside the front-end electronics. Therefore, supplying each of the modules separately with parallel powering with a high power loss within the cables is not feasible and would introduce a tremendous amount of material with the cables to be installed. In order to save material and reduce the voltage drop on the supply services alternative power concepts are under study. Out of the two possible solutions (DC-DC conversion and serial powering) the chosen baseline for the ITk Pixel Detector is serial powering.

The concept of this powering scheme is to power the modules via a constant current and the current to voltage conversion is done on module or chip using shunt regulators. This way, the current being transported via the supply line is just the current for one module, while the voltage is the sum of the voltages needed by all modules: For a serial powering chain with n modules, the current is $I_{chain} = I_{mod}$ and $V_{chain} = n \cdot V_{mod}$.

The serial powering scheme foreseen for the ITk Pixel Detector builds the chain from the individual modules being mounted on the same support structure. This leads to different

ground levels at each of the modules, which needs to be reflected by adding DCS-chips, supplying the high voltage to the modules and using AC coupled data transmission. The voltages for the individual front-end chips of the modules is distributed parallel and each front-end chip has its own shunt regulators to generate the needed voltages.

The foreseen regulator, a shunt low-dropout (shunt-LDO) regulator, is based on the experience gained with the FE-I4 ASIC, which has been installed in the IBL and provided a shunt-LDO already. The voltage regulation loop (LDO) delivers a constant voltage defined by an internal generated reference voltage (i.e. $V_{out} = 2V_{ref}$) and the current regulation loop keeps the current through the regulator constant, while the input characteristic is ohmic, see Figure 15.23.

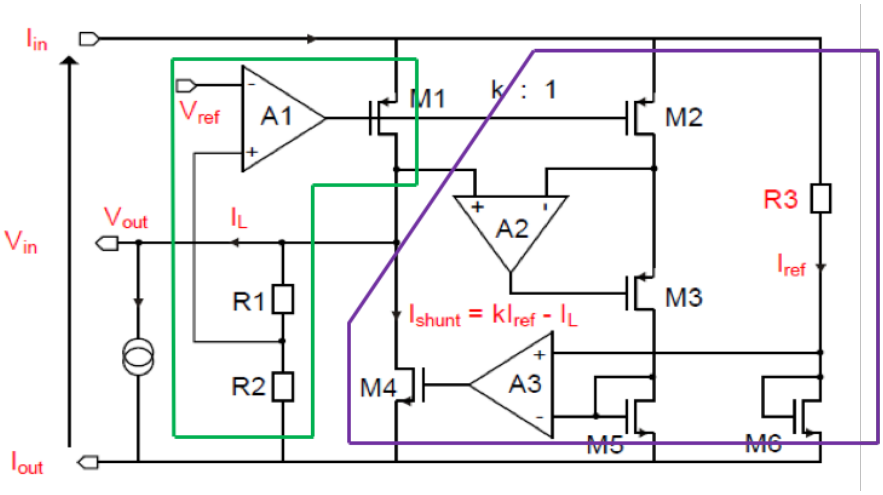


Figure 15.23: Schematic of a shunt LDO regulator. The input characteristic is ohmic: $R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R_3}{k}$

The main features of this regulator are:

- robust design against process variation and mismatch for safe parallel operation (i.e. sharing I_{in} and I_{out} connection, but not V_{out}).
- Parallel operation of regulators with different output voltages possible.
- Ability to shunt extra current if one of the regulators in parallel fails.
- Different working modes for current and voltage based power distribution.
- Shunt current for stable operation can be just 10 mA.

First prototypes of serial powering chains have been set up and the module performance is very promising and not disturbed by the different powering approach. Nevertheless, more studies are needed and several topics need to be addressed such as: module bypass in the case of failures (incl. switching individual module on and off), keeping the power consumption as constant as possible and always well under the limit of the provided current,

HV powering scheme (HV level depending on the sensor type), AC-coupled data transmission (as each module has a different ground potential), and constant current power supply.

To ensure reliability of the entire serial powering chain, control must act on the module level. The main component of the control path is a Pixel DCS chip (Pixel Serial Powering and Protection, PSPP) which provides monitoring and control capabilities on module level. Figure 15.24 shows how the Pixel DCS chip is integrated within the serial power chain.

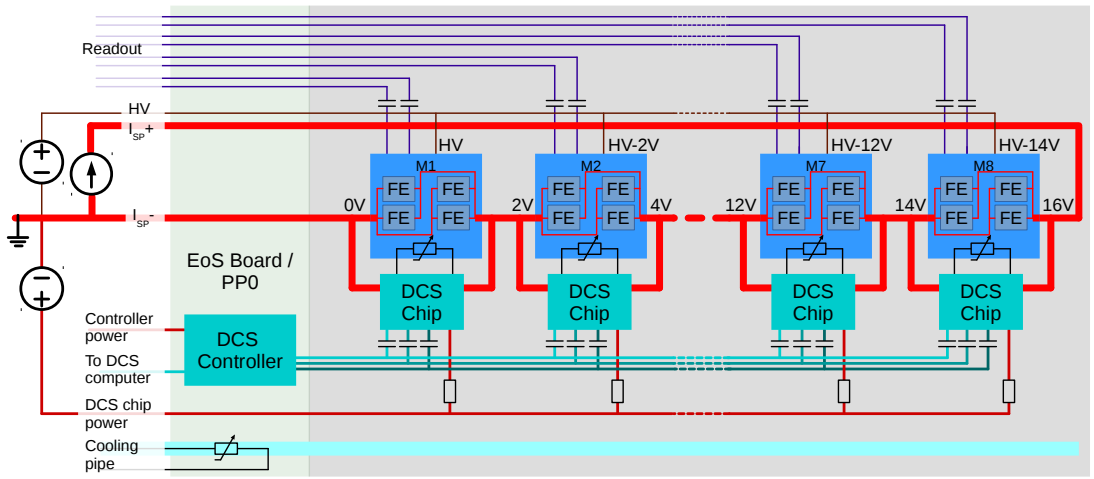


Figure 15.24: Schematic of the Serial Powering distribution on the local support.

The Pixel DCS chip is specially designed to work in a serial power chain and powered separately from the serial powering scheme. It is placed near or on the module flex of each pixel module and designed as a chip independent of the front-end for reliability reasons. It includes bypass capability for the modules, realised by a shunt transistor. The bypass can be activated or deactivated by command. Furthermore a hardwired automatic activation of the bypass transistor in the case of over-voltage or over-temperature is included. The thresholds for the automatic activation are defined with external components on the flex print. This bypass is off after power-up or in the case of power-loss. For feedback the Pixel DCS chip includes an ADC, which allows for monitoring of the module temperature and voltage. As the Pixel DCS chip is mounted in close vicinity to the detector modules, even in the innermost layer, it needs to fulfil the same radiation hardness as the front-end chips of the innermost pixel layer. The Pixel DCS chips are powered independently from the front-end chips. The Pixel DCS chips of one serial input current (I_{sp}) chain share the same power line (see Figure 15.24). The power return of the Pixel DCS chips is merged with the serial supply current I_{sp}. The DCS power line is also used as an external reference for detecting drifts of the internal reference.

There are three independent communication lines to the Pixel DCS chips of one I_{sp} chain. The Pixel DCS chips are AC coupled to the communication lines. Currently there are up to

eight modules in one I_{sp} chain foreseen. The maximal length of the communication lines between Pixel DCS chip and DCS controller is foreseen to be 1.5 m. The DCS controller realises the communication between the DCS computer and the Pixel DCS chip. It serves as a bridge between a long range communication from the computer to the short range communication used by the Pixel DCS chip. The location is not yet fixed, but will either be on the End of Stave board, or a patch-panel.

15.5 Detector Control System and Interlocks

The overall concept of the ITk Pixel Detector control system foresees three independent paths for safety, control and feedback, and diagnostics. These paths differ in granularity, availability, and reliability. Each has its own signal paths. The safety path is formed by a hardwired interlock system described in Chapter 12. For the ITk Pixel Detector the control and feedback path is the interface between operator and detector and covers use cases like calibration, commissioning, and data taking. It steers all components of the detector and provides monitoring information as feedback. It is made up by the DCS network, consisting of DCS chip and DCS controller. This path is mandatory for the detector operation and therefore requires a high reliability as well. Details of the control and feedback path are described in Section 15.4. From the DCS computer the commands are sent to the DCS controller over a long term protocol. The CAN protocol is currently envisioned for use.

The diagnostics path provides the operator with additional monitoring values in order to debug the behaviour of the detector or tune its performance. It delivers information per front-end chip and so provides the most detailed information. As it is embedded into the data stream no additional lines are required.

15.6 Data Acquisition and Transmission

A full GEANT4-based simulation of minimum bias events with $< \mu >= 200$ was used to derive hit and cluster rates. The Pixel layout was based on five extended or inclined barrel layers and full end-cap disks as described in Section 3. Pixel hits are derived from particle hits using the IBL digitisation modified to be compatible with the front-end pixel size of 50 μm $\times$50 μm and an expected lower threshold compared to IBL.

The resulting occupancy for the extended layout is shown in Figure 15.25 for the five barrel and the four end-cap layers. In the barrel region, the ratio of pixel hits per particle hits rises towards the higher η region due to tracks traversing many pixels. In the end-caps, the ratio of pixel hits per particle hits is similar over all layers.

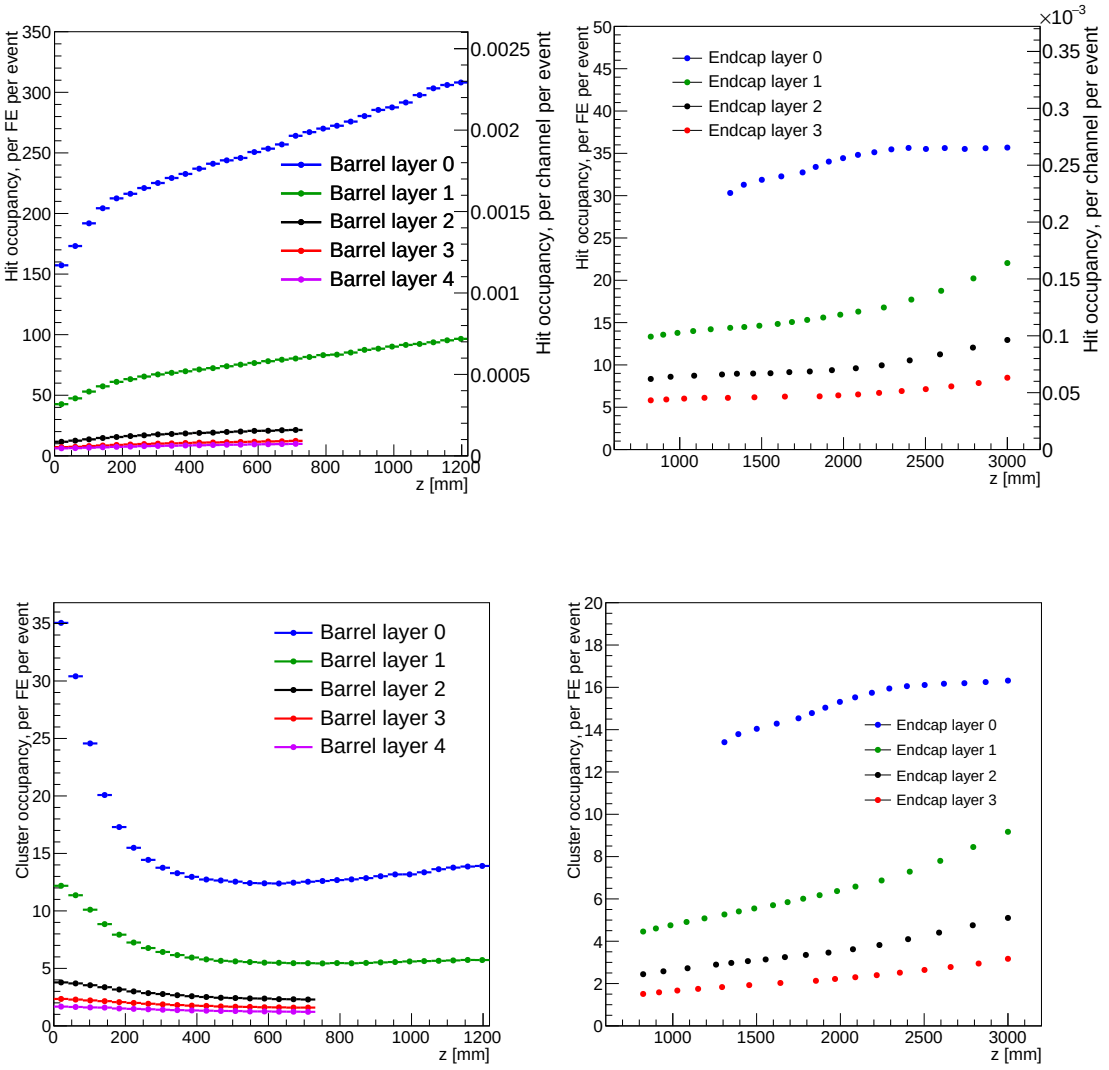


Figure 15.25: Occupancies in barrel and end-cap layers from a minimum bias simulation with extended layout; top: hit occupancies, bottom: cluster occupancies.

15.6.1 Read-Out Simulation Studies

The performance of the read-out chain was simulated focussing on the innermost barrel layer for which the requirements are most challenging. In the innermost layers the accumulated hits are read out as clusters. It is assumed that the front-end stores clusters in a 3×3 pixel window[8)] with 64 bits being sufficient to read out the full cluster information, i.e. address of the hit, distribution of hits in the cluster, and the measured charge determined

[8] This is a working assumption given that the actual design of a RD53-style ATLAS chip is still pending.

as ToT[9]. In the central barrel region, such front-end clusters correspond to actual particle clusters while at high η in the extended layout several front-end clusters per particle cluster must be read out, with the cluster rate estimated to be similar to the central barrel region. Figure 15.26 (left) shows the latency to accept 99% of the L0 triggers (signal from the first hardware-based trigger level, see Chapter 16) to be processed for a fixed maximal read-out bandwidth of 5 Gb/s. Different cluster rates are taken into account: 10 corresponds to the cluster rate per front-end per event at the outer radii, while 35 clusters per front-end per events is expected for the innermost layer. These numbers are based on the minimum bias simulation described above. A cluster rate of 50 per front-end per event is simulated to estimate some headroom in case the inner radius is reduced. It can be easily seen that for higher trigger rates the latency is increasing rather quickly. For a given latency the maximal trigger rate can be estimated.

Furthermore the bandwidth required can be estimated from Figure 15.26 (right). For the cluster rate of 35 per front-end and event expected for the inner radii the latency to accept 99% of L0 triggers is simulated versus the trigger rate for various read-out bandwidths. The bandwidth required for a reasonable latency is therefore estimated to be 5 Gb/s for the inner radii layers. But this is only valid up to 1...2 MHz trigger rate. A significant data compression is already assumed in these simulations.

In summary, it can be stated that the trigger rate for the inner radii should not exceed 1 MHz if the latency to read out 99% of the clusters at 5 Gb/s bandwidth should be below 10 μs. For the outer radii even higher trigger rates, up to 4 MHz, are possible.

15.6.2 Bandwidth Estimations

Bandwidth needs for the data transmission are driven by the trigger requirement to allow an L0 accept rate of 1 MHz. The ITk Pixel Detector will be read out fully at L0 independently of the trigger architecture and a possible second (L1) trigger level (see Chapter 16). Based on the maximum hit occupancy of the simulations described at the beginning of this section and assuming a raw hit data word size of 26 bits, the data rates per front-end link were estimated. For the innermost barrel layers, a data compression based on on-chip clustering is considered as described above, assumed to effectively reduce the hit occupancy by about 0.5 while an effective compression of one was assumed for the outer barrel layers and for the end-caps because the expected hit rate allows full read-out without compression.

Table 15.7 shows the parameters of the transmission path for the pixel modules in the barrel and end-cap layers. The average raw data rate per link for the outer layers approaches the input data rate of the envisaged lpGBTx chipset of 1280 Mb/s, leaving little or no headroom for most layers. The outermost barrel layer or ring could be read out by lpGBTx, which however is discarded for reasons of keeping the read-out homogeneous.. Therefore

[9] Time-over-threshold, the time that the signal remains above the discriminator threshold.

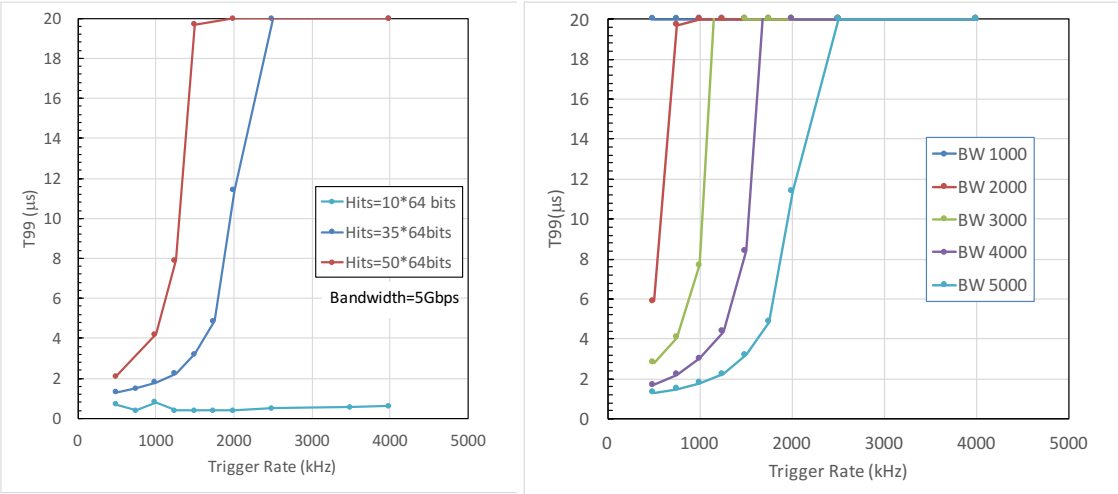


Figure 15.26: Simulated latency to read out 99% of L0 triggers. The latency is simulated vs. the trigger rate for either different cluster rates (left) or different read-out bandwidth (right). 10 clusters per front-end per event are expected for the outer radii, 35 clusters per front-end per event for the inner radii. The simulations are done with either fixed read-out bandwidth of 5 Gb/s (left) or fixed cluster rate of 35 per front-end per event (right).

the format to be defined for the front-end chip will be also used for transmission on the electrical links described below.

15.6.3 Link Architecture

Due to the very high radiation levels expected in the innermost detector volume, placing the opto-elements at the end of staves or rings is not feasible. Therefore, the data transmission link will be split into an optical part, running from the counting caverns down to the ID-end-plate region (final location still to be defined, a radiation dose in the order of 10 MRad is expected) and an electrical part, connecting the opto-components to the front-end electronics on the rings or staves.

The off-detector components are located in service caverns with negligible radiation levels and therefore can be off-the-shelf commercial components. Optical plugins and FPGA based signal processing logic will be placed here. The optical signal will run via optical fibres, which need to be radiation hard to withstand the irradiation along the routing path up to the opto-converter boards including a reasonable safety margin to guarantee an appropriate power budget for the optical link. The electrical part needs to serve the data transmission between optical converters and front-end electronics at the needed bandwidth, which depends on the location inside the detector, and must not introduce too much material into the detector not to disturb the particle flight towards the outer sub-detectors. As the innermost layers will run at the highest bandwidth, this is the driving factor for the de-

Table 15.7: The main bandwidth parameters of the pixel read-out with a 1 MHz L0 rate. For the barrel layers 0 and 1 an effective compression of 0.5 was assumed, no compression for all other layers. The layout of staves or rings is specified according to Tables **??** (extended barrel layout) and 3.5.

Detector layer	Number of modules per stave/ring	Module type	Number of links per layer	Data rate per FE [Gb/s]	Data rate per link [Gb/s]
barrel 0	60	dual	1920	4.20	4.20
barrel 1	60	quad	1920	1.30	2.60
barrel 2	36	quad	2304	0.56	1.12
barrel 3	36	quad	1584	0.24	0.96
barrel 4	36	quad	1944	0.21	0.84
ring 0	24	quad	816	0.94	1.88
ring 1	36	quad	1368	0.56	2.24
ring 2	48	quad	1536	0.35	1.40
ring 3	60	quad	1920	0.21	0.84

velopment. Very thin cables serving a bandwidth of around 5 Gb/s are under development and study.

Electrical Cable Solutions

The electrical data transmission system for the ITk Pixel Detector runs from the front-end read-out chip to the optical transceiver box outside the ITk volume, approximately seven metres away. The point-to-point data links must operate at speeds up to 5 Gb/s for the inner barrel layers and 2.5 Gb/s for the outer barrel layers and end-caps. All of the components, both active and passive, must be radiation tolerant to 2×10^{16} n_{eq}/cm^2 over the lifetime of the HL-LHC. Significant effort has been invested in finding data transmission solutions that satisfy these specifications with the least amount of material in the active detector region.

Long flexible 100 Ω twinaxial cables have been designed and tested for speeds up to 6 Gb/s over distances of 7 m. This transmission rate is achievable with suitable signal conditioning (pre-emphasis, equalisation, signal encoding). Bit-error rate measurements with pseudo-random bit patterns confirmed low error rates and minimal cross talk between shielded differential pairs.

Twisted-wire pairs of extremely fine gauge (wire diameter of 0.127 mm and below) have been designed, also with a characteristic impedance of 100 Ω. This design features less material than the twinaxial solution tested over longer distances. These cables successfully transmitted data over 1 m at rates up to 6 Gb/s with no errors, but the error rate increased

dramatically for transmission over longer distances. A hybrid solution composed of 1-m twisted pair plus 6-m twinaxial cable is attractive because of the minimal material in the central region and a robust transmission rate over long distances.

Kapton flexible printed circuit cables also offer a radiation-hard, low-mass electrical transmission solution. These flex circuits have been irradiated to the expected neutron-equivalent fluence with no degradation in electrical properties. At least two solutions for data transmission inside the pixel volume using Kapton flex technology with a differential embedded micro-strip arrangement and cross hatched ground plane have been developed. The Kapton flex option can easily incorporate low voltage for serial powering, high voltage for low current detector bias, controlled impedance differential pairs for a shared chip command and clock signal, and connections for module temperature sensing in addition to the differential data transmission. For each module, the front-end chips share a clock and a control line, but each front-end has a dedicated data line. Both flex designs have demonstrated transmission over 1 m with rates above 5 Gb/s using signal pre-emphasis and equalisation in addition to 8b10b encoding[10)]. The required rate can be achieved without significant cross talk between adjacent data lines on the flex.

The data transmission lines for the ITk Pixel Detector end-caps operate at up to 2.5 GBit/s. The current design uses small twinaxial cables or twisted pairs, with matched impedances. These cables, which may be the same as those used in the barrel layers, have special conductor and dielectric materials to reduce conductive losses and skin effect losses. Earlier designs used flex cables in a strip-line or micro-strip arrangement, with guard traces between signal lines to reduce interference. The choice of wire cable over flex circuits allows for more flexibility in the layout and for reduced material in the transmission line.

All of the data transmission options for the ITk Pixel Detector depend on robust, low-mass connector options for mating at the front-end chip and optical transceiver (and possibly at the end of the pixel stave). Suitable connectors exist in miniature form and are being characterised in the different design options.

Optical Components

The optical link between off-detector components and on-detector opto-converters should be array-based. This will save space needed for the connectors and driver/receiver circuitry and saves multiplicity in terms of connector front-end electronics. Two approaches are followed currently, one is based on the experience made for the Run-1 Pixel detector and one is based on the Versatile Link+ project developments. In general 12-channel optical transmitters and receivers will be used. The basic requirements are:

- The transmitter is optimised to operate at 5 Gb/s per channel,

[10] 8b/10b is a line code that maps 8-bit words to 10-bit symbols to achieve DC-balance.

- electrical signal equalisation to properly receive the signals from the electrical cables are to be added if needed,
- the transmitter and receiver connect to a 12-way fibre ribbon each,
- the receiver is optimised to operate at 2.5 Gb/s (5 Gb/s),
- transmitter and receiver operate within the environment of the ATLAS detector.

In the following the two concepts will be described.

Opto-board based development

Based on the experience from the Run-1 and Run-2 Pixel detector, studies for the design of optical links based on the opto-board concept, which has been successfully deployed in the two generations of optical links for the Pixel detector of ATLAS, are ongoing. There will be two flavours of opto-boards, one for transmitting and the other for receiving optical signals. Each transmitter opto-board contains an ASIC with 12 channels of VCSEL (Vertical-Cavity Surface-Emitting Laser) drivers for coupling to a 12-channel VCSEL array. The ASIC will be operating at 5 Gb/s. Each opto-board receives the electrical signals via thin cables from the pixel modules about seven metres away. Each receiver opto-board contains up to 12 channels of receivers to amplify the signals from an array of PIN diodes. Each receiver will be operating at either 2.5 Gb/s (if using 130 nm CMOS technology) or 5 Gb/s (if using 65 nm CMOS technology). The received signals would then be sent to a lpGBTx (Gigabit Transceiver, see Section 12.1) chip for de-serialisation into multiple 160 Mb/s signals for transmission via thin twisted pair cables to the pixel modules up to 8 m away.

The transmitter ASIC, the VCSEL driver, has been successfully prototyped in a 4-channel version using a 65 nm CMOS technology. The corresponding transmitter opto-board has also been prototyped. The optical package for the VCSEL array is very similar to that used in the second generation opto-boards and the RXs modules (the off-detector optical receiver modules) produced for phase-0 upgrade. The optical coupling uses commercial connectors which can be readily mounted and dismounted during production testing and installation. The performance at 5 Gb/s is satisfactory [142]. The plan is to lay out the ASIC in 12 channels in the near future. For the receiver ASIC, the plan is to take the single channel GBTIA circuitry (IP) and lay it out in array format. Also needed is the de-serialiser in the lpGBTx which should also be laid out in an array format.

Groups of opto-boards will be mounted inside an opto-box, a mini-crate similar to that used in the second generation optical links of the Pixel detector. Due to space constraints, the opto-boxes for only two inner barrel layers and possibly the inner most end-cap rings will be located inside the ID end-plate. The remaining opto-boxes will be mounted near the LAr electronics The arrangement is similar to that of the current Pixel detector. The use of array-based receiver opto-boards reduces the physical size of each opto-box by a factor

of two, a much needed space saving. Overall, there are ≈20 K data links and ≈10 K TTC links (or ≈ 3 K TTC links with the use of lpGBTx array proposed above).

Versatile Link Array Driver (VLAD) Development

Recent developments towards a compact radiation-tolerant array optical transmitter module (ATx) [143] provide a prototype candidate. This optical transmitter will have the following additional features:

- The transmitter is low profile, low power and operates without a heat-sink.
- The transmitter provides channel redundancy built in and is controlled through an I^2C interface.

The module consists of a VCSEL array and a connected VCSEL array driver. This array driver ASIC (VLAD or lpVLAD[11)]) has been designed and prototyped in the TSMC 65 nm CMOS technology with less channels. It operates with a data rate of 10 Gb/s per channel. The fibre connection will be done via commercial connectors. Together with the ATx module, this new driver can be used for test purposes in a read-out system to study its behaviour in a close to real detector system [144]. With this the performance of optical transmission, power consumption, heat load and others will be tested in system testbeds once available. A 12-channel version with built-in redundancy and an equaliser circuit in the receiver part is foreseen for the coming year based on the testing experience using the prototype ASIC.

15.6.4 General Read-Out

Read-out related activities in the next years will address the compatibility of the concept of an ATLAS-wide general read-out system based on FELIX as discussed in Chapter 16 and in addition provide test benches for module and system development needs. Apart from more stringent requirements concerning data rates, the concepts for off-detector read-out of Pixels are very close to that of the Strip Detector. Differences are described in the following.

The TTC links are operated at a bandwidth of 160 Mb/s, likely using 8b10b[12)] encoding. This makes sending of more complex commands than a simple trigger signal possible. Consequently, it is considered to send full or at least reduced trigger counter information with the bare trigger signal. This allows a more robust cross-check of bunch-crossing and trigger counter synchronisation with the off-detector read-out than the conventional simultaneous off- and on-detector counting. Sending of trigger tags needs to be accommodated in FELIX.

[11] VLAD: Versatile Link Array Drive, lpVLAD is the low power version.
[12] 8b/10b is a line code that maps 8-bit words to 10-bit symbols to achieve DC-balance.

The TTC links are aggregated using the lpGBTx protocol and thus follow standard FELIX specifications. In contrast, the data links will use the encoding as provided by the front-end such as 64b66b[13)], possibly after multiplexing of the links of front-ends on one module in case the available bandwidth allows this, which can be accommodated by FELIX.

Data of some pixel layers may be used for fast track-finding between L0 and L1 triggers. Given that the Pixel front-end will send all data on the arrival of a L0 trigger, storage and distribution between L0 and L1 triggers must be dealt with in the off-detector read-out system.

15.7 Global Pixel Mechanics

The design of the local supports for the ITk Pixel Detector depends upon the type of the layout that will be adopted. At the moment the layout is not frozen yet. However, most of the mechanical options under study for the barrel section are self-supporting i.e. the local support provides the required stiffness without the need of major external structures.

In contrast, end-caps are organized in "layers" of rings supported by cylindrical shells as described in Section 15.3.3.

The Work Packages to be executed in SR1[14)] are still under discussions and they depend upon the commitments that the collaboration groups will engage with. However, the baseline is as follows:

- Outermost Barrel: The barrel section of the Outermost Assembly is integrated in SR1 starting from loaded (with modules) Local Supports.
- Outermost Disk Assemblies: The two end-caps are not integrated in SR1 where they are delivered in two units already tested.
- Outermost Assembly: This Sub-assembly is composed by the Barrel, the two end-caps, and the Inner Support Tube (IST). Integration of these parts takes place in SR1.
- Innermost Assembly: It is formed by the innermost barrel local supports, the forward parts and the beam-pipe. Although actually planned in SR1, its integration might take place in other labs and be delivered to CERN as one unit.
- Outermost insertion into Strips: The Outermost assembly will be inserted first into the Strip Detector sliding in the Pixel Support Tube (PST). The operation will take place on surface in SR1. A second composite tube (IST) is supported off it the at the lowest radius.

[13] 64b/66b is a line code that maps 64-bit words to 66-bit symbols.
[14] SR1 is the Assembly Facility at ATLAS Point1 in building 3197.

- Innermost Insertion into Strips: The Innermost Assembly carries the Beam-pipe and it will be also installed on surface. Although the innermost Layers are designed to be replaceable in the pit, the integration plan foresees its first insertion into Strips on surface in order to minimise the work in the pit. In fact the ALARA[15] principle, adopted by ATLAS, forces to minimise the dose delivered to the personnel and to avoid distributing unjustified doses to the personnel. A dose is considered unjustified when there is a reasonable alternative that can avoid it. Inserting the Innermost Assembly on surface is certainly a reasonable and possible alternative.

Both of the insertions will be conducted by means of a ZIF system (Zero Insertion Force) that allows to provide the required pulling force without exchanging components with the Strip Detector. It is a concept tested on the current Pixel detector: the pulling force required to slide the detector along the PST is grounded back to the PST shell through the flange at PP1[16]. The result is a force system that evolves inside the PST and anything outside it, like the Strip Detector, sees it as a PST "internal force" and therefore it cannot share forces with it.

The ITk Pixel Detector requires a sealed dry volume at PP1. The humidity and thermal barrier does not provide enough cross section to accommodate the thermal insulation on the cooling lines. Such sealed volumes (one on each PP1 side) will be installed and tested at the end of the integration phase after the insertion of the Pixel sub-detectors into Strips is completed.

[15] ALARA: As Low As Reasonably Achievable

[16] Patch-Panel 1 (PP1) is located at about $z = 3500$ mm from the interaction point and it houses the services brakes (i.e. electrical connectors, fittings)

16 Off-Detector Electronics, Read-Out and Control

The ITk read-out and control architecture is closely coupled to the ATLAS TDAQ common read-out and control architecture. The TDAQ community will provide a software framework, and common hardware platform and associated interfaces that will be used wherever possible throughout the Phase-II upgrade of ATLAS. This section details aspects of the system common to both the ITk Strip and Pixel Detectors, with Strip specifics in Section 16.8, that follows.

The details of the TDAQ architecture will be presented in the TDAQ Technical Design Report that will be released in 2017. The front-end ASICs and the off detector data formats are still under development. For this reason development will continue to evolve. It is foreseen that an ITk-TDAQ read-out demonstrator will be built in years 2017 to 2018. It will be used the characterise the performance of the system.

An overview of the TDAQ architecture, is shown in Figure 16.1. On the left is the baseline architecture - with a single-level trigger which operates at a maximum of 1 MHz. On the right is the optional two-level trigger based architecture that may be introduced later in Phase-II operation. In designing the read-out, care is taken to ensure that the detector can be read out in either mode. In the baseline architecture all data is read out after receiving a Level-0 trigger (as happens in ATLAS today, except it is called a Level-1 trigger). In the optional scheme a second stage trigger - Level-1 - and a hardware track-finding system are added. In this case the Level-0 trigger does not initiate read-out of the entire detector, and the track-trigger is used to refine the Level-0 decision using data read-out from fractions of the detector, such that the Level-1 trigger can read-out a reduced number of events.

The Front-End Link eXchange (FELIX), the Local Trigger Interface (LTI) and the Data Handler (DH) are the TDAQ components used by the ITk off-detector electronics [145]. All front-end data and control signals flow through the FELIX fibre-interface and, subject to further studies and development, detector-specific firmware will reside here. The LTI interfaces with the ATLAS Trigger, Timing and Control (TTC) system and generates ITk specific signalling. The Data Handler processes ITk data in software and interfaces with the data storage system. Overall management is via ITk Controller software, residing on a dedicated or shared PC.

The ITk-FELIX component may deal with a set of firmware for dealing with the front-end links, data formats and critical processing. Formatting of the triggers and other signals and

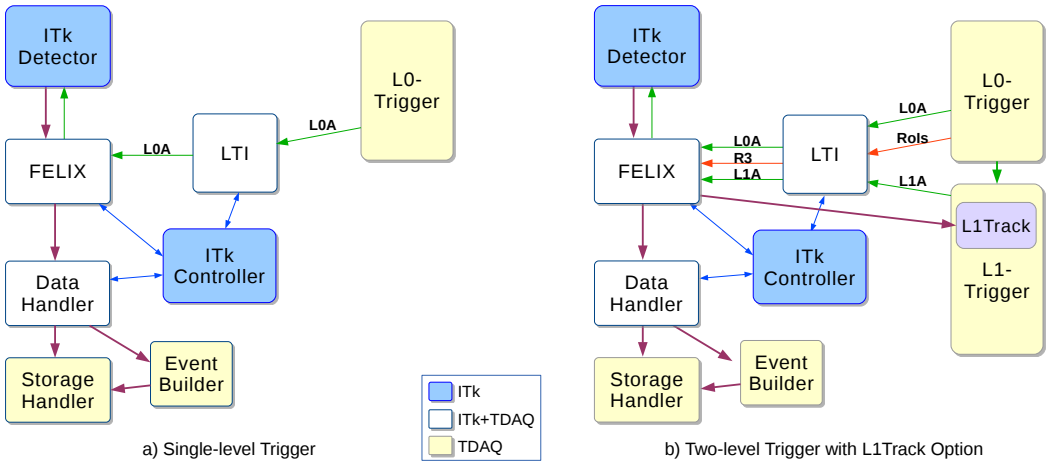


Figure 16.1: An ITk centric view of the TDAQ architecture, showing a) the baseline single-level trigger architecture, and b) the two-level trigger with Level-1 track-trigger option.

commands into ITk specific protocols may also take place here. The ITk Data Handler will be a software package that resides within the TDAQ standard PC/software architecture.

The read-out of the ITk detector is handled by a combination of FELIX units and Data Handler PCs. Front-end control will be via LTI units coupled to FELIX units, and may also include portions of FELIX firmware. The ITk Controller will be responsible for coordinating these devices, for instance when calibrating, or while starting a physics run. The bulk of the read-out operations will be performed by the FELIX units and Data Handlers, while the interfaces to the ATLAS global triggers and control, and local signal generation and distribution will be provided by LTIs.

In each of the TDAQ common units - LTI, FELIX and Data Handler - ITk specific firmware or software possibly will be required in agreement with the ATLAS TDAQ group. The Controller will run dedicated ITk software, using TDAQ libraries to communicate with the lower-level systems. The use of both common and custom infrastructure by the ITk predicates a number of interfaces that need to be carefully specified. Figure 16.2 shows the interactions between the various components. It is expected that system management will be via a TDAQ specified common messaging infrastructure, as depicted by the orange arrows. Connections between ITk specific functions and TDAQ functions (the orange boxes) will be via specified interfaces to allow for easier development and maintenance.

Figure 16.3 shows a functional view of the system, including some TDAQ functions. It is split between read-out (left) and front-end-control (right). Read-out looks after the reception of data, routing as needed, monitoring and analysis, storage and fragment building. Front-end control covers clocks, triggers, resets and configuration. Common to both paths is calibration. Although read-out and control operate independently in most cases, when

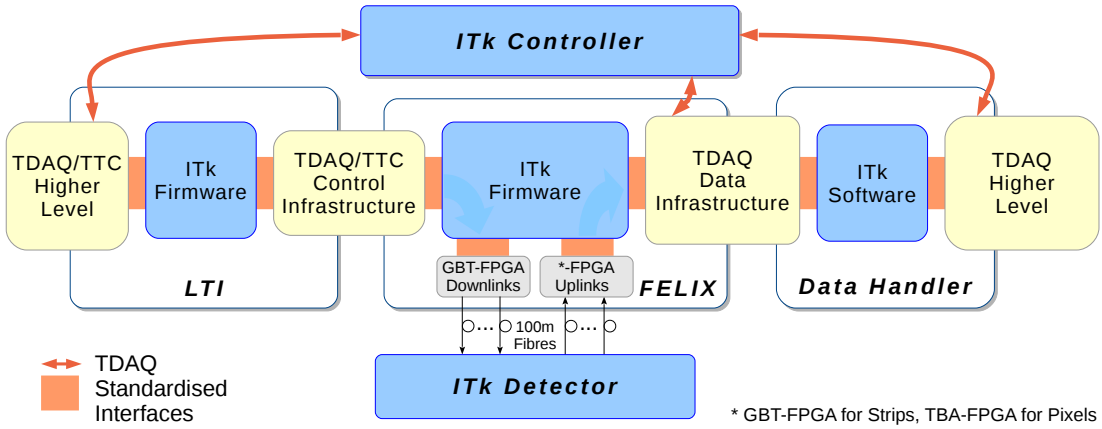


Figure 16.2: Diagram showing the FELIX, Data Handler, LTI and Controller interfaces

performing a calibration loop the operation must be synchronised - this is covered in Section 16.5 for details.

The ITk Controller oversees data-taking, providing an interface and hub for the ITk coordination of the system. It is capable of independently controlling multiple divisions of the ITk detectors, but it is not yet known whether this could be a single shared system for all of ITk, or dedicated instances for both the ITk Strip and Pixel Detectors. An operator console completes the system. It will be a dedicated expert terminal, located, for instance, in the satellite control room.

16.1 FELIX

The ITk on-detector electronics are connected directly to FELIX off-detector via optical fibres approximately 100 m long. At the highest level, the FELIX can be described as a unit that interfaces between a detector specific signalling and a standards based signalling protocol (e.g. Ethernet) where possible [146].

This is a change from the current inner-detector system (e.g. SCT) where all of the (electronic) low-level bi-directional access to the detector modules is performed within one VME crate and mostly within one VME board. Using a FELIX, data is sent to the Data Handler PC for processing. This is a promising line of development and will be studied in detail in 2018.

In the counting room, the fibres from the individual staves and petals connect to FELIX units. Inside each FELIX FPGAs will provide the necessary resources for decoding the ITk unique front-end protocols. The front-end data-frames and packets may be processed by

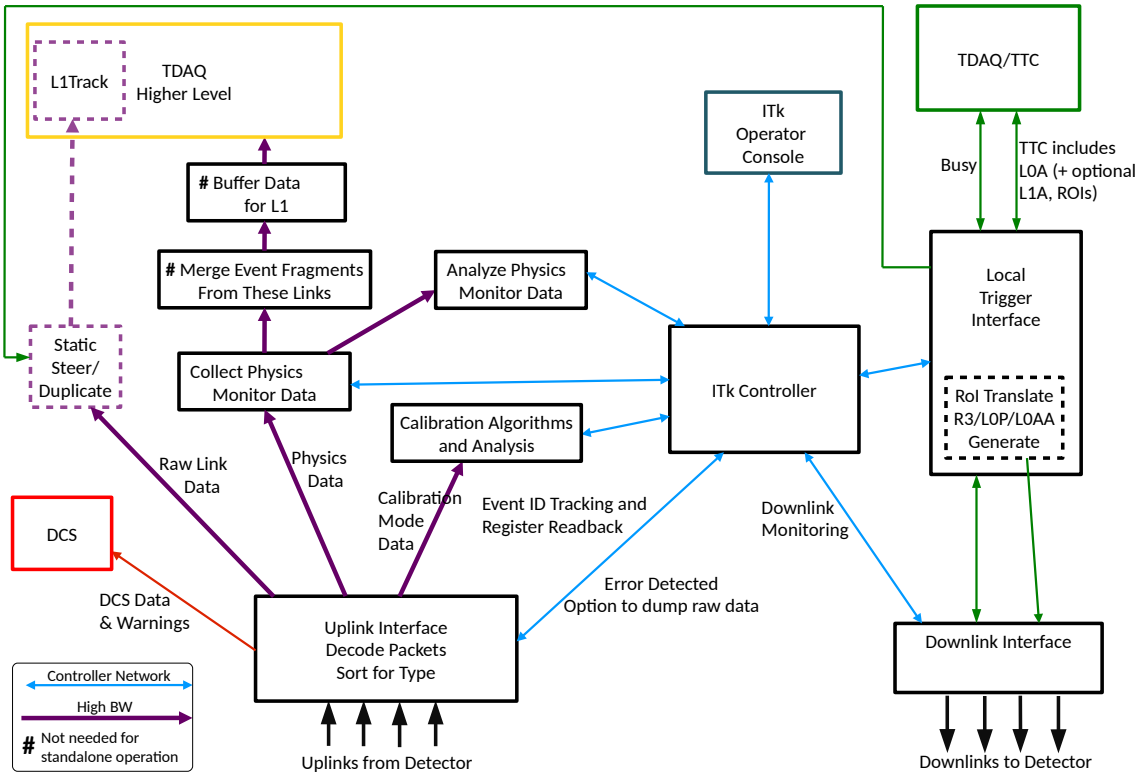


Figure 16.3: Off-detector read-out and controls overview

ITk specific firmware, responsible for decoding the custom front-end-data encodings/formats, performing all ITk functions and interfacing to standard FELIX data-formatters and data transport (for transferring data to the Data Handlers).

As the FELIX is shared with TDAQ, and still under development, a description of the ITk requirements of the TDAQ system follows.

16.1.1 FELIX Functions

Front-End Physical Link Interface

Depending on the nature of the physical optical link, different optical transceiver plug-ins are required. The ITk will use VTRx+ links with VTRx+ specified plug-ins, except for the ITk-Pixel uplinks, where other options may still be explored. The modularity of fibre-ribbons, and that of the plug-ins also need to be taken into account.

Front-End Frame Interface and Decoding

The front-end link and e-link configuration is customisable and highly detector specific. For example, data from each HCCStar are not aligned with respect to data from other HCCStars. The data is transferred serially, so a dedicated deserialiser and packet detector is needed. In cases where 8b/10b encoding is used in the HCCStar, dedicated 8b/10b decoding will also be needed.

Data-Type Handling

The link from each front-end hybrid carries multiple data types. Firmware will separate these data into different queues as needed. In general all data will go to the Data Handler, but with a few important exceptions:

- **Error flagging/handling and monitoring:** To ensure prompt recovery from errors that are numerous and unavoidable (because of radiation induced SEU for example), it will be advantageous to deal with errors within the FELIX firmware, or to send an alert to the Controller. Any errors detected in the front-end-frame or clock and data recovery (where used) will be reported. If errors become frequent on a link, the raw data can be dumped through the ITk Controller to the ITk Operator Console for further diagnosis by the experts (see Figure 16.3). Each packet will be examined for any recognisable corruption and if any is found, an error flag message will be sent to the ITk Controller with the option of dumping the bad packet to the ITk Operator Console, discarding the packet or accepting the packet even with the corruption. To reduce the error-message volume, it is required that errors be counted and messages only sent when thresholds are transgressed.
- **Calibration:** When calibrating the front-end modules, large numbers of triggers and much higher occupancy levels (a factor of 10000 more in the Pixel case) generate large amounts of data. This data determines the configuration used for the next set of triggers. To minimise calibration time, calibration data may need to be dealt with in the FELIX, where histogramming and/or event counting can be handled locally, before the added delay of sending the data to the Data Handler. More details of this process can be found in the Calibration Section 16.5. Details specific to the ITk Strip Detector, including data volumes, are in Section 16.8.3.
- **Track-trigger data:** In the case where a hardware Level-1 track-trigger (L1Track) is connected to FELIX- implying a two-level trigger architecture, the Strip Detector will use a regional signal to obtain some data (<10%) early, and Pixels will read-out all layers at the L0 trigger. This high priority data will be filtered and forwarded to the L1Track processors using a low-latency data path under the responsibility of TDAQ. Optionally the data can also be sent on as standard data to the Data Handler. For the ITk Strip Detector, L1Track data will arrive at the FELIX with a unique data-type and

can be sorted using this identifier. For Pixel data a filter on FELIX could make use of regional information from the L0-trigger system to sort data, or all the data could be sent to L1Track.

Additionally, the ITk Strip Detector transfers Detector Control System (DCS) data mixed with event-data, and this is detailed in Section 16.8.2 later in the chapter.

Busy

If any of the queues in FELIX exceed a depth threshold, the busy needs to be asserted. Other error conditions could also generate a busy, for example a large number of links sending bad data, but this needs to be considered in conjunction with the ITk Controller operation. For instance, the errors could be flagged to the Controller, and it asserts busy, or it could set count or rate thresholds in the FELIX that automatically generate busy. Front-end data will also contain information about error states and FIFO depth that FELIX can use to generate a busy. If this is exercised, and for it to be effective and not swamp the system, logic will be needed to aggregate and pre-scale these sources.

Event Integrity Checking (Low Level)

Beyond checking for data corruption, event data may need to be checked for synchronisation and correlation with the sent-trigger information (the trigger tag, and possibly bunch-crossing identifier).

This is performed as near to the front-end-links as possible because the near-synchronous behaviour can be used to provide error information. For example, the time between sending a tagged-trigger and data returning with that tag can be used to diagnose congestion. During commissioning a comprehensive picture of the data-flow and congestion points will be built up.

Control Functions

The FELIX sends clocks (via the lpGBTx directly) and control signals (via lpGBTx e-links) to the detector. Most of the control functions are handled by the LTI, but some may be duplicated such that they can be applied to each downlink individually, for example local triggers and resets. In particular the encoding of TTC signals into the detector front-end-protocols should be done in the FELIX. Some signals, for example configuration streams, will need delay paths to facilitate interleaving with synchronous signalling like triggers.

Command Stream

FELIX will provide the capability to send command streams - both broadcast or unique to each downlink. These will be buffered in the FELIX to allow for asynchronous transmission in-between triggers, because the trigger and commands share the same downlink. It is presumed that lists of many commands (10-1000 per downlink) will be stored on FELIX to minimise time wasted between communicating that a list is nearly empty and it being re-filled.

Register Refresh

Even with SEU protection the front-end chip configuration registers are refreshed with some regularity. It is expected this will be needed every 2-10 minutes. There is sufficient downlink bandwidth to support this, but the exact requirement will depend on the final ASIC design (Section 6.2.3 has more detail on SEU). This can be done by drip-feeding configuration commands - possibly by inserting a register write in each orbit, or when the trigger is not active. This may need a local mirror of front-end registers in the FELIX and will need to respect the orbit timing.

16.2 Data Handler

The Data handler implements the final detector-specific data processing layer before event data is sent to the global storage handlers, e.g. formatting and/or monitoring [147]. The Data Handler is a TDAQ PC with a common software framework in which ITk software components are run as well. The infrastructure can be shared between physics and calibration running.

Front-end data will be parsed and decoded into hits or register data. These data will then be grouped and passed onto the relevant TDAQ or ITk components using common software elements.

16.2.1 Stand-Alone Local Running

In standalone running, a trigger is generated locally in the LTI (more details in Section 16.3 below). This will sometimes be a common trigger from the top-level ITk-LTI, but an LTI could send different triggers to different sub-trees down to individual triggers to individual staves. The Data Handler will need to communicate with the LTI to determine which triggers were sent to where and therefore which data to expect from the FELIX.

Histograms will be populated from this data and fits performed where needed (particularly for calibration). Results will be gathered for perusal by the ITk Controller and stored in long-term storage (around 100 MB per stave side per calibration session).

16.2.2 Fragment Merging

Data can be grouped by L0ID - such that larger event-fragments can be sent to downstream TDAQ.

16.2.3 Register Read-Back

Register read-back data can be compared with expected values, or forward to the ITk Controller.

16.2.4 Event Integrity Checking (High Level)

Event-data trigger numbers (L0ID or tag) and bunch numbers (BCID) will be compared with those sent with the trigger, or information received with a trigger from higher up the hierarchy, and any discrepancies flagged. This functionality will be shared with that of the FELIX firmware, although at this level there is more detail from the multiple links and triggers available to aid a detailed analysis.

16.3 Local Trigger Interface - LTI

The ATLAS-wide TTC system connects to the ITk via LTIs. The LTI is also connected directly to the Level-0 Trigger System, and the Level-1 Trigger System in architectures where this is implemented.

The LTI forms part of the hierarchy of control signal distribution and generation, connecting directly to FELIX. Much of the ITk control functions could be driven by either the FELIX, or the LTI. This division will need to optimised based on programmability and FELIX- LTI bandwidths and other factors that will become clear as the design progresses.

In stand-alone operation the LTI is expected to provide a subset of the functions normally provided by the Central Trigger Processor (CTP).

16.3.1 Local Triggers and Other Broadcast Signalling

Generation of triggers for debugging and calibration of a portion of the detector (a partition) can be done by the LTI. For example asynchronous calibration of two staves. Local generation of synchronous signals, bunch-counter-reset (BCR) for example, needs to take place in the LTI.

16.3.2 Busy

The LTI will receive a busy from systems nearer the detector (e.g. FELIX) or the ITk Controller (e.g. when configuring the detector before a run). These signals are aggregated and either transferred to higher-level ATLAS TTC , or acted upon locally when the LTI is generating triggers (e.g. trigger gating). Busy monitoring functions (e.g. histogramming) can also take place in the LTI.

16.4 The ITk Controller

The ITk Controller manages the data-flow from the detector, and forms a hub for status and error flagging. The unit will likely be a PC, connected to all other systems via a dedicated Controller network. In most cases only commands and status updates will travel on this network, but it may be required that it can handle debug data dumps (tens of megabytes) if other means are not present.

During data-taking, the Controller will set up the core systems to receive physics triggers (including the configuration of the modules), build monitoring histograms and then keep track of status and handling any errors when running.

During non-physics running, module calibration will be coordinated from the Controller.

16.5 Calibration

To calibrate the front-end electronics for optimal performance, various regular calibrations runs are required. To calibrate the front end electronics of a binary read-out system, a parameter is set in the front-end ASICs, data accumulated (as a result of sending a sequence of triggers), changing the parameter value, sending more triggers and so on.

The most important use cases are the response curve and trim scans. These are based upon a large number of threshold scans, so that the changes in the noise and threshold as a function of injection charge can be monitored, and fine tuning of the threshold for each channel applied.

In more detail, calibrations are carried out using a hierarchy of loops over bursts of triggers. The different levels of the hierarchy include the main scan parameter(s) as well as mask changes (for charge injection, avoiding cross-talk or very high occupancy events). For the innermost loop, a trigger will be an arbitrary short command sequence sent to the front-end chips in order to generate a response. This includes injecting a calibration charge, sending L1, R3, L0 triggers, as well as register read-back commands. For diagnostics purposes, a trigger sequence might be specified in terms of the raw signals to be sent on the e-links (i.e. sent without any encoding). This command will be repeated many (e.g. 100) times and in order to make the complete scan as fast as possible, an automatic adjustment of the repetition frequency depending on the amount of data being received is desired. Otherwise, delays created in this loop will be multiplied by the repetition from higher parameter loops levels.

Calibration thus depends on closely coupled nested loops - the operation of these needs to be optimally shared between the front-end ASIC, FELIX, LTI firmware and Data Handler. Much of this is dependent on the dead-time (unused time between loops) of the system.

The calibration procedure will involve sending the entire chip configuration at the start and individual portions of the configuration as part of the loop structure configuring individual registers for each burst of triggers. A scan is made up of bursts of triggers, with a different configuration applied for each burst. A series of these scans is analysed and used to build a picture of the module status and performance. The calibration needs to be done simultaneously for multiple modules, requiring configuration data with different values to be sent out for each scan.

The immediate result of the trigger loop will be a representation of the data acquired during this burst. This will usually include the occupancy histograms, but other data will be useful, including histograms of chip occupancy, cluster size and count. For low-level investigations, a direct map of the bits on the link might be collected.

Histograms can either be built in the FELIX or in the Data Handler. For the ITk Strip Detector, there is an option to histogram hits in the front-end ASIC in a very low-level form (hit counter per strip). When histogramming in the Data Handler, where the data might be available only asynchronously, it should be pointed out that this data needs to be correctly assigned a loop index in order to put the data in the appropriate histogram bin.

16.6 Monitoring

During data taking (but not necessarily enabled all the time) the physics data will need to be monitored. This function will also be an important part of the stand-alone operation during integration.

The primary purpose is to look for faults in modules that may not be obvious from examining data available at the output of the event builder and to respond to any warnings issued

by the on-detector electronics. The collection of this data must have no effect on the physics data flow.

Monitoring data will be passed from the FELIX and Data Handlers to the Controller for assessment. Potentially all data sent from the detector should be available to be monitored, although in practice the volume of data used at any time will need to be within the capabilities of FELIX and Data Handler resources.

16.6.1 Collect and Analyse Physics Monitor Data

In addition to chip occupancies, this monitoring should include measuring the occupancy of the front-end link, i.e. how much more data can be sent down this link. This is a function of the raw event size, and the space between packets. Another important variable to keep track of is the latency, how much time has passed between the transmission of the trigger and reception of the last data.

16.6.2 Triggers that are not Useful for Data Analysis

It will also be useful to collect data based on conditions when no hits are expected, for example looking for stuck memory cells, or based on low level event characteristics like unusually large events, which could be due to a threshold misconfiguration (caused by an SEU).

16.7 Track-Trigger Option

The ATLAS detector for Phase-II physics will have a single-level trigger, but will retain the option to add a Level-1 track-trigger (L1Track) [147].

To use tracking information ATLAS will operate in a two-level trigger mode. The first trigger, the Level-0 Accept (L0A), generated by the TDAQ L0-trigger system, is used to initiate the storage of data in buffers on the front-end ASICs. A second trigger, the Level-1 accept (L1A), from the L1-trigger system initiates the transfer of the event data for the strip detector and outer pixels.

In the two level architecture, the L0A rate is expected to be 2-4 MHz, and the L1A at 600-800 kHz. The L1-trigger only operates on events identified by the L0-trigger, and, to achieve the rate reduction, needs additional information - in this case tracks from the ITk.

The period between the L0A and the L1A trigger signals is used to extract data from the detector, perform the tracking and integrate the results with other L1-trigger components. The time available - 15-20 μs - imposes tight latency requirements - as low as 5 μs - on the time needed to transfer data from the detector to L1Track.

This is achieved in 2 ways: the ITk Pixel Detector outer barrels and disks will read out upon receiving an L0A, and the ITk Strip Detector will make use of a third signal, the Regional Read-out Request (R3) that acts like the L1A - initiating read-out, but only affecting a small portion (<10%) of the ITk Strip Detector. This is detailed in Section 16.8.6.

To further reduce latency, the data needs to be handled promptly in the FELIX, where it may be efficient to perform some L1Track related functions.

16.7.1 FELIX L1Track Pre-Processor

The L1Track system is a responsibility of ATLAS TDAQ group and will be fully detailed in the TDAQ TDR to be released by the end of 2017. The system will conceivably have multiple track-finder units arranged in a number of ATCA shelves. Data from the ITk- all Strip Detector layers and the outer-layer Pixels - will need to be routed to these shelves, and in some cases duplicated to a second shelf. There is a static correspondence between a data uplink and a shelf (or pair of shelves). To reduce the number of links they can be aggregated in the FELIX, where, for example, ten uplinks can be combined into 10 channels on a single 100 Gbit/s link. The FELIX may also be able to duplicate links where needed by L1Track.

The links from FELIX to L1Track will be in addition to those required to send data to the Data Handlers. This may require increasing the number of FELIX units in the system.

16.8 Strip Detector Specific Off-Detector Electronics

The ITk Strip Detector off-detector read-out and control electronics are part of the common ITk DAQ system, shared with Pixels and detailed in the first part of this chapter. This section details functionality unique to Strips.

The ITk Strip Detector has its own front-end chipset, data transfer protocols and link architecture (lpGBT). It also uses a small portion of the read-out bandwidth for sending DCS data off-detector.

16.8.1 Strip Detector Architecture

On the detector, within a module, a hybrid hosts 6-11 ABCStar ASICs connected to the silicon strips. After receiving a trigger and a read-out signal from the HCCStar, the ABCStar ASICs pass their data to the HCCStar ASIC at the end of the hybrid, where the data is aggregated with that from the other ABCStar chips, formatted, optionally 8b/10b encoded and transmitted via 640 Mbit/s serial e-links to the lpGBTx chips at the EoS. The data from an HCCStar are sent as variable length packets - each containing a single data

type (and, for the event-data type, data from only one event). The lengths are expected to average between 15 and 30 bytes. The predominant type (by data volume) will be event-data, but other types include register-readback, occupancy counter data, DCS data and warnings/alerts.

For read-out purposes, each HCCStar operates as an independent unit, transferring data when ready, without any awareness of the other HCCStar ASICS and sending data using its own e-link. This means that, because of variations in occupancy and regional read-out, events will not be transferred at the same time, and are therefore not aligned in time.

The lpGBTx aggregates up to fourteen 640 Mbit/s e-links onto a 10 Gbit/s optical fibre link [148], transporting the data to the counting room using the CERN VTRx+ optical transmission system. The physical transmission and protocol used are internal to lpGBTx VTRx+ chipsets and detailed elsewhere (see Section 12.1).

DCS data from the HCCStar and ABCStar ASICs is also transported over these links. Further DCS data will also travel from the modules using a different route, via the AMAC ASIC (6.2.7, but ultimately via the lpGBTx).

During power up, the DC-DC converter on each module must first be enabled in order to power the HCCStar and the ABCStar chips. This is done by the AMAC ASIC which communicates with the DCS system by means of an lpGBTx slow control adapter (SCA) channel and the downlink fibres. AMAC also includes several ADC channels which allow on-module currents, temperatures and voltages to be monitored throughout the powering procedure.

Ultimately, all the DCS data is routed off-detector via the FELIX system.

16.8.2 Strip Detector-FELIX

The FELIX provides a generic platform for multi-function, multi-detector use. In the Strip Detector case, it provides the only, with the exception of interlocks, path for controlling and monitoring the detector. FELIX may make provision for required sub-detector specific firmware and interfaces, and will need to be able to provide a reliable path to DCS, and mechanisms for decoding Strip Detector specific data.

As the ITk Strip Detector will be using the lpGBTx VTRx+ physical links and protocols, the Strip Detector-FELIX provides end-to-end lpGBTx- to Ethernet-protocol conversion. Inside a FELIX FPGA, the lpGBTx frames will be expanded into their component e-links, and strip-detector specific firmware may decode and process the Strip Detector custom data.

The ITk Strip Detector has 384 petals and 256 long-strip staves with one lpGBTx per side, and 136 short-strip staves with two lpGBTx per side, totalling 1824 uplinks and 1168 downlinks.

The number of uplinks that can be accommodated by a FELIX unit is not yet known, but expected to be between 50 and 100 with 20-40 FELIX units in the system.

Strip Detector-FELIX Functions

In addition to the functions for all ITk, the FELIX may need several customisations for use in the ITk Strip Detector.

- **Front-End Frame-Interface, Decoding:** With use of a CERN library (GBT-FPGA [148]) it is expected that FELIX core firmware will decode the bulk lpGBT frames, and perform the GBT protocol level error detection and correction. The payload data will then be made available via a standardised interface to ITk Strip Detector packet-detection and protocol decode. The first stage of the FELIX firmware will be to de-multiplex the lpGBT frames into their component e-links.
- **DCS Data Handling:** In most cases data flows through the FELIX to the Data Handler, but there are a few important exceptions. In addition to the data-types detailed in the common DAQ Section 16.1.1, the ITk Strip Detector also deals with DCS data.

  DCS data is considered high priority, although not critical for detector safety (See Section 12.2). This data is queued separately from other data, and passed to the DCS subsystem (external to FELIX) via a dedicated and/or prioritised connection. Data will need to be formatted as required by the DCS system. Some additional details are in the Monitoring Section 16.6.

16.8.3 Calibration

Configuration Data Volume

Much of the time spent in calibration is in changing registers on the front-end ASICs. For the ITk Strip Detector this is about 128 registers per chip (32 bits each, but taking about 60 bits to send a register write command). With ten chips per barrel hybrid, 2 hybrids per module and 14 modules per stave side (and half that for a petal side), the configuration sent on each downlink totals about 2 Mbit.

Histogram Data Volume

The calibration data is stored online while it is being analysed, and should be stored persistently for access later. An estimate of the storage required is as follows: The output of each burst can be stored in 1-4 bytes per channel. With 2650 channels per hybrid, and 28 hybrids per stave, about 72 kBytes per barrel stave-side can be expected - the largest object.

A calibration sequence will be made up of many hundreds of these bursts. It is not decided if this data will be stored in a verbose (raw) format or condensed (results of fits) mode.

16.8.4 Bandwidth

The ABCStar has a 128-level buffer that serves both as storage for L0-accepted data, and as a derandomising buffer for read-out, detailed in Section 6.2.1. Congestion on a read-out link will increase read-out latency and increase the risk that the L0-buffer over-flows, resulting in data-loss. It follows that latency and bandwidth are closely linked, and the likelihood of data loss due to buffer overflow is a good indicator of insufficient bandwidth. Latency is dealt with in the following subsection (16.8.5).

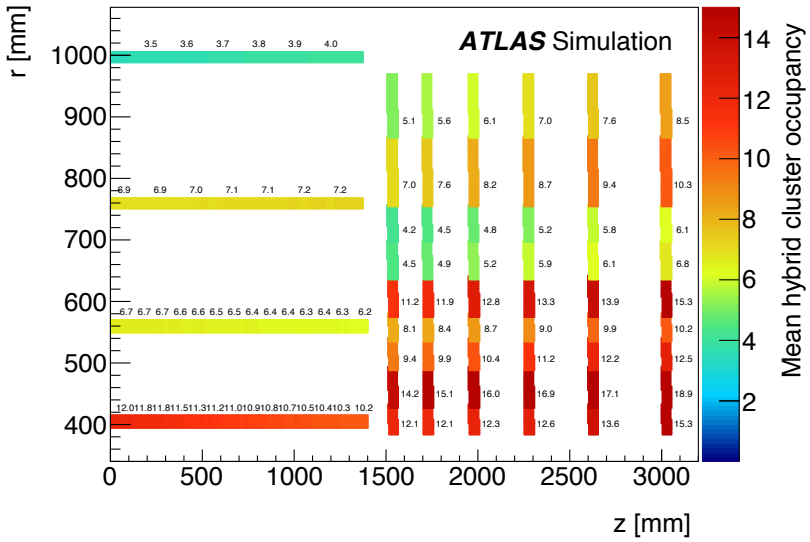


Figure 16.4: Map of average read-out clusters per hybrid per event, showing that the innermost barrel hybrid, and second-innermost disk-5 end-cap hybrid have the highest occupancies.

Each read-out cluster is encoded as a 4 bit chip address, 8 bit strip address and a 3 bit map of adjacent strips. That is 15 bits per read-out cluster. If a cluster is wider than 4 strips, it is split into multiple 4-strip read-out clusters. An HCCStar has between 6 and 11 ABCStar connected to it, depending on the location of the module on which it resides. In every event, it aggregates data from all ABCStar chips connected to it into a single variable length packet and sends it off-detector. This packet also has maximum 32 bits of meta-data included (type, L0-tag, BCID, error-flags etc.). The HCCStar packet format is still under development, but it is expected to be approximately 200 bits long. For example, a barrel hybrid has 10 ABCStar and, assuming a single read-out cluster per ABCStar, an HCCStar will aggregate 10x15 bits into an event packet. Adding the 32 bit meta-data, gives a total 182 bits per event per HCCStar.

Figure (16.4) shows the average number of read-out clusters per hybrid across the detector. These are used to calculate e-link utilisation (see Table 16.1). The plot shows that the highest bandwidth will be found in the end-caps disk-5 ring-0 outer-hybrid, and the inner barrel hybrid.

Each HCCStar is connected to an lpGBTx via a 640 Mbit/s e-link. When using 8b/10b encoding the effective available bandwidth is reduced by 20% to 512 Mbit/s. With start- and end-of-frame symbols (an additional 2-bytes per unencoded packet), and a possible 7 bits of padding to round up to an integer number of symbols, an additional 23 bits is needed per event before 8b/10b encoding. If 8b/10b encoding is not used approximately 3 bits of header and 16 bits of trailer will be added to ensure unambiguous packet detection. The start/end symbols and header/trailer are called framing bits here. The average number of read-out clusters per region (see Figure 16.4) at a 1 MHz event-read-out rate is used to calculate link utilisation. This is shown in Table 16.1 for various regions, and, with a maximum on 55%, none of which are near saturation.

Table 16.1: Average event size and e-link utilisation from the various regions of the detector for $\langle\mu\rangle$ = 200.

	HCC avg/evt		**% 640Mb e-link BW**	
Location	**Read-out-clusters**	**Data bits + meta**	**1Mevt/s + framing unenc.**	**8b/10b**
Barrel 0	11.10	167	29.1%	37.1%
Barrel 1	6.45	97	18.1%	23.4%
Barrel 2	7.15	107	19.7%	25.4%
Barrel 3	3.75	56	11.7%	15.4%
Disk 0	12.63	190	32.7%	41.6%
Disk 1	13.33	200	34.2%	43.6%
Disk 2	14.08	211	35.9%	45.7%
Disk 3	14.97	225	38.1%	48.4%
Disk 4	15.93	239	40.3%	51.2%
Disk 5	17.33	260	43.6%	55.3%

Table 16.2 shows the breakdown of data volumes for the various regions of the detector (HCCStar and ABCStar numbers are from Table 5.1). The volumes are without framing bits added, but with all meta-data included. At a 1 MHz event-read-out rate, it is expected the ITk Strip Detector will generate 465 GBytes of data per second at $\langle\mu\rangle$ = 200.

Table 16.2: Average total event size for $\langle\mu\rangle$ = 200.

Location	# HCC	# ABC	Avg ABC/HCC	Bits/evt/HCC	Total bytes/evt
Barrel 0	3136	31360	10	167	65k
Barrel 1	4480	44800	10	97	54k
Barrel 2	3136	31360	10	107	41k
Barrel 3	4032	40320	10	56	28k
Disk 0	1664	12672	7.6	190	39k
Disk 1	1664	12672	7.6	200	41k
Disk 2	1664	12672	7.6	211	43k
Disk 3	1664	12672	7.6	225	46k
Disk 4	1664	12672	7.6	239	49k
Disk 5	1664	12672	7.6	260	54k
Total	**24768**	**223872**		**1752**	**465k**

16.8.5 Latency

Latencies have been calculated using a discrete event simulation[1)]. Randomised triggers select events generated by ATLAS simulation - in this case the extended barrel layout, with data from an official production. The flow of triggers and data through virtual ABCStar and HCCStar are modelled and latencies recorded. If the L1Track option is exercised, much lower latencies (2 μs as opposed to 10 μs) for regional data are needed (more details on L1Track are in Section 16.8.6).

Maximum ABCStar Data Storage Time

In the single level trigger architecture, the risk of data-loss is dominated by read-out congestion - if data cannot be read-out in time from the ABCStar event-data buffer, it will be over-written by new data. The same is true in the two-level architecture, but this is evaluated as the maximum interval between the L0A and L1A at the ABCStar. The most critical is at the maximum L0A rate (4 MHz) because the random, instantaneous, fluctuations in trigger rate are a proportionally larger problem - increasing the risk of event loss further. These numbers are shown in Figure 16.5.

Looking in more detail, after receiving an L0A the ABCStar moves data from the pipeline to a 128 position buffer. In the two-level architecture this data must be kept until the L1A arrives, in the single-level architecture an internal L1A is automatically generated for each

[1] An earlier but functionally equivalent version of the discrete event simulation for the ITk Strip Detector is described here: [149]

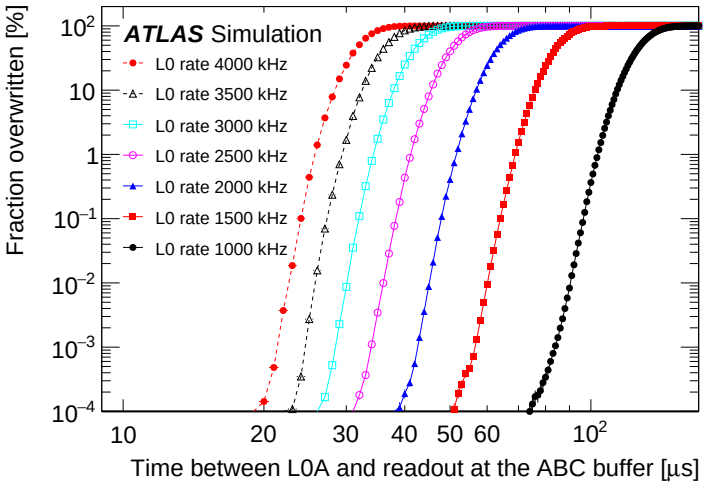


Figure 16.5: Effect of time between L0A and data read-out on buffer overwrites (event loss) in ABCStar.

L0A received. L1As are queued until read-out resources are available in both architectures.

Single-level Trigger Limits

In the single level architecture, the maximum L0A rate is limited by the bandwidth of the read-out links and buffer-depth in the ABCStar. Using the discrete event simulation, the time to transfer 99% of event data out of an HCCStar is evaluated. A rapid increase in the latency over a small increase in data rate indicates that the maximum trigger rate has been reached. Figure 16.6 shows this effect over a range of representative trigger rates. In all cases the highest occupancy hybrids in each layer are used (see Figure 16.4). It can be seen the the single level architecture is limited to a maximum trigger rate of about 1.2 MHz by the end-cap.

Two-level Architecture Limits

The two-level trigger architecture is limited in very much the same way as the single-level system: the L1A must arrive before data in the ABCStar buffers are over-written. In this case the L1A latency, at the ABCStar, must be lower than that at which data-loss occurs - as shown in Figure 16.5. These numbers are further constrained if there is read-out congestion (where part of the buffer is effectively used as a de-randomiser).

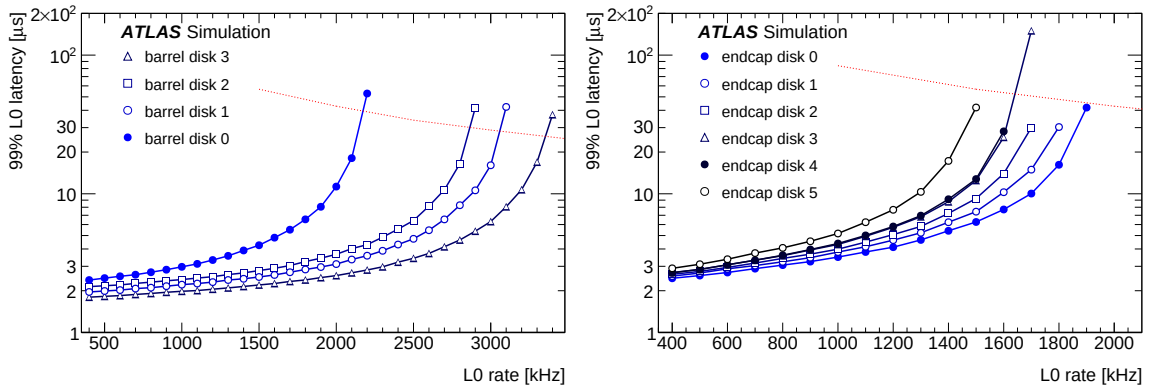


Figure 16.6: Read-out latencies for 99% of data in the single-level trigger architecture for various L0A (event read-out) rates. The red dotted line indicates the boundary above which buffer-overwrites occur (from Figure 16.5). (Note the y-axis is in log -scale.)

When L1Track is included in the system, the Regional Read-out Request (R3) signal is used to read-out up to 10% of the modules for each L0-triggered event. The data is sent via a low-latency path such that it can contribute to the L1-trigger decision. Figure 16.5 shows that the maximum period between an L0A and an L1A needed to prevent data loss is 20 μs. Considering that this time includes data-transfer, track-finding and other L1-Trigger operations, the target for data arrival at L1Track is 6 μs after an R3 is sent from the FELIX.

Both R3 and L1A signals share a control line to the front-end modules with asynchronous signalling. This allows R3 signals to be sent in preference to L1A signals that are queued. The same happens on the HCCStar, as well as for R3-data in the ABCStar where it has priority read-out over L1-data.

Given that the R3 targets each module only in 10% of L0A events and that the overall event read-out rate (R3 + L1A) of all modules is constrained to be 1 MHz, increasing the L0A rate means reducing accordingly the L1A rate. In Figure 16.7, that shows the effect on the 99% data read-out latency for a number of L0A rates, the L1A rate values corresponding to the given L0A values on the x-axis are shown alongside the L1A data points.

16.8.6 Track-Trigger Considerations

If the L1Track option is exercised, it mandates using the two-level trigger architecture with regional read-out. General details are provided in Section 16.7 above.

Integrating the L1A and R3 into the ITk Strip Detector system involves using the second control line to the HCCStar (called L1R3) on the stave/petal. As the physical connections already exist, the changes are only off-detector, in the FELIX and LTI firmware. The L1A is broadcast, from the L1-trigger, via the LTI, and FELIX, to the detector. It is an asynchronous

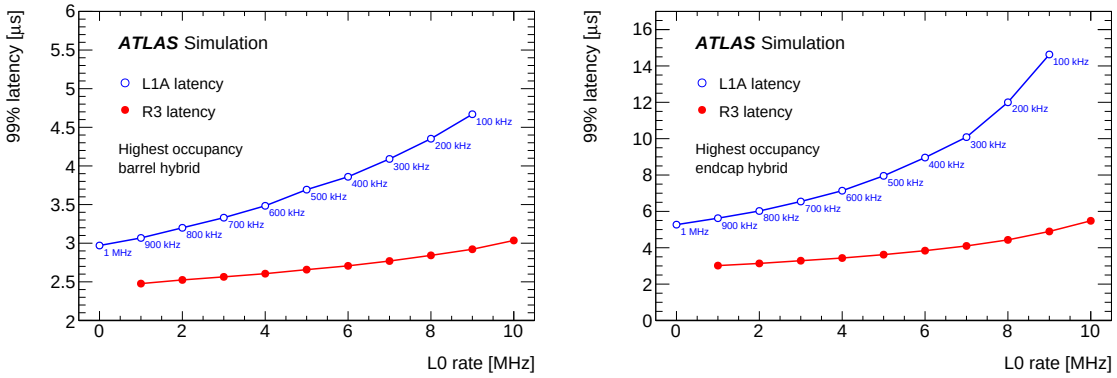


Figure 16.7: Read-out latencies of R3 data (red) and L1A data (blue) as a function of the L0A rate in the two-level trigger scheme, for the highest occupancy hybrid in the barrel (left) and end-cap (right).

signal and can be queued as needed. In particular it may need to be delayed while R3 signal sending is in progress on the FELIX.

The R3 signal makes use of RoI information in the regions that generates the L0A, and are sent to the LTI. Only a subset of the detector (less than 10% of a 465 kB event - see 16.8.4) is read out using the R3 for each corresponding L0A. An R3 signal is unique to its downlink, so a hierarchical decoding/translation scheme is needed and this is distributed across the LTI and FELIX.

The RoIs will be sent as a list accompanying each L0A to the LTI. The list will detail which regions of the detector need to send event-data for tracking. It is expected that each list will contain 5-15 RoIs, each encoded in 12 bits. This means an extra 180 bits need to be transmitted with each L0A.

In the LTI, the list entries are converted into a collection of downlink/module identifiers and transferred to the relevant FELIX. As this transfer will contain as many unique R3 commands as there are L1R3 e-links (4 per downlink) connected to the FELIX, a higher bandwidth connection between the LTI and FELIX may be required. One alternative to this scheme currently under consideration is that the conversion can be done in the FELIX.

In the FELIX, an R3 command pattern is generated and serialised, merged, encoded and sent to the front-end chips. The R3 targets only a subset of the modules connected to a given downlink for read-out. The front-end chipset will give priority to R3 initiated read-out over L1A read-out, allowing R3-data to be sent less than 2 μs after the corresponding R3 has been received. Data returned to the FELIX in response to an R3, will have a dedicated type field as part of its header, and can be routed to L1Track using this information alone. To ensure minimal delay, additional high-bandwidth links will be needed to transfer data from FELIX to L1Track, or the ratio of input to output link bandwidth will need to be changed, increasing the number FELIX in the system.

17 ITk Powering and Cables

This chapter will cover the powering of the ITk from power requirements, the supplies external to the detector as well as the cabling and fibres. The shielding and ground referencing strategy for the entire ITk will also be described. The expected pixel powering will be summarised briefly.

17.1 Power Dissipation in the ITk Strip Detector

The power in the front-end electronics of the ITk Strip Detector is a critical input to understanding the requirements of the cooling and environmental control of the tracking detector. The total power depends critically on understanding the power dissipated in the on-detector ASICs and power converters. As discussed in Chapter 6 the module development has been with the prototype ASIC ABC130. The digital and analogue currents are likely to change in the production chip ABCStar. In addition, it is understood that the digital current in the ABCStar and HCCStar, which are fabricated using the 130 nm Global Foundry process, will evolve with ionising radiation, increasing to a peak around 1 MRad total ionising dose and then decreasing back towards the initial value. The value of the digital current at the 1 MRad peak depends on the rate of ionising radiation and the chip temperature (see Chapter 6).

The efficiency of the on-detector DC-DC converters depends on the output current and temperature. In initial calculations the best estimates of the current expected in the front-end ASICs from the simulations of the production chip have been used. Additionally, a combination of estimates and simulations of the efficiency of the DC-DC converters have been used to calculate the power at operational temperatures. The power in the optical transmitters, which is designed in 65 nm technology, are not expected to change with ionising radiation and this expectation has been confirmed by measurements. In calculating the increase of digital current at different points (barrel layers or end-cap disks) in the detector due to ionising radiation an understanding of the rate of ionising radiation is required. This comes from a combination of the model of the evolution of HL-LHC provided and simulations of the Total Ionising Dose (TID) at different points in the detector. Measurements of the increase ABCStar and HCCStar digital current at representative rates of ionising radiation and temperatures have been used to predict the increase at all points in the detector (see Chapter 6). The predictions are made for an operation model in which the detector is cooled down from the beginning of operation. An option remains to run the detector

warmer during the first few years and this would mitigate the increase in digital current due to ionising radiation.

In Table 17.1 the power dissipated in the front end electronics in modules at different points in the detector without damaging the sensors is presented. The values are calculated for: short-strip modules (SS), long-strip modules (LS) in the barrel and end-cap modules from Ring 0 to Ring 5 (R0-R5). The dissipated power is shown for no ionising radiation (at the time of installation) and at the peak of the increase of digital current. It should be stressed that not all modules will reach the peak of digital current at the same time.

Table 17.1: Front-end power for the different module types without and with TID induced current increase.

Power [W]	**SS**	**LS**	**R0**	**R1**	**R2**	**R3**	**R4**	**R5**
No TID	4.72	2.42	4.17	4.94	3.22	7.10	3.98	4.36
TID	5.64	2.88	4.99	5.89	3.87	8.53	4.76	5.21

In Table 17.2 the total value of front-end power from the front end electronics is presented. The value for the barrel and end-cap is conservative as it is assumed that the modules in those regions reach the peak of digital current at the same time, which will not be the case due to the different radiation levels at different radii and z-position.

Table 17.2: Total value of power from the front end electronics for the two cases, with and without the TID induced current increase.

	Without TID [W]	**With TID [W]**
Barrel	36769.9	43542.7
End-caps	22413.3	26624.4
Total	59183.2	70167.1

The sensor current and thus power is also depending on the fluence (see Chapter 6). However, at the time of the peak in power consumption due to the Total Ionising Dose the sensor power is comparable small, and will never increase above the maximum power at the peak. In order to have a conservative estimate for the power, 10% of the total front-end power are added for the sensor power and another 10% for the loss in cables, resulting of a conservative overall estimate of the power dissipation by the ITk Strip Detector of 84 kW.

The sensor current and thus power also depend on the fluence (see Chapter 6). However, the peak in the front-end power due to the increase in digital current caused by the ionising radiation occurs within a few years of the start of operation at a time when the sensor power is still close to its minimum. The peak in sensor power occurs, at the end-of-life, when the effects of ionising radiation on the front-end digital current have decreased and are close to zero. To obtain an estimate of the total on-detector power to set the requirements for the cooling system following factors are added:

- the power in the front-end electronics without any effects of radiation plus the end-of-life sensor power and a conservative estimate for the power dissipated in the on-detector cables,
- an additional safety factor of 10% of the total front-end-power.

This results in a total on-strip-detector power of 84 kW.

17.2 Overview of Powering the ITk Strip Detector

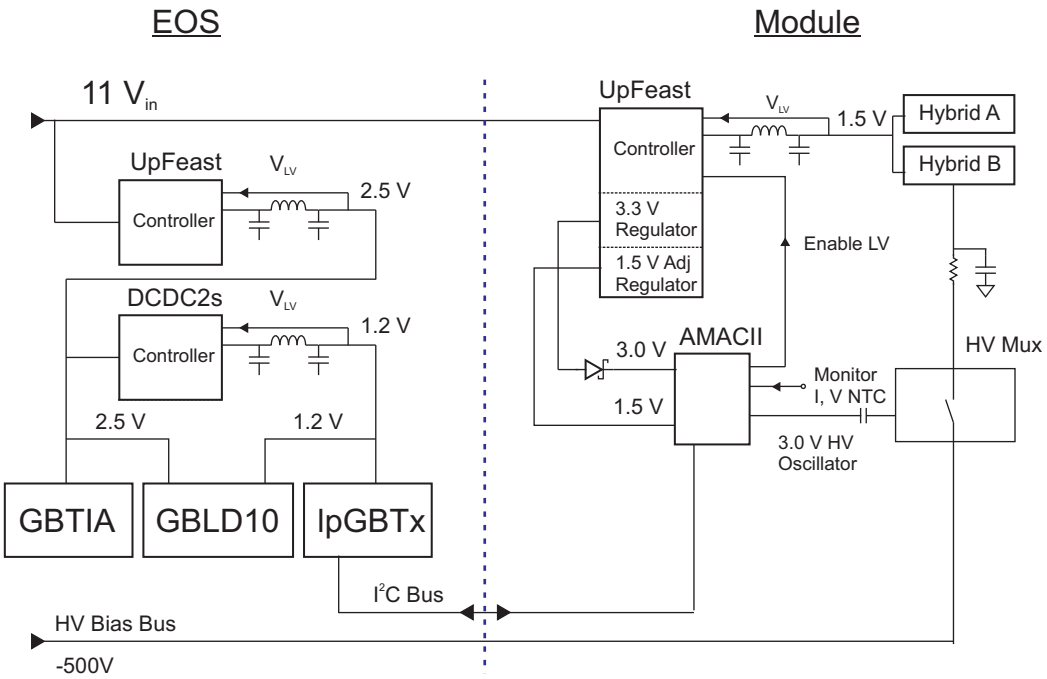


Figure 17.1: Overview of the powering for the ITk Strip Detector on the end-of substructure side (EoS) and the module side.

As discussed in Chapter 5, the basic unit of the ITk Strip Detector is a module. Multiple modules are mounted on barrel staves and end-cap petals. Power for the modules is conditioned by power boards mounted on the surface of the silicon sensors. The EoS cards, described in Section 12.1 for each stave and petal, also have a power board for their power requirements. Power is distributed to each module along the staves and petals, as well as to the EoS cards, by a bus tape discussed in Chapter 9. Power to the staves and petals is provided by power supplies external to the ITk itself through a cable plant. The read-out, control and data transmission circuitry require low voltages in the range of 1.2 V to 3 V while the sensors require a bias voltage in the range of 100 V to a maximum of 700 V increasing as the sensors are exposed to increasing amounts of radiation. In order to minimise

power loss in the cables, low voltage power is supplied to the staves and petals at 11 V and then stepped down to the required voltages by the power boards. The high voltage for the silicon sensors is provided at the desired voltage directly to the staves and petals since the current drawn on those lines is small enough to make the voltage drop insignificant.

From the standpoint of the externally supplied power, the modular unit is one side of a barrel stave and one side of an end-cap petal. Each of these units contains one bus tape. There is one low voltage (LV) power supply channel for each of these bus tapes and four high voltage (HV) power supply channels per bus tape. Since the low voltage output of the power board for each module can be shut off should a problem on that module develop, it is acceptable to provide one LV power bus for the entire bus tape. As discussed in Chapter 6 high voltage switches are being investigated for the power board, which will allow the bias voltage for each sensor to be likewise shut off. However, the qualification of these HV switches will not be completed until the middle of 2017 at the earliest and therefore their reliability has not yet been assured as they involve new technologies. For this reason, four HV channels are currently envisioned for each bus tape in order to partition the modules on a stave or petal into smaller groups such that a smaller group than a whole stave or petal can be turned off should a problem occur on one and the HV switches are not qualified in time for the start of construction. Referring to the numbers in Table 17.3, there are 392 staves and 384 petals. With a bus tape on both sides of these staves and petals, there are a total of 1552 bus tapes for both the barrels and end-cap. This then requires 1552 LV channels and 6208 HV channels.

In the interests of minimising the cost, the existing ATLAS Inner Detector (ID) cable plant will be reused as much as possible. Figure 17.2 gives a rough overview of the planned cable plant for the ITk Strip Detector as a cross section of the collider and service caverns viewed from above. With power supplies located in service caverns USA15 and US15, ATLAS-SCT Type IV cables are used to reach patch-panel 3 (PP3) now located in racks on either side of the ATLAS detector outside the Muon spectrometer. From there one option is to use ATLAS-SCT Type III cables which run through the Muon spectrometer area to places marked as PP2 (patch-panel 2) in the figure. Another option is to replace these cables with new ones as discussed further in Section 17.6. The existing TRT PP2s will be removed and replaced for this purpose. Additionally, new cables to run from PP2 to PP1 (patch-panel 1) located just outside the ITk outer enclosure will be purchased. It was decided not to use the existing cables from the PP2 region to PP1 because it is unsure what their condition will be after being irradiated for the full life of the present ATLAS ID. They will likely be activated and unsafe to handle for any extended period of time. PP1 is actually part of the Service Module assembly (labelled SM in Figure 17.2), which brings power cables, data fibres and cooling pipes to the barrel staves and the end-cap petals. The service module assembly is in detail described in Chapter 11.4.

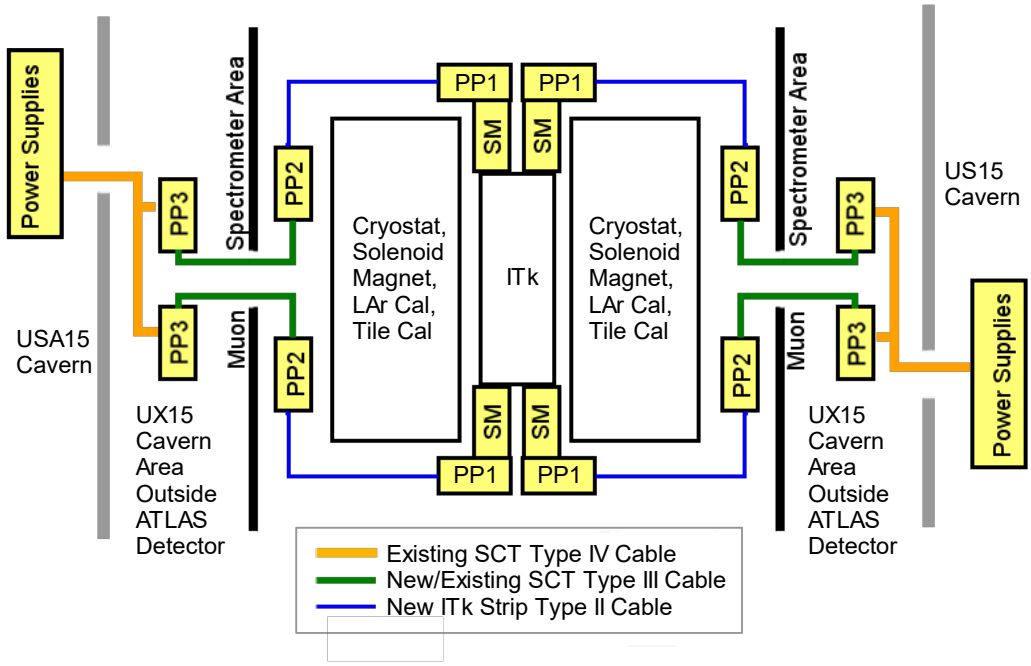


Figure 17.2: Overview of planned ITk Strip Detector cable plant. Patch-panels are labelled PP3, PP2, and PP1. SMs are the Service Modules that connect services from PP1 to the individual EoS cards for the Staves and Petals.

17.3 Overview of Powering the ITk Pixels

The details of powering and cabling for the ITk Pixels is not worked out as well as it has been for the ITk Strip Detector because many of the details of the Pixel layout are still under discussion and will be finalised in the forthcoming Pixel TDR. Chapter 15.4 describes the base line choice of a serial powering design to provide the low voltage for the on-detector ASICs. The constant current supplies required to power this serial power arrangement as well as the high voltage power supplies to provide bias voltage for the sensors will again be located in the service caverns, USA15 and US15, with a cable plant to deliver the power to the detector system.

The goal is to reuse as many of the existing ATLAS ID cables as possible. The present arrangement of pixel power cables is shown in Figure 17.3. LV cables now run from the two service caverns to patch-panel 2s (PP2s). A tabulation of how much LV power will be required for the full pixel system indicates that there is sufficient copper cross section to carry the necessary currents to the PP2s. It is not clear yet whether the modularity of these existing Type III cables matches the necessary modularity of the ITk Pixels. The required modularity should be achievable by possible rearrangement of cable connections at PP2. A new PP2 will be required. New power cables will be purchased to run from PP2 to PP1

because the condition of the existing cables is not known until the ID is extracted in preparation for ITk installation; too late to order cables. The present Type II cables, especially the connectors at PP1 are likely to be activated from their years of radiation exposure.

The present HV cables run continuously from their power supplies in the service caverns to the detector bypassing all the patch-panels. These cables will be cut at the PP2 areas, terminated with appropriate connectors to plug into a new PP2.

The other issue with the Pixel HV cables is that they were originally specified to operate up to 700 V, while ITk Pixels currently specify a bias voltage as high as 1200 V. Since the ITk requirements state that HV cables must be tested to twice their expected operating voltage, a sample of the Pixel HV cables will be tested up to 2400 V to determine if they can operate at the higher setting. A backup plan for this would be to use the TRT HV cables that are rated up to 3 kV.

The quantity and arrangement of cables, both LV and HV, from PP2 to PP1 will be determined once the details of the Pixel layout are finalised in the forthcoming Pixel TDR.

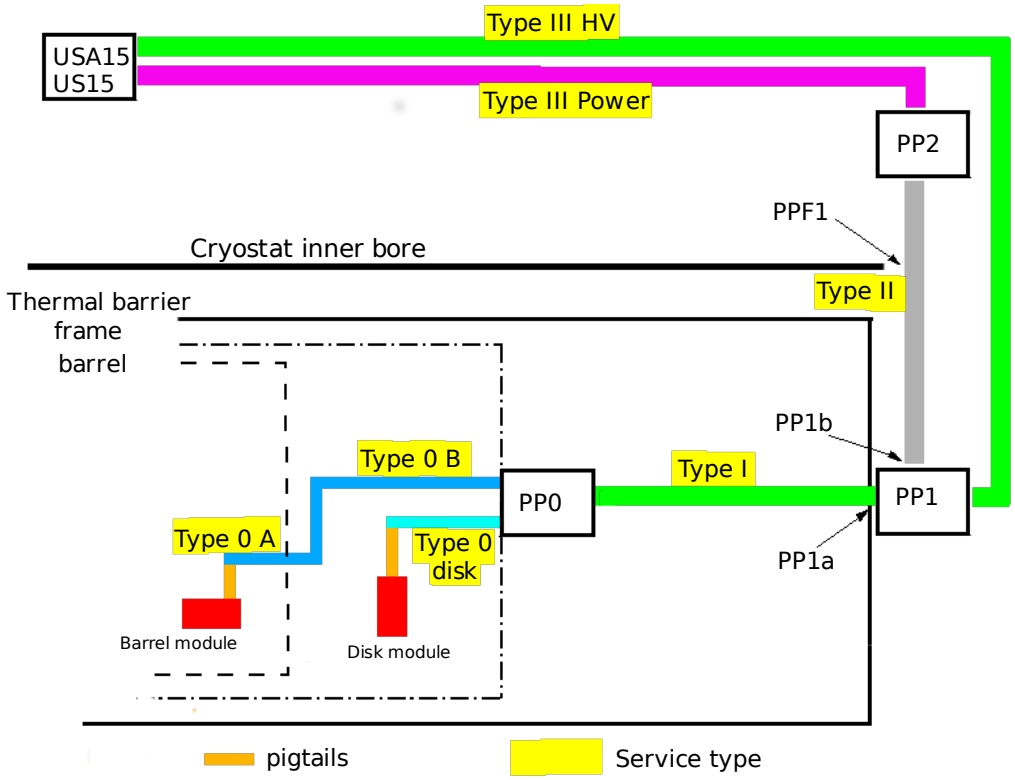


Figure 17.3: Overview of existing pixel cable plant. Patch-panels are labelled PP2, and PP1.

17.4 Power Requirements for the ITk Strip Detector

The power requirements for the read-out and control ASICs are discussed in Chapter 6 including the effects of radiation on the chip's leakage current. To determine the amount of current that must be supplied, the worst case scenario conditions are taken, namely at the radiation induced peak of chip required current and at the end-of-life bias leakage current for the sensors. Table 17.3 summarises the currents required for each bus tape. There are three rows in the table given the different amounts of current required for each type of stave or petal. The inner two barrels contain two read-out hybrids for each module, therefore, twice the number of ABCStar and HCCStar as the outer two barrels. The petals contain only nine modules but the number of ASICs per module varies given the varying trapezoidal sizes of the sensors. Therefore, the average numbers are quoted. The LV currents in the worst case column are estimated based upon the radiation tests and modelling discussed in Chapter 6 and the HV worst case currents are based upon post radiation tests of prototype sensors.

The numbers in Table 17.3 indicate a large amount of LV current to be supplied to each bus tape, especially for the inner barrel. This issue will be discussed further in the next two sections with some options for supplying the LV power. The HV currents are more manageable especially if they are divided by the four channels discussed in Section 17.2.

Table 17.3: Current requirements for the three types of bus tapes. Currents are stated at 11 V supply voltage. Worst case values for LV are at the peak of the radiation induced current bump. HV values are for end-of-life leakage currents at 700 V. * These are ranges for the end-cap modules with the minimum and the maximum currents.

Type of Bus Tape	$N_{Modules}$	$N_{ABCStar}$ on Module	$N_{HCCStar}$ on Module	PreRad per Module	PreRad per EoS	WC per Bus Tape
Inner Barrel LV Inner Barrel HV	14	20	2	480 mA	230 mA	8.2 A 28.0 mA
Outer Barrel LV Outer Barrel HV	14	10	1	240 mA	230 mA	4.1 A 9.3 mA
Petal LV Petal HV	9	8-21*	1-2*	390-610* mA	140 mA	3.6 A 10.0 mA

17.5 Power Supply Options

Given the large LV currents required, care must be taken in the design of the power system and some options can be considered for distributing the supply components. The HV power can be supplied directly from power supplies located in the two service caverns. The

options for delivering the LV power from power supplies located in service caverns to the End of Structure cards and detector modules for the staves and petals is closely connected with the arrangement and parameters of the cables, which was described in Section 17.4 and will be discussed in more detail in Section 17.6. There are several aspects to be taken into account, namely: power losses in the cables and overall efficiency of the powering system, amount of material, cost of additional new cables and safety of the DC-DC converters on the Staves and Petals. The ASICSs that drive these converters will be operated at a nominal input voltage in the range of 11 V to 10 V along the stave or petal bus tape while their maximum operating voltage is 12 V and their absolute maximum voltage specification is 14 V (see Chapter 6). Thus, if the power system operates with significant voltage drops in the cables, decreases in the supplied current could result in a large increase in the voltage applied at the detector DC-DC converters. While excursions beyond the 12 V limit of a very short time duration might be tolerated, the 14 V limit must never be exceeded. Three options are being considered:

- **Direct powering:** The power supplies in service caverns deliver power directly to power boards located on the staves and petals at the required voltage. With conservative assumptions regarding the maximum currents required and cable resistances, the voltage drop in the whole cable run can be as large as 4 V with a power supply voltage of 15 V. This will require the power supplies in the service caverns to provide voltage regulation according to remote sensing, which will have a slow response given the overall impedance of cables and needs for heavy filtering of the power lines and sensing lines. Stability of such a system has to be considered very carefully and will require close interactions with the vendor(s) of the power supplies. In addition a voltage limiter will be needed in order to prevent fast transient changes of the supply voltage at the staves and petals exceeding 14 V. The voltage limiter will have to operate using a sense line for activation and its reaction time will be determined also by the length of the cables between the limiter and the sensing node. Given the expected voltage drops along the bus tapes stated in Chapter 9, the sensing nodes can be placed at the EoS. Given the very limited space at patch-panel 1 (PP1) and the high radiation levels there, locating the voltage limiters at patch-panel PP2 will be preferable if the voltage drop between patch-panel PP2 and PP1 can be limited to less than 2 V.

- **Additional DC-DC converter in PP3:** The power supplies in service caverns provide an output voltage of 48 V and a DC-DC step down converter is placed in the PP3. The output voltage of this converter should cover the 11 V required for the power boards plus voltage drops in Type III cables, and Type II cables. This solution will result in reduction of power dissipation and voltage drops in the Type IV cables so that main power supplies could be operated without remote sensing. On the other hand regulation with remote sensing will have to be implemented in the DC-DC converter and taking a very conservative approach voltage limiters will be required, likely installed at PP2. Cooling will also have to be added to the PP3s. The radiation levels

and the magnetic field in the PP3 area (up to 900 Rad, 1.5×10^{11} n_{eq}, 96.4 mT) prohibit using standard commercial DC-DC converters. However, the radiation levels are low enough that a custom-developed radiation tolerant DC-DC converter using commercial components with some magnetic shielding may be feasible by employing a COTS (Commercial off the Shelf) design approach with proper selection and qualification procedures.

- **Additional DC-DC converter in PP2:** This option is similar to the second option but it places the DC-DC converters at PP2 instead of at PP3. It may allow to eliminate the voltage limiter, but cooling will have to be added to the PP2s. The requirements regarding radiation tolerance (up to 2.2 kRad and 2.8×10^{11} n_{eq}) will be in the same range as in the PP3. Magnetic field (0.55 T) is, however too high to consider magnetic shielding so that using air core coils will be required. This option will be investigated in parallel in order to understand whether it may be compatible with the space constraints of new PP2s.

All powering options then will include remote sensing to adjust the supply voltage according to the current being provided and maintain the voltage at the detector within the correct operating range. Programmed changes in the electrical load such as turning on or off modules on a stave or petal should be done so in steps, one at a time, so that the remote sensing has time to properly react. A voltage limiter or clamp will also be required to suppress unplanned current changes from exceeding the absolute maximum voltage of the on-detector DC-DC converters. Ideally the voltage limiter will be placed at PP2 provided that the voltage drop from PP2 to the EoS cards can be maintained at less than 2 V, allowing a safe margin between operating at 11 V and a 14 V absolute maximum. Otherwise, the limiter will need to be located at PP1 where space is extremely limited and radiation levels are high. In that location a radiation hard circuit would need to be designed and space provided for a high current limiter.

17.6 Cabling Options

An overview of the cabling plans is presented in section 17.2. An important issue that must be addressed by the cable plant is the large amount of low voltage (LV) current that must be supplied to each side of each stave or petal. The SCT Type IV and Type III cables can provide sufficient copper cross section to handle the full ITk Strip Detector LV currents provided that they are grouped in parallel. Two SCT cables will be assigned to each single-sided petal and to each single-sided stave for the outer two barrels with four cables assigned to each single-sided stave of the inner two barrels. The high voltage wires already contained in the SCT cables will be utilised for the ITk Sensor bias voltage and the new cables to be purchased will also include the necessary HV lines. Sense lines are also included in the SCT cables and will be included in new cables as well for the LV power to allow remote sensing by the powering system. Voltage drops on the HV lines will be small enough that

remote sensing will not be required. The grouping of conductors will be rearranged at PP2 to better match the stave/petal power distribution of the ITk as defined by the structure of PP1. See Figure 17.4 for an illustration of where the TRT PP2s are now located.

Table 17.4 summarises the cable types and the location of the patch-panels for the ITk strip tracker.

Table 17.4: ITk strip cables and patch-panels.

Cable type	**Start-finish**	**Maximum length (one way) (m)**	**Strategy**
Type-IV	USA15/US15-PP3	70	Re-use SCT Type-IV
Type-III	PP3-PP2	32	Re-use SCT Type-III or new cables
Type-II	PP2-PP1	15	New cables
Type-I (service module)	PP1-stave/petal	2.6	New cables
Patch-panel	**Location**		
PP3	ATLAS cavern, outside muon spectrometer		
PP2	Inside muon spectrometer, next to calorimeter feed-throughs		
PP1	Outside ITk outer enclosure		

The existing SCT Type IV cables running from USA15 and US15 to the PP3 racks outside of the ATLAS detector will be used without any modifications. The existing SCT Type III cables would also meet the needs of the ITk Strip Detector except that they are not quite long enough to reach the present location of the TRT PP2, where the new ITk Strip Detector PP2s will be located. Currently the SCT Type III cables are spliced to Type II cables, which then run all the way to SCT PP1 inside the cryostat bore. Cutting these cables at the splice and attaching a connector would not allow the cables to reach the new PP2s. Cutting the cables downstream of the splice and attaching the connector to the remaining piece of Type II cables has at least two issues. First, the existing Type II cables have a much smaller copper cross section than the Type III cables increasing the voltage drop to PP2. Secondly, the Type II cables are more difficult to work with, because of the type of insulation that was used. It has been decided that it will be problematic to successfully attach new connectors onto these Type II cable ends. The Type III/II cables will be cut at the splice with the Type III parts pulled back to the PP3 racks and the Type II parts pulled out towards the cryostat face and discarded. Two options beyond that are being pursued. One option is to replace the Type III cables with ones that are long enough to reach the new PP2s. The second, less favoured option, is to splice an extension onto the Type III cables with a piece of identical cable in order to reach PP2. In both cases, the cables will be rerun through the same passageway to span the distance from PP3 to PP2. The first option will be adopted unless it is much more costly than the second option.

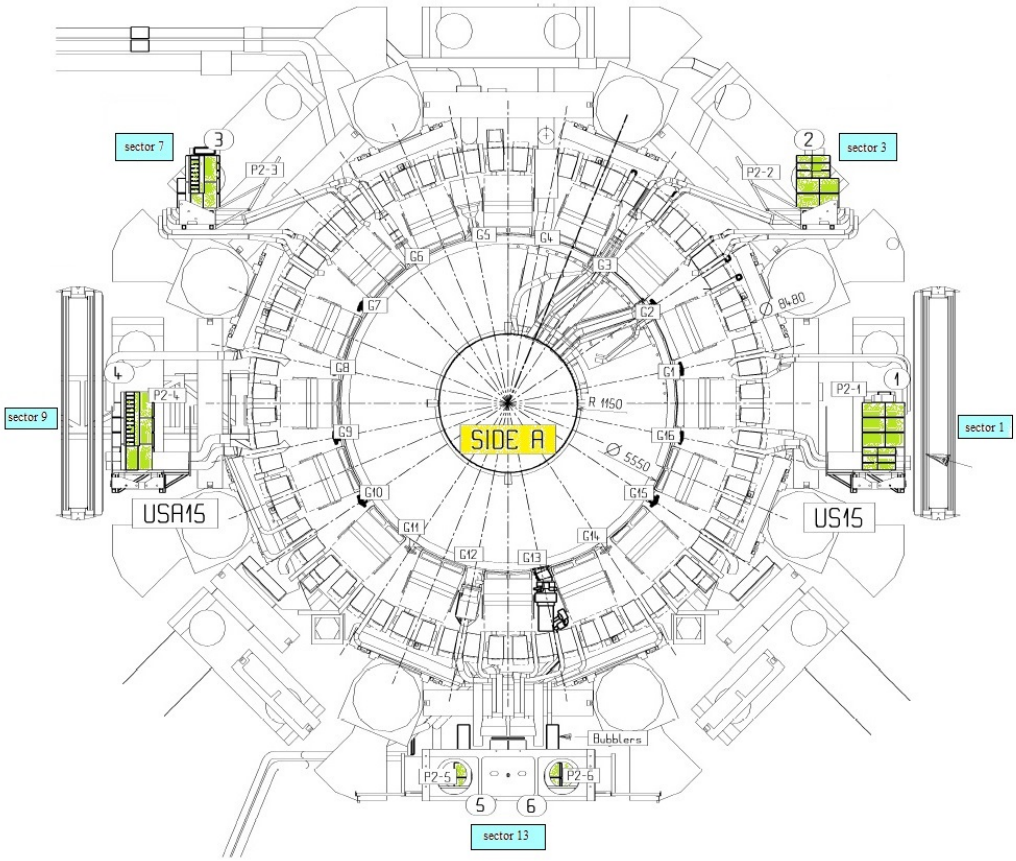


Figure 17.4: An end view of the barrel part of the present ATLAS detector. The green boxes in sectors 1, 3, 7, 9 and 13 are the locations of the present TRT PP2s.

As stated already, new cables will be purchased for the run from PP2 to PP1. The plan is that these cables will have the same copper cross section for the low and high voltage lines as the existing SCT Type III cables, that is larger than the existing SCT Type II cables. This again is to minimise the voltage drop. Even though the copper cross section to carry the LV currents will be larger than the existing Type II cables, the total cross section of each cable will not be equal to the existing Type III cables because the existing cables also contain several sense wires that are not needed for ITk Strip Detector. The last piece of the cable plant is the service module connecting the various PP1s to EoS cards at the end of staves and petals. The details of the service module wiring are covered in Chapter 11.4. The service modules include other services in addition to wiring for power and constraints of space and wire flexibility must be satisfied. The voltage drops of all components, Type IV, Type III, and Type II cables plus service module wiring must be included in the analysis of the voltage drops and possible voltage excursions at the EoS point of connection. As discussed in Section 17.5, three options for supplying low voltage power are being considered. Given the parameters of the cable sections discussed above, estimates of the voltage drops through

the cable plant are summarised in Table 17.5 for the direct powering option. While cable lengths vary depending upon the exact positions of PP3 and PP2 for each run, the maximum length for each cable segment has been used for these estimates. The three options are still being analysed to find the optimum solution, but a final solution will also wait until questions about the allowable size to the Type II conductors and the service module wiring are finalised.

Using the values in Table 17.5, the drop from PP2 to EoS of less than 2 V fits within the 11 V supplied to the EoS of each stave and petal and the 14 V absolute maximum rating for the UpFEAST ASICs used in the DC-DC converters on the staves and petals. This will allow for a voltage clamp to be placed at PP2 to assure that the UpFEAST ASICs are safe against sudden overvoltage excursions. The radiation levels at PP2 are much lower than those at PP1 making such active circuitry easier to design and commercial parts can likely be used as long as the accepted procedures for COTS designs are followed.

The SCT cables also include wires capable of carrying high voltage (HV) to provide a bias potential for the silicon sensors. The HV wires in the SCT cables were specified to operate up to a voltage of 500 V. While 500 V is the planned maximum operating voltage, the ITk Strip Detector would like to keep open the possibility of increasing the bias voltage up to 700 V near the end-of-life point for sensors. The procurement documents for the SCT cables specify that the HV wire to its return line were tested up to 1500 V and the HV line and its return were tested to the shield and to the other conductors to 1000 V. ITk requirements state that HV cables must be tested to twice their expected operating voltage and thus several spare SCT cables will be tested from 1000 V to 1500 V in 100 V steps. Given how the cables were tested by the vendor, it is possible to increase the operating rating of the cables from 500 V to 750 V. This will allow operation of the sensors up to 700 V with a 50 V margin for voltage lost in the local bias filters that are included in the power board for each module. Ten spare SCT Type IV cables have been tested up to 1500 V with no failures and the operating rating of their HV wires was increased up to 750 V. A similar number of Type III cables will be tested up to 1500 V. In case they do not pass, new cables rated to 750 V will be purchased.

There is one more adaptation of the SCT cables. As mentioned above in Section 17.2, there are four HV channels per bus tape. The two SCT cables allocated for each petal and outer barrel bus tape contain two wires designated for high voltage, a high voltage line and a high voltage return line. Both are rated for carrying the specified high voltage. To provide the desired four HV channels, both of the HV wires are to be used to carry high voltage and two wires now allocated for powering the SCT optical components, a low voltage, are to be used for the two high voltage return lines in each cable. Since the HV-Return lines are tied to the LV-return line and ultimately to ground at the detector, these HV-Return lines will operate at only a few volts above ground, that small voltage caused by the return currents they carry. We have also simulated the extraordinary circumstances of a beam loss where the sensor back plane starts to short to the sensor strips and the HV-Return lines only rise less than 10 V above ground. Therefore, we believe this is a safe adaptation

of the SCT cables. The only other potential downside to this adaptation is that the HV line and its HV-Return line will no longer be twisted with each other thus removing some immunity to noise pickup on the cable. Since this adaptation will only apply to Type IV and possibly Type III cables, common mode chokes will be included in the PP2 design and this will remove any pickup that should occur on these untwisted pairs. Any newly purchased cables will provide dedicated HV and HV-Return lines twisted together.

To summarise, the existing SCT Type IV cables are to be used for both LV and HV power from the service caverns USA15 and US15 to the PP3s. The existing SCT Type III cables may be replaced with longer ones or may be reused by splicing a few meters of the same type cable onto its end in order to span the distance from PP3 to PP2, these PP2s also being new to replace TRT PP2s. New cables are to be purchased to carry the LV and HV power from PP2 to PP1 where service module wiring connect to the EoS cards. The optimum powering scheme still needs to be chosen from the three options being evaluated but a voltage clamp is needed, likely located at PP2, to guarantee that the voltages at the EoS never exceed 14 V.

Table 17.5: Voltage drop estimates of the four sections of the cable plant assuming the first direct powering option in the service caverns US(A)15.

	US(A)15 to PP3 Type IV Cables Cables	**PP3 to PP2 Type III Cables**	**PP2 to PP1 Type II Cables**	**PP1 to EoS (Through Service Module)**
Max Length	70 m	32 m	15 m	2.6 m
Voltage Drops for Inner Barrels	0.62 V	1.1 V	0.54 V	0.31 V
Voltage Drops for Outer Barrels	0.62 V	1.1 V	0.54 V	0.31 V
Voltage Drops for End-Caps	0.55 V	1.0 V	0.47 V	0.28 V

17.7 Grounding and Shielding across ITk and its Interconnection to ATLAS

The ITk grounding and shielding (G&S) is the entire array of connected conductive elements of the ITk that attenuates electromagnetic interference (EMI) that interferes with the physics signal reception and the amplified signal data path. The equipment in the G&S system includes the service crates and modules in the service caverns, all of the metal conductor cables and shields that connect electrically with the ITk, and the detectors and data transceivers themselves. Optical fibres having no electrical conductivity, are not part of the G&S system. The discussion on the G&S scheme is based on the successful scheme used in the current ATLAS SCT detector.

The primary strategy for EMI attenuation is the full enclosure of the ITk system in a Faraday

cage. The cage constitutes both the shield and the 0-volt reference for the entire ITk system.

The purpose of the shield is to reduce the propagation of electromagnetic fields from the outside to the inside of the system, so that EMI contribution to electronics noise is negligible. Shielding is achieved using high conductivity materials. For ITk, the shield is mainly constructed from aluminium foils and plates. This shield reduces the electromagnetic field through reflection and absorption of the incident waves, and by reducing capacitive coupling between sensitive internal conductors and external EMI sources. The shielding power is frequency dependent and for a given conductor is a function of its thickness. For ITk the minimum required thickness for copper shield is 18 μm, for aluminium 25 μm, and for carbon-fibre plates 5 mm.

The ITk detector exists in an intense external static magnetic field, which is minimally distorted by the low permeability materials used. The shield material and thickness is chosen to leave the static magnetic field undisturbed. The shield EMI attenuation effectiveness is dominated by the necessary seams, joints, and connectors that build up the shield system. Therefore, the mechanical design and assembly of the system demands detailed attention, so that joining metal plates, foil or carbon-fibre is continuous leaving only small gaps or holes. All shield joints must have an inductance comparable to or lower than the shield inductance.

Non-conductive services entering the Faraday cage do so using a hole array with minimum apertures rather than a larger hole, or using a field attenuation collar as appropriate. Every service cable conductor entering the cage has an RF filter which bonds to the cage wall at the entry point. Service cooling tubes have an electrical insulator outside the cage wall as close as is practical. Electrical service cables are fully shielded external to the Faraday cage, and their shields have connector designs that RF bond the shield to the cage with a 360deg connection.

Because of external cable shield connections on opposite faces of the Faraday cage, externally induced EMI currents flow on and inside the Faraday cage. An ITk module or module array will DC bond to the cage wall only using the module service cable path. These independent, single paths avoid EMI pickup caused by common impedance coupling.

EMI currents will tend to flow through adjacent modules that reference to different areas of the cage. These ground loop currents will be reduced through collaborative design of the service structures, using the conductive materials of the services themselves. Minimal additional material will be needed for EMI attenuation optimisation.

The power supplies located at PP2, PP3, or the service caverns are part of the ITk grounding and shielding system. The ITk shield skin extends up to them, so each individual power cable is fully bonded to the power supply shield enclosure. Starting from the service cavern, the service cable shields are continuous and fully bonded on both sides of intervening cabinets all the way to the Faraday cage wall. The service cables and cabinets have no

earth ties: they are locally floating. The Faraday cage has a single bond to Atlas ground, line voltage earth. The shield conductors are designed so that an accidental line voltage conductor fault will reliably trip the line circuit breaker. For this safety purpose, the shield is tied to earth at a single low impedance point. No additional earth ties are necessary or useful.

In order to decrease capacitive coupling, electrostatic discharge events, and EMI antennae structures, all conductive pieces within ITk have a reliably designed bonding path to the Faraday cage. If a significant conductor is located close to a module, its tie to the cage should be made close to the detector module cage tie so as to minimise stray currents induced on the module.

The G&S design will address cable EMI emissions on data transmission within the cage. The Strip detectors may be susceptible to the Pixel data cables and thus the emission from the pixel cables will be measured to optimise the design.

ITk power supplies are mostly switch-mode type. The outputs are floating locally, with the referencing potential being the ITk Faraday cage wall. For each detector module or module array, the inside-cage tie to the cage wall carries no DC current, so the detector array end-of-substructure tie points be at the cage wall potential. The power supply design will be tested for EMI emissions from the service cable, which implies that supply outputs will probably need common-mode chokes.

If foil alone is used for a service cable shield, the foil should be wrapped so that the foil seam is parallel to the cable run. 25 μm Aluminium foil thickness will provide sufficient shield performance for this type of construction. If spiral-wrapped foil construction is used, then supplementary techniques such as braid may be needed to achieve equivalent shielding performance to longitudinal seam shielding. Service cables that bond to the cage will be tested for transfer impedance characteristic from 50 kHz to 500 MHz frequency.

17.8 Fibre Cables

The fibre cables will run from patch-panel PP1 at the end of the service modules to the counting room. A short length of custom radiation-hard fibre spliced to a radiation-tolerant commercially available fibre will be used (see Chapter 12.3). There are several options for the fibre cable itself. The fibre cables installed for the current generation of LHC experiments are based on multiple ribbons within one cable. For example the SCT fibre cables have either 6 or 8 12-way ribbons inside a cable. The radiation hardness of the cable itself has been validated, so this type of cable would be an option for the ITk. However, newer multi-fibre cables are now commercially available which achieve a higher fibre density than the multiple ribbon cables. There are cables based on fibres in loose tubes and with several of these tubes inside one cable. A schematic picture of one such fibre cable is shown in fig. 17.5.

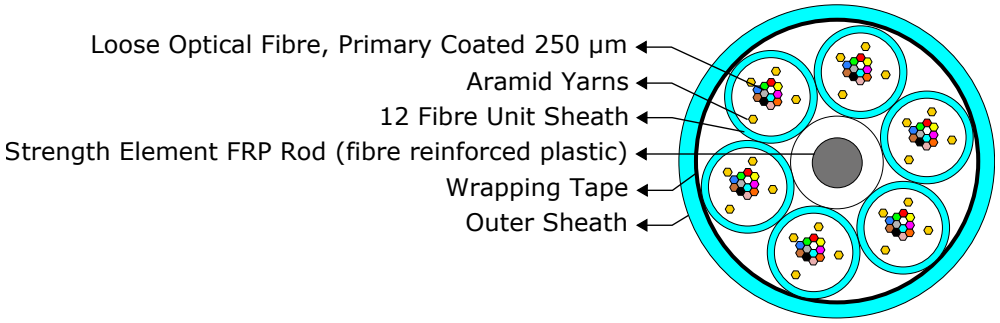


Figure 17.5: Schematic of a fibre cable with 6 loose tubes each containing 12 fibres.

The ends of the fibres will be terminated to MT/MPO connectors. These new cable types are attractive because they can achieve a higher fibre density and have smaller minimum bend radii than the multi-ribbon fibre cables. As these cables are symmetric, the minimum bend radius is identical for both directions unlike the multi-ribbon fibre cables, which would make cable routing much easier. Fibre cables are being investigated in the context of the VL+ project by CERN. They will perform a market survey, and test radiation hardness.

18 Common ITk Mechanics

The overall mechanical design of the ITk is driven by the aspiration to minimise the time needed for assembly and integration of the tracker, and in particular for the installation and service connections in the underground area. In the latter case, this is to satisfy the overall schedule constraints for ATLAS within long shutdown LS3, to thoroughly test the services, and to minimise exposure of personnel to activated material in the experiment. The ITk will therefore be fully integrated and tested on the surface before it is lowered down into the underground area and inserted into ATLAS.

Throughout the project, modularity of all components in the ITk is one of the main goals. A modular design is a hierarchical assembly made up of well-contained sub-assemblies with simple interfaces to other parts of the project. Sub-assemblies will be thoroughly tested before integration into the next hierarchical layer, so that each integration step is simple and the risks to the integration process are small. Production and testing of sub-assemblies can be parallelised and distributed. Where assemblies are needed in large numbers, they are designed to be identical as much as possible. This allows for interchange and a reduced number of spares, and further improves schedule robustness and reliability.

The ITk is contained by the outer cylinder (OC – see Section 18.2) during the surface integration, the transport from the surface integration site to the experiment, and in the final location within ATLAS. At its ends, this cylinder is closed by structural elements maintaining the hoop stiffness. These are the structural bulkheads (SBs – see Section 18.2, and thermal, humidity and electrical barriers (see Section 18.3), which are penetrated by the tracker service patch-panels 1 (PP1s). The PP1s also provide the necessary seals to maintain the integrity of the barriers for all service penetrations. All strip services will terminate in a connector of some sort at this location to provide a clear envelope for the tracker during transport and allow a fast connection of the tracker to the type II services.

The main function of the mechanical structures within the ITk is to support and place the detector modules. The positioning requirements for the ITk have been documented in Ref. [150]. They are based on the observation that for the current ATLAS detector, track-based software alignment is used to locate the sensor elements with the required precision, needing no support from a hardware alignment system and little reliance on build precision and survey data. A similar strategy will be adopted for the alignment of the ITk.

For track-based alignment to work, only moderate placement accuracies are required, mostly to maintain hermeticity and clearances (typically in the order of 100 μm). However, the key requirement is stability of the positions of the detector sensors over periods where data for

a software alignment cycle are collected. Table 18.1 lists the stability requirements relevant for the strip system, with their timescales and typical loads. Similar performance has been achieved in the current ATLAS ID.

Table 18.1: Stability requirements for the ITk in $r\phi$ and expected loads. Stability requirements in the other directions are 10 times higher [150].

Timescale	**RMS stability [μm]**	**Comment**	**Load**	**Load level**
Short ($\sim$ 1 day)	2		External vibrations	$< 10^{-7} g_N^2/\text{Hz}$
			Front-end power variations	$< 5\%$
			Temperature variations	$\pm 1^\circ$C
Medium ($\sim$ 1 month)	5	Always within sub-systems,	Mechanical shocks (magnet ramps, cooling system stops etc.)	
		on a global scale only between seismic events	Temperature variations	$\pm 2^\circ$C
Long (several months to years)	As assembly placement accuracy			

18.1 Support Hierarchy of the ITk

The support hierarchy of the detectors within the outer cylinder (OC) intentionally follows the assembly sequence of the ITk on the surface (SR1) and in the ATLAS cavern. This sequence is like the one which has been used for the currently installed Inner Detector, but with the outer cylinder acting as the inner warm vessel (IWV) on the surface. As before, the strip barrel is installed first, followed by the forward extensions of the PST (Pixel Support Tube) cantilevered on each side of the strip barrel, and concluding with the Strip Detector end-cap insertions. The Strip Detector end-caps are tightly integrated with the structural bulkheads (SBs), so the SBs will be installed simultaneously with the strip end-caps. The PST forward sections are then supported by the SBs. The insertion of Pixel Layers 2-4 and Layer 1 will not be covered in detail here, just an attribution of where along Z the Pixel subsystem will be supported within the PST.

Before the installation of the ITk the complete removal of the current ID and all of the type II services from the calorimeter end-faces to the calorimeter boxes is foreseen. It is assumed that the ITk and its services will satisfy the same envelopes as the current system. To guarantee compliance of the ITk designs with the external envelopes and to achieve internal consistency, an envelope model of the ITk is maintained [151].

The outer extent of the envelope model is the inner warm vessel of the barrel calorimeter. Inside of that is a 3 cm layer of polymoderator (described in Section 18.3.1). This is directly supported by the IWV. Inside the outer cylinder, in the barrel region of the cylinder, is

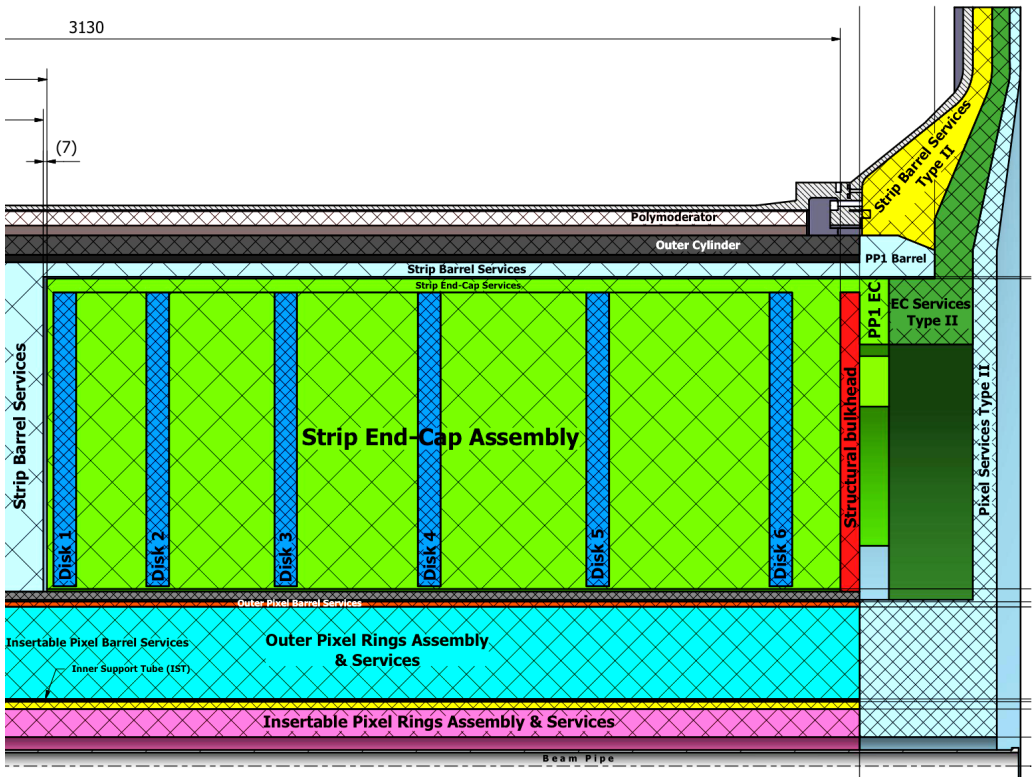


Figure 18.1: Envelope model of the ITk Detector. Only one quadrant of the detector is shown.

another 3-4 cm of polymoderator, supported by the outer cylinder. The outer cylinder itself is supported by several rollers riding on rails within the cryostat. These rollers are aligned with the structural planes at either end of the strip barrel, and in the plane of the structural bulkhead - there are four rollers per side. One side will have a "V" and the other a flat surface, i.e. the V-rail will constrain in X/Y, and the flat rail only in Y. The outer cylinder will be constrained in Z by the rollers on the C-Side at the end of the rail. This is over-constrained in Y and moderately in X on the V-rail. This is intentional to benefit from the stiffness of the IWV, as well as to reduce the stability requirements on the outer cylinder by placing the supports in the planes where the loads are transferred to the carbon-fibre shell. It is worth noting that the expected gravitational sag of the outer cylinder is larger than the surveyed straightness of the currently installed rails.

It is assumed that the rollers can be placed with similar precision on the outer cylinder. The expected gravitational sag between rollers is in excess of 1 mm, so it is assured that all rollers will be in contact with the rails. This can be verified during load tests of the as-delivered outer cylinder in the assembly cradle with mock-rails, and perhaps adjusted after new rails are installed.

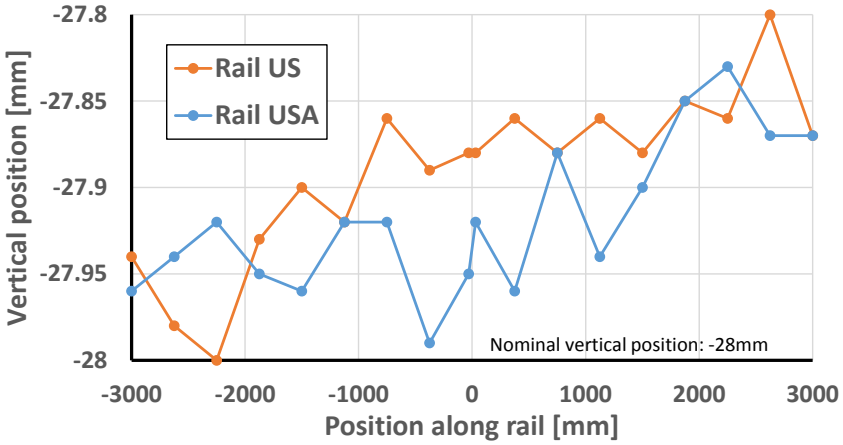


Figure 18.2: Survey data from the current IWV rails for the US and USA sides compared to nominal.

The rollers are in-line with the interlinks of the strip barrel, which span radially all the way to the Pixel system. The Strip end-cap supports are a short distance away in z, as shown in Figure 18.3.

The Pixel subsystem will be supported near the same plane as the barrel interlinks. The PST is shown here as a separate structure for clarity. The PST in the barrel region is the first shell for the strip barrel staves. In the forward region of the end-cap, it does not interface at all with the end-cap radially. The bulkhead moves with the end-cap due to many service penetrations which are designed to be flexible. The bulkhead connects radially and axially to the OC and the PST. The strip end-cap is solely supported by rails inside the outer cylinder.

The Pixel subsystem has some uncertainty in its layout. A layout with maximum active area was used to estimate the likely mass loads that the various support planes would be required to carry. In Figure 18.4, the forward patch-panel 0 (FPP0) is carried by the barrel interlinks, where $F_{EndPlate}$ and F_{PP1} are carried by the structural bulkhead. $F_{EndPlate}$ gets transmitted to the SB via the PST extension. All loads in are in kg force and sum to 205 kgf/side. The different load cases are based on whether the detector consists of cantilevered halves (unlikely) or is has a simply supported barrel region ("standard trainstructure"). The total mass of the installed detector is 400 kg.

18.2 Outer Cylinder and Structural Bulkheads

The outer cylinder is a thin-wall cylindrical structure. Its length is about 7 m while the diameter is 2 m. This gives a ratio L/D of 3.5, which is substantially less than the 8 required

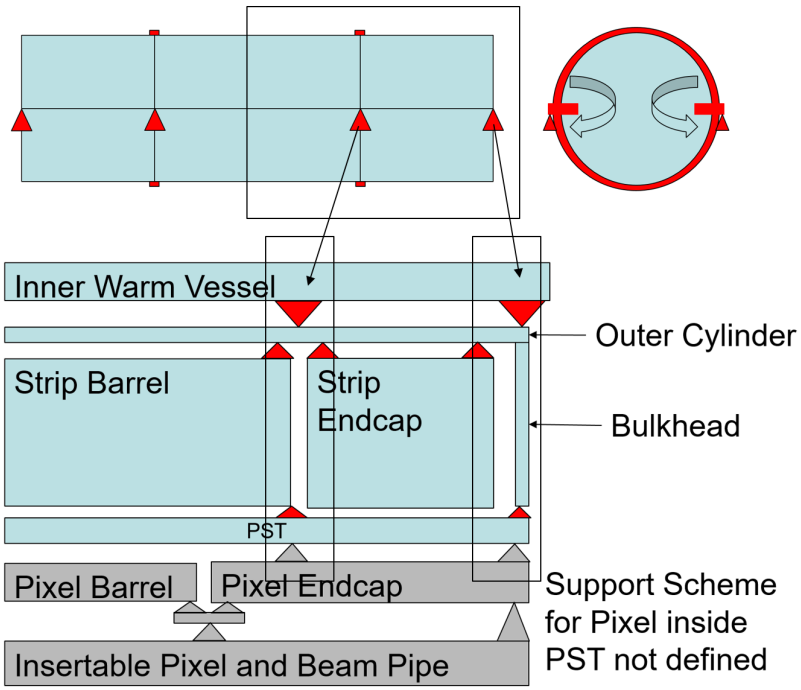


Figure 18.3: Support hierarchy of the ITk. The upper image shows the four locations of the rollers on the rail, the lower image is just a quarter of the detector.

REACTION FORCES [Kg]				
		F_{PP0}	$F_{EndPLate}$	F_{PP1}
	Z [mm]	1500.0	3170.0	PP1 > 3000
Standard train structure		93.2	38.7	73.3
Contelivered (Split @ Z=0)		87.3	44.7	73.3

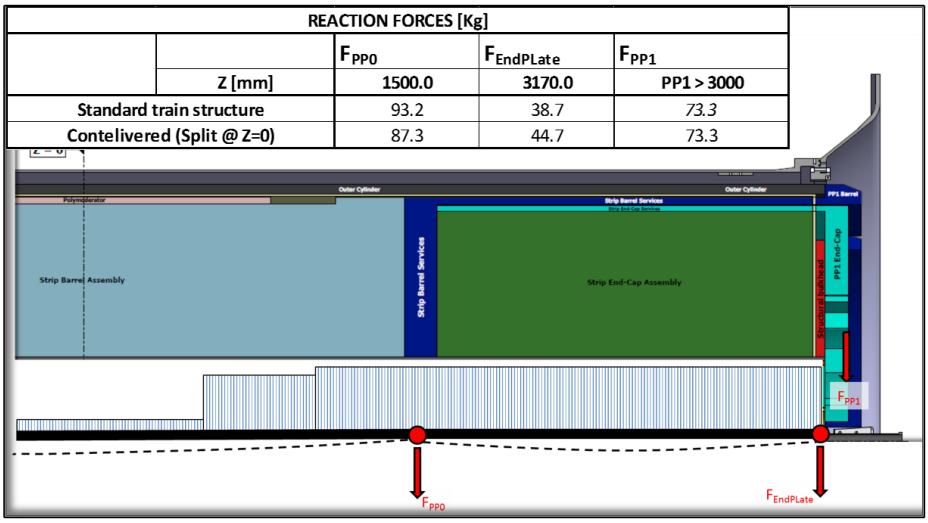


Figure 18.4: Mass loads of the Pixel Detector on the Strip barrel and outer cylinder and structural bulkhead.

to behave like a beam. The outer cylinder (OC) is a "shear dominated" design in its length dimension i.e. it does not behave like a beam along its length. The only way to stiffen a shear dominated structure is to add material or increase supports. The OC primary deflections will be determinded by how loads are introduced and transferred through its thin cylindrical wall to the rollers that support it on the rails. The radial envelope of 30 mm compared to a radius of 1 m is under 3% t/D. The local bending (flexure) of the cross-section is important. It is in the hoop (circumferential dimension) that minimising local deflections can benefit from interplay of sectional inertia.

18.3 ITk Barriers

18.3.1 Neutron Polymoderator

The polymoderator serves as a neutron shield which reduces silicon damage fluences by lowering the energy of neutrons 'back-splashing' into the ITk due to elastic collisions with protons in the calorimeter [152]. Various combinations of polymoderator geometry surrounding a strawman description of the ITk inside a detailed description of most of the current ATLAS detector have been studied [153]. The conclusions in this section are based on that study. In the current ATLAS design, the TRT acts as a neutron polymoderator for the SCT Barrel and the shielding [152] lines the end-cap and forward calorimeters. Since the ITk is a completely silicon-based design, it requires a more extensive polymoderator layout forming an envelope around the entire detector.

Assuming that the polymoderator material will be boron-doped polyethylene, a base design shown in Ref. [153] assumes 5 cm thick layers running along the barrel and end-cap cryostat walls, the inner face of the FCAL, and parallel to the beam-pipe between the end-cap cryostat wall and the inner face of the FCAL. This design reduces the 1 MeV neutron equivalent fluence in the central region (z = 0), which has the highest fluences, by at least 50% at radii greater than 40 cm, and approximately 70% at a radius 100 cm.

In order to allow for services, a similar study has been done with gaps in the polymoderator which simulate the required access. The effect of the gaps is expected to be less than 10%. Increasing the thickness of the polymoderator layer is only useful along the end-cap cryostat wall, where an increase in thickness to 10 cm is very beneficial; increases elsewhere have only marginal benefit.

18.3.2 Humidity Barrier

The ITk humidity barrier has to prevent the diffusion of moisture into the tracker. It is planned to re-use the current dry nitrogen supply system (3200 L/h N_2 or about half a volume exchange per hour, with a dew point of -80°C, corresponding to a water content

of 0.54 mm^3/L). In the current tracker, a dew point of $-40°C$ (water content of 127 mm^3/L) is achieved, corresponding to a back-diffusion rate of about 25 L/h of cavern air with a dew point of 15°C. It is believed that the biggest leaks in the current system are the service feed-throughs. In the barrel SCT, so far it is not possible to achieve measurable overpressure for a flow rate of 960 L/h. In the future tracker, the coldest components within the ITk will be the cooling-system return lines at a temperature of minimally $-40°C$. Therefore a dew point requirement of $-50°C$ is set in the ITk. For the given nitrogen flow this limits the maximum acceptable back-diffusion rate of cavern air to 7 L/h. Due to this more stringent requirement, the service feed-throughs for the ITk Detector are more carefully designed.

It should be noted that this humidity barrier is integral to the ITk and is therefore already functional during the surface integration of the ITk (sub-system PP1s will be installed progressively during the integration and need to be blanked off before that).

A secondary humidity environment is foreseen outside the tracker ends and extending into the gap between the calorimeters to the outer perimeter of the barrel calorimeter, similar to the current ID end-plate volume. The exact dew point requirements for this volume will be defined once the designs for the PP1s and the temperatures of services outside the ITk will be better understood, but currently a dew point requirement in this volume of about $-25°C$ is expected. This means that all cooling services in this volume need to be insulated to prevent condensation, although the performance required of this insulation will not necessarily be very demanding. Services will penetrate this enclosure in feed-throughs at the outer perimeter of the service gap, from which point the cooling services will feature high-performance thermal insulation.

The diffusion of moisture into the tracker needs to be prevented at all times, including access to the inner or outer pixel systems, even if the tracker is warm. While it is not intended to use internal thermal barriers in the future tracker, it is planned to implement internal moisture barriers between the strips and the outer pixels, and the outer and inner pixel layers to maintain the integrity of the humidity environment during the removal of these smaller units.

The humidity barrier will be physically part of the OC and the SBs. The exact implementation of the humidity barrier will be studied when the design of these structures will be more advanced. The strip services will penetrate the ITk humidity barrier just inside PP1. At this location, the service modules will contain a sealing block which will provide the internal humidity seal. The service module will then seal to the opening in the SBs to complete the hermetic humidity barrier.

18.3.3 Faraday Cage

The ITk Faraday cage needs to satisfy the grounding and shielding strategy for the ITk. It will be integrated into the outer humidity barrier, consisting of the OC, the tracker endplates and the beam-pipe insulation shield just within the inner pixel layers and their

services. There will be no electrical shield between the inner and outer Pixel systems, or between the Pixel and Strip systems. This implies that the end sections of the inner Pixel system would have an RF bond (continuous as possible) to the shield of the main tracker.

The electrical shield could be a thin $\sim$50 μm metal layer. Shielding properties of metal cylinders are being investigated to help in determining this thickness. All system cabling will have a braid shield so that the metal shell connectors can bond well and reliably. The referencing metal for the cable shields will be the Faraday cage. Service cabinets will have a complete shield enclosure. Both, cabinets and the tracker shield skin, need particular attention to joints and seams between metal shield components, such as galvanically compatible metals or plating. The use of bare aluminium in the shielding system will be avoided. Joints and seams need detailing that provides continuous electrical contact wherever practical. One technique which can be used between stiff metal components is plated BeCu finger-stock gaskets compressed by assembly fasteners.

All conductors entering the Faraday cage will bond at the entry, or be conditioned by an EMI filter mounted on the cage (Figure 18.5). This is standard EMI shielding practice. DC connections of shields are emphasised because the shield skin can be more complete. Practices such as pigtail connections of cable shields will be avoided. Metal shell connectors with full capture of the cable shield and circumferential bonding to a service enclosure give better EMI attenuation.

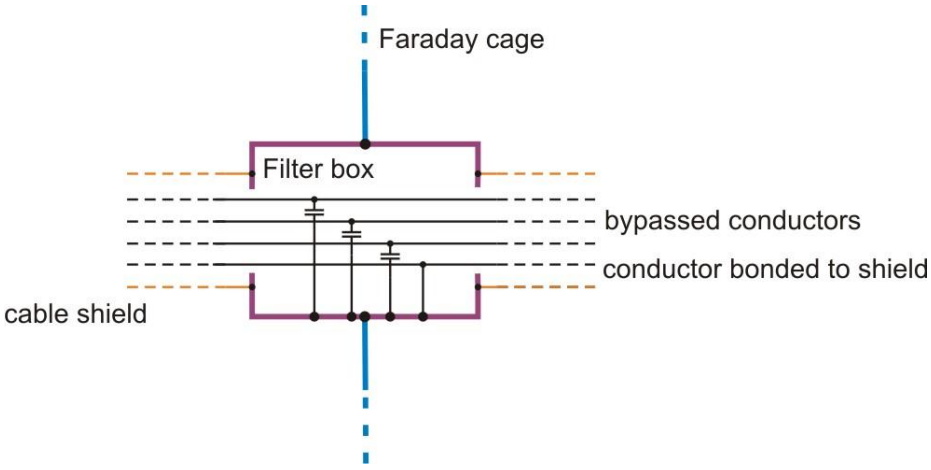


Figure 18.5: Ground connection concepts at the Faraday cage.

18.4 Installation at CERN

The assembly of the complete tracker, with all the sub-detectors and internal (Type I) services installed and qualified, will be done on the surface. Therefore the installation and

commissioning time in the pit will be minimised, limiting the exposure of operators to a potential harsh radiation environment, and the integration work can be done in parallel to the decommissioning of the present tracker in the pit.

The Inner Tracker (ITk) with all the subsystems and internal services will be delivered as a single unit into a cylinder of about 6.4 m length and an envelope diameter of about 2.25 m ready to be inserted into the LAr calorimeter bore and connected to the pre-installed (Type II) services.

The tracker has been conceived as a modular hierarchical structure where fully tested, contained components with simple interfaces (e.g. local detector supports such as staves or petals, or modular service assemblies) are combined into progressively larger units. These modular components of the tracker are delivered to the surface integration site from the distributed assembly sites tested and ready for installation. The surface integration site should allocate space for the actual integration of the tracker sections, for the storage of the components, as well as infrastructure for reception testing of these components.

18.5 End-cap Reception and Full System Testing at CERN

The strip end-caps will be assembled at macro assembly sites outside CERN. Chapter 11 describes the assembly procedure of the two end-caps in those assembly sites. This section will describe the required infrastructure needed for the reception tests and for final assembly after these are inserted into the outer cylinder.

A space will be needed to test each end-cap as it arrives at CERN as well as for individual petal testing for repair and or replacement. The end-caps will stay in the transport cradles during those tests. A temporary thermal enclosure will be needed for cold tests to allow working on the barrel in parallel. After insertion of the end-caps, cold tests will be done within the OC as with the barrel.

The methodology for transporting the end-caps will follow that used for the transport of the current ATLAS SCT end-caps [154, 155]. There are a number of requirements for this and the reception testing at CERN that come from the following considerations:

- The petals and the support structure are built with very high precision. High temperatures may compromise that precision. Also, the detector modules can be irreparably damaged by condensation. Therefore, the atmosphere inside the test box must be kept below 80% relative humidity (with 40% preferred) and temperatures must be guaranteed to be below 35 °C.
- Since the carbon-fibre end-cap support structure has been design to be as light as possible and to hold its load mainly in the vertical direction, the tilt angle should not exceed 10° during handling or transport.

The assembly frames will be supported from the transportation frames by wire-rope isolators, which have high damping coefficients in order to reduce vibrations. The transported object will be instrumented with accelerometers to record accelerations in all three directions, as well as temperature and humidity.

The transportation framework depends on the final transport option chosen and whether it is more appropriate to lift from below or crane from above.

19 ITk Cooling

The cooling system for the ITk Strip and Pixel Detectors will be based on evaporating CO_2 in a liquid pumped cycle cooled by an external primary chilling source. There will be a common cooling system for both, the Strip and Pixel systems in the ITk, which will be made up of several interchangeable cooling plants of the same design. CO_2 cooling is chosen as this gives significant mass savings inside the detector due to the possibility of having smaller diameter tubing than conventional refrigerants or liquid cooling applications [156]. CO_2 is able to work in smaller channels due to a few favourable physical properties. CO_2 evaporates at much higher pressures than common refrigerants. This high pressure keeps the vapour compressed and therefore the volume low. The boiling temperature is a function of the pressure and, as this is relatively high, a pressure drop in the lines due to small diameter piping does not cause too much change in the evaporation temperature. In addition to the benefit of high pressure, CO_2 also has a very low viscosity and high latent heat, meaning less flow is needed than with other refrigerants. The narrower pipes can accomodate much higher flow speeds, which is a benefit for the overall boiling heat transfer coefficient. This implies that not only the temperature gradients in the pipes are small due to the high pressure, but the temperature gradients from the fluid to the pipe wall are small as well due to the increased heat transfer coefficient. In summary, the fluid properties of CO_2 make it an ideal fluid for detector cooling. Furthermore CO_2 is radiation hard, it is cheap to use and environmentally friendly, which are all beneficial properties for the use in detector cooling. However the high pressure of CO_2 is the main challenge with its associated safety aspects, but due to the small allowable pipe diameters, the overall stored energy (the product of volume and pressure) is equal to low-pressure systems with larger volumes. For safety classification, the stored energy is what counts, not the pressure as such.

19.1 Requirements

The global power requirements for the ITk Strip Detector are shown in Table 19.1. The table also lists the foreseen number of cooling loops beyond patch-panel 1 (PP1) and the foreseen grouping of these loops connected to the PP1-PP2 distribution lines. For the ITk, a common cooling system is foreseen for the Strip and Pixel systems, so numbers are given for both systems.

The evaporation temperature for the ITk evaporative cooling is driven by the needs of the Pixel system. To maintain thermal stability of the Pixel Detector at the end of the ITk oper-

Table 19.1: Overview of the heat loads and cooling loop granularity. The pixel numbers include safety factors while the strip numbers are without any safety factors.

Detector	Power [kW]	Number of evaporators	Qty PP2-PP1 transfer lines	Transfer line power [kW]
Pixel EC	86	272	2×9	4.8
Pixel Barrel	57	135	2×8	3.6
Pixel insertable	17	15	2×2	4.3
Total Pixel	160	422	38	4.2 average
Strip EC	34	192	2×12	2.25
Strip Barrel	55	384	2×24	1.7
Total Strip	89	576	72	1.9 average
Total ITk	249	998	110	

ational lifetime, it is currently believed that a maximum evaporation temperature of $-35°C$ must be maintained in the Pixel system. This requirement is under review and will be updated once the Pixel system parameters are better understood.

19.1.1 The 2PACL Loop and Operational Experience

All current evaporative CO_2 cooling systems in particle physics are built according to the 2-Phase Accumulator Controlled Loop concept (2PACL) [157]. It provides a stable cooling temperature in the detector over a large temperature range from room temperature down to $-35°C$. In general the cooling temperature is very stable and nearly independent of the heat load. The system concept is such that all active hardware is away from the detector in accessible areas. The hardware inside the detector's acceptance is minimal and consists mainly of small tubing. This all makes the CO_2 2PACL approach an ideal method for tracking detector cooling. The developments described here are based on experiences from various particle physics experiment using CO_2 cooling [158–161].

A simplified schematic of a 2PACL loop is shown in Figure 19.1. The 2PACL method circulates an overflow of liquid through the detector. Only a fraction of the liquid is evaporated. The vapour quality range at the output is typically from 0% up to 30-50%. This low vapour quality range provides a high heat transfer from the pipe wall to the fluid.

The transfer lines from the distant plant in the service cavern "USA15" towards the detector are concentric with the liquid feed lines inside the vapour return lines. This concentric concept conditions the inlet liquid to be the same temperature as the 2-phase return line. The inlet liquid has a higher pressure than the 2-phase return, and therefore is always in liquid state by design. This is a must for the manifolds, as the presence of vapour would result in a very unstable flow distribution.

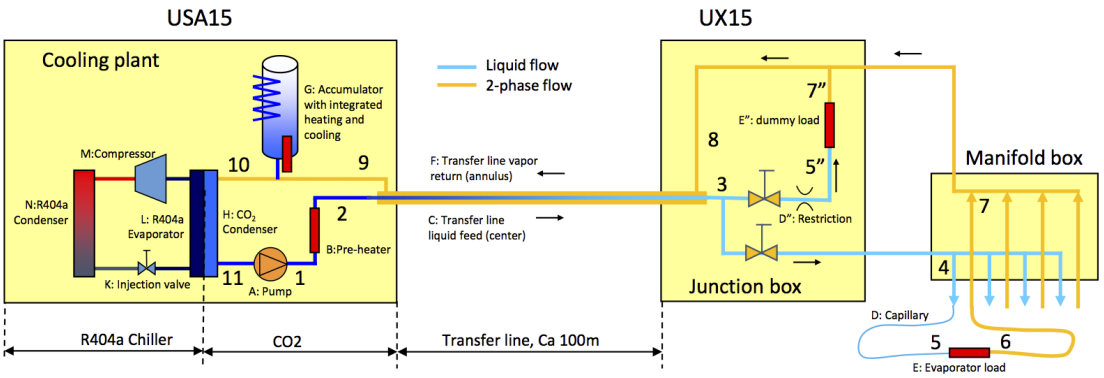


Figure 19.1: Simplified schematics of the 2PACL concept as it is used for the ATLAS IBL CO_2 cooling.

The thermal conditioning of the inlet liquid following the 2-phase return temperature also has a welcome regulation effect. The thermodynamic cycle of the 2PACL is shown in the pressure–enthalpy diagram in Figure 19.2. No matter what the 2-phase temperature is, the liquid temperature will adjust, following the 2-phase temperature. The liquid feed is state-point number 3, the 2-phase return is state-point number 8 in Figure 19.2. An expansion of the inlet liquid into the detector evaporator loops brings the loops into a low vapour quality state (state-points 4 & 5). Note that both, liquid and 2-phase state-points (3 & 8), lie on the same isotherm, which is horizontal in the 2-phase region and vertical in the liquid region.

The 2-phase temperature is the main parameter which needs to be controlled in a 2PACL loop. This is done by an accumulator vessel in the distant plant in USA15. The accumulator vessel always contains a liquid/vapour mixture and its pressure is controlled by heating and cooling. The controlled pressure of the accumulator dictates the pressure in the return line from the detector, which has a relative low pressure drop over the transfer line. The pressure of the return line sets the 2-phase temperature in the detector and, together with the previously explained liquid temperature regulation, makes that the system fully controlled by the accumulator only. This is why the concept is named 2PACL (2-Phase Accumulator Controlled Loop). This simple approach to control and the passive nature of the distribution inside the detector makes the concept ideal for detector cooling.

The evaporator status in the detector loops is represented by the state-points 5 and 6. The temperature is a bit higher than the regulated 2-phase temperature in the accumulator as the on-detector cooling distribution has a pressure drop due to the small lines needed for integration. A higher pressure drop and hence evaporator pressure leads to a higher temperature in the detector loops. Therefore pipes need to be designed with care to find the right balance between the pipe sizes and integration challenges, and between the thermal performance and the added cooling system mass. This is especially important for low-temperature operation as the temperature loss due to pressure drop increases with decreasing temperatures. On the other hand, the cooling system is prevented from going to the

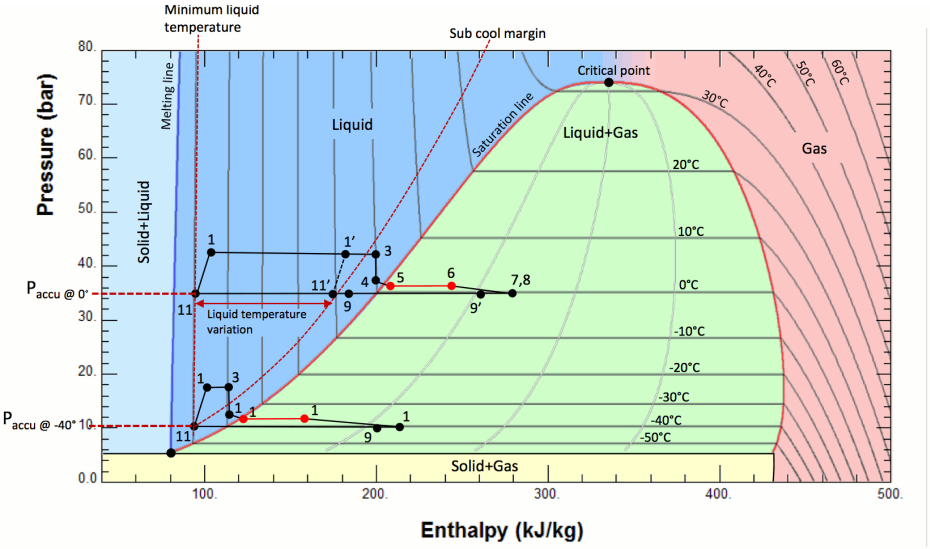


Figure 19.2: The 2PACL operation in the CO_2 pressure enthalpy diagram (State-point numbers the same as in Figure 19.1).

CO_2 freezing temperature (about $-55°C$). The lower limit is shown in Figure 19.2 with the lower cycle. Both the minimum temperature lines with sufficient offset to freezing and the sub-cool margin line come together, defining the lower limit of the cooling system.

19.2 Layout and Distribution System

The cooling system challenge in ITk is the increased number of parallel loops with respect to previous systems. LHCb-Velo, ATLAS-IBL and CMS Pixel have respectively 27, 14 and 24 loops per system. For ATLAS-ITk it is foreseen to have more than 100 loops per system (more than 1000 evaporators in total - see Table 19.1). This increased number of loops will require two manifold levels, one split at PP2 and an additional split close to PP1. The manifold in PP1 is inaccessible and thus should not contain any active regulation. The PP2 manifold will be located within the ATLAS muon system, where it will be accessible on the time scale of a day, and may contain some active regulation components. This means that the distribution must be carefully designed as the thermodynamics must take care of the proper conditioning of the cooling fluid state in the detector evaporator loops [162].

Previous experience with the ATLAS IBL and LHCb-Velo cooling has shown that the 2PACL concept in combination with capillary cooling pipes is sensitive to superheated liquid entering the detector loops. Such liquid is above the saturation temperature, but has not yet started boiling. This is a consequence of the purity of the liquid and the short time from the exit of the capillary to the start of the evaporator. Therefore the detector loops have liquid

cooling at the beginning rather than 2-phase cooling. Possible solutions are under study to guarantee boiling at the start of the evaporator. These raise the temperature of the liquid above the boiling point well before the evaporator and/or use improved tube surface qualities in the evaporator to encourage nucleation leading to evaporation.

The concept for the detector loop granularity is shown in Figure 19.3. Flexible vacuum insulated concentric lines connect the main manifold in the muon area to several so-called splitter boxes in the ID-end plate. In the splitter box, the cooling is distributed with single (vacuum) insulated lines into the detectors. The manifold at PP2 is typically served by a single cooling unit in the service cavern. The capacity of each flex lines is around 5 kW, and the typical grouping is 10 flex lines per PP2 manifold. Table 19.1 contains an overview of the foreseen granularity of the cooling loops and flex line distribution.

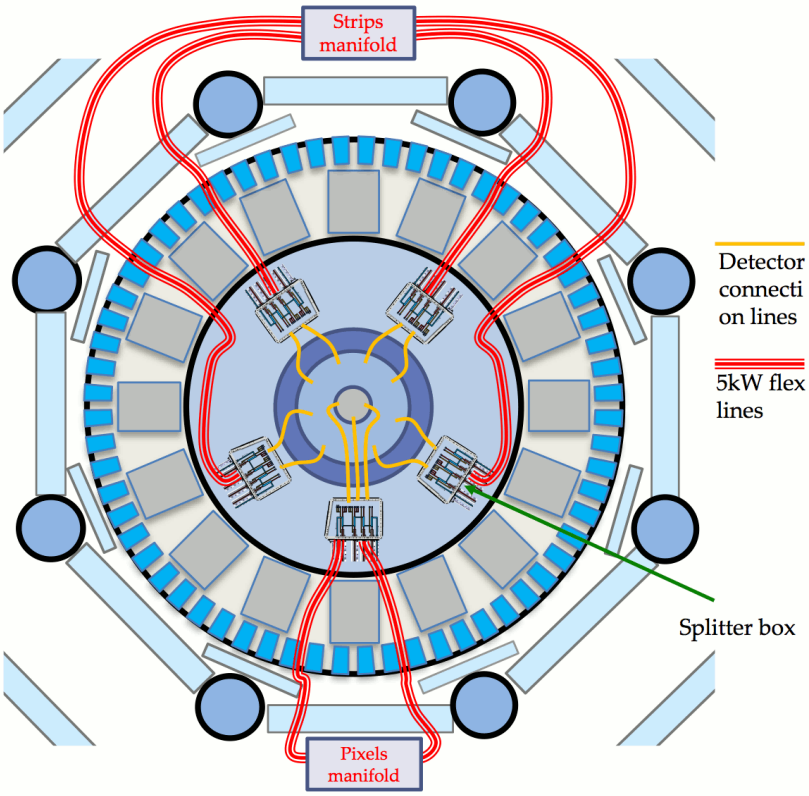


Figure 19.3: On detector cooling distribution with manifolds in PP1 and PP2.

The flex-lines' concentricity ends in the so-called splitter boxes inside the ID-end plate (see Figure 19.3). In the splitter box, the concentric line is split into separated inlets and outlets. The inlets are warmed up by a few degrees C to enhance boiling after the capillary or the orifice expansion into the detector loops. The warm-up is done by the so-called warm-nose loop which is discussed in Section 19.6.

From the splitter boxes, the liquid is fed to the detector loops where internal manifolds divide the flow over several parallel evaporator tubes inside the detector. Extra manifolding can be done inside the splitter box, but this increases the amount of cooling connections at the very busy outer periphery of the detector and therefore is not preferred. A PP1 manifolding of the Strip cooling lines is foreseen to optimise better the heat-loads for the 5 kW flex-lines. By doing so, the number of flex-lines can be reduced by 33% (see Table 19.1).

The manifold which is responsible for the last splitting into the detector loops inside the ITk must be designed with restrictions causing a 5-15 bar pressure drop. These restrictions are needed to regulate the flow distribution evenly among all the cooling loops. In evaporator loops, the pressure drop depends on the vapour content and thus the absorbed power. Without flow distribution restrictions, the flow will depend on the power input in an inverse way, meaning that less flow is fed to a higher powered evaporator loop, which can cause dry-out in these lines. A restriction in the liquid inlet of the last manifold in PP0 with a dominant pressure drop will minimise the flow imbalance effect. The liquid inlet conditions is the same for all branches and does not depend on the downstream heat absorption.

A second important aspect of the inlet restrictions is that the manifold pressure is high. This higher pressure suppresses possible boiling in the inlet manifold. Boiling in the inlet manifold is dangerous since a phase separation might cause a vapour feed to an individual cooling loop, which also causes a sudden dry-out of the evaporator line. To suppress possible boiling in all manifold levels, the last one inside the ITk must contain the major pressure drop and hence is the location for restrictions or capillaries.

All loops connected to a single system and hence PP2 manifold must be designed with the same pressure drop. If different flows are needed the restrictions must be chosen such that the pressure drop over the loops and restrictions is the same. A default design pressure drop is of the order of 5-15 bar, from minimum to the maximum required flow.

19.3 Cooling Plants

The cooling plants will be located in the accessible service cavern in USA15. There are multiple cooling plants connected to one or more PP2 manifolds. The currently foreseen granularity of the cooling plants is of the order of 30-45 kW each, but the optimum sizing is still under study. 45 kW seems to be a capacity which is reachable by currently available technology. A series of five to ten cooling units makes redundancy within the cooling system easily achievable. A spare stand-by unit can be swapped in place of a unit which is malfunctioning. An impression of a swappable unit configuration is shown in Figure 19.4. The accumulator is not part of the swapped unit as it needs to stay connected to associated transfer lines for fluid containment. To allow easy exchange of the actuators and sensors in the accumulator, a separate mounting in a parallel circuit is foreseen which can be disconnected and hence serviced from the main accumulator volume, such that the accumulator

pressure vessel can always stay connected. Figure 19.5 shows a simplified Piping and Instrumentation Diagram (P&ID) of a single unit.

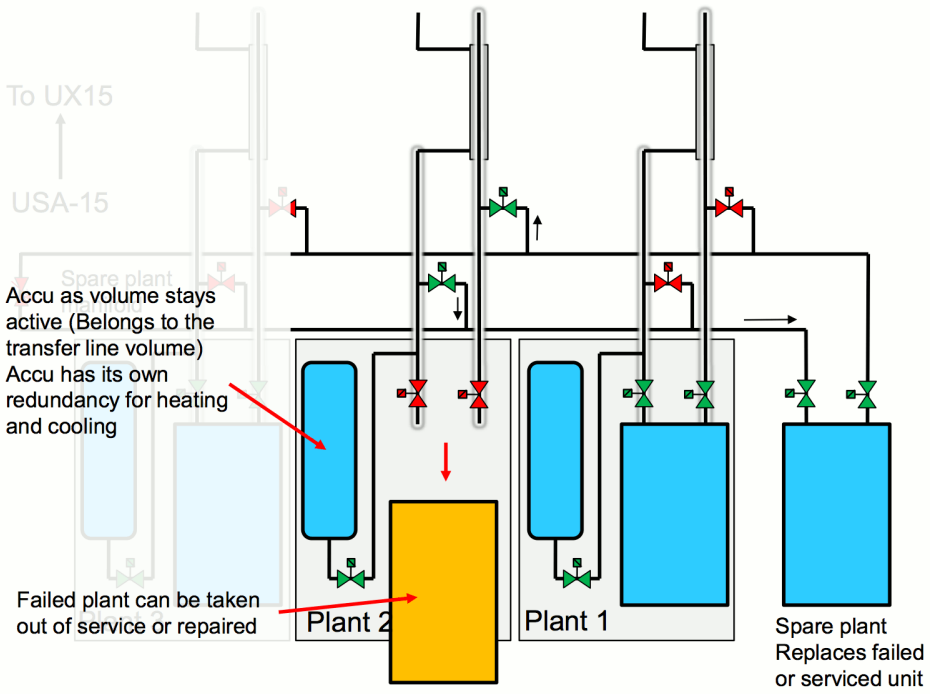


Figure 19.4: Layout of multiple units with a stand-by spare plant.

Each swappable cooling plant core unit contains the pump, the condensers, the dampers, the plant sensors and the internal by-pass. There are two primary cooling circuits, each connected to one plant core. The active primary cooling loop can be selected by two parallel mounted condensers and a selection valve on the liquid outlet. The primary cooling technology is still under discussion: it can be a direct expansion cooling system as it is done in current systems, but a liquid brine solution is also considered as it is easier to be applied to the cooling of multiple systems and is likely to be more stable, which is needed if the cooling temperature for ITk is considerably lower (below $-40°C$) than the current systems.

19.4 Pipework to PP2 (Type III)

The pipe work between the cooling plant located in the ST/CV technical room in USA15 and the PP2 distribution manifold placed inside the detector will be the vacuum insulated rigid triaxle transfer line. The inlet pipe will carry cold liquid CO_2 towards the detector and the outer pipe will return 2-phase CO_2 from the detector. Both coaxial pipes will be encapsulated inside the permanent vacuum insulation. The line size shall conform to industrial

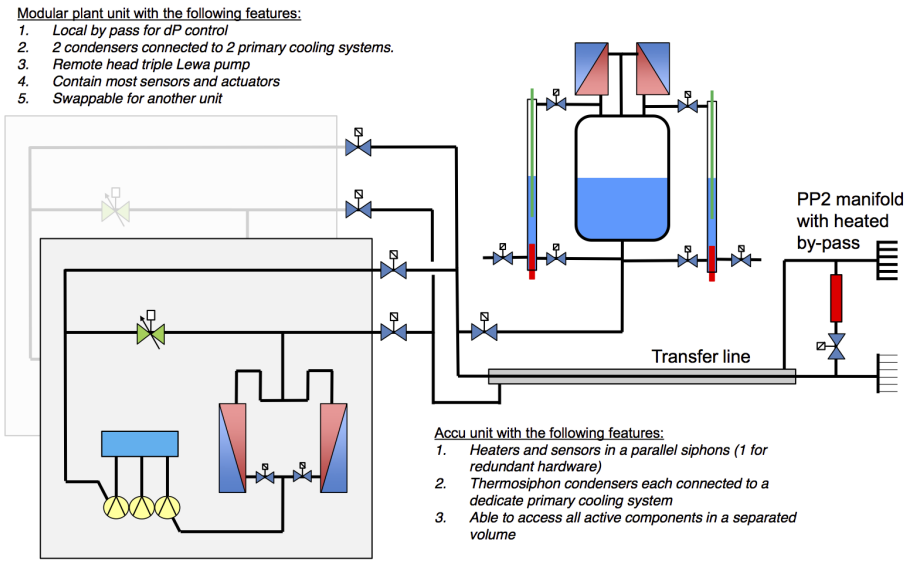


Figure 19.5: Possible layout of a cooling unit with an exchangeable cooling plant and accumulator controls. The accumulator volume remains with the connected transfer line.

standards with a minimum number of upwards columns in the return-line flow. Upward columns in a 2-phase flow cause a static pressure drop which is translated to a temperature gradient. Siphons should be avoided as much as possible to minimise fluid slug containment during standstill. Fluid slugs can be dangerous as they can be pushed through an already warmed up system causing thermal shocks. The vacuum level of the insulation tubes must be lower than 10^{-3} mbar, guaranteed by the supplier for at least 10 years. The line must be produced in sections to facilitate installation in the underground area. The individual sections have to be equipped with service ports allowing the connection of a portable vacuum pumping unit in case vacuum degradation occurs. Water condensation on the outer surface of the transfer line is not acceptable. During the system installation, the outer surface temperature shall be regularly verified using a thermal camera.

19.5 Cooling at PP2

The manifolds in PP2 will split the main transfer line into flexible transfer lines with a typical capacity of 5 kW. The flexible transfer lines have a 1/4″ flexible metal bellow hose for the liquid inside a 3/4″ flexible metal bellow hose for the returning 2-phase fluid. Both hoses have a multilayer braid for pressure containment. Multi Layer Insulation (MLI) is wrapped around the 3/4″ hose for thermal shielding. A glass-fibre braid wraps around the MLI and acts as a continuous spacer towards the outer vacuum bellow. The total outer diameter of a concentric flex line is 50 mm. A first study revealed that the quantity of flex-lines

in Table 19.1 can be accommodated and fed through the available passages. The principle routing is shown in Figure 19.3. In total, 55 or 37 flex-lines need to be accommodated per ID end plate.

19.6 Type II Pipes and Warm Nosing

The flex-lines terminate in the ID end plate. The concentric layout is split into normal pipe connections in the splitter box. Multiple flex-lines terminate in the same box. The liquid lines are fed through a warm-nose heat exchanger with condensing CO_2. All the warm-nose heat exchangers inside one box are connected in series. See Figure 19.6 for a typical warm-nose layout in a splitter box with seven flex lines. The warm-nose loop with condensing CO_2 is routed to the PP2 manifold using single lines (non-concentric). A back-pressure regulator in PP2 regulates the condensing pressure in the warm-nose loop and hence the liquid temperature of the liquid feed lines to the detector. In this way, the liquid temperature can be controlled inside the ID end-plate in a local passive way. A minimum amount of heat needs to be applied to the start of the warm-nose loop. This can be provided by a heater in the PP2 manifold or any other source of heat upstream of the warm-nose heat exchanger.

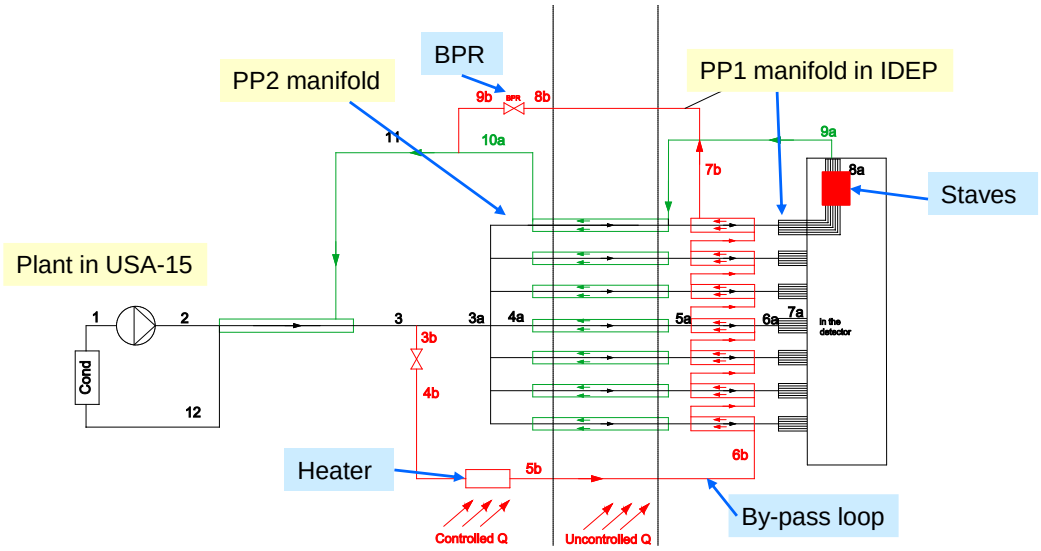


Figure 19.6: Layout of the PP2-PP1 distribution with a warm-nose pre-heater.

Figure 19.7 shows the operation of the warm-nose loop in the pressure enthalpy diagram. The vapour quality of the inlet of the detector after expansion (state-point 7a) is directly linked to the back-pressure regulator setting as the lines 6a and 4b and 5b are always crossing at the saturation line.

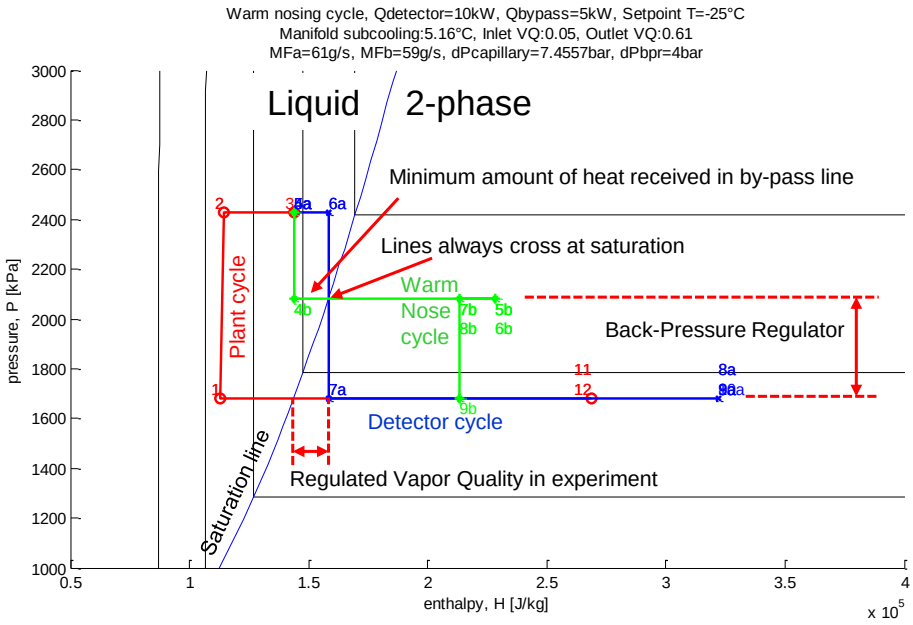


Figure 19.7: The warm nose regulation in the pH-diagram.

19.7 Control

The control system of the CO_2 detector cooling plant and its associated distribution will be based on industrial programmable logic controllers (PLCs) of Siemens or Schneider and Siemens WinCC OA as Supervisory Control and Data Acquisition (SCADA) to comply with CERN and ATLAS standards [163]. Both PLCs and SCADA will conform to latest version of UNified Industrial COntrol System (UNICOS) Continuous Process Control (CPC) framework of CERN. The UNICOS framework deals with the two upper layers of a classical control system: Supervision and Control, employing the terminology and models of the ISA-88 standard for batch control system. The PLCs and SCADA server for the process security will be placed within the CERN Technical Network which is physically detached from outside world. All the acquired data will be stored in the LHCLogging database, or equivalent, for long-term archiving. Additionally, via DIP and direct MODBUS, or equivalent communication protocols, data will be sent to the Detector Control System. The 2-way hardwired communication shall be provided to link the CO_2 control system with the ATLAS Detector Safety System.

If a distributed I/O topology for system modularity will be required, then the modern industrial field-buses will be used, such as Ethernet IP or PROFINET.

All cooling systems User Interfaces (UI) for the ITk will be accessible from one common point and based on unified structure. The SCADA visual instrumentation representation will be common to other CO_2 detector cooling systems at CERN.

20 Decommissioning of the Current ATLAS Inner Detector

The ATLAS Inner Detector (ID) decommissioning is defined as the ensemble of tasks associated with the removal of the first generation ATLAS ID and the preparation of the cryostat for installation of the ITk Detector. These tasks include, but are not necessarily limited to:

1. Engineering of the decommissioning process and the definition of procedures
2. Design and construction of necessary mock-ups, training platforms, and tooling
3. Training of personnel and documentation
4. Handling of radiation issues, both before, during, and after the in-cavern work
5. Realising the removal of the current ID
6. Preparing the cryostat bore for insertion of the ITk
7. Removal of all services from the ID up to PP1
8. Preservation of key elements of the current ID for future use in various ways (museum, posterity, archival, or additional physics searches)

The decommissioning project is divided into two phases. The explicit goal of the first phase of decommissioning is to define an ID removal procedure that is sufficiently advanced as to allow the writing of a detailed decommissioning plan. The process of writing this document is not explicitly included as a task within the project, but is understood to be the final goal, in addition to an initial cost estimate and a schedule for the decommissioning intervention itself. The second phase of decommissioning begins with the actual preparatory work for ID removal (a year or two before access to the cavern for LS3) and continues through the complete removal of the ID and preparation of the cryostat for ITk.

The explicit milestones of the Decommissioning Project are:

- Decommissioning Plan - End of 2017 (delivered as part of the Pixel TDR)
- Removal preparations begin - 2022
- ID removal start - March 2024
- ID removal completed - September 2024 (6.5 months total)

20.1 Baseline Decommissioning Process

There are several variations of the general decommissioning process. The baseline process proceeds step-wise and in series on both sides A and C. There is no concurrent work on sides A and C, except that which can be completed in a standard opening configuration. The reason for this assumption is two-fold: first of all, it is currently not possible to store both small muon wheels on the surface at the same time, limiting the possibility for a double full opening; second of all, there are not enough temporary access platforms (minivans) to open both sides of the detector to full open at the same time. Consequently, decommissioning will roughly proceed in the inverse order of original assembly; however, there are a two notable possible exceptions.

If an arrangement for storing both muon wheels on the surface can be found, and more minivans can be fabricated, then the process can proceed at both ends (A and C) in parallel. This will save time in the overall schedule.

If a method for removing both ID forwards from the same side (i.e. side C) can be found, then potentially the entire decommissioning process can be achieved from side C alone, avoiding the need for muon wheel storage and additional minivans. This could also save some time in the opening schedule.

20.1.1 Assumptions

Taking account of the status of the current ITk service design, the following assumptions have been made for the ID decommissioning:

- All services up to PP2 (see Figure 17.2) will be destroyed during the removal process (or at least may be rendered unusable after the decommissioning process is complete)
- The detectors should be removed intact.
- The beam-pipe should be removed intact.

The design of the interface between the beam pipe and the surrounding pipe (IPT) allow a quick and easy extraction as the beam pipe simply slides into the IPT. During the design of the extraction tooling, the beam pipe grabbing operation was estimated to be faster than the flange cutting operation. Not cutting the flange furthermore reduces the pollution on the coating inside the beam pipe during cutting and during the unavoidable re-welding operation in prevision of the re-conditioning for phase 2.

20.1.2 Decommissioning Steps

The decommissioning of the ID will use a step-wise removal process, which in the baseline scenario only assumes a sequential removal process.

The first step is to determine the activity of the beam-pipe end flange. If the activation is too high to permit work on services, then the beam-pipe end flange is cut off. After this initial step, the IBL and beam-pipe cables are either cut or disconnected and then removed or folded back from the end plate of the ID (IDEP). The IBL and the beam-pipe are then removed, most likely as one package, but removing them sequentially is also possible. Then the cables of the Pixel detector are either cut or disconnected at the IDEP nose. This includes both Type 1 and Type 2 cables at the PP1 patch-panel interface within the Pixel "nose". The Pixel detector is then removed from side C, as internal constraints of the Pixel detector make it impossible to remove it from side A. The entire Pixel package is then removed in one operation. The Pixel detector services and the IDEP Nose are removed. Normally care would be taken to support the end of the forward Pixel Support Tube, but in the case of decommissioning, no such action is required and forward Pixel Support Tube will remain cantilevered through the ID forward.

With the Pixel detector removed, the services for both the SCT and the TRT are cut and the Service Termination boxes are removed. The extent of removal of the service boxes depends on their inner radii, on their respect of the initial envelopes and the requirement that the ID forward can eventually be removed without collision. The end-cap is then removed while the barrel services remain on the cryostat bore. This is a multi-step process as the ID end-cap chariot must be lowered, installed, and aligned with the rails in order to accept the end-cap during their removal. Then the Forward Pixel Support Tube is removed and disconnected at the barrel end flange. The ID barrel services are cut or disconnected at the barrel end flange. These services must be removed within such a radius that it is possible to pass the ID barrel over the connection points.

Moving to side A, the Pixel services are either cut or disconnected and then removed or folded back. In the parallel scenarios (see Section 20.1) this can happen at the same time as with the work on side C. Then the Pixel detector services and the IDEP Nose are removed followed by cutting the SCT and TRT services, the removal of the ID end-cap, the associated services and the removal of the Forward Pixel Support Tube. This is concluded, as with side C, with the disconnection of the barrel services. Now the forward rails are exchanged for the barrel extraction. While the ID end-cap is installed on a flat rail, the ID barrel rolls on V rails, which are obstructed by the forward rails. Thus the forward rails must be changed in order to allow for the passage of the ID barrel.

With the barrel removed, the remaining services and rails that still remain on the cryostat bore are removed. This process requires the full scale removal of the services trays as a baseline. An option exists to leave the services trays intact, while allowing for them in the ITk envelope, but this will only be pursued if the removal of the trays cannot be done

without damage to the Inner Warm Vessel of the barrel solenoid cryostat. The last step of the decommissioning involves the removal of the existing rails, and then the stripping out of the cable trays (if at all possible) for a clean bore. Now the cryostat is ready for the installation of the ITk detector.

20.1.3 Removed Items and Condition of ATLAS after the Removal of the ID and Associated Infrastructure

Archival of the ID is considered to include all activities that take place once the ID has reached the surface. This falls into several broad categories:

- Post-mortem analysis,
- Posterity (i.e. museum use, exhibits, etc.) and
- Potential future physics searches, i.e. magnetic monopoles.

The uncertainty in this activity is large, since its scope could range from simply disposing of the current ID to doing a full extraction to investigate some as-yet-unknown catastrophic failure. While it is unwise to plan for all eventualities, it is also unwise to be completely unprepared for some form of post-removal activity.

After removal of the current ID, the cryostat will be left in near original condition (i.e. bare without cable trays). However, there are certain thin features (5 mm aluminium plates) which may be left in place, as they will have a minimum effect on envelopes but will be more difficult to remove than the cable trays. Initial removal tests on the cable trays installed into the prototype cryostat bore (in B180) have shown no issues in removing them completely.

20.1.4 Radiation Environment for ID Decommissioning

Planning for the ID decommissioning intervention and ALARA procedures is highly dependent on reliable dose calculations, adapted over time to the evolution in radioactivity as measured between now and LS3. It also requires a flexible work-time and zone-occupancy calculator that can be fed with a dose map and allowed to output individual and group dose levels per intervention. It is proposed that this will be achieved with an image-recognition based monitoring system, which allows:

- Zone-based “surveillance” camera data collection
- Time-in-zone calculation capabilities
- Software so that ATLAS can write algorithms to feed in custom dose maps based on the surveillance calculations.

Zoneminder is a multi-camera, open source, Linux based application [164] which may be ideally suited for adaption to this usage. The process would work as follows:

1. A procedure will be developed respecting ALARA principles
2. Technicians, under camera surveillance, will conduct exercises on the ID mock-up following the procedure. Their time in pre-defined dosage zones will be computed.
3. The currently understood dose map will be applied to these timings to compute the effective dose for the intervention
4. This dose will be compared to the initially calculated dose to determine where in the procedure the timings or work zones are incorrect
5. The procedure will be modified accordingly to improve the overall exposure of the intervention team
6. This whole procedure will iterate until the dosage reaches the minimally reasonably achievable level (ALARA).

This procedure relies on accurate dose maps. Calculations are currently underway for the majority of the detector configurations, and should allow a good initial assessment of exposure. Existing calculations of the dose maps will continue to be refined and cross checked with measurements through measurements at Year End Technical Stops. Considerations about the radiation simulation are discussed in Chapter 22.8.

20.2 Decommissioning Procedures and Tooling

20.2.1 Development of Procedures

It is one of the goals of phase 1 of the decommissioning project to determine the baseline process and procedures for the final decommissioning intervention. This includes documenting the process and defining which parts are missing or in need of new tooling development. An integral part of determining the baseline procedure will lie in evaluating alternative procedures as well, including:

- Removing both ID end-caps simultaneously
- Removing the entire ID from one side (both end-caps and barrel)
- Any other permutation deemed attractive by cavern movement considerations

Once procedures have been developed and practised on the ID mock-up[1)], a training programme will be developed for the phase 2 part of the project. The training program will need to insure that the technicians can carry out the work successfully, that they respect the dose allowances which have been previously attributed, and that there is sufficient overlap in the team competences to prevent single point failure. The intervention schedule will be extremely tight, so the program cannot rely on any one technician being essential to the removal process.

20.2.2 Tooling Custody, Archival, and Database

All tooling necessary for decommissioning must be either:

- Located, if it still exists
- Repaired, if it is damaged or partially missing (assumed to often be the case)
- Re-fabricated, if it no longer exists (probably the case for most of the smaller and more specialised tools)

Ideally, an associative database of specialised tooling, in addition to standard required tooling should be created in order to allow tracking of the tooling as it is located, repaired, or acquired, and which can alert the intervention crew to what tooling is required and when. In the case of A large part of the initial tooling custody work has already been undertaken by the ATLAS Technical Coordination (TC) and ATLAS Detector Operations (ADO), and assisted by various subsystem technicians.

20.3 Schedule for Planning, Preparation and Decommissioning

The overall ID decommissioning schedule is front loaded, as most of the preparatory work must take place before the end of 2017. However, it is also understood that much of the work for decommissioning is uncertain, and that there is significant slack time in the 2018 – 2020 time period. Thus it is highly likely that the scope of the project may change given potential problems that may arise during investigation of the decommissioning process. These unknowns will become less uncertain over the course of the next year. Likewise, it is currently unknown what tooling will need to be fabricated, what time that will take, and how much that will cost. Tooling fabrication for the actual intervention is therefore included here only as a placeholder, and will most likely not be approved until after approval of the Decommissioning Plan. This tooling fabrication will most likely fall in the 2018 – 2020 time period. The detailed schedule is being developed in detail.

[1] A 1:1 mock-up based on the original ATLAS ID mock-up is being adapted for the ITk studies.

21 Installation

21.1 Overview over the ATLAS Area

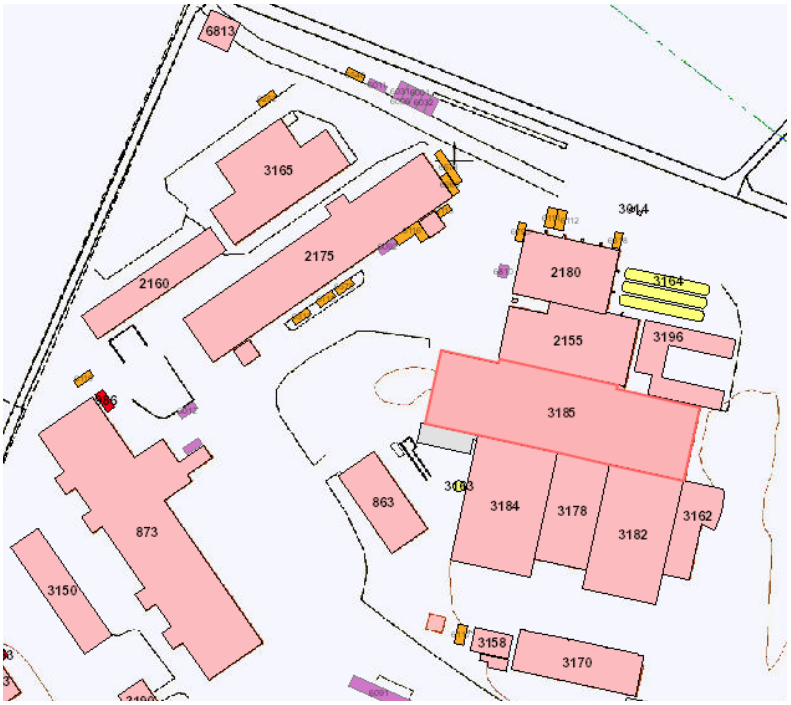


Figure 21.1: Surface map of the ATLAS experimental areas. SR1 is building 2175, shaft access to the ATLAS cavern is in building 3185.

A surface plan of the ATLAS experimental area is given in in Figure 21.1. The most important areas for the integration and installation of the ATLAS ITk will be SR1 (building 2175), where the surface integration of the ITk will take place and building 3185, which houses the access shafts to the underground cavern. A sketch of the underground areas is shown in Figure 21.2.

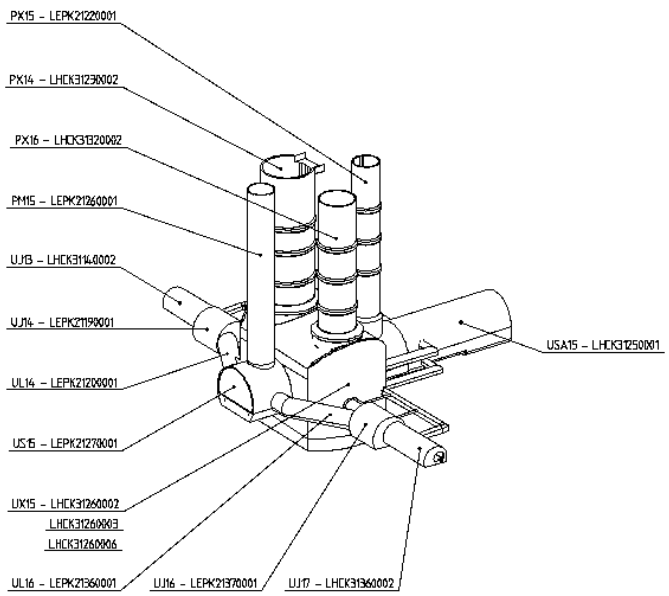


Figure 21.2: ATLAS underground areas. The accelerator is housed in the UJ tunnels. The experiment is in UX15 and the main service areas for the experiment are located in USA15 (main counting room, cooling plant etc.) and US15. The ITk will be lifted through PX14.

21.2 ATLAS Opening Configuration and Infrastructure

Because of the size of the Outer Cylinder the movement to the inner bore of the Barrel cryostat will require ATLAS to be in the "Large Opening" configuration, which is the only one that provides a gap between the end-cap and the barrel Toroid which is large enough for the Tracker to pass. Temporarily access platforms, called Minivans, will be installed on the ATLAS rails to provide a work platform inside the area, together with dedicated access tooling (rails, scaffolding, etc.). This configuration has been used to install the Inner Detector in 2007 and more recently the IBL detector in 2014.

Six minivans are installed in between the barrel and end-cap calorimeters, providing a work area of about 11 m $\times$ 6 m. Two rails are installed parallel to the beam axis in order to move the ITk on its insertion tooling (see section 21.4.2. The load capacity of one Minivan at the interface with ITk tooling has been certified for 3,000 kg; however, calculations have been performed showing that this load limit could be increased to up to 6,000 kg per Minivan. In case this is needed, no reinforcement would be required but the certification process would have to be partially revisited and an appropriate load test performed.

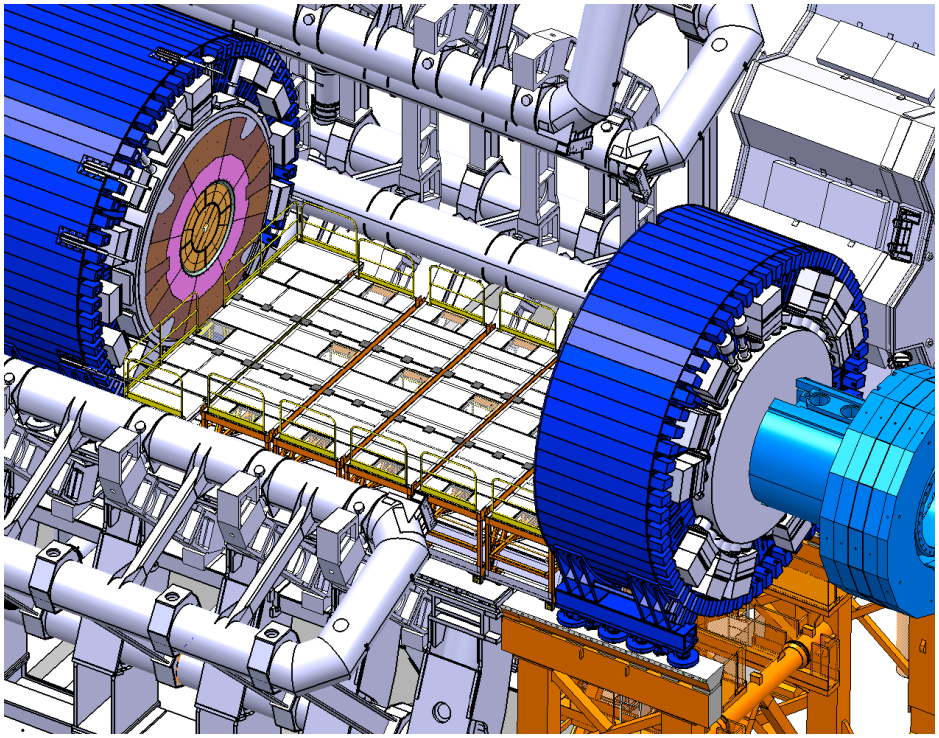


Figure 21.3: ATLAS Large Opening configuration, the end-cap calorimeter is moved as much as possible toward the Target Absorber Secondaries (TAS), six Minivans are positioned in between the barrel and end-cap calorimeters.

21.3 Preparations of the Cryostat before the ITk Insertion

21.3.1 Installation of Rails

The ITk is supported and guided during its insertion into the inner warm vessel by the ITk rails (see Figure 21.4). This new aluminium rail system is dimensioned such that it can take the load of the new tracker (about 5 t). The ITk rails are installed on both sides of the inner warm vessel on the same rail support that are used by the current Inner Detector, which is called the tracker support rail. The geometrical shape of the ITk rails will be defined with the interface support of the Outer Cylinder once its design is more advanced.

The Tracker Support Rails (tracker support rail) contain M5 threaded holes distributed every 60 mm along its length, which will provide the anchoring points and the vertical and horizontal references for the new rails. To be able to limit the traction forces on the M5 bolts, the lever arm to take the torque created by the load eccentricity is increased at the bottom part of the rail by a fixation point on the inner warm vessel.

Both rails are brought inside the inner warm vessel as a single element. Their weight (about

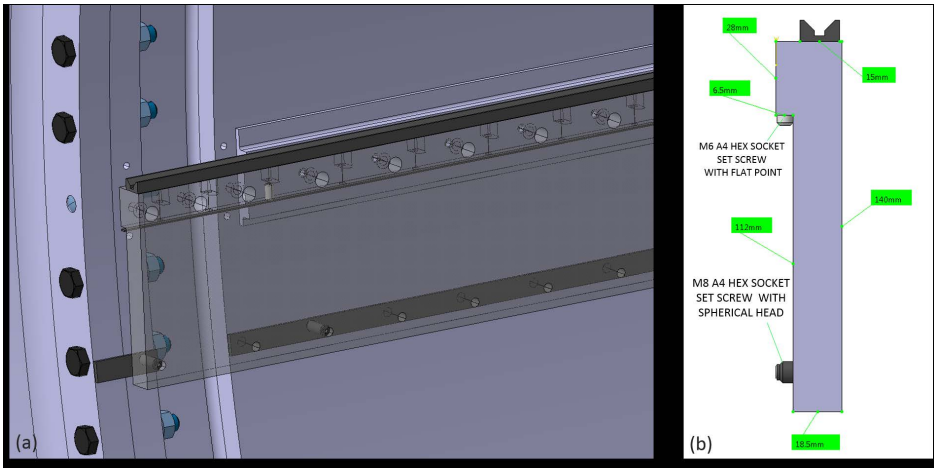


Figure 21.4: (a) ITk rail connected to the Inner Warm Vessel (inner warm vessel)and (b) ITk rail cross section.

50 kg) will allow a manual manipulation and installation on the tracker support rails. Once installed on the inner warm vessel rail support, a survey operation is done:

- to adjust the vertical position.
- to adjust the horizontal position at the level of the V-shape rails (Figure 21.5).

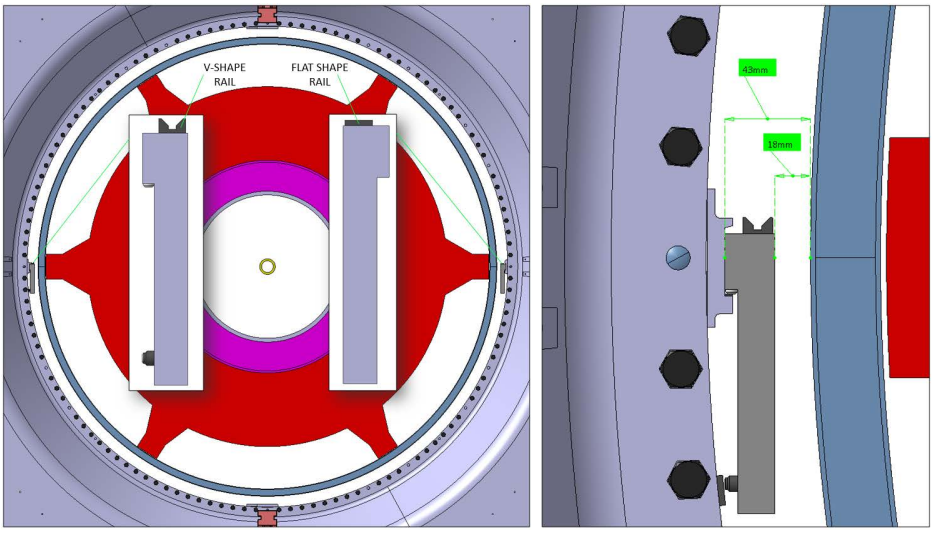


Figure 21.5: V-shape and flat shape rail guides on the ITk rails.

The expected range of positioning is in the order of 0.2 mm as achieved on the ID rail. The eccentric point of the rails will be brought close the inner warm vessel with a controlled gap of about 0.2 mm. Further analysis is required to finalise this gap value.

Access to the inside of the inner warm vessel over the full length will be possible on a platform supported at both extremities on the minivans as it was done during the installation of the ID rails. If the activation in the inner warm vessel is such that a shielding or any other tooling is required to allow access for work specific access these means will be developed.



Figure 21.6: Access platform inside the inner warm vessel during ID construction.

The time required to perform the installation and the adjustment operation will be measured on a scale one mock-up.

21.4 ITk Transport

At the current stage of the project it is not yet decided if the integration support structure that will be used for the integration activities in SR1 will be used also as the transport structure for the transport to building 3185 (SX1). It would make sense that a common support structure with both functionalities of integration and transport exists to minimise the manipulation and load transfer of such delicate detector. The functionality and feasibility details will be discussed and worked out during the tooling definition, once the architecture of the Outer Cylinder is better defined.

Several specific tools are needed to perform the transport and positioning of the ITk into the barrel cryostat inner bore. All these tools are still under design at a conceptual stage.

We can therefore not give a detailed description of these items here, but we present a list of these tools as well as their main functions.

- **Transport Frame:** The main function of the Transport Frame is to allow the lifting and the manipulation of the ITk with overhead and mobile cranes between the surface buildings and from the surface (Bldg. 3185, SX1) to the underground experimental cavern (UX15). The secondary function of this frame is to provide environmental protection for the ITk while it is transported out of clean and controlled environments.
- **Support Cradle:** The function of the Support Cradle is to support the weight of the ITk. The ITk detector is similarly interfaced with the Support Cradle as it is with the calorimeter bore rail system. The adjustment of the Support Cradle is allowing the positioning of ITk prior to its insertion into the calorimeter bore.
- **Rotating Table:** Whatever the lowering scenario will be, the ITk will be unloaded on the Minivans with its axis perpendicular to the beam axis. There is a need for rotating it by ninety degrees. This is the primary function of the rotating table. The table will also be used for the translation movement from the lowering point to the insertion point using wheels or rollers interfaced with the rails installed on the top of the minivans.

  The Rotating Table must be capable of supporting the weight of all the objects resting on it: The ITk, the Support Cradle and the Transport Frame. The preliminary estimate for the total weight of these objects is about 7 t.

The Transport Frame is interfaced with the Support Cradle; they can be combined such that they create a single tooling with both individual functionalities. Further study will define if a combined design makes sense with respect to the integration and transport constraints.

21.4.1 Crane Operation

The overall dimensions of the package that is possible to be handled, including attached services are defined in the envelope drawing; the outer diameter is 2,216 mm and the length is 8,000 mm. One should note that the Transport Frame for the Outer Cylinder needs to be added to the envelope in order to define the overall transport envelope. This work is ongoing and will be updated regularly, as the definition of the Transport Frame will progress. A conservative estimate of the ITk weight is about 5 t. Therefore even with the addition of the Transport Frame the total weight will stay below 7 t.

The transport operation from the Surface building (SX1) to the experimental cavern (UX15) will be done by the overhead 20 tonne crane of SX1 building. Although the operation could be performed either on side A or on side C of the experiment, the baseline has been defined to be on side C.

To access the Minivan platform two paths are identified currently:

a) Direct from the surface:

The ITk is lowered by the 20 tonne crane directly from the surface to the Minivans, through an open space at the top sector of the Barrel Toroid. The Inner tracker passes in between the end-cap calorimeter and the top toroid coils nearly vertically on top of the beam axis (Figure 21.7). The advantage of this solution is that the operation is direct with the 20 tonne crane and does not need any load transfer. However, the clearance between the Outer Cylinder and the various obstacles on its way is as small as 30 mm at the most critical place. This entails not only specific constraints on the design of the Transport Frame and Support Cradle but also a lot of care during the lowering operation. Among other constraints, this option requires the provisional removal of two main obstacles: the Forward Platform in sector 3 and the Barrel Toroid vacuum pipe as shown in Figure 21.7. Although this will require some additional work, it is not difficult and is not considered as a showstopper.

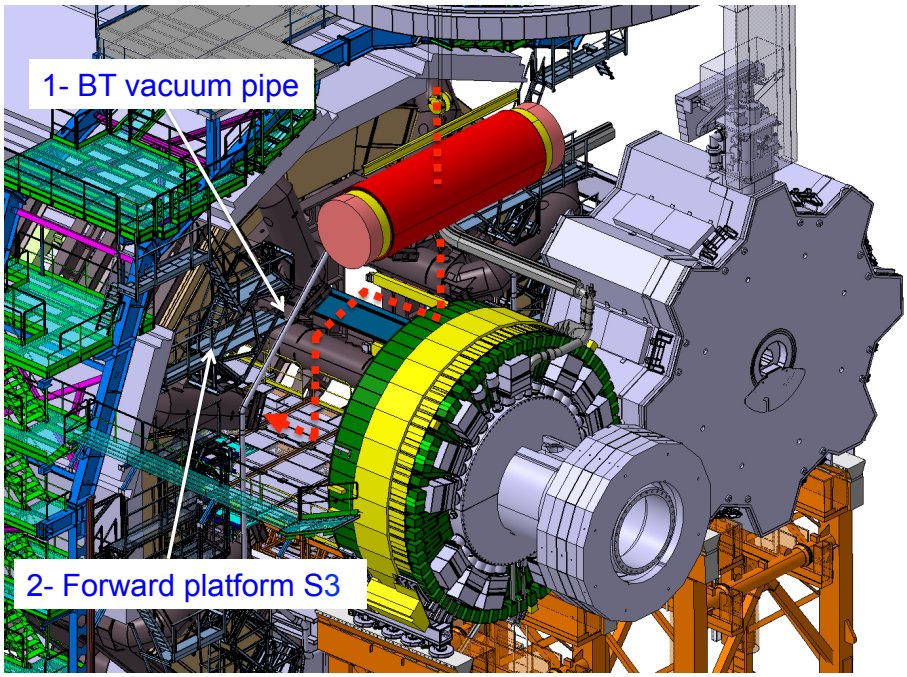


Figure 21.7: Path a: The ITk is lowered directly from the surface onto the Minivans; the red dotted line indicates the path.

b) Sideways lowering:

In this scenario, the ITk is inserted onto the Minivans platform from the US side (Sector 1). This path is incompatible with the coverage of the surface crane; a load transfer is required inside the experimental cavern (UX15) so that the operation can be performed using the local underground crane (65 tonne capacity). The only possible location for this load transfer is on the top of the end-cap calorimeter which needs

to be equipped with a resting platform to allow for this operation. Once the transfer is done, the ITk is lowered beside the calorimeter to the beam axis height and is then moved sideways until it can be unloaded onto the insertion tooling (Figure 21.8). This scenario has the main drawback that it requires the load transfer on the top of the calorimeter, which entails the design and manufacturing of an additional platform, including access means and personal protections. Nevertheless, the clearance between the Outer Cylinder and the various obstacles on its way is about 90 mm at the most critical place, which is a clear advantage of this option.

As for the previous scenario some conflicts have to be resolved by removing some items temporarily. Three main obstacles have been identified: the Forward Platform in sector 1, the Barrel Toroid vacuum pipe and the arch stairs as shown in Figure 21.8.

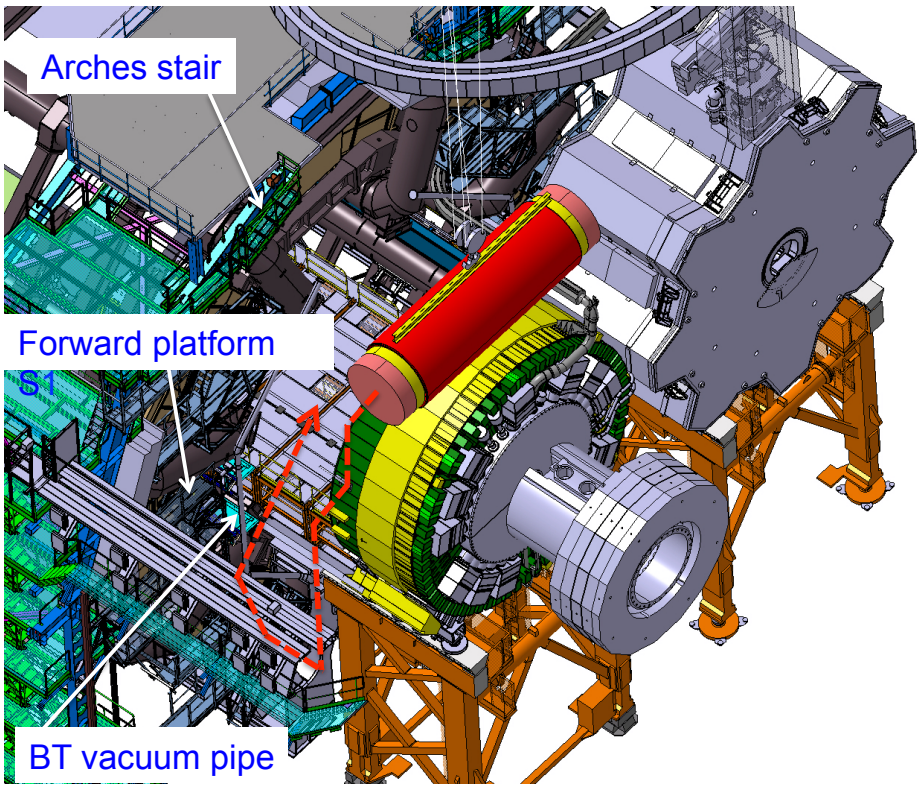


Figure 21.8: Path b: The ITk is lowered in 2 steps: first onto the top of the end-cap Calorimeter then sideways to the Minivans; the red dotted line indicates the path.

Option a) is more straightforward and is the preferred one despite the very small clearance involved. However, it is mandatory to ensure that the ITk can pass through such a small clearance. The opportunity to study the geometry of ATLAS in a Large Opening configuration is not frequent: a Large Opening was performed on side C during Long Shutdown 1 (2013-2014) and the next Large Opening will happen on both sides during Long Shutdown 2 (2019-2020). During LS1 an accurate survey has been done, in particular a 3D scan. The

data from this survey has been used to create an "as built" 3D CAD model of this region of ATLAS. This model is being used to study the lifting scenario and the installation tools.

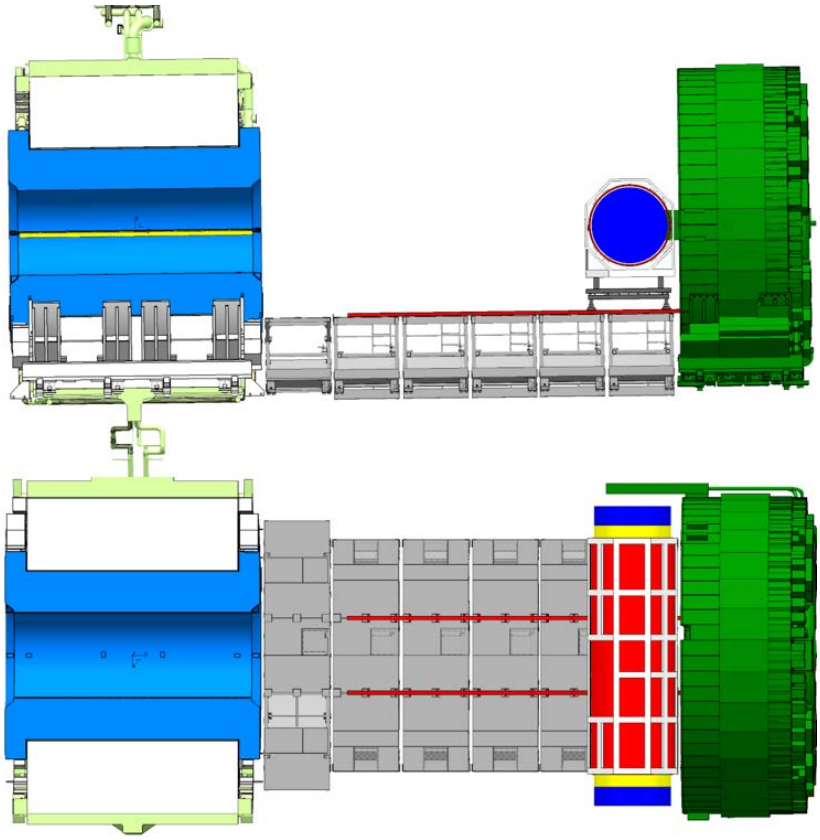


Figure 21.9: Position of ITk on minivans platform after release from the crane (Position 1).

In order to mitigate the risk related to the very small clearance, it has been decided to perform a blank test of the ITk lowering during LS2, which is the next opportunity when a Large Opening of ATLAS will take place. A dummy Outer Cylinder will be manufactured, including space reservation for services, together with a dummy Transport Frame and Support Cradle. The use of a spreader beam may be required; it has to be studied later on. The dummy package will be moved to the Minivans without unloading it, as the installation tooling will not be available at that time. However, no showstopper is expected in this step.

Both lifting scenarios will be tested in order to check that all conflicts have been detected.

In both scenarios, the BT vacuum pipe needs to be modified to allow its local removal to free the passage of the ITk package. It will be the right time during LS2 to implement the

modification on the vacuum line to anticipate the required LS3 configuration and to test the insertion paths with the dummy ITk package.

Preparatory work is one of the keys of such operation. Once the end-cap Calorimeter will have been moved to the Large Opening position, the six Minivans will be lowered successively and rails will be carefully positioned and surveyed with respect to the Barrel Cryostat inner bore. Then the Rotating Table will be lowered and installed onto the rails of the minivans, ready to host the ITk package.

Due to the access constrains, the ITk detector with its Support Cradle are released on the Rotating Table perpendicular to the beam axis close to the end cap calorimeter at about 13,400 mm from the IP (Position 1) as shown in Figure 21.9.

21.4.2 Rotation and Translation

To reach the insertion position, the ITk on its Support Cradle needs to be successively translated towards the IP at about 9,400 mm from the IP (Position 2), and rotated by 90 degrees to be coaxial with the beam axis (see Figure 21.10.

Then the package is translated up to its insertion position at about 6,775 mm from the IP (Position 3) as shown in Figure 21.11.

The translation movement is done on a rail system installed on the minivans, parallel to the beam axis, similar or identical to the one used by the ID. The rotation to bring the ITk axis onto the beam axis will be done on a Rotating Table similar or identical to the one that has been used for the Inner Detector.

At this stage of the project it has not been decided if these translation and rotation movements are manual or motorised using actuators. Several parameters need to be evaluated before taking that decision:

- The weight of the overall translated object.
- The activation in the environment that may limit the presence of operators during the operation.
- The precision needed for the control of the movement parameters like position, speed and acceleration.

21.4.3 Insertion of ITk into the Cryostat

At the end of the translation and rotation steps described in the previous section and prior to the insertion of ITk into the calorimeter bore, a precise positioning will be done to bring the ITk package co-axial with the inner warm vessel tracker support rails. This positioning

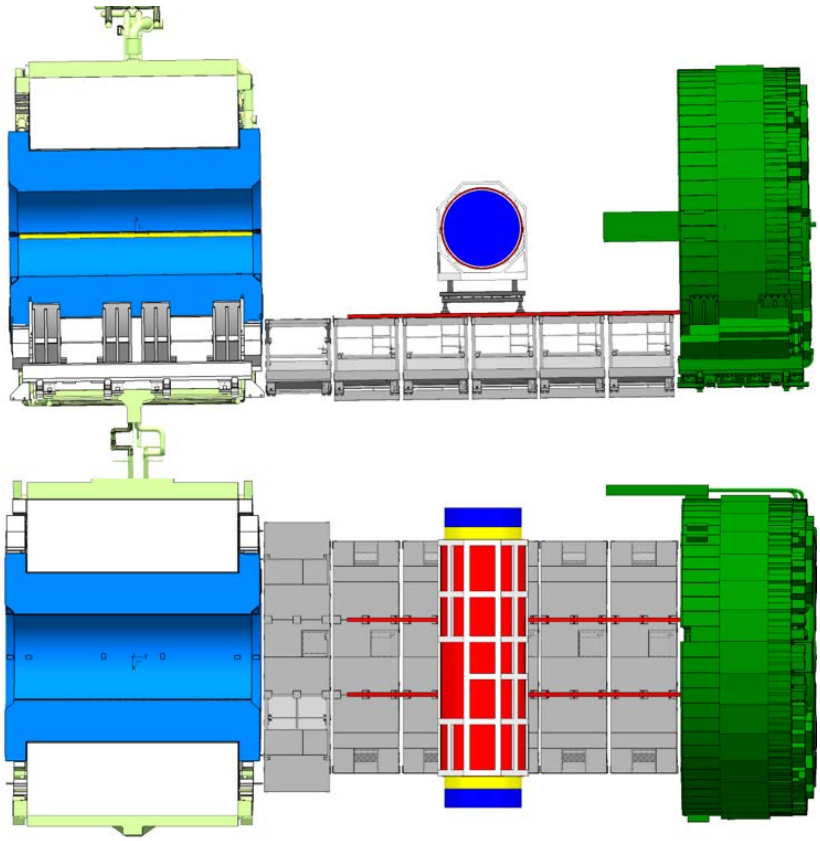


Figure 21.10: ITk Rotation position (Position 2) at about 9400 mm from the IP.

will be done with the help of the survey team and using adjustment mechanisms on the support structures (Rotating Table and Support Cradle).

The Support Cradle will have a matching rail system that will be connected to the inner warm vessel tracker support rails for continuity. After the mechanical connection of both rail systems, the tracker will be moved on the rails into the calorimeter bore. The insertion stroke is about 7,000 mm (see Figure 21.12).

The rails are acting as a guide and as the support of the tracker during its insertion. The tracker translation is foreseen to be motorised, to control the insertion force, position, speed and acceleration. The rail system has the advantage to reduce the ITk dynamic envelope during its insertion into the calorimeter bore. This dynamic envelope still has to be defined.

The complete insertion mechanism and tooling will be designed to allow both, the insertion and the extraction of the tracker. This means in particular that it will be designed to move

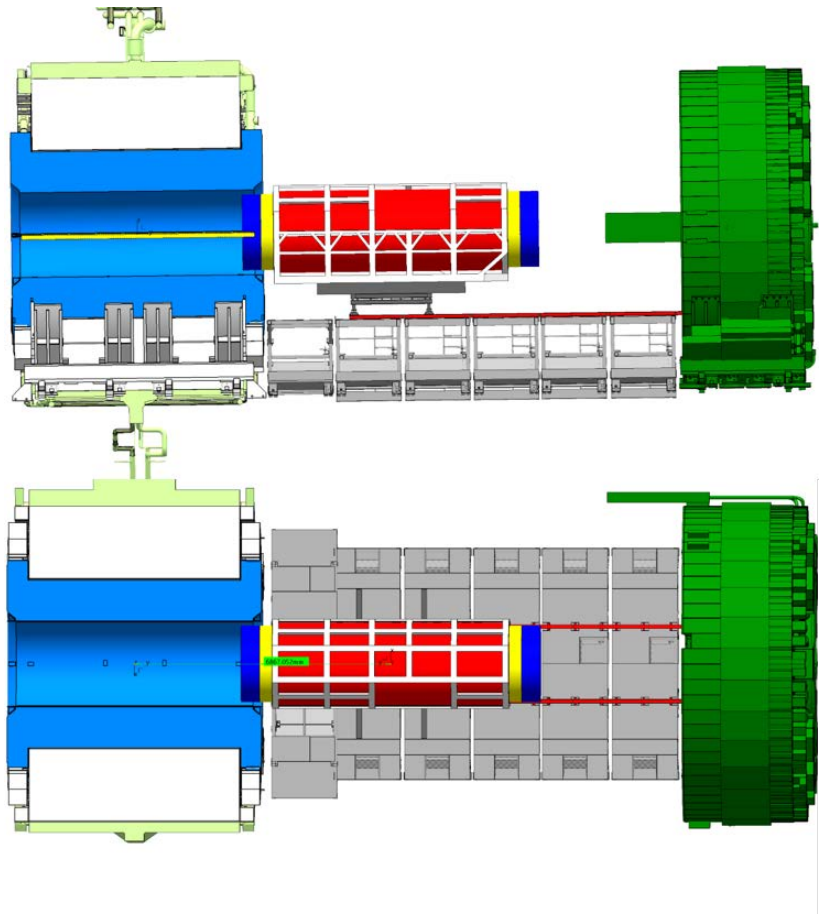


Figure 21.11: ITk ready for insertion (Position 3) at about 7000 mm from the IP.

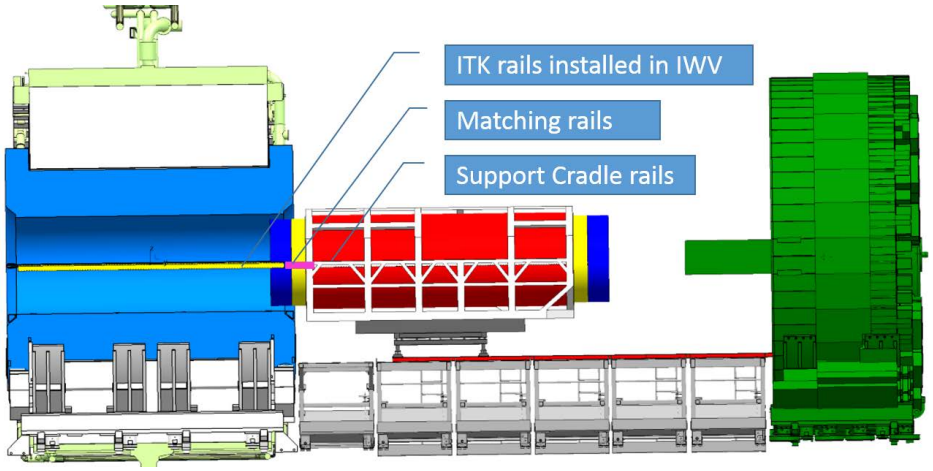


Figure 21.12: ITk ready for insertion (position 3) at about 7,000 mm from the IP with matching rails.

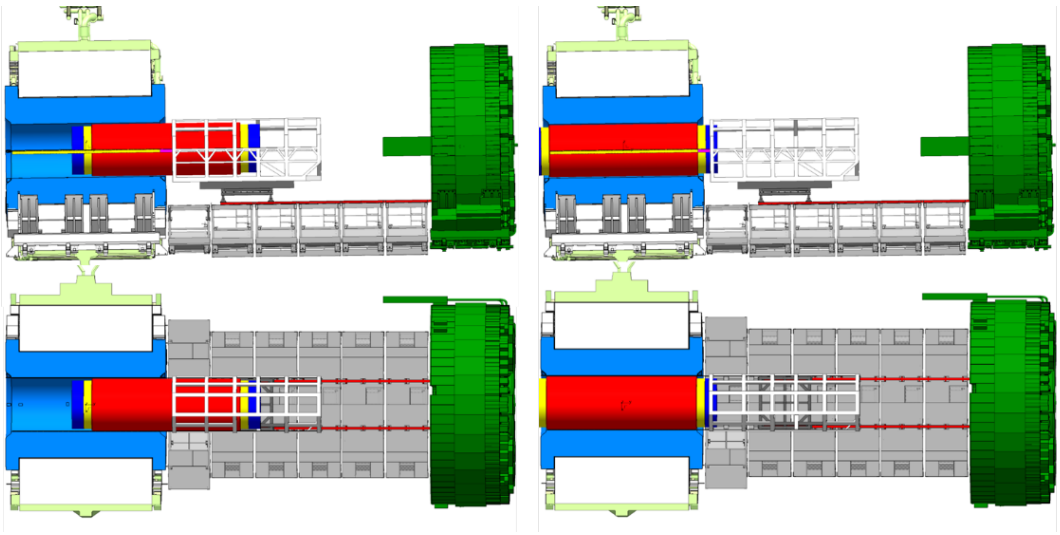


Figure 21.13: ITk insertion into the inner warm vessel.

the detector towards or against the ATLAS beam slope of 0.708 degrees.

The insertion tooling will be motorised to control the insertion speed, the acceleration but also to control the power consumption of the stage. For all parameters, maximum acceptable values will be set and once reached the movement will be stopped. The threshold values will be adjusted during commissioning work with one mock-up on the stage. In particular the power consumption will be optimised to detect any holding points or conflict during the insertion or extraction operation.

The ITk final position is defined in the following way:

- In z (along beam axis) the translation movement is stopped when the tracker reaches its target operating position (given by the survey team). To guarantee no movement over time, the tracker is fixed to the calorimeter. The geometry of the fixations on Side A or C and their position on the OC shall be decided in conjunction with the internal architecture and fixation points of the different ITk sub-systems.

- In Y (vertical) and X (horizontal) the positioning is done at the assembly stage by the vertical and horizontal positioning of the interfaces (V-shape rail and Flat-shape rail as well as the position of support wheels with respect to the tracker). Therefore no adjustment is foreseen during the insertion of the tracker into the calorimeter bore.

21.5 Radioprotection and Personal Safety during Installation

As for any activity on the CERN site concerned by radiological risk, the radiation protection ALARA (As Low As Reasonably Achievable) principles will need to be implemented [165, 166].

Those guiding principles are:

- Justification,
- Optimisation,
- Limitation.

To do so, the ITk-Strip Project Leader will need to ensure that the ALARA process is followed according to the General Safety Instruction [167]. The first step of the ALARA process will consist of a Provisional Interventions List (PIL) made in collaboration with all potentially intervening parties. As the installation of the ITk will occur during long shutdown LS3 the process will start the latest during LHC Run 3.

To establish this list, each intervening group will provide the following information:

- Short description of the intervention
- CERN group responsible of the intervention
- Description of the status of the intervening personnel: external company, Member of Personnel
- Information on the location of the intervention
- Estimation of the intervention duration
- Estimation of the expected dose to people based on simulations

Once the Large Experiment Group Leader in Matters of Safety (LEXGLIMOS) of ATLAS and Radiation Safety Officer consider the Provisional Interventions List sufficiently documented, they will contact the CERN Radiation Protection group, as well as the intervening parties to determine the radiological nature of the interventions. The interventions can be qualified as permanent, repetitive or unique.

In the case of the ITk-Strip installation the interventions will be classified as unique. The interventions will also be classified according to a radiological criteria: level I, level II or level III mentioned below and mentioned in the reference document General Safety Instruction [168]. The classification is indicated in Figure 21.14.

The ALARA process to be followed will depend on this qualification. The Radiation Protection service will inform the intervening parties about the expected content of the file to be provided for interventions in a radioactive environment, in French Dossier d'Intervention en Milieu Radioactif (DIMR).

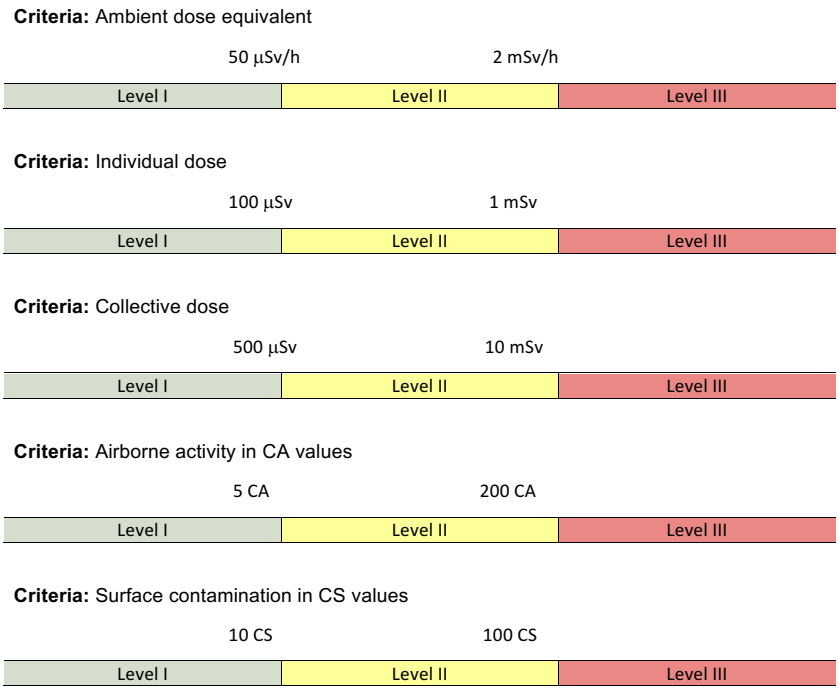


Figure 21.14: Radiation level classification.

Level I and II are not submitted to the ALARA committee, only level III intervention shall be approved by the ALARA committee as mentioned in the General Safety Instruction [169]. DIMR Level I and II will be prepared and discussed between the intervening parties, the ATLAS LEXGLIMOS, the RSO, and a representative of the radiation protection service several days before the start of the intervention. Discussions will be organised regularly all along the intervention with the presence of the representatives listed above. Before any intervention, the DIMR shall be approved. An intervention cannot start without an approved DIMR.

22 Access Scenarios and Configurations

Access to the ATLAS detector can only occur in breaks in LHC operation called stops. Several different kinds of stop are identified each of which can correspond to different kinds of access and configurations of the ATLAS detector. The four kinds of LHC stops are:

- Short access – few hours stop, primarily for LHC machine interventions.
- Technical Stop – one week maintenance for experiments and the LHC.
- Year End Technical Stop – regular maintenance for about 12 weeks.
- Long shutdown – large upgrade or consolidation programs for Experiments and LHC Machine, typically 2 years long.

The ATLAS detector configurations corresponding to these LHC machine stops are described below. In each case, the access to the experimental cavern is preceded by a radiation survey that measures the radiation level at multiple locations where activities are foreseen.

22.1 Short Access

A Short Access is typically a few hours long and they are usually announced on very short notice. Access to the cavern is usually provided immediately after machine stop, provided that the measured level of radiation is acceptably low. This last point will be very significant in the HL-LHC period because it may severely limit the scope of the work carried out during the intervention, especially in the area around the toroidal magnet. The detector RUN configuration is maintained, the magnetic field stays usually ON, no detector movement is allowed and the crane is not available. Access is possible through the existing gangways, with severe restriction to the toroid area because of the intensity of the magnetic field. In particular there is no possibility of direct access to the Inner Tracker; only a few areas, such as some of the PP2 regions or some of the CO_2 cooling manifolds would be accessible during such a short access.

22.2 Technical Stop

The configuration is the same as the Short Access but the magnetic field is usually ramped down. The access to the detectors is still the one allowed in the RUN configuration: no system or detector part is moved. The underground cranes can be used to carry heavy components (mainly related to infrastructure) or to permit access to parts of the detector in the forward region (muon big wheels for instance). However, the access shaft connecting the surface and cavern is not opened. For ITk, it means the maintenance and corrective actions are, again, limited to the ones that can be done at PP2 connections and on cooling system out of the envelope of the detector.

22.3 Standard Opening

The Standard Opening is the default configuration of ATLAS Detector during the Year End Technical Stops (YETS). The magnetic field is turned off; the two shafts connecting the surface and cavern are open so that the surface cranes can be used to lift the forward shielding parts to the surface and to store them in the radioactive buffer zone. The muon big wheels are moved to their parking position, the light trucks are installed to extend the ATLAS supporting rails then the end-cap toroid, muon small wheel and end-cap calorimeters can be moved in a predefined sequence. All of the system movements of are axial, parallel to beam axis. The beam pipe is left in place, but filled with Neon gas at atmospheric pressure. A three meter gap is created between the barrel and end-cap calorimeter in order to provide access to the Inner Tracker and barrel calorimeters. Gaps are also created on one side between the end cap calorimeter and the muon small wheel, on the other side between the muon small wheel and the end cap toroid (see Figure 22.1). Although these gaps are narrow, the construction of temporarily scaffolding is possible, providing access to each of these systems.

To implement this configuration, starting from the running configuration, takes about three full weeks, partially worked in two shifts. The reverse operation at the end of the YETS requires three to four weeks to come back to the running configuration including accurate re-positioning and survey of the systems.

22.4 Large Opening

The Large Opening is the only scenario where the beam-pipe is removed and the extraction of the Inner Tracker is possible. The Large Opening starts the same way as the Standard Opening. However, after the big wheel is moved and the forward shielding has been removed, the beam-pipe is progressively dismounted and brought to the surface so that the light truck, with the end cap toroid on top of it, can be moved perpendicular to the beam

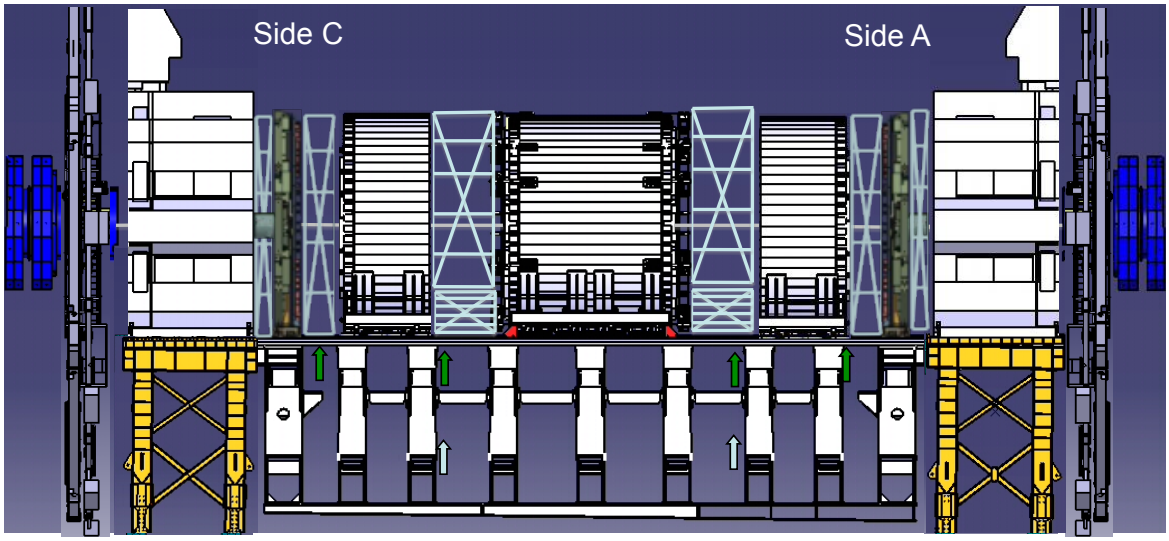


Figure 22.1: Layout of the Standard Opening configuration. The beam-pipe stays in place. The End-Cap Toroids are moved onto the light trucks. Scaffoldings are constructed to access the barrel calorimeter and inner detector, and the End-Cap Calorimeters and the Small Wheels.

axis. The heavy truck is installed to extend the ATLAS rails, the small wheel is lifted to the surface and stored in the radioactive buffer zone, after having been moved on the heavy truck and fully disconnected from services. In order to make the insertion (or extraction) of ITk possible, the end cap calorimeter has to be moved as far as possible away from the Interaction point (see Figure 22.2) and the environment has to be prepared as described in Section 22.2.

About ten weeks are required to get ATLAS detector is Large Opening configuration. The closing process takes even longer and is more complex because of the necessity to bake-out of the vacuum chambers. For this reason, the Large Opening configuration can only be foreseen during Long Shutdown of the LHC (or LH-LHC) machine.

22.5 Constraints related to ITk Maintenance

From the description of the access scenarios, it is clear that any ITk maintenance requires at least a standard opening. However, some additional aspects make this scenario very challenging, thus the large opening configuration is the final baseline for any serious intervention on the ITk.

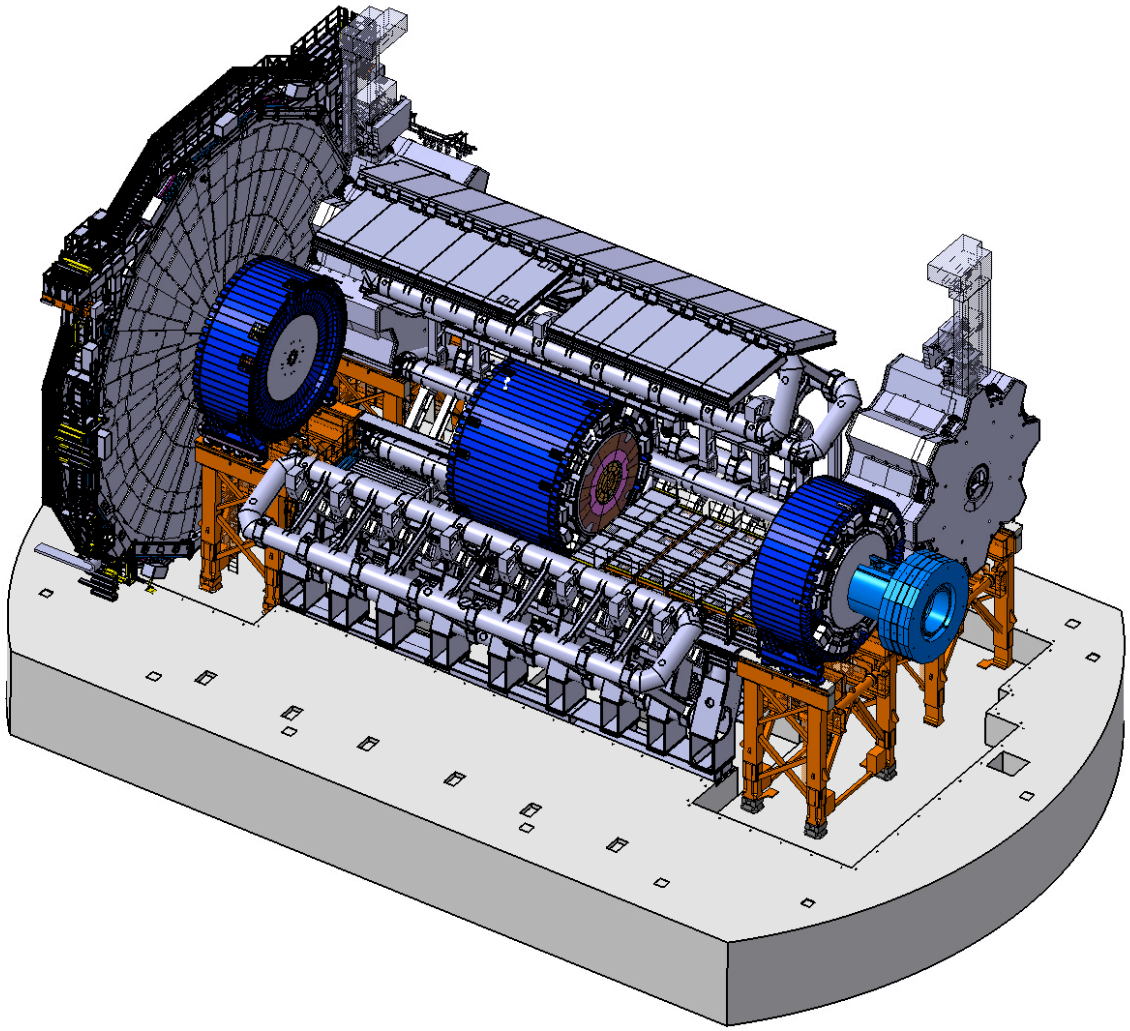


Figure 22.2: Large Opening configuration. The beam-pipe has been removed. The end-cap toroids, supported by the light trucks, are moved to the garage position. The small wheels have been lifted to the surface and the end-cap calorimeters are moved as far as possible away from the interaction point.

22.6 Constraints related to ITk Maintenance

From the description of the access scenario, it is clear that any ITk maintenance requires at least a Standard Opening. However, there are additional aspects making this scenario very challenging, so that the Large Opening configuration is the baseline of any significant intervention on ITk.

22.6.1 Standard Opening

In the LHC context, every Year End Technical Stop (YETS) is preceded by one week of technical stop potentially followed by a heavy-ion run of four weeks, which, from the viewpoint of radiation, can be seen as an extended period of cooling down. Taking into account the minimum period of three weeks needed for the opening process, it is reasonable to assume that access to Inner Detector is only possible after about 56 days of cooling time. For ITk, this assumption is only valid as long as a Heavy Ion run is part of the HL-LHC program, that is to say up to the Long Shutdown 4 (LS4). After LS4 the cooling time will only be about 28 days before the access is available. Simulations have been performed for this configuration for different run periods and for different cooling times. The initial analysis shows that the decrease of the cooling time from 56 to 28 days after LS4 results in an increase of the radiation dose by about 24%, with a peak dose at 190 μSv/h at 40 cm of the ITk. This level of radiation dose is much higher than the threshold defining the simple controlled area (50 μSv/h), therefore the work duration will be severely limited. Because there is no handling facility at the inner gap, only rather simple scaffolding can be built to access ITk, without any possibility of installing significant shielding.

Moreover this configuration is very limiting because

- It does not allow the installation of tooling heavy enough to extract any part of ITk
- The beam pipe is still present and makes it impossible the extraction of any part of ITk
- Even if it were possible to dismount partially the beam pipe, the duration of YETS is hardly compatible with such a process that will require a full bake-out of the vacuum chamber.

Maintenance activities during YETS will be extremely complicated and certainly limited to easily accessible components like connectors or fittings.

22.7 Large Opening

The Large Opening configuration can only be achieved during Long Shutdowns. The minimal cooling time is about 70 days, but the duration of the shutdown is not a restriction if we assume a cooling time of 84 days at least. At that time, the level of radiation dose is about 83 μSv/h, with a peak at 112 μSv/h very close to the beam pipe. This level of radiation dose is still higher than the threshold defining the simple controlled area and so the work duration will be strictly limited. In order to create an environment more appropriated for intricate and time consuming work that would be involved in the extraction of entire ITk or the inner pixel layer several solutions can be studied:

1. Longer cooling time: after about one year, the radiation at 40 cm from the ITk Detector is under the threshold of 50 μSv/h.
2. Installation of shielding: the configuration is compatible with the use of the crane and the minivans. The access platforms installed in the Large opening configuration can withstand the load of additional shielding.
3. Remote handling: it is certainly the most difficult and costly option to develop, nevertheless this option will be studied when the activities are better defined (including procedures and tooling) or when scenarios are identified that the first two options cannot solve.

The most challenging intervention scenario that might need to be carried out in Large Opening configuration is the replacement of the inner pixel layers during a Long Shutdown. The development of a detailed plan for this intervention requires a more precise knowledge of the residual radiation levels. As described in next section, new studies based on the ITk detector geometry and the realistic LHC luminosity profile have been produced and will be calibrated with measurements performed during the coming extended YETS. These radiation studies will be completed in the early months of next year and will be documented in the ITk pixel TDR.

22.8 Considerations concerning the Radiation Simulations

Simulations of the expected ambient dose equivalent rate H*(10)[1)] close to the ITk during long shutdown LS4 and LS5 were produced using the multi-purpose Monte Carlo particle transport and interactions code FLUKA [14, 170]. FLUKA can simulate the propagation and interaction in matter of about 60 different particles and their anti-particles, including photons and electrons from 1 keV to thousands of TeV, hadrons of energies up to 20 TeV (up

[1] H*(10) = standard quantity that it's used to evaluate the potential effects of penetrating radiation on humans. Given a certain radiation level It represent the dose equivalent in Sievert that would be found 10mm inside of a sphere with a composition similar to the one of the human body.

to 10 PeV by linking FLUKA with the DPMJET code). Neutrons can be transported down to thermal energies. FLUKA further allows the generation and transport of decay radiation (limited to gamma, beta-, beta+, x-ray and conversion electrons emissions).

For calculation of residual activities, FLUKA uses an exact analytical implementation (Bateman equations) of the activity evolution during irradiation and cooling down for arbitrary irradiation conditions. As a consequence, results for production of radioactive isotopes, their time evolution and residual doses due to their decays can be obtained for an arbitrary number of decay times and for a given, arbitrarily complex, irradiation profile.

Ambient dose equivalent rates are calculated by folding the particle spectra emitted from the decaying isotopes with energy dependent fluence to effective dose conversion factors [171]. In all cases, the generated gammas are transported in the same way as all other photons in FLUKA, using continuous cross sections and an explicit and detailed description of all their interactions with matter. The irradiation profile used in the simulations is based on the maximum operational scenario for pp collisions provided by the HL-LHC project team in July 2014. To calculate the equivalent beam-time and number of pp-collisions per second, 75% of the peak luminosity was used as average luminosity for simulations until LS3. After LS3, levelling of the luminosity was assumed and 100% of the peak luminosity was used. The ambient dose equivalent dose rate was scored using cylindrical scoring regions assuming symmetry in the azimuthal rotation, to increase statistics while reducing computing time. Only proton runs were considered as ion runs are presumed to contribute only minor to the total activation.

Simulations were based on the current ATLAS Detector geometry. The detector irradiation was simulated with the complete detector in closed position. The cool-down simulation was performed independently for individual detector elements, re-defining any other element of the FLUKA description of ATLAS detector as vacuum. The contributions of each detector element to the total radiation dose, for each of a set of cool-down periods were derived in this simplified way. This data were then re-combined to compute the total activity in the detector for different opening scenarios, after moving the different detector elements to their position in the corresponding scenario.

Measurements performed during the various openings have shown that this simulation method consistently produced estimates of radiation levels exceeding the measured ones. This is believed to be largely due to the underestimation of the shielding effect of different detector components, due to the simplified derivation of their contribution to the total radiation activity. Given these experimental observations, it is considered to be safe to use those estimates as a basis for initial intervention studies.

A new campaign of simulation has been launched recently. It is still based on FLUKA, but assumes

1. the final LHC luminosity profile described in the HL-LHC TDR [172]
2. an up-to-date detector description of the ITk.

In addition the new simulation method computes the activity in the cool-down period by displacing, at the end of the irradiation period, the different detector elements to their position in a given opening scenario, and by simulating the resulting dose with all elements in place, thus taking into proper account the shielding effect that was neglected in the initial estimates. Results from this new simulation campaign are already available for the various Long Shutdowns following the LS3 and for the standard opening scenario.

The new simulation method will also be used to derive the radiation levels expected in the coming extended YETS, given the current detector geometry and the observed machine activity. These predictions will then be used to validate the simulation approach by comparing them with actual measurements performed in selected areas during the opening period. Once validated the new method will be systematically used to derive the baseline assumptions for any future intervention study.

23 ITk Management

The management structure of the ITk is presented in this chapter. The definition and structure of the major sub-projects and other key groups and committees, how they relate to one another, as well as interdependencies within the ITk, with the rest of ATLAS and beyond are described. The four-level technical review process is also presented. The review process is structured to guarantee components and systems meet the requirements. It is aligned with the standard ATLAS upgrade review structure.

23.1 Upgrade Project Organisation

The highest-level executive body in ATLAS is the Executive Board, chaired by the Spokesperson with the Technical Coordinator as deputy chair. The overall steering and monitoring of the upgrade activities is delegated to the Upgrade Steering Committee, which is a subcommittee of the Executive Board with an extended membership. The Upgrade Steering Committee is chaired by the Upgrade Coordinator. The management of approved Upgrade Projects rests with the Upgrade Project Leader of that Upgrade Project, acting together with a steering group and with the Institute Board chair.

23.2 The ITk Project Overview, the Role of the ITk Project Leader and the ITk Steering Committee

The ITk Project Leader is responsible for ensuring the successful design, construction, integration and commissioning of the ITk tracking detector, and for ensuring that the ITk meets all the requirements of the ATLAS physics programme at the High Luminosity LHC. The ITk Project Leader is assisted by a steering group, the ITk Steering Committee. The ITk Project Leader reports to the Upgrade Coordinator and Upgrade Steering Committee during the design and construction phases. Unlike other ATLAS Upgrade Projects, the ITk will continue as a separate subsystem of ATLAS after the construction is completed, and thus the ITk Project Leader will continue through into the operation phase, then reporting directly to the Executive Board as for the other systems of ATLAS. Further reporting to the project community is provided in Institute Board meetings (Section 24.2.1) and in periodic general plenary meetings of the ITk Project. The ITk-PL is a member of the Executive Board.

The ITk construction is organised into four sub-projects: Strips, Pixels, Common Mechanics and Common Electronics. Each of these sub-projects is led by a project leader or one or two coordinators. The sub-projects each cover the construction and integration of a well-defined part of the ITk. Each sub-project operates with a substantial degree of independence, with its own coordinating structure, and also as part of ITk as a whole. The Strip and Pixel sub-projects are relatively self-contained. The Common Mechanics and Common Electronics sub-projects have a large number of interfaces and interdependencies with systems and organisations in the rest of ATLAS. This is reflected in their organisational charts. All four sub-projects have their own working group meetings with attendance appropriate for the topics under discussion. The organisation and function of each of the sub-projects is described in more detail in Sections 23.4 – 23.7.

The top-level organisational structure and reporting lines of the ITk are summarised in Figure 23.1. The Project Support Office supports the four sub-projects.

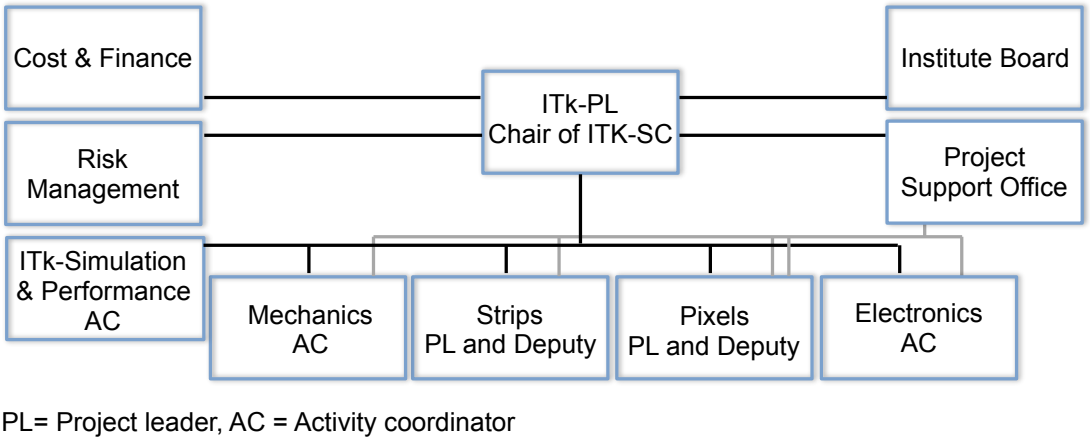


Figure 23.1: The top-level organisational structure of the ITk project, showing the major construction sub-projects and associated activities, committees and groups, as described in the text.

23.2.1 ITk Steering Committee

The ITk project is managed through the ITk Steering Committee. It is chaired by the ITk Project Leader. The ITk Steering Committee is the management and steering body of the ITk, ensuring the overall coherence and following closely the progress of the work. It includes the leaders of the major parts of the project, with membership including:

- The Pixel project leader
- The Strip project leader
- The Common Mechanics coordinator

- The Common Electronics coordinator
- The Simulation and Performance group coordinator
- The Risk Management Committee chair
- The ITk Resources Coordinator, representing the Costing and Finance group
- The Project Support Office leader.
- Further ex-officio members from outside ITk are also included in the ITk Steering Committee, specifically the Upgrade and Technical Coordinators.

Additional members from the different areas may be included to complement the membership, at the discretion of the ITk Project Leader. The membership of the ITk Steering Committee is endorsed by the ITk Institute Board described below.

23.2.2 Selection Procedures for Leadership Positions

The selection of the leaders of the different parts of the ITk project are handled differently depending on the type of work, and the associated community. The ITk Project Leader and the Project Leaders of the Strip and Pixel sub-projects are elected or endorsed by the ITk Institute Board, following a search process carried out by a search committee taking input from the ITk community, according to established ATLAS practice. The activity coordinators and leaders of Common Mechanics, Common Electronics and Simulation and Perfrmance are chosen by the ITk Project Leader in close consultation with the Strip and Pixel Project Leaders, and endorsed by the ITk Institute Board.

23.3 The ITk Institute Board

The ITk Institute Board has one voting member from each of the ATLAS institutions participating in the ITk project, currently numbering around 100. The institutional membership will, after the completion of the ITk construction MoU addenda, correspond to the set of ATLAS institutions which are contributing to the ITk construction. Resources (financial and human) for ITk construction, and later operation, flow from the institutions, and thus the ITk Institute Board is the main decision-taking body for all major questions involving sharing of resources and responsibilities within the ITk project (including resolving any gaps in the coverage of deliverables). The ITk Institute Board will also be called upon to endorse major technical choices: such decisions will normally be formulated by the project/subproject management, and brought to the Institute Board for endorsement. The ITk Institute Board also organises the elections of the project leaders, who serve a two year renewable term of office. The Project Leaders for the Strip and Pixel sub-projects are elected or endorsed by a subset of the ITk institutions who work in those areas. The ITk Project Leader

is elected/endorsed by the Institute Board members from the entire ITk community. The ITk Institute Board is a unitary body that covers the entire range of activity of the ITk. The ITk Project Leader maintains close connection with the ITk Institute Board through regular presentations at the ITk Institute Board meetings, and regular communications with the Institute Board chair. The ITk Institute Board chair is elected/endorsed by the ITk Institute Board voting members for a two-year renewable term.

23.4 Pixel Sub-Project Organisation

The present Pixel management organisation is shown in Figure 23.2. Pixel activities are coordinated by the Pixel Steering and Design Group chaired by the Pixel Project Leader. The Pixel Project Leader also appoints a lead engineer who is a member of the Common Mechanics group, and develops and maintains the work breakdown structure and many aspects of the schedule. Given the number of ongoing R&D activities within the Pixel subproject and the need to converge to a well-defined baseline for the Pixel TDR at the end of 2017, the present Pixel organisational structure has been built to control the discussion between different R&D lines, define the parameters and the benchmarks that will be used to evaluate different solutions and, in general, facilitate the definition of a common design supported by the entire community.

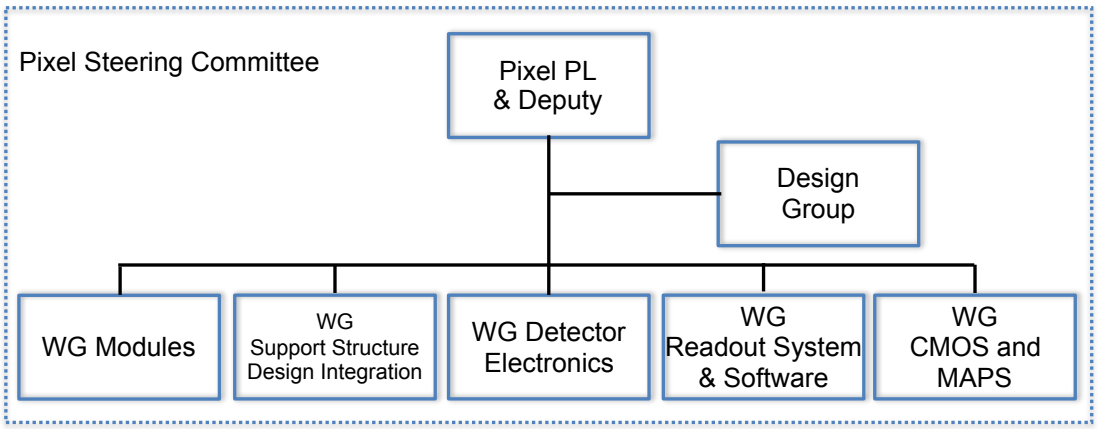


Figure 23.2: Organisational Chart of the Pixel Project.

Another important task of the Pixel Steering and Design Group is to keep close contacts with common ITk working groups (Mechanics and Electronics). The Steering and Design Group coordinates the activity of five Pixel working groups dedicated respectively to module design (sensors, front-end electronics, hybridisation and assembly), local support and integration (including service routing), Off-Detector Electronics and controls, readout system and software. The possible use "smart" CMOS sensors or even Monolithic Active Pixel Sensors in the Pixel Detector is covered in its own working group. The coordinators of

the Design Group, the coordinators of the five working groups, the Project Leader and the Deputy Project Leader form the Pixel Steering Group. The Design Group organises regular open meetings devoted to general design issues, while specific technical discussion happens in the regular meetings organised by the working groups. This structure will be reviewed after the Pixel TDR.

23.5 Strip Sub-Project Organisation

The Strip sub-project organisation is shown in Figure 23.3. The activities are coordinated by the Strip Project Leader through the Strip Steering Committee. The ITk strip sub-project is sub-divided into eight activities. The activities are formulated so that they combine barrel and end-cap parts of the detectors, to ensure coherence between the two regions. The Strip Project Leader also appoints a lead engineer who is a member of the Common Mechanics group, and develops and maintains the work breakdown structure and many aspects of the schedule.

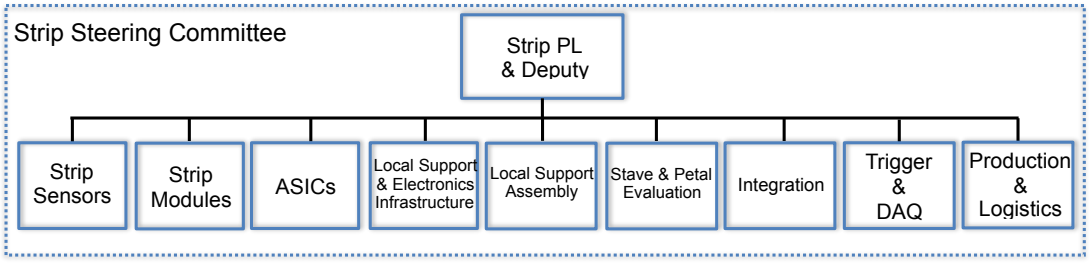


Figure 23.3: Organisational Chart of the ITk Strip Project.

The sensor group covers all tasks around the sensing element, addressing the standard silicon sensor approach. The module group controls all elements which are necessary to make a module, from the readout chips on the hybrids, the hybrid development and the actual module development including aspects of production. The local support electronics and infrastructure group connects the modules over bus-tape to the off-detector power supplies. The on-detector powering (LV and HV) is also part of this activity. The local support assembly group controls the research and development required for the cores supporting the modules. This includes thermo-mechanical FEA, material qualification as well as the assembly and test of the staves and petals. The stave and petal evaluation activity includes all testing from electrical tests to thermal tests of stave or petal prototypes. Test beam, quality control and quality assurance are also part of this task. The overall integration of the detector from space frame to alignment as well as insertion tooling is covered in the integration activity. The production and logistics group is preparing the production of the ITk Strip Detector in discussion with all involved institutes. This includes understanding part production rates and person power estimates as well as preparing schedules for the remaining R&D phase and the production phase.

23.6 Common Mechanics Sub-project Organisation

The organisation of the Common Mechanics activities is shown in Figure 23.4. The Common Mechanics group is made of six working groups. It is co-coordinated by the ITk lead engineer, and a physicist.

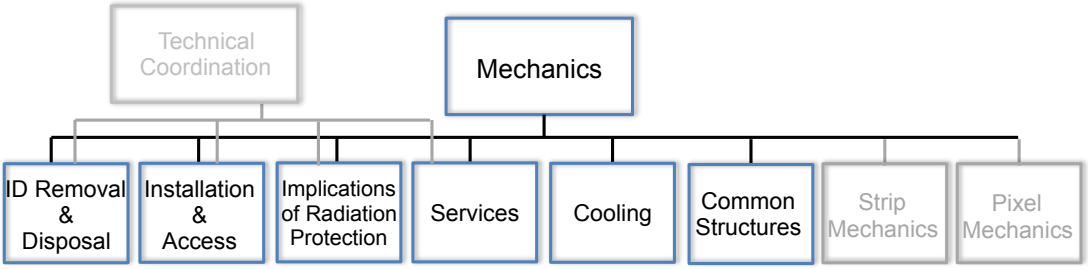


Figure 23.4: Organisational Chart of the ITk Common Mechanics Group.

The Inner Detector removal and disposal is the working group which is charged with developing the techniques for the safe removal of the existing Inner Detector from the ATLAS detector and preparation of the cryostat for the safe and rapid installation of the ITk. The Installation and Access working group prepares for the installation of the ITk and works through the access and maintenance scenarios and the decommissioning of the ITk at its end of life. The Implications of Radiation Protection working group works to understand the constraints that will be imposed on all aspects of the design, installation and access from activation. The services group looks after the servicing of the detector with: LV, HV, optical fibres, gas and cooling. The cooling working group will design, prototype and control the manufacture of the cooling system. The common structures group will provide the global supports, outer cylinder and thermal control and interface with the rest of the experiment.

All of the activities in the Common Mechanics group must be strongly coupled to the Strip and Pixel sub-projects. They must also be strongly coupled to Technical Coordination and there is one co-convenor from the technical coordination group in each ITk Common Mechanics working group. The Common Mechanics group also provide common standards for the design, construction and review of the mechanics. They will also provide guidance on the required alignment and stability of the detector in construction and operation.

23.7 Common Electronics Sub-project Organisation

The organisation of the Common Electronics and Readout group is shown in Figure 23.5. The group is coordinated by the ITk Common Electronics coordinator. The Common Electronics group serves as a single point to provide several functions across the entire ITk:

Common ITk components

These include: Off-Detector, Detector Control Systems, Environmental control and Monitoring and common ITk level guidance on grounding and shielding. These common components also have interfaces to other ITk groups including: Common Mechanics, Cooling and structures.

Common ITk oversight

This includes guidance on: quality control, quality assurance and standards, specifications validation, radiation qualification (Total Ionising Dose, bulk damage and Single Event Upset Studies) and the Common Electronics group will coordinate ITk level electronics reviews.

Sub-detector Components and Interfaces

Within both Strip and Pixel groups there are a series of common interfaces or components. The Common Electronics organisation will provide support and interfaces in these areas. These include: sub-detector readout architecture, data transmission, power (LV and HV), DCS, modules, ASICs, TDAQ, End-Of-Structure-Cards, opto-links etc.

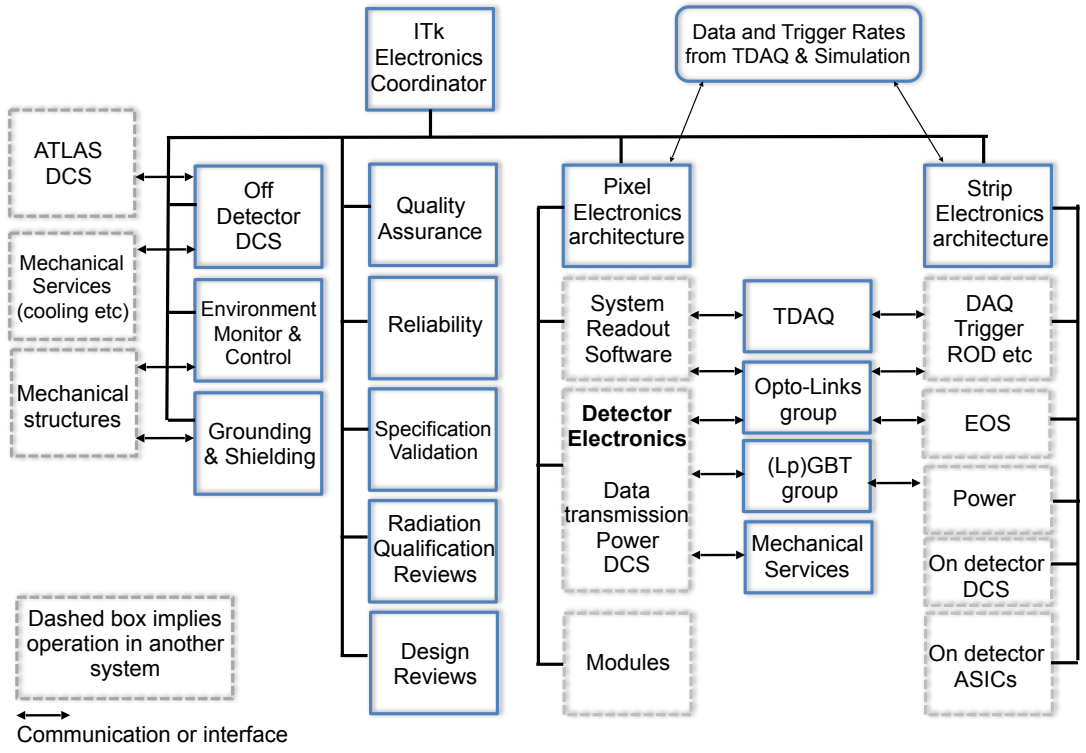


Figure 23.5: Organisational Chart of the ITk Common Electronics Group. The chart shows the complex interdependencies between Common electronics and the Strip and Pixel groups.

23.8 Simulation and Performance Group

The work of the ITk Simulation and Performance group is a critical activity and the ITk simulation and performance group maintain close connections to the existing ATLAS tracking performance group. Prior to the Strip TDR and up to the submission of the Pixel TDR the simulation and performance group has been augmented with the Layout Task Force, with a particular focus on finalising aspects of the tracker layout. Both the simulation and performance group and the Layout Task Force have strong connections to the Upgrade Physics group to provide insight on the role of the performance of the ITk in the exploitation of Phase-II physics. The simulation group also reviews the radiation calculations (ionising and non-ionising) that are a critical input to understanding of the radiation tolerance of detector components and its impact on the detector design. The work of the ITk Simulation and Performance and Layout groups is reported at ITk Steering Committee meetings. The Simulation and Performance group also relies heavily on tracking reconstruction code that is maintained and developed by the upgrade tracking group. The structure of the different groups that are currently contributing to the understanding of the performance of the ITk and how they relate to one another will be reviewed and refined after the TDR.

23.9 Risk Management

The process of risk management adopted in the ITk is explained in Chapter 25. Risk management will be conducted by a Risk Management Committee reporting to the ITk Steering committee, whose responsibilities include the identification and analysis of risks, the development of mitigation plans where appropriate and regular monitoring of tracked risks and response plans. The ITk Risk Register, containing a concise analysis of risks, will be maintained by the Project Support Office.

23.10 ITk Costing and Finance Group

Costings and finances are reviewed by the ITk Costing and Finance group. It is chaired by the ITk Project Leader and includes costing experts from the ITk sub-projects, related projects (like TDAQ), and members of the wider ITk community with strong connections to the funding agencies. An ITk Resources Coordinator tracks the spending on common R&D projects and reports to this group, to the ITk Steering Committee, and to the Institute Board. As the project moves into the construction phase, the Costing and Finance group will track the spending of the different sub-projects. The management of ITk funds, establishing contracts, and MoUs are also done in close cooperation with the ATLAS Resources Coordinator.

23.11 The ITk Project Support Office

The ITk Project Support Office serves to support the day-to-day activities of the construction sub-projects of the ITk: Pixels, Strips, Common Mechanics and Common Electronics. The office will perform this function throughout the R&D, prototype and design stages and into bulk component production. At the end of construction phase, the scope of the office will be re-examined. The Project Support Office also supports central tools, procedures and protocols required for the execution of the projects. The office does not duplicate functions that are carried out in the ATLAS Technical Coordination Upgrade Project Office. It works closely with the Upgrade Project Office adopting common standards and practices. The ITk Project Support Office reports directly to the ITk Project Leader through the ITk Steering Committee.

The ITk Project Support Office is virtual in the sense that it is not physically based in any one location. It is staffed by a small team of people organised by a physicist. The ITk Project Support Office meetings are attended by Project Leaders, lead engineers from each sub-system, key activity coordinators, representation from Technical Coordination and a core of individuals who are implementing the actions mandated by the office.

Some of the key functions of the ITk Project Support Office are listed below.

Drawing and CAD model maintenance
Maintain common point of support for ITk drawings, definition of common standard, lists of drawings including status (provide easy access to EDMS, CDS and other document servers from a common ITk webpage).

Maintenance of EDMS space and documents
Control of access, making sure documents are up to date
Maintain lists of documents in EDMS from the ITk webpage

Maintenance of ITk WBS and work package information
Maintenance of the documents related to the ITk WBS, WBS dictionaries and work pages, links from the ITk webpage. Documents related to the description and scope of these activities.

Preparation and schedules of internal ITk reviews
Scheduling and review preparation
Collection of inputs and distribution to reviewers ahead of time.
Presentation of material in a single place including review reports and follow up action items.

Maintenance of the official master ITk Schedule
Collection of inputs (MicroSoft projects) from: Strips, Pixels, Common Mechanics, Common Electronics.

Construction and integration of subparts from ITk and Technical Coordinator into a MicroSoft-project master for things like installation etc.
The ITk Project Support Office should give the ITk Project Leaders warning of the approach of upcoming deadlines so that progress can be monitored and corrective action can be taken to avoid missing milestones and deliverables.

ITk Buildings management
Interacts with Technical Coordination and the sub-projects to ensure the smooth operation of the surface building used for ITk activities.

Other Activities
Together with the ITk resources manager the Project Support Office maintain the spend model and monitor the spend details. Maintenance of the financial risk register. In consultation with sub-systems and activity coordinators maintain information related to component and system reliability testing and documentation.

The list of activities covered by the office will be reviewed regularly.

23.12 Specifications and Review Procedures

In order to guarantee that the ITk meets all of the requirements set out in Chapter 2, all of the components used in the ITk have to pass through a series of reviews before they can be used in the construction of the detector. These reviews are used to control the quality and reliability of the detector and to improve the efficiency of the development process as well as shorten the design cycle. The progress through the reviews is also used to monitor the progress of the project and to make sure it is on track. What is described below reflects a stepwise procedure that is found throughout the ATLAS experiment. Each part is required to pass a given stage before it is allowed to pass on to the next.

These procedures promote the concept that designs are created to meet specifications and specifications are written to meet requirements. An important corollary to this theme is that the interfaces between components that make up a system are critical features of the design that must be understood and guaranteed to work. Therefore, the interface of each component must be an important part of its specification in order to insure that it will function properly in its intended application. Reliability is another feature of each component that must be considered at the time of design and not after the component is built. The issue of reliability must be part of the specification of each component. These procedures do not deal with all the issues of production procurement. Production procurement, especially for large quantity items, will require a production plan and must follow procurement procedures required by the purchasing institution.

Each individual component that will be built into the ITk must have a written specification. System level specifications are needed in addition to specifications that describe individual components in detail. A generic template has been developed for ITk specifications. This template is generic enough that it can be used for all ITk components and assemblies. Specifications for each component are written and approved prior to the start of any serious design work on the component. This makes the design process much more efficient and minimises the need for re-design later. Since many components will be built in technologies new to ATLAS and some characteristics of those technologies, especially their level of radiation hardness, must be evaluated before a final approval of their use can be made, some component design fabrication and testing of test components can be done before formal component specifications are completed.

23.12.1 Specification Reviews

Each specification document must be reviewed and approved by a specification review team chaired by a specification validation coordinator. A key component of the specification is the section on interfaces, which will detail the quantitative characteristics of each interface. These must be checked for consistency with the component which will sit on the other side of each interface. The review should confirm that the specification details how the component will meet the requirements of the detector system of which it will be a part. It should also state what level of radiation, if any, that the device needs to withstand. The required reliability level should also be addressed. Reliability sections "Consequences of Failures" and "Prior Knowledge of Expected Reliability" should be covered as well as possibly the section "Measures Proposed to Insure Reliability of Component and/or System". The Reliability Coordinator should be part of the review.

23.12.2 Design Reviews

Design reviews will be conducted in accordance with the ATLAS Upgrade Review Office. There are three types of design reviews for each component or assembly: the Preliminary Design Review (PDR), the Final Design Review (FDR) and the Production Readiness Review (PRR). A review coordinator will assemble a review committee to include some experts in the relevant technology and also possibly some users of the object to be reviewed or those interfacing other objects to it. A preliminary design review should be held prior to the submission of any prototype design for fabrication or assembly. This would apply to ASICs, printed circuit boards, etc. Under no circumstances will a PDR be conducted without an approved specification for the design to be reviewed. The PDR should focus on whether the design meets all aspects of the specification. For new circuits, simulations should be presented to demonstrate this. Test plans should be presented to show how the prototype devices will be tested to demonstrate functionality that meets the specification. Regarding reliability, the section "Measures Proposed to Insure Reliability of Component

and/or System" should be addressed. The design must pass the PDR with only a small number of follow-up actions prior to submission in order for the submission to go forward. Otherwise, a follow-up PDR must be held and passed.

23.12.3 The Final Design Review (FDR)

When it is believed that a design is final and ready for production, there are two more steps to pass prior to placing a production order. The first is a Final Design Review (FDR). Like the PDR, this review should review all the available data from prototypes to determine how well the design meets specifications. If there have been any changes in the design since the last prototypes produced, those changes must be looked at very carefully, hopefully with full simulations. By this time a fully developed production test plan should be ready and exercised on some of the prototype devices. If the device will operate in a radiation environment, then full irradiation data must be reviewed. Whatever measures have been taken to insure reliability should be reviewed and a quality control plan to validate reliability of design and construction or manufacturing techniques should be defined for review. Once the FDR is passed, a pre-production fabrication or build is clear to proceed. The number of prototype devices produced after each PDR is usually small and is up to the discretion of the project leader. The pre-production fabrication or build must be of a large enough number to provide at least the minimum of meaningful statistics. For a custom ASIC this is typically a full fabrication lot (of order 20 wafers). For a printed circuit board or assembly it should be at least 10% of the full production quantity. A requirement of the pre-production fabrication or build is that nothing in the design or the manufacturing process can change between it and the start of full production.

23.12.4 The Production Readiness Review (PRR)

All the devices produced in the pre-production fabrication or build must be tested using the planned full production test and the quality control plan should be exercised at the planned sampling rate including any irradiations necessary for devices operating in a radiation environment. These results are then brought to the PRR for review. If the test results show acceptable yield to the production testing and an acceptable level of passing the quality control and irradiation tests, the design is cleared for full production. If the device does not pass the PRR and changes are required to the design or the manufacturing process, then the design must return to an FDR after the changes are implemented, followed by a pre-production fabrication or build and then another PRR.

23.12.5 Requirements to Start Full Production

The specification and review processes described in this document complete the technical requirements to prepare a design or a component for full production or procurement. These include having exercised the production test plan and quality control procedures, including having their appropriateness and their results on the preproduction units reviewed. In addition, a full production plan will need to be developed describing ordering procedures and material flow.

Also, CERN has well defined rules concerning the selection of vendors, as do some other institutes. It is essential that the rules of the organisation that is going to perform the purchasing are followed or production orders could be delayed for months or even years. The production plan and the procurement procedures, including the adjudication criteria, should be reviewed early in the development process but no later than at the time of the FDR. As the members of the FDR committee will be chosen mostly for their technical expertise and not their purchasing knowledge, the chairman of the FDR committee should request confirmation that the production plan and the procurement process have been approved by the appropriate purchasing department of the institute responsible for the procurement and by the relevant detector project leader.

23.13 ITk Part Production

The sub-projects of the ITk will manage the production of the different parts of the ITk Detector. The Project Leaders (Strips and Pixels) and activity coordinators (Common Mechanics and Common electronics) are responsible for the planning, execution, delivery and reporting of the production in their area. A Production Coordinator coordinates the overall production flow of the ITk Strip detector together with the Strip Project Leader and the Project Office (see Chapter 13). The Strip Project Leader will report progress to the ITk Project Leader, ATLAS management and LHCC as required, as well as report to the Institute Board. The ITk Project Leader will report regularly to the Institute Board on matters related to resources. The ITk Project Leader also reports to the ATLAS Upgrade Steering Committee. The risk management board also reports to the Project Leader through the ITk Steering Committee.

With such a large and distributed project great reliance will be placed upon the development and maintenance of the ITk production database that was presented in Section 13.5.

24 Schedule from TDR to Installation

In this chapter the schedule of the ATLAS ITk is discussed. Details for the timeline of the production (including purchase of components) and installation of the Strip Detector are given.

24.1 Overall Schedule

The ITk Tracking Detector (in the following the ITk) construction schedule is based around the CERN Medium Term Plan (MTP) for the period 2016-2020, which was presented at the CERN Council session [173] in June 2015. The ITk will be installed during Long Shutdown 3 (LS3) which starts at the end of 2023 and is expected to last for 30 months with colliding-beam operation expected to start in mid-2026. Before the installation of ITk Detector into the ATLAS experiment, the Inner Detector (ID) must be safely removed from the cryostat to the surface and handed over to the Radiation Protection group for consolidation, storage and eventual disposal. The schedule for the removal of the ID and installation of the ITk requires detailed planning with ATLAS Technical Coordination who must take account of the requirements of multiple sub-systems. Preparation is underway within the ID and ITk-Mechanics group to understand the details of the process, the required tooling and personnel and the associated timeline. The ITk is scheduled to be available for installation in the ATLAS pit by Q3-2024 and designed for rapid installation while in the ATLAS cryostat. The combined operation of installation and service connection is assumed to take no more than six months. Furthermore the ITk should be available for commissioning on the surface at point-1 one full year before it is required for installation. This requirement is based on the experience gained with the current tracking detector with intention to minimise exposure to radio activation during or after installation of the ITk (in-situ debugging) and minimise the time to full operation before physics data taking. This means the construction and surface integration of the ITk for testing must be complete before the end of Q3-2023. It is important to stress that any work carried out in the ATLAS detector during this time will be heavily constrained by the radiation environment in the cavern in general and the cryostat in particular. The removal of the Inner Detector is likely to be particularly difficult and the development of the required tooling and training of manpower and procedures will take several years. The removal will be a partnership between the ID, ITk community and ATLAS Technical Coordination.

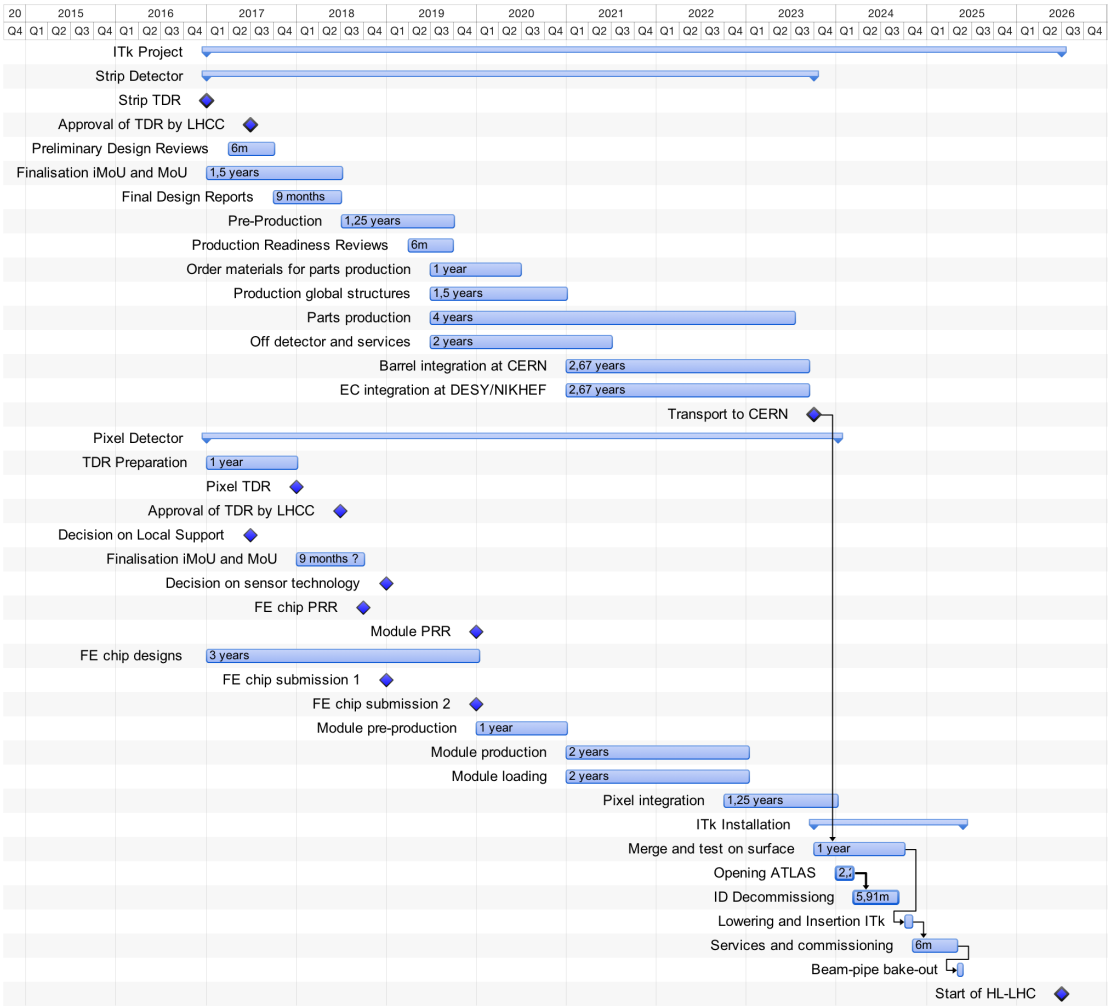


Figure 24.1: Gantt chart of the ITk project.

In Figure 24.1 a high-level Gantt chart for the strip and pixel sub-projects is presented. A more detailed development of the strip project is shown and discussed in Section 24.2. The top part of Figure 24.1 shows the most important blocks of the strip production schedule. The Preliminary Design Reviews of the various detector component will be completed by Q3-2017, the Final Design Reports will span over a 9-month period ending in Q2-2019.

The ordering of the final parts and the one year pre-production period terminate in the production readiness reviews in the middle of 2019. At that stage the orders for the production parts will be released and the 4-year period of bulk production can start. Integration of the detector starts in Q1-2021 and lasts for nearly 3 years.

The lower part of Figure 24.1 shows the high level development of the pixel schedule that will be presented in more detail at the time of the Pixel TDR at the end of 2017. It assumes two iterations of the front-end chip design, module development and testing which is com-

plete in Q3-2019. Module pre-production starts in Q4-2019 and bulk production starts at the end of 2020. Module loading on to staves starts as soon as the modules become available at the start of 2021 and is complete at the end of 2022. Detector integration starts in Q4 2022 and is complete by the end of 2023.

The ITk community will present an ID Decommissioning Chapter that will be part of the Pixel TDR, outlining the procedures for the removal of the ID, taking into account the activated environment, collection and cataloguing of information and tools from the ID installation, and preparation of 1:1 mock-ups of the current ID and its services.

In parallel to preparing final designs and as preparation for the TDR, Market Surveys will need to be launched with CERN procurement to identify potential suppliers for the major cost items that will be purchased through CERN. This will allow greater confidence in the accuracy of the prices for these items in the TDR. It is also important to qualify the potential suppliers for the long lead-time components before the final tendering process. A key difficulty when preparing the specifications that are part of a market survey and tendering process for many of the components that will be purchased for the ITk are the requirements that relate to radiation hardness, which cannot be easily captured in commercial Quality Assurance procedures. This places the burden on the ITk for extensive preparatory R&D followed by demands on the vendors for written assurances that device processing is kept identical to that of pre-production devices built to final specifications which have been through the full radiation qualification process. A qualification phase of early procurement of enough devices to final specifications to demonstrate these requirements is essential given the timescales required for adequate irradiation and test-beam studies. For the Semi-Conductor Tracker of the Inner Detector (SCT), there was a pre-production procurement of a small fraction of the final order with contractual break-points to allow the SCT to be able to withdraw from the purchase in case problems were encountered either in terms of radiation tolerance in sample testing, QA difficulties or delivery schedule issues.

Another issue is that some sensor suppliers require separate early procurement of masks and polished wafers to mitigate cash-flow problems. Following previous procedures, after the TDR, the ITk will place contracts for a pre-production of about 5 % of the total volume with pre-negotiated break points that enable the ITk community or its representatives to terminate the contracts if the parts do not meet the specifications. Pre-production modules also need to be built and tested to the final specifications including a series of irradiation tests. These components are used to: qualify the vendors production procedures, capabilities, ITk reception and quality assurance procedures, streamline the component flow between sites including part-tracking and to bring the production sites through site qualification to production readiness. Based on experience gained during the construction of the ID, it is expected that this process will be time consuming. A slow ramp up to full production is anticipated taking care to guarantee the highest quality of the large number of mass produced parts. This will also be true for the ITk where, for the strips, a significant number of production sites are planned. The pre-production phase indicated on the schedule

covers the pre-production phase after the TDR. Because this phase of the project is so critical it is likely that it will be necessary to collect funds for the qualification of vendors and to pay for the pre-production phase before all of the formal phases of the financial review are complete. This bridging between pre-production and production will require interim Memoranda Of Understanding (iMOU).

24.2 Timeline of the ITk Strip Detector

More details of the strip schedule are presented in Figure 24.2. The main milestones are listed in Table 24.1. For each of the major parts of the Strip Detector the production is grouped into level-3 WBS items (2.2.1 Sensors, 2.2.2 Read-out Chips, 2.2.3 Modules, 2.2.4 Local Support Electronics, 2.2.5 Fully Assembled Local Supports, 2.2.6 Global Supports, 2.2.9 and 2.2.7 Services and Off-detector Electronics). It shows the details of the timing of the finalisation of the specifications, specification review, the Preliminary Design Review (PDR), validations of design, the construction and testing of prototypes, pre-production, the Final Design Reviews (FDR), purchase of materials ahead of production and the Production Readiness Reviews (PRR) ahead of bulk production. The first items to start the production phase are the local support electronics (bus-tapes), the sensors and the front-end ASICs as they are essential for the overall production. Module production starts shortly after with the production of the bare hybrids and subsequently the population of the hybrids with the tested and diced ASICs will follow. The local support cores will start the production when first bus-tapes are available. When the production of the modules and cores is established the loading of modules onto staves and petals will start at the loading sites. The barrel and end-cap global structures need to be produced early in the production phase as the staves and petals will be loaded into the structures as soon as they are fully assembled and tested. Thus the barrel integration starts at CERN in Q1-2021 and end-cap integrations starts in the institutes (DESY and Nikhef). This is complete in Q3-2023 ahead of one year of testing on the surface ahead of installation into the cryostat in Q3-2024.

24.3 Timeline of the ITk Pixel Detector

The ITk Pixel Detector production schedule is determined by two parameters: the availability of module components, fixing the start of the pre-production phase, and the date of the beginning of integration at CERN, when enough of the modules must be ready to commission the process and testing. The time to develop, test and qualify the Pixel front-end chip to make sure it meets all of the design requirements is a key driver of the schedule right up to the start of pixel module production. The end of the module production is dictated by the beginning of ITk detector integration at CERN. Both ATLAS and CMS are engaged in a common development program (RD53) to provide the building blocks required for the

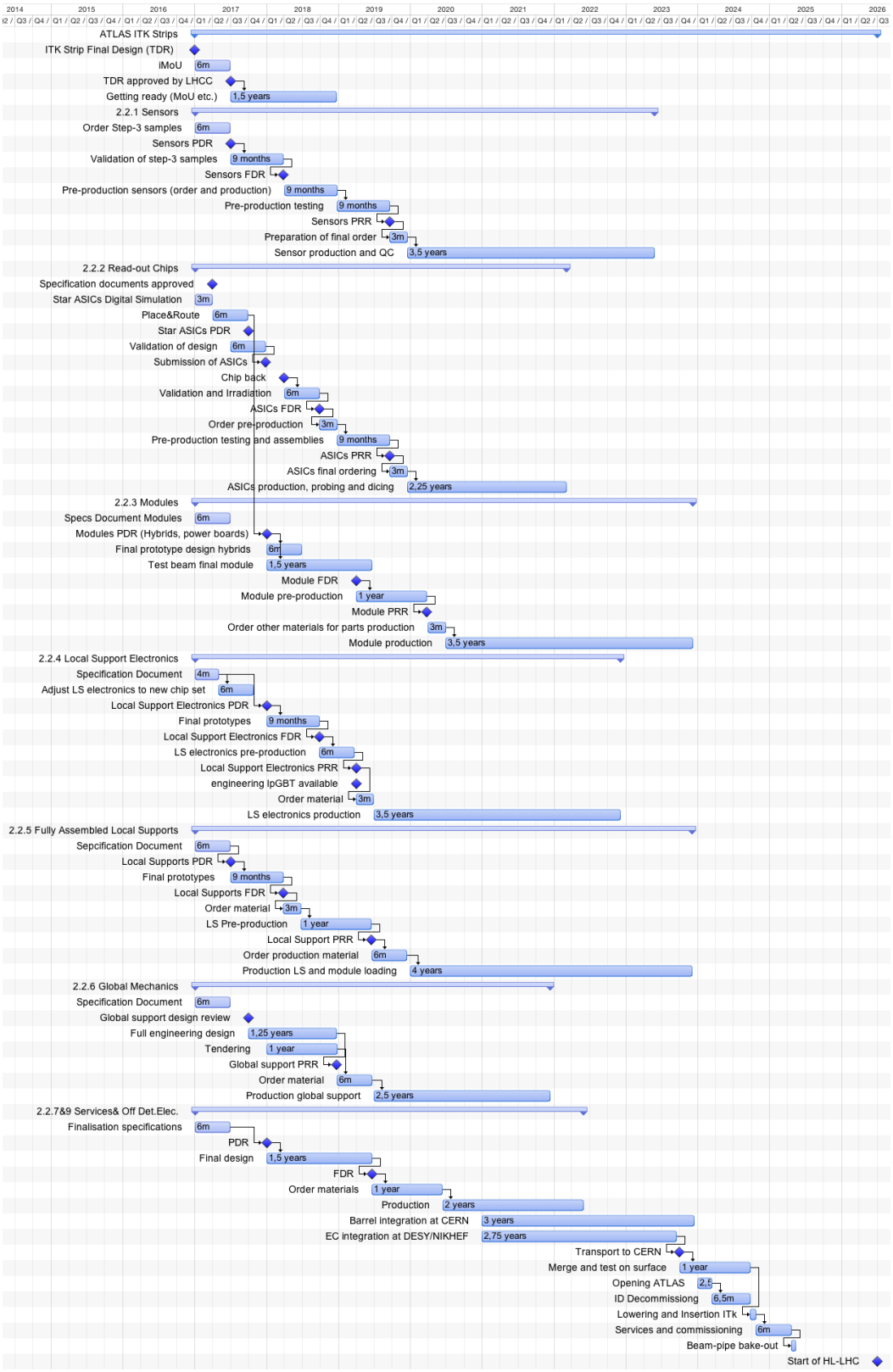


Figure 24.2: Gantt chart of the ITk strip project.

Table 24.1: Milestones for the ITk Strip Detector developments

Milestone	Date
2.2.1 Sensors	
Sensor Preliminary Design Review	Q2-2017
Sensor Final Design Review	Q1-2018
Sensor Production Readiness Review	Q3-2019
2.2.2 Read-out Chips	
Specification Review	Q1-2017
ASICs Preliminary Design Review	Q3-2017
Star ASICs submission	Q4-2017
ASICs Final Design Report	Q3-2018
ASICs Production Readiness Review	Q3-2019
2.2.3 Modules	
Specification Review	Q2-2017
Modules Preliminary Design Review	Q4-2017
Modules Final Design Report	Q1-2019
Modules Production Readiness Review	Q1-2020
2.2.4 Local Support Electronics	
Specification Review	Q2-2017
Preliminary Design Review	Q4-2017
Final Design Report	Q3-2018
Production Readiness Review	Q1-2019
2.2.5 Fully Loaded Local Support	
Specifications Review	Q2-2017
Local support Preliminary Design Review	Q2-2017
Local support Final Design Review	Q1-2018
Local support Production Readiness Review	Q2-2019
2.2.6 Global Mechanics	
Specifications and Design Review	Q3-2017
Global support Production Readiness Review	Q4-2018
2.2.7 Services	
Specifications Review	Q2-2017
Preliminary Design Review	Q4-2017
Final Design Review	Q2-2019
2.2.9 Off-Detector Electronics	
Specifications Review	Q2-2017
Preliminary Design Review	Q4-2017
Final Design Review	Q2-2019

design of a front end pixel chip. This development targets a 65 nm process. Common development chips are already in hand and undergoing evaluation and the initial results are very encouraging. A second RD53 submission (RD53-A) will be in Q2-2017 when ATLAS will embark on a program of module evaluation with this technology. At the same time that the RD53 modules are being evaluated, the design of the ATLAS-specific pixel front-end chip starts; the chip is expected to be fully qualified and ready for the module pre-production at the end of 2019 in the most pessimistic case of two design iterations. Even though the details of the pixel integration procedure are not yet worked out, it is understood that it must start in 2023. It is then required that all the modules, tested, qualified and mounted on the local supports must be available at CERN by the end of 2022. The total time available for module production and loading is 30 months, from Q2-2020 to Q4-2022. The detector integration is assumed to take the entire year 2023, while 2024 is reserved for extensive system tests on surface. The installation in the ATLAS cavern is foreseen for Q3-2025.

The estimate of the number of pixel modules depends on the details of the particular detector layout under consideration and ranges from 10,000 to 12,000, for a total active surface between 15 and 18 m^2. Most of the modules are quad modules, i.e. made of four front-end chips arranged in a 2×2 matrix. There are, however, single front-end and 2×1 modules, depending on the exact layout and on the sensor technology. In order to complete the module production in 30 months, a flat-top production, testing and loading capacity of 20-30 accepted modules per day must be achieved. This estimate includes the effect of yield and failure recovery procedures. Based on the experience accumulated with the fabrication of the ATLAS Pixel detector, it is believed that a similar production rate is achievable using seven to eight production clusters operating in parallel. This estimate is entirely consistent with the number of institutes that have expressed aspirations to build modules and who have indications from their funding agencies that funding will be available. The most time consuming phases during the assembly of a hybrid pixel module are the bump-bonding and the operational testing.

Pixel module testing procedures can be significantly improved with respect to previous productions, by implementing more parallelism in the read-out and increasing the level of automatisation of repetitive sequences. Bump-bonding, however, may represent a bottleneck for the production: it is a low volume industrial process and for this reason tends to be batched and the maximum capacity available is not continually exploited. Based on previous experience, delays in bump-bonding can occur for many reasons, so it would be prudent to anticipate that excess capacity will be needed to be able to catch up and keep assembly activities properly supplied. Efforts are in progress to qualify five or six bump-bonding vendors. Besides the investigation of the technical characteristics of the different processes, a significant effort will be made to verify the maximum production rate each vendor can achieve. The aim would be to select at least three vendors with a peak capacity of 20 modules/day each: this would ensure a large margin with respect to the required average rate, hence a safe handling of fluctuations and possible problems at one vendor. At the same time, the possibility of using automatic flip-chip machines available at different

institutes in the Pixel collaboration to alleviate the load on the industrial partners is being explored. Bump-bonding qualification is already on-going, using the previous generation of front-end chip (the FE-I4, used in the IBL) coupled to new sensors or dummy test structures. The final step of the qualification, including going to the smallest pixel pitch, will however only be possible at the beginning of the pre-production. Another aspect that can have a significant input on the schedule is the decision process to select between alternative sensors and/or module interconnection technologies. As explained in the previous paragraphs, the Pixel TDR will not define a complete baseline design for the different module types that will be used in the detector: the final decision on some aspects of the implementation will be postponed until the FDR, i.e. at the beginning of the pre-production. One recent development, and active area of research, which could have a significant impact on the schedule is the use of monolithic CMOS. In this case the simplification in module production and an important reduction of the load on the bump-bonding vendors may have a beneficial effect on the overall production schedule. On the other hand, the effect of postponing a decision on the technology may generate large delays elsewhere in the project. It is clear that the selection of the baseline technology to use in each layer of the detector cannot be postponed beyond the beginning of the pre-production phase (i.e. the beginning of 2019) to avoid interference with the tendering and procurement procedures.

In particular the decision on CMOS will not affect the development of standard planar hybrid modules up to the level required at the FDR. It is very likely that CMOS modules will only to be considered for outer layers, while the remaining part of the detectors will be built with standard hybrid modules. Moreover, each alternative technical solution to be considered between the Pixel TDR and the beginning of 2019 must be compatible with the local support thermal and mechanical specifications listed in the pixel TDR. This mandates that the new technologies are a "drop-in" solution replacing the de-selected technology. Several crucial R&D activities will still be in progress up the time of the Pixel TDR. This includes the front-end chip which will still be under evaluation. However, it should be possible to develop the TDR, around a robust baseline solution, based on the prototype work done so far and having gained experience with the bump-bonding providers to understand the achievable production rates. In Table 24.2 the scheduled reviews for the Pixel project are listed.

24.4 Schedule of the Common Structures for the ITk

The schedule for the common structures (outer cylinder and structural bulkheads and associated barriers) is driven by the need to have these components available at the start of the integration of the strip systems beginning 2021. The outer cylinder is needed to allow for the assembly of the barrel strip structures including the type I services in their final location inside the ITk. Whereas the structural bulkheads are not mechanically linked in the final configuration, they are so closely related to the strip end-caps that they need to be included

Table 24.2: Milestones for the ITk Pixel Detector developments

Milestone	Date
Local supports	
Specifications Review	Q1-2017
Preliminary Design Review	Q2-2017
Final Design Review	Q1-2019
Production Readiness Review	Q1-2020
Sensors	
Specifications Review	Q1-2017
Preliminary Design Review	Q2-2017
Final Design Review	Q2-2018
Production Readiness Review	Q4-2019
Front-end Chip	
Specifications Review	Q1-2017
Preliminary Design Review	Q3-2017
Final Design Review	Q1-2018
Production Readiness Review	Q4-2018 – Q3-2019
CMOS	
Specifications Review	Q1-2017
Preliminary Design Review	Q4-2017
Final Design Review	Q3-2018
Production Readiness Review	$<$ Q2-2020
Bump bonding	
Specifications Review	Q1-2017
Preliminary Design Review	Q2-2017
Final Design Review	Q4-2018
Production Readiness Review	Q4-2019
Module	
Specifications Review	Q1-2017
Preliminary Design Review	Q3-2017
Final Design Review	Q4-2018
Production Readiness Review Q4-2019 – Q3-2019	
Power distribution	
Specifications Review	Q1-2017
Preliminary Design Review	Q3-2017
Final Design Review	Q1-2019
Production Readiness Review	Q1-2020
Data transmission	
Specifications Review	Q1-2017
Preliminary Design Review	Q3-2017
Final Design Review	Q1-2019
Production Readiness Review	Q1-2020

in the construction of the end-caps. This would allow for a compact end-cap package including services. Other common structures, for example the pixel support tube, will be needed at a later stage of the ITk integration. An integration cradle, that provides support during the integration process and later transport to Point-1, is needed at the beginning of the strip integration phase. A prototype of this structure will be built so that it is available during LS2 (2019) for insertion trials into ATLAS to verify the envelopes for ITk and cradle, and the approach path.

A key milestone for the next few years is the demonstration that the low evaporation temperature of -35°C, which is primarily needed for the pixel system, can be achieved with a realistic feed and return pipe network and distribution. Because of the crucial importance of this issue for technology choices in the pixel system, a test facility ("baby demonstrator") is being set up, which is scheduled to provide results at the time of the pixel TDR (end of 2017). Because of the larger thermal headroom in the strip system the ultimate achievable evaporation temperature is much less critical for the strip system. However, use of the baby demonstrator facility will be made to verify our designs for evaporators and type I services in the strip system. As the goal of the baby demonstrator is to demonstrate low-temperature operation it will only supply a limited amount of cooling power (a few kW). It is anticipated that the final cooling plants will be larger by about a factor 10 (20-30 kW) and the design and performance of such a close-to-final plant will be investigated in a demonstrator plant to be available in 2020. After that the design of the cooling plants for the ITk will be finalised and production will be commenced.

In Table 24.3 the scheduled reviews for the different Common Mechanics items are listed.

24.5 ITk DAQ Schedule

A description of the ITk off-detector read-out and its interface to ATLAS TDAQ is contained in Chapter 16. At the time of this TDR the work focuses in two separate areas which will start to converge in 2017 (see Table 24.4).

Work is ongoing on DAQ systems required to be able to test Pixel and Strip modules as they start to be produced. These systems will evolve into production test systems. In parallel, a group representing the pixel and the strip systems are working with a FELIX group from the TDAQ organisation to define the hardware, firmware and software requirements needed to meet the ITk read-out and control specifications. Eventually, the components of the test DAQ systems will be incorporated into the online DAQ system interfaced to ATLAS TDAQ. While it is important to understand the requirements of the online DAQ system soon, the actual purchasing of hardware can be delayed for some time until it is needed and when it is hoped that the costs will have decreased. The PDR of the strips functional blocks will take place in 2017 and the final design review in 2019. A demonstrator of the system including integration with ATLAS components will be built for the FDR. The

Table 24.3: Major review dates for the ITk Common Mechanics project. Common structures are the outer cylinder, the structural bulkheads and the Pixel and Strip Support Tubes.

Milestone	Date
Surface commissioning infrastructure	
Specifications Review	Q2-2018
Preliminary Design Review	Q2-2018
Final Design Review	Q1-2019
Production Readiness Review	Q2-2020
Surface integration	
Specifications Review	Q3-2017
Preliminary Design Review	Q4-2017
Final Design Review	Q1-2019
Production Readiness Review	Q2-2020
IWV Support Rail System	
Specifications Review	Q3-2017
Preliminary Design Review	Q4-2018
Final Design Review	Q1-2020
Production Readiness Review	Q2-2021
OC support cradle and lifting	
Specifications Review	Q3-2017
Preliminary Design Review	Q4-2018
Final Design Review	Q1-2020
Production Readiness Review	Q2-2021
Common structures	
Specifications Review	Q2-2017
Preliminary Design Review	Q3-2017
Final Design Review	Q1-2018
Production Readiness Review	Q1-2019
Inner detector seal plate	
Specifications Review	Q1-2017
Preliminary Design Review	Q1-2019
Final Design Review	Q4-2020
Production Readiness Review	Q4-2022
CO_2 cooling plant	
Specifications Review	Q4-2017
Preliminary Design Review	Q4-2018
Final Design Review	Q4-2019
Production Readiness Review	Q4-2020
Cable cooling plant	
Specifications Review	Q4-2017
Preliminary Design Review	Q1-2019
Final Design Review	Q4-2020
Production Readiness Review	Q4-2022

Table 24.4: Milestones for the ITk/TDAQ developments

Milestone	Date
Specifications for top level ITk read-out system completed and reviewed	Q1-2017
Specifications for all ITk functional blocks completed and reviewed	Q3-2017
Preliminary Design Review of ITk-Strip functional blocks	Q2-2017
Preliminary Design Review of ITk-Pixel functional blocks	Q2-2018
Complete Build and Test a prototype read-out system	Q3-2018
Final Design Review (FDR) of ITk Read-out System including integration with ATLAS general components	Q2 2019
Complete Build and Test sample size of final system	Q4-2019
Production Readiness Review of final system	Q2-2020
Deployment of ITk Read-out System for Strip Detector	6 month before integration
Deployment of ITk Read-out System for Pixel Detector	

first small-scale purchase will be made in 2018 to test the DAQ system. The second large-scale purchase will be used for integration tests at the surface and the final full purchase is scheduled to allow full installation prior to the installation of the ITk into ATLAS.

24.6 Interlocks System Schedule

The Interlock System and Environmental Monitoring are described in Chapter 12. Pixels will incorporate a fully hardwired interlock system but the ITk Strip Detector must, because of the large number of modules, send some of its important monitoring information off detector via its optical system. Therefore, the interlock system will include both electrical signals obtained directly from the detector as well as information obtained through the SCA channel of the lpGBTx/VTRx+ system via the service caverns. In addition to that information obtained from the Pixel and Strip systems, temperature monitors mounted directly on the cooling pipes will be read out by the Interlock system. Because of the inclusion of Pixel and Strip information, the full interlock system cannot be defined until the Strip, and especially the Pixel read-out system is defined (see Table 24.5). This should, however, not affect the date of full deployment which is not required until before ITk installation in Q3-2024. A small scale version of the system is to be used for testing on the surface during integration.

Table 24.5: Milestones for the ITk Interlock System and Environmental Monitoring developments

Milestone	Date
Specification of Interlocks Completed and Reviewed	Q1-2017
Specification for Environmental Monitors Completed and Reviewed	Q1-2017
Preliminary Design Review of Interlocks	Q4-2018
Preliminary Design Review for Environmental Monitors	Q4-2018
Final Design Review (PRR not required) of Interlocks	Q3-2019
Final Design Review (PRR not required) of Environmental Monitors	Q3-2019
Start Construction of Interlocks	Q1-2020
Start Construction of Environmental Monitors	Q1-2020
Interlock System Complete	Q1-2021
Environmental Monitors Complete	Q1-2021

24.7 ITk Grounding & Shielding

The general concepts of the grounding and shielding (G&S) strategy are explained in Chapter 17. A more comprehensive description is being written and will be reviewed in early 2017. The development of the G&S scheme will, however, continue throughout the design and construction phases even to the installation of the ITk. All specifications - both electronic and mechanical - will be reviewed together with the details of the design reviews to assure that the ITk meets the G&S design strategy (see Table 24.6). During installation, final checks will be made for the requirement of a single point ground.

Table 24.6: Milestones for the ITk Grounding & Shielding developments

Milestone	Date
Completion of G&S Strategy Document	Q1-2017
ITk Meets G&S Design Strategy	To be complete when the ITk design is done
ITk Meets G&S Requirements	To be complete at the time of installation

24.8 ITk Pixel and Strip Cables and Powering

Plans for ITk powering and cabling are described extensively in Chapter 17 . Work is proceeding on the design of the Strip Detector as the layout and power requirements are generally understood. The Pixel design cannot be completed until the layout is finalised as this will determine the number of modules and ASICs and a good estimate of the ASIC power requirements. This work will be complete before the submission of the Pixel TDR. Based upon preliminary power estimates, the existing Pixel cables up to Patch Panel 2 appear to contain sufficient copper cross section. However, the assessment of the modularisation of cables to satisfy the Pixel requirement awaits the final layout. For the Strip Detector, the power and modular count of cables is understood and a few vendors were contacted to choose between a couple of bundling options and appropriate connectors in order to obtain realistic cost estimates. The purchase of cables and power supplies is much later in the schedule but space limitations, especially in the Patch Panel 2 area and along the face of the cryostat, demand that designs for patch-panels, connectors and cable bundling be sorted out in the near future as is reflected in the schedule shown in Table 24.7.

Table 24.7: Milestones for the ITk Pixel and Strip Cables & Powering

Milestone	**Date**
Specifications for Strip Cables Written & Reviewed (both existing and new cables)	Q4 2017
Specifications for Pixel Cables Written & Reviewed (both existing and new cables)	Q4 2017
Specifications for Strip Power Supplies Written & Reviewed	Q1-2017
Specifications for Pixel Power Supplies Written & Reviewed	Q1-2017
PDR for Strip Powering System	Q2-2017
PDR for Pixel Power System	Q3-2017
FDR for Strip Powering System	Q2-2018
FDR for Pixel Powering System	Q2-2019
PRR for Strip Powering System	2022
PRR for Pixel Powering System	2022
Strip Powering System Complete	2024
Pixel Powering System Complete	2024

25 Risk Analysis and Risk Mitigation

The scope of this section is to describe the process developed to assess, manage and mitigate risks associated with the ITk project and to summarise the status of the work at this point in time. Risk management is being integrated into the ITk project in two phases. In the phase leading up to the TDR, a team of technical experts identified by ITk project management have started the risk assessment process and are developing the implementation of the risk management structure. In the phase following the TDR and before pre-production begins the risk management process will become a fully integrated element in the ITk project organisation with, for example, a risk management plan with formal roles and responsibilities whose goal is to insure that the ITk project objectives can be met with a high degree of confidence. In the remainder of this section the initial actions carried out to establish a risk management process, the type of information acquired, a description of some of the issues and concerns in more detail with a focus on the Strip detector and an overview of the risk management plan to be implemented post-TDR and throughout ITk construction is presented.

The establishment of the ITk project risk management process has followed the guidelines of broadly-accepted risk management protocols:

- DOE G413.3 [174]
- Project Management Body of Knowledge [175].

Knowledge and experience from other large projects (CMS, The Upgrade to the Argonne Advanced Photon Source, DESI-II) has also been studied. A useful guide which may aid the reader in following the process of developing and executing a risk management plan, and risk mitigation can be found in Ref. [175]. There are also numerous commercial companies who provide tools and guidance on risk identification and management, for example Ref. [176], which provides some freely available charts and checklists. These references largely agree on the typical five-step approach to risk management listed below:

I Identify potential project risks.

II Analyse the risk.

III Plan risk mitigation strategies.

IV Execute risk mitigation strategies.

V Monitor and track the results, revising the mitigation strategies as necessary.

In the context of this project it is, however, worth noting the added complication that comes from the way resources are typically controlled in large international particle physics programmes, with resources mainly held at a national level with a large number of different funding agencies involved (all with very different reporting systems). This means that for deliverables linked to a specific funding agency, different risk reporting may be required within that specific national framework in parallel to the processes described here. The different ways in which staff effort is accounted can also lead to national differences in possible mitigation strategies within fixed funding envelopes. Furthermore, contingency is also typically handled at a national level, again with very different approaches adopted by different funding agencies.

As shown in the ITk organisation (Chapter 24, Fig 24.1), risk management will be conducted by a Risk Management Committee (RMC), which reports through the ITk Steering Committee to the ITk Project Leader. The responsibilities of the RMC include the identification of potential project risks, the analysis of these risks, response planning such as the development of mitigation strategies and monitoring and tracking of the risks and mitigation plans. In this context, a risk is any event not included in the project plan which can have a potential impact (positive or negative) on the ITk project. The RMC will comprise a chairperson, the system project engineers, a number of technical experts drawn from the ITk project as a whole, a representative from ATLAS Technical Coordination and the ITk, Pixel and Strip Project Leaders (ex officio). The chair of the RMC will be appointed by the ITk Project Leader who will be a member of the ITk Steering Committee. The technical experts are to be nominated by the subproject leaders in consultation with the Project Engineer and Project Leader. As an example a technical expert (commonly referred to as a Subject Matter Expert in the language of Risk Management) would represent areas such as electronics, powering, grounding and shielding, mechanical design, construction and integration, cooling and services. The Risk Management Committee will formulate a Risk Management Plan (RMP), which will define the procedures within which project risks will be identified, monitored and are reported at the ITk Steering Committee. These procedures will take account of the special international character of the ITk project such that the work is conducted through negotiations with many different national funding agencies, each with their own internal reporting and monitoring requirements. Risks identified as having high potential impact or probability will be given a greater level of scrutiny and oversight. The reporting period will be quarterly, though more frequent reporting may be required during different phases of the project and for some categories of risk. A risk register containing the information that is used to assess and prioritise risks will be maintained as a part of the risk management process. This will, for example, define thresholds at which additional scrutiny will be applied to individual risks and will codify the routine monitoring of risks and risk mitigation.

For the purposes of the RMP, project completion is defined as the point in time following the completion of the beam-pipe bake out after full installation of the ITk. The project scope and performance is given in the individual system Technical Design reports.

The development of the plan for ITk risk management has begun. A uniform approach to

obtaining the information needed to populate the risk registry is needed and a template form has been produced to be used for this purpose. This form includes information such as: risk identifier, risk submitter, risk owner, WBS element, brief risk description, risk analysis, risk mitigation plan for risk assigned a high level. A document defining roles and responsibilities and background information to aid in the identification and description of risk has been developed and an initial collection of a set of project risks completed. In the sections below we discuss the goal and timeframe for the development and implementation of the ITk Risk Management Plan, the risk register, provide more information on some examples of risks identified and discuss how a more comprehensive list will be generated once the proposed structures are implemented.

25.1 Risk Management Plan

Following accepted practices, a draft Risk Management Plan (RMP) is being prepared which will cover both Strip and Pixel detector systems of the ITk. This plan is based on prior work by members of the ITk Risk Assessment Team taking into account the special international nature of the ITk project with, for example, contributions and commitments to the project made through negotiations involving multiple national funding agencies. The RMP defines the roles and responsibilities of the members of the Risk Management Committee, the documents to be prepared as part of the RMP, the thresholds used to characterise risk probability and impact, and the process of monitoring and controlling risks throughout the project. The plan is to have all documents associated with risk management in place and active by the second quarter of 2017. This schedule fits well with the schedule for key decisions associated with the strip and pixel systems. A failure mode and effect analysis (FMEA) will be carried out and will address such characteristics as single point of failure. This is a design issue and the FMEA report will be reviewed as part of the PRR and FDR.

25.2 Risk Register

The starting point in risk management is to assemble a list of risks, review them and then begin the process of documenting and monitoring them. A list of risks has been gathered via one-on-one exchanges with individual experts; and a series of brainstorming sessions with the broad participation of members of the collaboration, and by the Strip and Pixel Detector Project Leaders. The level of detail has varied from simple statements requiring follow-up with experts and the risk submitter, to a detailed technical and schedule risk analysis, for example for the ITk Strip Detector local support and the ITk pixel sensor procurement. As a means of engaging technical experts and to facilitate assessment, the list of risks acquired has been categorised by technical area including:

Generic: manpower; schedule; supply of parts; layout; other

Pixel: identified risks include problems in complicated build, flip-chip bonding

Strip: general production; distributed build; technical performance of components

Common mechanics: interfaces; cooling; other; global mechanics

Local supports: thermal; electrical; stability

Modules: technical; ASICs; sensors; system test; macro assembly

Some examples of the risks characterised in this phase of the risk management process are given below.

A prototype ITk risk register has been based on the risk register excel spreadsheet developed for the DESI-II project at LBNL, which was developed in part by one of the ITk Project Engineers.

Date Registered	Submitter	ID	Type	Owner	Subproject	WBS	Title	Description	Notes on potential response plans	Response

Figure 25.1: Prototype ITk Risk Register with columns providing a general description of the risk item.

Figure 25.1 and 25.2 show key elements of the risk register. The column entries shown in Figure 25.1 provide a general description of the risk element:

Date Registered: date on which the risk was first registered in the risk register

Submitter: individual who was responsible for identifying and describing the risk item

ID: ID assigned to the risk item in the Risk register (e.g. "R2-01")

Type: the type of risk (Threat or Opportunity)

Owner: the individual in the ITk project organisation directly responsible for the management of this risk item

Subproject: the subproject within which this risk element falls (e.g. 2.2)

WBS: the WBS element associated with this risk item (e.g. 2.2.1)

Title: a brief title for this risk element (e.g. "Strip Sensors")

Description: a brief description of the risk item (e.g. "Only a single vendor is qualified or bids for production"

Notes on potential response plans: brief description of how one might manage and mitigate this risk item (e.g. "Market survey included six vendors. Vendor qualification concludes 12 months prior to first production delivery.")

Response: Approach which is to be adopted in managing this risk (e.g. "Work with vendor to obtain agreed upon delivery plan and cost with early delivery option within CERN FRAME Contract").

					Risk Impacts					Risk Rank				
Likely Fiscal Year of risk event	Cost impact excl. burn rate (kCHF)	Schedule impact on activity (months)	Total float (working days)	Probability	Cost Impact (kCHF)	Schedule Impact on CP (months)	Scope Impact	Performance	Notes on probability and impact	Cost Risk Rank	Schedule Risk Rank	Scope Risk Rank	Performance	Risk Rank

Figure 25.2: Prototype ITk Risk Register with columns providing more specifics of the risk item.

The column entries shown in Figure 25.2 provide more information on the specifics of the risk and risk mitigation. Note that some of these entries are calculated in the spreadsheet based on the data entered and defined thresholds for risk rank (high, medium, low):

Likely Fiscal Year of risk event: year in which this risk item is expected to occur

Probability: likelihood of risk event as estimated by risk owner and reviewed by RMC

Cost Impact (kCHF): potential cost impact (in kCHF) of risk event as estimated by risk owner and reviewed by RMC (cost impact can be subcategorised as "optimistic", "most likely", "pessimistic")

Schedule Impact on CP (months): Potential schedule impact (in months) of risk event as estimated by risk owner and reviewed by RMC (schedule impact can be subcategorised as "optimistic", "most likely", "pessimistic")

Scope Impact: potential scope impact ("low", "medium", "high") of risk event as estimated by risk owner and reviewed by RMC

Performance: potential performance impact ("low", "medium", "high") of risk event as estimated by risk owner and reviewed by RMC

Notes on probability and impact: brief description of details justifying likelihood and impact of risk item

Cost Risk Rank: calculated low/medium/high risk rank based on potential cost impact and likelihood in comparison to defined threshold

Schedule Risk Rank: calculated low/medium/high risk rank based on potential schedule impact and likelihood in comparison to defined threshold

Scope Risk Rank: calculated low/medium/high risk rank based based on potential schedule impact and likelihood in comparison to defined threshold

Performance: calculated low/medium/high risk rank based on potential performance impact and likelihood as estimated by risk owner and reviewed by RMC

Risk Rank: calculated summary risk rank based on calculated cost, schedule, scope and performance risk ranks

For risks having a Risk Rank of "high" additional material beyond the summary material in the Risk Register will be collected by the risk owner and used by the RMC to control and manage such risks. The process of collecting more detailed information on items on elements in the above mentioned lists is under way. In the absence of a comprehensive risk analysis, the risk assessment and analysis is illustrated using a number of examples considered to have the potential for high impact on the ITk project:

I The strip sensor procurement requires that vendors must be qualified as being able to meet specification through following a procurement protocol and there is a possibility that only one such vendor will be qualified. A market survey was carried out from which two of six possible vendors are being considered for the next set of requirements in the protocol (STEP-3). Multiple prototyping runs with the STEP-3 vendors are ongoing to allow vendors to develop production processes which meet the sensor full specifications. If necessary it will be possible to work out any remaining issues during pre-production. It may also be possible to qualify new vendors if schedule permits.

II There are concerns that additional design and fabrication cycles may be needed for the front end readout chips (such as the ABCStar and the HCCStar). An extensive review of specifications, designs and test structures prior to submission of these chips is planned. Should the availability of effort of design and testing become an issue then the possibility of moving manpower from lower priority tasks will need to be considered. A delayed chip production schedule could be compensated by an increased production rate for module production, either through finding resources to run multiple shifts or supporting additional production sites.

III Given the experience with the IBL, it is possible that final versions of ABCStar or HCCStar have differing processing resulting in higher current increases with total ionising dose. Early radiation testing of chips will be planned to allow this effect to be measured in sufficient time to allow for adequate margin to be provided in the cooling budget. Consequences may include an increased material budget due to the cooling system.

IV There are key elements of the readout electronics such as the opto-electronics and the lpGBTx whose design and delivery are not controlled by the ITk project. These are common risks with, for example, CMS, and the design and delivery plan for these components will be closely monitored with respect to the ATLAS ITk construction

schedule. Schedule mitigation may be achieved, for example, through use of electrical pre-production parts for testing a fraction of staves/petals during assembly before the final components can be retro-fitted.

V The strip cooling system requires many tube connections and connectors which must be welded with 100% reliability. Extensive pressure testing of joints is planned as is the development of in-situ techniques for the repair of joints and connections failing to meet pressure tests.

VI Commercially available glues are not specified in terms of HL-LHC operating conditions, so extensive testing by ITk is required. This has been a major R&D topic with considerable expertise built up within the collaboration. There is a concern that glue composition in production may be different from that used in qualification. Extensive destructive testing (including full size objects) in terms of mechanical, thermal and electrical properties both before and after irradiation will be carried out to verify that glues meet mechanical and thermal requirements (such as that experienced during any thermal shock).

VII A number of system issues such as grounding and shielding and thermal and mechanical performance are covered by a small number of experts. The training of additional experts will be a priority, such as could be accomplished through early system level testing at the qualification and pre-assembly stages of construction.

VIII At the present time there is only a single vendor for thermo-mechanical foam used to bond the cooling tubes to the staves and petals of the detector elements. This vendor has been reliable in prior projects. However, alternative bonding agents will be considered with the consequence that possibly the material budget of the cooling system will have to increase.

Following accepted risk management practices, in the next phase of review the RMC will acquire additional material on risks and concerns, in consultation with subject matter experts and the risk owners to assess the potential impacts of the identified risks in terms of cost, schedule and probability of occurrence.

Thresholds, integrated in the Risk Register, will be applied to schedule impact and cost risk for elements to be monitored by the Risk Management Board. Typically these will be elements in the moderate/high risk categories in the chart above. The thresholds will be determined once a sufficient number of risks have been identified and assessed. Risks for which a sound mitigation plan is in place, may be identified, assessed and retired while others may be added to the list of risks for which there is a high level threat or opportunity and then subjected to even closer scrutiny.

26 ITk Strip Detector Costing

The overall cost of the ITk Strip Detector is described in this chapter. The structure of the cost estimate, its current value, and the uncertainties of the estimate are discussed. This is followed by the expected time profile of the spending during the production phase of the ITk Strip Detector, which is based on the production model introduced in Chapter 13. A path toward the final costing for the ITk Strip Detector will be outlined in Section 26.3. The cost estimates for the ITk Pixel system and the common items will be summarised in Sections 26.4 and 26.5, respectively.

26.1 Costing Structure, current Costing Estimates for Items and Item Cost Uncertainties

The CORE cost estimate for the ITk Strip Detector is detailed with individual elements for most items. The numbers of installed items have been calculated based on the layout discussed in Chapter 5. The 5% pre-production is included in the CORE costing and is in addition to the installed units. These pre-production components, constructed using final tooling and staff, will demonstrate readiness for the final production. The costs of generic infrastructure, prototypes, and spare components are all excluded from the CORE costing.

For each significant production step, the yield is estimated based on current prototyping and past production experience with the ATLAS SCT and the CMS SST production. The loss of components is propagated through the system taking into account the point of failure, i.e. when a module fails at the last testing step, the wastage of ASICs, sensors and power boards is calculated correctly. This results in different yields for most items in the costing. Sensors and custom ASICs have a significant non-recurrent engineering (NRE) value for their production mask sets. Based on past experience, two complete mask sets have been assumed for each submission in order to cover the risk for needing a final revision of the ASICs or sensors.

To minimise inaccuracies due to exchange rates, the items' costing estimates are done in the expected currency for the final procurements. For the ITk Strip Detector system costings presented here, the exchange rates to Swiss Francs (CHF) have been fixed to the three month average in the CERN accounting system for the period of September 1 to November 30, 2016.

The price estimates for all the individual items are based on the most accurate information available; the level of cost certainty of an item depends on the amount of technical development and understanding of its procurement process. For items based on quotations, an inflation factor of 10% has been applied if no updates have been made available since the 2014 scoping exercise. To describe the level of uncertainty of the costs, the methodology used for the ATLAS Phase-II Upgrade Scoping Document [2] and 2014 HL-LHC accelerator upgrade costing exercise has been used, as shown in Table 26.1; the quality factor of the estimate depends on the level of design and availability of vendor quotes. QF1 has the highest certainty and is based on a vendor quote for the final item or a catalogue price; QF5 has the least amount of certainty and is based on a rough estimate without any detailed design. Quality factors have been assigned to all items within the full strip costing. For the level of work breakdown structure (WBS) detail shown in this document, an cost-weighted average quality factor for the items within the given category has been assigned.

Table 26.1: Quality factor definitions

Quality factor	Description
QF1	Based on a vendor quote or catalogue price
QF2	Based on a similar part or purchase
QF3	Based on an engineering design
QF4	Based on a conceptual design or scaled from similar systems
QF5	Based on a rough estimate without any detailed design.

The most precise current estimates (QF1) of item valuations are those produced within the CERN frame contracts and/or are CERN deliverables. As the frame contract sets the pricing once the layers used in an ASIC and its size are known, the costs of the ASICs produced in the Global Foundries 130 nm 8RF (such as the ABCStar) are very well known. The items produced by CERN, like the upFEAST or the lpGBTx, similarly have a precise cost estimate due to their maturity and technologies chosen.

A number of items have had multiple prototyping cycles using one or more firms with cost estimates provided for full-scale production (QF2). There is more uncertainty for these costs as the vendors used for production cannot be determined before a full tendering process. Additionally, the details of the quality control processes to be performed by the vendors have not been finalised, which can influence the cost. This category includes items such as sensors, hybrids, barrel service modules, and carbon fibre materials.

Items with an uncertainty of QF3 typically have had multiple prototyping cycles, but not necessarily with final materials, layups, or packaging. These include power boards, bus cables, End of Substructure boards and Titanium pipe assemblies. The details of the global supports for the barrel are also at the engineering design phase. Other items with QF3 are off-the-shelf items of which the final models have not been chosen (low voltage and high

voltage power supplies). Finally, core jigging where multiple iterations and variants have been produced but not finalised have been given this quality factor including bus cable probe systems, stave shipping boxes, and module mounting tooling.

Items whose costs have been scaled from similar systems, including the end-cap global supports, and petal shipping boxes, have been given a QF4 rating. The type 2 & 3 services are also QF4. The details of these services have not been completely finalised. Early vendor quotes for components with representative cross-sections and complexity have been used in the costing. Finally, core jigging with more uncertainty have been included here, such as ASIC and sensor probing components, hybrid and module assembly tooling, and module boxes.

Finally, a number of items have a QF5 cost uncertainty. For items with labour from industry, the costs could vary significantly depending on the country and on the estimated time necessary to provide the given service. For the costing, a reasonable estimate per person-hour has been used, based on the costs for a number of firms in different countries. The best estimate for required time in production is then used to cost the item. These items include local support core assembly, hybrid wire bonding, and ASIC and sensor probing. Additional, certain core jigging has not been finalised and their value has been estimated from past experience in ATLAS SCT production or current prototyping. These include tooling for loading local supports into the global support, the costs of transport of the end cap to CERN.

26.2 Current Cost Estimates including Spending Time Profile

The cost estimates presented here are broken down to the third level of the WBS shown in Table 13.1. The total CORE cost estimate for the ITk Strip Detector is 60.7 MCHF. The most significant costs are for planar silicon strip sensors (about 39% of the total) as expected, followed by modules (∼16%), local supports (∼11%) and global mechanics areas (∼8%), respectively. The remaining categories all represent $1-6\%$ of the total estimated costs, see Figure 26.1.

The total CORE value of the system is consistent with the targets set by the scoping exercise [2].

In order to better understand the needs of the project with respect to funding, the cost profile in time has also been estimated (see Table 26.2). The basis for the timing is the schedule shown in Chapter 24. The schedule determines the latest period when components can be delivered based on the current assumptions for procurement, production and reception testing timing. Rates of production by foundries have also been taken into account. In addition, the collaboration's ability to receive these shipments in a reasonable time frame has been factored into the estimates. Finally, the various funding agencies within the project have indicated a preference for as flat of a spending profile as possible; the project has been

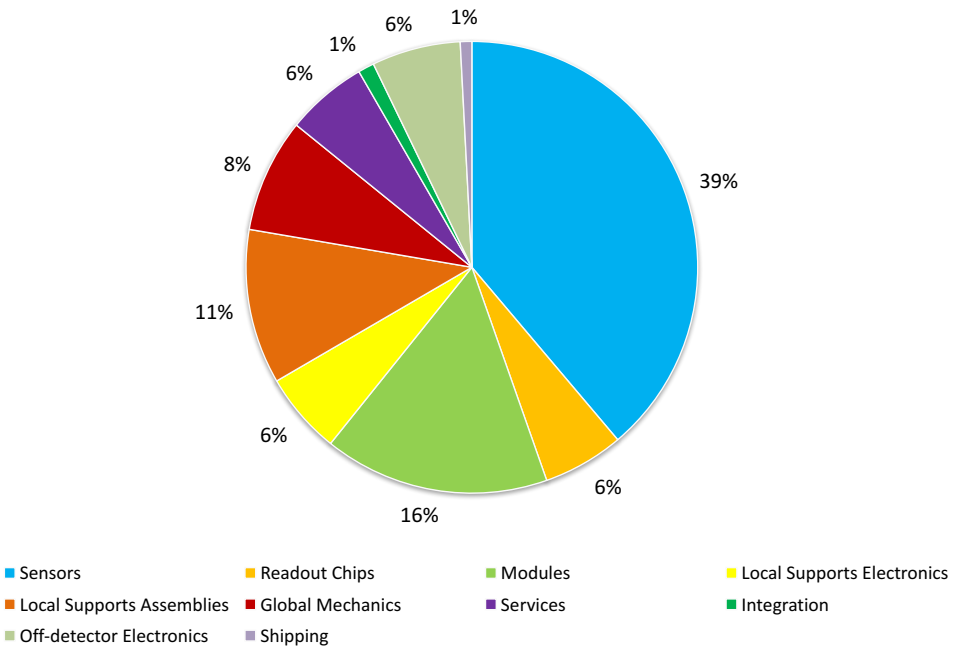


Figure 26.1: The estimated component CORE costs for the ITk Strip Detector.

adjusted as much as reasonable within the other constraints to try to achieve a flat spending profile (see Figure 26.2).

Early spending from 2017 onwards is necessary for the first production sensors and read-out chips to allow for the necessary quality assurance including irradiations prior to the pre-production. To reduce risk and increase uniformity, read-out chip and local support electronics productions are as fast and as early as reasonable. Global mechanics production starts early (2019 – 2021) to allow for the insertion of the completed staves and petals into the larger structures early in the assembly process. The spending for the large-scale production of parts (modules and local support assemblies) are spread throughout the 4-year production period. Services are split into two distinct time periods: in 2020 – 2021, the service modules necessary for integration into the barrel and the two end-cap global structures are produced. The type 2 and 3 cabling will be needed much later for insertion into ATLAS (2023 – 2024) during the shutdown period. Finally, the off-detector electronics need to be purchased in three blocks: a pre-production in 2019 is necessary to support systems testing, a 10% production in 2019 is required to support the barrel and end-cap integration efforts and finally the production order in 2023 – 2024 is needed for the full-system integration into ATLAS and for operation.

Table 26.2: Estimated CORE spending profile for the ITk Strip Detector in MCHF.

	Ave. QF	2017	2018	2019	2020	2021	2022	2023	2024	**Total**
Sensors	2.0	0.11	1.11	1.04	2.69	6.29	6.96	5.39	0.00	**23.58**
Read-out Chips	1.2	0.64	0.76	1.02	1.05	0.06	0.00	0.00	0.00	**3.52**
Modules	3.0	0.00	0.00	0.85	1.48	2.52	2.79	2.16	0.00	**9.80**
Local Supports Electronics	3.0	0.00	0.18	0.29	1.49	1.59	0.00	0.00	0.00	**3.55**
Local Supports Assemblies	4.1	0.00	0.10	1.18	2.09	1.69	1.15	0.54	0.00	**6.73**
Global Mechanics	3.4	0.00	0.00	1.98	2.47	0.49	0.00	0.00	0.00	**4.95**
Services	3.0	0.00	0.00	0.11	1.62	0.55	0.00	0.63	0.63	**3.54**
Integration	4.8	0.00	0.00	0.00	0.00	0.35	0.10	0.25	0.00	**0.70**
Off-detector Electronics	3.1	0.00	0.00	0.19	0.00	0.39	0.00	1.55	1.74	**3.86**
Shipping	5.0	0.00	0.00	0.03	0.06	0.14	0.16	0.12	0.00	**0.50**
Total	**2.7**	**0.75**	**2.15**	**6.68**	**12.95**	**14.06**	**11.15**	**10.63**	**2.37**	**60.75**

26.3 The Path towards the Final Costing for the ITk Strip Detector

An improved costing will be necessary at the time of the Memoranda of Understanding (MoU) to establish the final CORE valuation of each item or collection of items. The timing of this process depends on the time required for the tendering, purchasing and when production starts. For common HL-LHC items delivered from CERN (UpFeast, lpGBTx and versatile link), the cost estimates are already accurate. For the items produced within the frame contracts, the cost uncertainty is dominated by the number of ASICs per wafer and the ASIC yields which are both well understood. For the silicon sensors, which are the largest single purchase within the system, CERN has organised a joint market survey with CMS. The process will terminate with the invitation to tender to one or more vendors in Q2 2018. The purchases of type 2 and 3 cables is planned to go through CERN. An initial costing based on direct communications with specific companies used in the initial construction is available in the current estimates. The final procurement may be much later, as these items are only needed at the point of installation in ATLAS after 2024. For all other items in the Strip system, the tendering and purchase will be performed by the lead institute or institutions designing the object. The start of the procurement will be determined by the expected tendering period needed and consistent with the corresponding national rules.

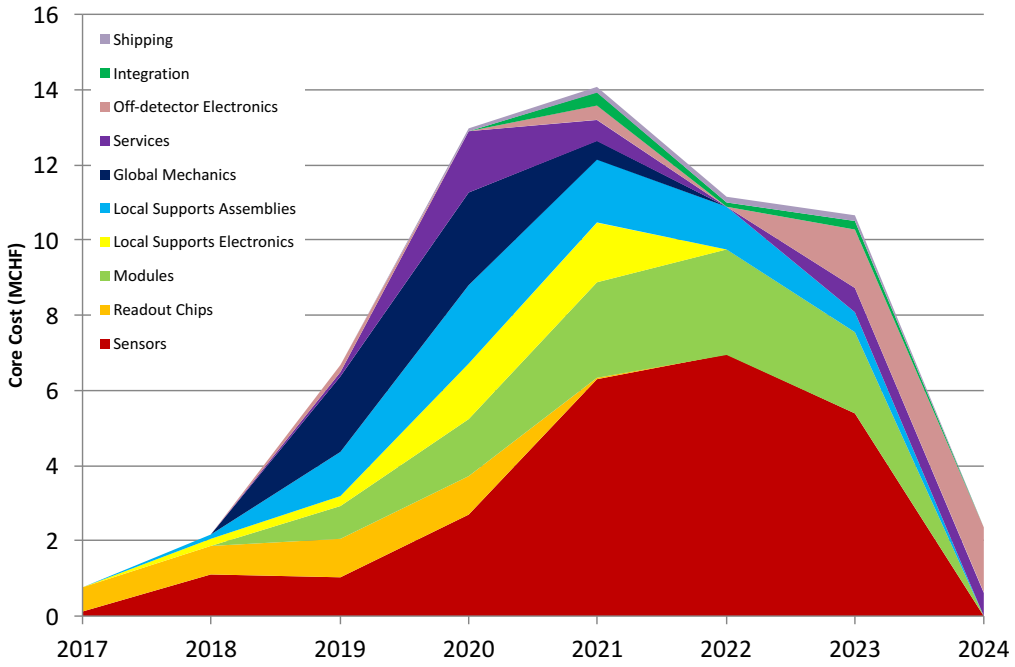


Figure 26.2: Estimated CORE cost spend profile.

26.4 ITk Pixel Detector

The pixel costing is based on a layout currently under consideration that includes a five-layer barrel configuration with a disk arrangement in the forward direction covering the pseudorapidity range up to $|\eta| = 4.0$. The construction of the barrel pixels is divided between the inner (layers 1 and 2) and outer (layers 3 and 4) barrels. The estimate is based on standard planar sensors bump-bonded to the front-end chip. It is assumed that the inner layer sensors will be n-in-n with 100 μm thickness for layers 1 and 2, and n-in-p for the outer layers. The construction of the inner layers is more challenging. The cost of the hybridisation includes the cost of bump bonding. The cost of the bump bonding is a significant fraction of the cost of module construction and here quotes have been used obtained from several vendors in 2015. The uncertainty on the cost of bump bonding is one of the key risks in the pixel module production. Market surveys for the planar sensors and bump-bonding vendors will start in 2017. It will be important to identify multiple (perhaps 5 or 6) bump bonding vendors for the production period. The front-end chips will be purchased through CERN using existing frame contracts. The values shown include the cost of the mask sets for production. The values quoted also include a pre-production period when 10% of the modules in the outer regions and disks and 15% of the modules in the inner regions will be fabricated. The estimate includes conservative yield values that are based on previous experience of pixel module construction. This estimate will be refined as the layout of the ITk Pixel Detector is fixed.

26.5 ITk Common Items

A list of the common ITk items with CORE values that will be covered by the institutes participating in the construction of the ITk is presented in Table 26.3. Only WBS items with a finite CORE value are presented in this table. The CORE values for these items have been determined from estimates based on experience with previous constructions (ATLAS ID and IBL) and in some cases scaling by area from previous costings has been applied. In most cases the detailed designs are not complete at the time of this TDR and will only be presented at the time of the Pixel TDR at the end of 2017.

Table 26.3: Costing of the common items for the ITk Detector in MCHF

	Common mechanics	
WBS	**Title**	**Amount [MCHF]**
2.3.1 – 2.3.2	Surface integration commissioning and integration	4.00
2.3.3	ITk common structures	2.40
2.3.6	Dry gas delivery	0.05
2.3.9	Cooling plant	6.30
2.3.10	Cable cooling plant	0.05
	Sub-Total	12.80
2.4.1	Environmental monitoring	0.42
2.4.2	Interlock system	0.50
2.4.3	Read-out system	2.50
2.4.4	Grounding and Shielding	0.03
	Sub-total	3.45
Total		**16.25**

It is expected that it will be possible to reuse the existing dry-gas and cable cooling plant systems. The latter will need some modifications to eliminate the use of fluorocarbon liquids. The value for the common structures, including the outer cylinder and the pixel support tube, are based on previous experience building large scale carbon-fibre support structures (for example the existing pixel support tube) and correcting for inflation to arrive at 2016 values. The $C0_2$ cooling system is still in development. A small-scale prototype system (5 kW at $-30°C$) will be constructed ahead of the Pixel TDR and test results will be available for that document. A full scale development system of the cooling system will follow. The value presented here is based on experiences from the construction of similar systems for ATLAS, CMS and LHCb.

The environmental monitoring estimate is the sum of a significant number of small-scale monitoring systems (temperature, gas-flow, humidity, radiation backgrounds etc.). The CORE value of the interlock system is based on estimates on the construction of similar systems used in other experiments. The cost of the read-out system is based on the development needed from our current understanding of the requirements for the Phase-II TDAQ system.

26.6 Total Cost of the ITk Detector

Table 26.4 presents a summary of the total costs of the ITk for the Strip and Pixel Detectors and the common mechanics and common electronics.

It should be stressed that the costs for the Pixel and the common items will only be finalised at the time of the Pixel TDR.

Table 26.4: Total cost of the ITk Detector in MCHF

	Strip Detector	
WBS	**Description**	**CORE cost [MCHF]**
2.2.1	Sensors	23.58
2.2.2	FE electronics read-out chips	3.52
2.2.3	Modules	9.80
2.2.4	Local support electronics	3.55
2.2.5	Local support assemblies	6.73
2.2.6	Global mechanics	4.95
2.2.7	Services	3.54
2.2.8	Integratoin	0.70
2.2.9	Off detector electronics (incl PS + DCS)	3.86
	Shipping	0.50
	Sub-total	60.75
	Pixel Detector	
2.1.1	Sensors	7.87
2.1.2	FE chips	3.11
2.1.3	Hybridisation and module assembly	10.39
2.1.4	Services	6.67
2.1.5	Local supports	5.27
2.1.7	Integration and system test	2.52
2.1.8	Off detector electronics	7.24
	Sub-total	43.07
	ITk common items	
2.3	Common mechanics	12.80
2.4	Common electronics	3.45
	Sub-total	16.25
Grant total		**120.07**

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