

A program to drive the ATLAS Local Trigger Interface (ALTI) at the ATLAS experiment

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Abstract. During the High Luminosity upgrade of the Large Hadron Collider at CERN, the LHC experiments will undergo a series of upgrades in order to maintain high physics performance following an increased data rate. The largest Phase 1 upgrade project at the ATLAS muon system is the replacement of the current inner station (end-cap regions) with the New Small Wheels. In addition, the ATLAS Local Trigger Interface (ALTI), a part of the Timing, Trigger and Control (TTC) system, will replace the four existing TTC modules. In normal operation, the detectors, along with the surrounding electronics, will receive TTC related signals from the Central Trigger Processor (CTP). This information is forwarded to the front-end electronics of each of the ATLAS sub-detectors through an optical network via the ALTI. The interface currently produces an artificially generated pulse pattern that contains the TTC information. This paper will summarize the creation of a program that generates pulse pattern files which are used to drive ALTI. Various tests have been conducted in order to study the performance of the NSW trigger electronics while using these files. Software development and data analysis using ROOT framework were used to validate the results of these tests.

1. Introduction

1.1. Large Hadron Collider

The Large Hadron Collider (LHC) is the world's highest energy particle accelerator, operated by the European Organization for Nuclear Research (CERN). Subatomic particles are accelerated close to the speed of light inside a 27-km circular tunnel near the Swiss-French Border. Beam collisions occur at four points, where four large experiments (ALICE, ATLAS, CMS and LHCb) are located. There, counter rotating, high intensity bunches of protons or heavy ions collide at a centre of mass energy $\sqrt{s} = 13$ TeV (Run II).

The nominal LHC beam structure describes the time distribution of these bunches along one LHC orbit (figure 1). It is comprised of 3564 bunches, of which 2808 full bunches, with $1.15 \cdot 10^{11}$ protons per bunch and spacing of 25 ns (or 7.5m in distance) [1].



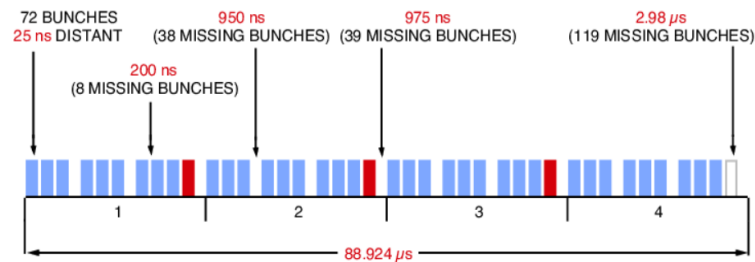


Figure 1. LHC beam structure [1].

1.2. From LHC to HL-LHC

The High Luminosity Large Hadron Collider is an upgrade to the Large Hadron Collider. It aims to increase the total number of proton-proton collisions, and thus reaching LHC peak luminosity by a factor of 10 beyond the nominal LHC value [2]. At the HL-LHC era, the experiments will upgrade to improve particle detection and enable the observation of rare events, increasing the potential in the search for new physics.

The path to High Luminosity includes two phases:

- Phase 1: (2018-2021)
Luminosity up to $L = 2 \cdot 10^{34} \text{cm}^{-2}\text{s}^{-1}$, Integrated Luminosity: $L_{int} = 350 \text{fb}^{-1}$ at Run 3.
- Phase 2: (2025-2027)
Luminosity up to $L = 5$ to $7.5 \cdot 10^{34} \text{cm}^{-2}\text{s}^{-1}$, Integrated Luminosity: $L_{int} = 3000 - 4000 \text{fb}^{-1}$ at Run 4.

2. The ATLAS experiment – Phase 1 upgrade

During Phase 1 of LHC upgrade, new or updated detector technologies, trigger electronics and data acquisition systems have been deployed by the LHC experiments in order to withstand the increased particle rate. At the ATLAS experiment, one of the major areas that will be affected is the muon spectrometer. The upgrade will include the replacement of Small Wheel, the current inner station of the experiment's muon end-cap system, by New Small Wheel.

The New Small Wheels aim to:

- Improve tracking efficiency in the high-rate environment (up to $15 \text{kHz} / \text{cm}^2$).
- Reduce fake triggers from background hits (figure 2). Currently 90% of muon trigger rate in the end-cap region ($1.3 < |\eta| < 2.7$) is caused by noise or accidental coincidences.
- Provide spatial resolution at $100 \mu\text{m}$ and angular resolution $< 1 \text{mrad}$ at the muon Level-1 Trigger system.

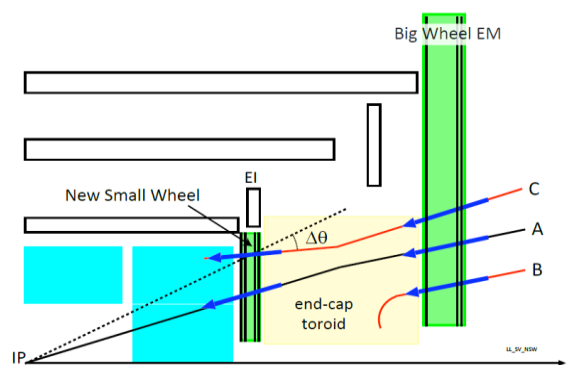


Figure 2. Track selection by New Small Wheel. Track A is accepted, while track B (producing hits only in the Big Wheel) and track C (not pointing to the interaction point) would be rejected [3].

2.1. New Small Wheel detector technologies and layout

The New Small Wheel will be comprised of two gaseous detector technologies:

- the Micromegas (MM) detectors - Optimized for precision tracking
Parallel plate detectors with a metal mesh separating the drift and amplification region.
- the small-strip Thin Gap Chambers (sTGC) - Optimized for triggering
Multiwire ionization chambers comprised of anode wires and segmented cathodes. The parallel cathode planes are divided into strips, that are perpendicular to the wires, on the one side and into pads on the other side.

Each New Small Wheel (figure 3) will be composed by eight large and eight small sectors. Sectors consist of two sTGC wedges and two MM wedges aligned in the following sequence: sTGC-MM-MM-sTGC and supported by a central spacer. A wedge is a quadruplet, providing four active layers of individual detector technology.

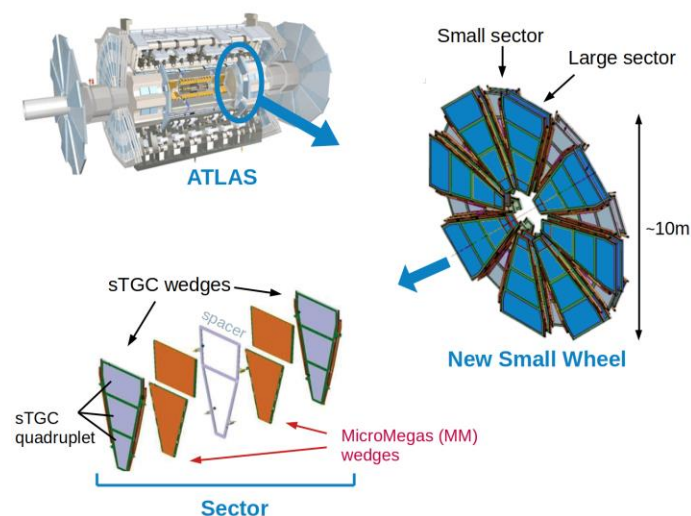


Figure 3. NSW Layout [4].

2.2. New Small Wheel Trigger electronics and Data Acquisition (DAQ) dataflow

The NSW trigger electronics and DAQ dataflow includes 128 detectors, ~2.4 million readout channels and separate trigger, readout and configuration/monitoring paths for both detectors (figure 4).

It is divided into two categories: on-detector electronics and off-detector electronics (cavern area). On detector electronics include Front-End Boards (FEB) with radiation-tolerant Application Specific Integrated Circuits (ASICs), Level-1 Data Driver Cards (L1DDC), Low Voltage Distribution Boards (LVDB) and ART Data Driver Cards (ADDC). Off detector electronics, on the other hand, include the Rim Crate (hosts Pad Trigger, rim Level-1 Data Driver Cards, Routers), Trigger Processor, Sector Logic, ALTI, Front End Link eXchange (FELIX) and Services (Read Out Drivers (ROD), Detector Control System (DCS) etc.). Communication between the electronics is achieved via mini-Serial Attached Small Computer System Interface (SAS SCSI) cables and optical fibers.

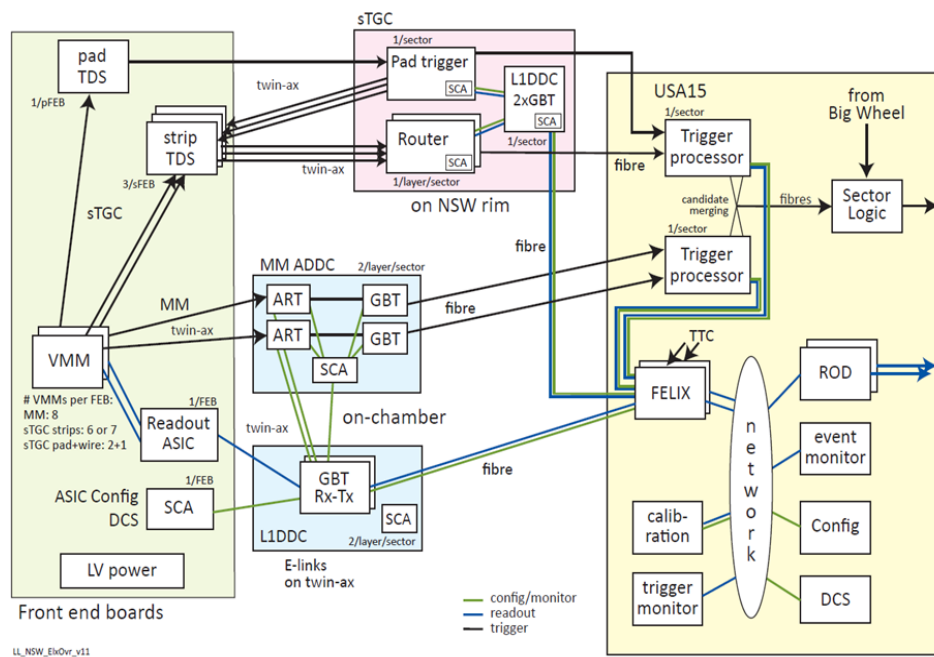


Figure 4. Schematics of NSW trigger electronics and DAQ dataflow [5].

3. ATLAS Local Trigger Interface (ALTI)

ALTI is a custom made 6U VME64x module (figure 5) which integrates the functionalities of four Timing, Trigger and Control (TTC) modules currently used in the experiment: Local Trigger Processor (LTP), Local Trigger Processor Interface (LTPI), TTC VMEbus Interface (TTCvi) and TTC Encoder/Transmitter (TTCex). Control software for ALTI is being executed on a single-board computer (SBC).

The primary function of ALTI is to provide the interface between the Level-1 Central Trigger Processor (CTP) and the TTC optical broadcasting network to the front-end electronics of each of the ATLAS sub-detectors. The Central Trigger Processor is responsible for making the initial trigger decision (Level 1 trigger accept signal) by identifying interesting particle candidates coming from the Level-1 calorimeter and Level-1 muon trigger systems, reducing the event rate to a maximum of 100kHz.

3.1. ALTI pattern and TTC signals

In normal operation, ALTI receives the TTC signals from the CTP and forwards them to the sub-detector electronics through the optical TTC distribution network. The TTC system is responsible for the distribution of the timing signals (BC, ORB), the trigger signal (L1A) and the control commands like Bunch Counter Reset signal (BCR) [6]. The following table (table 1) summarizes the 22 digital TTC signals, both FORWARD (from the CTP to the detectors) and BACKWARD (from the detectors to the CTP) in direction.

Currently for test purposes, ALTI provides an artificially generated pulse pattern (figure 6) which contains the TTC information. Additionally, it provides the Bunch Crossing clock, the main timing signal produced by the LHC, at a frequency of 40 MHz for data synchronization.

Table 1. TTC signals [6].

TTC signal	Direction	Description
BC	forward	Bunch crossing clock: 40.079MHz, 50% duty ratio.
ORB	forward	Periodic signal representing one LHC turn. Period is 3564 bunch crossings, pulse width is 40BC.
L1A	forward	Level-1 trigger accept signal of 1BC pulse width.
TTR[3..1]	forward	Auxiliary triggers generated locally by the partition.
BGO[3..0]	forward	Signals for sending B-channel TTC commands.
TTYP[7..0]	forward	8-bit trigger type identification word associated with each L1A.
BUSY	backward	Used to inform the CTP to introduce L1A dead-time, i.e. throttle L1A generation when the readout buffers are overwhelmed.
CALREQ[2..0]	backward	3-bit word issued by the sub-detector and used by the CTP to generate calibration triggers.

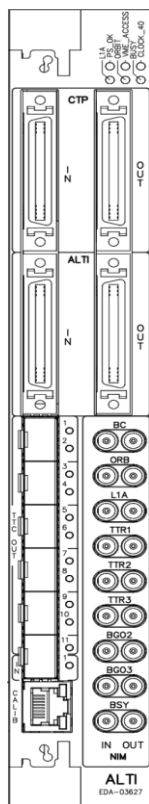


Figure 5. ALTI VME module (front panel view) [6].

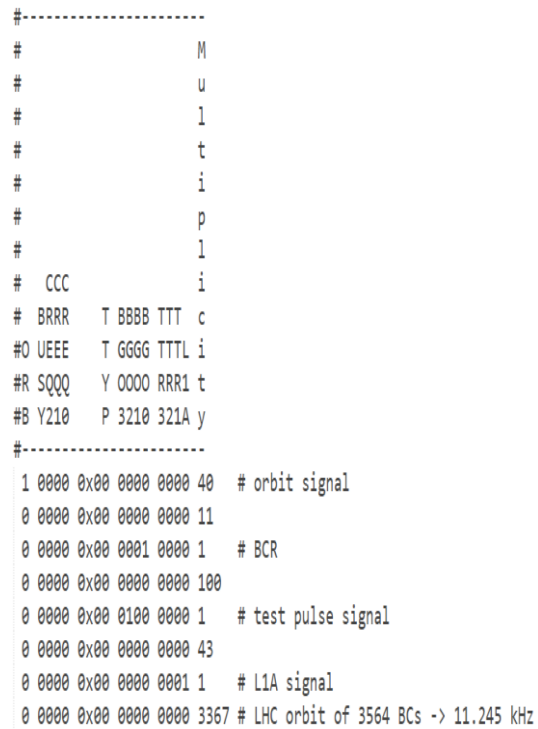


Figure 6. ALTI pattern file with TTC signals.

4. ALTI pattern generator

In order to simulate real-time trigger conditions and study the response of the NSW trigger electronics under them, a program has been created that provides the generation of ALTI pulse pattern files. These files are produced at different trigger rates, containing multiple TTC signals, parameters and trigger mechanisms that are used by the Central Trigger Processor in normal operation.

Three files are provided by the program: the ALTI configuration file, a text file containing the generated data and information related to them, and a pdf file for produced histograms.

4.1. Trigger mechanisms

Trigger mechanisms are implemented in the Central Trigger Processor in order to minimize BUSY signals from sub-systems of the ATLAS detectors [7]. To achieve that, the following mechanisms are deployed:

- Simple deadtime
Deadtime of 4 BC is introduced following the arrival of an L1A signal. It is used to prevent overlapping of readout time-frames for some front-end systems.
- Complex deadtime - “Leaky” bucket algorithm
Defined by the size S of the electronic buffers and the transmit rate R (figure 7). Deadtime is introduced when buffers are full. It is used to prevent de-randomisers of front-end systems to fill-up. The following buckets (S / R) were used in Run 2:
 - bucket 0: 15 / 370 for L1 Calorimeter and CSC
 - bucket 1: 42 / 384 for TRT
 - bucket 2: 9 / 351 for LAr
 - bucket 3: 14 / 260 for L1Topo
- Sliding window: Maximum 15 L1A signals in 3600 BC
Limits L1A signal trigger rate and prevents Pixel front-end to suffer from data de-synchronization due to single very large background event.

The program implements the aforementioned trigger mechanisms along with additional trigger rules related to test pulse - L1A signal latency, orbit duration, frequency limits etc.

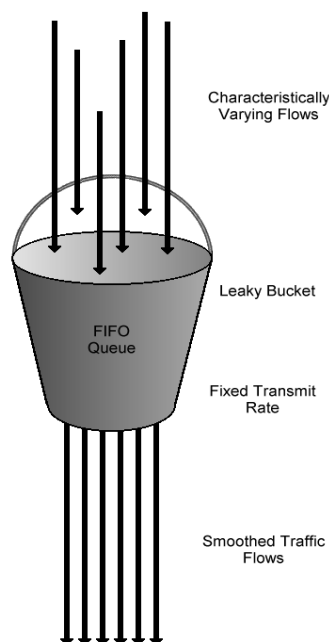


Figure 7. “Leaky” bucket algorithm [7]

4.2. Generation of ALTI pattern file

The user can generate ALTI pattern files, which contain TTC signals in the required ALTI format. The type of trigger rate can vary from clocked test pulses (figure 8), where the distance between consecutive test pulse signals is fixed throughout an LHC orbit, to random test pulse signals, where the arrival of a test pulse signal is random (figure 9).

```
#-----
#                               M
#                               u
#                               l
#                               t
#                               i
#                               p
#                               l
#   CCC                         i
# BRRR   T BBBB TTT   c
#O UEEE   T GGGG TTTL i
#R SQQQ   Y 0000 RRR1 t
#B Y210   P 3210 321A y
#-----
1 0000 0x00 0000 0000 40 # orbit signal
0 0000 0x00 0000 0000 11
0 0000 0x00 0001 0000 1 # BCR
0 0000 0x00 0000 0000 347
0 0000 0x00 0100 0000 1 # test pulse signal
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1 # L1A signal
0 0000 0x00 0000 0000 355
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0001 1 # deadtime between signals
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 355
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 355
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 355
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 320
```

Figure 8. Clocked test pulse pattern generated at 100 kHz with 44 BC test pulse - L1A latency.

```
#-----
#                               M
#                               u
#                               l
#                               t
#                               i
#                               p
#                               l
#   CCC                         i
# BRRR   T BBBB TTT   c
#O UEEE   T GGGG TTTL i
#R SQQQ   Y 0000 RRR1 t
#B Y210   P 3210 321A y
#-----
1 0000 0x00 0000 0000 40 # orbit signal
0 0000 0x00 0000 0000 11
0 0000 0x00 0001 0000 1 # BCR
0 0000 0x00 0000 0000 431
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 39
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 3
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 39
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 101
0 0000 0x00 0100 0000 1 # test pulse signal
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1 # L1A signal
0 0000 0x00 0000 0000 569
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 294 # deadtime between signals
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 455
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 65
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 345
0 0000 0x00 0100 0000 1
0 0000 0x00 0000 0000 43
0 0000 0x00 0000 0001 1
0 0000 0x00 0000 0000 897
```

Figure 9. Random test pulse pattern generated at 100 kHz with 44 BC test pulse - L1A latency.

4.3. LHC beam structure

For the random mode of operation, implementation of the LHC beam structure on the generated data is possible (figure 10). Bunch Crossing IDs (BCIDs) of random test pulse – L1A signals are evenly distributed along an LHC orbit, in agreement with the LHC beam structure.

Additional histograms depict the probability of a bunch crossing to occur, which decreases exponentially over time with a mean rate inversely proportional to the frequency of a Bunch Crossing in each LHC orbit.

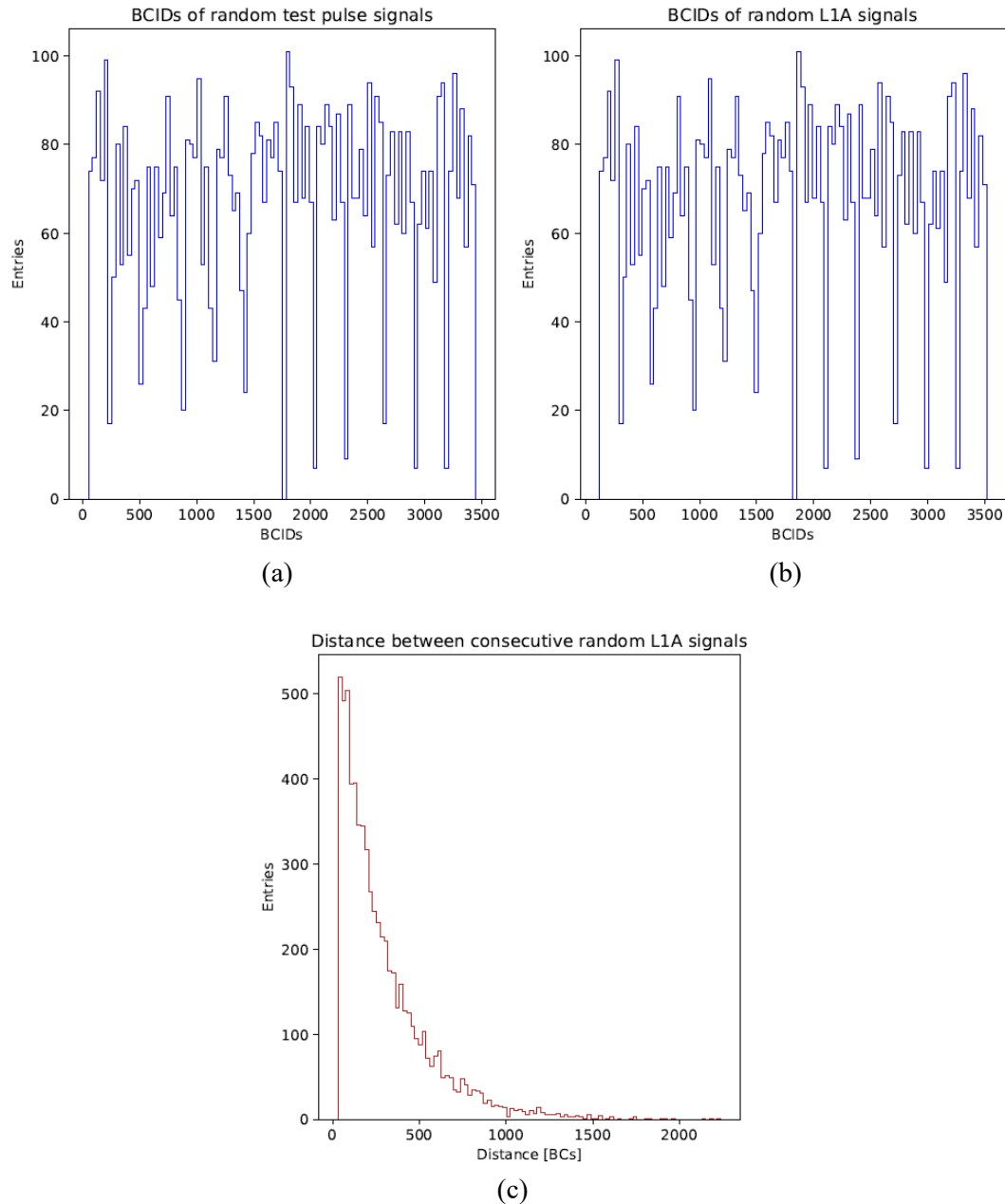


Figure 10. Histograms for random operation at 200 kHz, 70 BC test pulse – L1A signal latency. (a) BCIDs of random test pulse signals. (b) BCIDs of random L1A signals. (c) Distance between consecutive L1A signals.

4.4. ALTI pattern tests

In order to verify the program's functionality, ALTI was configured with pattern files at different rates, both for clocked and random operation. NetIO publish/subscribe system used was used to obtain distributed data from the Pad Trigger on the NSW sTGC trigger path. Test sequence is as follows:

- Test pulse and L1A signals are assigned a specific BCID in each orbit.

- ALTI forwards the TTC information, contained in these pattern files, through the optical TTC network to the Front-End Boards (FEB).
- At the VMM ASIC of the pad Front-End Boards, a test pulse is generated at the next BC.
- The signal is processed by the Trigger Data Serializer (TDS) on the FEB and arrives at the Pad Trigger three BC later.

The motivation behind these tests was to observe the required time differences between ALTI pattern BCIDs and outgoing data BCIDs from the Pad Trigger.

4.4.1 Analysis

Software development in C++ was used to decode received data while data analysis was performed using ROOT framework. In both modes of operation, the generated ALTI pattern files produced the expected time differences. In detail:

- Distance between test pulse BCIDs in the ALTI pattern file and test pulse BCIDs generated by the pad FEBs is observed at 1 BC for clocked operation (figure 11). For random triggers, this distance is not always stable (a behaviour that is still under investigation).
- Distance between test pulse BCIDs generated by the pad FEBs and the BCIDs of outgoing Pad Trigger data is at 3 BC, both for clocked and random operation (figure 12).

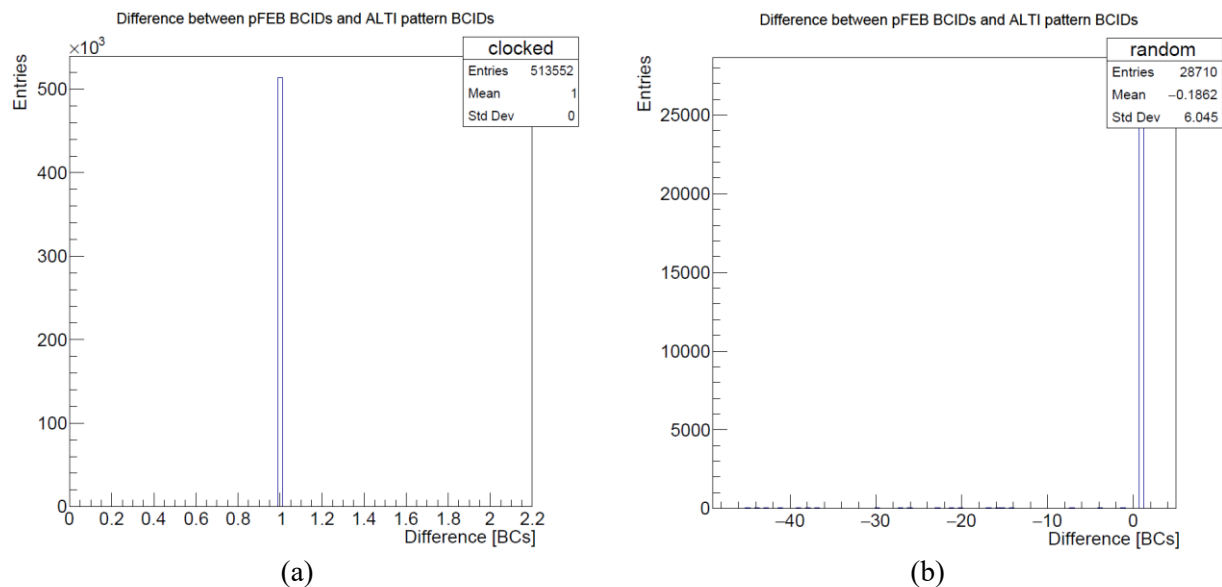


Figure 11. Time differences (pFEB BCIDs – ALTI BCIDs) at 10 kHz. (a) clocked test pulse signals. (b) random test pulse signals.

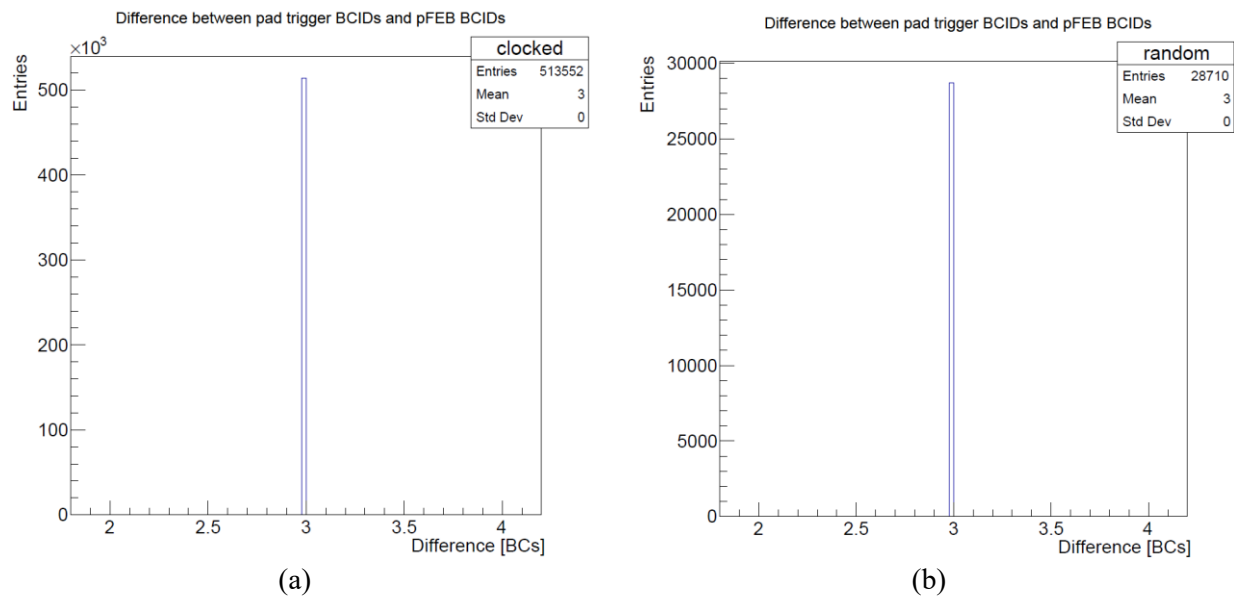


Figure 12. Time differences (pad trigger BCIDs - pFEB BCIDs) at 10 kHz. (a) clocked test pulse signals. (b) random test pulse signals.

5. Conclusion

A program has been created in order to configure the ATLAS Local Trigger Interface at the ATLAS experiment. The program is used by the NSW Trigger group, both for the Micromegas and the sTGC systems development, in order to test how the NSW Trigger electronics respond under the generated conditions. Results are promising for clocked and random triggers, produced by this program.

References

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