Published by IOP Publishing for Sissa Medialab

Received: *October 21, 2024*
Revised: *December 18, 2024*
Accepted: *January 23, 2025*
Published: *March 19, 2025*

Topical Workshop on Electronics for Particle Physics
University of Glasgow, Scotland, U.K.
30 September–4 October 2024

Development of high-speed serializer transmitters in 180-nm technology for CEPC vertex detector readout electronics

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Abstract: The TaichuPix chip, designed as a dedicated monolithic active pixel sensor for CEPC vertex detector R&D, requires a raw data rate of up to 3.84 Gbps and a power consumption of less than 25 mA/Gbps for the serializer circuit. The initial prototype TaichuPix1 achieved a maximum data rate of 3.36 Gbps but exhibited significant jitter and current issues. Subsequently, two 4-Gbps serializers were developed and optimized to meet the specified requirements. Despite encountering a bias issue initially, test results demonstrate that the root mean square (RMS) jitter of both phase-locked loop (PLL) clocks is less than 1.8 ps. A revision was implemented to address the bias problem by utilizing simple diode-connected transistors to provide the reference current. Tests conducted revealed a clear eye diagram at 4 Gbps, with a total jitter of 62.1 ps, power consumption of 151.2 mW, and the RMS jitter of the ROPLL less than 1.4 ps.

Keywords: Analogue electronic circuits; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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https://doi.org/10.1088/1748-0221/20/03/C03029

Contents

1 Introduction

In recent years, numerous research and development programs related to the proposed Circular Electron Positron Collider (CEPC) have been ongoing [1, 2]. The high luminosity levels associated with the collider present challenges for the vertex detector. TaiChuPix serves as a dedicated monolithic active pixel sensor designed for CEPC vertex detector research and development. It operates on a 180-nm CMOS imaging sensor technology with a final goal of achieving a spatial resolution better than 3 µm with high-speed readout capabilities [3]. The readout electronic features a 25-ns bunch spacing, 25-µm square pixel size, and a 512×1024 pixel-array scale, resulting in a 32-bit data format and a raw data rate requirement of 3.84 Gbps [4]. Following an 8b10b encoding process, the data width and rate increase to 40 bits and 4.8 Gbps, respectively.

The initial prototype, TaiChuPix1, exhibited a serializer operating at 3.36 Gbps with a total jitter of approximately 150 ps and a current consumption exceeding 100 mA [5]. To optimize performance, two 4-Gbps serializers were designed using a different 180-nm process, incorporating an architecture comprising a shift-register chain combined with a binary-tree structure. However, an issue with biasing arose during testing, causing problems [6]. Subsequently, a revision was implemented to address this bias issue. This paper primarily focuses on presenting the latest measurement results of the revised design and offers an analysis of the start-up issue related to the bias generator.

2 Design of the revision

2.1 Issue and modification of the first version

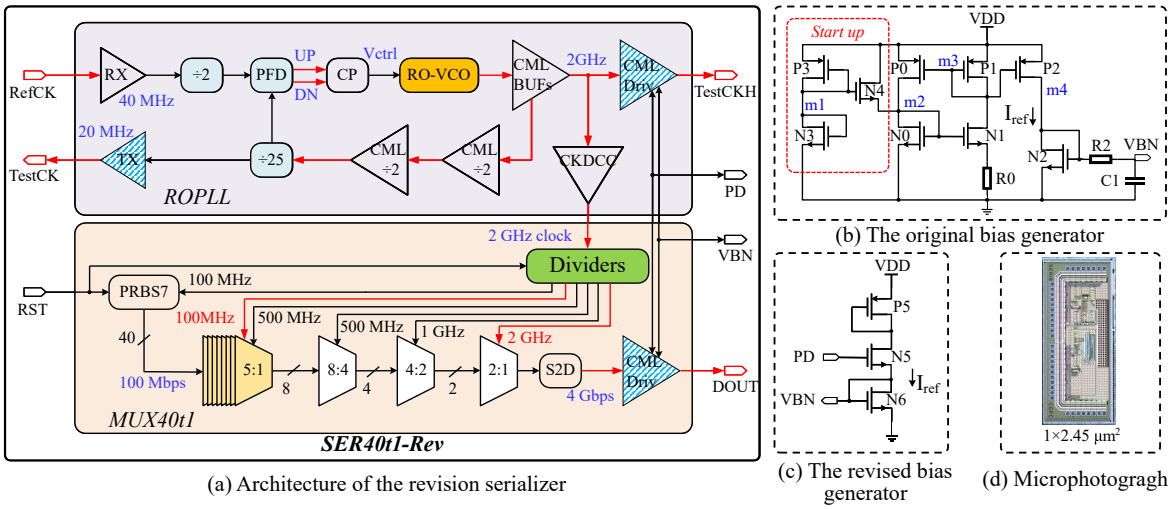
Figure 1 illustrates the schemes and microphotograph of the revision design (Ser40t1rev), which includes a ring-oscillated phase-locked loop (ROPLL) and a 40-to-1 multiplexer. Compared to the initial prototype [6], the overall scheme has been slightly modified due to the area limitation.

During the initial prototype measurements, a bias issue was identified where the 2-GHz output clocks and serial data outputs could not be detected stably and effectively. The same bias generator was utilized in various building blocks, such as the charge pump (CP), clock and data outputs drivers

(CMLDriv), and the LC voltage-controlled oscillator (VCO). Each bias generator had a different R0 value, and the CP bias generator did not have an RC filter (R2 and C1). Test results showed that the ROPLL functioned normally, but random abnormal behavior was observed in the LCVCO and CMLDrivs. In such a case, the clock random jitter (Rj) of the ROPLL was measured using a 20-MHz test clock (TestCK), which was less than 1.8 ps [6].

For the LCPLL and serial data outputs, the power supply was increased to 2.6 V, resulting in some chips obtaining effective signals. The measured clock Rj of the LCVCO was around 1 ps, both serial outputs were correct, and the measured total jitter (Tj), eye height, and eye width of the 4-Gbps eye diagram were 145.2 ps, 150 mV, and 0.729 UI (unit interval), respectively [6].

In the revised design, CML drivers utilize simplified diode-connected NMOS and PMOS transistors (N6 and P5) arranged with a switch N5 to provide the reference voltage (VBN) of the NMOS-current tail in each stage, as shown in figure 1(c). Figure 1(b) displays the original bias generator. The simulated overall current at 4 Gbps is about 78 mA.



(a) Architecture of the revision serializer

(b) The original bias generator

(c) The revised bias generator

(d) Microphotograph

Figure 1. Schemes and microphotograph of the revision serializer.

2.2 Analysis

In the previous analysis, we initially believed that the issue stemmed from the bias generator, leading to a start-up anomaly. However, further long-time simulations failed to reproduce the anomaly. Figure 2(a) displays post-simulation waveforms of the old bias generator with and without the start-up circuit. With the start-up circuit, node voltages such as m2 to m4 stabilize after 3 μs, while without it, they stabilize after an additional 9 μs. The R2-C1 filter suppresses bias noise but prolongs the stability time. However, theoretically, the filter should not impact the start-up operation. The top waveform in figure 2(b) provides evidence that the CMLDriv functions normally with a single-end amplitude of about 409 mV, albeit with an extended stability time (nearly 15 μs). The revised bias generator is simplified without considering start-up, which helps identify the anomaly related to start-up issues, but it is more sensitive to the power supply. It is used in the CML driver, which mainly transmits a data stream containing large digital signals, hence the impact of process-voltage-temperature (PVT) and power supply rejection ratio (PSRR) can be disregarded. But the simplified bias generator is not suitable for the LCVCO, which requires a stable and low-noise biasing current, such as a bandgap

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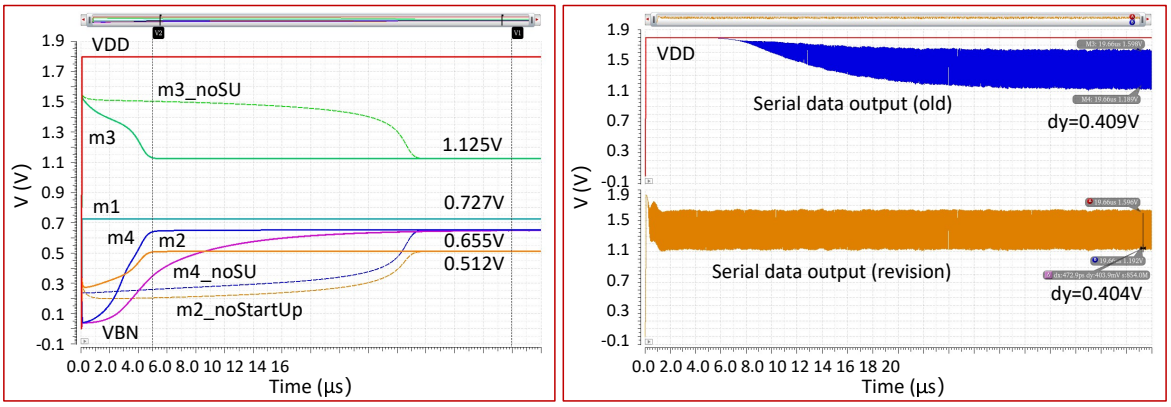
reference. However, bandgap circuits should also consider the start-up issue. The bottom waveform in figure 2(b) depicts one of the revised CMLDriv outputs.

DC and corner simulations also fail to identify the bias issue. Consequently, we are unable to determine if it functions after modifying parameters of some devices. In fact, the same structure of the bias generator, with slight parameter differences, was utilized in the TaiChuPix and also in other processes and designs, without any anomalies observed. In this scenario, using such a commonly used bias generator in future designs based on the same process poses a risk.

The initial prototype chip consists of two different designs, whereas the revised design only focuses on one of them. It is because the tapeout process for the revision design does not support the inductor device required for the other design based on the LCPLL. It is expected to offer improved jitter performance. Therefore, we intend to utilize the focused ion beam (FIB) technique to make modifications to some routings for additional verification of the biasing issue, as well as to assess the effects of using an external bias for the LCPLL. Initially, we plan to sever the connections between the IOs and the enable or power-down signals for the LCVCO and two CML drivers, and then connect them to nearby power or ground. Subsequently, we will connect the three VBNs (as shown in figure 1(b)) of the bias generators to the available IOs for external bias overriding. However, the evaluated yield of the FIB schemes was only 50%. We are continuing our efforts to explore other FIB companies for higher yield or accept the 50% risk.



(a) Start-up simulations of the old bias generator (b) Comparision of the CMLdriv outputs

Figure 2. Transient waveforms of the start-up simulations.

3 Measurements

Figure 3 shows the test setup. The clock and serial data are tested by a 16-GHz wide-band oscilloscope (LeCroy SDA 816Zi-A) via SMA connectors and 0.5-m coaxial cables. The chip power supply (1.8 V) is provided by a TLV1117 chip on the PCB board, while the input power supply (3.3 V) is sourced from the GPD 4303S. The reference clock for the PLL is generated by a pulse/pattern generator (Agilent 81130A). The revision functioned normally. And the total current measured for the die is approximately 84 mA at 4 Gbps, excluding additional test blocks, which is 6 mA higher than the post-simulation value, primarily to the CML driver with a measured current of 38 mA.

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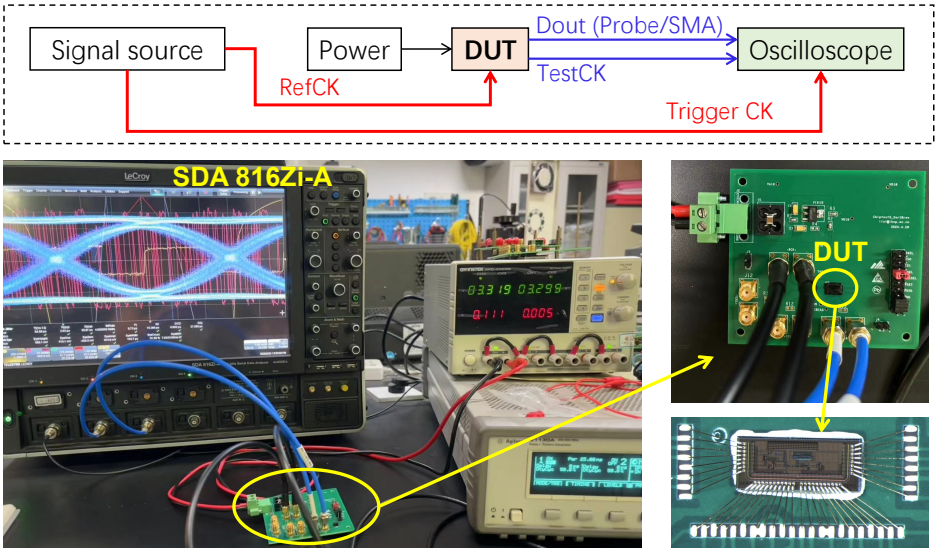

Figure 3. Test setup.

3.1 Performance of the clock

Figure 4 shows the measured performance of the 20-MHz test clock. The locking frequency range of the PLL spans from 0.33 to 3.07 GHz. The Rj of the 40-MHz reference clock is measured to be 2.65 ps by the oscilloscope, while the Rj of the 20-MHz test clock is less than 2.1 ps under the smallest loop bandwidth (S-LBW = 0.5 MHz), slightly larger than in previous tests of the initial prototype. The 2-GHz test clock was also tested with Rj less than 1.4 ps.

Additionally, a spectrum analyzer (Agilent N9320B) and the spectrum analyzer tool in the oscilloscope were utilized to characterize the clock performance [7]. The N9320B received one of the differential outputs and obtained phase noise values at various offset frequencies. Figure 5 displays the measured phase noise curves of the ROPLL and a post-simulation curve of the free-running VCO. The results reveal that the phase noise at a 1-MHz frequency offset (PN-1M) is approximately -94.2 dBc/Hz at the S-LBW, which is 8.7 dBc/Hz higher than the simulated value of the VCO.

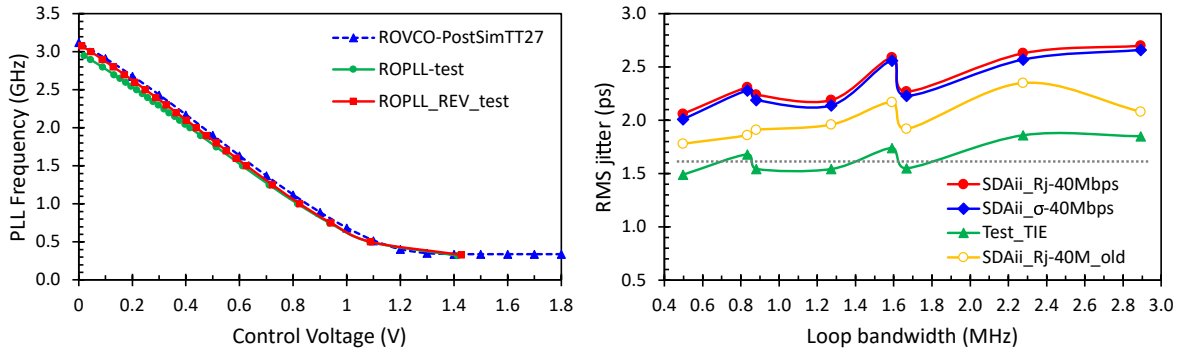

Figure 4. Frequency range (left) and jitter performance (right) of the 20-MHz test clock @1.8 V.

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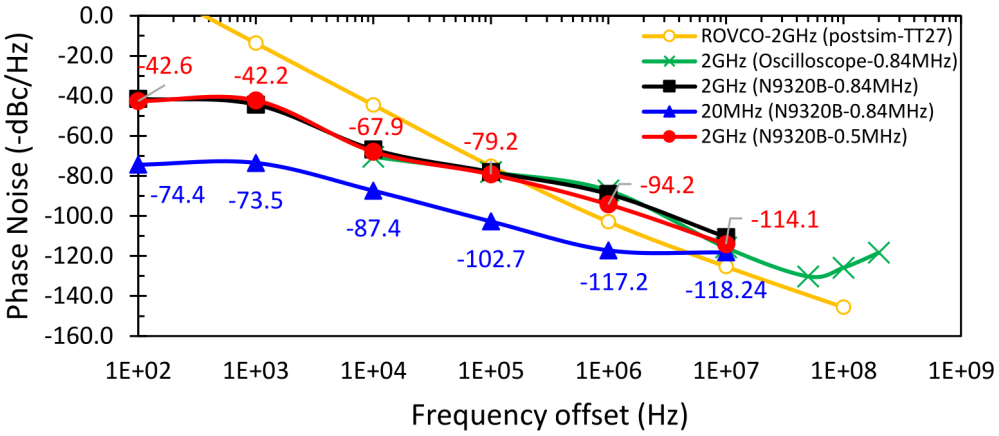

Figure 5. Phase noise curves.

3.2 Performance of the serial output

Timing of the revised serializer operated normally at a data rate of up to 5.2 Gbps. However, the driving capability of the classical CML driver proved to be insufficient as the data rate increased. The driving requirements are dependent on the actual application, and techniques for driving enhancement will be considered for future upgrades [8]. For the 4-Gbps transmission application, the current design meets the speed and power consumption requirements.

Figure 6 displays measured eye diagrams at data rates of 4, 4.8, and 5.2 Gbps, with a 3.92-Gbps eye of the TaiChuPix1 provided for comparison. At 4 Gbps, the measured Rj, Tj, eye height, and width are 1.5 ps, 62.1 ps, 576.3 mV, and 0.843 UI, respectively. At 4.8 Gbps, the eye is still clear with a Tj of 64.7 ps, but the driving capability needs enhancement. Further tests will be conducted later, including bit error rate (BER), irradiation, and FIB tests.

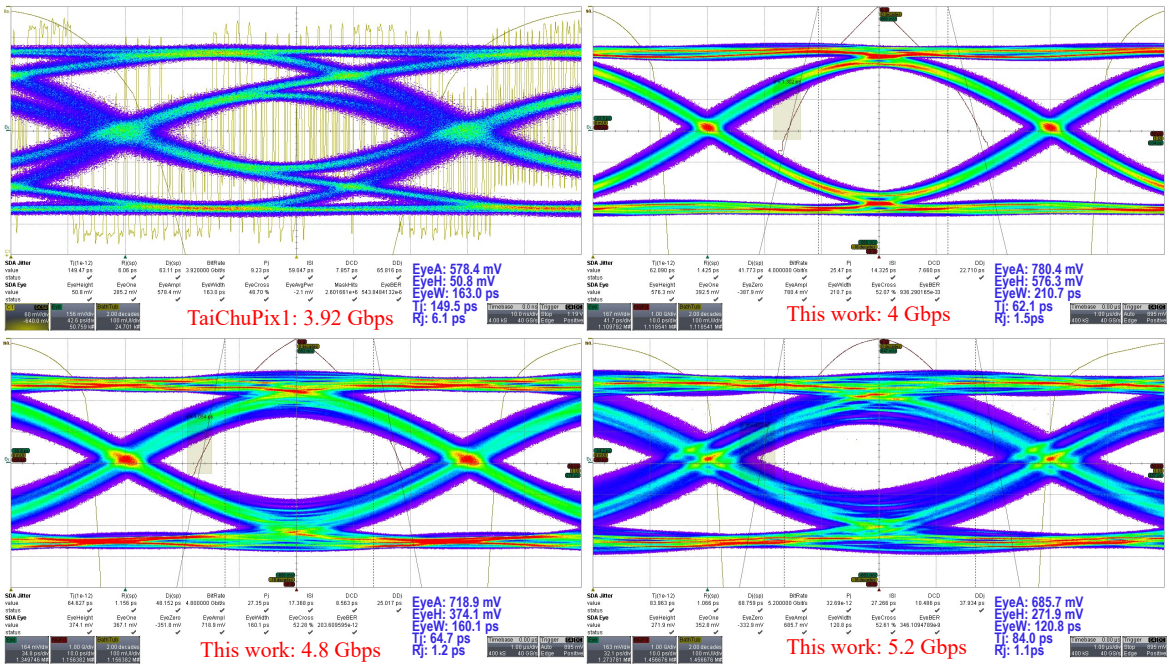

Figure 6. Eye diagram measurements (0.5-m cable).

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4 Conclusion

The prototype and revision designs confirmed that the internal CMOS transmission timing sequence supports data rates up to 5.2 Gbps at least in a 180-nm process node; however, the driving capability probably requires enhancement. Additionally, we are continuing our efforts to correct the prototype chip using FIB to facilitate further debugging and measurements, despite the yield of the FIB approach being only 50%. Next, the CEPC vertex detector R&D for the readout electronics will transition to a 65 nm technology, aiming for a spatial resolution better than 3 µm and lower power consumption. Our current design schemes and experiences will serve as valuable references.

Acknowledgments

This work was supported in part by the funding of the National Natural Science Foundation of China (No. 12005245 and No. 22127901), and the independent deployment project of Institute of High Energy Physics, Chinese Academy of Sciences (No. 2023000134). It was also partially funded by the National Key Research and Development Program of China under Grant No. 2018YFA0404302 from the Ministry of Science and Technology, the Scientific Instrument Developing Project of the Chinese Academy of Sciences (No. ZDKYYQ20200007), the Youth Innovation Promotion Association of the Chinese Academy of Sciences (No. Y201905), and the State Key Laboratory of Particle Detection and Electronics (No. SKLPDE-ZZ-202315).

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