MexSIC, a Data Acquisition Channel for SiPMs

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***Abstract*— This work describes MexSIC, a data acquisition (DAQ) channel designed for silicon photomultipliers (SiPMs), composed of a mixed-mode application-specific integrated circuit (ASIC) front end, a field programmable gate array (FPGA)-based processing stage, and a user interface. The ASIC provides a 1-bit sigma-delta modulator ($\Sigma\Delta - M$) digital equivalent of the input SiPM current, a flag indicating the start/end of the SiPM pulse, and a clock reference generated by an internal phase-locked loop (PLL). At the ASIC input stage, the SiPM current is converted to voltage by means of a 1.57-GHz bandwidth (BW) transimpedance amplifier (TIA), the gain of which can be switched between 21 and 48 dB, allowing for an input current range between 20 μA and 20 mA. The generated voltage signal is then fed to a trigger unit (TU) implemented to discriminate between desired signals and the spurious ones and, in parallel, also to a second-order $\Sigma\Delta$ modulator providing 6.1 effective number of bits (ENOB). The TU circuit sends a start/end bit flag by comparing the SiPM voltage signal with an 8-bit programmable voltage reference. $\Sigma\Delta$ was selected to have a single output line instead of using a data bus with many lines, which is important in applications where the number of SiPM channels being read out is very large. The 10-MHz BW $\Sigma\Delta - M$ uses an oversampling ratio (OSR) of 50 and a 1-GHz sampling clock that is generated by a PLL using an off-chip 100-MHz reference. The FPGA receives the ASIC $\Sigma\Delta$ modulated output signal and performs a decimation process by means of a cascade integrator comb (CIC) filter to complete the data recovery. The recovered signal is visualized in a MATLAB-programmed graphical user interface (GUI). The MexSIC ASIC was designed in a 180-nm CMOS standard process using Cadence software, and the processing stage was implemented in a Kintex-7 FPGA.**

***Index Terms*— Decimator, field programmable gate array (FPGA), front end, modulator, readout, silicon photomultiplier (SiPM), transimpedance amplifier (TIA).**

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I. Introduction

In recent years, the development of silicon photomultipliers (SiPMs) has had significant advances, whereby they proved to be a good alternative to traditional photomultiplier tubes (PMTs), mainly due to their much lower operating voltages, robustness, compactness, low sensitivity to magnetic fields, and the ability of operation at cryogenic temperatures [1]. Applications based on the use of SiPMs as radiation detectors range from medical imaging (e.g., hybrid positron emission tomography (PET)/magnetic resonance imaging (MRI) [2]), hazard/threat detection, applications in high-energy physics, neutron detectors [3], observational astronomy (e.g., in atmospheric Cherenkov telescopes (ACTs) [4]), or light detection and ranging (LiDAR) [5], to mention just a few. To make the most of the advantages offered by SiPMs, it is necessary to use readout and signal processing electronics, normally integrated into an application-specific integrated circuit (ASIC), which allows for the conditioning, filtering, and subsequent digitization of the signals delivered by SiPMs, especially in those cases where the number of channels is very high, as discussed, for example, in [6], [7], [8], and [9].

The first generation of SiPM readout chips includes the future linear collider (FLC) [10], fabricated in 0.8-μm CMOS technology. Allowing 18 input channels, it is composed of a charge preamplifier and a capacitor resistor – resistor capacitor capacitor (CR-RC^2) shaper. Another example is the SiPM integrated read-out chip (SPIROC) [11], [12], fabricated in a 0.35-μm silicon germanium (SiGe) technology, designed for 36 input channels, and capable of performing charge and time measurements. Both readout chips were designed for the International Linear Collider (ILC) Analog Hadronic Calorimeter [10]. The second generation of SiPM readout ASICs, led by Weeroc company [13], became more complex. These are the cases of the Maroc and the Citiroc 1A chips, both fabricated in a 0.35-μm SiGe technology. The Maroc was implemented in the ATLAS luminometer [14], [15], and it consists of 64 input channels, 64 trigger outputs for time-over-threshold (ToT) measurements, and one multiplexed analog charge output based on pulse shapers. Likewise, the Citiroc 1A was used in the Cherenkov ASTRI dual-mirror

small-size telescope (ASTRI SST-2 M) prototype [16] and also for amplitude measurements in [17]. The Citiroc 1A was designed to support 32 input channels, and it is capable of performing charge measurements using SiPM output peak current shapers, peak detection, and time triggering. Moreover, the second generation also includes ASICs used for time-of-flight (TOF) measurements in PET (TOF-PET) applications. Examples of this kind of ASICs are the TOFPET2 chip, fabricated in a 110-nm CMOS technology [18], the BASIC family [19], [20], ANGUS [21], or the Triroc [22] ASICs.

Despite that most of the SiPM readout ASICs measure the charge generated in each SiPM output pulse using voltage mode peak shapers as the input stage and calculate the TOF and ToT values of those pulses by means of time-to-digital converters (TDCs), new ASIC design techniques have been explored in the past years. The work proposed in [23] places a 1-bit sigma–delta modulator inside the input integrator to create a circuit-based charge-to-digital converter (QDC). In [24], a low-impedance fully current-mode analog front end was designed to achieve high-precision charge readout over a large dynamic range, while a similar approach was undertaken by Tang et al. [25] with the only difference that it requires an SiPM yielding a fast output.

In this case, the application vehicle on which the present work is focused is the development of a data acquisition (DAQ) front-end electronics module to be used by an SiPM-based ACT, designed to detect cosmic gamma rays with energies ranging between several hundred GeV and up to about 10 TeV using the imaging atmospheric Cherenkov technique (IACT). The IACT detects very short flashes of Cherenkov radiation generated by the cascade of relativistic charged particles produced when a very-high-energy gamma ray (or a hadron) strikes the atmosphere, yielding radiation in the spectral range between 260 and 900 nm with a peak wavelength of 330 nm and a duration of approximately 1 ns for muons and 3 ns for high-energy gamma rays while 5–20 ns for accompanying hadron showers.

The actual discrimination between the different particles creating the Cherenkov radiation flashes is carried out based on the form of obtained maps of detected Cherenkov flashes, these having a well-defined ellipsoid form in the case of gamma-rays, and a less defined form in the case of hadrons. This characteristic calls for the development of Cherenkov images, mapping the detection outputs of individual SiPMs.

Previous developments, as described in [4] and [26], were carried out in the frame of the First G-APD Cherenkov Telescope (FACT) project [27]. In the application addressed in this work, an image sensor comprising 1440 SiPMs is proposed, broken down into a set of individual SiPM miniarray modules. As reported in [26], in a camera with 1440 sensors, a rate of avalanches per channel (SiPM) of between 50 Mcps/cm^2 on "dark" nights and up to 2 Gcps/cm^2 on "full-moon" nights is expected to be induced by the diffuse night-sky background (NSB) photons [4].

Based on previous experiences, the SiPMs are operated in this case at a gain of 7.5×10^5, with a peak photon detection efficiency (PDE) of 33% between 450 and 500 nm and a crosstalk probability of 13% [4]. In this project, On-Semiconductor SensL MicroFJ-30035-TSV SiPMs [28] were chosen. They have a 3.07×3.07 mm^2 active area and are based on a p$^+$-on-n silicon foundry process, yielding a breakdown voltage of roughly 24.4 V, having 5676 microcells per SiPM with a size of 35 μm^2 and a microcell fill-factor of 75% [28]. Moreover, the SiPMs chose to deliver a typical dark current of 230 nA measured on average at 2.5 V of overvoltage and at a room temperature of 21 °C. A dark current rate (DCR) obtained for the same operating conditions is 50 kcps/cm^2 on average, yielding 1.35×10^{-4} average dark counts within a 3-ns Cherenkov flash or 9×10^{-4} dark counts in average within a 20-ns Cherenkov flash [28].

The maximum output current for the chosen SiPMs is 10 mA at the anode-cathode output, delivering an average output quenching time constant typically of 250 ns, considering the anode output capacitance for the entire through silicon via (TSV) package of 1.07 nF. If 1×1 cm^2 light concentrator lenses are used in front of every SiPM, the NSB values translate into 0.15 counts for a gamma-caused Cherenkov burst of 3 ns or up to one count for hadron-caused Cherenkov burst of up to 20 ns on "dark" nights and six counts for a gamma caused Cherenkov burst of 3 ns or up to 40 counts for hadron caused Cherenkov 20-ns-long bursts on "full moon" nights. On the other hand, as reported in [26], an average signal in a single gamma event impinging a single SiPM with an active area of 1 cm^2 including the NSB is between 72 Gcps and 2.9 Tcps or 216 signal counts in a 3-ns-long Cherenkov flash that results equivalent (at a gain of 7.5×10^5) to 162×10^6 electrons or a pulse charge of 25.9 pC on one extreme and 8700 signal counts equivalent to 6.5×10^9 electrons or a charge of 1.04 nC in the same flash signal on the other extreme. The manufacturer reports a crosstalk probability of 8% and an after-pulsing probability of 0.75%, which have to be considered with the DCR.

Thus, if the minimum signal to be detected is considered adding the DCR, crosstalk, after-pulsing, and NSB contributions at a "dark night" within a 3-ns-long Cherenkov flash signal, it yields an average of 1.15 counts, while the maximum signal within a 20-ns burst measured during a "full-moon" night delivers 8746 counts in average. The latter indicates a required system dynamic range of approximately 77.6 dB. One additional restriction for the ASIC developed was the chip area, limited to 2×2.5 mm^2, which imposed the necessity of reducing the number of I/O pins to an absolute minimum.

Considering the above information, this work presents an approach based on a 1-bit sigma–delta modulator used for QDC measurements and is organized as follows. Section II discusses the required bandwidth (BW) of the input transimpedance amplifier (TIA) to acquire and digitize the current mode signals delivered by the SiPM. Section III presents the proposed architecture for the entire MexSIC single-channel readout system composed of a mixed-signal ASIC, a field programmable gate array (FPGA) digital filter/decimator, and a MATLAB digital user interface. Section IV describes the testbench used for the system characterization and the measurement results obtained. Finally, Section V poses a set of final remarks.

II. Importance of Proper Bandwidth Selection for Signal Processing in SiPMs

The appropriate selection of BW in the input amplification stage is critical for detecting photogenerated charge in SiPM-based radiation detectors. These devices are sensitive and capable of near single-photon counting, generating

electrical signals that are proportional to the accumulated charge. Given that these signals are short in duration, a wide BW is required to capture most of the charge level without significant loss. A key challenge lies in determining the optimal BW necessary for the specific task at hand.

The SiPM signal can be modeled as a time function $s(t)$, to which a Fourier transform $S(f)$ can be applied to encompass all its frequency content. To preserve the shape and information of the signal, the detection system's BW must be greater than or equal to the maximum significant frequency of the signal ($f_{\max}$), i.e., BW $\geq f_{\max}$. However, the nonperiodic nature of SiPM signals implies that they lack a fixed fundamental frequency and exhibit broad frequency spectra. This contrasts with periodic signals, where energy is concentrated in discrete harmonics. SiPM signals, generated by photon detection, consist of random pulses varying in amplitude and time occurrence, reflecting the random arrival of photons. Consequently, determining the appropriate BW for these signals is particularly challenging. Unlike periodic signals, which allow for more straightforward spectral analysis, SiPM signals necessitate an approach that considers their temporal variability, leading to a frequency spectrum that can theoretically extend to infinity.

One way to approximate this BW issue is to model a time-domain SiPM signal as a square pulse. This simplified approach is beneficial because the spectrum of a square pulse is a sinc function, which also possesses infinite spectral content. The Fourier transform of a time-domain square pulse $x(t)$ of duration T_p is expressed in the following equation:

$$X(f) = \mathcal{F}\{x(t)\} = T_p \cdot \operatorname{sinc}(fT_p) = T_p \cdot \frac{\sin(\pi f T_p)}{\pi f T_p}. \quad (1)$$

Based on the intersymbol interference (ISI) theorem, which seeks to preserve the information (charge in our case) contained within a pulse while ensuring efficient use of BW, a raised-cosine filter can be applied to (1). This approach results in the time-domain pulse losing its square shape, as the rise and fall times are increased by a factor α known as roll-off. As a result, the effective BW expands to encompass the region where the filter influences the signal decay, as described in the following equation:

$$\mathrm{BW}_p = (1+\alpha) \cdot \frac{1}{T_p}. \quad (2)$$

Modeling the SiPM signal in this manner implies that any attempt to limit the BW may result in the loss of essential spectral components rather than direct distortions. Therefore, the challenge lies in striking a balance between capturing the maximum charge level while maintaining an acceptable noise level, taking into account the inherent complexity of these signals. The resolution of charge measurement Q and the ability to discern between individual photon events are both directly related to the temporal precision of the signal. The total charge Q can be computed using the following equation, where $i(t)$ is the current generated by the SiPM over the total integration time τ:

$$Q = \int_0^{\tau} i(t)\, dt. \quad (3)$$

According to (3), proper BW selection ensures that current pulses are accurately captured, allowing for correct integration and precise charge measurement. Insufficient BW may result in inadequate capturing of current pulses, thereby affecting the integrity of the measured charge. Moreover, the presence of thermal and dark current noise in a detection system is a critical factor that degrades charge resolution, especially if such noise is exacerbated by the BW of the input stage in the analog front end. In most analog front ends, electronic noise is considered to be uniformly distributed across the frequency spectrum (white noise) and can be modeled as an additional signal $n(t)$ that adds to the SiPM signal. The power of the white noise P_n is proportional to the BW of the front-end input stage (BW) and is described by the following equation, where k is Boltzmann's constant and T is the temperature in Kelvin:

$$P_n = k \cdot T \cdot \mathrm{BW}. \quad (4)$$

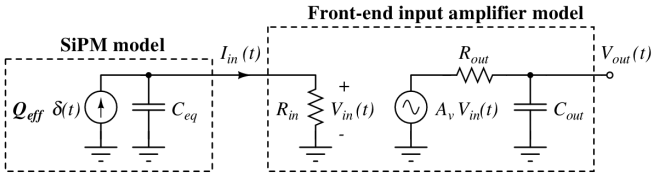


Fig. 1. Simulation model used to quantify the charge error function.

Based on (3) and (4), SiPM signal acquisition represents a significant tradeoff between BW and the noise generated by the input stage of the front end. An excessively wide BW will introduce more noise, which degrades the signal-to-noise ratio (SNR) and, consequently, the resolution of the detected charge. It is crucial to select a BW that minimizes noise without sacrificing important signal components, thus optimizing the SNR and ensuring accurate charge measurements.

Given the difficulty in mathematically defining the optimal BW for nonperiodic signals generated by SiPMs, a simulation-based modeling approach is proposed, as shown in Fig. 1. This approach allows for simulating operational conditions and the spectral characteristics of generated signals, evaluating different BWs and their impact on signal quality. The approach illustrated in Fig. 1 employs an electrical model of an SiPM along with an analog front end featuring an input resistance $R_{\mathrm{in}} = 50\ \Omega$ that converts the SiPM's input current $I_{\mathrm{in}}(t)$ into an input voltage $V_{\mathrm{in}}(t)$. The voltage $V_{\mathrm{in}}(t)$ is buffered to $V_{\mathrm{out}}(t)$ by a one-pole voltage amplifier with a gain of $A_v = 1$ V/V and BW $= 1/(2\pi R_{\mathrm{out}} C_{\mathrm{out}})$, where $R_{\mathrm{out}} = 50\ \Omega$ and C_{out} is swept to achieve BWs between 10 and 100 MHz. The *SiPM model* symbol in Fig. 1 embeds the seven-passive/one-active elements electrical model described by Turchetta [29] with all its parameters. However, other SiPM electrical models such as [30], [31], and [32] can be used.

By simulating the circuit depicted in Fig. 1, it can be observed how BW limitations affect charge detection accuracy, providing a clear view of the tradeoffs between BW and integration time. This tradeoff can be quantified using the charge error function ε_r described in (5), where Q_{in} is the ideal integrated charge and Q_{out} is the integrated charge limited by the amplifier's BW, both expressed in (6), where τ is the integration time and τ_{param} is a fraction of τ

$$\varepsilon_r = \frac{|Q_{\mathrm{out}} - Q_{\mathrm{in}}|}{Q_{\mathrm{in}}} 100\% \quad (5)$$

$$Q_{\mathrm{in}} = \frac{\int_0^{\tau} V_{\mathrm{in}} dt}{R_{\mathrm{in}}}, \quad Q_{\mathrm{out}} = \frac{\int_0^{\tau_{\mathrm{param}}} V_{\mathrm{out}} dt}{A_v R_{\mathrm{out}}}. \quad (6)$$

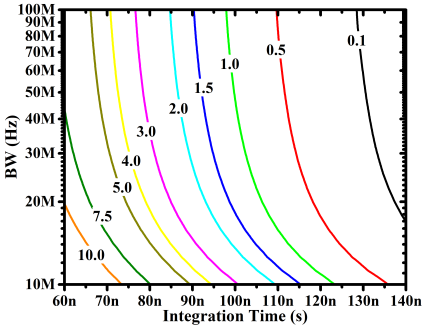


Fig. 2. Charge error as a function of BW and integration time.

Fig. 2 illustrates the performance of the front-end input stage as a function of the signal integration time and the amplifier's BW. The contour lines show the charge error, with the green line marking the 1% error. Notably, an amplifier designed with a BW of 10 MHz and an integration time of 124 ns can achieve the same precision level as the one with a BW of 100 MHz and an integration time of 97 ns, but with significantly less power consumption. This is because the longer integration time allows the amplifier to operate more efficiently, reducing power consumption.

III. System Architecture

The system-level architecture of the MexSIC DAQ channel for SiPM readout is shown in Fig. 3. It is composed of three main blocks: a mixed-mode front-end ASIC, an FPGA-based processing unit, and a user interface. The ASIC performs three tasks: 1) acquires and digitizes the current signal coming from the SiPM; 2) delivers a digital pulse whose width is proportional to the SiPM's event duration; and 3) generates a clock signal for ASIC/FPGA synchronization purposes. The FPGA is used to implement the downsampling and decimation process to reconstruct the SiPM digitized signal. Also, the FPGA sends the collected data to a PC via a serial port. The collected data are displayed on the PC's screen by means of a graphical user interface (GUI) developed in MATLAB.

A. Mixed-Mode Front-End ASIC Architecture

The proposed mixed mode front-end ASIC, as shown in Fig. 3 (left part), is made up of five building subsystems: a TIA, a sigma–delta modulator ($\Sigma\Delta - M$), a trigger unit (TU), a phase-locked loop (PLL), and bias circuits.

The TIA converts the $i_{\text{in}_{\text{TIA}}}$ current signal delivered by the SiPM into a $v_{\text{out}_{\text{TIA}}}$ voltage signal that is further amplified either by a 21-dB low-gain voltage path or by a 48-dB high-gain voltage path, leading to v_{lg} and v_{hg} output voltages, respectively. The v_{lg} and v_{hg} output voltages can be selected by employing an analog multiplexer (A-mux) that is ruled by a b_s control bit; $b_s = 0$ enables the low-gain path, while $b_s = 1$ activates the high-gain path. After that, the v_{lg} or v_{hg} signals are modulated in the sigma–delta domain to obtain a $v_{o_{\text{SD}}} = v^+_{o_{\text{SD}}} - v^-_{o_{\text{SD}}}$ differential voltage limited in a 10-MHz BW, 1-bit quantization level, and an oversampling ratio (OSR) of 50.

The TU sends a $v_{o_{\text{TU}}}$ digital pulse, the width of which maps the duration of the v_{hg} pulse when it crosses a v_{ref} threshold voltage level. The v_{ref} dc reference is created by a resistor 2-resistor (R2R) 8-bit digital-to-analog converter (DAC), and it is controlled by an 8-bit word coming from the FPGA.

The PLL delivers a 1-GHz clock signal, $v_{o_{\text{CLK}}}$, which is synthesized from a 100-MHz external reference. This $v_{o_{\text{CLK}}}$ clock is used by the sigma–delta modulator for sampling purposes, and it is used to synchronize the ASIC with the FPGA.

The $v_{o_{\text{SD}}}$, $v_{o_{\text{TU}}}$, and v_{CLK} signals are fed into an output buffer capable of switching at 1 GHz while matching a 50-Ω load. This load restriction was imposed to perform laboratory characterizations and to withstand the load provided by the FPGA's input pins. Also, the TU, $\Sigma\Delta - M$, and PLL use, each one, an independent bias circuit to isolate noise among them.

1) Bias Circuits: Fig. 4 presents the bias circuit used to generate the reference voltages, $V_{\text{BP}_{1,2}}$ and $V_{\text{BN}_{1,2}}$, inside the proposed ASIC. All transistors operate in the saturation region, except for m_{p_c} and m_{n_c}, and were sized using the g_m/I_D methodology [33]. From now on, all transistors will operate in the saturation region, except when indicated.

The $\Sigma\Delta - M$ and PLL are biased using two bias circuits, and their voltage reference nodes, $V_{\text{BP}_{1,2}}$ and $V_{\text{BN}_{1,2}}$, are loaded with very large metal oxide semiconductor - capacitor (MOS-CAP) to minimize/mitigate the injection of high-frequency harmonics, coming from the 100-MHz and/or 1-GHz clock reference, into the low-frequency circuits. To this end, m_{p_c} and m_{n_c} were sized very wide and very large. On the other hand, the TU uses a bias circuit without m_{p_c} and m_{n_c}.

2) Transimpedance Amplifier: The TIA comprises a two-output TIA (TO-TIA) and an A-mux. The TO-TIA is drawn in Fig. 5, and it is made up of an input transresistance preamplifier (black-dashed wide line box), a four-stage high-gain wideband voltage amplifier (red-dashed wide line box), and a two-stage low-gain wideband voltage amplifier (blue-dashed wide line box). The TO-TIA's symbol is shown at the bottom left corner in Fig. 5. All transistors operate in the saturation region, except m_c that works as a MOS-CAP and m_r that are used as very-large resistors.

The input transresistance preamplifier uses the transconductances $g_{m_{n1}}$ and $g_{m_{p1}}$ provided by the m_{n_1} and m_{p_1} input diode-like transistors to generate a $v_{\text{in}_{\text{TIA}}}$ voltage proportional to the $i_{\text{in}_{\text{TIA}}}$ current. This diode-like transistor parallel array offers the advantage of being dc self-bias, and the input current is conveyed by an input impedance equal to $1/(g_{m_{n1}} + g_{m_{p1}})$. The $v_{\text{in}_{\text{TIA}}}$ voltage is further isolated and amplified by the transistors $m_{n_{2,}p_2}$. The small-signal model of the input transresistance preamplifier is shown in Fig. 6, where $g_{m_1} = g_{m_{p1}} + g_{m_{n1}}$, $g_{m_2} = g_{m_{p_2}} + g_{m_{n_2}}$, $C_i = C_{\text{gs}_{p1}} + C_{\text{gs}_{n1}} + C_{\text{db}_{p1}} + C_{\text{db}_{n1}} + C_{\text{gs}_{p2}} + C_{\text{gs}_{n2}}$, and $C_a = C_{\text{gs}_{p3}} + C_{\text{db}_{p3}} + C_{\text{gd}_{p2}} + C_{\text{db}_{p2}} + 2C_{\text{gd}_{n2}} + 2C_{\text{db}_{n2}} + 2C_{\text{gs}_{p4}} + 2C_{\text{gd}_{p4}}$. Also, g_{m_i}, C_{gs_i}, C_{gd_i}, and C_{db_i} are the transconductance, gate–source capacitance, gate–drain capacitance, and drain-bulk capacitance of the ith transistor.

After solving the small-signal model in Fig. 6, a second-order transfer function is obtained, as shown in (7), where A_R is the transresistance gain, and a_1 and b_1 are coefficients described by (8) and (9), respectively. The locations of the zero, dominant pole, and nondominant pole are given by (10)–(12). Also, (8) reveals that the current-to-voltage conversion is performed by the preamplifier input impedance $Z_{\text{in}} \approx 1/g_{m_1}$, while the m_{n_2} and m_{p_3} transistors provide a small inverting gain of $1.5g_{m_2}/g_{m_3}$. Also, (11) shows that the preamplifier's BW is governed by the input and output

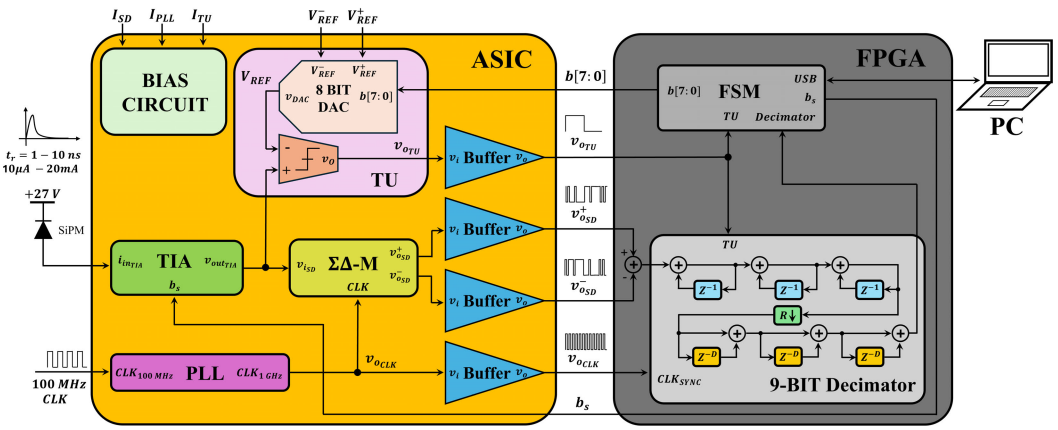


Fig. 3. MexSIC DAQ architecture.

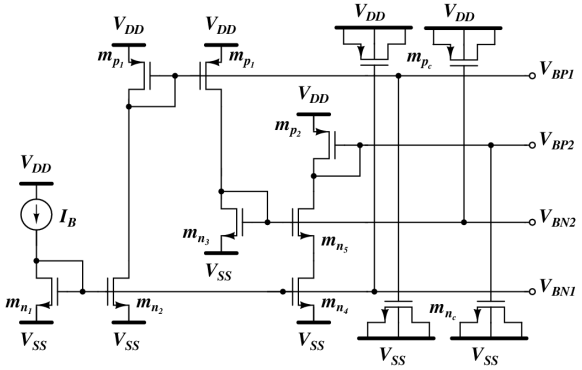


Fig. 4. Bias circuit.

capacitances C_i and C_a

$$\mathrm{TF}(s) = \frac{v_a(s)}{i_{\mathrm{in_{TIA}}}(s)} = A_R \cdot \frac{-\frac{2}{3}\frac{C_{\mathrm{gd}_2}}{g_{m_2}}s + 1}{a_1 s^2 + b_1 s + 1} \tag{7}$$

$$A_R = -\frac{1}{g_{m_1}} \cdot \frac{1.5\ g_{m_2}}{g_{m_3}} \tag{8}$$

$$a_1 = \frac{C_i(C_a + C_{\mathrm{gd}_2}) + C_a c_{\mathrm{gd}_2}}{g_{m_1} g_{m_3}}$$

$$b_1 = \frac{C_i g_{m_3} + C_{\mathrm{gd}_2}(g_{m_1} + 1.5\ g_{m_2} + g_{m_3}) + C_a g_{m_1}}{g_{m_1} g_{m_3}} \tag{9}$$

$$\omega_z = \frac{3}{2}\frac{g_{m_2}}{C_{\mathrm{gd}_2}} \tag{10}$$

$$\omega_{p_1} = -\frac{g_{m_1} g_{m_3}}{C_i g_{m_3} + C_a g_{m_1} + C_{\mathrm{gd}_2}(g_{m_1} + 1.5\ g_{m_2} + g_{m_3})} \tag{11}$$

$$\omega_{p_2} = -\frac{C_i g_{m_3} + C_a g_{m_1} + C_{\mathrm{gd}_2}(g_{m_1} + 1.5\ g_{m_2} + g_{m_3})}{C_i(C_a + C_{\mathrm{gd}_2}) + C_a c_{\mathrm{gd}_2}}. \tag{12}$$

Based on (8) and (11), the m_{n_1,p_1} diode-like transistors must be sized to meet three very important constraints. First, the input impedance of the transresistance preamplifier must be very low, $1/g_{m_1} \leq 50\ \Omega$, in order to ensure proper current transfer from the SiPM into the transresistance preamplifier. Second, the current-mode input range of the transresistance preamplifier can be extended by increasing the dc I_D drain current of the m_{n_1,p_1} input transistors. Third, by keeping I_D of m_{n_1,p_1} much higher than the maximum value of the current delivered by the SiPM, the transresistance preamplifier's BW can be considered constant due to the fact that the transconductance deviation of the m_{n_1,p_1} transistors is very small.

To fulfill these three constrains, and assuming a maximum $i_{\mathrm{in_{TIA}}}$ input current of 20 mA delivered by the SiPM, the drain current of the m_{n_1,p_1} transistors is set to $I_D = 40$ mA. This scenario, where $i_{\mathrm{in_{TIA}}}$ can be as large as half of the I_D biasing current through the m_{n_1,p_1} transistors, leads to a large signal behavior that causes deviations on the BW and the total harmonic distortion (THD) of the transresistance amplifier. Fig. 7 plots how the BW and THD of the transresistance amplifier change against the amplitude of the $i_{\mathrm{in_{TIA}}}$ current. Fig. 7(a) reveals that the BW remains quasi-constant from 2 μA to 20 mA, deviating the ω_{p1} location by a 18% factor. Also, from Fig. 7(b), THD values less than 1% can be found for $i_{\mathrm{in_{TIA}}} \leq 4$ mA from 100 kHz to 100 MHz. Likewise, a THD $\leq 1\%$ can be observed for $i_{\mathrm{in_{TIA}}} \leq 6$ mA at 1 GHz.

The high-/low-gain wideband voltage amplifier paths of the TIA, as depicted in the red/blue-dashed wide line boxes in Fig. 5, are composed of an input voltage buffer, an n-stage wideband amplifier, an offset cancellation servo loop, and an output voltage buffer. The input voltage buffers, m_{p_4} and m_{n_3}, isolate the v_a signal from the capacitive load imposed by the n-stage amplifier at node $v_{f_{1,2}}$, and it acts as a current-mode summing point. The n-stage broadband amplifier provides the overall voltage gain of each path by means of cascading n common-source voltage amplifiers: m_{n_4} and R_L. The offset cancellation circuit is confirmed by a very-large time-constant RC network, m_r and m_c, and a voltage-to-current converter, m_{n_5}. The offset correction at node $v_{b_{1,2}}$ is done by subtracting an $i_{f_{1,2}}$ very-low frequency error current from the $v_{f_{1,2}}$ node. The output buffer, $m_{p_{5,6}}$ and $m_{n_{6,7}}$, is used to isolate the $v_{b_{1,2}}$ node from the kick-back transients and noise coming from $\Sigma\Delta - M$ that is switching at 1-GHz frequency.

The $v_{\mathrm{hg,lg}}(s)/v_a(s)$ transfer function of the high-/low-gain paths can be computed by solving the block diagram presented in Fig. 8. Also, the denominator of the resulting transfer function can be approximated by a third-order polynomial, where the assumptions $C_f R_f \gg C_L R_L$ and $g_{m_{p4}} = g_{m_{n3}} = g_{m_{n5}}$ were applied. The transfer function of the high-/low-gain paths is described using (13), where a_1, b_1,

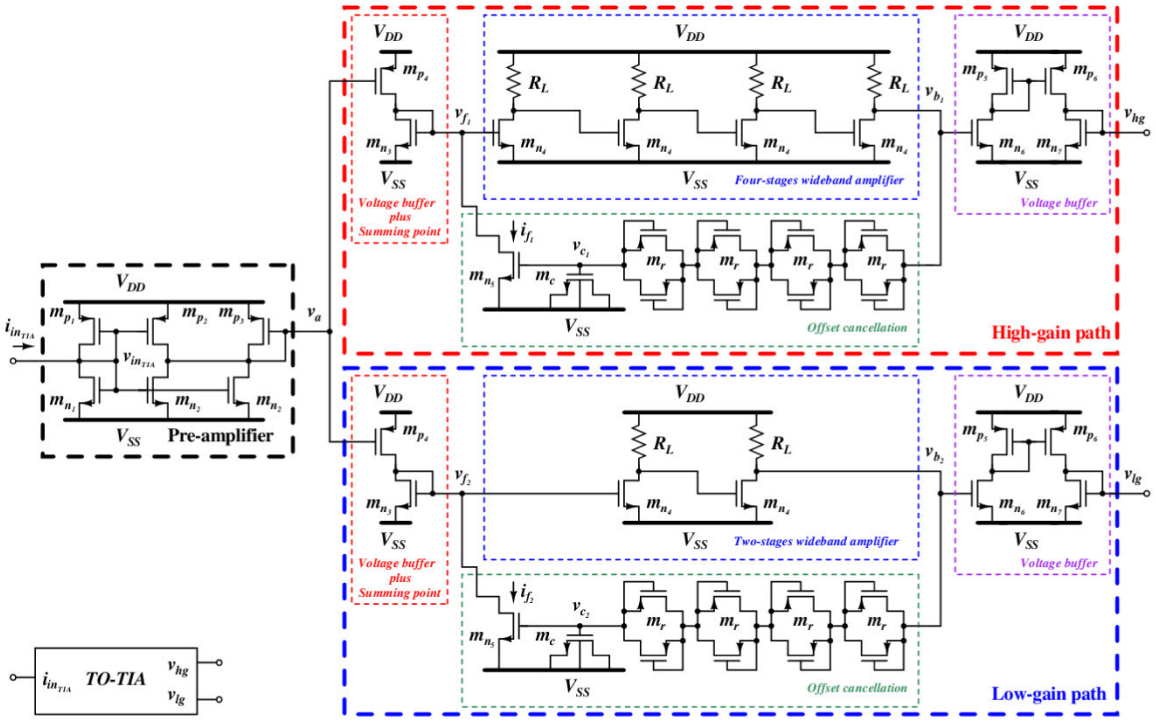


Fig. 5. TIA schematic circuit.

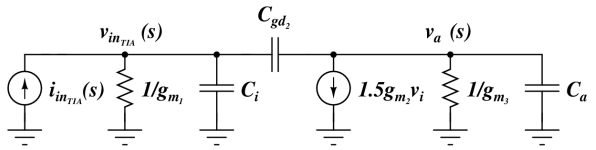


Fig. 6. Small-signal model of the transresistance preamplifier.

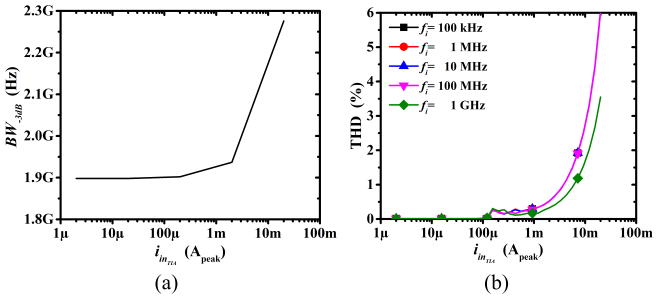


Fig. 7. Variation on (a) BW and (b) THD of the transresistance amplifier against the amplitude of the $i_{\mathrm{in_{TIA}}}$ current.

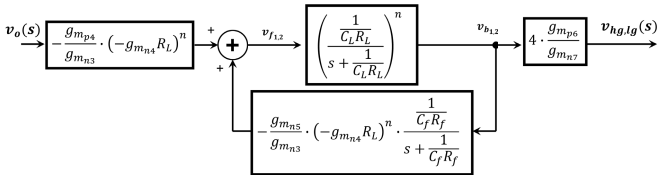


Fig. 8. Block diagram of the high-/low-gain paths.

and c_1 are the coefficients of the third, second, and first terms, respectively; such coefficients are given by (14). Also, $C_f = C_{\mathrm{gs}_c} + C_{\mathrm{gb}_c} + C_{\mathrm{gd}_c}$, $R_f = 2/g_{\mathrm{ds}_r}$, n can be 2 or 4, and $C_L \approx [(1 + g_{m_{n4}} R_L) \cdot C_{\mathrm{gd}_{n4}}] + C_{\mathrm{gs}_{n4}} + C_{\mathrm{db}_{n4}}$

$$\mathrm{TF}(s) = \frac{v_{\mathrm{hg,lg}}(s)}{v_a(s)} \approx -\frac{(g_{m_{n4}} R_L)^n}{(g_{m_{n4}} R_L)^n + 1} \cdot \frac{C_f R_f s + 1}{a_1 s^3 + b_1 s^2 + s + 1} \tag{13}$$

$$a_1 = \frac{(\frac{5}{2}n - 4)(C_L R_L)^2 C_f R_f}{(g_{m_{n4}} R_L)^n + 1}, \quad b_1 = \frac{n C_L R_L C_f R_f}{(g_{m_{n4}} R_L)^n + 1}$$

$$c_1 = \frac{C_f R_f}{(g_{m_{n4}} R_L)^n + 1}. \tag{14}$$

A brief overlook on (13) suggests a bandpass frequency behavior whose magnitude of the low-frequency stopband is limited by (15). After applying the dominant zero/pole approximation on (13), one left-half-plane (LHP) zero and three LHP poles are obtained. The locations of the ω_{z_1} zero, ω_{p_1} first pole, ω_{p_2} second pole, and ω_{p_3} third pole are given by (16)–(18), respectively,

$$|A_v| \approx \frac{4(g_{m_{n4}} R_L)^n}{(g_{m_{n4}} R_L)^n + 1} \approx 4 \tag{15}$$

$$\omega_{z_1} \approx -\frac{1}{C_f R_f} \tag{16}$$

$$\omega_{p_1} \approx -\frac{(g_{m_4} R_L)^n}{C_f R_f} \tag{17}$$

$$\omega_{p_2} \approx -\frac{1}{n C_L R_L}, \quad \omega_{p_3} \approx -\frac{2}{(n-1) C_L R_L}. \tag{18}$$

Fig. 9 presents the bandpass frequency response of the whole TIA drawn in Fig. 5 where the zero/pole locations are pointed out. As can be noted from Fig. 9, the servo loop used for offset corrections adds a ω_{z_1} zero and a ω_{p_1} pole that creates the low-frequency transition band, which also sets the lower cutoff frequency at ω_{p_1}; because ω_{z_1} and ω_{p_1} are

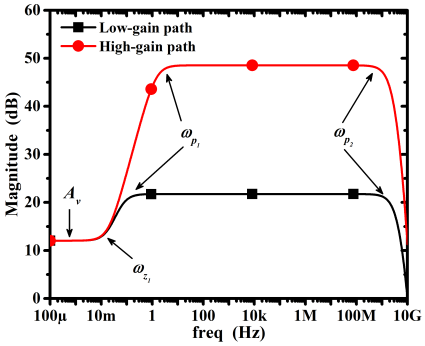


Fig. 9. Frequency response of the high-/low-gain paths.

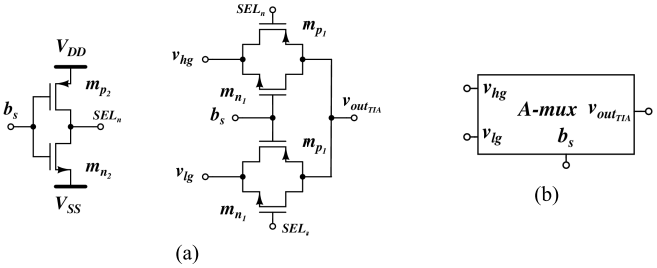


Fig. 10. Schematic circuit of the A-mux. (a) A-mux circuit. (b) Symbol.

ruled by the $C_f R_f$ product, their location is at extremely low frequencies. Also, the upper cutoff frequency is defined by the ω_{p_2} pole, while the passband gain is given by (19). The lower cutoff frequency, the upper cutoff frequency, and the transresistance passband gain of the high-gain path are 1.34 Hz, 1.57 GHz, and 13.3 kΩ, while the lower cutoff frequency, the upper cutoff frequency, and the transresistance passband gain of the low-gain path are 54 MHz, 2.6 GHz, and 610 Ω. It is worth mentioning that the upper cutoff frequencies of the high-/low-gain paths are very large because of the TIA's input signal current range that was set to 20 mA. However, the upper cutoff frequencies can be easily set to 10 MHz, as stated in Section II, at the expense of decreasing the input signal range

$$A_{v_{\text{pass}}} \approx (g_{m_{n4}} R_L)^n. \tag{19}$$

The output buffer is sized to provide a 4-V/V voltage gain while setting its output impedance, $Z_{\text{out}_{\text{TIA}}} = 1/g_{m_{n7}}$, ten times lower than $Z_{\text{in}_{\Sigma\Delta}}$, the input impedance of $\Sigma\Delta - M$. Thus, the output buffer must fulfill the $Z_{\text{out}_{\text{TIA}}} \ll Z_{\text{in}_{\Sigma\Delta}}$ condition.

On the other hand, the A-mux, as shown in Fig. 10, is used to select between the v_{LG} or v_{HG} trajectories by the b_s control bit; $b_s = 0$ enables the low-gain path, while $b_s = 1$ activates the high-gain path. The m_{n_1} and m_{p_1} transistors were sized to operate in the linear region and to have an $r_{\text{DS}_{\text{ON}}}$ drain–source ON-resistance 100 times smaller than $Z_{\text{in}_{\Sigma\Delta}}$. Thus, the $r_{\text{DS}_{\text{ON}}} \leq 0.01 \cdot Z_{\text{in}_{\Sigma\Delta}}$ relation must be accomplished in order to ensure proper voltage transfer. Also, the m_{n_2} and m_{p_2} transistors were sized to achieve a symmetrical high-to-low and low-to-high propagation delay times [34], $t_{p\text{hl}}$ and $t_{p\text{lh}}$, for a 1-MHz clock frequency.

3) Sigma–Delta Modulator: $\Sigma\Delta - M$ is used to digitize the $v_{\text{out}_{\text{TIA}}}$ voltage signal coming from the TIA. The $\Sigma\Delta$ architecture was chosen despite the advantages of alternative approaches including the successive-approximation-register (SAR) approach, pipeline, flash, and so on mainly due to the fact that its digitized output is encoded in only one serial bitstream, which means that it uses one transmission channel to send its data; one transmission line is used for single-ended mode operation, while two transmission channels are implemented for the fully differential mode. This feature contributes to the reduction of I/O pins in both the ASIC pad frame and the package.

The implemented $\Sigma\Delta - M$ is shown in Fig. 11(a). It is composed of a single-to-differential buffer (red-dashed line box on the left) and a continuous-time second-order 1-bit quantizer fully differential $\Sigma\Delta - M$ (black-dashed line box on the right) [35], [36]. $\Sigma\Delta - M$ in Fig. 11(a) was designed to achieve a 10-MHz BW and an OSR of 50 while using a f_s sampling frequency of 1 GHz. This BW value was selected based on the analysis carried out in Section II.

Fig. 11(b) shows the $\Sigma\Delta - M$'s block diagram used to obtain the signal transfer function (STF) for $v_{n_{\text{SD}}}(s) = 0$ and the noise transfer function (NTF) for $v_{i_{\text{SD}}}(s) = 0$. This diagram includes two blocks (the red block on the left and the blue one on the right), which add error mechanisms to the first and second integrators: the OTA's finite gain and the loading effect at the OTA's output. Both error mechanisms affect the summing point precision and the integrator accuracy.

Fig. 12 draws the STF and NTF that are described using the block diagram in Fig. 11(b). As can be seen, the STF BW peaks at 10 MHz, while the NTF presents a −73-dB rejection band from very-low frequencies to 100 kHz, caused by the OTA's finite gain and its loading effect. One side-effect of a limited rejection band in the NTF is the reduction in the amount of an effective number of bits (ENOB) of $\Sigma\Delta - M$.

Despite the quite acceptable response to ac input sinusoidal signals shown in Fig. 12, the integrators of $\Sigma\Delta - M$ must be capable of dealing with very-high-frequency sharp transitions set by a 1-GHz f_s sampling clock. Thus, the operational transconductance amplifier (OTA) used as an active element inside the integrators must have a gain–bandwidth product (GBW) large enough to process most of the harmonic content of a sampling square wave. To this end, the GBW of the OTA_2 should be greater than 5 GHz in order to bypass the $f_s + 3f_s + 5f_s$ harmonics. Fig. 13 presents the schematic circuit and symbol of the fully differential OTA used as integrator in $\Sigma\Delta - M$. The ac response of the OTA_2 shows a dc gain of 25.89 dB, a GBW of 6.64 GHz, and a phase margin of 83°.

Fig. 14 draws the schematic circuit and symbol of the latched-comparator used in Fig. 11(a). All transistors, nMOS and pMOS, were optimized to achieve a symmetrical $t_{p\text{hl}}$ and $t_{p\text{lh}}$ for a 1-GHz f_s sampling clock.

Considering that the intrinsic load for any CMOS digital gate is a capacitor, the output of the latched comparator is not capable of managing resistive loads. To overcome this issue, a buffer composed of four cascaded inverters was used to drive a $R_{f1} \parallel R_{f2}$ load. Fig. 15 presents the schematic circuit and symbol of the implemented four-stage buffer. The sizes of the transistors were obtained by using logic-effort and minimum-delay design techniques for a 500-MHz frequency.

The last circuit to describe the $\Sigma\Delta - M$ functionality is the single-to-differential buffer, which is illustrated in Fig. 11(a) (red-dashed line box). It is composed of two fully differential

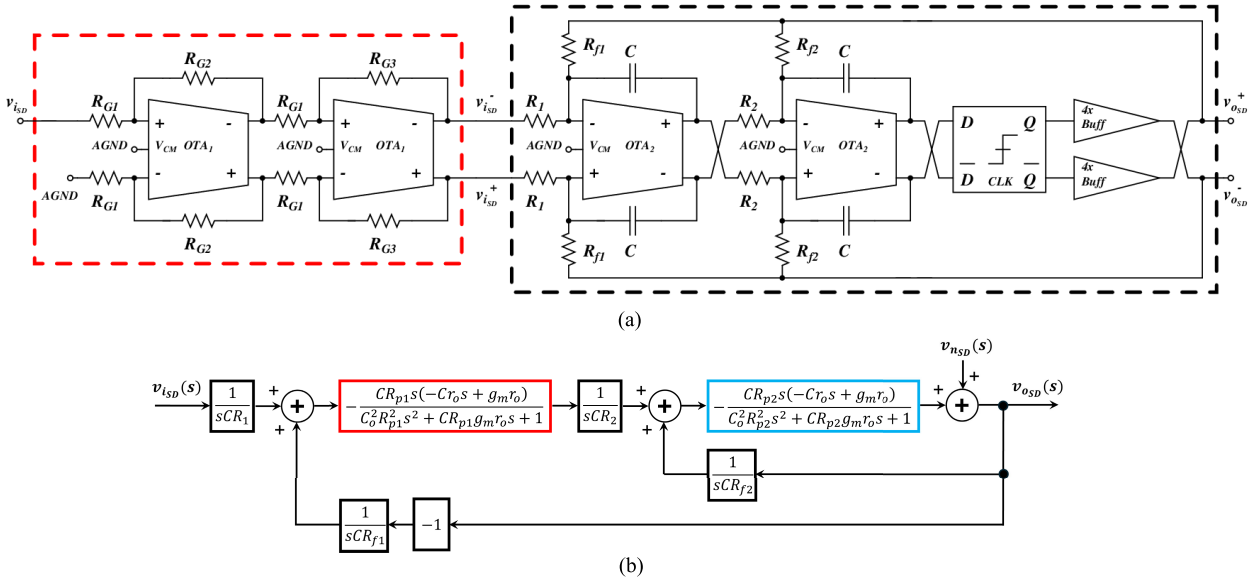


Fig. 11. Sigma–delta modulator. (a) Schematic circuit. (b) Block diagram used to compute the STF and NTF.

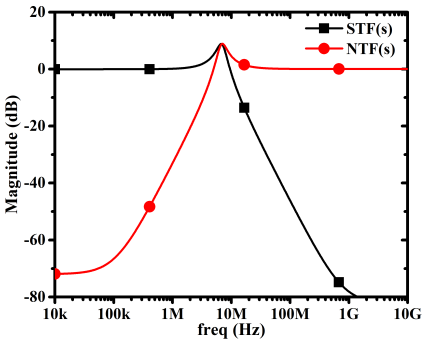


Fig. 12. Frequency responses of $\Sigma\Delta - M$.

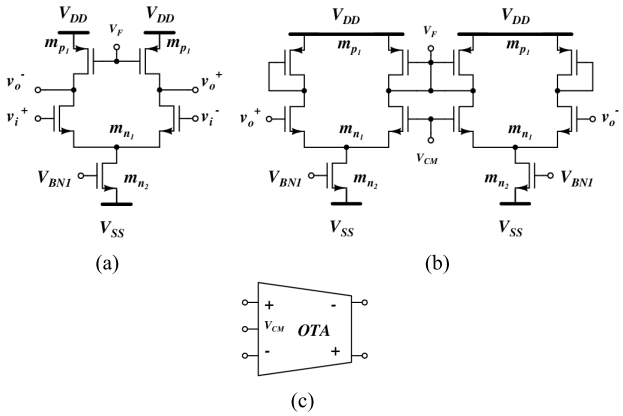


Fig. 13. Schematic circuit of the OTA_1 and OTA_2. (a) Fully differential OTA circuit. (b) Common-mode circuit. (c) Symbol.

inverter amplifiers. The first inverter amplifier transforms the single $v_{i_{SD}}$ voltage signal into a differential mode using a 0.5-V/V gain, while the second inverter amplifier boosts the resulting signal by a 2 V/V. Equation (20) presents the overall voltage gain of the single-to-differential buffer where $R_{G_{1-3}}$ are the gain resistors and ϵ_1 and ϵ_2 are the error functions due to the finite OTA's open-loop gain; ϵ_1 and ϵ_2 are described

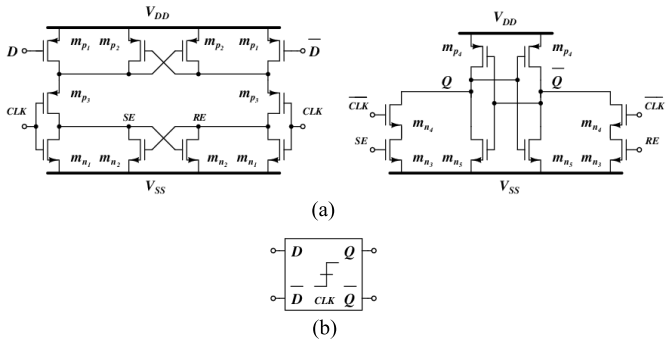


Fig. 14. Schematic circuit of the latched comparator. (a) Latched comparator circuit. (b) Symbol.

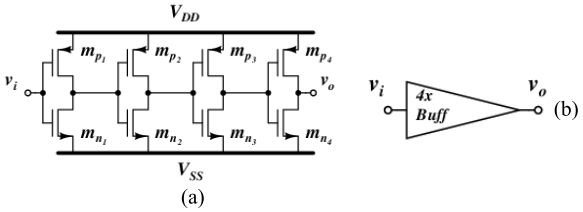


Fig. 15. Schematic circuit of the four-stage buffer. (a) Four-stage buffer circuit. (b) Symbol.

by (21) and (22), respectively. The OTAs used in the single-to-differential buffer are shown in Fig. 13. The open-loop ac response of the OTA_1 shows a dc gain of 25.89 dB, a GBW of 2.5 GHz, and a phase margin of 85°

$$\frac{v_{i_{SD}}^{+}}{2} - \frac{v_{i_{SD}}^{-}}{2} = 0.5\frac{R_{G_2}}{R_{G_1}}\epsilon_1 \cdot \frac{R_{G_3}}{R_{G_1}}\epsilon_2 \cdot v_{i_{SD}} \approx v_{i_{SD}} \tag{20}$$

$$\epsilon_1 = \frac{1}{1 + \frac{1}{g_{m_1}(r_{o_1} \| R_{G_2} \| R_{G_1})}\left(1 + \frac{R_{G_2}}{R_{G_1}}\right)} \tag{21}$$

$$\epsilon_2 = \frac{1}{1 + \frac{1}{g_{m_1}(r_{o_1} \| R_{G_3} \| R_1)}\left(1 + \frac{R_{G_3}}{R_{G_1}}\right)}. \tag{22}$$

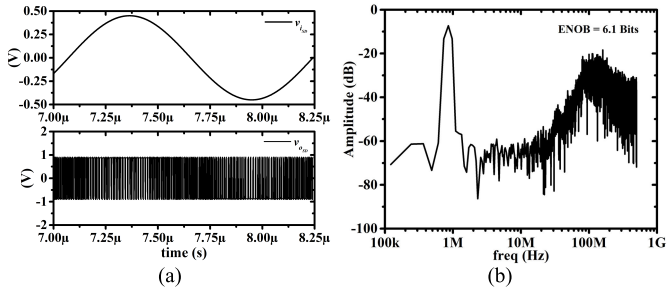


Fig. 16. Overall $\Sigma\Delta - M$ response. (a) Transient input and output signal. (b) Spectrum of the output signal.

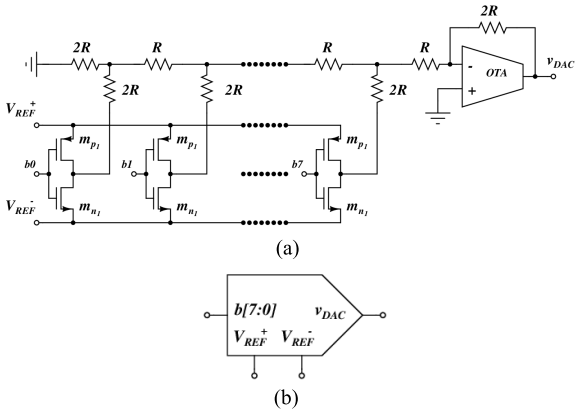


Fig. 17. Schematic circuit of the DAC. (a) DAC circuit. (b) Symbol.

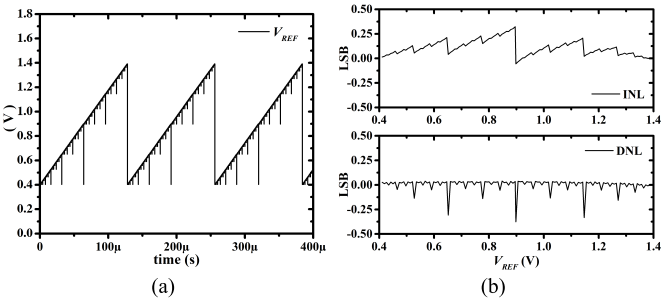


Fig. 18. DAC's nonlinearity. (a) DNL. (b) INL.

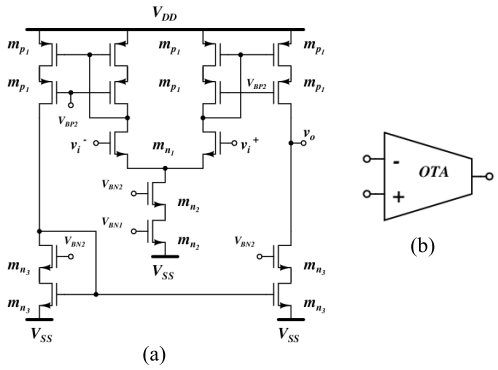


Fig. 19. Schematic circuit of the OTA used in the DAC. (a) OTA circuit. (b) Symbol.

Fig. 16 presents the transient and frequency response of the whole $\Sigma\Delta - M$, as depicted in Fig. 11(a), where an 854-kHz sine wave with a peak-to-peak amplitude of 0.9 V, −6 dB regarding the power supply, was applied. Such 854-kHz frequency was selected to observe how any spectral growth of at least ten spurious tones increases the noise level inside the 10-MHz $\Sigma\Delta - M$'s working BW. Fig. 16(a) shows how the $v_{i_{\mathrm{SD}}}$ sine wave increases and decreases the density of ones and zeros at the $v_{o_{\mathrm{SD}}}$ output of the modulator. From Fig. 16(b), it can be noted a −65-dB average noise floor from low frequencies until 10 MHz, while a 40-dB/decade noise shaping between 10 and 100 MHz can be observed. After the signal-to-noise calculation inside a 10-MHz BW, a 6.1-bit ENOB was obtained. The ENOB was computed using the methodology described in [35], [36], and [37].

4) Trigger Unit: The TU, shown in the pink box in Fig. 3, is composed of an 8-bit DAC and a comparator. The DAC generates a V_{REF} voltage that is used as a threshold level in the comparator. When $v_{o_{\mathrm{TIA}}}$ exceeds the V_{REF} level, the comparator sends a digital one to a buffer that delivers a $v_{o_{\mathrm{TU}}}$ voltage signal to the FPGA.

The schematic circuit and symbol of the implemented 8-bit DAC are illustrated in Fig. 17. It is comprised of an 8-bit 2-kΩ R2R network, a three cascode current-mirror OTA, and simple m_{p_1} and m_{n_1} transistors with an $r_{\mathrm{ON}} \leq 200\ \Omega$, which replace the typically used transmission gates to connect $V_{\mathrm{REF}}^+ = 1.4$ V and $V_{\mathrm{REF}}^- = 0.4$ V to the R2R network. The DAC's differential nonlinearity (DNL) and integral nonlinearity (INL) responses were tested for a 1-bit increasing code from b'00000000' to b'11111111' every 128 μs, leading to an LSB change every 500 ns. Fig. 18 presents the INL and DNL characterization.

The schematic circuit and symbol of the OTA used in the 8-bit DAC are presented in Fig. 19. The open-loop ac response of the OTA shows a dc gain of 48 dB, a GBW of 350 MHz, and a phase margin of 78.75°.

The schematic circuit and symbol of the high-speed comparator implemented in the TU are shown in Fig. 20. A full rail-to-rail input, m_{n_1} and m_{p_3}, was selected to improve the comparator's input range, while the strong arm latch, m_{n_4}, increases the comparison precision on which its decision making is based. Likewise, the self-biased amplifier, $m_{n_{5,6}}$ and $m_{p_{5,6}}$, and the output buffer, were used to boost the comparator's speed, $m_{n_{7,9}}$ and $m_{p_{7,9}}$, and capacitive driving capability.

Fig. 21(a) shows the transient response of the TU's comparator when a 1.5-mV square signal with a rising/falling time of 50 ps crosses the $V_{\mathrm{REF}} = 0.9$ V threshold, leading to a $t_{d_{\mathrm{HH}}}$ high-to-high delay time of 1.449 ns and a $t_{d_{\mathrm{LL}}}$ low-to-low delay time of 0.751 ns. These two delay times, $t_{d_{\mathrm{HH}}}$ and $t_{d_{\mathrm{LL}}}$, were minimized as much as possible while maintaining a decision capacity of 3 mV. Also, Fig. 21(b) presents a parametric analysis over different V_{REF} values from 0.2 to 1.6 V. This analysis confirms the comparator's ability to discern 1.5-mV square signals with rising/falling edges of 50, 66.6, 100, and 200 ps over its rail-to-rail input. Such rising/falling times are proportional/comparable to the rise time of the pulses delivered by the SiPM.

5) Phase-Locked Loop: The architecture of the PLL used by the MexSIC is depicted in Fig. 22. It is composed of a phase–frequency detector (PFD) [38], a charge pump

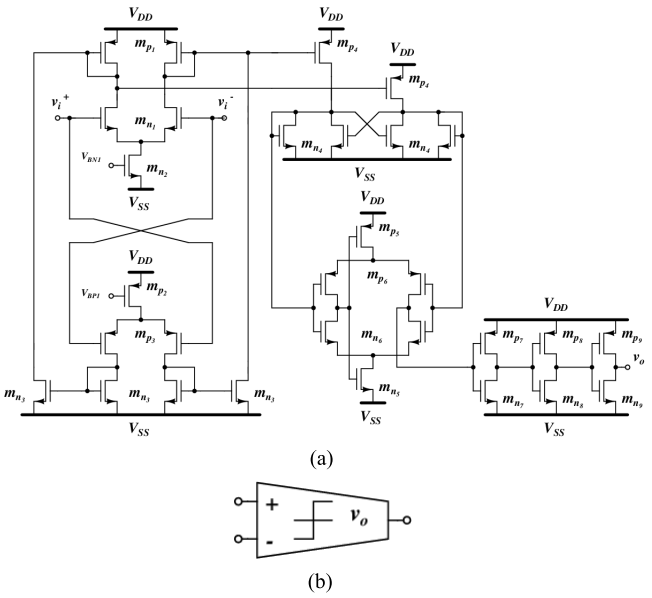


Fig. 20. Schematic circuit of the comparator used in the TU. (a) Comparator circuit. (b) Symbol.

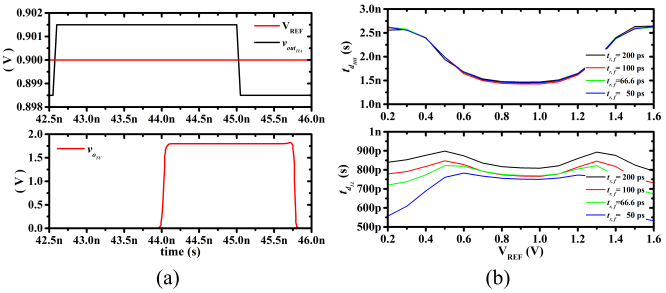


Fig. 21. Comparator's transient response. (a) Time response. (b) Parametric transient response.

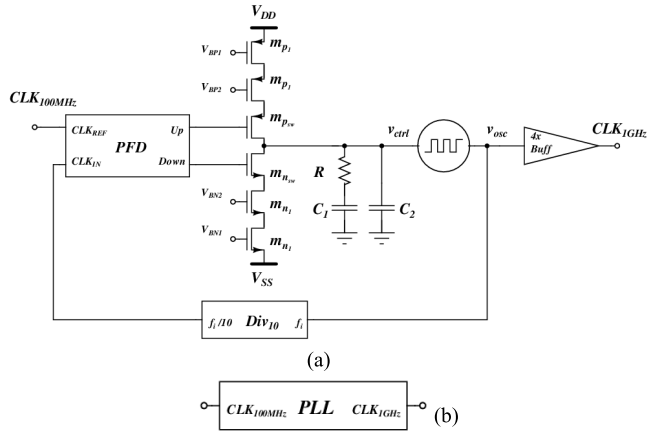


Fig. 22. Schematic circuit of the PLL. (a) PLL circuit. (b) Symbol.

(m_{p_1,n_1} and $m_{p_{sw},n_{sw}}$), a second-order filter ($C_{1,2}$ and R), a 1-GHz LC-tank voltage-controlled oscillator (VCO), a 10× frequency divider, and an output buffer. The behavior, circuits, and design equations of this well-known PLL can be found in [39]. The implemented PLL showed a phase noise of −96.4 dBc/Hz.

B. Digital Filtering (FPGA Architecture)

The $v_{o_{SD}}$ bitstream given by $\Sigma\Delta - M$ needs to be downsampled and filtered at very high rates to recover the SiPM signal in digital format. According to [40], the cascade integrator comb (CIC) filter presents the best response at high frequencies or high data rate decimation process. Equation (23) describes the CIC transfer function in the Z domain, where S is the number of cascaded integrators and Comb filters, D is the delay required by the Comb filter, and R is the downsampling factor

$$H(z) = \left(\frac{1 - Z^{-R\cdot D}}{1 - Z^{-1}}\right)^{S}. \tag{23}$$

Based on the design specs of $\Sigma\Delta - M$, the frequency response of the CIC filter [see (23)] was evaluated in MATLAB to achieve the maximum attenuation level at 10 MHz for a 1-GHz sampling frequency. To this end, the D parameter must be 2; otherwise, the filter cannot perform the average correctly. Also, because of the input integrators, the number of output bits N_b will increase as stated by the following equation, where b_{input} is the number of input bits, 1 bit for the implemented $\Sigma\Delta - M$:

$$N_b = b_{\text{input}} + \log_2(R \cdot D^S). \tag{24}$$

Fig. 23 presents how the S, D, and R parameters modify the CIC filter frequency response. Fig. 23(a), where $S = 3$ and $D = 2$, while R is swept from 4 to 10, shows the worst frequency response due to the −3-dB attenuation of the main lobe ranging between 13.18 and 33.2 MHz. Also, the peak of the second attenuation lobes is located at −40 dB. To make the attenuation band of the main lobe narrower, the R and D parameters were set to 8 and 2, respectively, and S was varied from 4 to 10 in two steps [see Fig. 23(b)]. This modification allows a −3-dB attenuation from 9.17 to 14.16 MHz, while the second attenuation lobes were located below −52 dB. Also, with the same goal of decreasing the cutoff frequency of the main lobe and decreasing the attenuation level of the second lobe, the R parameter was swept from 8 to 12, while $S = 6$ and $D = 2$ were set. This final evaluation over (23) led to a −3-dB attenuation from 15.62 to 9.27 MHz, but the attenuation level of the second lobe was drastically decreased until −80 dB [see Fig. 23(b)]. Therefore, and based on the mentioned considerations, the CIC filter was implemented using $R = 10$, $S = 6$, and $D = 2$ despite that the output had to compute 27 bits.

IV. Testbench and Measurements

To validate the proposed MexSIC system, a functional prototype was assembled using the MexSIC ASIC fabricated in a TSMC 180-nm CMOS standard technology, a Kintex-7 FPGA, and a laptop with an i7-Intel processor with 64 GB of RAM. The ASIC was fabricated in a 2.5 × 2 mm die [see Fig. 24(a)], and it was encapsulated in a QFN-100 package. Likewise, Fig. 24(b) presents the printed circuit board (PCB) used for bias, power supply, and connectivity purposes of the ASIC.

The ASIC shown in Fig. 24 includes a full channel and some building blocks added to test their functionality separately. The full channel has a silicon area of 0.478 mm^2, where the TIA, TU, $\Sigma\Delta - M$, and output buffers occupy areas of 0.134 (28.169%), 0.104 (21.84%), 0.237 (49.57%),

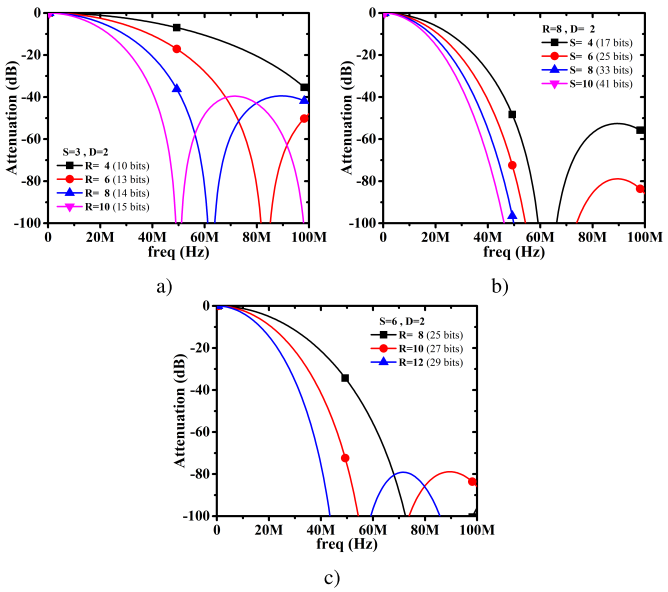
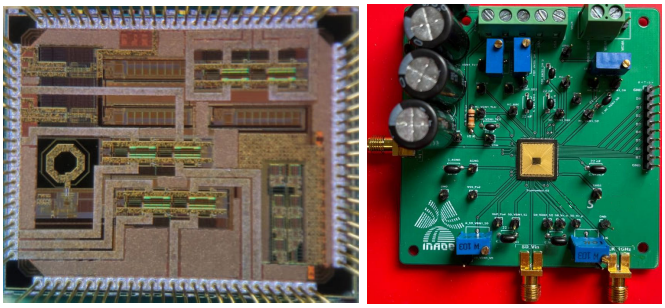


Fig. 23. CIC filter frequency response. (a) Parametric sweep for R. (b) Parametric sweep for S. (c) Final refinement and parametric sweep for R.



(a) (b)

Fig. 24. MexSiC prototype. (a) Microphotography of the MexSIC die. (b) MexSIC's PCB.

and 0.001 mm^2 (0.4%), respectively. The PLL's area, 0.4 mm^2, was not considered as part of the full channel's area due to the PLL will be shared by the 2^n number of full channels that will be included in the next MexSIC ASIC version. Also, one full channel of the proposed ASIC presented a 376-mW power consumption under a 1.8-V power supply, where the TIA, TU, $\Sigma\Delta-M$, and output buffers spend 97.7 (25.9%), 10.8 (2.86%), 252 (66.88%), and 16.2 mW (4.3%), respectively.

Fig. 25(a) draws the interconnection diagram of the whole equipment (testbench) used to characterize the MexSIC prototype, while Fig. 25(b) shows the physical accommodation of the equipment in the laboratory. The testbench was planned in three major units: power management, input signal excitation, and output signal measurements.

The power management unit is confirmed by three power supplies and three multimeters. Two Keithley 2231A power supplies were utilized to power the ASIC (V_{DD}, AGND, and GND) and to bias the DAC voltage references ($V_{\mathrm{REF}}^{\pm}$), while the third powers the J-Series 30035 SiPM. The three Agilent 34401A digital multimeters are employed to monitor a 400-μA dc current that properly biases $\Sigma\Delta - M$, PLL, and TU.

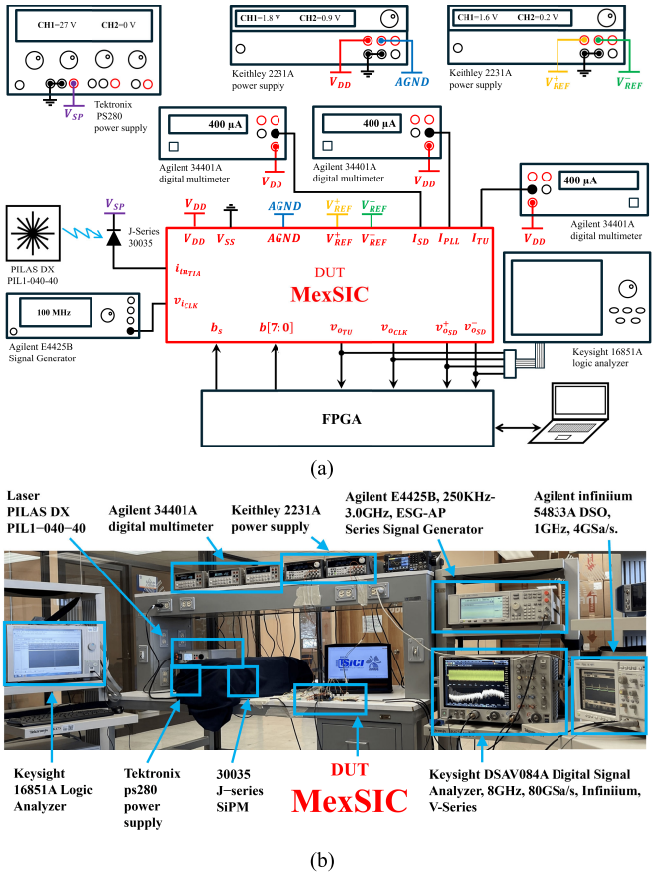


Fig. 25. Testbench used to characterize the MexSiC prototype. (a) Interconnection diagram. (b) Physical implementation.

On the other hand, the input signal excitation unit is composed of a PILAS DX PIL1-040-40 laser that sends 405-nm wavelength pulses to excite the SiPM and the Agilent E4425B signal generator, which provides a very clean 100-MHz signal to the ASIC to synthesize its 1-GHz clock reference. Finally, the Keysight 16851A logic analyzer is used as a signal measurement unit to compare the data processed by the FPGA/laptop.

A. Measurements and Discussion

The measurements for the proposed MexSIC were conducted by setting the TIA's gain in the ASIC under the low-gain mode (see Fig. 26) and the high-gain mode (see Fig. 27), respectively. In each gain mode, the laser emitted 10 000 pulses at a periodic 500-kHz event rate. In addition, the laser intensity was attenuated by 70%, 80%, and 90% to observe how the digitized pulse reduced its amplitude. Table I summarizes the configuration of the six measurement groups (G1–G6) used to characterize the MexSIC, as well as the corresponding figures showing the measurement results of each group.

Fig. 26 presents the MexSIC measurements when the ASIC's TIA is configured for a 21-dB low gain ($b_s = 0$), and Fig. 27 shows the results for a 48-dB high gain ($b_s = 1$) TIA configuration. All the graphs in Figs. 26 and 27 were experimentally obtained and displayed by the MATLAB GUI, meaning that the SiPM current was collected and sigma–delta modulated by the ASIC, then decimated by the FPGA,

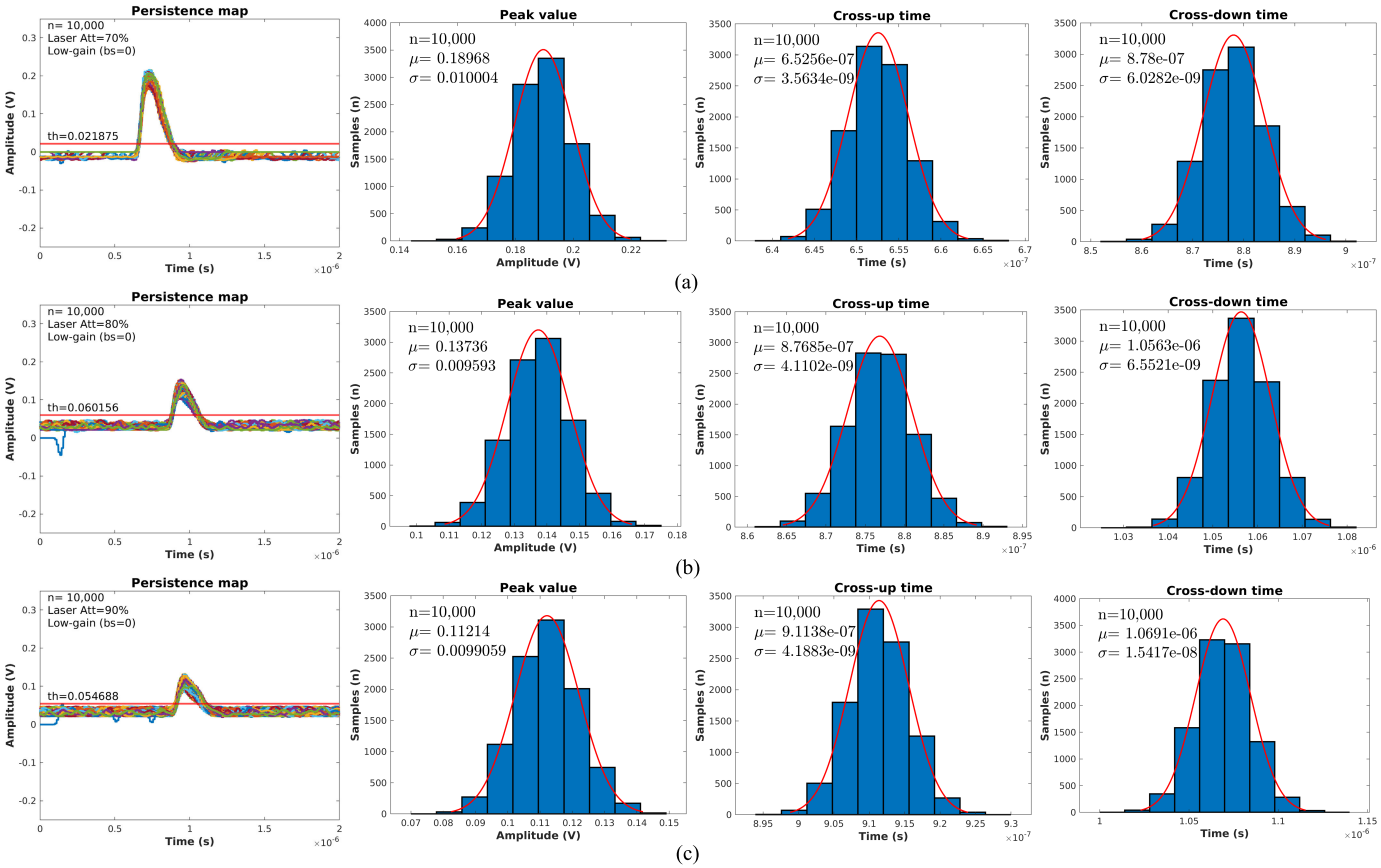


Fig. 26. Measurements performed using a TIA with a low-gain setting (21 dB, $b_s = 0$) and 500-kHz pulsed laser. (a) Laser attenuated at 70% and a threshold of 21.875 mV. (b) Laser attenuated at 80% and a threshold of 60.156 mV. (c) Laser attenuated at 90% and a threshold of 54.688 mV.

TABLE I
MEASUREMENT TEST PLAN

TIA's gain	Laser attenuation	Number of pulses	Group name	Figure
Low-gain (21 dB, $b_s = 0$)	70%	10,000	G1	Fig. 26a
	80%	10,000	G2	Fig. 26b
	90%	10,000	G3	Fig. 26c
High-gain (48 dB, $b_s = 1$)	70%	10,000	G4	Fig. 27a
	80%	10,000	G5	Fig. 27b
	90%	10,000	G6	Fig. 27c

and finally processed by the MATLAB GUI. Figs. 26 and 27 are organized as follows. Each column draws the persistence maps for 10 000 pulses grouped in 2-μs time slices, peak value histograms, cross-up time histograms, and cross-down time histograms for different thresholds, while each row groups the mentioned measurements based on the laser intensity attenuation of 70%, 80%, and 90%, respectively. It is important to note that in all persistence maps, the first column to the left-hand side in Figs. 26 and 27, the ASIC's analog ground (AGND = 0.9 V) was shifted to 0 V by the algorithm executed in the FPGA.

Fig. 26 allocates the characterization results when the TIA is configured in the low-gain mode, and the threshold level (horizontal red line) is used to compute the cross-up/cross-down times. Fig. 26(a) shows the results of the G1 group for a laser intensity attenuation of 70% and a threshold level of 21.875 mV. From Fig. 26(a), a mean peak value (μ_p) of 189.68 mV and a standard deviation (σ_p) of 10 mV, a mean cross-up time (μ_{cu}) of 652 ns with σ_{cu} of 3.56 ns, and a mean cross-down time (μ_{cd}) of 878 ns and σ_{cd} of 6.028 ns can be noted. These values lead to a TU pulse of 225.44-ns width. Likewise, Fig. 26(b) put in place the results of the G2 group using a laser attenuated to 80% and a threshold voltage of 60.156 mV, revealing $\mu_p = 137$ mV with a $\sigma_p = 9.59$ mV, $\mu_{\text{cu}} = 876.86$ ns with a $\sigma_{\text{cu}} = 4.11$ ns, $\mu_{\text{cd}} = 1.056$ μs, and $\sigma_{\text{cd}} = 6.55$ ns, leading to a TU pulse whose width is 179.5 ns. Also, Fig. 26(c) exhibits the results of the G3 group for a laser attenuation of 90% and a threshold voltage of 54.68 mV, obtaining $\mu_p = 112$ mV with $\sigma_p = 9.9$ mV, $\mu_{\text{cu}} = 911.38$ ns with $\sigma_{\text{cu}} = 4.18$ ns, $\mu_{\text{cd}} = 1.069$ μs, and $\sigma_{\text{cd}} = 15.41$ ns, leading to a TU pulse whose width is 157.72 ns.

Based on the results reported in Fig. 26, the standard deviations σ_p, σ_{cu}, and σ_{cd} increase with higher laser attenuation. This is because a lower laser intensity generates a current pulse with a smaller amplitude, resulting in longer rise and fall times. On the other hand, the baseline shift, from -10 to 25 mV in the persistence plots in Fig. 26(a)–(c), is because the offset-cancellation circuit in Fig. 5 subtracts the rms component from the current signal delivered by the SiPM within a BW governed by the RC network composed of m_r and m_c. In fact, this baseline shift is more noticeable in the persistence maps in Fig. 27(a)–(c), where the baseline shifts from -160 to -30 mV. The ASIC's ability to shift the baseline is a desirable mechanism because it enables the use of most of the ADC's input range. In addition, and for visualization purposes only, the baseline shift can be eliminated

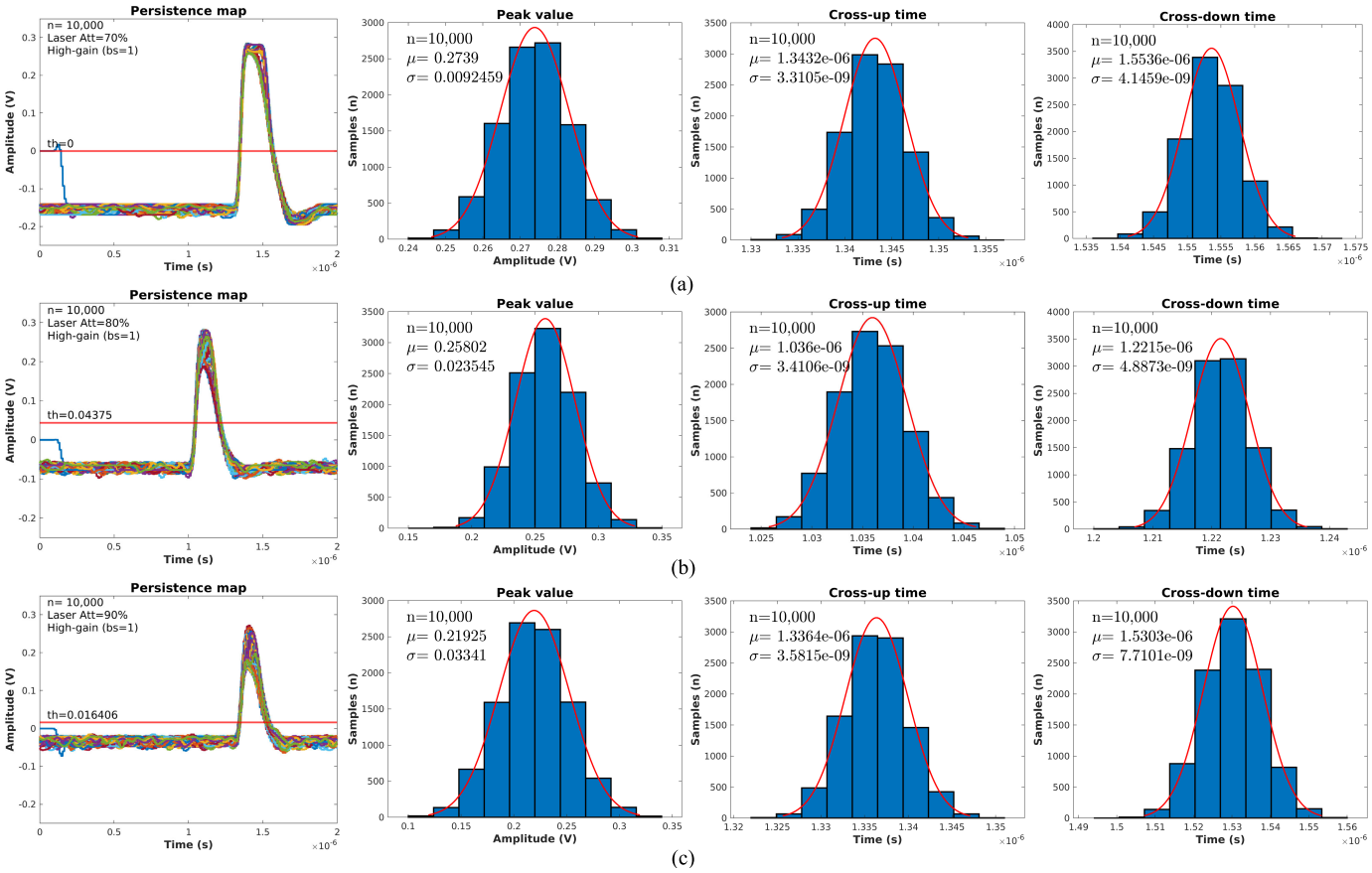


Fig. 27. Measurements performed using a TIA with a high-gain setting (48 dB, $b_s = 1$) and 500-kHz pulsed laser. (a) Laser attenuated at 70% and a threshold of 0 V. (b) Laser attenuated at 80% and a threshold of 43.750 mV. (c) Laser attenuated at 90% and a threshold of 16.406 mV.

and centered on a zero level using a peak-preserving baseline correction algorithm. However, it is important to note that all measurements presented in this work are in raw form.

Fig. 27 allocates the characterization results when the TIA is configured in high-gain mode and the threshold level (horizontal red line) is used to compute the cross-up/cross-down times. Fig. 27(a) shows the results of the G4 group for a laser intensity attenuation of 70% and a threshold level of 0 V. From Fig. 27(a), a mean peak value (μ_p) of 273.9 mV and a standard deviation (σ_p) of 9.24 mV, a mean cross-up time (μ_{cu}) of 1.343 μs with σ_{cu} of 3.31 ns, and a mean cross-down time (μ_{cd}) of 1.553 μs and σ_{cd} of 4.145 ns can be noted. These values lead to a TU pulse of 210-ns width. Likewise, Fig. 27(b) puts in place the results of the G5 group using a laser attenuated to 80% and a threshold voltage of 43.72 mV, revealing $\mu_p = 258$ mV with $\sigma_p = 23.54$ mV, $\mu_{\text{cu}} = 1.036$ μs with $\sigma_{\text{cu}} = 3.41$ ns, $\mu_{\text{cd}} = 1.221$ μs, and $\sigma_{\text{cd}} = 4.887$ ns, leading to a TU pulse whose width is 185 ns. Also, Fig. 27(c) exhibits the results of the G6 group for a laser attenuation of 90% and a threshold voltage of 16.4 mV, obtaining $\mu_p = 219$ mV with $\sigma_p = 33.41$ mV, $\mu_{\text{cu}} = 1.336$ μs with $\sigma_{\text{cu}} = 3.581$ ns, $\mu_{\text{cd}} = 1.53$ μs, and $\sigma_{\text{cd}} = 7.71$ ns, leading to a TU pulse whose width is 193.9 ns.

Based on the measurements shown in Fig. 27, the standard deviations ($\sigma_{p,\text{cu,cd}}$) increase as the laser attenuation increases. This leads to smaller amplitudes, causing longer rise and fall times. Analysis of the persistence maps reveals that the baselines are shifted from -160 to -30 mV in Fig. 27(a)–(c), indicating proper operation of the offset-cancellation circuit within the TIA. In addition, the persistence map in Fig. 27(a) shows a saturated signal near the peak, which occurs when the signal delivered by the TIA exceeds the input signal range of the sigma–delta modulator. This means that the SiPM current and the TIA's gain are big enough to deliver an output signal that exceeds $0.45v_{\text{peak}}$ (measured from the baseline to the maximum peak), while the sigma–delta modulator has a maximum peak input range of -6 dB over VDD/2, leading to 0.501*(1.8/2). This peak value corresponds to the maximum theoretical peak value allowed by all 1-bit quantizer sigma–delta modulators [36]. Despite being configured in high-gain mode, the persistence maps in Fig. 27(b) and (c) do not show any saturation because laser attenuation is greater than 80%.

B. Comparison With Other Reported Results

Table II compares the proposed MexSIC with the state of the art. As noted, all acquisition channels are intended for QDC, as their main function while offering TDC, ToT, or self-triggering as a second function. However, the number of elements used to assemble the full channel architecture makes a big difference, which, in turn, is fully related to the ASIC architecture. The MexSIC and the works in [22], [24], and [25] offer the easiest architecture to implement because they only require three elements: an ASIC, an FPGA, and a PC. This advantage is due to their ASIC-embedded ADCs, either Nyquist or oversampling type.

TABLE II
COMPARISON WITH OTHER WORKS

Feature	[22]	[21]	[23]	[24]	[41]	[25]	This work
Charge measurement	QDC plus TDC	QDC plus TOT	QDC	QDC plus TDC	QDC plus self-trigger	QDC plus TOT	QDC plus TOT
ASIC channel architecture	TIA + ADC + TU	TIA + TU + peak strecher	◁	TIA + ADC + TU	TIA + Integrator + TU	TIA + ADC + TU	TIA + ADC + TU
Full channel architecture	ASIC + FGA + PC	ASIC + ADC + FGA + PC	RC + OpAmp + FPGA + PC	ASIC + FGA + PC	ASIC + ADC + FGA + PC	ASIC + FGA + PC	ASIC + FGA + PC
Technology	350 nm SiGe BiCMOS	350 nm CMOS	COTS	180 nm CMOS	350 nm CMOS	180 nm CMOS	180 nm CMOS
Input range	1 p.e - 2000 p.e.$^{\odot}$	–	1 pC - 550 pC 5 μA - 2.75 mA$^{\ominus}$	20 pC - 800 pC 100 μA - 4 mA$^{\ominus}$	10 pC - 3 nC 71 μA - 21.42 mA$^{\otimes}$	20 pC - 800 pC 100 μA - 4 mA$^{\ominus}$	4 pC - 4 nC 20 μA - 20 mA$^{\ominus}$
Input-stage impedance	–	50-100 Ω	–	–	20 Ω	23 Ω	50 Ω
Input-stage bandwidth	–	100 MHz	–	–	65 MHz	7.6 MHz	1.57 GHz
ADC type	Wilkinson	– ◁	Sigma-Delta	SAR	– ◁	SAR	Sigma-Delta
ADC's ENOB	10 bit$^{\diamond}$	– ◁	–	8.24 bits	– ◁	8.52 bits	6.1 bits
ADC's sampling rate	–	– ◁	200 MHz	16 MS/s	– ◁	1 MS/s	100 MS/s
Silicon area per channel	2.25 mm^2 $\triangle$	0.833 mm^2 $\triangle$	–	0.214 mm^2 $\triangle$	0.600 mm^2 $\triangle$	0.293 mm^2 $\triangle$	0.478 mm^2
Power per channel	–	10.55 mW $\triangledown$	50 mW$^{\oplus}$	3.89 mW	17.5 mW $\triangledown$	4.1 mW	376 mW 124 mW $\bowtie$

– Not specified. $\diamond$ Not reported as ENOB. ◁ Not embedded in the ASIC. $\triangle$ Calculated from the total chip area over number of channels.
$\triangledown$ Calculated from the total chip power consumption over number of channels. $\oplus$ Only the analog front-end power consumption is reported.
$\ominus$ Calculated over a 200 ns pulse duration. $\otimes$ Calculated over a 140 ns pulse duration. The lower limit was estimated from plots.
$\odot$ Only photo-electron values are given. $\bowtie$ Removing the ADC power consumption.

Many SiPM ASIC readouts utilize Nyquist ADCs. In fact, Nyquist ADCs were implemented in [22], [24], and [25]. In [22], a 10-bit Wilkinson ADC was used, but it is unclear whether these 10 bits are ENOB. However, in [24] and [25], their SAR ADCs were designed for 10-bit resolution yet reported ENOBs of 8.24 and 8.52 bits, respectively. In recent years, oversampling ADCs have been successfully explored, as seen in the MexSIC and [23], where sigma–delta ADCs were employed. Despite MexSIC's sigma–delta ADC only achieving 6.1 ENOB, its 100-MS/s sampling rate allows for 20 samples of a pulse with a duration of 200 ns. In contrast, the SAR ADCs in [24] and [25] can only take one sample each microsecond, necessitating a shaper.

On the other hand, the proposed ASIC includes an input TIA that offers the largest charge (current) input range, which is only comparable to [41], and a wider BW that is ten times greater than [21]. However, these wide input ranges and BW come with a power penalty. As shown in Table II, the larger the input range and BW, the greater the power consumption. For example, the power consumption of MexSIC's ASIC is 11.75 times more than [21] and seven times more than [41]. It is important to note that the ASICs [21], [41], which reported comparable input ranges and BWs with MexSIC, do not include ADCs.

Even though the proposed ASIC has a higher power consumption compared to most reported SiPM front ends, this can be optimized based on IC design methodology, technological limitations, and functionality. From the IC design methodology point of view, two statements are valid. First, the TIA's input uses a 40-mA bias current to manage SiPM currents as large as 20 mA. Thus, the TIA's power consumption can be reduced by decreasing the TIA's input range, i.e., a TIA's input range of 200 μA can be implemented with a 400-μA bias current, leading the TIA's power consumption up to 8.46 mW. Second, the power consumption of $\Sigma\Delta-M$ can be dropped by dividing the CLK sampling frequency by two. This strategy allows to set the OTA_1 GBW to lower frequencies, diminishing its tail current almost by half, reducing the $\Sigma\Delta - M$ power consumption by 50%. Another advantage of reducing the CLK sampling frequency is that the output buffers will consume less dynamic power.

On the other hand, the proposed ASIC can be implemented in more advanced technologies such as 0.35-μm SiGe or 110-/90-/65-nm CMOS standard. For instance, SiGe technologies offer larger g_m/I_d ratios and larger cutoff frequencies using lower bias currents compared with CMOS, plus the advantage of using bipolar transistors. Similarly, using 110-/90-/65-nm technologies will decrease the power consumption due to nominal supply voltages being as low as 1 V and the transistor threshold voltages and the parasitics being reduced, leading to larger cutoff frequencies.

Finally, most ASICs intended for SiPM signal processing aim to deliver QDC using pulse shapers and low-frequency ADCs, as well as ToF/ToT measurements based on TDC. In contrast, the MexSIC uses the first ASIC that fully digitizes the SiPM signal using a high-speed sigma–delta ADC and delivers a pulse for ToT calculations.

V. CONCLUSION

The MexSIC DAQ channel for SiPMs is presented, composed of a mixed-mode MexSIC ASIC front end and an FPGA-based processing stage. The proposed ASIC is capable

of modulating, in the sigma–delta domain, SiPM output currents ranging between 0.02 and 20 mA with a resolution of 6.1 bits and a BW of 10 MHz. This BW offers an information loss of only 1% in QDC and TDC measurements for signals typically generated by SiPMs. To complete the digitization of the SiPM signal, the FPGA performs a decimation process by means of a cascaded integrator filter. The ASIC was designed in a 180-nm CMOS standard process using Cadence software, and the processing stage was implemented in a Kintex-7 FPGA.

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