Nanosheet Transistors Produced in 300 mm Fabrication Platform for Quantum Computing

Claude Rohrbacher, Dominic Leclerc, Joffrey Rivard, Romain Ritzenthaler, Christian Lupien, Hans Mertens, Naoto Horiguchi, *Member, IEEE*, and Eva Dupont-Ferrier, *Member, IEEE*

***Abstract*— We report on the first cryogenic characterization of a nMOS nanosheet transistor down to 1.2 K. We demonstrate that the device operates at low temperatures both in the transistor regime with improved DC characteristics (subthreshold swing) and in the quantum regime with adjustable charge occupation of the quantum dot down to a single electron. We further perform extensive low-frequency charge noise measurements in the quantum dot regime over a broad range of charge occupation numbers and observe low average charge noise of $\langle S_0 \rangle = 28 \pm 10\ \mu eV/\sqrt{Hz}$ at 1 Hz. These results demonstrate that nanosheet transistors are promising for large scale quantum/classical co-integration of CMOS devices for quantum information processing applications.**

***Index Terms*— 300 mm fabrication, charge noise, cryogenic, nanosheet transistor, quantum dot.**

I. Introduction

SPIN qubit devices in CMOS are promising candidates to achieve scalable quantum computers as they have demonstrated several significant milestones including long coherence time [1], single and two-qubit gates beyond the error correction threshold [2], [3] and high-temperature operation [4], [5]. The use of silicon allows to leverage the skill of the CMOS industry for very large-scale integration (VLSI) to scale up quantum processors and to co-integrate control electronics with quantum systems at cryogenic temperatures [6]. If most silicon spin qubit devices have been so far fabricated within academic labs, more recently there have been various demonstrations of qubits in standard FDSOI [7] and FinFET devices [4], [8]. In those devices, charge noise reduction has become a main focus [8], [9] as its effect is detrimental to coherence and gate fidelity [10], [11].

In the meantime, the cryogenic performance of a wide variety of CMOS technologies has been studied for cryo-electronic applications including bulk MOSFET [12], FD-SOI [13], [14], FinFET [15], [16], Gate-All-Around nanowires [17], [18]. But the semiconductor industry is still evolving with the next generation of nanosheet transistors aimed to go beyond the current FinFET technology [19]. A transition from FinFETs to nanosheets allows to overcome the issues with the so-called fin depopulation (variability increase, and impossibility to reduce the number of fins beyond one fin) used to maintain node-to-node area targets. By vertically stacking nanosheets, a better trade-off between area footprint and performance can be obtained [20]. Additionally, nanosheets leverage the excellent control of the gate over the silicon body and allow for a variable device width in design. As such, nanosheets are obvious candidate for quantum information processing (QIP) applications, both for cryogenic control electronics and as quantum devices. However, the investigation of their performances at cryogenic temperature has only been done in a pMOS SOI nanosheet [21] at 6K so far.

In this letter, we investigate state-of-the-art bulk nMOS nanosheet transistors for quantum computing applications. We perform standard output characteristic measurements for a transistor down to 4.2K and demonstrate improved performance at low temperature. We also demonstrate the first formation of a quantum dot and characterize the charge noise at 1.2K in a nanosheet device.

II. Device and Method

Starting from bulk silicon wafers, a Si/SiGe superlattice is grown by epitaxy and patterned. Subsequently, a dummy gate stack is deposited and patterned, followed by spacers deposition/etch. The Si/SiGe layers are then recessed in the source/drain cavities, and epitaxial Si:P Source/Drain are grown. After the formation of the interlayer dielectric the dummy gate is open and removed, revealing the Si/SiGe superlattice in the channel region. The SiGe sacrificial layers are subsequently selectively etched in order to form the Si nanosheets, and the RMG (Replacement Metal Gate) gate stack (SiO2 interfacial Layer, HfO2, and Work Function Metals) deposited. The rest of the flow consists of RMG W gate fill, and interconnect modules up to M1 level. A more comprehensive description of the device process flow can be found in [22] and [23]. The measured device consists of two vertically stacked nanosheet channels with layout gate length $L_G = 14$ nm. Standard DC output characteristics were performed in a Lake Shore Cryotronics probe station from room temperature down to 4.2 K. Coulomb diamonds and charge

Received 7 March 2025; accepted 26 March 2025. Date of publication 1 April 2025; date of current version 23 May 2025. This work was supported in part by the Canada First Research Excellence Fund, FRQNT établissement de la relève professorale under Grant 2020–NC–268397, and in part by the NSERC under Grant RGPIN–2020–0573. The review of this letter was arranged by Editor A. I. Khan. *(Claude Rohrbacher and Dominic Leclerc contributed equally to this work.) (Corresponding author: Dominic Leclerc.)*

Claude Rohrbacher, Dominic Leclerc, Joffrey Rivard, Christian Lupien, and Eva Dupont-Ferrier are with the Institut quantique and the Département de Physique, Université de Sherbrooke, Sherbrooke, QC J1K 2R1, Canada (e-mail: dominic.leclerc2@usherbrooke.ca).

Romain Ritzenthaler, Hans Mertens, and Naoto Horiguchi are with IMEC, 3001 Leuven, Belgium.

Digital Object Identifier 10.1109/LED.2025.3556348

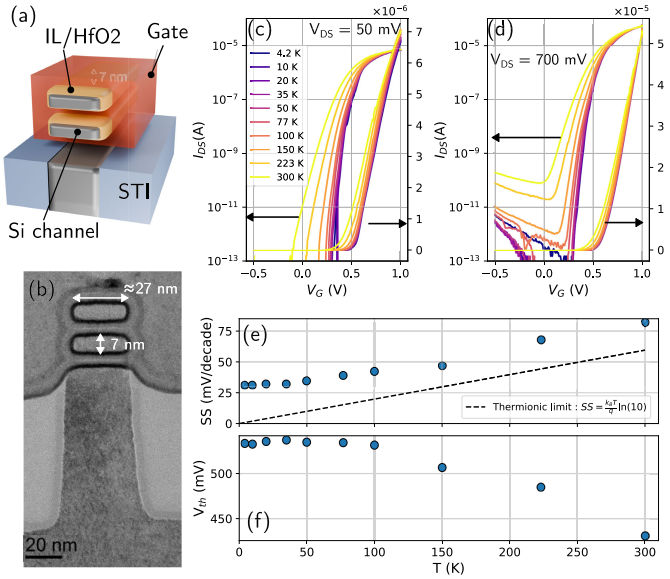

Fig. 1. (a) 3D Schematic of a 2-stack nanosheet transistor outlining the gate-all-around, oxide layer and silicon channel. (b) TEM cut along the gate of a nominally equivalent device with the main dimension indicated. (c-d) Transfer characteristics from 300 K to 4.2 K of the nanosheet transistor in linear (c) and saturation regime (d) in log scale (left axis) and linear scale (right axis). (e) Temperature dependence of the subthreshold swing in saturation regime with the theoretical thermionic limit outlined for reference. (f) Temperature dependence of the threshold voltage in the linear regime.

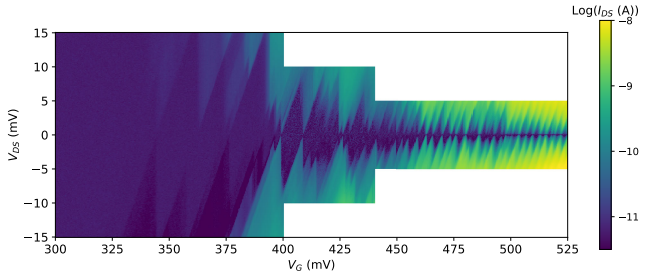

Fig. 2. (a) Stability diagram at 1.2 K showing Coulomb diamond down to the single electron regime.

noise measurements were performed in an ICE Oxford cryostat operating at a base temperature of 1.2 K. To demonstrate device functionality at cryogenic temperature, the output operation from room temperature to 4.2 K is shown in Fig. 1(c-d) both in linear and saturation regime. Threshold voltage and subthreshold swing are extracted with respect to temperature in Fig. 1(e-f). The evolution of the threshold voltage (V_{th}) with temperature is extracted using linear extrapolation method [24] and shown in Fig. 1(f). An increase in V_{th} from 430 mV at 300 K to 533 mV at 4.2 K is measured, mostly due to Fermi-Dirac scaling with temperature and bandgap widening [25]. This increase in V_{th} combined with the anticipated rise of mobility at cryogenic temperature [16] result in the current at $V_G = 1$ V remaining at ~ 53 μA in Fig. 1(d). Subthreshold swing (SS) in mV/decade in saturation regime is extracted at $I_{DS} = 1$ nA. Temperature dependence of SS in Fig. 1(e) shows an improvement from 81.8 $\pm$ 0.5 mV/decade at 300 K to 31.3 $\pm$ 1.1 mV/decade at 4.2 K. We notice that the SS linearly decreases with temperature until it saturates below 50 K. This degradation from thermionic behavior is

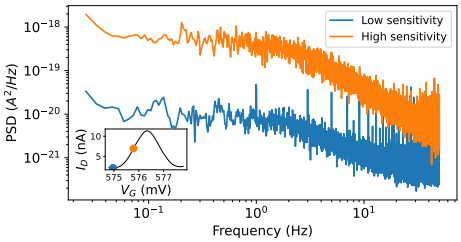

Fig. 3. Typical comparison of charge noise over a Coulomb peak ($V_{DS} = 1$ mV) at a low sensitivity point (blue) and a high sensitivity point (orange) demonstrating that we are measuring charge noise effect on the quantum dot current.

universally observed in a wide variety of CMOS technologies [16], [18], [26]. This can be attributed to a disorder-induced band tail at the conduction band-edge [27] and direct tunneling from source to drain in very short channel devices [16], which is most likely responsible for the observed behavior in our measurements.

III. Quantum Dot Operation and Charge Noise

At low temperatures, transfer characteristics at low V_{DS} exhibited Coulomb oscillations indicating the formation of quantum dots. Stability diagram measured at a base temperature of 1.2 K is displayed in Fig. 2 showing regular Coulomb diamonds confirming the formation of quantum dots in the nanosheet channels with a filling going from the single electron regime to about tens of electrons for higher gate voltages. Slightly irregular pattern is due to the superposition of Coulomb diamonds indicating that at least two quantum dots in parallel are measured [28], consistent with the two parallel nanosheet channels involved in the transport. From the Coulomb diamonds shape, we can extract key parameters: the charging energy $E_C = \frac{e^2}{C}$, the energy required to add an electron to the dot with C the total capacitance of the quantum dot. The lever arm $\alpha = \frac{E_C}{\Delta V_G}$ in eV/V^{-1} with ΔV_G the gate voltage required to add one electron. This parameter indicates the coupling strength between the gate and the dot and is highly relevant for fast measurement technique of the quantum dot such as reflectometry readout [29]. We extract those parameters over an average of seven diamonds in the range $V_G = [451; 477]$ mV (Fig. 2): $\alpha = 0.73 \pm 0.05$ eV/V, $E_c = 1.27 \pm 0.17$ meV. The high lever arm indicates strong coupling, consistent with the gate-all-around shape of the nanosheet.

We now characterize the low frequency charge noise in these quantum dots. Charge noise in quantum dots arises from Two-Level Fluctuator (TLFs) switching between two metastable states [30]. This topic has become a major focus in silicon spin qubit development, has it is detrimental to coherence and fidelity of qubits. The frequency response of a single TLF is Lorentzian, if TLFs are uniformly distributed in frequency the overall response becomes the well known $1/f^{\alpha}$ noise with α ranging from 0.5 to 2 [9], [11], [31]. In silicon-based devices, those TLFs are known to come primarily from defect at the interface between the gate oxide and the silicon channel [32]. In our case, we extract charge noise using the SET current spectroscopy method [11], [31].

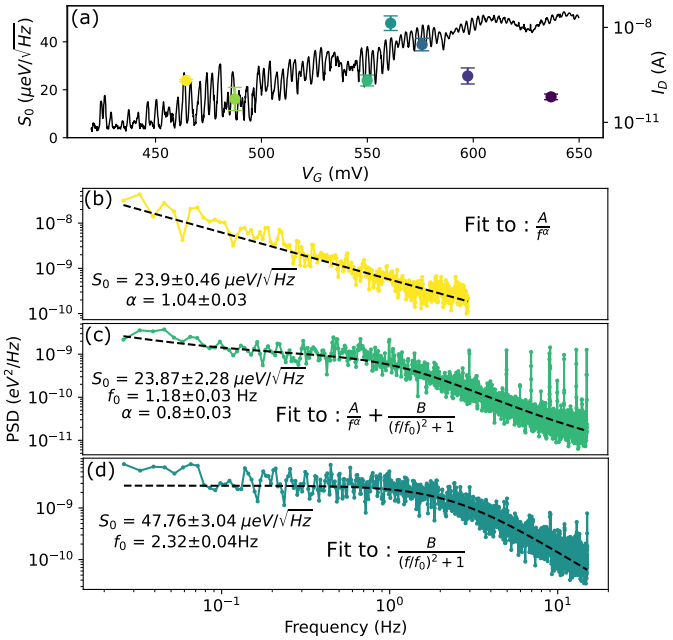

Fig. 4. (a) Coulomb oscillations at V_{DS} = 1 mV in log scale (black) with the extracted S_0 over different Coulomb peaks (dots). Examples of different types of spectrum of noise measured on the device with corresponding fit. (b) Typical 1/f spectrum, (c) a combination of 1/f and a Lorentzian spectrum and (d) a purely Lorentzian spectrum.

The current noise spectrum $S_I(f)$ is extracted at the maximum slope of a Coulomb peak, where the device is most sensitive to charge noise (Fig. 3). From this measurement charge noise is calculated in eV^2/Hz as

$$S(f) = \frac{\alpha^2 S_I(f)}{(\partial I/\partial V_G)^2}, \quad (1)$$

with α the lever arm and $\partial I/\partial V_G$ extracted at the maximum slope of the Coulomb peak. We measure the charge noise on several Coulomb peaks over a wide range of bias, corresponding to different electron filling. Fig. 4(b-d) show three typical evolution of the noise spectra as a function of frequency. We notice first a typical 1/f behaviour (Fig. 4(b)). However, some spectra deviates from 1/f behaviour, showing Lorentzian shape (Fig. 4(d)) or combination of 1/f and Lorentzian (Fig. 4(c)). This has been interpreted in the literature as the signature of a single or a few TLFs dominating the charge noise [9] which can be expected given the nanoscale devices usually considered. For comparison with noise studies performed on a variety of CMOS devices [8], [9], [11], [31] we extract the charge noise of the nanosheet transistors at 1 Hz S_0. The extracted value of S_0 for different Coulomb peaks are reported on Fig. 4(a). We report no clear dependence between the S_0 and the gate voltage V_G indicating that the value at 1 Hz seems uncorrelated of electron population as reported in other studies [9]. We report an average value $\langle S_0 \rangle = 28 \pm 10\ \mu eV/\sqrt{Hz}$, an order of magnitude higher than those reported in other standard CMOS silicon devices [8], [9] which can be explained by two factors. First, the use of high-k gate dielectrics which have higher interface defect density compared to the standard Si/SiO_2 interface used in silicon spin qubit devices [33]. Second, charge noise has a linear temperature dependence [34], as our measurement are performed at high temperature (1.2 K), we do expect higher noise than experiments performed at millikelvin temperatures with value of S_0 ranging between 0.5 and 10 $\mu eV/\sqrt{Hz}$ [8], [9], [31].

IV. Conclusion

We demonstrated improved DC performances of nMOS nanosheet transistors at cryogenic temperatures which could potentially be used for cryogenic control electronics. The nanosheet devices also shows the formation of a quantum dot in its channel that can be controlled over a wide range of gate voltages and down to the single electron regime. This demonstrates the potential of nanosheet transistors for co-integration of qubit and control electronics. Analysis of charge noise in the quantum dot shows slightly higher value at 1 Hz than other reported value in CMOS spin qubit device which can be explained by the presence of a high-k dielectric, the higher base temperature at which the measurements were performed and the gate-all-around architecture of the device. On the other hand, the high coupling to the gate makes it a strong candidate for advanced and compact readout technique such as gate-based reflectometry, a key requirement for scalable architectures.

References

[1] J. T. Muhonen, J. P. Dehollain, A. Laucht, F. E. Hudson, R. Kalra, T. Sekiguchi, K. M. Itoh, D. N. Jamieson, J. C. McCallum, A. S. Dzurak, and A. Morello, "Storing quantum information for 30 seconds in a nanoelectronic device," *Nature Nanotechnol.*, vol. 9, no. 12, pp. 986–991, Dec. 2014, doi: 10.1038/nnano.2014.211.

[2] X. Xue, M. Russ, N. Samkharadze, B. Undseth, A. Sammak, G. Scappucci, and L. M. K. Vandersypen, "Quantum logic with spin qubits crossing the surface code threshold," *Nature*, vol. 601, no. 7893, pp. 343–347, Jan. 2022, doi: 10.1038/s41586-021-04273-w.

[3] A. Noiri, K. Takeda, T. Nakajima, T. Kobayashi, A. Sammak, G. Scappucci, and S. Tarucha, "Fast universal quantum gate above the fault-tolerance threshold in silicon," *Nature*, vol. 601, no. 7893, pp. 338–342, Jan. 2022, doi: 10.1038/s41586-021-04182-y.

[4] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann, "A hole spin qubit in a fin field-effect transistor above 4 Kelvin," *Nature Electron.*, vol. 5, no. 3, pp. 178–183, Mar. 2022, doi: 10.1038/s41928-022-00722-0.

[5] J. Y. Huang, R. Y. Su, W. H. Lim, M. Feng, B. van Straaten, B. Severin, W. Gilbert, N. Dumoulin Stuyck, T. Tanttu, S. Serrano, J. D. Cifuentes, I. Hansen, A. E. Seedhouse, E. Vahapoglu, R. C. C. Leon, N. V. Abrosimov, H.-J. Pohl, M. L. W. Thewalt, F. E. Hudson, C. C. Escott, N. Ares, S. D. Bartlett, A. Morello, A. Saraiva, A. Laucht, A. S. Dzurak, and C. H. Yang, "High-fidelity spin qubit operation and algorithmic initialization above 1 k," *Nature*, vol. 627, no. 8005, pp. 772–777, Mar. 2024, doi: 10.1038/s41586-024-07160-2.

[6] M. F. Gonzalez-Zalba, S. de Franceschi, E. Charbon, T. Meunier, M. Vinet, and A. S. Dzurak, "Scaling silicon-based quantum computing using CMOS technology," *Nature Electron.*, vol. 4, no. 12, pp. 872–884, Dec. 2021, doi: 10.1038/s41928-021-00681-y.

[7] R. Maurand, X. Jehl, D. Kotekar-Patil, A. Corna, H. Bohuslavskyi, R. Laviéville, L. Hutin, S. Barraud, M. Vinet, M. Sanquer, and S. De Franceschi, "A CMOS silicon spin qubit," *Nature Commun.*, vol. 7, no. 1, p. 13575, Nov. 2016, doi: 10.1038/ncomms13575.

[8] A. M. J. Zwerver, T. Krähenmann, T. F. Watson, L. Lampert, H. C. George, R. Pillarisetty, S. A. Bojarski, P. Amin, S. V. Amitonov, J. M. Boter, R. Caudillo, D. Correas-Serrano, J. P. Dehollain, G. Droulers, E. M. Henry, R. Kotlyar, M. Lodari, F. Lüthi, D. J. Michalak, B. K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, O. K. Zietz, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen, and J. S. Clarke, "Qubits made by advanced semiconductor manufacturing," *Nature Electron.*, vol. 5, no. 3, pp. 184–190, Mar. 2022, doi: 10.1038/s41928-022-00727-9.

[9] A. Elsayed, M. M. K. Shehata, C. Godfrin, S. Kubicek, S. Massar, Y. Canvel, J. Jussot, G. Simion, M. Mongillo, D. Wan, B. Govoreanu, I. P. Radu, R. Li, P. Van Dorpe, and K. De Greve, "Low charge noise quantum dots with industrial CMOS manufacturing," *npj Quantum Inf.*, vol. 10, no. 1, p. 70, Jul. 2024, doi: 10.1038/s41534-024-00864-3.

[10] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, N. Usami, K. M. Itoh, and S. Tarucha, "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%," *Nature Nanotechnol.*, vol. 13, no. 2, pp. 102–106, Feb. 2018, doi: 10.1038/s41565-017-0014-x.

[11] L. Kranz, S. K. Gorman, B. Thorgrimsson, Y. He, D. Keith, J. G. Keizer, and M. Y. Simmons, "Exploiting a single-crystal environment to minimize the charge noise on qubits in silicon," *Adv. Mater.*, vol. 32, no. 40, Oct. 2020, Art. no. 2003361, doi: 10.1002/adma.202003361.

[12] C. Luo, Z. Li, T.-T. Lu, J. Xu, and G.-P. Guo, "MOSFET characterization and modeling at cryogenic temperatures," *Cryogenics*, vol. 98, pp. 12–17, Mar. 2019, doi: 10.1016/j.cryogenics.2018.12.009.

[13] H. Bohuslavskyi, S. Barraud, V. Barral, M. Cass, L. Le Guevel, L. Hutin, B. Bertrand, A. Crippa, X. Jehl, G. Pillonnet, A. G. M. Jansen, F. Arnaud, P. Galy, R. Maurand, S. De Franceschi, M. Sanquer, and M. Vinet, "Cryogenic characterization of 28-nm fd-soi ring oscillators with energy efficiency optimization," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3682–3688, Sep. 2018, doi: 10.1109/TED.2018.2859636.

[14] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electron.*, vol. 159, pp. 106–115, Sep. 2019, doi: 10.1016/j.sse.2019.03.033.

[15] A. Chabane, M. Prathapan, P. Mueller, E. Cha, P. A. Francese, M. Kossel, T. Morf, and C. Zota, "Cryogenic characterization and modeling of 14 nm bulk FinFET technology," in *Proc. IEEE 47th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2021, pp. 67–70, doi: 10.1109/ESSCIRC53450.2021.9567802.

[16] H.-C. Han, F. Jazaeri, A. D'Amico, A. Baschirotto, E. Charbon, and C. Enz, "Cryogenic characterization of 16 nm FinFET technology for quantum computing," in *Proc. IEEE 51st Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2021, pp. 71–74, doi: 10.1109/ESSDERC53440.2021.9631805.

[17] S. Sekiguchi, M.-J. Ahn, T. Mizutani, T. Saraya, M. Kobayashi, and T. Hiramoto, "Subthreshold swing in silicon gate-all-around nanowire and fully depleted SOI MOSFETs at cryogenic temperature," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 1151–1154, 2021, doi: 10.1109/JEDS.2021.3108854.

[18] C. Rohrbacher, J. Rivard, R. Ritzenthaler, B. Bureau, C. Lupien, H. Mertens, N. Horiguchi, and E. Dupont-Ferrier, "Dual operation of Gate-All-Around silicon nanowires at cryogenic temperatures: FET and quantum dot," 2023, *arXiv:2312.00903*.

[19] G.-J. Bae, D.-i. Bae, M. Kang, S. M. Hwang, S. S. Kim, B. I. Seo, T. Kwon, T. J. Lee, C. Moon, Y. M. Choi, K. Oikawa, S. Masuoka, K. Y. Chun, S. H. Park, H. Shin, J.-C. Kim, K. K. Bhuwalka, D. H. Kim, W. J. Kim, J. Yoo, H.-j. Jeon, M. Yang, S. J. Chung, D. Kim, B.-H. Ham, K. J. Park, W. D. Kim, S. H. Park, G. Song, Y. H. Kim, M. Kang, K. Hwang, J. Lee, D.-W. Kim, S.-M. Jung, and H. Kang, "3nm GAA technology featuring Multi-Bridge-Channel FET for low power and high performance applications," in *IEDM Tech. Dig.*, Dec. 2018, p. 28, doi: 10.1109/IEDM.2018.8614629.

[20] M. G. Bardon, Y. Sherazi, D. Jang, D. Yakimets, P. Schuddinck, R. Baert, H. Mertens, L. Mattii, B. Parvais, A. Mocuta, and D. Verkest, "Power-performance trade-offs for lateral NanoSheets on ultra-scaled standard cells," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 143–144, doi: 10.1109/VLSIT.2018.8510633.

[21] X. Zhu, L. Cao, G. Wang, and H. Yin, "Low temperature (down to 6 K) and quantum transport characteristics of stacked nanosheet transistors with a high-K/metal gate-last process," *Nanomaterials*, vol. 14, no. 11, p. 916, May 2024, doi: 10.3390/nano14110916.

[22] R. Ritzenthaler, H. Mertens, G. Eneman, E. Simoen, E. Bury, P. Eyben, F. M. Bufler, Y. Oniki, B. Briggs, B. T. Chan, A. Hikavyy, G. Mannaert, B. Parvais, A. Chasin, J. Mitard, E. D. Litta, S. Samavedam, and N. Horiguchi, "Comparison of electrical performance of co-integrated forksheets and nanosheets transistors for the 2nm technological node and beyond," in *IEDM Tech. Dig.*, Dec. 2021, pp. 26.2.1–26.2.4, doi: 10.1109/IEDM19574.2021.9720524.

[23] H. Mertens, R. Ritzenthaler, Y. Oniki, B. Briggs, B. T. Chan, A. Hikavyy, T. Hopf, G. Mannaert, Z. Tao, F. Sebaai, A. Peter, K. Vandersmissen, E. Dupuy, E. Rosseel, D. Batuk, J. Geypen, G. T. Martinez, D. Abigail, E. Grieten, K. Dehave, J. Mitard, S. Subramanian, L.-Å. Ragnarsson, P. Weckx, D. Jang, B. Chehab, G. Hellings, J. Ryckaert, E. D. Litta, and N. Horiguchi, "Forksheet FETs for advanced CMOS scaling: Forksheet-nanosheet co-integration and dual work function metal gates at 17nm N-P space," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.

[24] A. Ortiz-Conde, F. J. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 583–596, Apr. 2002, doi: 10.1016/s0026-2714(02)00027-6.

[25] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOSFET threshold voltage model," in *Proc. 49th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Poland, Sep. 2019, pp. 94–97, doi: 10.1109/ESSDERC.2019.8901806.

[26] R. M. Incandela, L. Song, H. A. R. Homulle, F. Sebastiano, E. Charbon, and A. Vladimirescu, "Nanometer CMOS characterization and compact modeling at deep-cryogenic temperatures," in *Proc. 47th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2017, pp. 58–61, doi: 10.1109/ESSDERC.2017.8066591.

[27] H. Bohuslavskyi, A. G. M. Jansen, S. Barraud, V. Barral, M. Cassé, L. Le Guevel, X. Jehl, L. Hutin, B. Bertrand, G. Billiot, G. Pillonnet, F. Arnaud, P. Galy, S. De Franceschi, M. Vinet, and M. Sanquer, "Cryogenic subthreshold swing saturation in FD-SOI MOSFETs described with band broadening," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 784–787, May 2019, doi: 10.1109/LED.2019.2903111.

[28] M. Nilsson, L. Namazi, S. Lehmann, M. Leijnse, K. A. Dick, and C. Thelander, "Electron-hole interactions in coupled InAs-GaSb quantum dots based on nanowire crystal phase templates," *Phys. Rev. B, Condens. Matter*, vol. 94, no. 11, Sep. 2016, Art. no. 115313, doi: 10.1103/physrevb.94.115313.

[29] J. C. Frake, S. Kano, C. Ciccarelli, J. Griffiths, M. Sakamoto, T. TeranishiY. Majima, C. G. Smith, and M. R. Buitelaar, "Radio-frequency capacitance spectroscopy of metallic nanoparticles," *Sci. Rep.*, vol. 5, no. 1, p. 10858, Jun. 2015, doi: 10.1038/srep10858.

[30] A. Bermeister, D. Keith, and D. Culcer, "Charge noise, spin-orbit coupling, and dephasing of single-spin qubits," *Appl. Phys. Lett.*, vol. 105, no. 19, Nov. 2014, Art. no. 192102, doi: 10.1063/1.4901162.

[31] E. J. Connors, J. Nelson, H. Qiao, L. F. Edge, and J. M. Nichol, "Low-frequency charge noise in Si/SiGe quantum dots," *Phys. Rev. B, Condens. Matter*, vol. 100, no. 16, Oct. 2019, Art. no. 165305, doi: 10.1103/physrevb.100.165305.

[32] S. Machlup, "Noise in semiconductors: Spectrum of a two-parameter random signal," *J. Appl. Phys.*, vol. 25, no. 3, pp. 341–343, Mar. 1954, doi: 10.1063/1.1721637.

[33] M. V. Haartman and M.stling, "1/f noise performance of advanced CMOS devices," in *Low-Frequency Noise in Advanced MOS Devices*. Dordrecht, The Netherlands: Springer, 2007, ch. 4, pp. 103–107, doi: 10.1007/978-1-4020-5910-0.

[34] L. Petit, J. M. Boter, H. G. J. Eenink, G. Droulers, M. L. V. Tagliaferri, R. Li, D. P. Franke, K. J. Singh, J. S. Clarke, R. N. Schouten, V. V. Dobrovitski, L. M. K. Vandersypen, and M. Veldhorst, "Spin lifetime and charge noise in hot silicon quantum dot qubits," *Phys. Rev. Lett.*, vol. 121, no. 7, Aug. 2018, Art. no. 076801, doi: 10.1103/physrevlett.121.076801.