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Cold electronics for “Giant” Liquid Argon Time Projection Chambers

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Abstract. The choice between cold and warm electronics (inside or outside the cryostat) in very large LAr TPCs (>5-10 ktons) is not an electronics issue, but it is rather a major cryostat design issue. This is because the location of the signal processing electronics has a direct and far reaching effect on the cryostat design, an indirect effect on the TPC electrode design (sense wire spacing, wire length and drift distance), and a significant effect on the TPC performance. All these factors weigh so overwhelmingly in favor of the cold electronics that it remains an optimal solution for very large TPCs. In this paper signal and noise considerations are summarized, the concept of the readout chain is described, and the guidelines for design of CMOS circuits for operation in liquid argon (at ~89 K) are discussed.

1. Introduction

The Liquid Argon Time Projection Chamber (LAr TPC) is a very promising detector technology for future beam-based neutrino research and nucleon decay research. This technology offers extraordinarily precise event reconstruction and particle identification, as well as scalability to very-large detectors. To go beyond the sensitivities of current experiments for neutrino physics and proton decay, the next generation of liquid argon TPCs are envisioned to be in the range of 20-100 kton, and must be placed deep underground. Detectors of this size pose many engineering challenges. In order of difficulty and cost these are: 1) mechanical and thermal design of the cryostat including the cryogenic system; 2) design, construction and installation of the signal and drift electrode system; 3) electronic readout system.

The number of sense wires, i.e., input signal channels is expected to be in the range of 5-7 hundred thousand for a 20 kton scale TPC (up to several million for 100 kton). To achieve a good signal to noise ratio, while scaling to the large sized detectors, we are developing CMOS ASICs with high degree of multiplexing (128 – 1024) operating inside the cryostat. These front end circuits will be placed close to the sense wires, eliminating the need for long cables which would present major contributors to electronics noise (due to their capacitance and resistance) and to contamination of the high purity liquid. The number of output signal links will be greatly reduced due to the multiplexing, greatly reducing the number of cryostat penetrations (feedthroughs) necessary to read out all the sense wires. The resulting small number of feedthroughs can be placed anywhere on the cryostat (near the end), as there is no need

to place them near the wire frames as would be the case with external (warm) electronics.

This gives the cryostat designers complete freedom to choose the optimum size, shape, configuration of the cryostat and the mechanical structure of the top of the cryostat. It also greatly reduces the risk of leaks in the feedthroughs.

It should be noted that an *a priori* assumption that warm electronics would be the only solution in almost all TPC concepts discussed so far at various workshops and conferences has compelled the designers toward detector concepts with **very long drift distances (up to 20 meters)** resulting in very high purity requirements, **very long sense wires or wires from several wire frame modules connected in series and long cables**, all in an effort to avoid large numbers of signal channels exiting the cryostat. The **signal-to-noise ratio** (i.e., the detector sensitivity) suffers twofold, from the **attenuation of the signal charge** during a long drift and from the **increased electronic noise** due to the capacitance of very long sense wires and long cables.

Cold electronics makes possible an optimum balance among various design and performance requirements.

Pioneering work on LAr TPCs has been done by the ICARUS collaboration [1]. The chamber sizes realized (<1kton of LAr) allowed the use of warm electronics. Truly “giant” detectors require a different approach to the readout, as well as to the overall detector design.

In this paper we summarize the basics of signal formation and electronic noise, present a functional outline of the readout chain and an outline of the front end CMOS ASIC design. We discuss briefly some principal design guidelines to ensure a long life of MOS transistors.

2. TPC electrodes and signal formation

One of the detector concepts under study for the LBNE experiment is based on two or more units, each consisting of a cryostat, with approximate dimensions of $70 \times 15 \times 15 \text{ m}^3$, containing $\sim 20,000$ tons of liquid argon (LAr) instrumented with time projection chamber (TPC) modules. In each TPC module, ionization electrons created by charged particles produced in neutrino or nucleon decay interactions are drifted up to 2.5 m in a uniform field of 500 V/cm to the readout electrodes.

The simplest electrode configuration which allows track reconstruction with dE/dx measurements consists of three planes of sense wires, arranged one in the vertical direction and two at angles of $\pm 45^\circ$ to the vertical, as illustrated in figure 1. These three planes of wires are biased such that electric field lines terminate only on the last plane in the drift direction, so that they collect electrons, while wires in the other two planes (at $\pm 45^\circ$) observe induction without collection, allowing two dimensional coordinate determinations in the plane of the wires. This configuration is based on a square cell, where the sense wire pitch is equal to the spacing between the wire planes, figure 2. Under a constraint that each wire is read out, variations in the ratio of these dimensions (i.e., departure from the square cell) offer no overall advantage. More ideal electrode configurations would all require either more wires (to form denser grids), or pad/pixel electrodes in great numbers, where the costs and mechanical construction requirements would become prohibitive.

The total number of wires in each cryostat unit would be on the order of 500,000 to 650,000, for 4 and 3 mm wire spacing respectively. Since each wire spans half the height of the cryostat, each wire approaches ~ 10 m in length, corresponding to a capacitance of about 200 pF. Each wire is connected directly to one channel of an electronic circuit located at the wire frame in the LAr (at ~ 89 K).

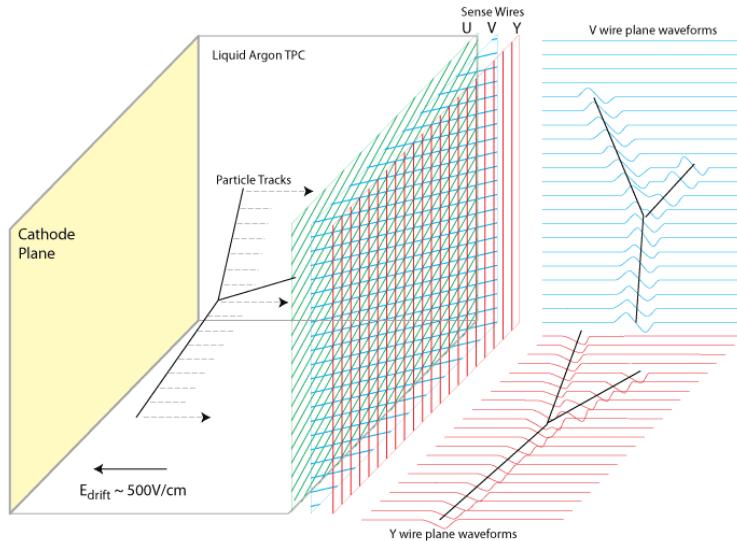


Figure 1. Schematic illustration of a liquid argon TPC: Ionization electrons produced by the passage of charged particles through the liquid argon are transported by a uniform electric field to three wire planes, where they induce electric signals on the sense wires. By recording and analyzing the waveform on each wire, the original track can be precisely reconstructed.

An estimate of the charge signal size on the collection wire plane for a track perpendicular to the sense wire and parallel to the wire plane is as follows:

- A 3 mm MIP track should create $210 \text{ keV/mm} \times 3 \text{ mm} / 23.6 \text{ eV/e} = 4.3 \text{ fC}$.
- After a 1/3 initial recombination loss (at 500 V/cm): $\sim 2.8 \text{ fC}$. This would be the maximum signal for tracks close to the wire planes.
- It is expected that the TPC design will maximize the drift path to equal or exceed the charge life time, thereby reducing the signal to $1/e \approx 0.368$.
- The expected signal for 3mm wire spacing is then $\approx 1 \text{ fC} = 6250 \text{ electrons}$.
- The expected signal for 5 mm wire spacing is $\approx 10^4 \text{ electrons}$.
- The induction signals on the first and second wire plane are smaller as shown in figures 2 and 3.

These signal sizes are for a track perpendicular to the sense wire and parallel to the wire plane. For track inclinations α and β with respect to this orientation, the signal has to be multiplied by $1/(\cos\alpha \cdot \cos\beta)$ and there is a change in the shape of the signals as shown in figure 3. The expected maximum induced charge on a single wire due to a shower would be $\sim 300 \text{ fC}$.

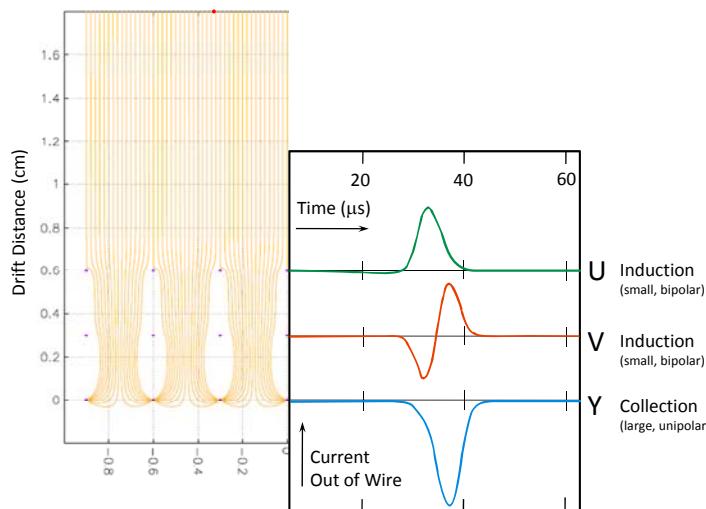
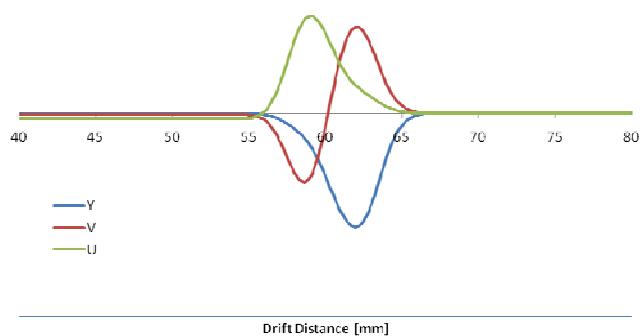


Figure 2. A planar illustration of electric field lines (i.e., electron trajectories) and the signals induced by an ionizing track at 90 degrees to the wire direction and at 0 degrees to the wire planes. The wires in the induction planes u and v are inclined at ± 45 degrees with respect to wires in the y plane (the wires in this figure are shown all in the same direction for simplicity).

0° track, 0.6 μ s rms "diffusion", 3x3 cell



30° track, 0.6 μ s rms "diffusion", 3x3 cell

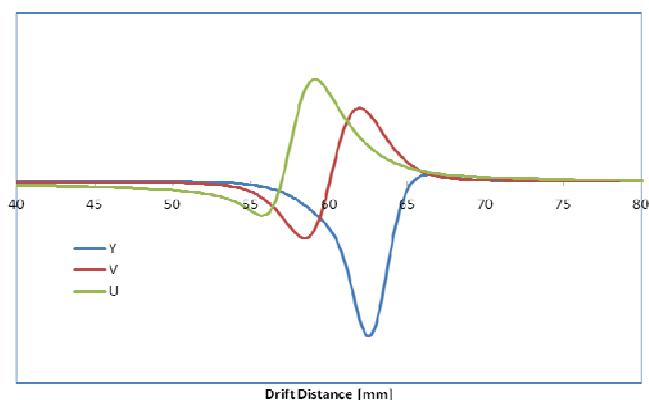


Figure 3. Induced current waveforms for an ionizing track at 0 and 30 degrees to the wire planes. **Wire plane spacing** and **electron drift velocity** determine the **time scale** of the signals and of all the subsequent signal processing. The transit time between the two planes is about 2 and 2.7 microseconds for the 3mm x 3mm and 4 mm x 4 mm cells respectively, for an assumed drift field of 500 V/cm. Both sets of signal waveforms have the same horizontal and vertical scale.

The waveforms in figures 2 and 3 were calculated using Ramo's theorem, as described in [2]. The results of the calculation were then convolved with a gaussian to simulate smoothing and broadening due to charge diffusion. Standard deviation of 0.6 μ s was assumed, corresponding to longitudinal diffusion over a drift distance of ~ 0.5 m.

3. Electronic Noise

We consider here only the unavoidable sources of noise: 3.1. The **first transistor noise** associated with the physics of amplification, and 3.2. The **thermal noise from the sense wire** and connection leads (signal cable). We assume that any resistors connected to the amplifier input, such as the feedback and sense wire bias resistors, are chosen so that their thermal noise is negligible.

3.1. The **first transistor noise** contribution to the measured signal charge is due to the total capacitance, comprised of the sense wire capacitance, cable capacitance and input transistor capacitance. **This total capacitance limits the signal-to-noise ratio and it is the one dominant factor on which the feasibility and scalability of a LAr TPC design critically depends.** This noise contribution is well understood, and the result has been well established analytically and experimentally. The equivalent noise charge (ENC_A) due to the first transistor noise (thermal noise in the case of field effect transistors) can be expressed as,

$$ENC_A^2 = e_n^2 C_{in}^2 / t_p$$

where: $e_n^2 = 4k_B T R_s$ = transistor series white noise spectral density in $[V/Hz^{1/2}]$

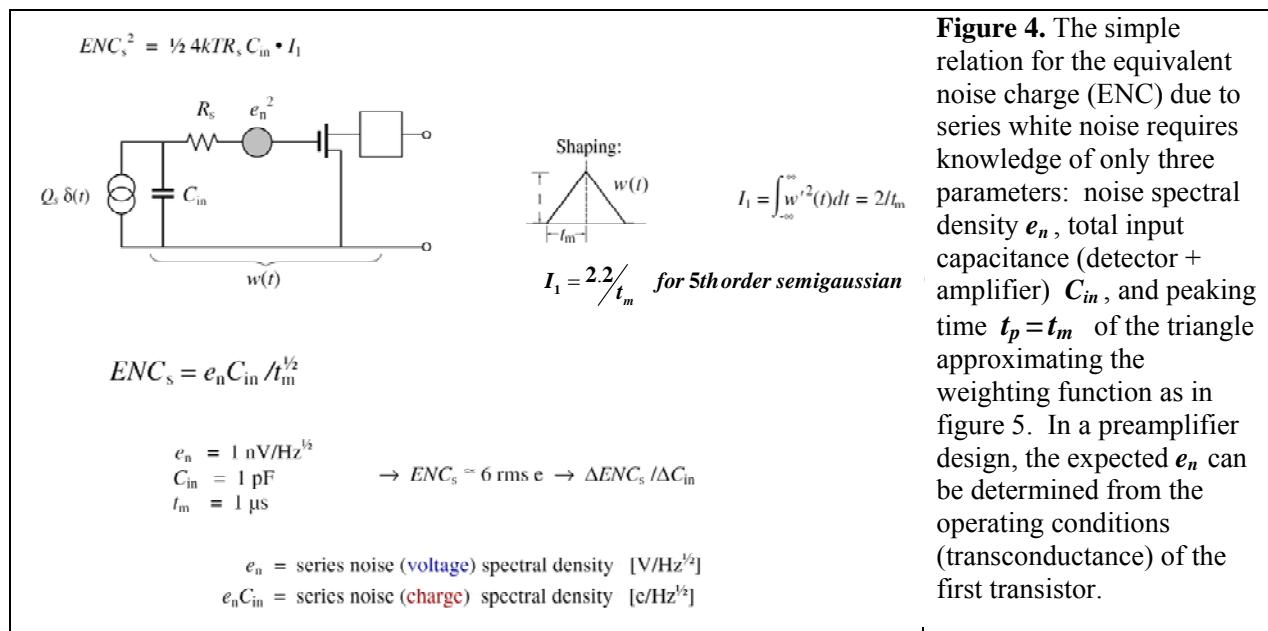
R_s = transistor equivalent series noise resistance

$C_{in} = C_{wire} + C_{Cable} + C_{ampl}$

t_p = weighting function peaking time $\square 1/\text{bandwidth}$

k_B = Boltzmann constant

Derivation of equation (1) is summarized in figure 4. See also reference [2].



3.2 **Thermal noise from the sense wire** is calculated based on the transmission line model of the sense wire. The equivalent noise charge can be expressed as,

$$ENC_w^2 \cong 4k_B T C_w^2 \left(\frac{R_w}{3} \right) \left(\frac{1}{t_p} \right) \quad (2)$$

where : C_w = sense wire capacitance
 R_w = sense wire resistance

The sense wire noise contribution is equivalent to that of a resistor equal to one third of the wire resistance inserted between the receiving end of the wire and the amplifier. This contribution becomes significant for long sense wires (10 to 20 meters) if stainless steel is used. It can be made negligible by using Cu+Au coated stainless steel, or Cu+Be [3].

Both expressions (1) and (2) for ENC contain a weighting function width parameter $t_p = \tau$ (the inverse bandwidth). We assume here the simplest weighting function, illustrated in Fig. 5. This function is optimal for transistor white noise and an impulse signal.

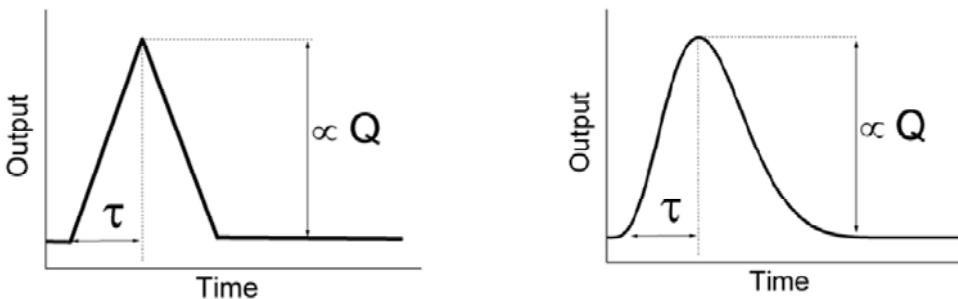


Figure 5. Signal processing weighting functions: **triangle** is the theoretical optimum for amplifier white series noise and impulse signal; **semigaussian** is easily realized in practical circuits. $t_p = \tau$ in equations (1) and (2), and it results in an ENC within few percent of the triangular one.

In a large TPC we will use different weighting functions to optimize separately the measurements of dE/dx , track segment position coordinates, timing and double track resolution. A function of the type in Fig. 5 will be used for “prefiltering” or “band limiting” prior to sampling. This function will be realized in the front end (preamplifier and pulse shaper) analog circuits. Desired weighting functions for the specific measurements listed above will be realized by weighting multiple samples in subsequent digital processing. For the electron transit times from one wire plane to another of 2-3 microseconds, we choose $t_p=1 \mu\text{s}$ to define prefiltering and the single-sample ENC , corresponding to a bandwidth of 1 MHz. This bandwidth requires a sampling frequency of 2 megasamples/second to avoid noise aliasing.

Input transistor: The best one can reasonably achieve with JFETs at 300K for external (warm) readout and with PMOS at 90 K for electronic readout in the cryostat is $e_n = 0.5 \text{ nV/Hz}^{1/2}$, which corresponds to a resistance $R_{sn} = 15 \text{ ohms}$. Trying to reduce these values further for warm electronics would bring a diminishing return as the resistance values of the signal cables are approached (~a few ohms). For cold electronics, power dissipation limits any further reduction in the noise.

With these assumptions, two plots of ENC vs sense wire length and signal cable length are given in figures 6 and 7, to cover the likely range of parameters to be encountered in a very large TPC, for either external (warm) or internal (cold) electronics.

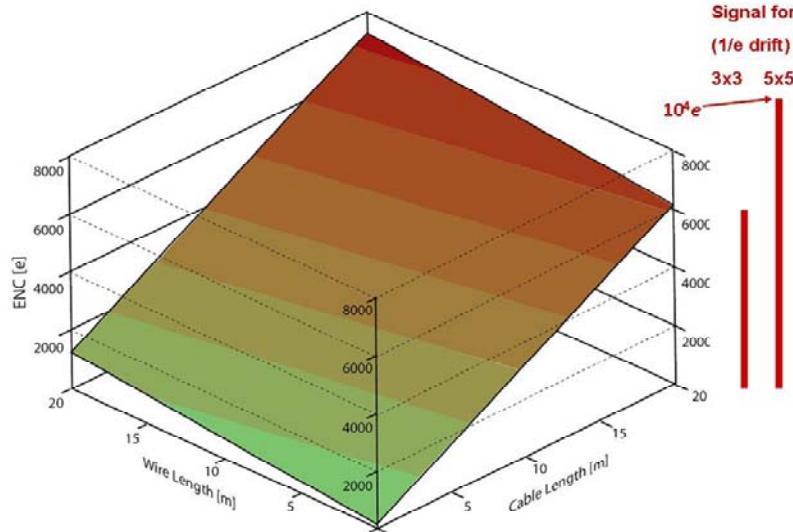


Figure 6. Contour plot of equivalent noise charge (ENC) vs sense wire length and signal cable length due to amplifier noise with a spectral density of $0.5 \text{ nV/Hz}^{1/2}$ and weighting function peaking time $t_p=1 \mu\text{s}$. Sense wire capacitance is $\sim 20 \text{ pF/m}$ and signal cable capacitance $\sim 100 \text{ pF/m}$ is assumed (for a different cable capacitance, the cable length scale should be changed). Note that for cold electronics, the cable length is zero. Low resistance sense wire is assumed, figure 7.

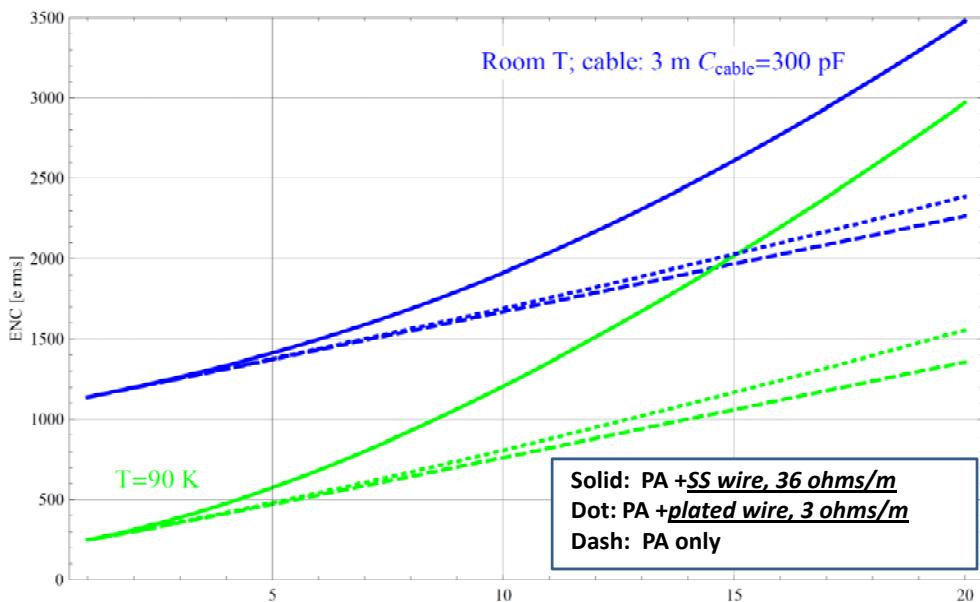


Figure 7. Noise vs sense wire length with internal (cold) CMOS electronics in comparison to external (warm) electronics. For calculation purposes, the warm electronics is assumed to have, in the best case, a 3 meter cable. The cold electronics has no cable (only a few cm long connections from the sense wires to the ASIC). Shown is ENC vs sense wire length due to amplifier noise with a spectral density of $0.5 \text{ nV/Hz}^{1/2}$ for two different sense wire materials, and for weighting function peaking time $t_p=1 \mu\text{s}$. Sense wire capacitance is $\sim 20 \text{ pF/m}$ and signal cable capacitance is assumed $\sim 100 \text{ pF/m}$. For longer wire lengths, low resistance sense wire (such as Cu+Au plated SS wire) offers a significantly lower noise. PA=preamplifier.

4. The readout chain

The readout electronics must digitize signals with 12-bit resolution at a rate of 2 mega-samples per second (MS/s), limited by the longitudinal diffusion of electrons, and compress, buffer and multiplex the data. The power dissipated by each channel must be limited to a few mW to minimize local boiling of the LAr. The expected dynamic range from the signal and noise estimates in sections 2 and 3 would be, $\sim 300 \text{ fC}/0.1 \text{ fC} = 3000$, i.e. ~ 12 bits. Essentially all the readout electronics should be placed on the sense wire-frame structure as illustrated in figure 12. This would place front-end ASICs next to the sense wire connections and minimize the cabling from the wire frames to the feedthroughs.

A challenging aspect is to bring the data out of the cryostat. For a ~ 20 kton LAr TPC with half a million sense wires (4 mm wire spacing) the raw data rate would be: $(500 \text{ k wires} \times 2 \text{ Ms/s} \times 12 \text{ bits}) \sim 10^{13} \text{ bps}$. Some data compression will be possible without loss of particle track information. The degree of compression and the compression schemes are being studied. Assuming a compression by $\sim 1/8$, the data rate would be $1.25 \times 10^{12} \text{ bps}$. Both copper links and fiber optic links are being investigated and both are indicated in the figure with their respective data rates.

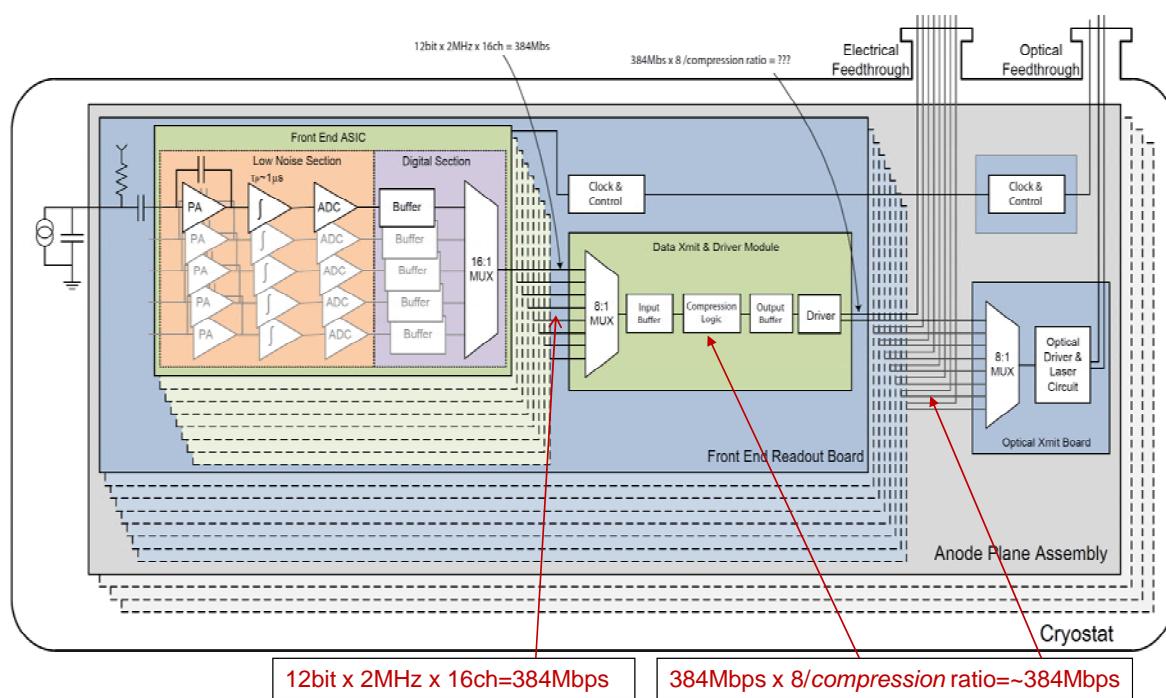


Figure 8. Functional Outline of a Multiplexed Readout Chain for Very Large LAr TPCs. Multiplexing will be performed in two to three steps by 1/128, or by 1/(512-1024). Two options are shown for digital links leading out of the cryostat: copper links at ~ 400 Mbps, and fiber optical links at 1.6-3.2 Gbps. For each data link (after multiplexing by 1/128, or more), a redundant link with auxiliary circuits (e.g. driver etc.) will be implemented.

5. MOS transistors at low temperature

For design and operation of CMOS circuits at liquid argon temperature (~ 89 K) two critical aspects must be considered. The first is accuracy of the device models used in the transistor and circuit design in terms of operating point, signal response (transconductance, output resistance and capacitance), noise, interconnects and passive components (resistors and capacitors). The second is the long-term lifetime, since the LAr TPC is required to operate for over 20 years without access to the electronics, short of a very major overhaul.

Concerning the device models, we have characterized a complete mixed-signal CMOS 0.25 μ m ASIC, originally developed for room temperature applications [4], at temperatures down to 40 K, observing encouraging results (see for example figure 9). A comparison of the signal response to the simulation suggests that the models are to a first order reliable, and that they may only need some minor adjustments. We are also in the process of fabricating in a CMOS 0.18 μ m technology a dedicated analog front-end ASIC (described in the next Section) and a number of test structures.

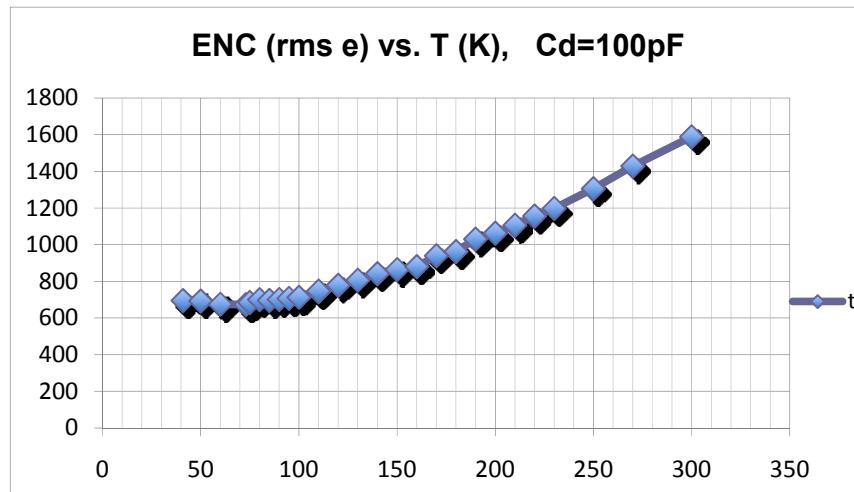


Figure 9. Noise (ENC) vs temperature measured on a mixed signal ASIC designed for room temperature operation. CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio. Peaking time = 0.5 μ s

With regard to the **long-term lifetime**, the major failure mechanisms such as, *electromigration (EM)*, *stress migration (SM)*, *time-dependent dielectric breakdown (TDDB)* and *thermal cycling (TC)* scale with temperature in favor of cryogenic operation [5]. The only mechanism that affects the lifetime adversely at cryogenic temperature is *degradation due to impact ionization*, which introduces trapped charge in the MOSFET gate oxide [6, 7]. Fortunately the *substrate current is a good quantitative monitor of impact ionization*, which makes possible *accelerated tests and lifetime extrapolation*.

This is illustrated in figure 10. Impact ionization depends on the electric field near the FET drain. Therefore the lifetime depends strongly on the drain-source voltage. Operation close to liquid nitrogen temperature requires about 10% lower drain-source voltage than at room temperature.

Conversely, the lifetime is decreased or increased by an order of magnitude if the voltage is changed by plus or minus $\sim 10\%$. This makes accelerated lifetime tests practical.

Some simplified design guidelines for long lifetime at low temperatures are: design both analog and

digital circuits with transistors operated at $V_{DS} \leq 2/3 V_{DD}$, at low current density and with non-minimum channel length L .

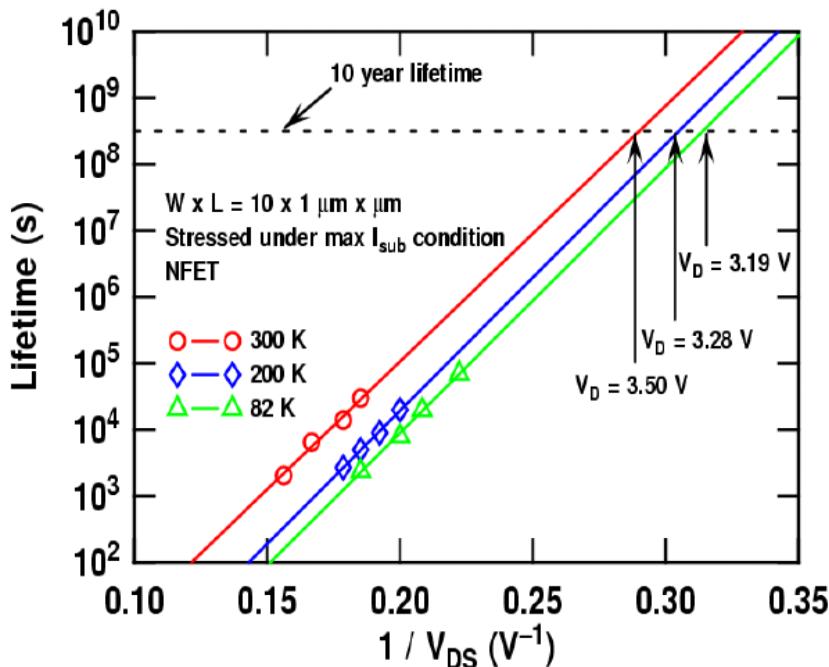


Figure 10. n-channel MOSFET lifetime due to impact ionization as a function of drain-source voltage and temperature.
From: J. Cressler

6. Front end ASIC design concept

In this section an outline is given of some of the circuits leading to the design of the front-end ASIC. In figure 8, a conceptual block diagram of a 16-channel front-end ASIC is shown. Each channel implements a charge amplifier with adjustable gain (4.7, 7.8, 14 and 25 mV/fC), a high-order shaper with adjustable peaking time (0.5, 1, 2, 3 μs), optional AC coupling, baseline adjustment for operation with either the collecting or the non-collecting wires (Y and U, V in figures 1 and 2), a 12-bit 2 MS/s ADC and a data compression stage. Shared among the 16 channels are the bias circuits, registers, a temperature monitor, the digital multiplexer (16:1), the FIFO and the digital interface. The ADC, currently being designed, aims at 12-bit resolution, converting in less than 500 ns, and dissipating about 2 mA (3.6 mW). The ADC design is based on the current mode concept described in [8]. The analog section of the channel (charge amplifier and shaper) has been fabricated and it is being tested and characterized at this writing.

This first prototype of the front-end ASIC is being developed in a commercial CMOS 0.18 μm platform (available through MOSIS). The final choice of the technology will be determined based on the results from the characterization of several test structures from different platforms and sources. For a project of this magnitude, an established technology will be chosen that must be available from more than one source.

A functional diagram of the charge amplifier is shown in figure 11. The input MOSFET is a p-channel biased at 2 mA with an L/W ratio of $0.27 \mu\text{m}/10 \text{ mm}$, followed by a dual cascode stage. The charge amplifier is composed of two stages and it provides a charge gain of up to 20×16 prior to the fifth order shaper. The overall weighting function will be semigaussian as shown in figure 5. The circuits used here are based on well proven concepts developed previously, [4], and [8].

Charge sensitivity calibration.

Charge calibration is accomplished by the charge injection method well established in nuclear and x-ray spectroscopy. A voltage step is generated in every ASIC from an accurately known dc voltage. A simple uniform calibration of numerous channels has been made possible by advances in CMOS technology: the spread in the values of capacitances on a single wafer used for charge injection is remarkably small, $\sigma < 0.25\%$, and the lot-to-lot spread is $< 0.5\%$. A check on the capacitance for a single chip could be included as a step in a standard automated test procedure. The capacitances in CMOS are very stable.

The whole TPC with hundreds of thousands wires would thus have well known ($\sim 1\%$) charge sensitivity, allowing accurate dE/dx measurements calibrated with cosmic muons and determination of the attenuation distance and lifetime.

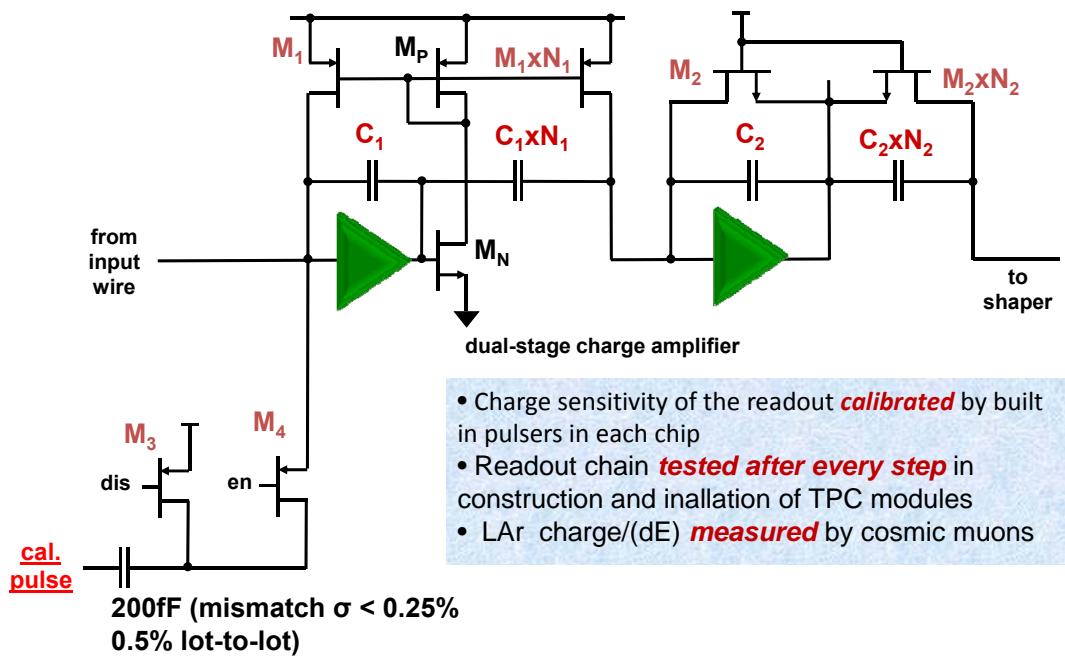


Figure 11. Two-stage charge amplifier with charge calibration. The design concept is described in reference [4]

7. Summary

Cold electronics in very large LAr TPCs allows almost unlimited freedom in the design of the cryostat and anode wire frames. This is an essential condition to enable economical solutions to the cryostat structural and thermal design, an interface between the cryostat walls and the cavern walls not hampered by numerous signal feedthroughs, as well as to make possible a design of anode wire frames which can be completely assembled with integral readout electronics off the detector site, transported and installed in the cryostat. The charge calibration scheme described in the previous section allows rapid testing at every step of this process. The main features of such a design are illustrated in figure 12.

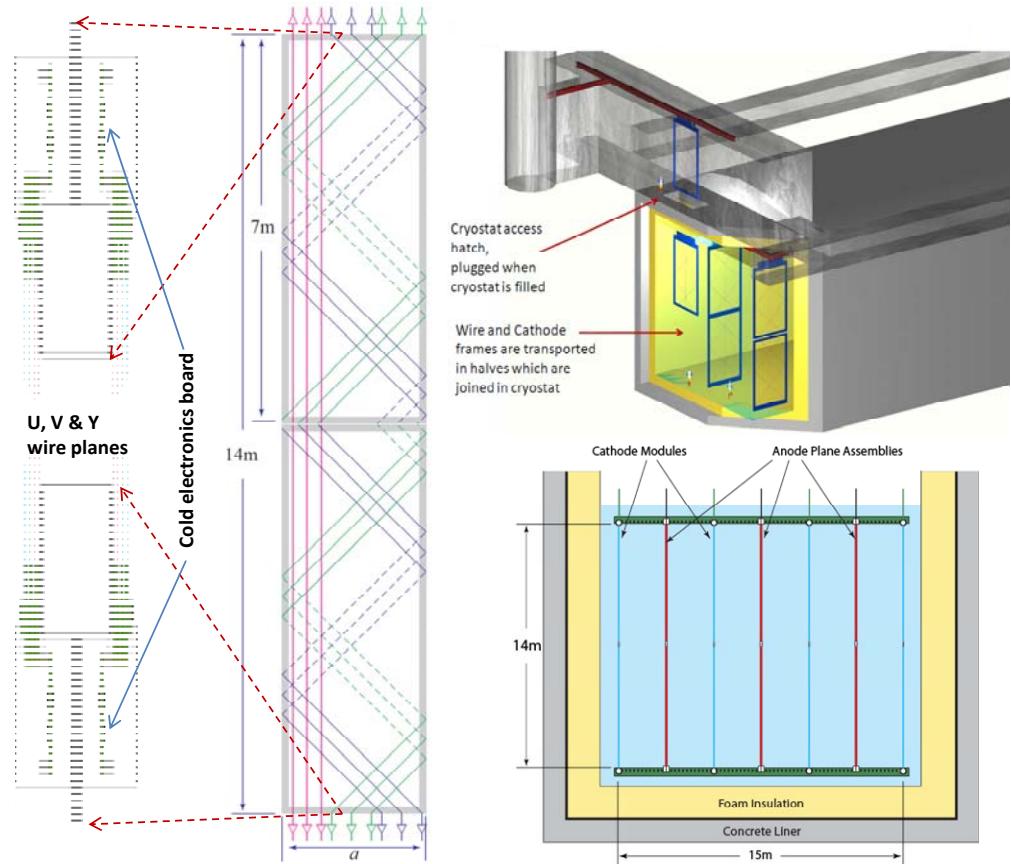


Figure 12. Key components of a possible ~20 kton LAr TPC: The cryostat (a cutout on upper right and a crosssection on lower right); a wire frame (middle of the figure: two 7 m long wire frames on top of each other, with readout electronics at the top and at the bottom); horizontal structural parts of the wire frames showing electronics boards and sense wire attachments, on the left of the figure. The very few feedthroughs needed are at the near end of the cryostat. A feedthrough design proven in LHC/ATLAS is described in reference [9]. The “folded u,v , wires” concept is due to Hans Jostlein (FNAL).

While the electronics in some large experiments (e.g., LHC) can hardly be considered accessible (an access usually requiring a long shutdown and disassembly of large equipment), the difficulties of access to a giant underground detector are much more apparent. While it is possible to conceive of a solution with a storage tank where the liquid argon could be transferred allowing access into the tank for a major overhaul, we concentrate in our development work to design a reliable detector system for long operation. In addition to understanding the dominant aging phenomenon, such as the one mentioned in section 5, as well as the design process to minimize it, a carefully designed testing procedure for all cold electronics components will be essential. Such a verification and testing procedure will have to include, at a minimum, the following steps:

- The CMOS devices will be designed and fully qualified in the Design and Development phase for operation at cryogenic temperatures. All circuit boards (fully assembled with ASICS) will be cycled several times between liquid nitrogen temperature (by immersion) and somewhat above room temperature (~ 50 C).
- At the TPC assembly stage, once each TPC module (wire frame with electronics) is installed in the cryostat, a calibration run of all electronics channels will be conducted ... and then again, after cooling with Ar gas, prior to filling with LAr.

With the charge calibration built into the ASICS such testing of all channels will be straightforward.

In addition to the noise and performance advantages of the cold electronics location at the sense wires, all the advantages for the cryostat and TPC design are entirely due to a high degree of multiplexing (1/128, 1/512, or 1/1024), and the resulting radical reduction in the number of signal feedthroughs and cables (with the attendant reduction in outgassing and probability of leaks). This raises the question of a single point failure in the output data links. *Redundant links and associated circuits will have to be used, with the redundancy increasing toward the top of the multiplexing pyramid.* Given the decreasing number of links with the degree of multiplexing, the cost of redundancy will be low.

{Discussion of costs is beyond the scope of this paper. Since this question comes up naturally, a glimpse will be given: Initial estimates indicate that the cost of the cold electronics readout expressed as a fraction of the cost of the detection medium (liquid argon) alone is less than one. Somewhat of a surprise to many would be that the cost of a warm electronics readout would come out higher (mainly due to the cost of feedthroughs and cables, the cost of the active electronics being nearly the same; the cost of added complexity in the cryostat design not taken into account).}

Note added in proof: The front-end ASIC containing preamplifier and shaper, outlined in figures 8. and 11, has been designed and successfully fabricated and tested. The results have been presented in Ref. [10].

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