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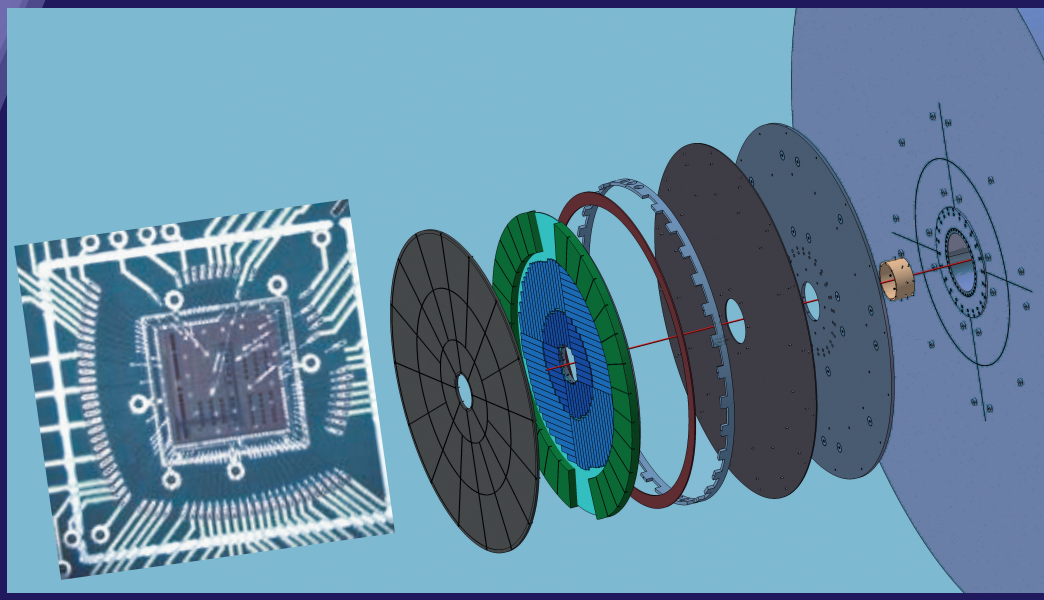
ATLAS

A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade



Technical Proposal

Technical Proposal: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade

The ATLAS Collaboration

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Abstract
The large increase of pileup interactions is one of the main experimental challenges for the HL-LHC physics program. A new powerful way to mitigate the effects of pileup is to use high-precision timing information to distinguish between collisions occurring very close in space but well-separated in time. A High-Granularity Timing Detector, based on low gain avalanche detector technology, is therefore proposed for the ATLAS Phase-II upgrade. Covering the pseudorapidity region between 2.4 and 4.0, with a timing resolution of 30 ps for minimum-ionising particles, this device will significantly improve the performance in the forward region. The high-precision timing information greatly improves the track-to-vertex association, leading to a performance similar to that in the central region for both jet and lepton reconstruction, as well as the tagging of heavy-flavour jets. These improvements in object reconstruction performance translate into important sensitivity gains and enhance the reach of the HL-LHC physics program. In addition, the HGTD offers unique capabilities for the online and offline luminosity determination.

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1 Introduction

The high-luminosity phase of the Large Hadron Collider (HL-LHC) at CERN is scheduled to start in 2026 and will deliver an integrated luminosity of up to 4000 fb^{-1} over the decade that follows. The instantaneous luminosity will reach up to 7.5×10^{34} cm^{-2} s^{-1}, corresponding to an increase by an approximate factor of 5 compared to the typical luminosities of Run 2. Two extended periods without physics operation, Long Shutdown 2 in 2019–2020 and Long Shutdown 3 from 2024 until mid 2026, are anticipated prior to the HL-LHC phase. Significant upgrades of the ATLAS detector will take place during these periods in order to cope with the high-radiation environment and the large increase in the number of collisions per bunch crossing (pileup). The ATLAS Phase-II Scoping Document [1] provides an overview of the Phase-II plans.

Pileup is one of the main challenges at the HL-LHC. In the nominal operation scheme, the interaction region will have a Gaussian spread of 45 mm along the beam axis[1] and a pileup of 200 simultaneous pp interactions on average ($\langle\mu\rangle = 200$), corresponding to an average interaction density of 1.8 collisions/mm.

A major challenge for the tracking detectors is to efficiently reconstruct the charged particles created in the primary interactions and correctly assign them to the production vertices. This requires the resolution of the longitudinal track impact parameter (z_0), provided by the Inner Tracker (ITk), to be much smaller than the inverse of the average pileup density (0.6 mm). The z_0 resolution is well below this limit in the central region, but becomes very large in the forward region, reaching up to 5 mm for particles with low transverse momentum (p_{T}). As a result, tracks cannot be associated to the correct vertices in an unambiguous way, leading to reduced performance in terms of heavy-flavour tagging, lepton isolation and the identification of jets originating from pileup interactions.

A powerful new way to address this challenge is to exploit the time spread of the collisions in each bunch crossing to distinguish between tracks originating in collisions occurring very close in space but well-separated in time. This requires the ability to measure the time of individual tracks with a precision much smaller than the spread of the collision times. In the nominal operating scheme of the HL-LHC, this distribution has a Gaussian

[1] The ATLAS experiment uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upward. Cylindrical coordinates (r, ϕ) are used in the transverse plane, ϕ being the azimuthal angle around the z-axis. The pseudorapidity is defined in terms of the polar angle θ as $\eta = -\ln\tan(\theta/2)$.

spread of 175 ps. This timing information is complementary to the spatial information and kinematic measurements provided by the tracker and calorimeters, and thus helps resolve ambiguities.

In this context, the High-Granularity Timing Detector (HGTD) is proposed. With an expected time resolution for minimum-ionising particles (MIPs) of approximately 30 ps, corresponding to the performance of the currently available technology, this device will be able to assign each incident charged particle to an interaction vertex with significantly improved accuracy, effectively reducing the amount of pileup by a factor of $175/30 \approx 6$.

The HGTD is a unique new tool that enhances the physics performance capabilities of the ATLAS detector in the endcap and forward regions, enabling similar performance for the reconstruction of forward jets, leptons, and the tagging of heavy-flavour jets as is expected in the central region. In addition, the HGTD offers unique capabilities for the online and offline luminosity determination, and can provide a minimum-bias trigger.

The proposed HGTD will complement the ITk to provide:

- Significantly improved pileup mitigation up to $|\eta| = 4$, covering a very important region for vector-boson fusion (VBF) processes.
- Timing information for nearly all primary vertices.
- Timing determination for charged particles in the region $2.4 < |\eta| < 4.0$.
- Powerful luminosity measurements for each bunch crossing separately, including valuable estimates of background processes.

Since the Scoping Document [1], the ATLAS HGTD group has made significant progress on the impact of time measurements on the global object-level performance, the sensitivity of physics measurements and the conceptual design of the detector. These developments are presented in this document, and intensive R&D on sensors and front-end electronics is still ongoing. Most of the object-level results are presented for several scenarios corresponding to the time resolution expected at different points during the lifetime of the detector, as it evolves with radiation damage and replacement of the detector and electronics parts at inner radii.

This document is organised as follows. Section 2 gives an overview of the requirements on the detector design, including details of the relevant HL-LHC operation parameters and radiation levels. Section 3 summarises the physics motivation for the HGTD, presenting the resulting improvements in object reconstruction, luminosity measurement capabilities and impact on selected physics analyses. The details on the conceptual detector design, the sensor specifications and results from irradiation, laboratory and beam tests, followed by the design and initial results for the readout electronics are described in Section 4. Section 5 describes the installation procedures, the infrastructure for the cooling and power systems and integration in the ATLAS cavern. Finally, Section 6 discusses the costs and schedule of the project activities before an outlook towards the next steps are presented in Section 7.

2 Detector requirements

The space available to install new detectors in front of the ATLAS endcap calorimeters is limited and this constrains the location and acceptance of the HGTD. The minimal inner radius of the HGTD cannot be less than 110 mm, so as to allow the endcap cryostat to move over a pump located on the beam pipe when opening and closing the detector. The outer radius of the vessel is limited to 1000 mm, and it needs to house the detector electronics, moderator and space for routing services to the outside. Taking these constraints into account, the radial extent of the active area is 120 mm to 640 mm, yielding an acceptance in pseudorapidity from 2.4 to 4.0. The envelope in z for the full detector including supports and front and rear covers is 75 mm. In addition, to protect the ITk and the HGTD from back-scattered neutrons, 50 mm of moderator material will be installed in front of the endcap calorimeters, as in the current ATLAS detector. The detector will be located at $z = \pm 3.5$ m, in the volume currently occupied by the Minimum-Bias Trigger Scintillators (MBTS), just outside the ITk volume and in front of the endcap and forward calorimeters, as shown in Figure 2.1 and Table 2.1.

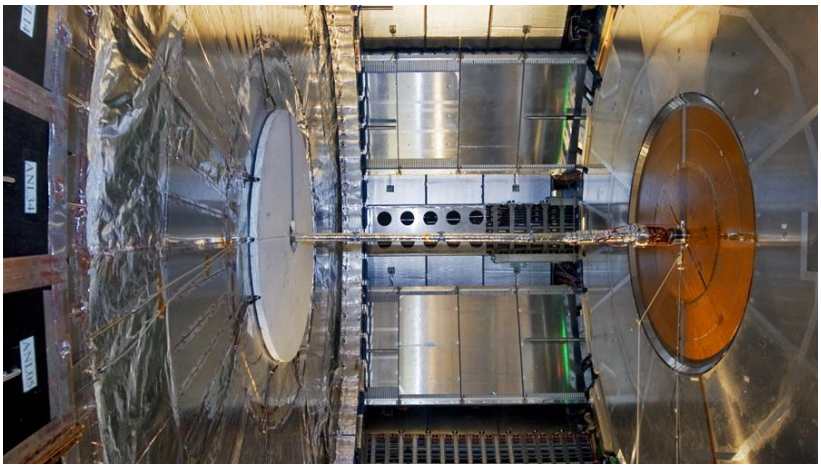


Figure 2.1: A photo of the current ATLAS layout (opened for maintenance), showing the gap between the ATLAS endcap calorimeter on the left and the tracking detectors on the right, where the HGTD will be installed. Currently the space is occupied by the MBTS (white disk, in front of the endcap calorimeter).

A silicon-based timing detector technology is preferred due to the space limitations. The sensors must be thin and configurable in arrays. In close collaboration with RD50 [2] and

Pseudorapidity coverage	$2.4 < \|\eta\| < 4.0$
Thickness in z	75 mm (+50 mm moderator)
Position of active layers in z	3435 mm $< z <$ 3485 mm
Radial extension:	
Total	110 mm $< R <$ 1000 mm
Active area	120 mm $< R <$ 640 mm
Time resolution per track	30 ps
Number of hits per track:	
$2.4 < \|\eta\| < 3.1$	2
$3.1 < \|\eta\| < 4.0$	3
Pixel size	1.3×1.3 mm^2
Number of channels	3.54M
Active area	6.3 m^2

Table 2.1: Main parameters of the HGTD.

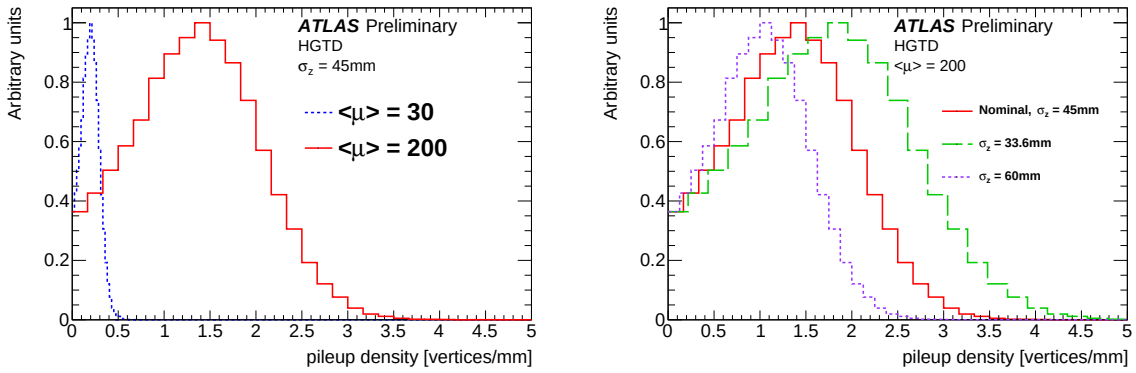
manufacturers, an extensive R&D program is progressing quickly towards sensors that provide the required timing resolution in harsh radiation environments. Low Gain Avalanche Detector (LGAD) [3] pixels of 1.3×1.3 mm^2 with an active thickness of 50 µm fulfil these requirements. This pixel size ensures occupancies below 10% at the highest expected levels of pileup, small dead areas between pixels, and low sensor capacitance which is important for the time resolution. A custom application-specific integrated circuit (ASIC), which will be bump-bonded to the sensors, is being developed to meet the requirements on time resolution and radiation hardness. The ASIC will also provide functionality to count the number of hits registered in the sensor and transmit this at 40 MHz to allow unbiased, bunch-by-bunch measurements of the luminosity and the implementation of a minimum-bias trigger. After optimising the layout for timing performance and cost, the detector design described in this document will give an average of three (two) hits per track at $R < 320$ mm ($R > 320$ mm). A detailed description of the detector layout is presented in Section 4.

2.1 Beam conditions at the HL-LHC

The beam-spot characteristics of the HL-LHC have not yet been determined. At present, the longitudinal beam-spot size (Gaussian width) is expected to be between 30 to 60 mm, while the width in time could be between 175 and 260 ps. The case considered in the studies presented here is the *nominal* one, with Gaussian spreads in z and time of 45 mm and 175 ps respectively.

The spatial pileup line density, i.e. the number of collisions per length unit in the z direction during one bunch crossing, is a key quantity for evaluating the performance of ATLAS with and without the HGTD. For an average of 200 collisions per bunch crossing, denoted $\langle\mu\rangle = 200$, an average pileup density of 1.8 collisions/mm is expected. This average masks

the effect of the local variations illustrated in Figure 2.2. The local pileup vertex density is calculated by summing the number of collisions in a window of ± 3 mm around the signal vertex for $\langle \mu \rangle = 200$. This is large enough to avoid quantisation effects and small enough to probe the tails of the distribution. The other curve is obtained by scaling which effectively increases the window size.



(a) Nominal HL-LHC scenario for $\langle \mu \rangle = 30$ and 200.

(b) Different HL-LHC beam-spot scenarios.

Figure 2.2: Local pileup vertex densities for (a) different values of $\langle \mu \rangle$, and (b) different HL-LHC beam-spot scenarios.

Figure 2.2(a) shows the pileup densities for $\langle \mu \rangle = 30$ and 200 for the same beam spot size, the latter corresponding to the nominal beam-spot scenario at the HL-LHC. The most probable local pileup density for this scenario is around 1.44 collisions/mm, corresponding to an increase by a factor six with respect to $\langle \mu \rangle = 30$. In Figure 2.2(b) the local pileup density is presented for the nominal and two alternative beam-spot scenarios at the HL-LHC. They differ in vertex density due to the difference in the size of the beam spot along z. All three distributions are at significantly higher values than $\langle \mu \rangle = 30$, and all feature most probable values in the range 1–2 collisions/mm.

Timing information can supplement the tracker z_0 measurement in assigning tracks to vertices and mitigate the impact of a high vertex density. To illustrate this, an example is presented in Figure 2.3, which shows a single event with 200 interactions in the z–t plane, where each ellipse corresponds to a truth vertex. The extent of each ellipse is 30 ps in time and 1 mm in z. The vertical dotted lines indicate the z position of the reconstructed primary vertices in the event. The red ellipse and the red solid line indicate the hard-scatter vertex. The tracker sees the event as a one-dimensional projection on the z axis, where a large number of tracks from vertices occurring at different times but very close in space lead to ambiguities in the track-to-vertex association. This happens when the distance between vertices is of the same order or smaller than the resolution of the longitudinal impact parameter of the track, which happens more often for tracks in the forward region. With the addition of the HGTD, ATLAS can view the event in two dimensions, making it possible to resolve the ambiguities of tracks belonging to different interactions.

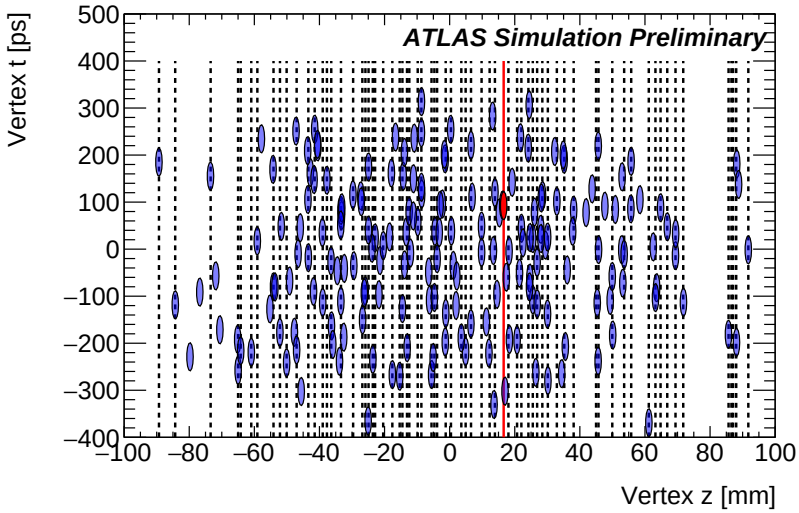


Figure 2.3: Visualisation in the z–t plane of an event with a hard scatter (red ellipse) with about 200 pileup interactions (blue ellipses) superimposed. The dashed vertical lines represent the positions of reconstructed vertices.

2.2 Time resolution

The goal of the detector design is to provide the best possible time resolution in order to effectively suppress the effects of pileup in the forward region. A time resolution of 30 ps per track has been shown to be achievable in test beam studies and would provide a factor of 6 improvement in the track-to-vertex association. This per-track resolution is therefore established as a requirement for the detector design.

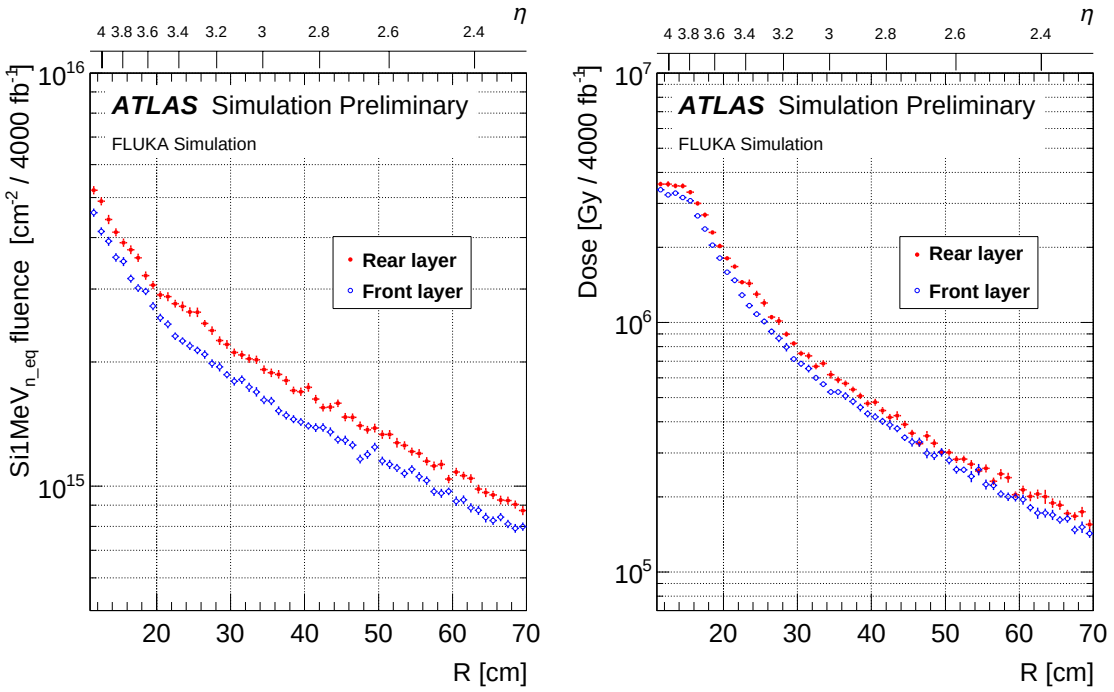
The main contributions to the time resolution of a detector element are:

$$\sigma^2_{\text{total}} = \sigma^2_{\text{L}} + \sigma^2_{\text{elec}} + \sigma^2_{\text{clock}} \tag{2.1}$$

where σ^2_{L} are Landau fluctuations in the deposited charge as the charged particle traverses the sensor, σ^2_{elec} are the contributions from the readout electronics, and σ^2_{clock} is the clock contribution. Beam tests and sensor simulations show that thinner silicon reduces the contribution from Landau fluctuations. With a 50 µm thick LGAD sensor, this contribution amounts to approximately 25 ps. With fast detector signals and a high signal-to-noise ratio, the contribution from the electronics can be kept to approximately 25 ps. This is achievable only if applying corrections for the time walk induced by different signal amplitudes, using small bins in the time-to-digital conversion and applying precise in-situ inter-calibration. The details of the design of the readout electronics to achieve this are described in Section 4.4. The clock contribution is required to be below 10 ps; its distribution is discussed in more detail in Section 4.4.13.

2.3 Radiation hardness

At the end of the HL-LHC (4000 fb^{-1}), the maximum neutron-equivalent fluence at a radius of 120 mm should reach $4.9 \times 10^{15}\,n_{eq}/cm^2$ and the total ionising dose (TID) will be about 3.6 MGy, as shown in Figure 2.4. A safety factor of 1.5 is applied to both numbers to account for uncertainties in the simulation. An additional factor of 1.5 is applied to the TID due to uncertainties in the behaviour of the electronics after irradiation. This leads to a total safety factor of 1.5 for the sensors that are most sensitive to the particle fluence, and 2.25 for the electronics which are more sensitive to the TID. After applying these, the detector would need to withstand $7.35 \times 10^{15}\,n_{eq}/cm^2$ and 8.1 MGy.



(a) Nominal Si1MeV$_{n_{eq}}$ fluence for HL-LHC.

(b) Nominal ionising dose for HL-LHC.

Figure 2.4: Nominal fluence and ionising dose as functions of the radius in the innermost and outermost sensor layers of the HGTD for 4000 fb^{-1}, i.e. before including safety factors. The η range shown at the top corresponds to the z-location of the second layer.

This amount of radiation damage to lowest-radius sensors and electronics suggests that this innermost part of the detector should be replaced after half of the HL-LHC program. The plan is therefore to replace the sensors and ASICs located at a radius up to about 320 mm ($3.08 < |\eta| < 4.0$). This corresponds to about 32% of the sensors and ASICs. Consequently, the sensors and ASICs will be exposed to a maximum of $3.7 \times 10^{15}\,n_{eq}/cm^2$ and 4.1 MGy. More details can be found in Sections 4.3 and 4.4.

3 Physics motivation

This section discusses how the precision time measurement capability introduced by the HGTD enhances the performance for tagging jets, tagging b-jets, and calculating lepton isolation in the forward region, as well as the resulting impact of these improvements on the sensitivity of a few selected physics analyses. Additional applications of the HGTD, including luminosity measurements and trigger usage, are also presented.

The studies done to optimise the detector design and to measure track-level performance are based on full simulation and reconstruction. In the full simulation of the HGTD, each sensor is implemented as a single homogeneous volume. The active area implemented in the full simulation is 120 mm $< R <$600 mm (smaller than the 640 mm of the proposed detector design), with a granularity of 0.5×0.5 mm^2. Four layers of sensors were implemented, with a distance of approximately 8 mm between each layer. Different granularities, as well as the inactive inter-pixel zones in the sensors and the distribution of the modules in the layers (readout row layout, overlap between modules, etc) are implemented downstream at the analysis level. Differences between this simplified geometry, and a much more detailed description at the GEANT level, are expected to have a minor effect on the simulated results.

In most of the object-level performance studies, full simulation and reconstruction of the tracker, calorimeters and muon system is combined with a fast simulation of the HGTD which smears the nominal track times with the expected per-track resolution. This does not include the expected contribution of the clock distribution to the resolution. The efficiency of assigning hits to a track is also taken into account, based on the studies presented in section 3.1.1. In the jet performance studies, the time of the hard-scatter vertex, t_0, is assumed to be known with a precision much smaller than 30 ps. In general, for a timing detector which is not hermetic, the ability to accurately determine t_0 depends on the acceptance and the event topology. For HGTD in particular, this ability depends on how many tracks from the hard-scatter vertex are within $2.4 < \eta < 4.0$ and their p_{T} distribution. Dedicated studies of t_0 reconstruction and the resulting impact on physics-object performance are planned for the Technical Design Report (TDR).

The expected timing performance for this smearing is discussed in Section 4.1 where four scenarios are defined. The first one, referred to as *Initial*, corresponds to the expected performance at the beginning of the HL-LHC operation. The second one, denoted *Intermediate*, takes into account the expected timing resolution degradation due to radiation damage after half of the HL-LHC program (2000 fb^{-1}). The *Final* scenario represents the expected

timing resolution at the end of the HL-LHC program (4000 fb^{-1}) assuming that the sensors and readout electronics at $R < 320$ mm are replaced after half of the integrated luminosity has been delivered. The *Worst Case* scenario assumes a timing resolution of 60 ps per hit for the sensors, independent of the radius. This is worse than the expected resolution of the innermost sensors after 4000 fb^{-1} without replacement.

The performance for several physics objects is also studied as a function of η to show the improvement in the endcap region and compare it to that of the central region to motivate the chosen acceptance of the HGTD.

3.1 Performance for object reconstruction

The precision timing measurement of the HGTD can improve the overall performance for reconstructing physics objects. The key to these improvements relies on the use of timing information, in addition to spatial (z) information, to associate tracks to vertices with high efficiency and low pileup contamination. The use of the HGTD for track-to-vertex association is described below, followed by studies that quantify how the HGTD improves pileup-jet suppression, b-tagging, and electron isolation in the forward region.

3.1.1 Track-level performance

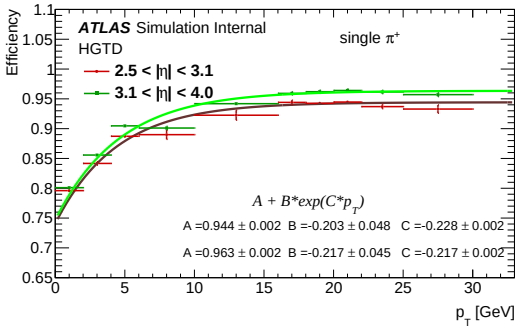
Track extrapolation to the HGTD

The matching of tracks reconstructed with the ITk to hits in the HGTD has been studied using single-pion samples ($\langle\mu\rangle = 0$) and a physics sample with VBF-produced $H \to Z(\nu\nu)Z(\nu\nu)$ at $\langle\mu\rangle = 200$, both with full simulation of the HGTD. The matching is performed by extrapolating the tracks to the HGTD; only tracks with an extrapolation within the HGTD region are used. The hits in the pixels that are within a radius of 5 mm of the track extrapolation in the transverse plane are considered, and the closest one is matched.

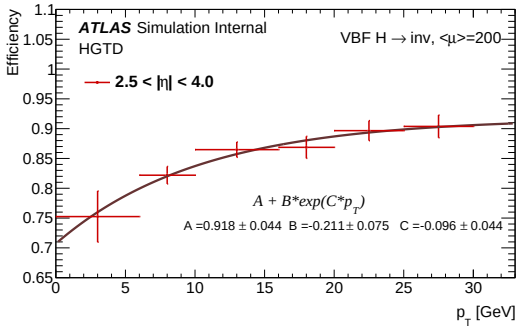
The distribution of the minimum distance between the track extrapolation and a hit can be described as a Gaussian core with non-Gaussian tails. In the case of pions, the fraction of tracks outside the core varies between 15% at low p_{T} to about 5% at high p_{T}. For $p_{\mathrm{T}} = 2$ GeV, the track extrapolation is typically within 1 mm of the hit, and improves at higher p_{T}. It is limited primarily by the pixel size.

Figure 3.1(a) shows the efficiency for matching a reconstructed track with at least one HGTD pixel as a function of the reconstructed track p_{T} for samples of single pions with p_{T} between 0.5 and 20 GeV. The figure shows two curves, one for $R < 320$ mm (the region with higher overlap between modules), corresponding to $|\eta| > 3.1$ and the other for $R > 320$ mm. Tracks with $|\eta| < 2.5$ or $|\eta| > 4.0$ are not considered in order to avoid border effects. An exponential fit is performed to both sets of points, and the obtained values of the parameters are presented in the figure. These functions are used in order to take into

account the effect of the efficiency in the performance studies presented in the following sections. At high p_{T}, the efficiency approaches 95%, limited by non-instrumented regions. At low p_{T}, the efficiency decreases to about 80%, due to the increased effect of interactions with the material in front of the HGTD. This material corresponds approximately to 0.2 interaction lengths at $|\eta| = 2.4$, and increases to about 0.4 interaction lengths at $|\eta| = 3.8$. The comparison of the two curves shows a small $|\eta|$ dependence for all p_{T} values, the higher $|\eta|$ region presenting an efficiency approximately 3% higher than the lower one.



(a) Efficiency for matching a reconstructed track to at least one HGTD hit.



(b) Estimated efficiency for assigning the correct time to reconstructed tracks.

Figure 3.1: Efficiencies for matching tracks to at least one pixel in the HGTD in single-pion events and for correctly reconstructing the time of a track in a high-pileup environment. An exponential fit is performed on the points, and the obtained values of the parameters are shown.

With a pileup of $\langle\mu\rangle = 200$, almost all tracks have hits closer than 5 mm; because most of them correspond to pileup interactions, timing information needs to be used to assign hits to the track. The hits matched to a track are selected so as to be the closest to the track in the layers that have consistent timing between them. They must be within 5 mm of the extrapolation, and it is required that their RMS deviation from their average time is smaller than 60 ps. The efficiency for correctly assigning a time to a track in a high-pileup environment is shown in Figure 3.1(b) as a function of track p_{T}. The dependence of the efficiency with p_{T} is similar to that obtained with single-pion samples, though 4% lower. There is a slight decrease for large $|\eta|$, due to the increased flux of pileup tracks, increasing the probability of an incorrect hit association.

The hit-to-track matching efficiency in the HGTD was also measured in a sample of single muons with $p_{\mathrm{T}} = 45$ GeV, and found to be 98% independent of η. The higher efficiency with respect to pions is due to the reduced probability for the muons to interact with material in front of the HGTD.

This study is a first step in the development of the association of the track information with timing information in the HGTD. The main inefficiency for the association has been identified as interactions in the material in front of the HGTD. In the future, more sophisticated pattern recognition algorithms should be studied to improve this efficiency.

Track-to-vertex association

The precise assignment of tracks to primary vertices (track-to-vertex association) is one of the key elements to mitigate the effects of pileup on the full suite of event reconstruction algorithms at hadron colliders. Jet reconstruction and calibration, pileup-jet mitigation, b-tagging, lepton isolation, and jet substructure measurements rely strongly on the correct assignment of tracks to primary vertices and jets.

A track is associated to a vertex if its origin is geometrically compatible in z with the vertex position. The compatibility is determined by the resolution on the track z_0 impact parameter such that

$$\frac{\left|z_0 - z_{\text{vertex}}\right|}{\sigma_{z_0}} < 2, \tag{3.1}$$

where σ_{z_0} is the per-track resolution on the longitudinal impact parameter and depends primarily on the track η and p_{T}. Figure 3.2 shows a parameterization of σ_{z_0} as a function of η, for different p_{T} values. This parameterization was obtained as the inter-quartile range of the impact parameter resolution. The choice of $2\sigma_{z_0}$ as selection cut is to ensure a track selection efficiency of 95% independent of η and p_{T}.

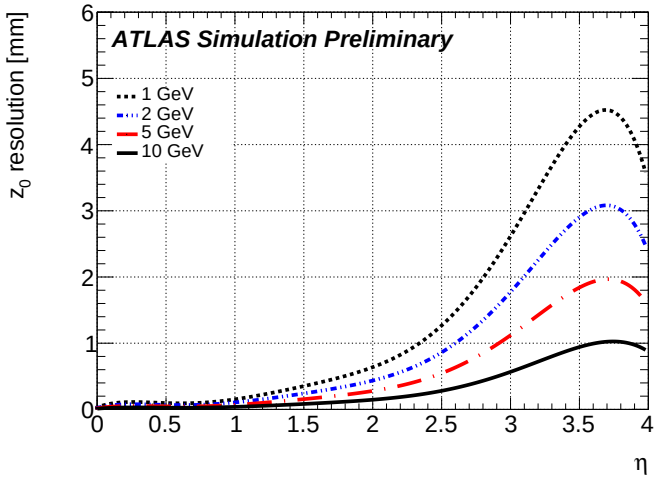


Figure 3.2: The resolution of the longitudinal track impact parameter, z_0, as a function of η for different p_{T} values.

The reliability of the track-to-vertex association depends on the value of σ_{z_0} relative to the average pileup density $\langle\rho(z)\rangle$. The average number of interactions within a window of $\left|z_0 - z_{\text{vertex}}\right| = 2\sigma_{z_0}$ is given by $N = 2\langle\rho(z)\rangle 2\sigma_{z_0}$. This means that in order to unambiguously associate tracks to vertices based on Equation. (3.1), N has to be smaller than 1, or $\sigma_{z_0} < 1/4\langle\rho(z)\rangle$. For a track with z_0 at the origin, where the average density peaks, this value is approximately 160 µm. If σ_{z_0} is larger than this value, the association of tracks to vertices becomes ambiguous because one same track may be compatible with multiple

nearby vertices. It is important to note that this argument applies to prompt tracks such as those produced in light-quark and gluon jets, or prompt leptons. The association of displaced tracks from the decay of B/D hadrons to primary vertices requires the use of a larger z window, which will lead to greater pileup contamination.

While the longitudinal impact parameter resolution is relatively constant and small for $|\eta| < 1.5$, it grows rapidly with pseudorapidity, reaching very large values of several millimetres for $|\eta| \gtrsim 2.5$. The resolution is further degraded at low track p_{T} due to multiple scattering effects. The η dependence of the impact parameter resolution is mostly determined by the geometry of the inner detector. As η increases, tracks become more collinear to the beam line. The form of the distribution, including the improvement at the largest η is related to the material distribution in the tracker.

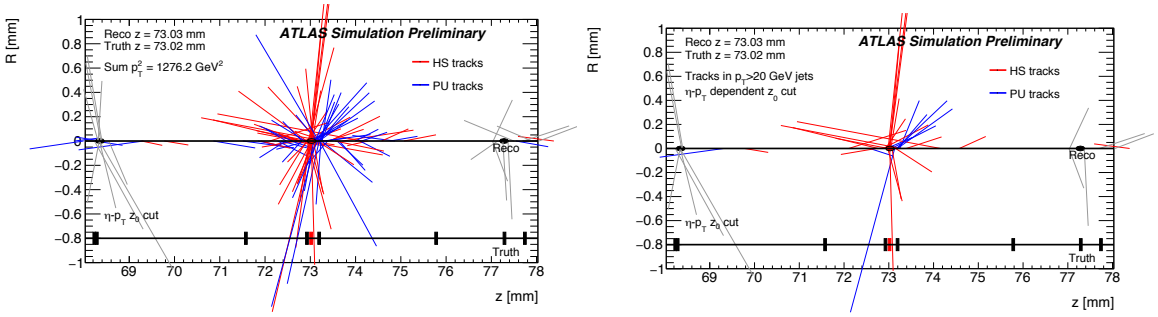
Based on Figure 3.2, a 1 GeV track with $\eta = 3$ has a z_0 resolution of approximately 2.5 mm, leading to a $\pm 1\sigma$ window of 5 mm in z for the vertex position. With a most probable average pileup vertex density of 1.8 vertices/mm at $z = 0$, this means that, on average, a forward track can be compatible with up to about 13 near-by vertices on average. Or, in other words, track-to-vertex association will suffer significantly from pileup contamination.

This effect is illustrated in Figure 3.3(a), which shows the pileup-track contamination around a hard-scatter vertex in a R–z view. All tracks displayed in this figure have been assigned to the reconstructed primary vertex (drawn in the centre of the figure) according to Eq. (3.1). All tracks are required to pass standard quality selections [4] and have $p_{\mathrm{T}} > 0.9$ GeV. Figure 3.3(b) shows a similar view of the same event but it includes only the tracks associated with calorimeter jets with $p_{\mathrm{T}} > 20$ GeV. This figure clearly shows the presence of a jet entirely made of pileup tracks (shown in blue), that cannot be identified as such because all tracks have been assigned to the hard-scatter vertex. It also shows the large reduction of pileup when only considering tracks inside jets. This is due to the effect of the reduced jet area (A^{jet}), which, for the case of the anti-k_t algorithm with distance parameter $R = 0.4$ and under the assumption that pileup tracks are uniformly distributed in pseudorapidity, is given by

$$\frac{A^{\mathrm{jet}}}{2\pi \cdot 2 \cdot \Delta\eta} \rho(z) \cdot \Delta z^{\mathrm{trk,vtx}} = \frac{\pi \cdot 0.4^2}{2\pi \cdot 2 \cdot 4.0} \rho(z) \cdot 2\sigma_{z_0}.$$

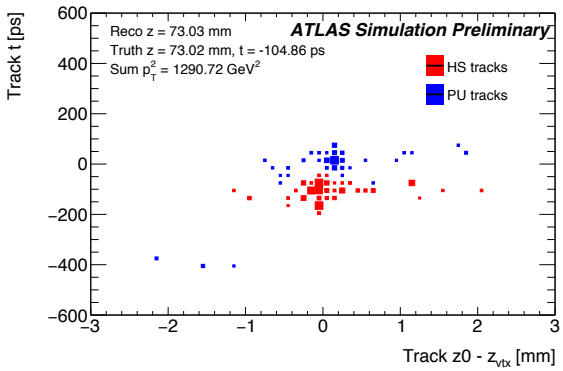
As an example, for a $R = 0.4$ anti-k_t jet in the forward region ($|\eta| > 2.4$) under nominal HL-LHC beam conditions, this fraction is about 10%.

Figure 3.4 shows different views of the same event. A two-dimensional distribution of the reconstructed times and z positions of the p_{T}-weighted tracks is shown in 3.4(a), while 3.4(b) and 3.4(c) show one-dimensional projections in z and time, respectively. While the high-p_{T} (and predominantly central) hard-scatter and pileup tracks are visibly separated in z, forward low-p_{T} tracks are indistinguishable if only spatial information is considered. The time

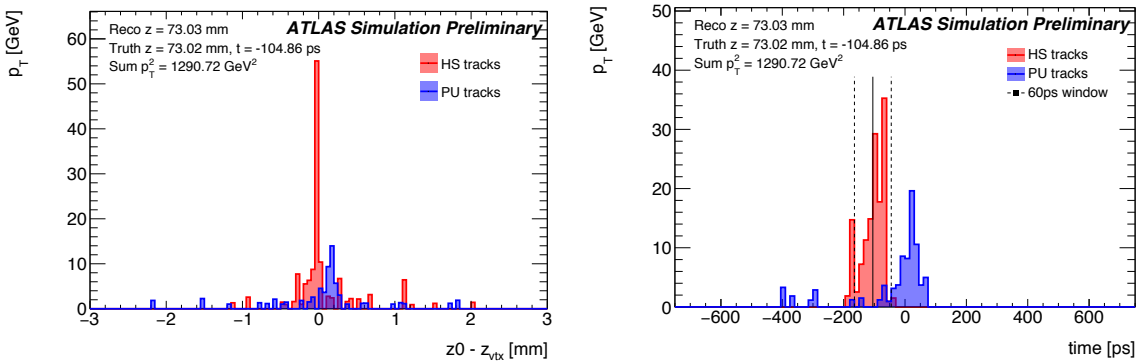


(a) All tracks associated with primary vertices. (b) Only tracks also matched to jets with $p_{\mathrm{T}} > 20$ GeV.

Figure 3.3: View in the R–z plane of the tracks associated to the primary vertices in a VBF-produced $H \to Z(\nu\nu)Z(\nu\nu)$ event at $\langle\mu\rangle = 200$. The length of each line is proportional to the track p_{T}. The positions of the reconstructed and truth vertices are indicated at $R = 0$ and $R = -0.8$ mm, respectively. Grey lines show tracks attached to other (pileup) reconstructed vertices.



(a) Reconstructed times and z positions.



(b) Reconstructed z positions. (c) Reconstructed times.

Figure 3.4: Distributions of reconstructed times and z positions of the p_{T}-weighted tracks associated to the hard-scatter vertex of an event with a VBF-produced Higgs boson decaying invisibly with $\langle\mu\rangle = 200$.

projection in Figure 3.4(c), on the other hand, shows that both vertices can be effectively resolved with a time resolution of 30 ps.

The only handle for the forward tracker to address the challenge of pileup on track-to-vertex association in the forward region is to tighten the selection cuts used in Eq. (3.1), reducing the track-to-vertex association efficiency. The HGTD detector can extend the track-to-vertex association capability of the tracker in the central region to the forward region by the use of two-dimensional z-t selection criteria. In addition to Eq. (3.1), the following selection is introduced,

$$\frac{|t - t_0|}{\sigma_t} < 2, \tag{3.2}$$

where t is the track time measured by the HGTD, and σ_t is the track time resolution, assumed to be 30 ps constant in p_{T} and η. The vertex time, t_0, is assumed to be known with high accuracy by averaging the track time of high-p_{T} good-quality tracks attached to the primary vertex. The use of this two-dimensional track-to-vertex association allows to maintain high track-selection efficiency while greatly reducing the contamination of pileup tracks within the z selection window. The use of timing information in the forward region, hence, can compensate for the worsening of the z_0 impact parameter resolution, allowing the tracker to maintain good track-to-vertex association performance for all η, mitigating the impact of the large pileup contamination in the forward region. The methods used here give correct results as long as there are enough high-p_{T} tracks within geometrical acceptance of the HGTD. Since this requirement depends on the event topology, dedicated studies are required to determine the impact of a non-ideal t_0 reconstruction for different physics processes. Even in the cases where t_0 cannot be measured with certainty, pattern recognition algorithms may still be capable of separating tracks in jets originating from different pileup interactions for jets containing more than one track, resulting in improved performance in jet reconstruction. Given the complexity, the development of these algorithms is beyond the scope of this document, but a high priority moving towards the TDR.

The following sections show how the enhanced pileup-mitigation capability of the HGTD in the forward region impacts the identification and rejection of pileup jets, the tagging of heavy-flavour jets, and the efficiency for for lepton-isolation requirements.

3.1.2 Suppression of pileup jets

Pileup is one of the most difficult challenges for object identification under HL-LHC conditions. Particles produced in pileup interactions can contaminate the jets of interest coming from the hard-scatter vertex, thereby reducing the accuracy of the jet energy determination. Pileup interactions can also produce additional jets which do not originate from the primary hard-scatter interaction. These pileup jets can be produced as the result of a hard

QCD process from a pileup vertex, or by random combinations of particles from multiple vertices. At low jet p_{T}, the latter mechanism is dominant, whereas at high jet p_{T}, the majority of pileup jets are QCD jets.

Pileup jets can reduce the precision of Standard Model measurements and the sensitivity to discover new physics. For example, additional jets can increase the amount of background events passing a selection, as well as reduce the efficacy of kinematic variables or discriminants to separate signals from backgrounds. Hence, the efficient identification and rejection of pileup jets is essential to enhance the physics potential of the HL-LHC.

The key element to suppress pileup jets is the accurate association of jets with tracks and primary vertices. A simple but powerful discriminant for pileup-jet suppression is the $R_{p_{\mathrm{T}}}$ jet variable, defined as the scalar sum of the p_{T} of all tracks that are inside the jet cone and originate from the hard-scatter vertex PV_0, divided by the fully calibrated jet p_{T} , i.e.

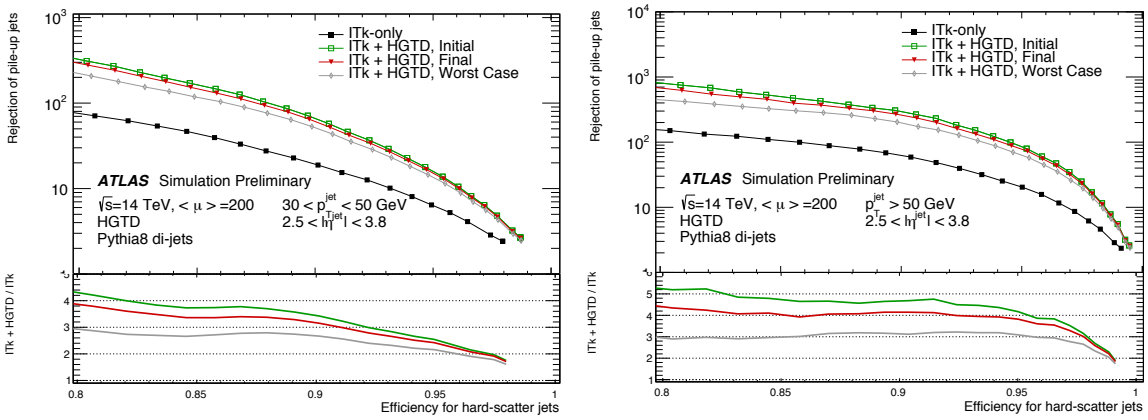
$$R_{p_{\mathrm{T}}} = \frac{\Sigma p_{\mathrm{T}}^{\mathrm{trk}}(\mathrm{PV}_0)}{p_{\mathrm{T}}^{\mathrm{jet}}}.$$

The tracks used to calculate $R_{p_{\mathrm{T}}}$ fulfil the quality requirements defined in Ref. [5] and are required to have $p_{\mathrm{T}} > 1$ GeV. The distance between the hard-scatter vertex and the longitudinal impact parameter of the tracks used in the $R_{p_{\mathrm{T}}}$ calculation is required to be within 1 mm and 4 mm, depending on the $|\eta|$ of the track.

Hard-scatter and pileup jets for simulated events are defined by their matching to truth jets, which are reconstructed from stable and interacting final state particles coming from the hard interaction. The matching criteria are defined in Ref. [6]. Reconstructed hard-scatter jets are required to be within $\Delta R = \sqrt{(\Delta\eta)^2 + (\Delta\phi)^2} < 0.3$ of a truth jet with $p_{\mathrm{T}} > 10$ GeV. The pileup jets must be at least $\Delta R > 0.6$ away from any truth jet with $p_{\mathrm{T}} > 4$ GeV. The performance has been studied using a mixture of full reconstruction (for tracks and jets) and fast simulation (for the HGTD).

At moderate levels of pileup, where track impact parameter measurements can be used to assign tracks to vertices with relatively little ambiguity, small values of $R_{p_{\mathrm{T}}}$ correspond to jets which have a small fraction of charged-particle p_{T} originating from the hard-scatter vertex PV_0. These jets are therefore likely to be pileup jets. However, at high pileup conditions, and particularly in the forward region, the power of this discriminant is reduced. The effect can be mitigated by including timing information from the HGTD, removing tracks outside a $2\sigma_t$ window around the time of the hard-scatter vertex, as shown in Figure 3.4(c). This figure shows an example event where a jet originating from a pileup interaction (in blue) is misidentified as a hard-scatter jet when only using tracking information. All tracks from the pileup jet are compatible with the hard-scatter vertex within the z_0 resolution. The use of timing information in the $R_{p_{\mathrm{T}}}$ discriminant can suppress this pileup jets, improving the overall performance of pileup-jet suppression.

Figure 3.5 shows the rejection[1] of pileup jets as a function of the efficiency for selecting hard-scatter jets using the R_{p_T} discriminant for jets with low and high p_T in dijet events with $\langle\mu\rangle = 200$ without and with the HGTD for the different timing resolution scenarios. A significant improvement in performance of up to a factor of 4 higher pileup-jet rejection at constant efficiency is achieved with the use of timing information. This study was done using the smearing functions to simulate the HGTD performance and taking into account the matching efficiency.



(a) Jets with $30 < p_T < 50$ GeV.

(b) Jets with $p_T > 50$ GeV.

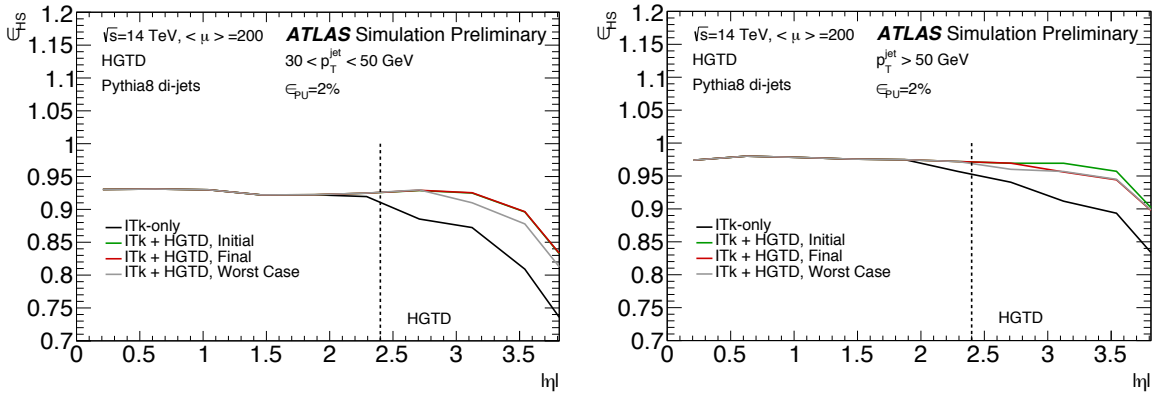
Figure 3.5: Pileup-jet rejection as a function of hard-scatter jet efficiency in the $2.4 < |\eta| < 4.0$ region, for the ITk-only and ITk + HGTD scenarios with different time resolutions.

It is possible to use a p_T and $|\eta|$ dependent requirement on R_{p_T} to define different working points at fixed efficiencies on hard-scatter and pileup jets. Figure 3.6 shows the hard-scatter jet efficiency for a fixed pileup-jet efficiency, ϵ_{PU}, of 2% (i.e. a rejection factor of 50), as a function of $|\eta|$ of the jet. The HGTD recovers the 10-30% drop in efficiency observed in the forward region, allowing to maintain similar pileup-jet suppression performance as in the central barrel over a large part of its acceptance. Due to the width of the jets, the HGTD improves the efficiency also for jets at slightly lower $|\eta|$ than its geometrical acceptance. The effect is more evident for high-$|\eta|$ and low-p_T jets.

3.1.3 Tagging of heavy-flavour jets

The efficient identification of b-jets and high rejection of light-quark jets is of central importance in the HL-LHC physics program. Tagging b-jets is particularly sensitive to pileup-track contamination. This is due to the fact that b-tagging algorithms consider tracks with large impact parameters (in both the transverse and longitudinal directions) from the decay

[1] Throughout this document, the rejection is defined as the inverse of the mis-tag efficiency.



(a) Jets with $30 < p_{\mathrm{T}} < 50$ GeV.

(b) Jets with $p_{\mathrm{T}} > 50$ GeV.

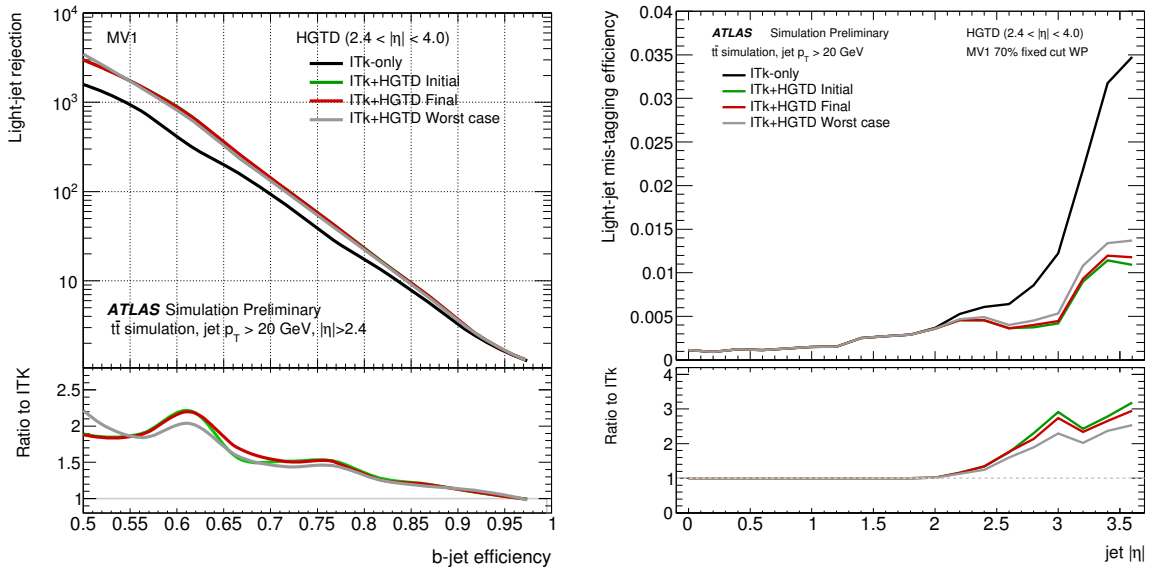
Figure 3.6: Hard-scatter jet efficiency versus $|\eta|$ for a 2% pileup-jet efficiency using p_{T} and $|\eta|$ requirements on the $R_{p_{\mathrm{T}}}$ discriminant, in dijet events.

of displaced vertices. With a larger z_0 window, tracks from nearby pileup interactions are more likely to be selected, leading to an increased rate of misidentified light-quark jets.

Using simulated $t\bar{t}$ events at $\langle\mu\rangle = 200$ and the fast HGTD simulation described above, the impact of the HGTD on the performance of a multivariate b-tagging algorithm is studied for forward jets ($|\eta| > 2.4$). Figure 3.7(a) shows the light-jet rejection versus b-tagging efficiency for the MV1 b-tagging algorithm. The addition of the HGTD removes the majority of pileup tracks from the track selection. As a result, the performance of the b-tagger is significantly improved. For a b-tagging efficiency of 70% and 85%, the corresponding light-jet rejection for MV1 is increased by approximate factors of 1.5 and 1.2, respectively. These factors could be greater for processes where more b-jets are expected in the forward region. Figure 3.7(b) shows the light-jet mis-tag efficiency for a 70% b-tagging efficiency working point as a function of jet $|\eta|$. In both figures, the performance is shown for the ITk-only scenario as well as three scenarios with HGTD timing performance representing different stages of the HL-LHC program. It can be seen that all timing scenarios yield significant improvements in the performance, even in the *Worst Case* scenario. Importantly, significant improvements are observed also after the full radiation damage expected during HL-LHC operation.

3.1.4 Lepton isolation

In this section, studies of how the electron isolation efficiency is improved with HGTD are presented based on the full simulation of the HGTD. The HGTD can be used to assign a time to leptons in the forward region. This information can be exploited to reject tracks which come from other interactions but are spatially close to the energy deposits in the calorimeter



(a) Light-jet rejection.

(b) Light-jet mis-tag efficiency.

Figure 3.7: (a) Light-jet rejection versus b-tagging efficiency for the MV1 tagger and (b) Light-jet mis-tag efficiency for a 70% b-tagging efficiency working point as a function of jet $|\eta|$. The study uses $t\bar{t}$ events at $\langle\mu\rangle = 200$ and shows the achieved performance for different time resolution scenarios. The ratio plots at the bottom show the relative performance achieved with the HGTD with respect to the ITk-only scenario.

and/or the track associated to the lepton. The timing information can reject additional tracks from interactions close in z, according to Eq. (3.1) but separated in time from the hard-scatter vertex, as in Eq. (3.2). The isolation efficiency is defined as the probability that no track with $p_{\mathrm{T}} > 1$ GeV is reconstructed within $\Delta R < 0.2$ of the electron track.

The isolation efficiency is shown in Figure 3.8 as a function of the local vertex density for the ITk-only scenario and three HGTD timing resolution scenarios. While the efficiency drops strongly with the increase of the pileup density when using only the ITk, the addition of the HGTD timing information reduces this drop, keeping an efficiency above 90% even at high pileup density, i.e. with up to three additional vertices around the hard-scatter vertex. For an average pileup density of the order of 1.8 vertices/mm the electron isolation efficiency is improved by about 14%. Even in the *Final* timing scenario, the resolution is sufficient to achieve an isolation efficiency essentially independent of the pileup density at the end of the HL-LHC. The performance in the forward region reaches a level similar to that in the central region. The improvement of the performance is essentially independent of the timing scenario, rendering further improvements to the resolution past 30 ps/track unjustified for this usage.

In addition to these studies of lepton isolation improvements[2], the impact of the HGTD

[2] If a high-η muon-tagger were to be added to the Phase-II upgrade program for ATLAS, the HGTD would be

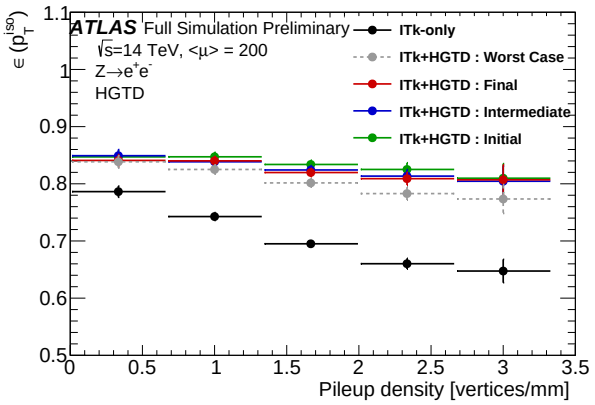


Figure 3.8: Selection efficiency for the electron isolation criteria as a function of the pileup density using the ITk and ITk + HGTD for different timing resolutions.

on the rejection of jets misidentified as electrons is being studied, along with potential optimisations of the isolation criteria natively exploiting the timing information from the HGTD.

3.2 Luminosity measurement

Precise luminosity determination will be a critical component of the precision measurements that make up cornerstones of the HL-LHC physics program. For example, achieving $\mathcal{O}(1\%)$ accuracy on certain measurements of Higgs boson production and its couplings can be limited by the luminosity uncertainty. It is therefore important to be able to determine the luminosity at least as accurately as done in Run I [7] and II of the LHC, and this will be a challenge at the harsh environment at the HL-LHC. The increased pileup leads to increased detector occupancies, posing serious problems for the technologies used traditionally for luminometers.

As a fast high-granularity detector in the forward region, the HGTD provides unique capabilities for measuring the luminosity at the HL-LHC. With detector signal durations in the few-ns range, the charged-particle multiplicities within the acceptance can be determined accurately for each individual bunch crossing separately. The high granularity gives a low occupancy, and therefore excellent linearity between the average number of hits and the average number of simultaneous pp interactions over the full range of luminosity expected at the HL-LHC.

The instantaneous luminosity can vary between each Bunch Crossing ID (BCID) in the LHC. For the best precision of the total delivered luminosity, accurate measurements of

able to provide similar isolation efficiency improvements for muons in the forward region.

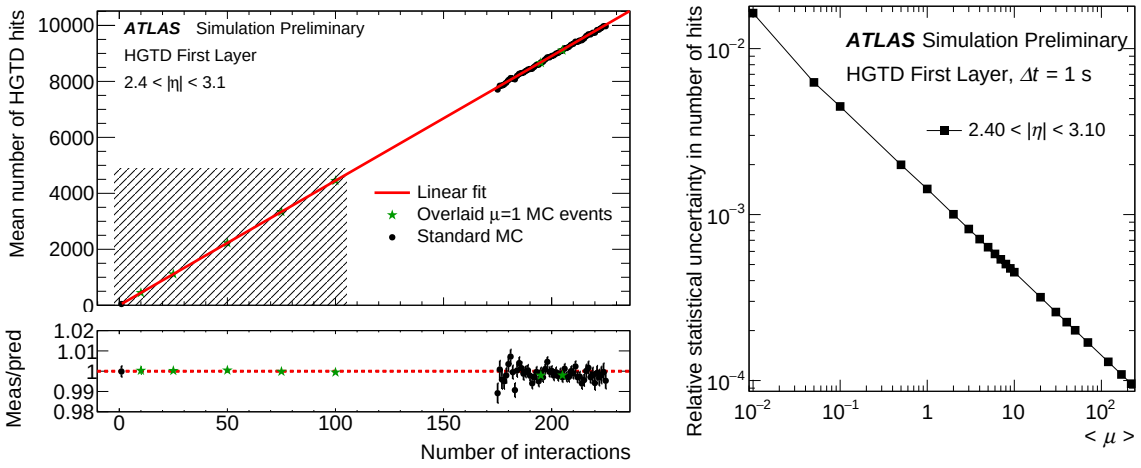
these bunch-by-bunch variations are needed. In the Phase-II ATLAS detector, some luminometers can only measure the bunch-integrated luminosity (e.g. integrated current measurements in the Tile or LAr calorimeters) whereas other more dedicated luminometers such as LUCID and BCM measure the luminosity for each bunch. All these luminometers make fast estimations of the luminosity available online. Other methods for determining the bunch-by-bunch luminosity such as measuring the number of pixel hits, the number of reconstructed tracks, or the number of reconstructed vertices, are only available after a dedicated offline analysis. As HL-LHC is expected to operate with luminosity levelling, there is additional need for an accurate and fast online luminosity measurement to be sent to the machine. The idea for using HGTD as a luminometer is straightforward: the occupancy will be linearly correlated with the number of interactions (i.e. the luminosity). The principle is the same as for measuring luminosity through counting reconstructed tracks [7] or clusters in a pixel detector [8]. If the HGTD is read out independently of the ATLAS trigger, it has the potential to provide an accurate estimate of the bunch-by-bunch luminosity and make it available both online and offline. With detailed occupancy information at 40 MHz, i.e. for every bunch crossing, the HGTD will thereby allow unbiased high-statistics per-BCID luminosity measurements. The measurement is made in a reduced $|\eta|$ range, and in this proposal the plan is to read out the ASICs for sensors at $320\,\text{mm} < R < 640\,\text{mm}$ (equivalent to $2.4 < |\eta| < 3.1$) for the luminosity determination. The exact choice of inner radius for the luminosity data can perhaps be optimised further.

3.2.1 Linearity of luminosity determination

For the proposed range $|\eta| < 3.1$, the average number of hits per layer per pp collision is 44.6, and approximately 7% of the events have no hits. Figure 3.9(a) shows the average number of hits per event registered in the first layer (both sides of the innermost cooling plate) of the HGTD as a function of the number of simultaneous pp interactions. The black points at μ of 1 and around 175-225 are determined from fully simulated minimum-bias events with $\mu = 1$ and $\langle\mu\rangle$ in the range 190-210, respectively. The green stars represent samples where several $\mu = 1$ minimum-bias events have been overlaid to produce samples with intermediate numbers of interactions, while making sure not to double-count multiple hits in the same pixel. A linear fit made to the points in the hatched region at low and intermediate μ values is extrapolated to the $\mu \sim 200$ region where its prediction can be compared to the hit multiplicities extracted from properly simulated high-pileup samples.

3.2.2 Non-linear effects for HGTD luminosity determination

There are two main sources of non-linear effects to consider, due to multiple particles passing through the same pixel and due to noise or background from so-called *afterglow*, caused primarily by activated material in the detector volume, which is distributed approximately uniformly in time. The HGTD is expected to have a low occupancy, which will mitigate the



(a) Linearity of $\langle n_{\text{hits}} \rangle$ as a function of μ.

(b) Statistical uncertainty versus $\langle \mu \rangle$

Figure 3.9: Quantities relevant to the luminosity performance as a function of pileup.

non-linearity of the luminosity measurement from multiple particles passing through the same pixels. Especially at the outer radii, the effect of multiple hits will be negligible. It is also possible to correct for the multiple-hits effect by parameterizing the probability for this to occur as a function of $\langle \mu \rangle$. The time resolution of the HGTD can reduce the effects of noise and background activity, e.g. from activated material in the detector volume. By reading out the occupancy before and after the time window during which particles from the collisions arrive, an estimate of this component can be obtained, for each BCID separately. This estimate can then be used to increase the precision of the luminosity determination by subtracting the occupancy which is expected to be due to noise and background activity. The ability to do an in-situ measurement of the noise and background level for each bunch crossing and BCID separately is a unique capability of the HGTD compared to other luminometers.

3.2.3 Statistical precision of the luminosity determination

Offline luminosity measurements are limited by systematic uncertainties. To confirm that statistical uncertainties are subdominant also for the short time periods used for online luminosity measurements, this has been studied as a function of the duration of the averaging period and $\langle \mu \rangle$. The average number of hits per bunch crossing is simulated using a toy Monte-Carlo method with inputs extracted from fully simulated samples. For each value of $\langle \mu \rangle$, a random number of pp interactions is drawn from a Poisson distribution with a mean equal to μ. For each pp interaction, a number of HGTD hits is then generated randomly based on the distribution of hits per pp interaction extracted from full-simulation samples. By repeating this process 11 000 times (for the number of turns the LHC beams

will make) and averaging the number of hits, the statistical precision achieved in each individual BCID during 1 s of LHC running is emulated. Figure 3.9(b) shows the relative uncertainty expected from statistical fluctuations as a function of $\langle\mu\rangle$ using this method. The coverage of $|\eta| < 3.1$ presented here gives a statistical uncertainty of 0.14% at $\langle\mu\rangle = 1$ and 1.6% at $\langle\mu\rangle = 0.01$. For measurements in the low-μ regime (e.g. during van der Meer scans) better precision can be achieved through a longer averaging time.

3.3 Use of the HGTD in the trigger system

3.3.1 Minimum-bias trigger at Level-0

The data made available at 40 MHz for the luminosity measurements can also be used by the Level-0 (L0) trigger to record minimum-bias events under low-μ data-taking conditions. Such data-taking conditions are expected during e.g. heavy-ion runs, van der Meer scans or for runs dedicated to soft-QCD measurements. The HGTD will be installed where the current MBTS detector is located. The MBTS detector has been used extensively for these purposes during Run-1 and so far in Run-2, e.g. during the heavy-ion runs where it played a crucial role. However, it will not survive at the HL-LHC. With improvements of several orders of magnitude in both granularity and time resolution, the HGTD can provide all the functionality of the MBTS, and much more. The number of hits in the time window centred around the nominal collision time provides good separation between empty bunch crossings and those with pp collisions, and it would be straightforward to implement a trigger condition based on this information. The latency for reaching the Level-0 global trigger processors in time for a decision is not expected to be a problem but needs to be studied in detail.

Potential for improved pileup subtraction algorithms at Level-0 and High-Level Trigger

The data made available at 40 MHz for luminosity estimates could also provide a real-time estimate of $\langle\mu\rangle$ to the hardware-based trigger systems and facilitate pileup subtraction earlier in the trigger. If propagated to the Level-0 trigger system, this information could be used to implement more precise triggers based on jets and missing transverse momentum ($E_{\mathrm{T}}^{\mathrm{miss}}$), allowing lower rates and/or lower thresholds. The simplest pileup subtraction scheme that could be implemented within the CaloGlobal system [3] is an average correction, where an offset dependent on $\langle\mu\rangle$ and jet kinematics (η, p_{T}) is subtracted from the jet p_{T} [9]. The disadvantage of such a scheme is that it does not capture event-by-event fluctuations. The pileup subtraction scheme that is currently being used for jets reconstructed both offline and at the High-Level Trigger involves event-by-event information about the average

[3] Pileup subtraction schemes to be used at the trigger level are still under discussion in the technical design report of the trigger and data acquisition systems.

pileup event density and individual jet area, as detailed in Ref. [9]. This method does not rely on tracking information, and it could be implemented in the CaloGlobal system if the algorithms that derive such quantities are sufficiently fast, since the full event is available within FPGAs. However, the jet-area correction is not optimal in the forward region, due to the coarser segmentation of the calorimeter that prevents a precise calculation of the pileup event density for $|\eta| > 2$, and due to the increased sensitivity of the forward calorimeter signals to out-of-time pileup. An offset correction, employing $\langle\mu\rangle$ information from HGTD, would therefore be beneficial not only to restore stable jet performance in presence of pileup for forward jets, but also to the performance of the full η range. Such a pileup correction scheme will be investigated on the timeline of the technical design report.

3.4 Impact on example physics analyses

The physics performance improvements enabled by the HGTD can enhance the physics potential of ATLAS in several ways:

- The improved suppression of pileup jets is particularly important for searches for or measurements of VBF processes, which produce forward dijet pairs with large invariant masses. Additional forward jets mimicking the VBF topology increase the background from processes like Z+jets. Searches for heavy Higgs bosons produced via VBF are particularly affected by forward pileup jets because the VBF jets are produced at very large rapidity and the small cross section of the process requires high efficiency for low-p_{T} forward jets for which effective pileup suppression is critical.

- The improved b-tagging performance in the forward region can benefit physics analyses with forward b-quarks in the final state and in which the dominant backgrounds do not contain a large fraction of b-quarks in the forward region. Additionally, improved b-tagging can increase the rejection of the $t\bar{t}$ background in measurements of and searches for Higgs bosons produced via VBF.

- The improved lepton efficiency can enhance the precision of important Standard Model measurements at high luminosity that require forward leptons, such as the measurement of the weak mixing angle.

- The capability of the HGTD to assign a time to nearly all vertices can enable the reconstruction of masses of long-lived particles that decay within the HGTD acceptance. For any new massive particle that lives long enough to reach the HGTD, estimates of the increased ionisation energy loss and time-of-flight expected for a particle with $v < c$ could help identify them.

- Improvements in the luminosity accuracy and added trigger capabilities can further enhance the physics potential of many physics analyses at the HL-LHC.

While the HGTD is expected to bring improvements to a broad range of physics analyses, this section illustrates three cases: measurement of VBF $H\rightarrow WW^*$, $tH(\rightarrow b\bar{b})$ and the improvement of $\sin^2\theta_W$. The studies presented here are not exhaustive and the impact of the HGTD is being studied in several other physics analyses. They have been performed using the smearing functions mentioned before, following the recommendations for upgrade studies.

3.4.1 VBF $H\rightarrow WW^*$

High-precision measurements of the Higgs sector are one of the primary physics goals of the HL-LHC. VBF Higgs boson production can be computed with small theoretical uncertainties and is therefore a good channel for measuring the couplings between the Higgs boson and electroweak gauge bosons. The forward jet topology is a distinct feature which can be used to separate signal processes from many backgrounds. The precision of the VBF $H\rightarrow WW^*$ signal strength of $\mu = 1.27^{+0.44}_{-0.40}(\text{stat.})^{+0.30}_{-0.21}(\text{syst.})$ [10] was obtained from LHC Run-1 data at $\sqrt{s} = 7$ TeV and 8 TeV using a boosted decision tree (BDT). Increased pileup poses a challenge to the reconstruction of forward jets, and VBF final states are particularly sensitive to the precision with which jet-to-vertex association can be done in the forward region.

The object and event selection closely follows the selection used in Ref. [11]. The analysis requires electrons and muons to be isolated and have $p_{\text{T}} > 15$ GeV. Jets are selected with $p_{\text{T}} > 50$ GeV and must be identified as hard-scatter jets after passing pileup-jet suppression criteria. A veto for b-jets is also applied. Relative to the selection in the referenced result, the operating point for the veto of b-tagged jets is changed from 70% to 85% efficiency. The $E_{\text{T}}^{\text{miss}}$ is required to be larger than 20 GeV. The two leading jets are required to be in different hemispheres, each satisfy $|\eta_j| > 2.0$, and have an invariant mass $m_{\text{jj}} > 1250$ GeV. No jets with $p_{\text{T}} > 30$ GeV and both leptons are required to be inside of the η window between the two leading jets. The event yields are presented in Table 3.1.

N_{VBF}	N_{bkg}	N_{ggF}	N_{WW}	N_{VV}	$N_{t\bar{t}}$	N_t	$N_{Z/\gamma^*+\text{jets}}$	$N_{W+\text{jets}}$
203	280	39	29	7	146	25	34	0

Table 3.1: Expected signal and background yields after all selection requirements using the ITk, assuming 3 ab^{-1} of integrated luminosity and $\langle\mu\rangle = 200$. The background yields are summed together in the column labelled N_{bkg}.

The uncertainty on the signal strength (Δ_μ) is shown in Table 3.2, with the full, one-half, and none of the theoretical uncertainties for gluon-gluon fusion and VBF Higgs boson production from Ref. [11].

The improved pileup mitigation that HGTD enables is propagated to all affected physics objects. The impact on Δ_μ is shown in Table 3.3. The VBF $H\rightarrow WW^*$ analysis becomes more sensitive for higher pileup-jet rejection, so the enhanced pileup-jet reduction of roughly

	Signal unc.		
	Full	1/2	None
Δ_μ	0.16	0.13	0.13

Table 3.2: The expected Δ_μ without the HGTD is shown considering the same, half, and none of the theoretical systematic uncertainties on the VBF and ggF Higgs-boson production taken from Ref. [11].

	Δ_μ	% Improvement
ITk only	0.130	-
ITk + HGTD ($2.4 < |\eta| < 4.0$)	0.123	5%

Table 3.3: The relative improvement in Δ_μ for different η-coverage scenarios of timing measurements with 30 ps resolution.

a factor of 3 leads to an improvement of the analysis sensitivity. A full $|\eta| > 0$ timing acceptance improves the Δ_μ by around 7% whereas for the nominal HGTD acceptance, $|\eta| > 2.4$, the improvement is around 5%.

A multivariate analysis is also performed using a BDT including VBF topology variables. In addition, the lepton centrality and the $\sum m_{\ell j}$ variables from Ref. [12] are included in the training, which is done before the $p_{\mathrm{T}}^{\mathrm{tot}} < 20$ GeV selection is applied[4]. After the training, the $m_{\mathrm{jj}} > 500$ GeV is applied. The output of the BDT distribution is divided in bins with around 80 signal events per bin, which was found to be optimal. The resulting BDT distribution after including the HGTD is shown in Figure 3.10. The pileup-jet efficiency of 2% is found to give the smallest uncertainty on the Higgs production signal strength.

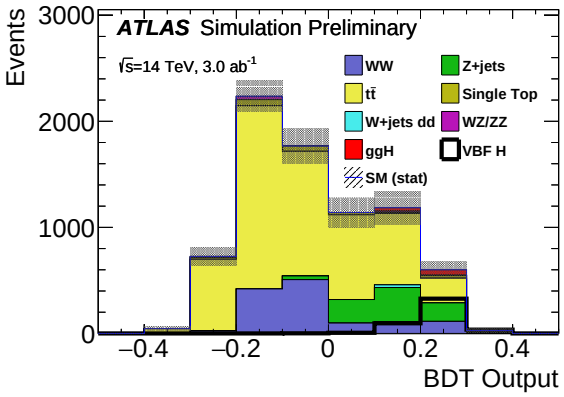


Figure 3.10: BDT score distribution when incorporating the HGTD.

[4] The $p_{\mathrm{T}}^{\mathrm{tot}}$ variable is defined as the magnitude of the vectorial sum $\mathbf{p}_{\mathrm{T}}^{l_1} + \mathbf{p}_{\mathrm{T}}^{l_1} + \mathbf{E}_{\mathrm{T}}^{\mathrm{miss}} + \sum \mathbf{p}_{\mathrm{T}}^{\mathrm{jets}}$

The event and background yields are shown in Table 3.4. The addition of the HGTD reduces the total background in the most sensitive BDT bin by a factor of 43%. Most of the background reduction comes from increased $t\bar{t}$ rejection.

Detector scenario	N_{VBF}	N_{bkg}	N_{ggF}	N_{WW}	N_{VV}	$N_{t\bar{t}}$	N_t	$N_{Z/\gamma^*+\text{jets}}$	$N_{W+\text{jets}}$
ITk	80	65	19	15	0	21	0	10	0
ITk + HGTD	80	37	19	4	0	5	0	10	0

Table 3.4: The signal and background yields are shown for the most sensitive BDT bin for different scenarios.

The uncertainty on the Higgs production signal strength is computed using the four bins with the highest significance added together assuming uncorrelated background uncertainties as the analysis is mostly statistically limited. Without the use of the HGTD, a Δ_μ of 0.096 is expected. The impact of the HGTD leads to an improvement of about 8%, with $\Delta_\mu = 0.088$. About 3% of this is due to the improved pileup-jet rejection; the rest comes from reducing the top background with better b-tagging.

In summary, an improvement of the order of 8% can be achieved in the BDT-based measurement of VBF-produced $H \to WW^*$ through including the HGTD.

3.4.2 Forward b-jets and measurements of tH production

Improved b-tagging in the forward region can benefit physics analyses characterised by the presence of forward b-jets. One example, considered in this section, is the $tH \to b\bar{b}$ final state.

A measurement of tH production is the only direct probe of the sign of the top-Yukawa coupling. The integrated luminosities produced by the LHC so far do not give sensitivity to this parameter, but determining it is an important goal for the HL-LHC physics program. In the Standard Model (SM), the interference between a positively signed top-Yukawa coupling and the coupling between Higgs and W bosons is destructive, resulting in a small expected tH production cross section. If the sign is negative, the interference would become constructive and the cross section for tH would increase by a factor of 10 relative to the SM process, while the $t\bar{t}H$ cross section would remain unchanged. Furthermore, an improved significance of this signal would improve the measurement on the strength of the top-Yukawa coupling, as the $t\bar{t}H$ measurement signal region is complementary to tH. The diagrams contributing to tH are shown in Figure 3.11. Signal regions are defined to contain events with one lepton and four or five jets, of which at least two are b-tagged. One of the non-b-tagged jets should have $|\eta| > 2.4$. The sum of the transverse momenta of the jets (H_T) must be at least 300 GeV. The pseudorapidity of the most forward jet is the most important variable to separate the tH signal from the $t\bar{t}$ and $t\bar{t}H$ backgrounds which produce more central jets. The distributions of the most forward jet in events with three b-tagged

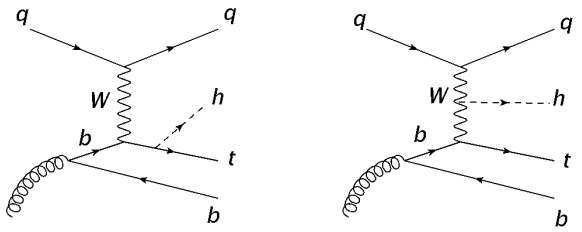


Figure 3.11: Contributing diagrams to tH production with the top-Yukawa coupling (left) and the W to Higgs-boson coupling (right). In both cases, a forward jet is expected, with additionally a gluon splitting to $b\bar{b}$ pair producing a b-jet in the forward region in 25% of the events.

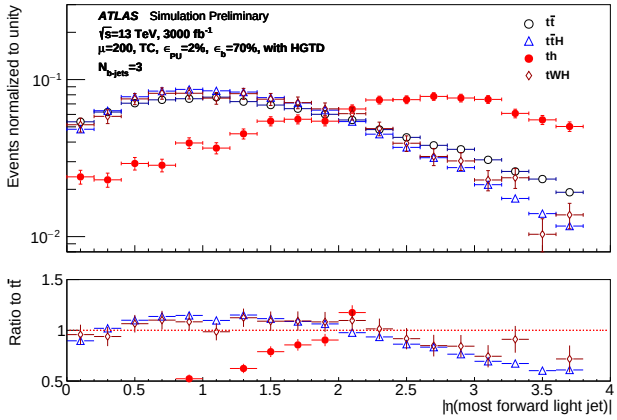


Figure 3.12: Distribution of $|\eta|$ for the most forward light jet in the three b-tag category for tH with $H \to b\bar{b}$ and the backgrounds from $t\bar{t}$ and $t\bar{t}H$ production.

jets can be found in Figure 3.12. A forward b-jet in the HGTD acceptance is present in 25% of the events. The relative gain from the improved light-jet rejection due to the HGTD is estimated using the MV1 algorithm with a working point of 70% efficiency for b-jets. Using a log-likelihood ratio binned in η of the light forward jet, the sensitivity to tH is improved by 11% as shown in Table 3.5.

Scenario	Signal significance
ITk	1.28σ
ITk + HGTD	1.42σ

Table 3.5: Expected (statistical only) signal significance of $tH \to b\bar{b}$ using ITk or ITk + HGTD.

3.4.3 Measurement of $\sin^2\theta_{\text{eff}}$

In the Standard Model (SM), the Z boson couplings differ for left- and right-handed fermions due to the mixing between the neutral states associated to the $U(1)$ and $SU(2)$ gauge

groups. The difference leads to an asymmetry in the angular distribution of positively and negatively charged leptons produced in Z boson decays and depends on the weak mixing angle, $\sin^2\theta_{\text{eff}}$ [13].

Experimentally, this asymmetry can be expressed as simply as

$$A_{\text{FB}} = \frac{N(\cos\theta^* > 0) - N(\cos\theta^* < 0)}{N(\cos\theta^* > 0) + N(\cos\theta^* < 0)},$$

where θ^* is the angle between the negative lepton and the quark in the Collins-Soper frame [14] of the dilepton system. This asymmetry is enhanced by Z/γ^* interference and exhibits significant dependence on the dilepton mass.

The weak mixing angle is one of the fundamental parameters of the SM. Several measurements of $\sin^2\theta_{\text{eff}}$ have been made at previous and current colliders, and the current world average is dominated by the combination of measurements at LEP and at SLD, which gives $\sin^2\theta_{\text{eff}} = 0.231530 \pm 16 \times 10^{-5}$. However, the two most precise measurements differ by over 3σ [13].

At HL-LHC, the best sensitivity to $\sin^2\theta_{\text{eff}}$ is at high Z rapidity when at least one lepton is present in the forward region [15]. Only Z bosons decaying to electrons are considered in this analysis since this final state provides the best experimental precision within the largest acceptance.

The fiducial acceptance of $Z/\gamma^* \to ee$ events is split into three independent channels depending on the electron $|\eta|$: CC, CF and FF, where C represents an electron reconstructed in the central region ($|\eta| < 2.47$) and F represents an electron reconstructed in the forward region ($2.5 < |\eta| < 4.2$). Both electrons are required to have $p_{\text{T}} > 25$ GeV. The invariant mass of the electron pair is required to be loosely consistent with the Z boson mass, $60 < m_{\ell\ell} < 200$ GeV, and the events are further categorised in 10 equal-size bins in absolute dilepton rapidity up to $|y_{ee}| = 4.0$.

The contribution of jets misidentified as electrons is suppressed using a tight electron identification and a track isolation requirement. In the forward region, the timing information provided by the HGTD is used to improve the electron isolation by rejecting additional tracks from interactions close in space, but separated in time from the hard-scatter vertex. The purity of the candidate sample is determined with simulation, and is found to be greater than 99% in the CC channel, between 90 and 98% in CF, and between 60 and 90% in the FF channel. The signal significance with HGTD is up to 20% higher with respect to the case of ITk only in the CF channel.

A_{FB} is calculated from the selected electron pairs, and unfolded to correct for detector effects and migrations in $m_{\ell\ell}$ and $|y_{ee}|$ bins. In the CF and FF channels, migrations in the $m_{\ell\ell}$ are up to 50 and 60% respectively. Various sources of uncertainty are considered. Those associated with background are mostly relevant in the CF and FF channels; they are estimated to be 5% on the background yield and considered uncorrelated for each $m_{\ell\ell}$ and $|y_{ee}|$ bin.

Significant uncertainties arise from the limited knowledge of the momentum scale and resolution of the electrons. Following Reference [16], in order to account for possible non-linearity in the energy scale of electrons reconstructed in the central (forward) region, a systematic of 0.5% (0.7%) is considered for electrons with $E_{\mathrm{T}} < 55$ GeV and up to 1.5% (2.1%) for $E_{\mathrm{T}} > 100$ GeV.

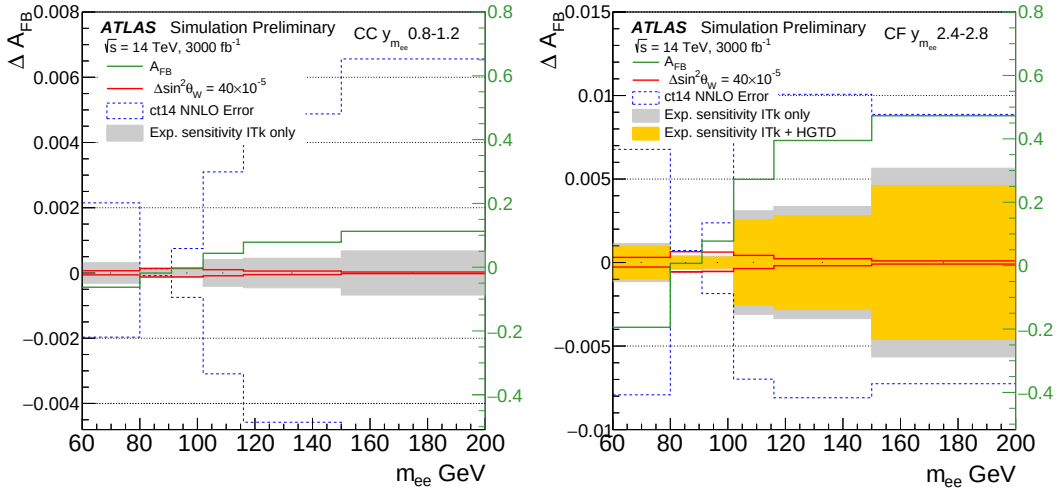
The expected sensitivity to particle level A_{FB} as a function of m_{ee} is shown in green in Figure 3.13 for each channel for a chosen rapidity bin. As expected, the largest asymmetry is observed in the CF channel. The extraction of $\sin^2\theta_{\mathrm{eff}}$ is done by minimising the χ^2 value between particle-level A_{FB} distributions with different weak mixing angle hypotheses, at LO in QCD, with an NNLO CT14 parton distribution function (PDF). As shown in Figure 3.13, the imperfect knowledge of the PDF results in sizeable uncertainties in A_{FB}, in particular in regions where the absolute value of the asymmetry is large, i.e. at high and low $m_{\ell\ell}$. On the contrary, near the Z boson mass peak, the effect of varying $\sin^2\theta_{\mathrm{eff}}$ is maximal, while being significantly smaller at high and low masses. Thus, in this projection a global fit is performed where $\sin^2\theta_{\mathrm{eff}}$ is extracted while constraining at the same time the PDF uncertainties [15]. With this analysis, the expected sensitivities of the extraction of $\sin^2\theta_{\mathrm{eff}}$ are respectively 25×10^{-5}, 21×10^{-5} and 40×10^{-5} for the CC, CF and FF channels The uncertainty of the results is dominated by the currently limited knowledge of the PDFs. When considering only the experimental uncertainties, including the HGTD in the ATLAS forward region brings a 13% improvement on the $\sin^2\theta_{\mathrm{eff}}$ sensitivity in the CF channel. Combining the three channels together, the expected sensitivity reaches a precision of $\Delta\sin^2\theta_{\mathrm{eff}} = 18 \times 10^{-5} \pm 16 \times 10^{-5}$ (PDF) $\pm 9 \times 10^{-5}$ (exp.), which exceeds the precision achieved in all previous single-experiment results so far.

3.5 Outlook and path towards the TDR

With a timing resolution of 30 ps per track, the HGTD provides important supplementary information for mitigating pileup effects. The contamination of low-p_{T} forward tracks associated to the primary vertex can be reduced by adding requirements on z_0 and on the compatibility of the time measurements of the associated tracks in the HGTD.

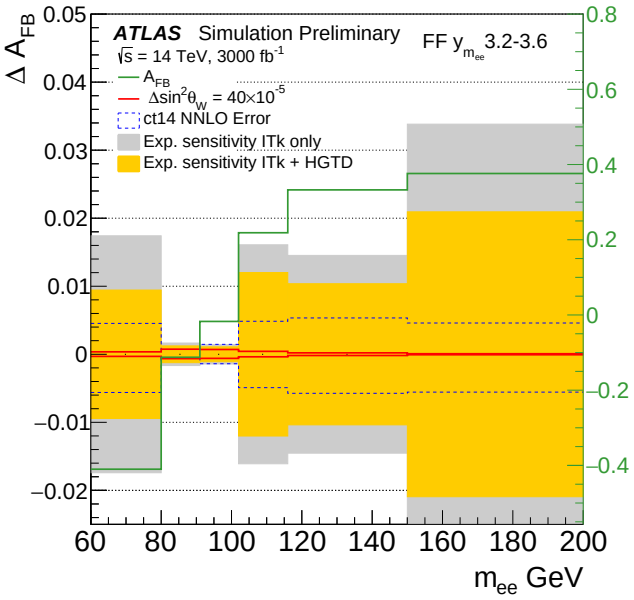
With the expected timing precision, rejecting pileup tracks with the $R_{p_{\mathrm{T}}}$ algorithm presented in Section 3.1.2 improves the identification of pileup jets by up to a factor of 4. The rejection of pileup tracks using timing information also improves the light-jet rejection at 70% b-tagging efficiency by a factor of 1.5. The electron isolation efficiency is increased by about 14%.

These performance improvements translate into an 8% improvement in the sensitivity of the measurement of VBF $H \to WW^*$ process. This is mainly thanks to the better b-jet veto and pileup-jet suppression in the forward region provided by the HGTD. An analysis targeting tH production with a final state containing forward b-jets shows up to 11% increase



(a) Central-central (CC)

(b) Central-forward (CF)



(c) Forward-forward (FF)

Figure 3.13: Distribution of ΔA_{FB} as a function of mass for the CC, CF and FF channels. The filled bands correspond to the experimental sensitivity with and without the HGTD. The solid red lines correspond to a variations of $\sin^2\theta_{\mathrm{eff}}$ corresponding to 40×10^{-5}. The dashed blue lines illustrate the total error from CT14 NNLO PDF. Overlaid green line shows the particle-level A_{FB} distribution.

in sensitivity due to better b-jet tagging in the forward region. The effect of the improvement of the electron identification performance in the measurement of the weak mixing angle, $\sin^2\theta_{\text{eff}}$, has been investigated. The most sensitive events for this measurement are the ones in which a Z-boson decays to one electron in the central region and another electron in the forward region, while the dominant systematic uncertainty comes from the limited knowledge of the PDFs. An improvement of 11% on the experimental uncertainty is obtained when adding the HGTD to the analysis. Potentially larger improvements on these analyses, as well as in other final states that benefit from improved pileup-jet rejection, b-jet tagging and lepton performance in the forward region, are currently being investigated.

The results presented in this section have been obtained using full simulation and reconstruction as well as a mixture of full and fast simulation. The study of more sophisticated pattern recognition algorithms might improve the capabilities of ATLAS even further when the timing information from the HGTD is used in a combined reconstruction. In addition to the analyses described in some detail above, these capabilities can give improvements in several other measurements and searches for new physics.

Regarding object reconstruction, the HGTD can refine the track selection used in the calculation of the missing transverse momentum. Studies are ongoing to evaluate the impact on the resolution and the possible reduction of tails of the $E_{\text{T}}^{\text{miss}}$ distribution, induced by tracks from pileup interactions. The improvements in the performance of jet reconstruction and the physics analyses that use jets were determined assuming an ideal vertex t_0 determination. The impact of using a realistic t_0 determination efficiency and precision is a high priority for the next steps and the TDR.

A more accurate luminosity determination, as well as potential improved jet and $E_{\text{T}}^{\text{miss}}$ trigger capabilities, can further enhance the precision and sensitivity of a broad range of physics analyses.

The MBTS detector has been used for measurements of the inelastic pp cross section at $\sqrt{s} = 7$ and 13 TeV [17, 18]. Despite the coarse segmentation of the MBTS, the distribution of the number of hits in the scintillator provides very valuable information for discriminating between different generators to improve the modelling of inelastic interactions. In the sample used for these measurements, the detector response was saturated in 90% of the events. The high granularity of the HGTD would therefore allow the level of activity for the bulk of the sample to be resolved, enabling significant improvements in the modelling of minimum-bias interactions. The same studies could also be done using tracks reconstructed by the ITk, but possibly the HGTD could give access to a lower-p_{T} region. The importance of accurate modelling of such processes increases linearly with pileup, and any per-event improvement is multiplied by a factor of 200 for high-$\langle\mu\rangle$ at the HL-LHC. A possible positive consequence of this is the improvement of the $E_{\text{T}}^{\text{miss}}$ modelling.

New long-lived particles (LLPs) are predicted by a range of beyond-SM models, including some that are particularly well-motivated from a Dark Matter perspective. Accurate timing and ionisation-energy loss measurements are key observables from heavy LLPs

traversing the detector, such as e.g. *R*-hadrons and long-lived sleptons in Split SUSY and Gauge-Mediated Supersymmetry Breaking scenarios, respectively. Though the acceptance of the HGTD is limited to the forward region and many LLPs are predicted to be produced primarily in the central η region, some improvement in sensitivity could be gained if the HGTD could be exploited in these searches. Studies of LLPs expected to give a signature primarily in the forward region, such as magnetic monopoles, will be carried out on the time scale of the TDR.

Finally, the timing capability of the HGTD is being investigated for the purpose of studying machine-induced non-collision background processes such as beam-gas interactions and beam-halo activity.

4 Detector design

This section describes the layout and design of the HGTD. The detector is based on LGAD sensors, a novel type of silicon sensor that provides the required timing resolution of 30-50 ps per hit in a compact and radiation hard format. A sensor is segmented into arrays of pixels or pads yielding a granularity high enough to match the requirements. The sensors are then bump-bonded to readout chips and connected to flexible circuits to construct the modules. These modules are arranged and mounted onto thin intermediate support plates, larger half-disk shaped for $R < 320\,\text{mm}$ and narrow rectangular *staves* for larger radii. The modules located in a row along the direction of the routing of the flex cables are considered part of a so-called *readout row*. The placement and spacing of the modules along the radial direction are optimised in such a way that a charged particle passing through will result in at least three (two) hits for $R < 320\,\text{mm}$ ($R > 320\,\text{mm}$) on average. The larger number of hits in the inner region, accomplished by increasing the overlap of the modules on the two sides of the cooling disk, is necessary to maintain the target per-track time resolution after irradiation. The cooling disks are divided into two halves to simplify installation. The active area of the detector spans the forward region corresponding to $2.4 < |\eta| < 4.0$, where it helps to restore the object reconstruction and identification performance to match that achieved in the central region, as presented in Section 3.

The first part of this section describes the different studies and considerations that led to the optimised design presented in this document. Then the assembly of the modules and detector layers is described. The last two subsections of the section are dedicated to the detailed description of the LGAD sensors and the readout electronics.

4.1 Design optimisation

The studies presented in this section were performed using the full simulation and reconstruction described in Section 3.

The first step of the detector optimisation is the definition of the pixel size, which is driven by the electronics and the occupancy, i.e., the probability of having a signal in a pixel. The smaller the surface of the pixel, the lower the electronics noise will be. The occupancy also calls for a small pixel size to avoid pixels having more than one hit and thus potentially losing the timing information. On the other hand a small pixel size increases the number of channels to be instrumented and introduces inefficiencies due to inter-pixel dead zones.

Although the probability to have a hit in a pixel decreases as a function of the distance from the beam axis, a fixed pixel size was chosen for simplicity. The choice was driven by the target of having a maximal occupancy at the lowest instrumented radius (120 mm) of 10%. This ensures a low double-hit probability (below 10%). The timing information for a particle from the hard-scatter vertex is only lost for 5% of the cases when a particle originating from a pileup vertex hits the pixel first.

Figure 4.1 shows the occupancy expected for a pileup of $\langle\mu\rangle = 200$, defined as the percentage of pixels of the HGTD registering a hit, for different pixel sizes. As expected, the occupancy decreases as a function of the radius and increases as a function of the pixel size. A slight increase is observed when moving outwards from the innermost to the outermost layer, primarily due to the increased probability of initiating showers due to hadronic interactions as more material is traversed. At the smallest radius the occupancy is 6% for pixel sizes of 1×1 mm^2, and 20% for 2×2 mm^2. By interpolating between these two results it is possible to see that a pixel size of 1.3×1.3 mm^2 gives an occupancy of 10%, which fulfils the requirements and is therefore chosen.

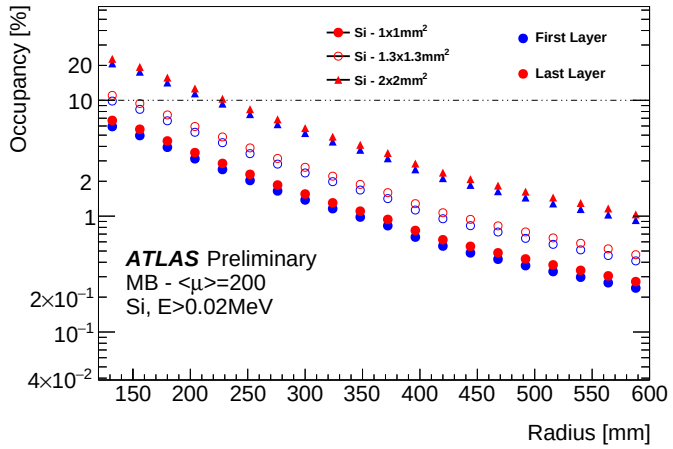
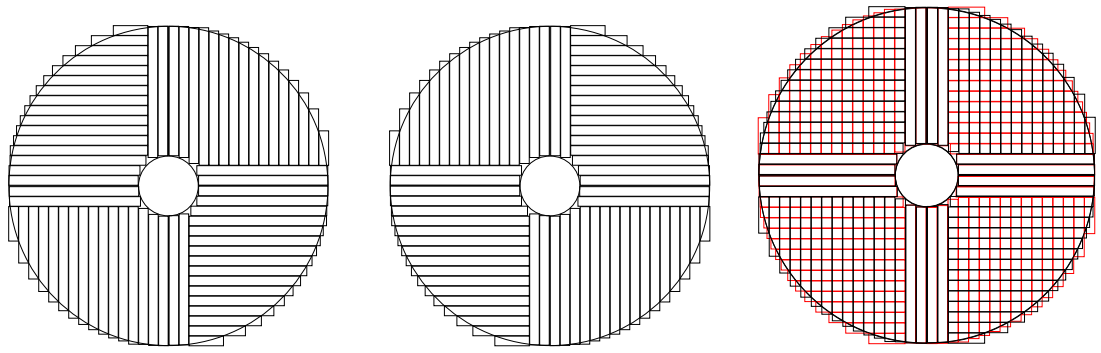


Figure 4.1: The occupancy as a function of the radius for different pixel sizes at a pileup of $\langle\mu\rangle = 200$. The occupancy for pixels of 1.3×1.3 mm^2 is the result of an interpolation.

The detector geometry was optimised in two steps. First the layout of modules for the two cooling plates in each endcap was defined by maximising the coverage and minimising the effect of non-instrumented regions due to mechanical tolerances. In the second step the spacing between modules was optimised to achieve a timing resolution of about 30 ps per track. In these studies a pixel size of 1×1 mm^2 was used, implemented at analysis level by merging the 0.5×0.5 mm^2 pixels used in the full simulation.

The readout rows are defined as the sets of modules whose flex cables are guided together towards larger radii to the peripheral on-detector electronics. Their disposition for the first and second cooling disks is shown as rectangles in Figure 4.2. The active width of a module is 39 mm which limits how well the area near the circular opening at $R = 120$ mm can be

covered. For $R > 150$ mm the coverage is complete. The maximum length of the readout rows is limited by the manufacturing capabilities for the flexible circuits used for the data transmission. The non-instrumented zone is 1 mm between two readout rows and 3 mm between each half disk to account for mechanical tolerances. The effective width of the readout rows is therefore 40 mm. These constraints lead to the helix structure shown in Figure 4.2(a) for the first cooling disk. The second disk, shown in Figure 4.2(b) is defined as a mirror geometry with respect to the first disk. Therefore, as shown in Figure 4.2(c), with the exception of four readout rows per quadrant, the non-instrumented zones of the two disks do not overlap.



(a) First cooling disk (b) Second cooling disk (c) Overlay

Figure 4.2: The orientation of the readout rows for the first and second cooling plates separately, and the overlay of both.

As demonstrated in Section 3 a timing resolution of about 30 ps per track should be provided by the HGTD. The geometry of the detector has been optimised to obtain a reasonably flat timing resolution as function of η. Due to radiation damage, the timing resolution of the detector will be degraded as the integrated luminosity delivered by the LHC increases. This radiation depends strongly on R, with higher radiation closer to the beam axis. Because of this, the geometry of the HGTD is designed such that at $R < 320$ mm on average three hits are obtained for a charged particle, whereas at $R > 320$ mm an average of two hits are expected to be associated to a track.

Each disk of the HGTD is double-sided, i.e., the modules with sensors and on-detector electronics are mounted on the front and back sides of the cooling plate. As illustrated in Figure 4.3, the modules on the two sides of a disk are arranged to overlap so that the number of hits exceeds the number of disks. A study using full simulation was performed to determine the optimal overlap between modules in $R < 320$ mm to achieve the required timing resolution. The overlap was varied between 20% and 80%, limited by the need for sufficient space between the modules to allow reading out the signals. For $R > 320$ mm, an overlap of 20% was found to be enough.

The HGTD acceptance is defined as the surface covered by the HGTD between a radius

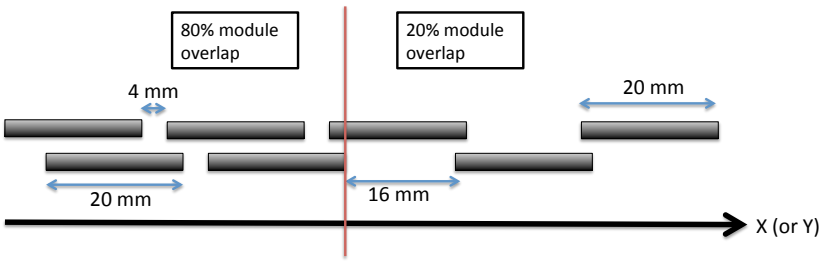


Figure 4.3: Schematic drawing showing the overlap between the modules on the front and back of a cooling disk.

of 120 mm and 640 mm (as mentioned earlier the simulation is only implemented up to 600 mm). The hit efficiency is studied using single-muon events with $p_{\mathrm{T}} = 45\,\mathrm{GeV}$ and flat distributions of polar and azimuthal angles. The inefficiency due to non-instrumented zones (e.g. areas not covered by modules) is defined as the fraction of muons that have no hits reconstructed in the HGTD, and was found to be 0.7% with the described layout. This does not take into account the inactive inter-pixel areas on the sensors themselves.

Figure 4.4 shows the average number of hits associated to a track. The results are summarised in Table 4.1 for an inactive inter-pixel region of 50 µm. The normalisation is performed separately in each region with respect to the surface covered by the HGTD. Over 81% of the extrapolated muon tracks have at least two matched hits in the HGTD. For at most 3% of the muons, no hits are registered. The inefficiency is mainly due to the track-matching efficiency of 98% which is discussed in Section 3.1.

	$R < 320$ mm ($\eta > 3.08$)	**$R > 320$ mm** ($\eta < 3.08$)
$N_{\mathrm{hits}} \geq 2$	93%	81%
$N_{\mathrm{hits}} = 0$	1.9%	3%
$\langle N_{\mathrm{hits}} \rangle$	2.9	2.0

Table 4.1: The percentage of tracks with at least 2 hits, the percentage of tracks escaping undetected and the average number of hits for muons with a p_{T} of 45 GeV are shown for the baseline detector layout. The values are given for inactive inter-pixel zones of 50 µm and include the effect of non-instrumented zones and the track-matching efficiency. The normalisation is the surface covered by the HGTD in each region separately.

The average number of hits is shown as a function of the radial distance from the beam axis in Figure 4.5. The non-instrumented zones and the inter-pixel dead zones of 50 µm are taken into account. For an overlap of 20% between the modules the average number of hits is about two. Increasing the overlap to 80% for $R < 320$ mm results in an average hit multiplicity of about three in this region. The resulting layout gives a relatively flat timing

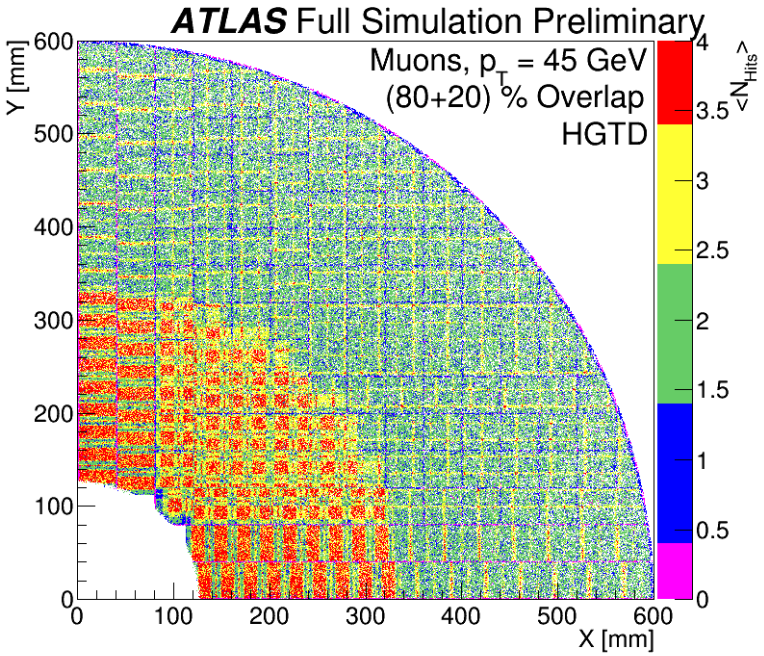


Figure 4.4: The number of hits as function of the position in the HGTD is shown for an overlap of 80% at $R < 320$ mm and 20% at larger radii.

resolution as a function of radius, also after the detector has been exposed to the expected radiation dose.

Four timing performance scenarios are defined: *Initial*, *Intermediate*, *Final* and *Worst Case*, shown in Figure 4.6. The first three scenarios correspond to the performance expected at the very beginning, after half of the delivered luminosity, and at the end of the HL-LHC lifetime (4000 fb^{-1}). The per-hit timing resolution of the sensors is expected to be 30 ps at the start of the HL-LHC, independent of the radius. As the integrated luminosity increases, the damage to the sensors caused by radiation will deteriorate their timing resolution inducing a dependence on the radial distance from the beam axis. It is planned to replace the inner part ($R < 320$ mm) of the HGTD after half of the HL-LHC programme, and therefore the timing resolution in this region for the *Intermediate* and *Final* scenarios are identical within statistical fluctuations. If the sensors of the inner ring were not replaced, the timing resolution of the sensors at a radius of 120 mm is expected to be degraded to the order of 50 ps. The *Worst Case* scenario assumes an additional degradation of approximately 20% on top of this for all radii, yielding a flat and overly pessimistic timing performance. The per-hit resolution curves in Figure 4.6(a) include a contribution from the electronics corresponding to 25 ps which has been added in quadrature to the sensor resolution values discussed above.

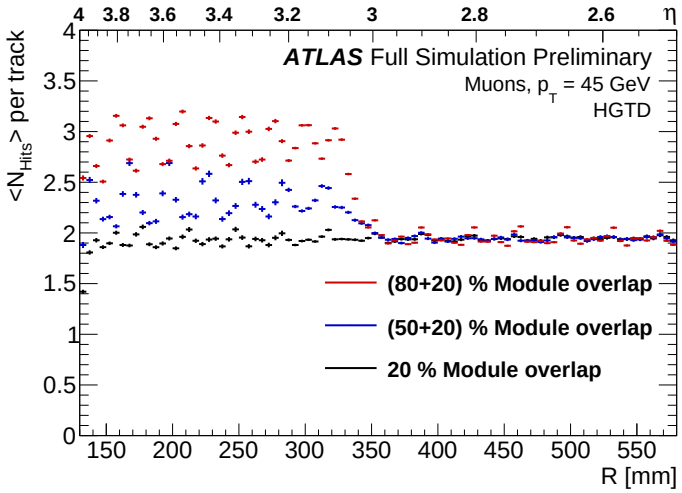
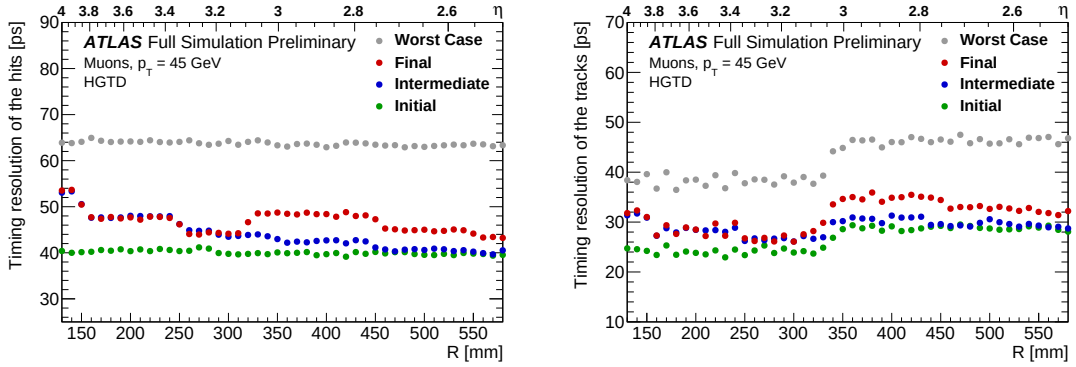


Figure 4.5: The average hit multiplicity as function of the radius (and pseudo-rapidity) for a module overlap of 20% in the outer region of the HGTD, and overlaps of 20%, 50% and 80% for the inner region.

The resulting timing resolution for tracks is shown in Figure 4.6(b) for the four scenarios. At radii lower than 320 mm ($\eta \approx 3.1$), the increased number of hits compensates the effects of radiation damage so that the resulting timing resolution is fairly independent of the radius. The per-hit resolution was implemented in full simulation. The reconstructed timing resolution for tracks shown here was determined using the single-muon events by comparing the reconstructed hit or track time to the expected time from the truth information. The distribution is dominantly Gaussian with negligible tails.



(a) Resolution per hit.

(b) Resolution per track.

Figure 4.6: The HGTD timing resolution is shown as function of the radius for four timing scenarios. The sensor resolution and the contribution from the electronics are considered, added in quadrature.

4.2 Module and layer design and assembly

The HGTD detector concept is based on individual planar layers of LGAD sensors to be fixed in front of both endcap calorimeter cryostats with active elements between 3435 and 3485 mm in z. Each layer is an independent object built on a cooling plate support disk (discussed in Section 5), allowing for a modular design. On both sides of this cooling plate, individual identical modules of 20×40 mm^2 consisting of LGAD sensors, ASIC and flex circuits will be installed. A schematic drawing of the detector is shown in Figure 4.7. Groups of up to 19 modules constitute readout rows (see Section 4) which can be of different lengths. The longest readout row is 546 mm and defines the most difficult constraints for the mechanical assembly and the most stringent requirements for the flex cable characteristics. The module design is described in the next section, including the ASIC to sensor connection through bump-bonding and the design of the flex cable used to transmit the data to the peripheral on-detector electronics. In the two following sections the general detector layout with sensors, modules, layers and support structures is presented.

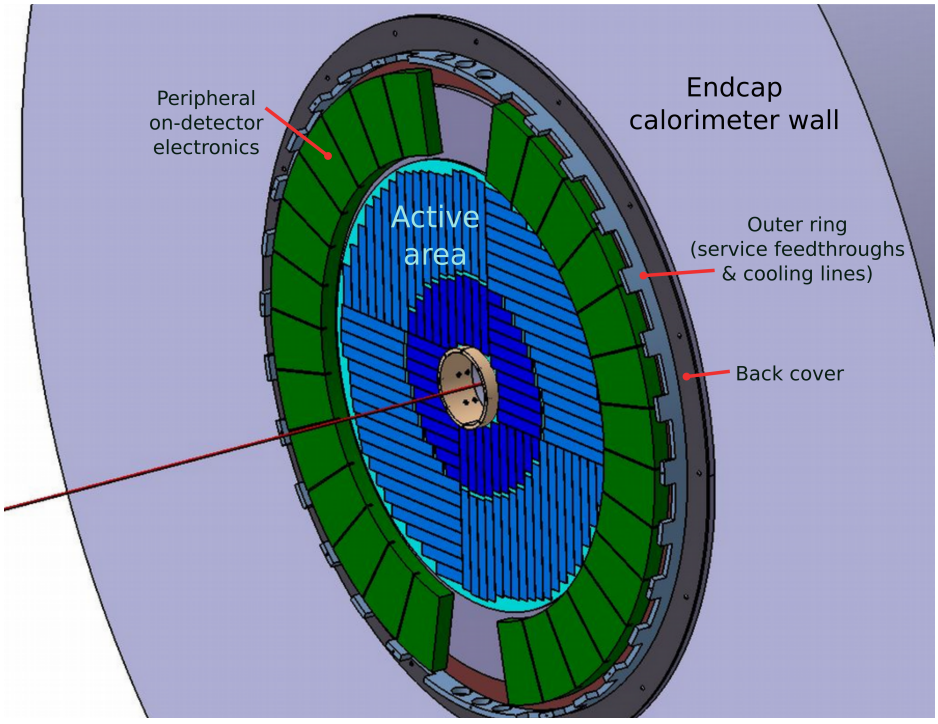


Figure 4.7: Illustration of the HGTD, showing the peripheral on-detector electronics in green and the layout of the readout rows, containing modules mounted on the inner half-disk support plates at $R < 320$ mm (dark blue), and on staves at larger radii (light blue).

4.2.1 Module design

Components and layout

The surface of a module is 20×40 mm^2 corresponding to a single LGAD sensor (see Section 4.3) with two ASICs (see Section 4.4.4) bump-bonded to it. This element is then glued with accurate positioning to the flex cable used to transfer the signals. ASIC signals and HV for the sensor will be connected by wire-bonding the flex cables to the module. Figure 4.8 shows three modules with the different components stacked in the z direction. The total thickness of a module is about 1 mm with the sensor, the ASIC and the flex cable contributing about 300 µm each. The needed space for each component, and in particular the curvature of the flex cable, is discussed in Section 4.2.3.

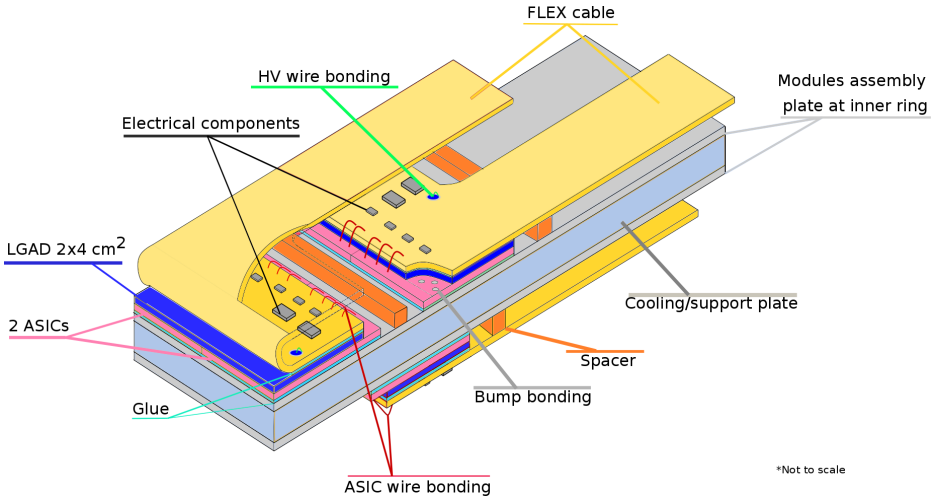


Figure 4.8: Schematic drawing of two adjacent modules on the top side and one on the bottom side of the cooling plate; the modules are mounted on thin support plates. The first flex cable is folded, while the others are straight.

ASIC-sensor interconnection

The interconnection of the sensor to the front-end chip is a critical procedure of the detector assembly process. Each sensor channel is DC-coupled to the corresponding readout channel on the ASIC through a small (typically 80 µm diameter) solder ball. The complete hybridisation process, called bump-bonding, consists of under-bump metallization (UBM)[1] (of sensor and ASIC pads, to prepare them for soldering), solder bump deposition (on the ASIC) and flip-chip. The R&D effort, presented below, is being carried out by dedicated groups within the HGTD community. For the full HGTD production phase, a combination of private companies and ATLAS institutions is foreseen to share the workload. Suitable

[1] Some investigations are in progress to evaluate the possibility to use Au bumps which will not necessitate UBM process

companies for the UBM and flip-chip processes have been identified and contacted, and first cost estimates are available.

In the hybridisation process, the aluminium pads of the sensor and readout chip are first covered with NiAu through an auto-catalytic chemical technique. The bumps are then deposited on the ASICs with a bump deposition machine that places SnAg (or SnPb) solder balls on the front-end pads and reflows them with an infrared laser system. The solder bumps are further reflowed in a dedicated machine in order to improve the placement and the shape uniformity of the bump balls. Flip-chip, the last step in the hybridisation process, is performed with a Süss Microtech bonder machine with a reflow arm that provides a 0.5 µm placement accuracy and 1 µm post-bond accuracy. During the bonding cycle the ASICs (with SnAg solder bumps) and the sensors are aligned, heated to 260 °C and pressed together lightly. After flip-chip the assemblies are reflown once again with formic acid.

First studies were performed on a 10×10 matrix of 1×1 mm^2 pixels in order to prepare for further tests with the ASIC prototype module. These preliminary tests confirmed that the critical steps of bump deposition and flip-chip can be conducted successfully with pixel pads 90 µm wide and bump balls of 80 µm diameter. In the following step, dummy samples that match mechanically the characteristics of the ASIC prototype modules were assembled obtaining excellent results with a bump strength of 60 g/bump. Altogether, these tests showed that a full assembly line is already available for the HGTD detector.

The first HGTD small-scale module prototypes using the first ASIC prototype (ALTIROC0_v1) and LGAD sensors were assembled in summer of 2017. Four assemblies were successfully produced following the same procedure used for the previous studies. The UBM of the diced chips and only partially diced sensors was done with thicknesses between 4 and 6 µm. After bump deposition, the chip solder joints were reflowed and then the flip-chip process with selected sensors was carried out. The four bump-bonding cycles were successful, and X-ray inspection indicated good connectivity of all the bump bonds.

Voltage distribution and signal readout

The flex cables supply the high voltage (HV) power needed for the bias voltage of the LGAD sensors, power to drive the ASICs and include the electrical links, or *e-links*, for data transmission, as well as high speed differential lines to transport the signals to the peripheral readout electronics. The signal lines needed for two ASICs are summarised in Table 4.2.

The geometry of the flex cables is defined by the geometry and dimensions of the HGTD, the LGADs and the ASICs. Their flexibility is given by the insulating support material (Kapton®) with which they are made. A four-layer design of the cable is needed to fulfil the requirements and it can be realised within a thickness of 300 µm. To reduce the total thickness of the stacked cables routed to the same peripheral electronics board, two L-shape geometries are proposed, with a layout where the signals are on the left side of the module and a specular version where the signals are on the right side (see Figure 4.9). The distance

between the innermost module and the start of the peripheral on-detector electronics is 630 mm, leading to a maximum length of around 700 mm needed for the flex cables.

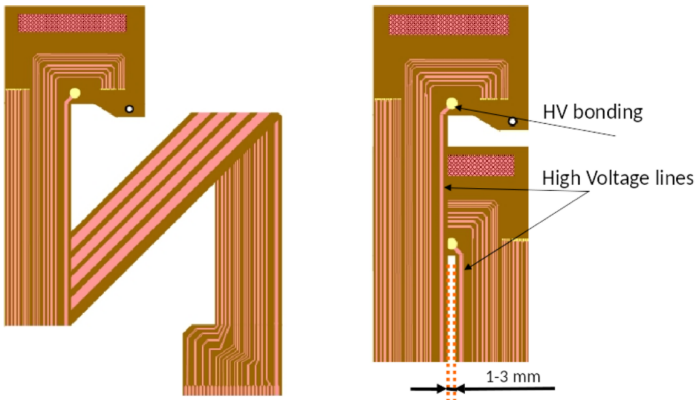


Figure 4.9: Left: Flex cable layout. Right: Sketch of two flex cables belonging to two contiguous modules. Clearance between HV lines is be considered. The bonding wires are placed in the centre-bottom part of the module.

Signal type	Signal name	Number of wires	Comments
HV	1 kV max.	2	Clearance
POWER	1x V_{vdda}, 1x V_{vddd}	2	Minimise voltage drop
GROUND		1 plane	Dedicated layer
Slow control	Data, ck, (opt. +rst, error)	2 to 4	I^2C link
Input clocks	320 MHz, Fast command e-link, (opt. 40 MHz(L1))	6 or 8	LVDS
Data out lines	Readout data (TOT,TOA,Lumi)	4 pairs	4 e-links differential SLVS.
ASIC reset	ASIC_rst	1	Digital

Table 4.2: Types of signals for two ASICs included in the flex cable design.

Each module is supplied by a separate HV line which will allow for adjusting the voltage value at smaller radii to minimise the deterioration induced by radiation damage (Figure 4.20). In practice two lines will be connected to a module to ensure redundancy if one is broken. A maximum HV of 1 kV is assumed. The HV lines in the flex cable design will be placed in one of the edges not to disturb the other signals and a clearance of 1–3 mm between two contiguous flex cables (see Figure 4.9) must be kept to avoid undesired effects such as corona or arcing. The bonding will be placed between the LGADs in order to facilitate the HV supply to the module. Having separate flex cables for HV and for all other signals, respectively, is still an open option.

Each set of signals has different characteristics, therefore, specific optimisations are needed. The resistance of both the power lines and ground plane must be as low as possible $< 80\,\text{m}\Omega$. The crosstalk must be studied in the case of the analog and digital signals, whose impedance will be 50 Ω. For the differential signals, the 100 Ω impedance must be controlled for the high-speed signal transmission (1.28 Gbit/s). The choice of the appropriate materials and the geometry of the tracks are crucial to meet these requirements.

A prototype of the longest flex cable with a representative set of lines of all required types is being designed together with a company that was identified as a potential partner for the final production. Loopback tests including a time domain analysis and a bit error rate test will be performed in the next months. About 10 identical cables will be produced both for redundancy and to test the behaviour of the single lines within a stack of cables. For the bias voltage line the addition of a coating for better insulation will be considered based on the results of these tests.

4.2.2 Module loading

Modules connected to the same peripheral electronics board belong to the same readout rows, aligned along the x or y direction. The longest rows contain 19 modules. Their geometry was optimised as shown in Figure 4.2. The modules will be pre-assembled and glued to a thin intermediate support plate which is then screwed to the cooling plate. At $R < 320\,\text{mm}$ the plate consists of half disks that can be replaced easily after half of the HL-LHC running time, while at larger radii each readout row has its own rectangular plate called a stave. The readout rows that include modules at radii both smaller and larger than 320 mm will therefore contain modules mounted on the inner half disk and on a stave that is assembled independently. Figure 4.10 shows a drawing of the modules assembled on the inner plate and the outer staves in one quadrant of sensors, i.e. one quarter of one side of a cooling plate.

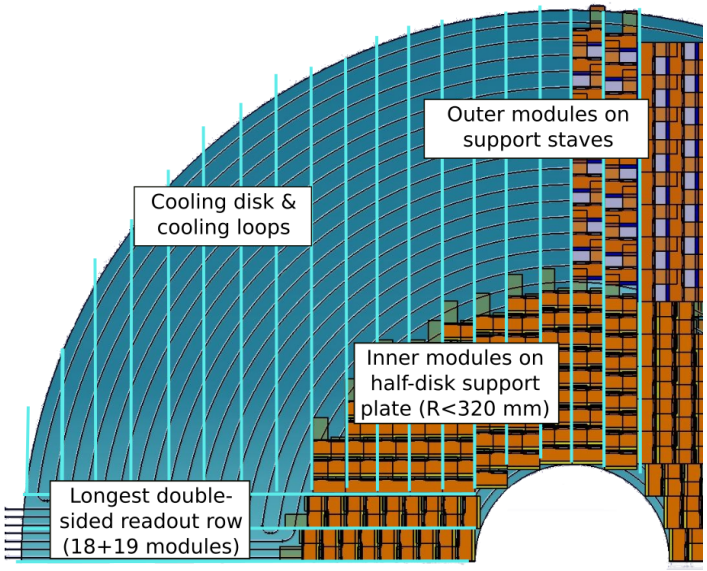


Figure 4.10: Drawing showing the assembly of the modules in one quadrant with cooling pipes visible. The modules at $R < 320\,\text{mm}$ are mounted on a half-disk support plate and positioned closer to each other, with an 80% overlap between modules on the front and back of the cooling plate. The modules at $R > 320\,\text{mm}$ are mounted on support staves with more space between them in the radial direction, yielding an overlap of 20%.

The overlap between the modules on either side of the cooling plate was optimised as shown in Figure 4.3: modules on the front and back of the cooling plate overlap by 80% in the inner region, while those assembled on staves in the outer region overlap by 20%. The innermost module of each readout row is rotated by 180 degrees such that the wire bonds face away from the first readout row of the adjacent quadrant or from the inner radius of the detector. Since the rotated sensors can be positioned flush with the perpendicular readout row of the adjacent quadrant, the non-instrumented area is minimised. To achieve this the flex cable corresponding to the first module needs to be folded backwards (see Figure 4.8). A bending diameter of 8 mm is expected to ensure the full functionality of the flex cable, while fitting well within the available space (as shown in Table 4.3). Due to the difficulties that could arise from this design, alternative layouts that could avoid cracks between the staves, while allowing for a simpler flex cable geometry, are under study.

The maximum thickness of one module package is 2.0 mm. Each disk has modules placed on both sides, leading to a total module package per disk of 4.0 mm plus 0.5 mm tolerance, as detailed in Table 4.3. This assembly has to prevent any flex cable crossing between two adjacent readout rows to assure correct routing. Accurate alignment in x and y directions and a controlled orientation of the peripheral on-detector connectors are required. The inter-disk gap (along z) should be fixed over the total active area. More details on the overall dimensions, including tolerances on the stacking of the various cooling layers are described in the next section.

Spacers will be used to maintain the distance between the support plate and the flex cable, guiding it up to the peripheral electronics. The high thermal conductivity of the spacers also contributes to drain the heat from the flex cables throughout the cooling panels. The materials under study for the spacers are carbon fibre composite, graphite reinforced PEEK, and a VESPEL polyimide graphite filler like SP-21 used in the interfase between the beam pipe and the Inner Detector. Assembly to the cooling panels by screwing and/or a gluing technique with interposed conductive media should give the right thermal bridge properties for the flex cables. A digital assembly process using Computer Numerical Control machining will be used in order to position the spacers accurately with respect of the staves in the x–y plane. This will help prevent the propagation of thermo-mechanical stress between staves, the modules and the flex cables.

With 20×40 mm^2 modules and the readout row concept, the rectangular structures cannot give perfect coverage in azimuthal angle ϕ in the innermost region. As a result, there is full coverage in ϕ up to $|\eta| = 3.86$. In the $|\eta|$ range 3.86–4.00, approximately 92% of the surface area will be instrumented. For $4.00 < |\eta| < 4.07$, some intervals in ϕ are instrumented.

One prototype of the local support plates will be produced to study the thermo-mechanical behaviour, temperature distribution, CO_2 cooling parameters and glue-layer integrity between modules and carbon fibre skins. A scale model of the longest stave will also be built to ensure the feasibility of module assembly and installation of flex cables.

Assembly plans
The assembly will consist of fixing the 7888 modules on their intermediate plates, the installation of the flex cables and the wire-bonding of the flex cables to the sensors and the ASICs. Dedicated tools and procedures will be needed because of the shape of the intermediate plates, constituted by half disks for the inner region and rectangular staves for the outer region. The procedure will therefore be specific to the inner and outer part. For the half-disk intermediate plates, there is two per side of each cooling disk, and four cooling disks, yielding a total of 16 half-disk support plates. For the outer part, there are 18 rectangular staves per quadrant, four quadrants for each side of a cooling plate, and a total of four cooling plates. This gives a total number of rectangular staves of 576 for the outer part. There are 14 different types of staves of varying lengths. The assembly step will be shared between four to six sites, where one or two will specialise on the inner plates and three or four on the outer staves. Different tests will be performed to control the electrical characteristics of the assembly (connectivity, sensors and ASICs operation) as well as the mechanical parameters (dimension, position). In addition, the packaging of each plate equipped with modules and the flex cables is a crucial point, allowing transport and then implementation on the cooling plates at CERN. At this stage, each half-disk cooling plate will be equipped with one inner half disk and the rectangular staves. The cables will be unrolled and attached to the entire length of the cooling plate.

4.2.3 Detector structure

Layers
A transverse view of the HGTD layers is presented in Figure 4.11, stacked to constitute the detector assembly, including cooling plates and silicon modules. The full layer assembly, with the given spacers gap, will match the total envelope of 125 mm, which includes the front and back covers of the vessel and the moderator.

A detailed breakdown of the dimensions of the different detector components is presented in Table 4.3. It lists the thickness of each component per side and per double-sided layer (when applicable), and the total in the detector. The size of the component is given as a nominal thickness (the compact volume occupied by material) and as an envelope thickness (the actual space needed per object, taking into account the tolerance). The current prototype of the sensor and ASIC assembly is about 1 mm thick (detailed in Section 4.3). This estimation gives a comfortable margin with respect to the final assembly protocol (gluing layers, etc.). As explained earlier, the thickness of one Kapton® flex cable is 0.3 mm, while the longest stave in a layer will have 19 modules. Thus, the maximum amount of stacked flex cables will be 10, yielding a maximum thickness per side of 3.0 mm. However, the current design must consider an envelope of 8.0 mm per side to allow the bending of the first flex. The envelope of the sum of the other flex cables and the coupling capacitors fits well within this parameters and doesn't need to be considered separately.

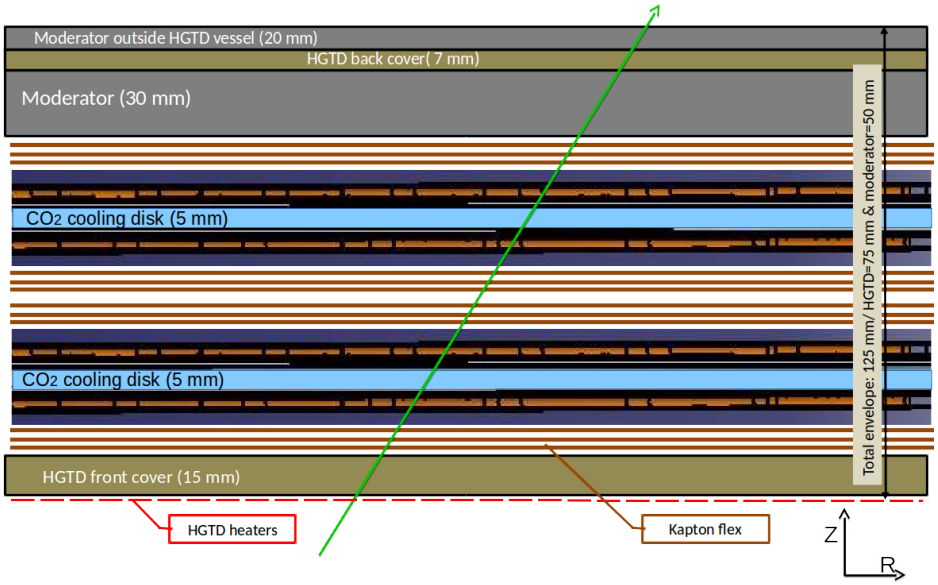


Figure 4.11: Cross section of the entire HGTD vessel including two active layers installed on the cooling plates, the front and back covers, and the moderator. An extra 20 mm moderator is located outside the vessel in close contact with the endcap cryostat.

Support structure

To assemble the individual detector layers, the detector modules will be installed on the highly conductive support plates made of carbon fibre and graphite foam with embedded cooling pipes, inspired by the future ATLAS and CMS trackers. These disks will be divided in two halves, in a way that will allow for an easier mounting and dismounting of the HGTD, even in the event of having the beam pipe in place during installation. The modules will be attached to both sides of the support plates and safely locked by using one screw-pin. The half-disks, staves and modules can be seen in Figure 4.7. An appropriate loading device will be used to guarantee the module alignment and its x-y positioning on the support plate. The flatness and roughness of the plate have to allow the gluing of the modules with the best reachable thermal conductivity.

The support plates will be enclosed by pultruded carbon fibre U-shaped rings which will be the direct interface with the global support (HGTD cold vessel and its central tube) to allow screwing, positioning and alignment with the ATLAS coordinates system.

The moderator is discussed in detail in Section 5.3.

Component	Module layer [mm]		Double-sided layer [mm]		Total HGTD [mm]	
	Nominal	Envelope	Nominal	Envelope	Nominal	Envelope
ASIC+sensor	1.0	1.0	2.0	2.0	4.0	4.0
Support plates	1.0	1.0	2.0	2.0	4.0	4.0
Flex circuit	2.8 - 5.5	8.0	5.6-11.0	16.0	11.2-22.0	32.0
Cooling panel	-	-	5.0	6.0	10.0	12.0
Total	7.5	10.00	20.0	26.0	40.0	52.0
Front cover	-	-	-	-	15.0	16.0
Back cover	-	-	-	-	6.0	7.0
Total HGTD					**61.0**	**75.0**
Inner moderator					30.0	30.0
Outer moderator					20.0	20.0
Total Moderator					**50.0**	**50.0**
HGTD+moderator					**111.0**	**125.0**

Table 4.3: Estimated values of thickness per component. The nominal thickness is the manufacturing dimension of the component. The envelope is the space needed to be allocated for the component. Some components are not considered in the envelope thickness because they are included within another value. Information is given for one side of a layer (when applicable), for a double-sided layer, and the total for one HGTD side.

4.3 Sensors

As discussed above, the time resolution for the HGTD is required to be 30 ps per track over its full lifetime. This translates to a requirement of 42, 52 or 60 ps/hit in case of 2, 3 or 4 independent timing measurements along the particle path. As shown in the following, a resolution in this range can be achieved with silicon sensors with internal gain (LGAD) of 50 µm active thickness. The radiation hardness requirement for the innermost radii (including a safety factor of 1.5) is a 1 MeV neutron equivalent fluence of $3.7 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, assuming one replacement of the inner part after half of the total integrated luminosity of 4000 fb^{-1} (see Section 1).

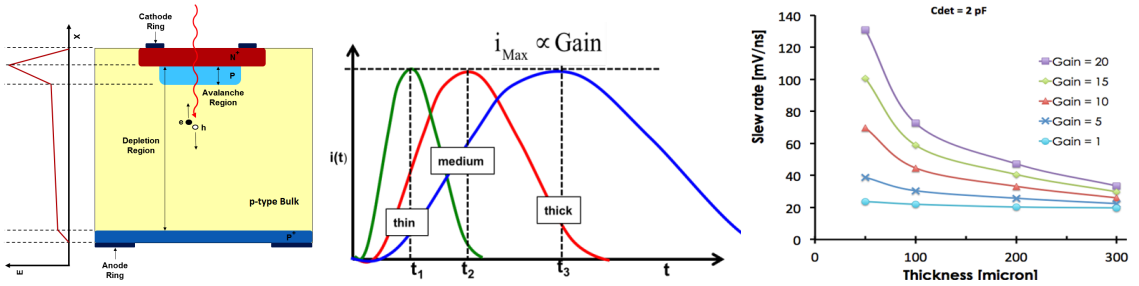
The sensor pad size is restricted by occupancy, pad capacitance and the fill factor. A unified pad size of 1.3×1.3 mm^2 everywhere with an expected capacitance of 3.4 pF is found to fulfil the requirements. The pads will be arranged in arrays of total area of about 20×40 mm^2 (15×30 pads) with a common backplane bias voltage connection.

4.3.1 Low Gain Avalanche Detectors

The technology chosen for the HGTD sensors is Low Gain Avalanche Detectors (LGAD). LGADs are planar silicon detectors with internal gain. They have been pioneered by the Centro Nacional de Microelectronica (CNM) Barcelona [3] and developed during the last 5

years within the CERN-RD50 community [2]. Much background and details are given in Reference [19].

LGADs are n-on-p silicon detectors containing an extra highly-doped p-layer below the n-p junction to create a high field which causes internal gain as displayed in Figure 4.12(a). When a charged particle crosses the detector, an initial current is created from the drift of the electrons and holes in the silicon. When the electrons reach the amplification region, new electron/hole pairs are created and the holes drift towards the p^+ region and generate a large current (i.e. gain).



(a) Cross section of an LGAD diode.

(b) Current signals for LGADs of different thicknesses.

(c) Signal slope as function of LGAD thickness.

Figure 4.12: Working principle of LGAD sensors and how their response depends on sensor thickness [19].

While the signal height i_{Max} of the LGAD is proportional to the gain M, it is independent of the detector thickness as illustrated in Figure 4.12(b). On the other hand, Figure 4.12(c) shows that the signal slope dV/dt depends on the thickness of the sensor, favouring thin sensors [19]. An LGAD thickness of 50 µm has been adopted as the baseline and studied in detail. LGADs of 35 µm thickness recently have become available as well and are studied as an option with an even larger signal slope at the expense of an increased capacitance.

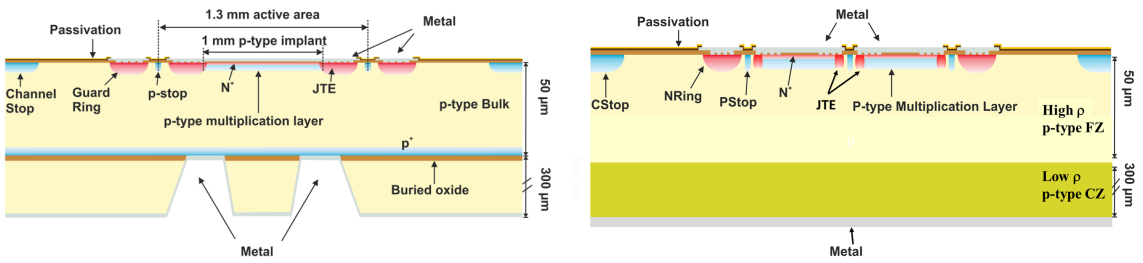
Two major effects from the electronics which determine the time resolution are the time walk and the time jitter. Both depend inversely on the signal slope dV/dt:

$$\sigma_{\text{TimeWalk}} = \left[\frac{V_{\text{th}}}{\frac{S}{t_{\text{rise}}}}\right]_{\text{RMS}} \propto \left[\frac{N}{\frac{dV}{dt}}\right]_{\text{RMS}}, \qquad \sigma_{\text{Jitter}} = \frac{N}{(dV/dt)} \simeq \frac{t_{\text{rise}}}{(S/N)}, \tag{4.1}$$

where S refers to the signal, N to the noise, t_{rise} to the rise time and V_{th} to the threshold voltage. Thus the time resolution of the LGAD is tied to the value of its signal slope. The dependence of the slope on sensor thickness and gain is shown in Figure 4.12(c). The best time resolution, i.e. the largest slope, is achieved with thin sensors and large gain. This observation feeds into the plan to operate LGADs at as large a gain as possible given restrictions from the leakage current and the breakdown voltage. Our investigations point to a safe gain of about 20.

In addition to the research carried out by CNM, the Fondazione Bruno Kessler (FBK) Trento has also designed and produced LGAD sensors [20], as well as Hamamatsu Photonics (HPK) [19]. In general, the LGAD sensors produced by different manufacturers appear to perform very similarly, with the exception of the leakage current before irradiation, and the bias voltage reach after irradiation.

CNM has produced thin LGADs in 2016 in run 9088 within an RD50 Common Project [2] and in 2017 in the HGTD specific run 10478 [21]. Both runs were on 4" wafers with nominally 50 µm thickness of the active high-resistivity Float zone volume. Run 9088 was in a silicon-on-insulator (SOI) process with the back-side contact done through wet-etched deep access holes through the insulator (see Figure 4.13(a)). Most of the tests were performed on single-pad sensors of 1.3×1.3 mm^2 active area (called *LGA*) and 2×2 arrays of pads with 2.063×2.063 mm^2 active area each and a no-gain gap of 63 µm between adjacent pads. Three sets of wafers were produced with a different multiplication layer implantation dose to optimise the gain: 1.8×10^{13} cm^{-2} (low), 1.9×10^{13} cm^{-2} (medium) and 2.0×10^{13} cm^{-2} (high). In run 10478, wafer-to-wafer (Si-Si) bonded wafers were used (see Figure 4.13(b)). The dose was nominally 2.0×10^{13} cm^{-2} (high2). It also includes arrays with 2×2 pads of 1.1 and 2.1 mm active width that are compatible with the HGTD ALTIROC0 readout chip (see Section 4.4) with under-bump metalization (UBM) to ensure bump-bonding (see Section 4.2.1). An important further development for improving the breakdown behaviour of the array sensors is the inclusion of a junction termination extension (JTE) around each individual sub-pad. Part of the wafers include carbon spray to test if this improves radiation hardness (see Section 4.3.4). CNM also finished the production of a 300 µm thick test run on 6" wafers and will use this wafer size for future 50 µm thick runs. Moreover, a run on 35 µm thick wafers is ongoing.



(a) LGA single-pad sensor.

(b) Array sensor with 2×2 pads.

Figure 4.13: Cross section of LGAD structures. (a) LGA single pad from CNM run 9088 (SOI substrate). (b) 2×2 array of CNM run 10478 including a JTE around each sub-pad (Si-Si wafer) [21].

Hamamatsu Photonics (HPK) delivered LGAD sensors from run #ECX20840. They were manufactured on Si-Si bonded 6" silicon wafers of 150 µm total thickness with a 50 µm or 80 µm thick high resistivity float zone (FZ) active layer on top. Samples with four different "gain splits" (denoted A-D) were produced, identical in the mask design but with a different p^+ dose of the gain layer, to study the optimum parameters of the charge multiplication

mechanism. A has the lowest, D the highest dose. The capacitance-voltage (C-V) measurements indicated that the difference between doping concentrations of adjacent splits is about 4%. The most studied devices have 50 µm thickness with C or D dose, denoted 50C or 50D in the following. The wafers contain circular single-pad sensors of area about 0.8 mm^2 and 2×2 arrays of 3x3 mm^2 pads. The arrays have a no-gain gap of 100 µm between adjacent pads. Recently also 35 µm thick LGAD single-pad sensors of 0.8 mm^2 area were provided with one single dose split, which will be referred to as B35 in the following.

4.3.2 Sensor tests: methodology and experimental techniques

The LGAD sensors have been tested by various HGTD groups, as well as within the RD50 community. Electrical measurements including capacitance-voltage (C-V) and current-voltage (I-V) characteristics have been performed in laboratory probe stations. The dynamic properties of LGADs, such as charge collection, gain and time resolutions, have been measured in response to ionising particles, both in the laboratory with ^{90}Sr β particles [19, 22–26] and lasers, as well as in beam tests with pions at CERN and Fermilab [24, 25, 27].

Different readout boards and amplifiers have been used, including commercial broad band or charge-sensitive amplifiers and an HGTD-specific development with a high bandwidth, allowing the recording of the pulse shape of the fast LGAD signals [24]. This readout board has been made available in the meanwhile to many HGTD institutes via production at CERN. The analog waveforms are then typically recorded with a fast oscilloscope.

Position-sensitive scans using red and infrared laser to deposit charge carriers inside the sensors have been made at various institutes, using the Transient Current Technique (TCT) setup.

Beam tests have been performed by the HGTD community in five periods in 2016 and 2017 at the H6 beam line of the CERN SPS with 120 GeV pions [27]. Data were taken in two modes: stand-alone and integrated into a beam telescope that provided track position information with about 3 µm precision.

The gain is extracted by dividing the collected charge in an LGAD device by the charge of no-gain PIN diodes without multiplication layer (for betas and MIPs about 3 ke^- or 0.46 fC for 45 µm thickness).

Time resolutions are typically extracted from the spread of the time-of-arrival difference between two sensors when a particle passes through both. Either at least two LGADs are used or LGADs and a fast Cherenkov counter based on quartz bars and a silicon photo multiplier (SiPM) with typical time resolution of about 10 ps. If at least three devices are measured simultaneously, a χ^2 minimisation is used to obtain the time resolution of all devices. In case only one device under test (DUT) is measured with respect to one reference device of known resolution, the DUT resolution is obtained by subtracting quadratically the reference contribution. Different time reconstruction algorithms have been investigated

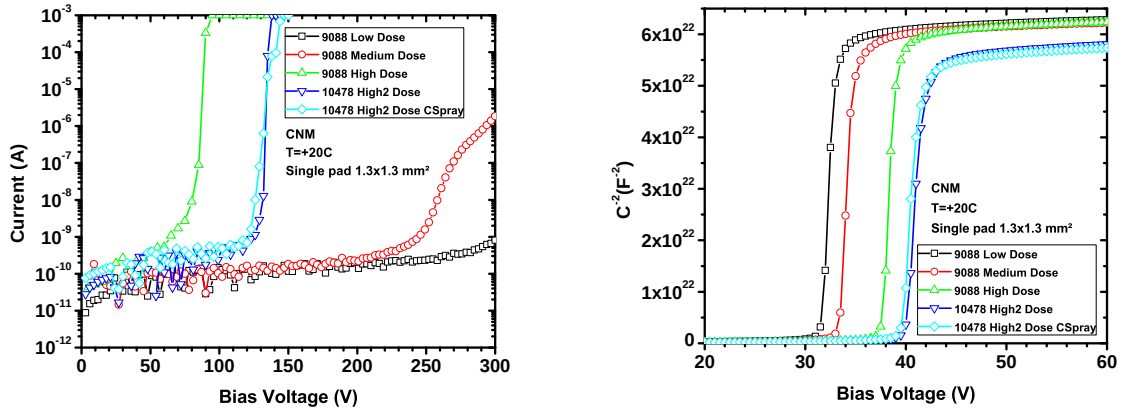
such as the Constant-Threshold Discriminator (CTD), the Constant-Fraction Discriminator (CFD), the Zero-Crossing Discriminator (ZCD) or corrections using the amplitude or Time-Over-Threshold (TOT) of the signal [27].

Preliminary studies carried out on irradiated sensors in test beam show negligible values of cross-talk between pads in a sensor array.

4.3.3 LGAD performance results before irradiation

Electrical characterisation: I-V and C-V

Figure 4.14 shows the I-V and C-V curves of 1.3x1.3 mm^2 LGAD pads of CNM runs 9088 and 10478 of different multiplication layer doses. The leakage current before breakdown is typically in the order of 0.1 nA. The breakdown voltage increases with decreasing multiplication layer dose for the same run (about 80, 240 and 300 V for high, medium and low doses of run 9088). The breakdown voltage of run 10478 is higher (125 V) than the one of 9088 with the same nominally high dose due to process improvements, especially in the JTE. Also the range of the "foot" of the $1/C^2$ vs. V (i.e. the region where $1/C^2$ stays at low values while the multiplication layer is being depleted, starting from the n-p junction at the front) is an indicator of the multiplication layer dose. Foot values between 30 and 40 V indicate substantial gains, as verified below. It can be seen that for the same nominally high dose of run 9088 and 10478, there are moderate run-to-run variations. The depletion of the bulk (indicated by the rise of $1/C^2$-V) happens rather fast within a few V due to the high resistivity and the small thickness. From the end capacitances of about 3.9 pF and 4.2 pF (measured with a connected guard ring) one can conclude an active thickness of 45 and 42 µm for runs 9088 and 10478, respectively.



(a) Current as function of bias voltage.

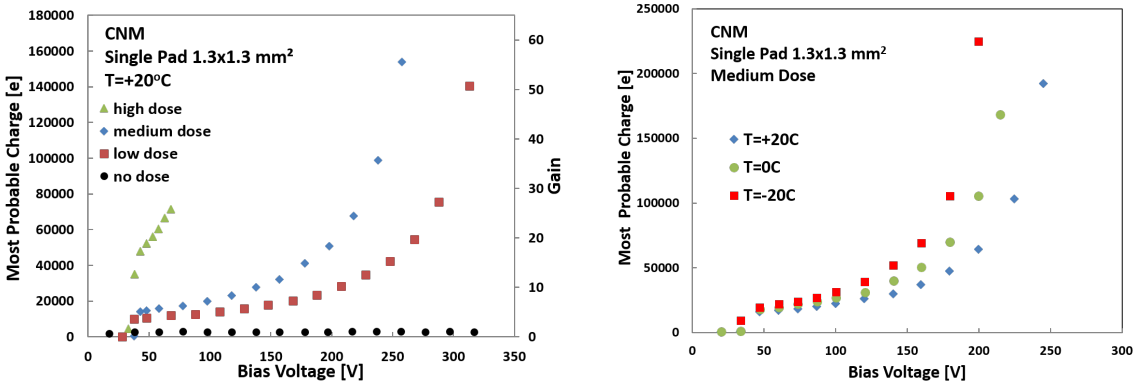
(b) Capacitance as function of bias voltage.

Figure 4.14: Measurements of (a) current-voltage and (b) capacitance-voltage of CNM LGA single-pad sensors from runs 9088 and 10478 of different multiplication-layer doses [21].

The current level of all HPK devices before breakdown is very low, typically below 0.1 nA. As expected, devices with lower doses have a much later breakdown (300 V for dose D, 700 V for dose A for 50 µm). The I-V curve uniformity between different samples was found to be very good for both single-pad and array sensors. The capacitance-voltage (C-V) measurements indicated that the difference between doping concentrations of adjacent splits is about 4%. The end capacitance of the 0.8 mm^2 single-pad sensors was measured as 2.7 and 4.6 pF for 50 and 35 µm, respectively (larger than expected from the nominal area due to an increased active area resulting from floating guard rings).

Collected charge and gain

For 50 µm thick CNM LGAD from run 9088, Figure 4.15 shows the gain and collected charge as a function of bias voltage. Figure 4.15(a) displays different doses measured at 20 °C. It can be seen that the charge and gain is higher for higher doses at a fixed voltage, as expected. The low and medium dose can be measured up to a final gain of 50–60 at breakdown voltages of 250 and 310 V, respectively, whereas the high dose breaks down already at 80 V at a gain of 20. Figure 4.15(b) shows the gain curve for different temperatures. Due to higher impact ionisation, the gain increases at lower temperatures, and the breakdown is decreasing. Similar results have been measured for HPK LGAD [26].



(a) Varying dosage.

(b) Varying temperature.

Figure 4.15: Gain or charge vs. bias voltage for sensors from CNM run 9088. (a) Comparison of all multiplication-layer doses at 20 °C. (b) The medium dose compared at 20 °C, 0 °C and −20 °C [23].

During beam tests the gain was measured also as a function of position for single-pad and array sensors and found to be uniform for fully metallized structures. For arrays, there is a no-gain gap between adjacent pads due to the missing multiplication layer in that region. Its width is measured as 70–100 µm for current sensor designs.

Efficiency

The hit efficiency was measured in HGTD beam tests using an external telescope for reference tracks [27]. For all devices before irradiation, mean values of 96–100% were obtained consistently with thresholds of at least 10 times the noise level. Figure 4.16(a)) shows the efficiency map of a 2×2 array, exhibiting a good uniformity in the centre of each pad. Only in the no-gain gap between adjacent pads, a reduced efficiency was found.

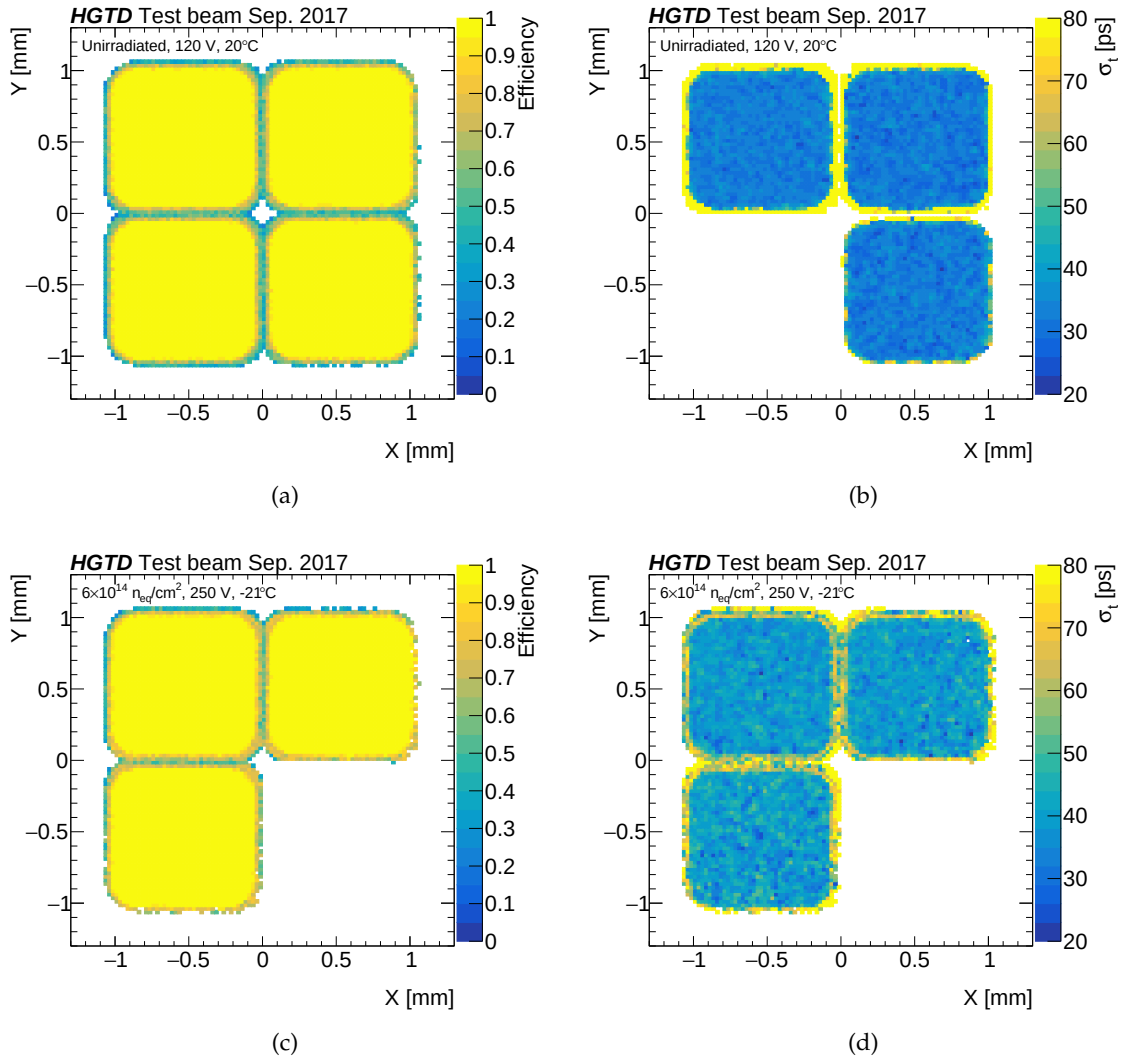
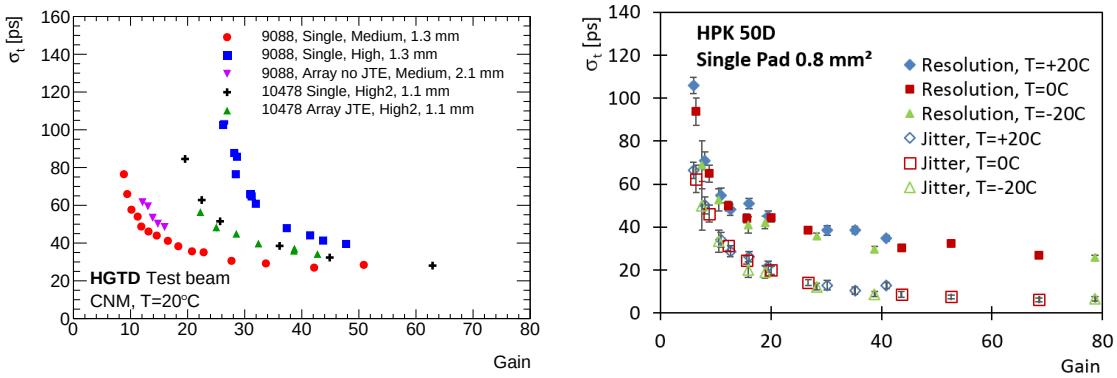


Figure 4.16: 2D maps of efficiency (left) and time resolution (right) before irradiation (top) and at a fluence of 6×10^{14} n_{eq}/cm^2 (bottom) for a 2×2 array from CNM run 10478 as measured in HGTD beam tests [27]. Sometimes only 3 channels were measured. The efficiency was evaluated at a threshold of 3 times the noise here.

Time resolution

The time resolutions of CNM and HPK devices have been extensively studied in various beam tests [24, 25, 27] and ^{90}Sr setups [19] (see Figure 4.17). It has been consistently shown that sub-30 ps time resolution can be achieved below the breakdown point before irradiation for sensors from all vendors with pad widths up to 1.3 mm and up to 5 pF capacitance on the custom-made test readout board explained above. Whereas in the early CNM run 9088, the 2 × 2 arrays did not achieve the gains and time resolutions of single pads due to the lack of a JTE and higher capacitances, the arrays including a JTE from run 10478 show similar performance as the single pads of same size. Devices with a high doping dose show a larger time resolution at the same gain for moderate gains because of lower applied voltages and hence larger rise times due to non-saturated drift velocities. Figure 4.16(b) shows the map of the time resolution for a 2 × 2 array, exhibiting a good level of uniformity, both within each pad and comparing the different pads of the array, except for the no-gain inter-pad regions.



(a) Sensors produced by CNM.

(b) Sensors produced by HPK.

Figure 4.17: Time resolution σ_t as a function of gain. For (a) CNM single-pad sensors and arrays with/without JTE of medium and high doping [27]; and for (b) HPK 50D single-pad sensors measured at different temperatures. Also the jitter is shown [19].

Whereas at a fixed voltage, the time resolution is improving for lower temperatures due to the higher gain, it can be seen that the resolutions measured at different temperatures collapse to a universal curve when presented as a function of gain before irradiation.

For HPK, Figure 4.17(b) also includes the measured electronic jitter, which is found to be significantly lower than the total time resolution, especially at high gains in the test beam. This indicates that contributions from Landau fluctuations dominate there.

4.3.4 Irradiation tests

Irradiation of silicon mainly results in the change of the effective doping concentration, the introduction of trapping centres that reduce the mean free path of the charge carrier, and the increase of the leakage current [2].

LGAD samples of 50 µm thickness from CNM (run 6827 and 9088) and HPK (run ECX20840) as well as 35 µm thick HPK B35 were irradiated by neutrons at the JSI research reactor in Ljubljana up to 1 MeV neutron-equivalent fluences of 6×10^{15} n_{eq}/cm^2 [23]. After irradiation the devices were annealed for 80 min at 60 °C. Also irradiations at CERN-PS with 24 GeV protons were performed; measurements and analyses are ongoing. The results after neutron irradiation are presented below.

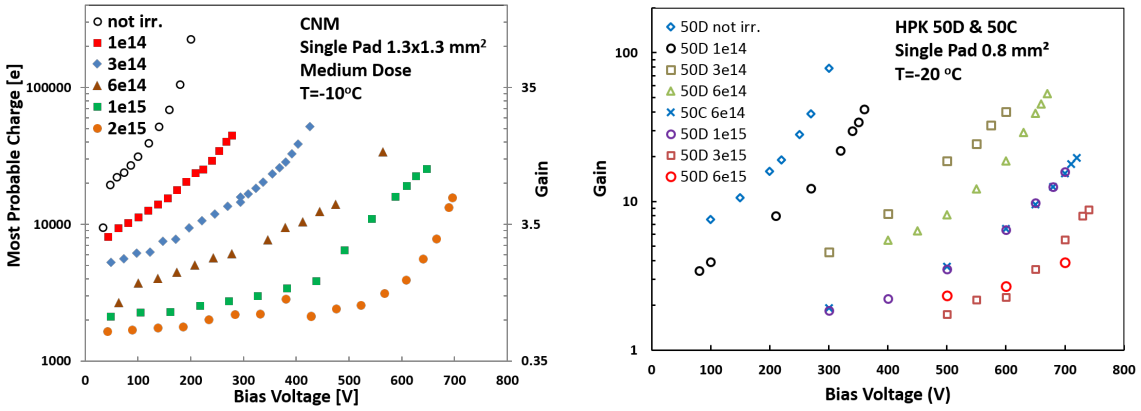
Gain evolution after irradiation and acceptor removal
The gain was found to decrease with irradiation which was attributed to loss of the effective doping concentration in the multiplication layer due to deactivation of initial boron as acceptors, as has been observed before on 300 µm thick LGADs [22]. This can be observed in Figure 4.18 for 50 µm thick CNM and HPK devices, which show a very similar behaviour. The gain G steadily decreases with irradiation.

Beyond a fluence of about 10^{15} n_{eq}/cm^2, there is little difference between devices without (PIN) and with (LGAD) a built-in multiplication layer due to its removal. However, at such high fluences a gain is observed for both PIN and LGAD devices since deep effective acceptors created by irradiation in combination with a higher breakdown voltage result in electric fields high enough for charge multiplication also in originally no-gain detectors. This effect has been observed before [28–30]. In this case the multiplication takes place over large parts of the volume at very high average fields (around 15 V/µm). Therefore the increase of charge with bias voltage is very steep after the onset of multiplication. This means that detectors are operated close to device breakdown which requires very good temperature control and voltage stability. Nevertheless gains of G=8 were measured for devices irradiated to 4×10^{15} n_{eq}/cm^2.

Owing to the small thickness of the device and consequently short drift times, the trapping of the drifting charge only marginally affects the collected charge. The larger the initial implant doping the longer the gain remains large, as can be seen from Figure 4.18(b) from comparing the lower dose 50C to the higher dose 50D at 6×10^{14} n_{eq}/cm^2. Hence, an initially larger dose is beneficial in terms of radiation hardness.

A regional dependence of the gain was found in position-sensitive beam tests for the CNM single-pad sensors (LGA) that have holes in the top metallization [31]: at 6×10^{14} n_{eq}/cm^2 the gain below the metal was found to be up to 2.5 times higher than below the hole. This effect, its cause and its impact on time resolution is still under study. The final HGTD detector will have a full metallization (where the gain was observed to be higher). The gain and efficiency of fully metallized sensors, however, was found to be uniform. The hit efficiency map for a 2×2 array from run 20578 is shown in Figure 4.16(c) for a fluence of

6×10^{14} n_{eq}/cm^2 at a threshold of 3 times the noise level. A mean efficiency in the pad centre of 99% is maintained up to a threshold of 5 times the noise level. The hit efficiency of higher fluences is under investigation.



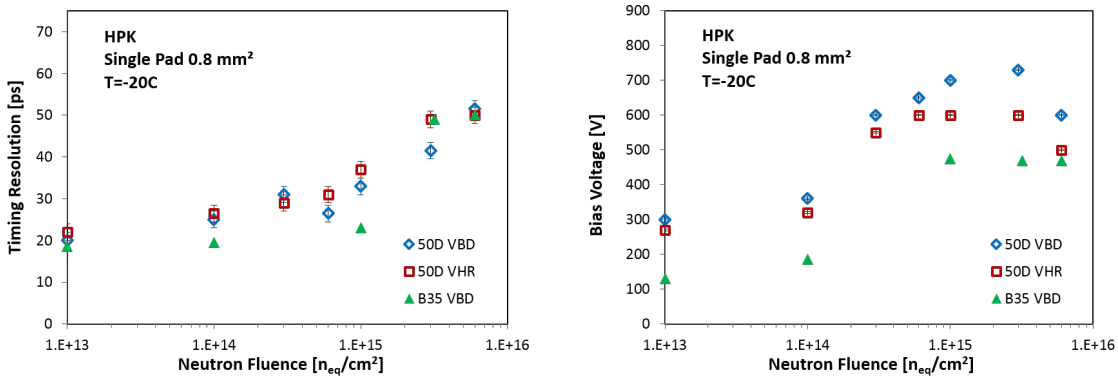
(a) Sensors produced by CNM.

(b) Sensors produced by HPK.

Figure 4.18: Most probable charge or gain dependence on bias voltage for different fluences (in n_{eq}/cm^2) measured for (a) CNM single-pad sensors from run 9088 with medium dose [23] and (b) HPK 50D/50C single-pad sensors [26].

Time resolution after irradiation

The timing performance of neutron irradiated CNM and HPK LGADs was studied in the laboratory with a β-telescope [19, 26, 32] and in beam tests [25, 31].



(a)

(b)

Figure 4.19: (a) Time resolution as a function of neutron fluence for HPK 50D at VBD and VHR and B35 at VBD at −20 °C. (b) Fluence dependence of VBD and VHR [26, 32].

The fluence dependence of the time resolution for HPK LGADs of 35 and 50 µm thickness (B35 and 50D) is shown in Figure 4.19(a). For 50D, to understand the "headroom" for detector operation, the time resolution was evaluated at a bias voltage just below breakdown

(VBD) and at a bias lowered by about 10% or more (headroom voltage, VHR). The corresponding voltage values are shown in Figure 4.19(b). For 50D, the time resolution at VHR was found to deteriorate from about 20 ps before irradiation to 40 ps after 1×10^{15} n_{eq}/cm^2 and to 50 ps after 6×10^{15} n_{eq}/cm^2. The needed bias voltages increase from about 300 V to about 600 V after 3×10^{14} n_{eq}/cm^2, after which they remain relatively stable. For B35, the time resolution before irradiation and at high fluences is similar to 50D, whereas at intermediate fluences the resolution is lower by about 10 ps. A major advantage of B35 is that the bias voltage needed is lower than for 50D, typically by 100-200 V. This translates into lower power dissipation as discussed below.

The resolution was found to improve by typically a few ps at a measurement temperature of −30 °C with respect to −20 °C for the same voltage.

Considering the low gain at high fluences (see Figure 4.18), a worse time resolution would have been expected. However, part of the charge multiplication occurs in the bulk of the sensor as explained above. This leads to a decrease in the rise time of the signal. Moreover, the noise was found to increase at high fluences and voltages. For these reasons, in that regime, the time resolution is not anymore a universal function of gain nor does it decrease monotonically with voltage as before irradiation or at lower fluences.

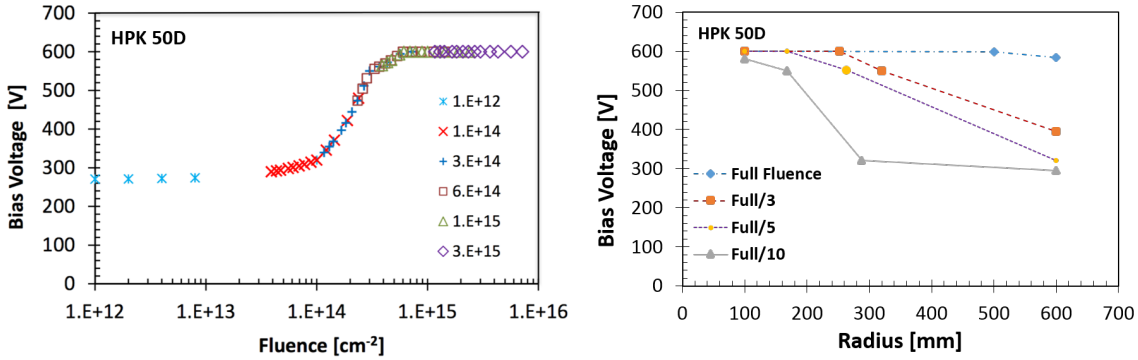
The time resolution of CNM devices after irradiation was investigated in a first study on LGA single-pad diodes [25]. However, as mentioned above, the gain was found to be lower in the metal hole of these devices, which results in a time resolution degradation. New measurements with fully metallized surfaces are ongoing. Figure 4.16(d) shows a first study of a fully metallized 2×2 array at 6×10^{14} n_{eq}/cm^2, exhibiting a mean time resolution of 39 ps with a spread of 3 ps in the pad centre.

To conclude, these results show that the currently available LGAD test sensors can be operated safely up to the HGTD target fluence of 3.7×10^{15} n_{eq}/cm^2, keeping a time resolution of 50 ps/hit under laboratory conditions. It is still under study what will be the full-system time resolution for a large array including final electronics in a power-limited readout chip, which might increase the jitter, in particular for B35 with a higher capacitance (see Section 4.4). In parallel, further development to improve the sensor time resolution after irradiation is ongoing as explained below. The final projected time resolution of the HGTD system will be known at the end of this full evaluation and after the decision of the final HGTD layout. Moreover, the time resolution measurements need to be complemented with hit efficiency studies for all fluences, which is a priority for upcoming beam tests.

Evolution of operation voltage during sensor lifetime

The gain degradation with fluence makes it necessary to adjust the operation voltage over the lifetime of the detectors. This is for example shown in Figure 4.19(b) where VHR is a good indicator for an operation voltage as a function of fluence that provides sufficient time resolution while still being safely below the breakdown point (these studies still need to be complemented with hit efficiency measurements). For the baseline thickness of 50 µm, it rises from about 300 V before irradiation to 600 V at 3×10^{14} n_{eq}/cm^2, after which it stays

relatively constant (it should be noted that the exact values are technology and doping specific, the values here refer to HPK 50D as an example). Monitoring of the leakage current and the TOT as an indicator of collected charge will give a good estimate of the gain evolution during operation, allowing to perform the necessary adjustments. The expected dependence of the fluence on the radius (Figure 2.4) and the required bias voltage for the increasing fluence (Figure 4.19(b)) permits a prediction of the bias-voltage distribution along the length of a readout row containing individual modules mounted on support plates (see Section 4.2). This is shown in Figure 4.20(a), where the bias voltage as a function of fluence for different fluence levels at a radius $R = 300$ mm are shown. In Figure 4.20(b) this is translated into the bias voltages for different radial position along the longest readout row for a few fluence steps. It shows that the ability to connect several nearby modules to the same bias supply allowing a 10% variation in the bias to modules on one bias supply will be limited.



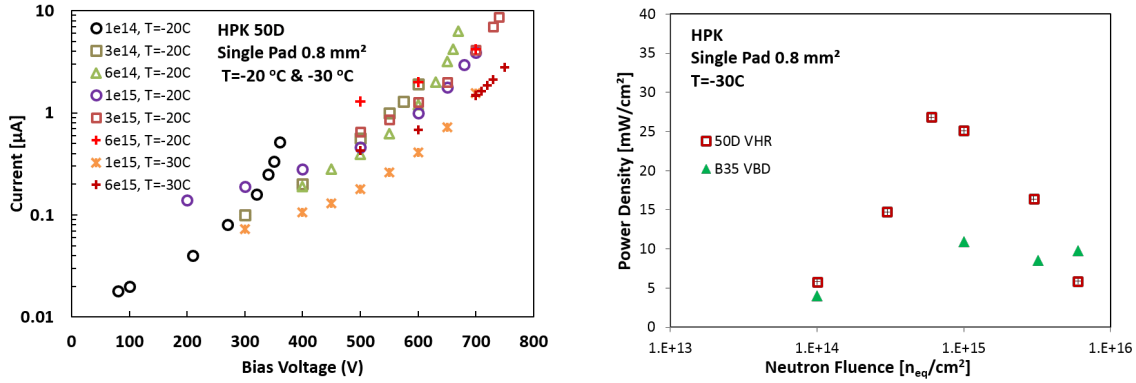
(a) (b)

Figure 4.20: (a) Required bias voltage vs. fluence for different fluence levels at $R = 300$ mm. A rapid increase is seen between 10^{14} and 3×10^{14} n_{eq}/cm^2. (b) Required bias voltage as a function of position along the longest readout row for four different fluence levels. Planned replacement of inner-radius modules not taken into account.

Leakage current and power dissipation after irradiation

In standard silicon sensors without gain, the leakage current originating from volume generation current increases linearly with fluence. However, for LGADs the situation is more complex due to the gain and its fluence evolution. The operation in gain mode leads to an increase of the leakage current, which is given by the product of the volume generation current and the current multiplication factor. As the gain decreases with irradiation and the generation current increases, the leakage current does not necessarily increase monotonically with fluence. The leakage current in multiplication mode contributes to parallel noise linearly, hence it is of high importance to run the sensors at low temperatures since cooling decreases the leakage current (roughly by a factor of 2 every 7 °C).

The total leakage currents (sum of bias ring and guard ring) for the different fluences as a function of the bias voltage shown in Figure 4.21(a) exhibit large increases for increased



(a) (b)

Figure 4.21: (a) Leakage current at −20 °C and −30 °C as a function of bias voltage for HPK 50D irradiated to the neutron fluences indicated. The current is the sum of the bias ring current which is multiplied in the gain layer and the current from the periphery collected by the guard ring. (b) Power density as a function of fluence at VHR (50D) and VBD (B35) at −30 °C for the leakage current collected by the bias ring only [26, 32].

bias, partially due to the increased gain. The current through the bias ring (as indicator for the current through the multiplication region only) has been also measured separately without the guard ring current, which allows to determine the power density (power/area) in the multiplication region. The power can be minimised by operating the sensors at the lowest temperature and the lowest bias voltage. For the assumed lowest possible operation voltage (−30 °C) and a bias voltage of VHR for 50D and VBD for B35, Figure 4.21(b) shows the measured power density as a function of fluence. It can be seen that the power density stays below the target of 30 mW/cm^2 for the full fluence range up to the end of lifetime at −30 °C. The power of B35 is typically significantly lower than for 50D.

Developments for improved radiation hardness

With the aim of improving the radiation hardness further, a project is underway in collaboration with RD50 to reduce the acceptor removal that is responsible for the gain loss.

The first idea is to replace the gain layer boron (B) with gallium (Ga), which is heavier than B and is expected to have reduced formation of interstitial Ga compared to B under heavy irradiation. The second one is to manufacture LGAD on carbon (C)-enriched wafers at the surface so that C will act as traps for the interstitial Si that was removed from its lattice by radiation. Hence the interstitial Si would react less with the multiplication layer B, hence reducing the probability for acceptor removal. Both CNM and FBK have performed LGAD runs with Ga implantation and C enhancement; studies are ongoing.

4.3.5 Roadmap for future sensor productions and activities

There are several new LGAD productions ongoing and in preparation. The most important aim will be to produce for the first time full-size LGAD sensors and determine their yield and uniformity. Sensors with the possibility of bump-bonding them to the next versions of the ALTIROC readout chips (arrays of 5×5 and 15×15 pads with under-bump-metallization) will be provided. Moreover, many test structures with technology variations are included such as different inter-pad gaps to optimise the fill factor and different slim-edge designs. It is planned to go as much as possible in parallel with HPK and CNM and implement the same device geometries with a similar mask layout in 6-inch runs of both vendors. 15 wafers are being ordered at each site, including 50 µm thickness as the baseline and a few 35 µm thick wafers as an option, with C-spray for possibly enhanced radiation hardness on a few wafers. Funding is shared between ATLAS and CMS institutions. A delivery is foreseen in Q2 2018, followed by extensive testing at HGTD institutes and beam tests. Priorities of the measurement program will be the evaluation of the time resolution, hit efficiency and power dissipation after neutron and charged hadron irradiation, as well as annealing and long-term stability studies. Based on these results, a new production iteration with optimised parameters and baseline designs is foreseen for 2019, before the pre-production is launched in 2021.

4.4 Readout electronics

The sensors will be read out by dedicated on-detector front-end electronics ASICs (bump-bonded to the sensors) which should keep the intrinsic excellent time resolution of the LGAD. The digitised ASIC output signals will be transferred through electrical links, or *e-links*, on flex cables to the peripheral on-detector electronics located at the periphery of the detector between 700 mm $< R <$ 900 mm (see Figure 5.8), and finally to USA15 with optical fibres. Taking the detector occupancy (which defines the bandwidth) into account, the detailed hit information will be read out only after a L0/L1 trigger (at about 1 MHz). The number of hits for each ASIC covering $R \geq 320$ mm in both layers will be transmitted at 40 MHz for online luminosity measurements.

The ASIC design is challenging due to the harsh radiation environment in which it will operate, and the need to meet the required performance while keeping power dissipation to a minimum. As mentioned before, one such requirement is to have a time resolution comparable to that of the LGAD. The contribution to the time resolution from the electronics is given by :

$$\sigma^2_{\text{elec}} = \sigma^2_{\text{jitter}} + \sigma^2_{\text{TW}} + \sigma^2_{\text{TDC}} \tag{4.2}$$

where σ_{jitter} depends on the noise and the pulse slope as defined in Eq. (4.1). The time walk (TW) contribution is expected to be negligible if an offline correction from a TOT measurement is applied. The TDC bin should be smaller than the timing resolution. With

a TDC bin size of 20 ps the contribution to the resolution is negligible, of about 5 ps. An additional contribution could come from the clock distribution, although it is expected to be small. The time offset of each individual channel will need to be calibrated in situ, as described in Section 4.4.13.

This section discusses the requirements on the HGTD front-end electronics, followed by a description of the global architecture to satisfy these requirements and the front-end ASIC architecture proposed. More detailed descriptions are then given on some of the ASIC components, namely the single channel analog and digital components and the phase shifter. A preliminary measurement of a first analog prototype is presented. Finally the clock distribution and time offset calibration are discussed.

4.4.1 Requirements

Front-end ASIC requirements
The following requirements of the ASIC are driven by the targeted 30 ps time resolution per MIP after irradiation obtained through the combination of multiple hits. A summary of these requirements is presented in Table 4.4.

- The ASIC will have to withstand high radiation levels. As in the case of the sensors, some ASICs will have to be replaced during the HL-LHC period. The expected radiation levels have been presented in Section 2.3, considering a 2.25 safety factor for the electronics. Thus, the maximal TID is 4.1 MGy (at $R = 120$ mm) and decreases with radius. At $R = 320$ mm (the edge of the region that will be replaced by half the HL-LHC lifetime) it reaches a value of of 1.6 MGy.

- The preamplifier dynamic range, up to 20 MIPs, has been determined by simulating electron showers in the HGTD detector.

- The electronics jitter for a charge of about 10 fC (equivalent to the charge deposited by a MIP in an 50 µm thick LGAD with a gain of 20) is required to be smaller than 25 ps, i.e smaller than the dispersion induced by the Landau fluctuations on the energy deposit which limits the time resolution to 25 ps at large sensor gain. The contribution to the time resolution from the TDC should be negligible and leads to a 20 ps TDC bin for the Time-Of-Arrival measurement (TOA) and a 40 ps (20 ps) TDC bin for the TOT measurement using a voltage (TZ) preamplifier. The TOA and the TOT require respectively 7 and 9 bits. The time walk should be smaller than 10 ps over the 20 MIPs dynamic range.

- The TOA and TOT information are transferred to the data acquisition system only upon L0/L1 trigger reception with latency up to 35 µs [33], therefore necessitating a large size memory.

- In order to measure the online bunch-by-bunch luminosity, each ASIC will report the sum of hits within two different time windows. A schematic drawing of the windows is shown in Figure 4.22. A first 3.125 ns wide window is centred at the expected arrival time of the particles from the collisions. The second window is adjustable in length and position in steps of 3.125 ns, and will count the number of particles arriving before and/or after those from the collisions. This side-band will provide valuable information of the background, as described in Section 3.2. The length and alignment is adjustable via configuration parameters, to be optimised based on operational experience.

  To limit the bandwidth required for the luminosity measurement, the hit summary information of only a subset of the ASICs is used. The current proposal is to use the sensors located at 320 mm $< R <$ 640 mm, or equivalently $2.4 < \eta < 3.08$. The use of both layers would not provide a significant increase in coverage with respect to just one of the layers, but the redundancy aids in estimating and reducing the systematic uncertainty on the measured luminosity and provides contingency in the event of failures in the instrumentation.

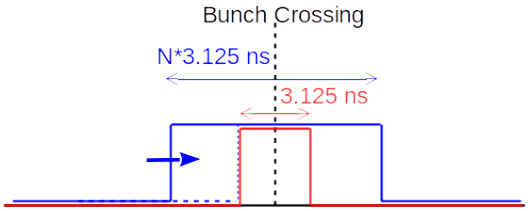


Figure 4.22: Illustration of the time windows used for counting hits for the luminosity data. The smaller window (in red) is 3.125 ns wide and is centred at the bunch crossing time. The width and relative location of the larger window (in blue) can be set in steps of of 3.125 ns through the control parameters.

- Finally the ASIC power dissipation should be kept below 300 mW/cm^2, where the value is set by the maximal cooling power provided by a single CO_2 cooling unit (for more details on the cooling system see Section 5.1).

Bandwidth requirements

The bandwidth of each ASIC strongly depends on the radial region it covers, as shown by the distribution of the average and maximum numbers of hits in each ASIC in Figure 4.23. The distributions are extracted from a sample of simulated events with an invisibly decaying Higgs boson at $\mu = 200$. A dedicated buffer is needed in the ASIC to average the rate variation and match the best speed of the e-link drivers/low power gigabit transceiver (lpGBT) inputs :

- The largest average hit rate at small radius does not exceed 30 hits, equivalent to a rate of 720 Mb/s (not including header). A bandwidth of 1.28 Gb/s will be enough for the innermost radius ASICs (up to $R \simeq 150$ mm).

Pad size	1.3×1.3 mm^2
Detector capacitance	3.4 pF
TID and neutron fluence	Inner region: 4.1 MGy3.7×10^{15} n_{eq}/cm^2
	Outer region: 1.6 MGy, 3.0×10^{15} n_{eq}/cm^2
Number of channels/ASIC	225
Collected charge (1 MIP) at gain=20	9.2 fC
Dynamic range	1-20 MIPs
(preamplifier+discr.) jitter at gain = 20	< 20 ps
Time walk contribution	< 10 ps
TDC binning	20 ps (TOA, TZ TOT), 40 ps (VA TOT)
TDC range	2.5 ns (TOA), 5 ns (TZ TOT), 10 ns (VA TOT)
Number of bits / hit	7 for TOA and 9 for TOT
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)
Total power per area (ASIC)	<300 mW/cm^2 (<1.2 W)
e-link driver bandwidth	320 Mb/s, 640 Mb/s or 1.28 Gb/s
Latency for L0/L1 triggering	10/35 µs

Table 4.4: Front-end ASIC requirements. The radiation levels include the safety factors defined previously and assume that the sensors and ASICs in the inner region ($R \leq 320$ mm) are replaced after half of the HL-LHC program.

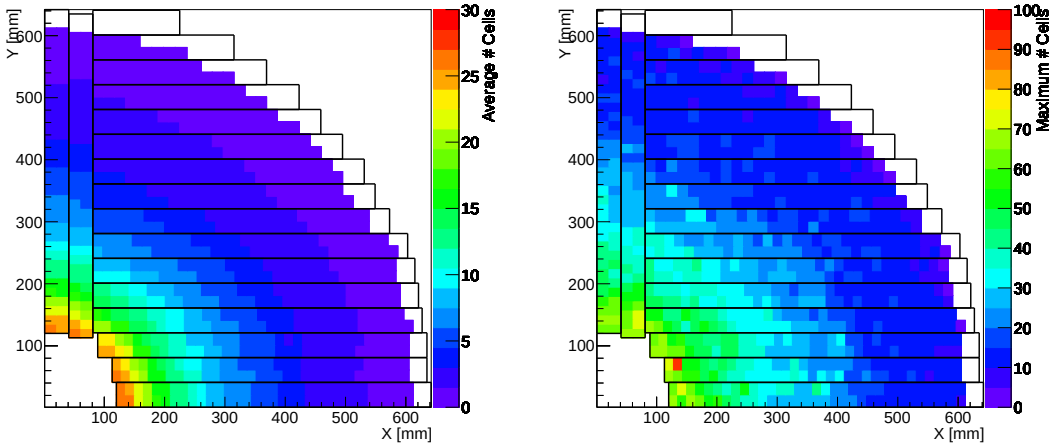
- For larger radii, a 320 Mb/s bandwidth can be used.
- For the luminosity data, the maximal number of hits per ASIC at $R > 320$ mm should be considered. This number does not exceed 40. With a 4-bit header in addition to the 7+5 bits of data for the two hit counts, a 640 MB/s e-link driver and lpGBT speed is needed.

The total number of lpGBTs is 1200 for the offline data from the entire detector and 880 for the luminosity. This amounts to 2080 up links, while one additional down-link is needed per lpGBT for the offline data in order to transmit the fast signals (clock, L0/L1 trigger) to the ASIC. Of the lpGBTs dedicated to offline data, 96 will transmit data at a speed of 1.28 GHz, 496 at 640 Mhz, and 608 at a speed of 320 MHz.

4.4.2 Time walk

The TOA, provided by the ASIC, will be measured with a fixed threshold discriminator and will suffer from time walk dispersion due to the signal amplitude variations[2]. To correct for it, the amplitude of the pulse needs to be measured. The most common way to perform this correction in silicon detectors (with small dynamics) is to measure the pulse width, which

[2] A Constant Fraction Discriminator (CFD) would in theory make the TOA measurement insensitive to the amplitude. However its implementation in an ASIC is quite complex for the performance required by the HGTD. A prototype of the CFD in 130 nm CMOS has been tested, showing a performance similar to the fixed threshold discriminator. Therefore the baseline for the HGTD is a to use a TOT correction



(a) Average number of hits per ASIC.

(b) Maximum number of hits per ASIC.

Figure 4.23: Average and maximum number of hits in each ASIC in one quadrant of the second layer in a simulated sample with $\langle\mu\rangle = 200$. The current simulation is limited to 600 mm while the HGTD design extends up to 640 mm explaining the white areas. The rectangles correspond to the readout rows defined in Section 4.

is proportional to the amplitude, with a TOT discriminator, instead of measuring the amplitude with an ADC. The measurement of the time of the rising edge of the discriminator pulse provides the TOA, while that of the falling edge, combined with the TOA, provides the TOT. Because of the use of a fixed threshold, any offset at the discriminator input needs to be controlled as it might induce a bias of the measured time.

The variation of the TOA as a function of the TOT is presented in Figure 4.24 for an input signal from 1 to 20 MIPs with a 3.5 pF detector capacitance. It is presented for two different types of preamplifiers, voltage (VA, in blue) and transimpedance (TZ, in red). A variation of about 700 ps is observed between 1 and 20 MIPs in both cases, although the TOT excursion is much shorter in the case of the TZ preamplifier (and therefore requires a more sensitive TDC). After correction, the time walk dispersion can be controlled to better than 10 ps, resulting in a negligible contribution to the total time dispersion.

4.4.3 Global architecture of the electronics in the HGTD readout chain

The LGAD sensor module will have an area of 20×40 mm^2 with 1.3×1.3 mm^2 pixels, equipped with two front-end ASICs. An overview of the HGTD readout chain is presented in Figure 4.25.

The path starts on the left of the figure at the ALTIROC ASIC, bump bonded on the sensor, which will read out 225 pixels. It will provide a precise time measurement of each hit in

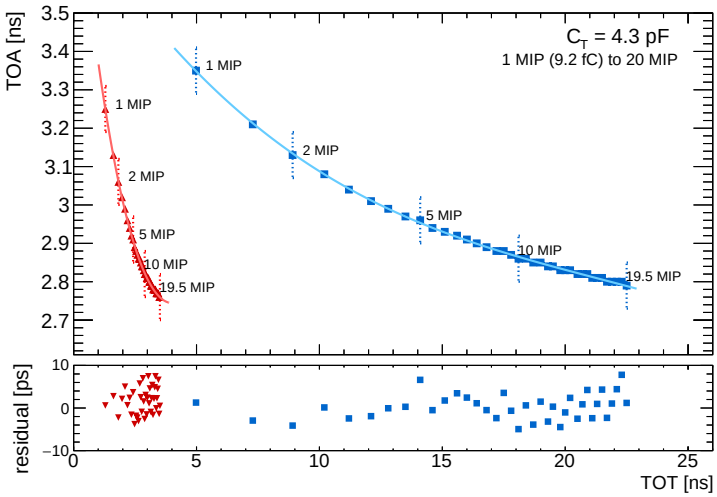


Figure 4.24: Simulation of the TOA as a function of the TOT with a 3.5 pF sensor capacitance and 0.8 pF parasitic (C_T = 4.3 pF) for an input signal from 1 to 19.5 MIPs. Two different preamplifier types are considered: a voltage preamplifier (blue squares) and a transimpedance preamplifier (red triangles). The bottom plot shows the residuals after correction of the amplitude variation.

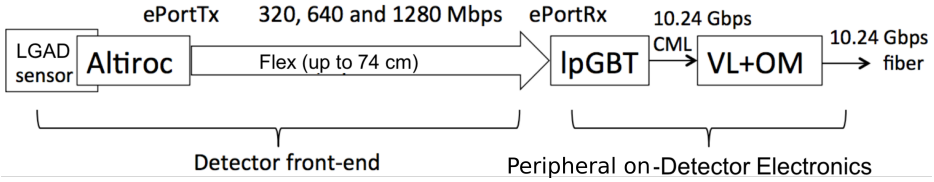


Figure 4.25: Upstream and downstream data flow. The ePortTx is the electrical transmitter protocol, defined by CERN, connecting the ASIC to the lpGBT. VL+OM is the Virtual Link+ on the optical module.

events accepted by the L0/L1 trigger.

The digital output data are transmitted with e-links on flex cables (<700 mm) to peripheral on-detector electronics boards located at the periphery of the HGTD ($R > 700$ mm). Each flex cable serves a module made of two ASICs and contains four differential e-links transmitting data at various speeds (320 Mb/s, 640 Mb/s or 1.28 Gb/s) depending on the ASIC position, to minimise the numbers of lpGBT and optical links. These cables also contain the ASIC low voltage power supplies, the control signals and clock, and the HV lines of the sensors.

Peripheral on-detector electronics boards will be located at $R > 700$ mm and will be based on components already developed for the ITk and Liquid Argon calorimeter Phase II upgrade. A possible implementation of these boards is shown in Figure 4.26. A first board contains two rows of connectors for the flex cables on the top and bottom faces of the

printed circuit board, to fit within a 40 mm width. All input (configuration parameter voltages) and output (data) signals should be routed inside this board to the optical board and the voltage connectors (one individual line per module for the bias voltage + low voltage supplies). In addition this board will also house the DC/DC converters (19 for the longest readout row). The lpGBT ASIC and the optical transmitter (or transceiver) modules developed by the lpGBT and the Versatile Link Plus (VL+) common projects are located on the optical daughter board. The receiving end of this optical link system provides the data to the data-acquisition system through FELIX [34] boards or to dedicated commercial receiver boards for the luminosity information. The size of an event is estimated to be in average 190 kB, with a range between 125 and 250 kB. A down-link to the detector will provide control information to on-detector electronics (ALTIROC and the supporting electronics) such as clock, configuring and control commands, monitoring and triggering signals.

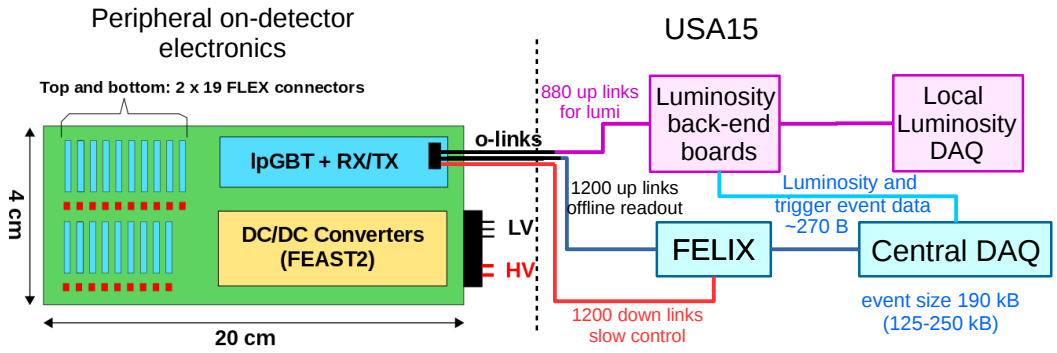


Figure 4.26: Possible implementation of the peripheral on-detector electronics for the longest readout row, and the readout chain. The flex connectors are located on the left; on the top right, the data transmitters and optical modules (lpGBT + VL + OM). The DC-DC converters are on the bottom right, where the low and high voltage connectors are. Three sets of optical links are connected to the lpGBT. The down links for slow control (in red) are connected to the FELIX boards in USA15, as well as the up links for the offline data readout. The up links with the luminosity information go to dedicated back-end boards.

Each ASIC will also provide two integers representing the hit counts in the central time window and the sideband for each event to allow a real-time measure of the luminosity. The information is sent via optical links to the dedicated luminosity processing system in USA15. This consists of FPGA-based luminosity boards that receive the data and aggregate the occupancy information over time, separately for each BCID. Different sums are kept for the narrow and the wide time windows (see Figure 4.22). Two such sums are kept for each of $2 \times 2 \times 4 \times 4 = 64$ regions, given by 2 endcaps with 2 layers each, 4 quadrants per layer and 4 radial divisions per quadrant. The exact number of regions can be tuned later as the implementation will be done in the firmware. The occupancy is aggregated over a time span of 1 second, after which the 128 short integers for each BCID are sent via Ethernet link to the control room for further processing (expected data rate is less than 1 MiB/s). The luminosity processing system will also implement the logics for the minimum-bias trigger using the hit counts as input. These criteria could include a minimum number of

hits globally in HGTD, on one side only, and/or coincidences between layers to suppress noise. The signals representing the decision for each of these criteria will then be sent to the CTP as simple trigger input signals. Per-event occupancy information for each of the 64 regions will be sent to the data-acquisition system for events that pass the L0 trigger. The information will be buffered on the luminosity back-end boards until a L0 accept signal is received. Each of the 128 per-event occupancy numbers will be encoded as short integers (in total 256 bytes of data per event, not including header information). Additional bits representing the trigger signals will also be sent with this data, adding $\mathcal{O}(10)$ bytes to the per-event size.

4.4.4 Front-end ASIC

Each pixel readout channel will consist of a preamplifier followed by a discriminator, both critical elements for the overall electronics time performance. The schematics for the single pixel readout are presented in Figure 4.27. Since the time walk will be measured using the TOT architecture described in Section 4.4.2, two TDCs are necessary. One for the TOA with a bin of 20 ps and a range of 2.5 ns providing 7 bits, and another for the TOT providing 9 bits. The bin and range of the TOT TDC depend on the type of the preamplifier, and will be of 40 ps bin and a range up to 20 ns for the voltage preamplifier, or configured with a 20 ps bin and a 5 ns range for the TZ preamplifier. The preamplifier is further described in Section 4.4.5, and the TDCs in Section 4.4.6. The 16 bits of the time measurement data, combined with 1 bit for a hit flag, are then stored in a local memory (named *hit buffer*). The content of this buffer is processed by a triggered-hit selector circuit on arrival of an L0/L1 trigger signal, so this memory should allow latencies of up to 35 µs. If a trigger signal is received, the information is passed on to a secondary buffer named *matched hit buffer*, where it remains until ready for transmission to the off-pixel common electronics. These local memories are further described in Section 4.4.7.

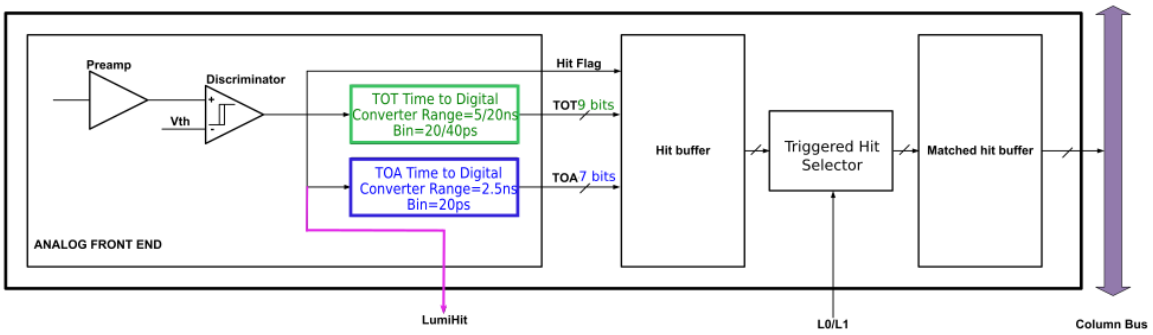


Figure 4.27: Schematic of a single-pixel readout block. The offline data from the TOA and TOT TDCs are stored in a buffer, while the luminosity information is gathered at the ASIC level.

Figure 4.28 shows the conceptual design of the entire HGTD ASIC with 225 channels. Each pixel is 1.3×1.3 mm^2. They are arranged into a matrix of 15×15, with a total matrix size of 19.5×19.5 mm^2. One of the sides of the complete chip will be slightly larger ($\sim$ 22 mm) to accommodate the off-pixel common electronics and the Input/Output pads.

The readout of the pixels is done by column, through an End-Of-Column (EOC) cell. A command decoder unit receives the fast commands and clock signal from the central Trigger Data Acquisition system (TDAQ). These are 8 bits on every bunch crossing, and a 320 MHz clock from which a 40 MHz clock is generated. Based on this, a phase-locked loop (PLL) generates all the different clocks needed to operate the ASIC, namely 320 MHz, 640 MHz and 1.28 GHz. These clock will be centred with an accuracy of $\sim$ 100 ps using a phase shifter, further described in Section 4.4.9.

A control unit handles the readout of the pixel matrix, and will be equipped to handle the bunch crossing identifier (BCID), L0/L1 trigger accept, and reinitialisation commands (to reset the buffers, registers and re-initialise the ASIC). The bunch crossing information is synchronised with the BCID from the TDAQ by the control unit. It consists of 12 bits that must be included in the ASIC to identify the events stored in the pixels. When an L0/L1 accept signal is received by the ASIC, the control unit generates an internal trigger signal and a trigger identifier (TrigID) that are passed to all the pixels. The TrigID is related through a table with the corresponding BCID.

Upon receiving the trigger signal, the control unit requests the EOCs to retrieve and store the data from the pixels. Then it is moved into the Hit Data Formatting module, where it is packed in frames, serialised and transmitted to the peripheral on-detector electronics through e-links. The transmission speed of the e-link will depend on the radial position of the ASIC, and will be set via and Inter-Integrated Circuit bus -I^2C- to one of three values: 320 Mb/s, 640 Mb/s and 1.28 Gb/s. It is connected to an equal speed port in the lpGBT.

Another main function of the control unit is to handle the readout of the luminosity measurement. The output of the discriminator in each pixel is transmitted to the Luminosity Data Formatting unit. Here the 225 channels are summed over two different time windows, the sizes of which are determined through the PLL. The smaller one (S1) is 3.125 ns wide, and is centred at the bunch crossing using the phase shifter described in Section 4.4.9. The larger one (S2) contains S1, and its size can be configured to be a 3.125, 6.25 or 12.5 ns. Both sums (S1 and S2) are sent to a subtractor. The 8 bits of S1 and the 8 bits of the subtraction (S2-S1) are then truncated to respectively 7 and 5 bits to reduce the total bandwidth. These 12 bits, as well as the 4 bits of the header, are then serialised at a rate of 40 MHz in the Data Serializer and sent to the lpGBT through a 640 MHz e-link.

The off-pixel electronics also include several programmable digital to analog converters (DACs) to generate different bias currents for all analog blocks of the ASIC, a band-gap, a temperature sensor (under consideration) and the configuration register. The latter is used to set different features of the ASIC, such as the values of the DACs, the transmission rate of the hit data and the PLL bias currents or frequencies. A configuration register will also

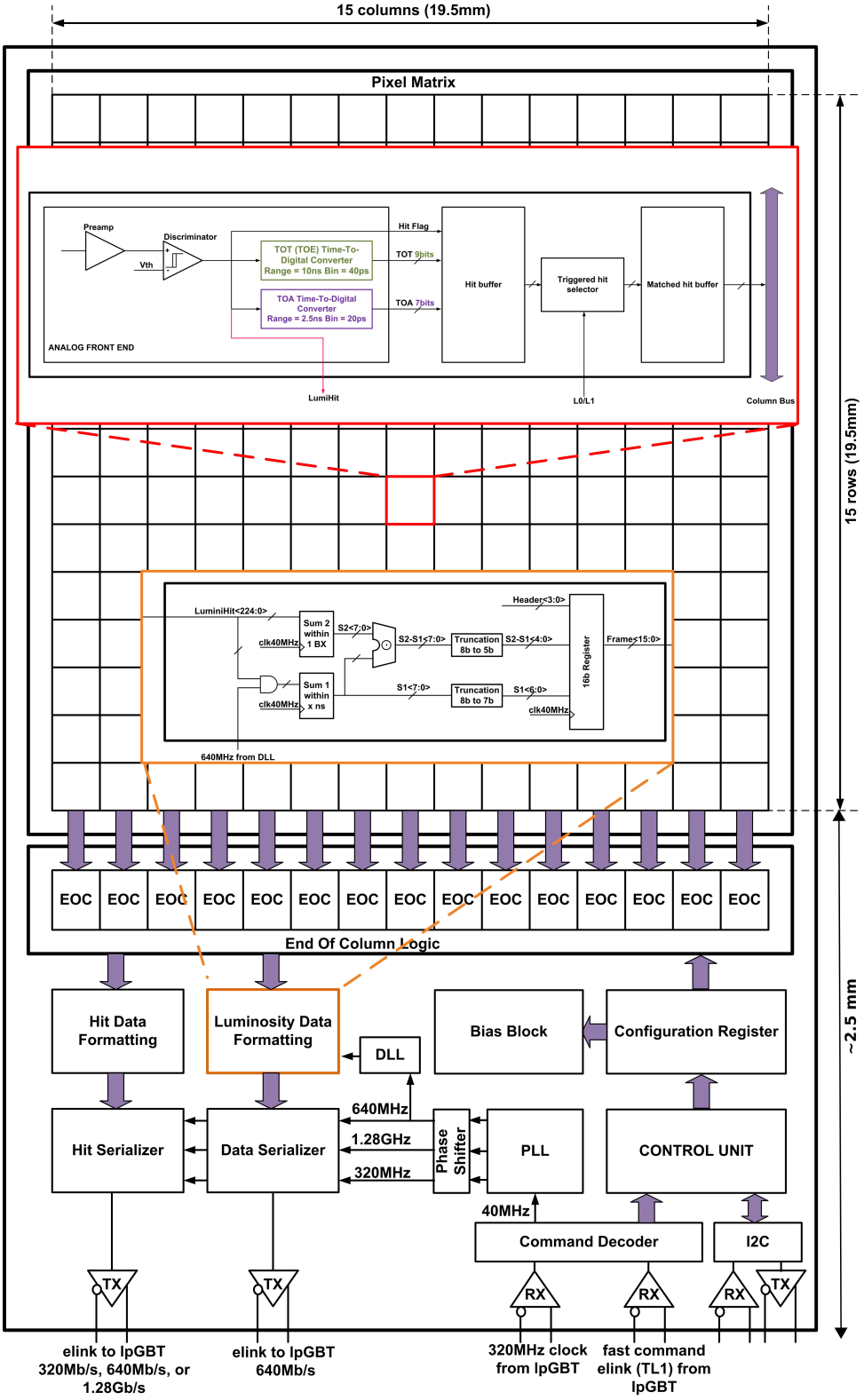


Figure 4.28: Schematic of the full HGTD ASIC. The top part represents the 15×15 pixel matrix, with the single pixel schematics. The bottom part shows the off-pixel modules, including the schematics of the Luminosity Data Formatting unit.

be present in each pixel. The I^2C link mentioned previously is also used to readout all configuration registers in order to check if SEU events have corrupted their content, and to retrieve information from the control unit about the status of the ASIC; the information related to data corruption will be passed on to the hit serializer.

4.4.5 Front-end preamplifier

From an electronics point of view the sensor can be modelled as a transient current source in parallel with the combined capacitance of the sensor and parasitics (which will be referred to as the total capacitance, C_T). When fully depleted, the value of the sensor capacitance is inversely proportional to the sensor thickness and the capacitance value grows with the area. The typical capacitance for a fully depleted sensor is 3.4 pF for a 1.3×1.3 mm^2 sensor with a 50 µm thickness.

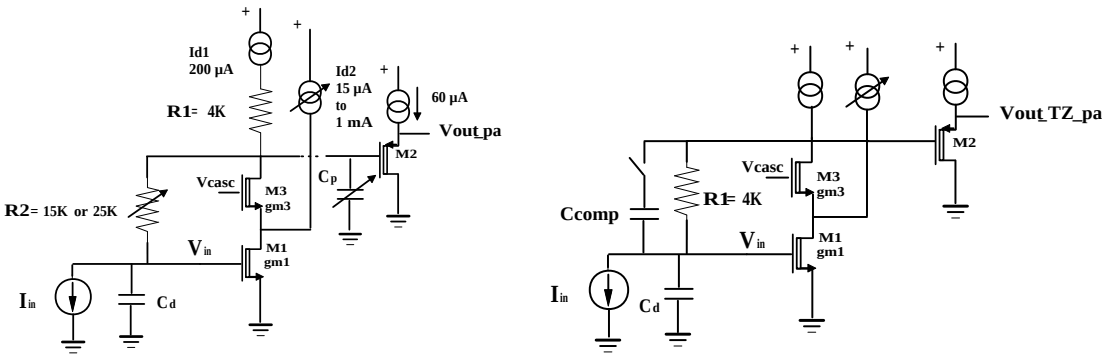
The baseline preamplifier architecture is a broadband preamplifier with a Common Source configuration, consisting of an input transistor ($M1$) and a follower transistor ($M2$), as displayed in Figure 4.29(a). Figure 4.29(b) shows an alternative architecture with a transimpedance preamplifier. In both cases the size of $M1$ and the bias currents are optimised to minimise the noise and the power consumption. The rise time of the preamplifier is optimised to be equal to the drift time of the sensor (t_s ∼0.5–1 ns) in order to minimise the jitter. This minimum jitter is given by :

$$\sigma_{\text{jitter}} = \frac{e_n C_T}{Q_{in}} \sqrt{t_s} = \frac{C_T}{Q_{in}} \sqrt{\frac{2kTt_s}{g_m}}, \tag{4.3}$$

where e_n is the noise spectral density, g_m is the transconductance of the preamplifier input transistor and Q_{in} is the input charge. Both preamplifier architectures, followed by a fast discriminator, have been simulated using the 130 nm TSMC[3] kit provided by CERN with various C_T values and considering that 1 MIP would deposit a 10 fC charge, which corresponds to an amplification gain of 20 in the LGAD. Two input signals were simulated, a calibration signal (to be compared with test bench measurements) and an LGAD-like signal.

The resistor $R2$ (15 K or 25 K) in 4.29(a) can absorb the sensor leakage current, estimated to be between 1 and 2 μA. The leakage current would cause the output of the preamplifier to drift by an amount of the order of $R2 \times I_{leak}$. The threshold of the discriminator that follows the preamplifier must then be changed accordingly. This can be done using the 7-bit DAC threshold correction that is integrated for each channel allowing a correction within ±50 mV.

[3] TSMC stands for Taiwan Semiconductor Manufacturing Company. The technology has been qualified up to 4 MGy [35].



(a) (b)

Figure 4.29: Architecture of the voltage preamplifier (a) and transimpedance (TZ) preamplifier (b) implemented in the latest ASIC design, ALTIROC0_v2.

Figure 4.30 compares the simulated output of the preamplifier and the discriminator for both preamplifier architectures using an LGAD-like input signal. The first two plots show the pulse of the preamplifier (top) and the output of the discriminator (bottom) for the voltage preamplifier shown in Figure 4.29(a). In both cases, two input signals are compared: 5 MIP in blue, and 1 MIP in green. The 5 MIP signal is 5 times larger, has a smaller rise time and larger TOT, which is reflected in the discriminator output, where the blue pulse starts first and is much wider than the green one. This comparison also applies to the two bottom plots, where the same is shown for the transimpedance preamplifier presented in Figure 4.29(b). The 5 MIP signal is shown in red, while the 1 MIP is presented in orange. In addition, it should be noted that the output of this type of preamplifier has a much shorter TOT than the previous one; this is reflected also in the plot presented previously in Figure 4.24. This would allow to reduce the conversion time, but at the same time require higher precision from the TDC.

A first prototype of the ASIC, ALTIROC0_v1, has been designed using the TSMC 130 nm process, and has already been through two iterations. It originally implemented the voltage preamplifier, the TOT and a CFD, but the latter has been removed. The latest version, corresponding to ALTIROC0_v2, contains eight channels, four for each of the preamplifier architectures presented in Figure 4.29. The design of the chip includes also the bump bonding pads, and a first LGAD array was assembled with ALTIROC0_v1 in summer 2017 (see Section 4.2.1), and tested with charged pions at CERN in September. The size of the chip is 3.4×3.4 mm^2 to accommodate the bump bonding to a sensor, but the area used for a single channel electronics is about 200 µm by 100 µm.

The ALTIROC0_v1 chip has been characterised with a single ASIC wire-bonded on a test board. Measurements have been performed using a picosecond generator to provide a voltage test pulse with a rise time smaller than 100 ps. This voltage is then injected through an integrated 100 fF capacitor that can be selected for each channel using the ASIC configuration parameters. This input current signal is faster than a typical LGAD current signal.

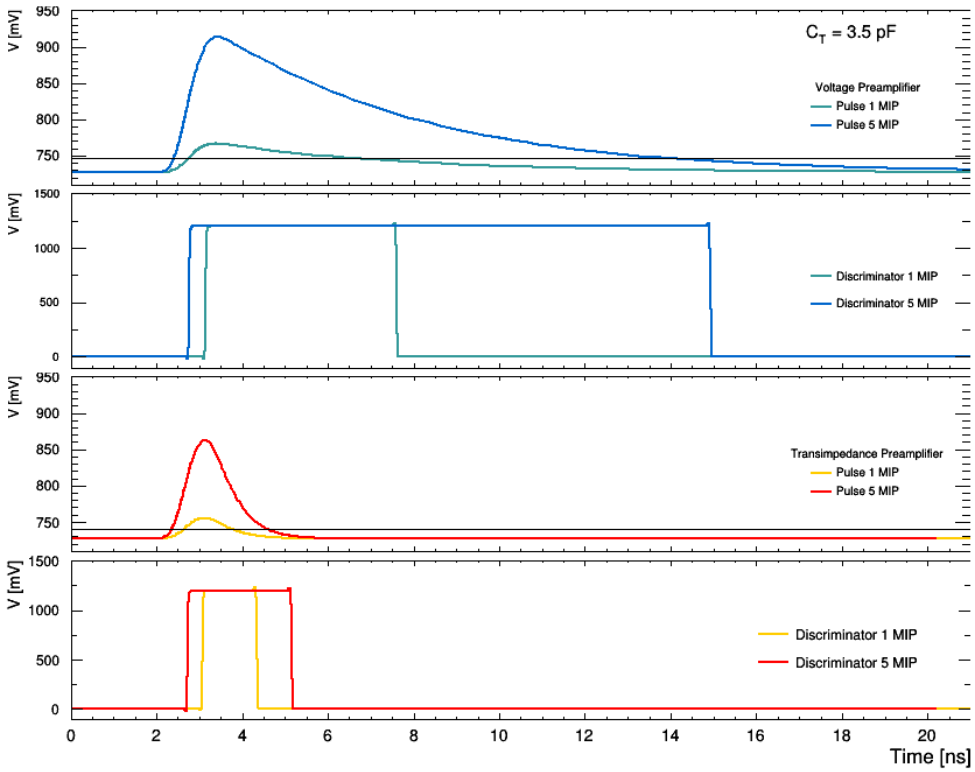
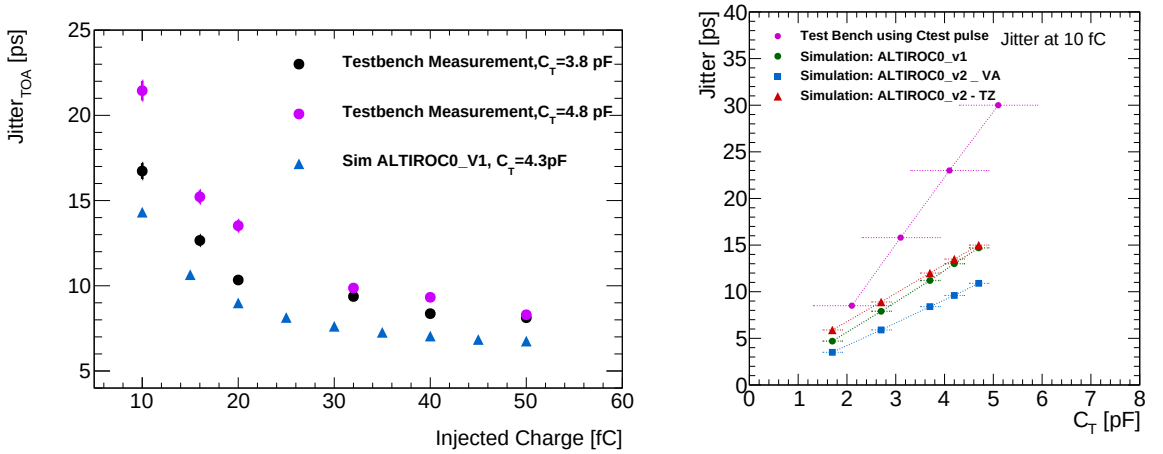


Figure 4.30: Simulation of the voltage preamplifier (top, where blue is 5 MIP and green is 1 MIP) and transimpedance preamplifier (bottom, red is 5 MIP and orange is 1 MIP). For each type of preamplifier, the output pulse is shown first and the discriminator output is shown below.

The jitter performance was measured as a function of the injected charge for capacitances of $C_T \sim 3.8$ and 4.8 pF and is shown in Figure 4.31(a). The total capacitance combines the soldered capacitance (1 or 2 pF) and the parasitics arising from the ASIC and board, which were estimated in this case to be 2.8 pF. The charge injected during the tests was varied from 5 fC to 120 fC. The threshold of the discriminator was set to 5 fC, corresponding to 50% of a MIP in an LGAD sensor with a gain of 20. The constant floor of 7 ps is reached for input charges larger than 20 fC and is attributed to the jitter of the generator. At 10 fC, the measured jitter is 17 ps for $C_T \sim 3.8$ and 22 ps for $C_T \sim 4.8$. The simulation of the jitter is also presented in this plot for the simulation of ALTIROC0_v1, implementing the post-layout view of the circuit (including all the parasitics). A total capacitance of $C_T = 4.3$ pF is used, that combines a simulated sensor capacitance of 3.5 pF and parasitics estimated to be 0.8 pF. The jitter attributed to the generator has been added to the simulation for a better comparison.

Figure 4.31(b) shows the measured and simulated jitter as a function of C_T, using as input a Ctest pulse. The simulations of ALTIROC0_v1 and both ALTIROC0_v2 preamplifiers (voltage and transimpedance) are shown. The total capacitance is obtained as the sum of the simulated sensor capacitance (or soldered in the case of the measurement) and the par-



(a) Jitter as a function of input charge.

(b) Jitter as a function of total capacitance (C_T).

Figure 4.31: (a) Simulated and measured jitter as a function of the input charge in ALTIROC0_v1. (b) Jitter as a function of C_T measured in testbench for ALTIROC0_v1 and simulated for ALTIROC0_v1 and ALTIROC0_v2. The value of C_T is obtained combining the soldered capacitance (sensor capacitance in the simulation) and the parasitic capacitance. The horizontal error bars correspond to the uncertainty in the parasitics.

asitics, which are (2.1 ± 0.8) pF in the measurement and (0.7 ± 0.2) pF in the simulation. The generator contribution of 7 ps has been subtracted. The jitter increases linearly with the detector capacitance, but with a different slope for each case. The difference between the measurement and simulation of ALTIROC0_v1 can be mainly attributed to the different noise in the simulated ASIC (1.2 nV/$\sqrt{\text{Hz}}$) and the measured ASIC+board (1.7 nV/$\sqrt{\text{Hz}}$). For $C_T \sim 3.5$ pF a jitter smaller than 15 ps is obtained for 10 fC (LGAD gain of 20). The simulation of the voltage preamplifier in ALTIROC0_v2 shows a smaller slope, which points to the possibility of improving the jitter performance of the modules prototype in the next iteration.

The measured power consumptions of the preamplifier and of the discriminator are 420 µW and 375 µW respectively.

Preliminary test beam measurements have shown resolution values of around 42 ps for the current combination of sensors and electronics. Additional test beam measurements are planned for 2018.

4.4.6 Time-to-Digital Converter

The Time-to-Digital Converter (TDC) is designed using TSMC 130 nm technology. The target timing resolution (quantisation step) of 20 ps is below the gate-propagation delay in

130 nm technology, thus the Vernier delay line configuration is employed. This configuration consists of two lines (see Figure 4.32), each composed of a series of delay cells implemented as differential shunt-capacitors, controlled by a voltage signal that determines their delay.

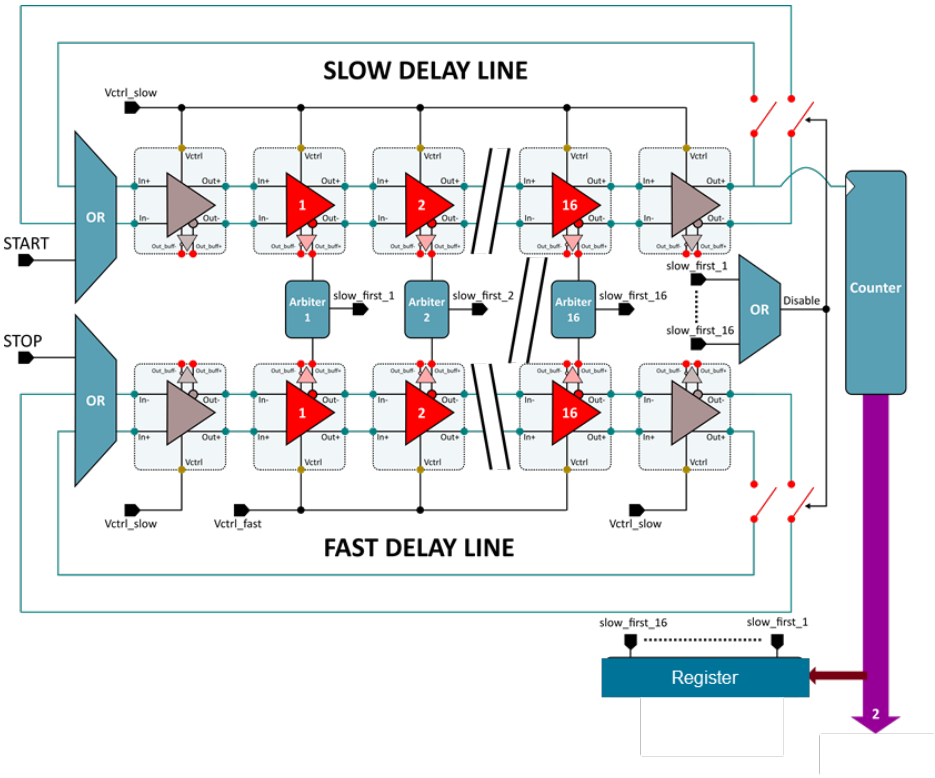


Figure 4.32: Schematics for the TDC showing the 'slow' delay line and the 'fast' delay line. The 20 ps speed difference between the two is used to provide the 20 ps time measurement bins.

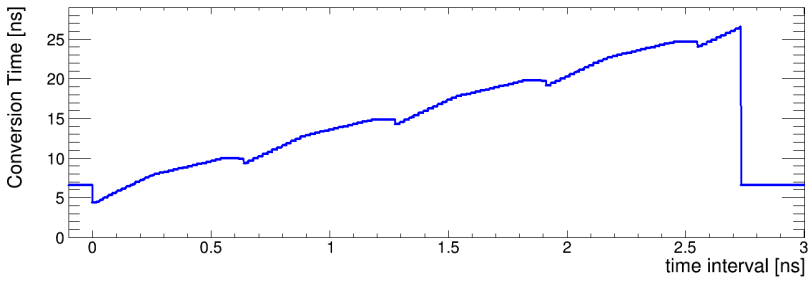
The timing resolution is determined by the difference in the delays of the cells in each line. In the 'slow' line, the control voltage fixes the delay of each cell to 140 ps, while on the 'fast' line it fixes it to 120 ps. The START signal (output of the discriminator) enters the 'slow' delay line while the STOP signal (end of measurement window) enters the 'fast' delay line. Although initially the START signal is ahead of the STOP one, each delay-cell stage brings them closer by an amount equal to the difference between the slow and fast cell delays, i.e. 20 ps. The number of cell stages necessary for the STOP signal to surpass the START signal represents the result of the time measurement with a quantisation step of 20 ps. A cyclic structure is employed to reduce the number of cells per line and results in a smaller occupied area. Since the time measurement is initiated only upon signal detection (instead of at each time-measurement window), the reverse START-STOP scheme is used as a power-saving strategy.

The TOT TDC will employ an additional coarse delay line for extending the range to 20 ns, while the Vernier delay line (identical to the one used in TOA TDC) will provide high

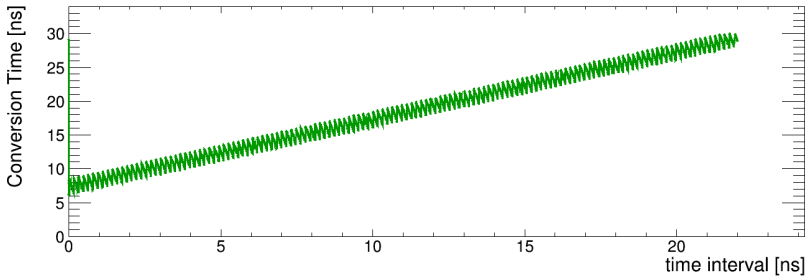
resolution. For the voltage preamplifier, the TOT TDC will be configured for 40 ps resolution and 20 ns range, while for the TZ preamplifier the TOT will be configured with 20 ps resolution and 5 ns range.

The TDC power consumption is dependent on time-interval being measured. For the TOA TDC with 2.5 ns (full dynamic range), the average power consumption over the 25 ns measurement period is about 5.2 mW. It will become 3.5 mW for the time-interval equal to half dynamic range. Thanks to the reverse START-STOP operation, the power consumption of the TDC is much lower in the absence of a hit over threshold. This results in an average power consumption per pixel of 0.4 mW, assuming a time interval uniformly distributed (1.25 ns average) and a maximal pixel occupancy of 10%. The average power consumption for the TOT TDC is 0.5 mW and 0.36 mW for voltage and TZ preamplifier configurations respectively.

Simulations of both the TOT and TOA TDCs have been implemented; the simulated conversion time as a function of the time interval is presented in Figure 4.33. The TOA TDC (Figure 4.33(a)) was simulated for a time range of 2.7 ns; the conversion time of a time interval of 2,5 ns is 25 ns. The simulation of the TOT TDC for voltage preamplifier (Figure 4.33(b)) shows that the conversion time for a time interval of 20 ns is $\sim$ 28 ns. These are preliminary results and studies are ongoing.



(a) TOA TDC



(b) TOT TDC

Figure 4.33: Simulation of the conversion time for the TOA TDC (a) and the TOT TDC (b).

4.4.7 Local memory

Each pixel electronics is composed of an analog part, already described, and a digital part. The purpose of the digital part is to temporarily store the data related to a hit and select hits of events that have been triggered, or, in other words, skip the stored hits that are not associated to a trigger. The hit buffer is the one that first receives the 16 bits of data (7 bits TOA and 9 bits TOT), and can be implemented in two different ways:

- **Full buffering**: at each bunch crossing, the pixel bits (TOA,TOT, hit flag) are loaded, although if no hit is present only the hit flag is stored. It therefore requires a memory position per bunch crossing, which amounts to a depth of 1400×17 bits to cope with the L1 latency of 35 µs.
- **Partial buffering**: the TOA and TOT of a pixel is stored only if there is a hit. In order to assign a hit to a specific event, the 12 bits of BCID must be added. Given that the average number of hits per pixel in 35 µs is 210, an estimation of the depth of such a memory starts at 210x28b. In principle a partial buffer would then be approximately 4 times smaller than a full buffer.

For each received trigger, the triggered-hit selector checks if there is data in the hit memory associated to that event. If there is, it is loaded into the matched hit buffer with a TrigID supplied by the control unit. This identifier allows to know which trigger event the data stored in the matched hit buffer are associated to.

The way that the triggered-hit selection is carried out depends on the hit buffer implementation. A full buffer would need to be implemented as a circular memory, allowing to store data in a continuous way for each bunch crossing. It has two memory pointers for reading and writing. The latter is incremented from position 0 to 1399 during 35 µs, and then goes back to position 0. The reading pointer is managed by the triggered-hit selector, which transfers the TOA and TOT information if when receiving a trigger it finds a hit flag equal to one.

A partial buffer could be implemented as a simple "first-in-first-out" (FIFO) memory. The triggered-hit selector would handle its content by continuously comparing the BCID of the outcoming data with a delayed copy of the BCID in the ASIC (the delay should equal the trigger latency). When the internal and external BCID match, and a trigger is received, it transfers the data to the next memory.

The matched hit buffer operates as an average rate memory. It will allow to cope with event-to-event fluctuations in the number of matched hits and to keep the bandwidth of the ASIC lower than 1.28 Gb/s. Matched hits are stored there until they are read by the control unit and passed to the hit data formatting module. Studies are ongoing to optimise its design.

An implementation in 130 nm CMOS and a simulation of a local 17×400 SRAM (10 µs latency) has been done, with a standard 6T cell configuration. Assuming a 10% maximal

occupancy, the average power consumption of the pixel local memory is 57.2 µW. For a 1400 depth SRAM, a power consumption 1.5/2 times higher is expected; the increase is related to the fact that the memory should be divided in multiple banks.

4.4.8 Matrix readout process

When the command decoder receives a trigger command, this is immediately passed to the pixel matrix as well as the corresponding TrigID. Simultaneously, the BCID and the TrigID are loaded into the trigger table. Events stored in the table are managed by the control unit. However, it might happen that the table be full. In that case, the control unit would generate an error message that would be transmitted to the TDAQ through the I^2C link. For each fetched entry in the table, the control unit initiates the readout of the pixels associated to that trigger. The process works as follows:

1. the TrigID is passed to all pixels as a requested trigger ID (RqtTrigID).
2. a circuit on-pixel checks if there is a matched hit with the same trigger ID than the requested trigger RqtTrigID. If there is, a hit flag on-pixel is asserted
3. only pixels with asserted matched hit flag are readout. The data plus the address of the read pixels are load into buffers placed at the end of column. When the data of a pixel has been read, the hit flag is de-asserted.
4. the end of column buffers are read by the control unit. The column address is added to each data read from one of the buffers. Data are passed to the hit data format circuit where the frames for transmission are built and serialised.
5. once all the pixels with a matched hit associated to the requested trigger ID have been read, that event is removed from the table, the next trigger event stored in the trigger table is read and the process starts again.

4.4.9 Phase shifter

The phase shifter is a function block located in the off-pixel electronics used for the adjustment of the clock phase for the clock system in the ASIC. It receives the clock CMOS signals of different frequencies (320,640 and 1280 MHz) generated by the PLL and outputs them with the same frequency but with an adjusted phase. This module is required to provide a shift step smaller than 100 ps, and additional jitter below 5 ps, and a power consumption around 10 mW.

The design presented here is adapted from an lpGBT designed in the 65 nm process. As can be seen in figure 4.34, the core of the phase shifter is a delay-locked loop (DLL) in which the delay line is used to delay the input clock signal. The 640 MHz clock signal reuses the delay line of 16 delay cells (not included the dummy cell at the end of the delay line) in

the DLL. The 320 MHz clock signal is delayed in other two delay lines that are controlled by the DLL. Two coarse phase adjustment circuits are needed for these two clock signals to keep the delay line length of 16 delay cells. The time resolution is 1/16 of the 640 MHz clock period, equal to 97.6 ps.

An estimation of the performance of the phase shifter is presented in figure 4.35 based on a previous version of the design that shared the same delay cell, charge pump and phase detect as the current one. The DLL used had 32 cells instead of the proposed 16. Figure 4.35(a) shows the jitter as a function of the selected phase for the cases with the highest and lowest jitter found. The maximum value remains below 1 ps. Figure 4.35(b) shows the delay time as a function of the selected phase for the same two cases presented previously. The maximum variation found is of 1 ps. The power consumption is 8.4 mW in the typical case in the previous design. The clock phase inaccuracy caused by mismatch of the delay cells is found to be no more than 3 ps (RMS) in the mismatch simulation. It is estimated that the new design will have a similar jitter phase accuracy performance; the power consumption would be of around 13 mW because it will have 3 delay lines. New studies will be available soon.

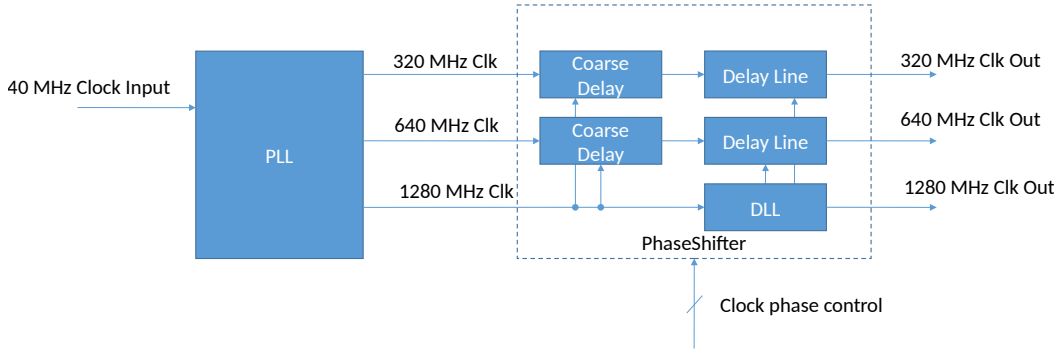
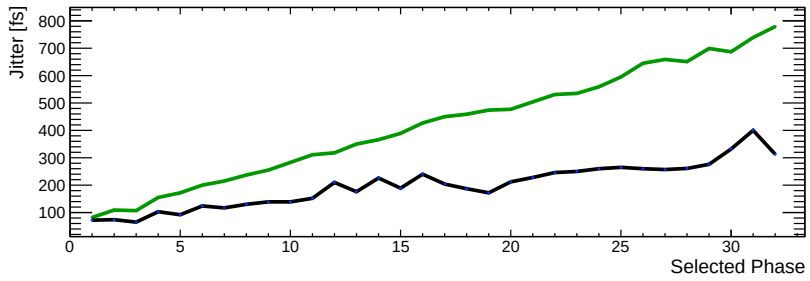


Figure 4.34: Top-level diagram of the proposed phase shifter

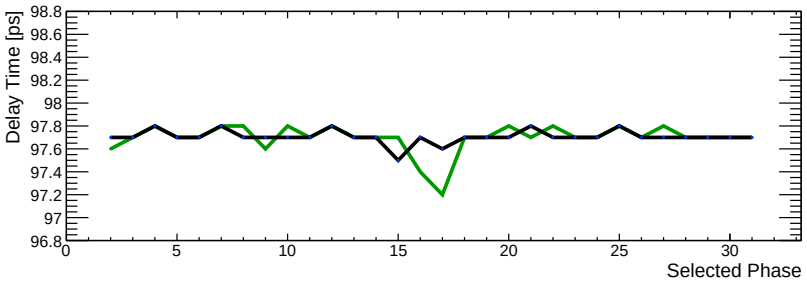
4.4.10 Power consumption of ASIC

Table 4.5 summarises the average power consumption of a single pixel electronics assuming 10% occupancy corresponding to the inner radius ASIC (worst case) . The values presented here have been estimated using simulations. The nominal single-channel power consumption is 2.66 mW.

In addition to the 225 single pixels, the power dissipation of the other ASIC blocks (hit formatting cell, rate average FIFO, PLL, clock distribution, etc...) has been estimated to be 100 mW. The estimated power consumption of the phase shifter is estimated to be around 13 mW. With a 10% occupancy the nominal power consumption of the entire ASIC is 700 mW, within the requirements of 1200 mW (300 mW/cm^2). Using the expected occupancy as a function of the position of each ASIC, the total front-end power consumption for



(a) Clock jitter.



(b) Phase accuracy.

Figure 4.35: Simulation of the jitter (a) and the phase accuracy (b) of the phase shifter. The simulation is shown for the cases with maximum and minimum jitter.

one HGTD layer is 2.1 kW. A more detailed study is presented later in Figure 5.2, where the power dissipation of the modules is shown as a function of the radius, taking into account the average number of hits expected.

Component	**Nominal [µW]**
Preamplifier	462
Discriminator+DAC	375
TDC TOT (10ns/40ps)	500
TDC TOA (2.5ns/20ps)	405
Local Memory	920
Total Pixel	2666

Table 4.5: Single-pixel average readout power consumption. For the TDC and local memory (full buffer option), a 10% occupancy factor is applied.

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4.4.11 Radiation hardness considerations

As stated before, the ASIC will have to withstand high levels of irradiation, up to 4.1 MGy (at $R = 120\,\text{mm}$). Several considerations are being taken into account regarding the design of

the chip. For example, in order to reduce the sensitivity to leakage currents of the TSMC CMOS 130 nm, only relatively large transistors and currents will be used in the analog readout circuit. In addition, a large number of substrate contacts will be used to avoid latch-up (SEL) and transistors with low voltage thresholds are avoided in current sources. Concerning the digital part of the chip, standard cells from the CERN library will be used, each enclosed with a strong substrate contact. No minimum size transistors will be used.

Irradiation tests will be performed on the second prototype of the ASIC, ALTIROC1, during the end of 2018/beginning of 2019. The tests will allow to check if it is necessary to switch to enclosed transistors in the analog part. ALTIROC1 will contain two variants of the SRAM, one with transistors of standard threshold voltage and the other with high threshold, and both will be tested for radiation resistance. Another important test for the memory will be to measure the SEU/SEL rates, although these tests will need to be repeated with the final version of the ASIC. This final version will have triple voting (I^2C) integrated, so as to implement an automatic correction for SEUs.

4.4.12 ASIC development next steps

The following steps are expected up to the final chip design:

- The ALTIROC0_v1 ASIC first performance was satisfactory, but presented some shortcomings. Several improvements have been implemented in ALTIROC0_v2, reducing the noise level, increasing the preamplifier bandwidth, and testing an alternative preamplifier architecture.
- A 25 channels chip containing both the analog (preamplifier + discriminator) and digital (TDC + local memory and possibly clock phase shifter) parts of the single pixel readout will be submitted in June 2018. The schematics of the elements implemented in ALTIROC1 are presented in Figure 4.36. It will contain variants for the architecture of the TDC and the preamplifier, as well as an "on-chip calibration module" (or pulser), the purpose of which is to calibrate the absolute value of the phase of the external clocks that are used by the TDCs. This chip will be bump bonded to a sensor and is expected to validate the single pixel readout chain with intensive characterisation before a TDR. Simulation of the data formatting and memory is being performed in parallel but will not be included in this circuit.
- A first submission of the final chip is expected in the spring of 2019, and a second iteration can be encompassed in the project schedule.

4.4.13 Clock distribution and calibration

The TDCs implemented in the HGTD sensor readout ASIC ALTIROC use an external clock signal, of (a multiple of) the 40.079 MHz LHC bunch crossing clock. The clock signal must

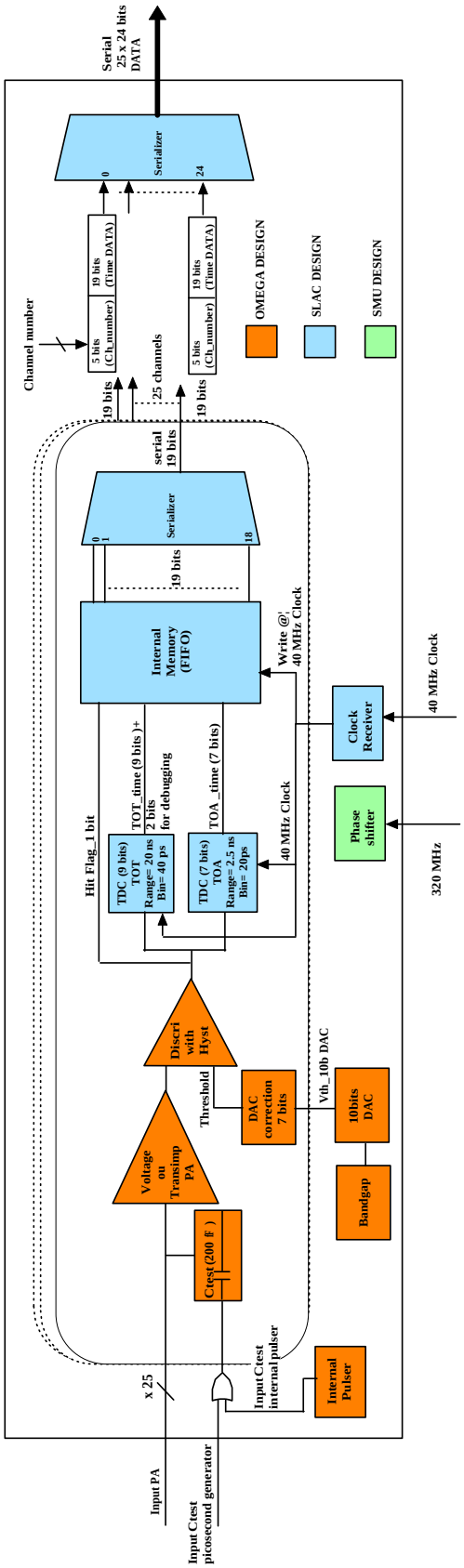


Figure 4.36: Schematics showing the design of ALTIROC1.

be stable and in phase with the average bunch crossing time as given by the machine. To avoid affecting the timing resolution of the detector (30–50 ps/sensor), the short-term (bunch to neighbouring bunch) RMS phase-jitter of the clock should be well below 5 ps. The same restriction applies to the long-term peak-peak jitter (*drift*) over periods equal or larger than a millisecond. In particular, the phase jitter and drift between the clocks of different ASICs should respect such limits.

It should be noted that phase *stability* rather than the actual phase value is of importance, because it is foreseen that the time offset of the individual channels can be measured and corrected to first order by a dedicated calibration procedure, and subsequently fine-tuned with the actual event data.

For each readout row, an electrical clock distribution must be implemented for several reasons. First, the space available precludes the use of optical-fibre receivers at individual ASICs; secondly, optical clock receivers and fibres would receive an intolerably high radiation dose at smaller radii; and lastly, for reasons of cost. With temperature fluctuations of O(1 K) and distances of O(1 m), copper lines can be used.

The LHC clock will be distributed in USA15 using a low jitter clock fan-out circuit, and then to the lpGBTs. Currently, the AFP collaboration [36] is successfully using the On-Semi NB7L series of clock fan-out buffers with $\leq$ 65 ps rise time and 0.2 ps RMS random jitter. A collaboration is being set up in CERN EP/ESE with both ATLAS and CMS to develop the best clock distribution scheme. The frequency-adjustable but fixed-phase clock output of the lpGBT will be used to distribute the clock to each ASIC. They are expected to have a jitter smaller than 5 ps. The phase of these clocks, as previously explained, will be adjusted internally in the ASIC with the phase shifter described in 4.4.9.

The time of arrival of a hit measured in the HGTD will be different between pixels and will need to be calibrated to keep the expected time resolution of 30–50 ps per pixel. The origin of the variations of the measured time can be static (radially dependent time of flight, signal/clock distribution in the ASIC and in flex cables of different length) or time dependent (day/night variation of the LHC clock if not centrally corrected in ATLAS). For instance, the current LHC clock shows a slow day/night drift of about 200 ps; not correcting such an effect over an LHC fill could induce 50–60 ps time dispersion.

Figure 4.37 shows the inclusive time distribution of hits in a simulated $Z \rightarrow e^+e^-$ sample. It shows a Gaussian core derived from the time dispersion of the LHC collision ($\sim$250 ps) with tails from particles with longer paths, e.g. low-p_{T} particles from displaced decays of long-lived SM hadrons, or loopers. With 10000 hits per pixel, a precision of a few ps per pixel can be easily reached. This would translate into 10^5 (10^6) events to be recorded at inner (larger) radius. With a few kHz data taking, such a time offset correction per pixel could be calculated online about every 10 minutes at the nominal HL-LHC luminosity. For a global shift as induced by the LHC clock, one can build the time distribution using all the pixels connected to the same clock (two ASICs, i.e 550 channels), and monitor faster time drift.

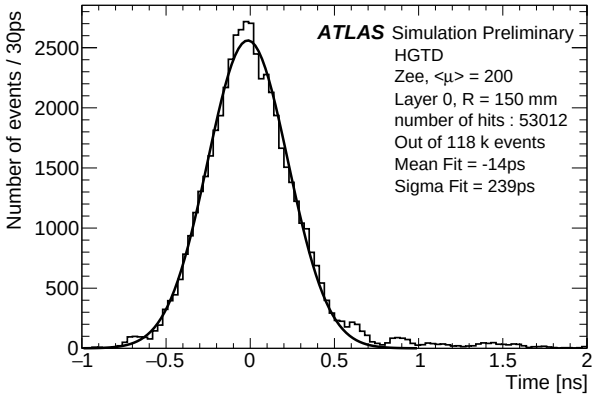


Figure 4.37: Hit times at $R = 150$ mm in $Z \to e^+e^-$ events. Hits in 9 pixels are used to increase the statistics. The small bias of the peak stems from the time reconstruction method.

The TOT, affected by the gain degradation under irradiation, will be monitored by the same set of data.

4.5 Outlook and path towards TDR

The R&D activities are expected to continue up to the end of 2020 with the following main milestones to be achieved before the TDR is delivered in Q1/2019 :

- The production of new sensors for 2018 has been launched both at HPK and CNM and the devices should be available over summer. A similar mask is used by each producer in order to make a direct comparison of the performance. The aim is to optimise the edge/interpad structure, to produce larger-size sensors and study their performance before and after irradiation. A decision about the sensor thickness (35 or 50 µm), the pad size and the sensor size (40×20 or 40×40 mm^2) is expected to be taken for the TDR.

- A full validation of the one-pixel readout (preamplifier+discriminator+TDC+local memory) performance should be demonstrated using the ALTIROC1 prototype to be submitted in June 2018. Test bench measurements to characterise the ASIC will be done over Q4/2018 and Q1/2019. In parallel the specifications of the final chip should continue with a preliminary design review to be organised in Q1/2019. A conceptual design of the peripheral on-detector electronics and of the bias voltage and low voltage distribution should be achieved.

- Flex cable prototypes will be produced before summer 2018 and their performance validated (data transmission, high-voltage distribution, ...). The ALTIROC1 ASIC

will be bump-bonded to HPK and CNM sensors and β source measurements could be done over Q1/2019, but not in test beam measurements before the TDR.

- A prototype of the clock distribution will be built and is likely to be installed before the beginning of Run 3. The goal is to demonstrate in-situ the stability of the clock distribution.

5 Detector installation and infrastructure

This section describes the design of the detector vessel, cooling system and the integration of HGTD in ATLAS. As discussed previously, the space allocated to the HGTD is very limited and constrains many of the HGTD engineering parameters. The detector design must allow easy and fast integration into the ATLAS detector, and enable repairs and a partial replacement during LHC shutdown periods. The present design consists of a single cylindrical cold vessel per endcap, with the module layers inside. The overall dimensions of this vessel have been presented in Table 2.1, with a more detailed description of the size of each component in Table 4.3. In addition, the routing of the services should be in the gap of 50 mm against the endcap wall.

The different components of the hermetic vessel are presented in Figure 5.1. The full detector thickness in z including supports, front and rear cover is 75 mm, plus 50 mm of moderator to protect the ITk and the HGTD from the back-scattering neutrons originating from the endcap calorimeter. The moderator is divided into two disks, as can be seen in the drawing. The HGTD cold vessel will be located at the z position of 3420 mm $< z <$ 3545 mm from the interaction point while the first and last active layers will be located at $z = 3435$ mm and $z = 3485$ mm. The total weight per endcap is approximately 350 kg, of which 70 kg comes from the moderator inside the vessel.

5.1 Cooling system

The HGTD cooling system will be based on a 2PACL-CO2 (two Phase Accumulator Controlled Loop of CO2), that will be integrated into the general cooling system developed for the ATLAS ITk detector [4]. The CO_2 is pumped in liquid state from an external primary chilling source and partially evaporates as it absorbs the heat dissipated by the HGTD components. Within each pipe, a small amount of CO_2 flows at high pressure in the form of small drops, and enough space is left for the vapour to circulate. A highly efficient heat extraction is achieved by making use of the large latent heat for a liquid to vaporise, meaning that not only less fluid is needed to extract a certain amount of heat, but also that the temperature of the liquid phase remains constant, while that of the vapour increases only slightly. The cooling power is then determined by how much CO_2 is left in liquid state. Because it is used in mixed states (liquid and vapour), a significant mass reduction is introduced when comparing with other liquid mono-phase refrigerants. Logically, the piping

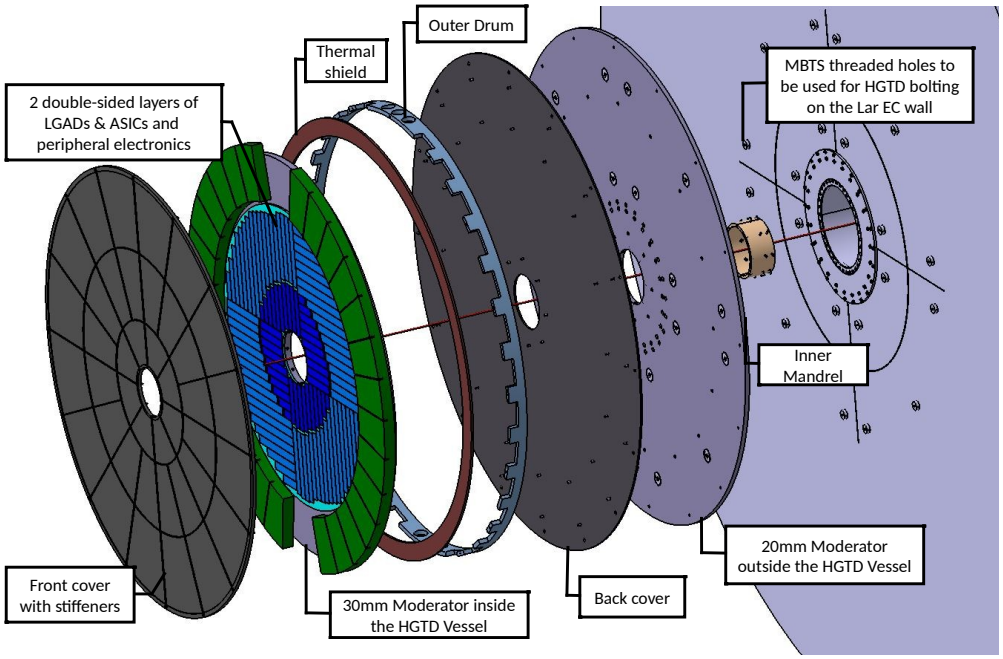


Figure 5.1: Global view of the various components of the hermetic vessel and moderator, excluding the cooling plates and the detector components assembled in them.

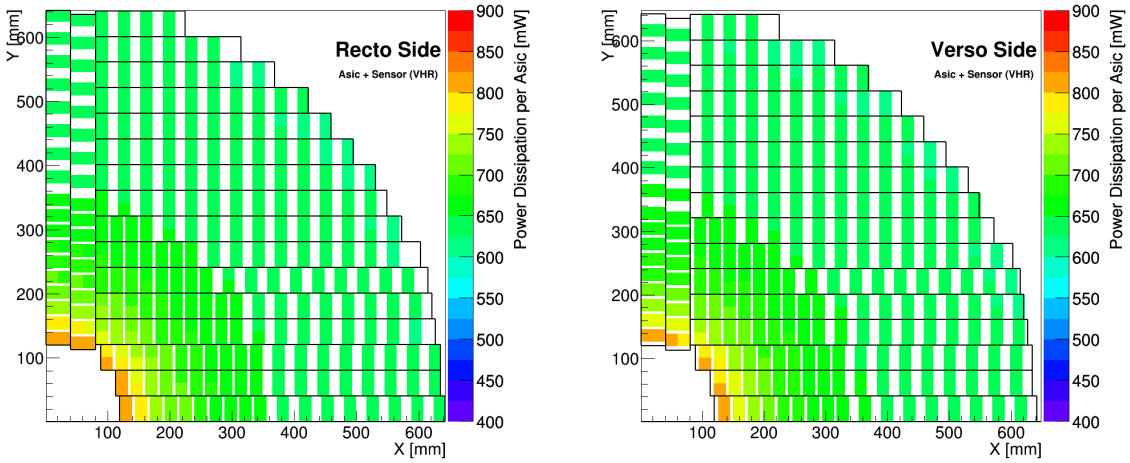
diameter can also be smaller, which is an additional benefit given the reduced space available for the detector. Lastly, CO_2 cooling is radiation hard, and is thus appropriate for the harsh environment the HGTD will operate in.

5.1.1 Requirements

An operation temperature of −30 °C must be maintained inside the HGTD vessel, close to the modules, with a stability of few degrees. As discussed in Section 4.3, the need to keep the operating temperature as low as possible arises because, after irradiation, the leakage current of the sensors increases with temperature (by a factor of 2 for every 7 °C). These conditions will limit the heat dissipation and ensure the good performance of the sensors.

The power dissipation of the modules was studied as a function of their position, taking into account the ASICs (with the average number of hits as shown in Figure 4.23) and the sensors in VHR mode. The results are presented in Figure 5.2, separately for each side of the cooling plate. The modules at the innermost radius present the largest power consumption, 820 mW per ASIC area (205 mW/cm^2), with 700 mW coming from the ASIC. The values

decrease as a function of the radius, reaching 625 mW per ASIC area (156 mW/cm^2) at the outer radius.



(a) Front side of cooling disk.

(b) Back side of cooling disk.

Figure 5.2: Power dissipation of the ASIC and sensor combined, shown per ASIC, for each side of a cooling disk.

Table 5.1 shows a breakdown of the power consumption estimated for the various components of the detector, which define the maximum cooling power needs (25 kW in total, i.e. 12.5 kW per endcap). The ASICs will be the component with the highest power consumption, reaching 175 mW/cm^2 at the innermost radius. The expected power consumption of irradiated sensors at 3.7×10^{15} n_{eq}/cm^2 running at a temperature of $-30\,^{\circ}$C is < 30 mW/cm^2 for the entire radius range. This corresponds to the maximum irradiation expected in the sensors considering a replacement of the inner part of the HGTD detector ($R < 320$ mm) after half of the HL-LHC program and including the appropriate safety factors (as summarised in Section 2.3). The power consumption of the peripheral on-detector electronics has been computed assuming a 70% efficiency for the DC/DC converters. The table also shows an estimate where power consumption of the ASICs, the flex circuits and of the peripheral on-detector electronics have been computed including a safety factor of 1.5 with respect of the ASIC power consumption. This factor is applied to take into account possible larger occupancies and calibration tests in which many pixels would be fired simultaneously.

The operating temperature of the peripheral on-detector electronics is quite flexible and can be in the range of $-30\,^{\circ}$C up to $20\,^{\circ}$C, making the cooling and stability requirements of these components much less strict. Taking into account that these electronics are located within the cold vessel, they will need to be maintained at a temperature close to the sensor operation point to avoid excess heat flowing towards the sensors.

5.1.2 Cooling design

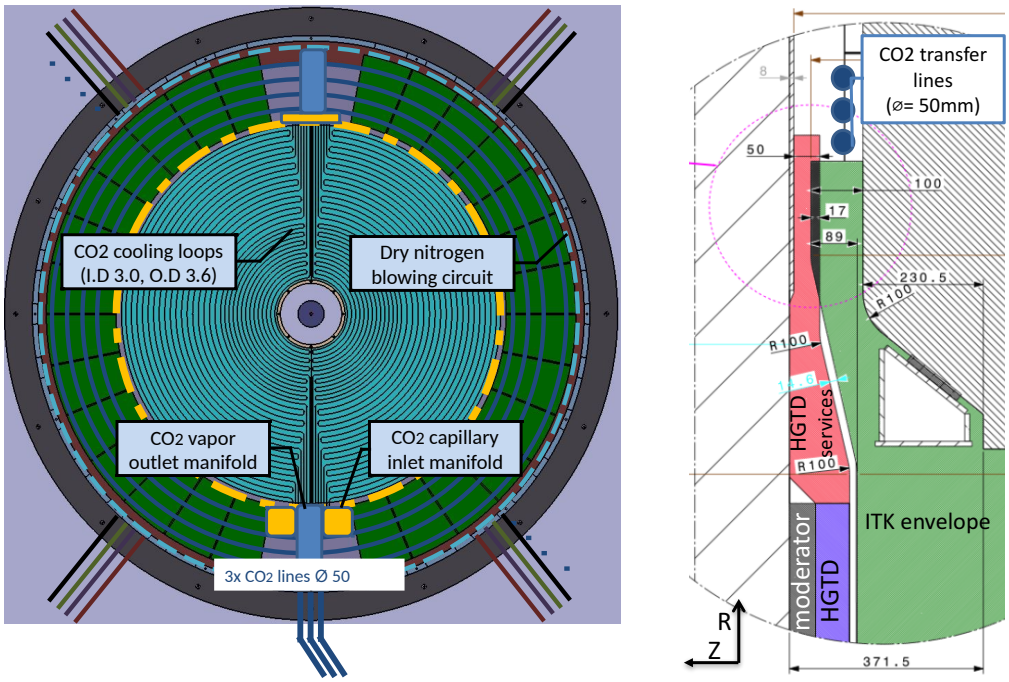
The cooling layout is illustrated in Figure 5.3(a), including all inlet-outlet manifolds and transfer lines located at the top and bottom of the detector. Based on the technology used for the ATLAS Insertable B-Layer detector and industrial standards, tri-axial stationary vacuum insulated rigid transfer lines will be used. Two transfer lines are dedicated to the module cooling and a third one provides the cooling of the peripheral on-detector electronics.

Liquid CO_2 flows from the transfer lines into the capillary pipes (shown in yellow in the drawing), which have an inner diameter of 0.75 mm, and are up to 3 m long. These capillary pipes supply the 7 cooling loops embedded in each half-disk cooling plate. The cooling loops are positioned in a concentric half-circle layout. The distance between the loops at $R > 320$ mm is 20 mm. For $R < 320$ mm it is reduced to 15 mm in order to take into account the larger heat dissipation (modules with 80% overlap), thus keeping a uniform temperature distribution. The characteristics of the pipes in the cooling loops are guided by the suggestions of the CERN Cooling group (EP-DT-FS). They will be made of stainless steel 304L; a non-magnetic, easy for manufacturing, bending and welding material. The wall thickness is set to be 0.3 mm, which should sustain the CO_2 high pressure level (the cooling system has safety release valves at 130 bar; to be tested according to CERN safety factor rules). The inner diameter will be of 3.0 mm, and the length should be in the range between 4 and 6 m. The average transfer capacity of such loops is thus 100 W/m, fulfilling the previously discussed requirements. Standard stainless-steel fittings are proposed for testing prior to installation.

The plan is to bring in fixed cable trays the three transfer lines per endcap of about 5 kW and 50 mm outer diameter each as shown in Figure 5.3(b). The possible location of these connections is marked in light blue in the photograph presented in Figure 5.4, where the side of the endcap cryostat is seen. During shut-down periods, in the opening/closing procedure of the endcap calorimeter, these cooling transfer lines will be temporarily disconnected/reconnected through a compact junction box to be located at $z \approx 8$ m. The connec-

Component	Power consumption	Total [kW]	Maximal [kW]
Sensor	< 30 mW/cm^2	1.9	1.9
ASIC	<175 mW/cm^2	8.5	12.8
Flex cable	< 100 mW/flex	0.5	1.1
HGTD cold vessel heaters	75 W/m^2-175 W/m^2	0.33	0.33
EC calorimeter cryostat heaters	120 W/m^2, 50% up to $R = 1600$ mm	< 0.6	0.6
Peripheral on-detector electronics	dominated by DC/DC converter	3.25	4.9
Total for CO_2 cooling		15.1	21.6

Table 5.1: Power consumption estimations of the various HGTD components and the total for the HGTD (for a total number of 7888 flex cables, 7888 sensors of 20×40 mm^2 each; 6.3 m^2 in total and 15776 ASICS). The last column includes a safety factor of 1.5 for the electronics.



(a) On-detector cooling pipes.

(b) R-z view of ITk and HGTD services region.

Figure 5.3: (a) Cooling layout (b) R-z view of the region around $R = 1$ m. The red region shows where services of the ITk and HGTD need to be extracted to the outside, sharing different slots in ϕ.

tions during opening/closing procedures are shown in Figure 5.5, with the ATLAS detector in closed (a) and open (b) position. While the opening/closing of the endcap calorimeter takes place, the cooling will stay disconnected and should be reconnected after the movement is finished. During this period the temperature inside the vessel will increase; a disconnection time of around 24 hs is deemed acceptable.

The cooling support plates are composed of a carbon fibre structure and a thermally conductive foam-like graphite or equivalent material. Carbon fibre is a stiff material with high thermal conductivity, thus providing a highly uniform temperature distribution in the cooling disk. A core made of conductive foam will absorb the different thermal expansion of the cooling pipes and carbon-fibre panels. The central plate and the outer rectangular staves will be made from a material with a high thermal conductivity (AlSiC, PEEK graphite reinforced, Carbon Fibre low epoxy) and bolted to the support plate with thermal grease media.

Given the challenging performance of the support plates, one full scale prototype will be produced with a half-disk composite plate, a few embedded cooling loops and one stave of dummy modules as heaters. This prototype will be submitted to several thermal cycles to study thermo-mechanical behaviour, temperature distribution, CO_2 cooling parameters

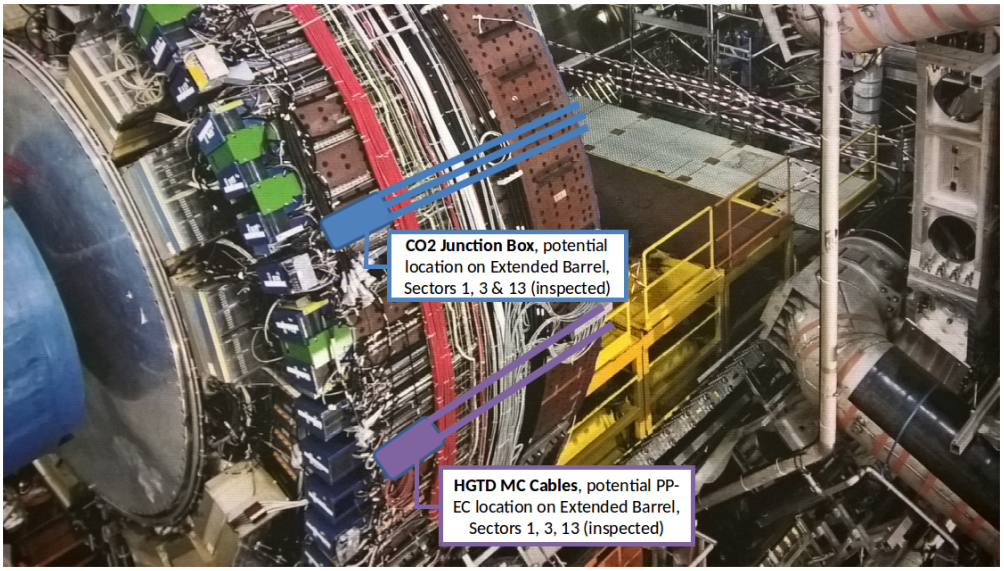
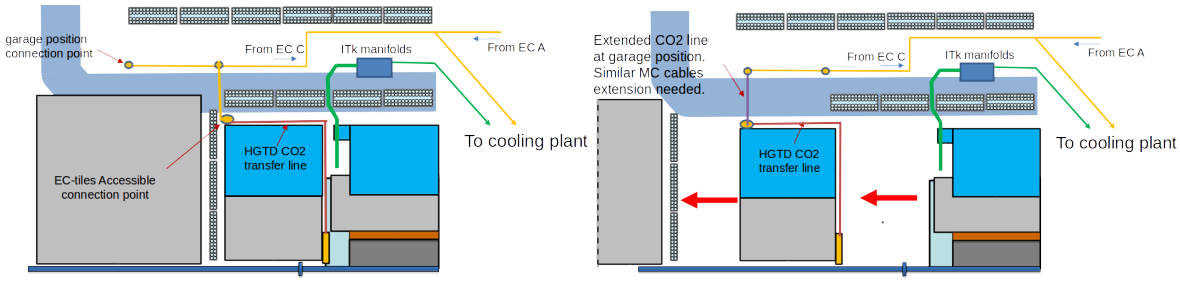


Figure 5.4: Picture showing the side of the endcap calorimeter, withdrawn from its usual position. The possible routing of services has been marked in colour.



(a) Closed detector.

(b) Open detector.

Figure 5.5: View of the possible routing of the HGTD cooling pipes with the ATLAS detector in (a) closed and (b) open position, showing the access to the connection/disconnection box before and after the movement of the endcap calorimeter.

and glue layers integrity between modules and carbon fibre skins.

5.1.3 Cooling performance

A finite element analysis of the current CO_2 cooling design has been performed for one side of a layer. The model considers a uniform power dissipation of the modules of 235 mW/cm^2 for $R < 320$ mm and 160 mW/cm^2 for larger radius (leaving a small margin with respect of the estimated values presented previously in 5.1.1). It considers the input cooling temperature of −30 °C at the centre of each cooling loop. The calculation has been made in a static regime, with no external exchange. The results are presented in Figure 5.6. The

obtained temperature distribution is of (-27±1)°C, in the active area; reaching −29 °C at $R > 640$ mm.

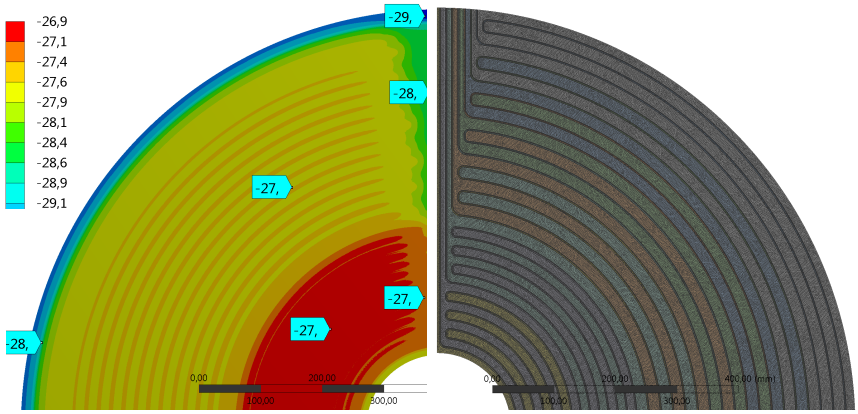


Figure 5.6: The left quarter disk shows the calculation of the temperature distribution in the cooling plate. On the right the FEA is shown.

The model used in these calculations will be improved by implementing a more realistic representation of the modules, the radial dependency of the power dissipation, and the thermal contact between components. A study of the power dissipation of the sensors as a function of irradiation was already presented in Figure 4.21. In addition, a study of the thermal runway will be performed to cover for a possible excess in heat productions from the electronics or a lack of CO_2 liquid. Such studies will provide important input to the optimisation of the cooling requirements presented in Section 5.1.1.

5.1.4 Cooling and power monitoring and control

The detector environment and parameters related to the cooling and power consumption will be monitored through links to the Detector Control System (DCS). It provides input to the interlock and power supply units as needed, for detector and operational security. In particular it will keep track of the humidity, temperature and pressure, with sensors installed in the whole volume of the HGTD: in the modules, flex cables, peripheral on-detector electronics, cooling pipes and the inside of the vessel walls. The outside temperature and humidity will also be monitored to ensure that adequate dryness and ambient temperature are maintained. In order to prevent thermal runaway, all elements that could be damaged from overheating will be equipped with Negative Temperature Coefficient sensors linked to the interlock system. Both sudden or slow changes are recorded and can trigger corrective actions from the cooling system or the power supply devices, as necessary.

5.2 Detector cold vessel and global structure

The primary role of the HGTD global structure is to provide a robust support to all active silicon layers and peripheral on-detector electronics in a cold and dry volume, precisely located on the front wall of the liquid argon endcap calorimeters. The chosen material should withstand the expected radiation levels and a wide temperature range as a safety requirement: from −55 °C to 60 °C. Thin large panels made of carbon fibre composite fit these requirements and provide a stiff support.

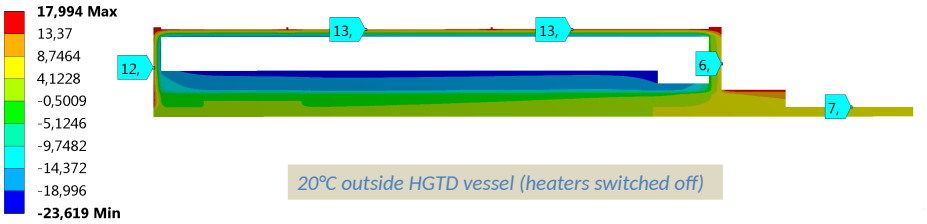
One of the main challenges is to preserve the detector volume dry. This can be achieved with a permanent dry N_2 flow (given a dew point of −60 °C). The flow will renew the air within the volume a few times per hour, with an over pressure of +5 mbar.

The second main challenge is to keep the temperature of the outer skins safely above the cavern condensation temperature (∼17 °C). In a way similar to what is done on the endcap calorimeters cover, heaters will be placed on the external face of the front cover of the HGTD vessel and on the outer ring, between the service feedthroughs. Their purpose is to ensure a temperature around 20 °C outside the HGTD vessel, in order to avoid the appearance of condensation. The face of the endcap calorimeter cryostat is already equipped with the necessary heaters. The expected power consumption of the front cover heaters is 75 W/m^2, and 175 W/m^2 for the outer ring. Figure 5.7 shows a calculation of the temperature distribution of the HGTD-vessel components and the moderator, considering that the inner volume (in white, not simulated) will contain the sensors at −30 °C. The difference in the external temperature achieved by having the heaters on can be appreciated by comparing Figures 5.7(a) and 5.7(b).

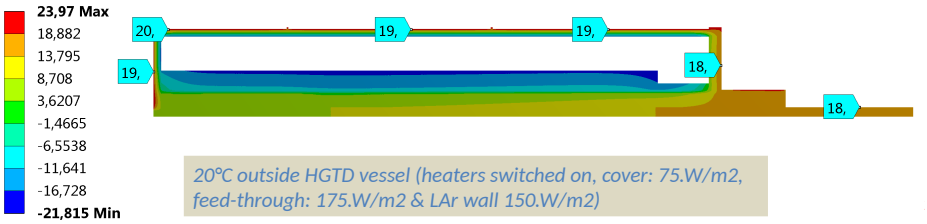
The bolting and locking interface with the endcap cryostat will use the same MBTS threaded spots and the central large hole of the warm tube taking into account the presence of moderator rings. The access to the holes should be possible without opening the HGTD cold vessel and should not affect its cold and dry volume. Possible conflicts with the cooling pipes of these moderator rings require further studies and optimisation. Since the expected performance of the proposed HGTD cold vessel is similar to the one of the ATLAS ITk global support, a collaboration program with the ITk team is underway in order to combine the R&D carbon fibre composite material studies, such as the selection of K13C2U (single skin) as material in an EX1515 matrix.

5.3 Moderator

A moderator disk made of borated polyethylene, with a density of 0.95 kg/l, will be placed in front of the endcap calorimeters on each side to shield the ITk and HGTD from backscattered neutrons The material is the same as the one used at present in the ATLAS detector. As can be appreciated in Figure 5.1, the moderator is divided into two disks, one inside



(a) With heaters on front cover *off*.



(b) With heaters on front cover *on*.

Figure 5.7: Simulation based on the FEA model of the temperature distribution of the HGTD vessel front cover and moderator. The view shows a transverse cut of the vessel, with $R = 0$ towards the left and the outer radius on the right. Only half the vessel is shown.

and one outside the HGTD vessel. Due to the very limited width in z between ITk and the LAr cryostat wall, and the fact that the latter is uneven, it is necessary for the moderator to be part of the HGTD assembly design. The moderator on the outside will be directly screwed to the LAr cryostat wall, and provide the necessary flat surface on which to install the HGTD and accessible bolting brackets. The part of the moderator inside the vessel gives an appropriate support for the instrumented layers, and because it goes up to $R = 900$ mm it leaves enough free space for the cooling services as shown in Figure 5.8.

The outside moderator disk has a thickness that varies along the radius: 10 mm covering the LAr calorimeter cryostat central flange and the bolting spots (110 mm<R< 342 mm) and 20 mm elsewhere (342 mm<R< 1100 mm);the weight of this disk will approximately 70 kg. It will be directly screwed to the endcap calorimeter cryostat and mechanically separated from the HGTD hermetic volume. The second moderator disk, inside the HGTD vessel, will have a thickness of 30 mm in the range of 120 mm $< R <$ 900 mm and weigh 70 kg per endcap. The total moderator thickness in z will be 50 mm except at the inner and outermost radii; it is 40 mm in the region between 110-342 mm and 20 mm for R>900 mm. During the maintenance (and when the expected replacement of the inner modules takes place at the surface), the two moderator disks will stay bolted in the LAr cryostat, together with the rear vessel cover. Consequently they will be made of unique circular disks to improve thermal insulation and mechanics stiffness.

5.4 Services

The HGTD data and powering services can be grouped into five categories: optical fibres for data transmission, bias voltage for the sensors (high voltage, or HV), power for the module electronics (low voltage, or LV), DCS links and powered components in the proximity (front-cover heaters and temperature sensors). A preliminary estimate of the required services per endcap (excluding the cooling lines) is summarised below.

- The number of optical links per endcap amount to 1640 and is composed of 600 up-links for the offline readout, 600 down-links for configuration and fast signals (clocks, L0/L1, etc) and 440 up-links for the luminosity readout. Optimising the number of input e-links per lpGBT for the luminosity could reduce this number by 10 %. The optical fibres are grouped in ribbons of 12 fibres (about 4×2 mm^2 cross section). In addition, these ribbons need to be encapsulated in cables in order to be routed in the flexible chains. The cables will contain six ribbons and have an outer diameter of 12 mm. Taking this grouping into account gives a total of 144 ribbons per endcap, including 88 spare fibres.

- The baseline for the bias-voltage distribution is to bring one individual line per module to the HGTD and to use some distribution fan-out boards in USA15 to group modules at the same radius and therefore require the same voltage. Consequently 3944 lines are needed, plus 288 return lines. The bias lines will be grouped into about 144 cables (outer diameter of 14 mm).

- The baseline for the power distribution is to use a design quite similar to the one used in the ITk-strip [4]: a 48 V voltage power supply in USA15, commercial DC/DC converters (48 V to 12 V) at the patch panel (PP-EC) which is proposed to be located at the back of the endcap cryostat, and radiation hard DC/DC converters (11 V to 1.2 or 2.5 V) on the peripheral on-detector electronics. The number of power cables (outer diameter of 14.0 mm) needed per endcap is approximately 16 from USA15 to PP-EC and 32 cables from PP-EC to each side of the HGTD.

- The number of DCS cables is still being optimised to fit the maximum size of ITk service corridors and the capacity of the flexible chains. Current estimates are around 2008 enable-status lines and 288 lines for grounding. Studies are ongoing to determine if all DCS connections need to be inside the flexible chains.

- Around 40 heaters are required per side (10 in each quadrant) in order to provide uniform heating. One PT100 gauge is used to monitor each heater, as is currently done for the heaters located on the LAr cryostat.

This information is summarised in Table 5.2, indicating the needed services. These numbers include spares to be installed in case of damage during installation or operation. The spares will not be connected unless they are needed.

	Optical fibres	**HV bias**	**LV power**	**DCS**		**Heaters**	
				Power	Probe	Power	PT100
Cable diameter [mm]	12.0	12.4	10.8	12.3	12.3	11.2	11.2
Number of wires/cable	72 fibres	37	2 conductors	34	57	20	20
Number of cables/quadrant	6	30	36	32	8	1	2
Number of spares/endcap	4×22 fibres	4×52	0	0	0	0	0
Total cables/endcap	24	120	144	128	32	4	8

Table 5.2: Summary of needed services (excluding cooling lines) per endcap of the HGTD. A *quadrant* is one quarter of one endcap. The DCS column includes the power management and probe monitoring.

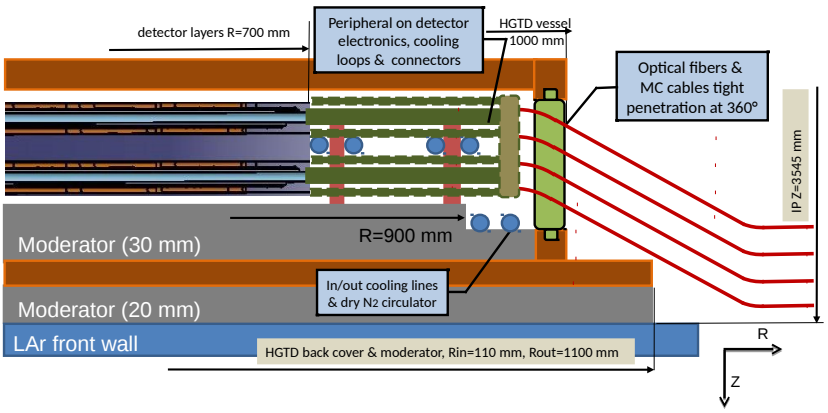
The readout links and DCS cables will be inserted in a flexible cable chain that goes from USA15 to the HGTD. It should run along the extended barrel region and allow monitoring of the HGTD even while opening and closing ATLAS. The bias-voltage and low-voltage services could be made of two cable types with a patch panel located at the back of the extended Tile barrel (as seen in figure 5.4 and 5.5). These cables will be disconnected when moving the endcap.

The baseline option is to extract the signals to the outside of the vessel and to route the needed cables/fibres to the detector using dedicated feedthroughs in the outer face of the vessel (see Figure 5.8). Custom-designed feedthroughs will be used, moulded from an elastomer soft flange with tight passage for electrical and cooling services. The services would then be routed to the outside of ATLAS in specific regions in ϕ, as shown in Figure 5.9. This figure shows a possible routing of the services, together with the nominal numbers of cables. A small quantity of spares, shown in Table 5.2, will be added. Studies are ongoing to optimise the accommodation of both HGTD and ITk services in the region around $1000 < R < 1100$ mm. The feedthrough studies for the TDR will be focused on a design for low heat loss using thermal shield materials and local heaters similar to what is planned for the front cover. In addition, the exact geometry and disposition of the detector components at R$>$ 900 mm may still be subject to optimisation.

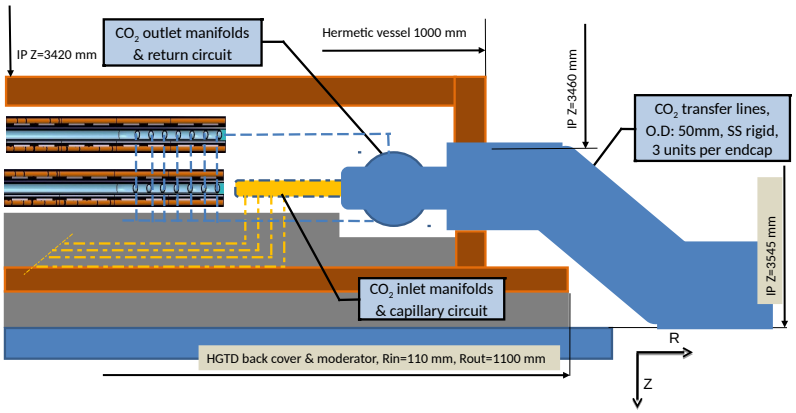
5.5 Outlook and path towards TDR

Three major activities are foreseen up to the TDR;

- A thermal demonstrator will be constructed using a stave with fake sensors and ASIC to establish the cooling performance of the proposed design. It should be available in autumn 2018. Relevant parameters will be measured using temperature sensors and thermal imaging cameras, and varying the heat dissipation, the CO_2 cooling parameters such as pressure and flow, and the flow for the dry nitrogen blowing. A stave with dummy modules and fake peripheral on-detector electronics will be used



(a) Other connections.



(b) Cooling pipes insertion.

Figure 5.8: Transverse view of the outer radius of the vessel. The peripheral on-detector electronics boards can be seen in (a) connected to the services via feed-through connections. In (b) a view of the position of insertion for the cooling pipes is presented.

to study the power dissipation in a realistic way and allow comparison with thermal simulations. These tests should also validate the part of the cooling circuit dedicated to the peripheral on-detector electronics.

- A simulation implementing a realistic model of the detector components needs to be performed to better estimate the cooling requirements. A study of thermal runaway will also be performed.
- A conceptual design of the feedthrough should be finalised by Q4 2018-Q1 2019.
- The services routing, compatible both with the HGTD and ITk needs, should be determined and implemented in a full 3D model of the ATLAS cavern. In particular, it needs to include the definition of the position of the patch panel needed to connect and disconnect the services when the detector is open. This work should be in an advanced state in Q1 2019.

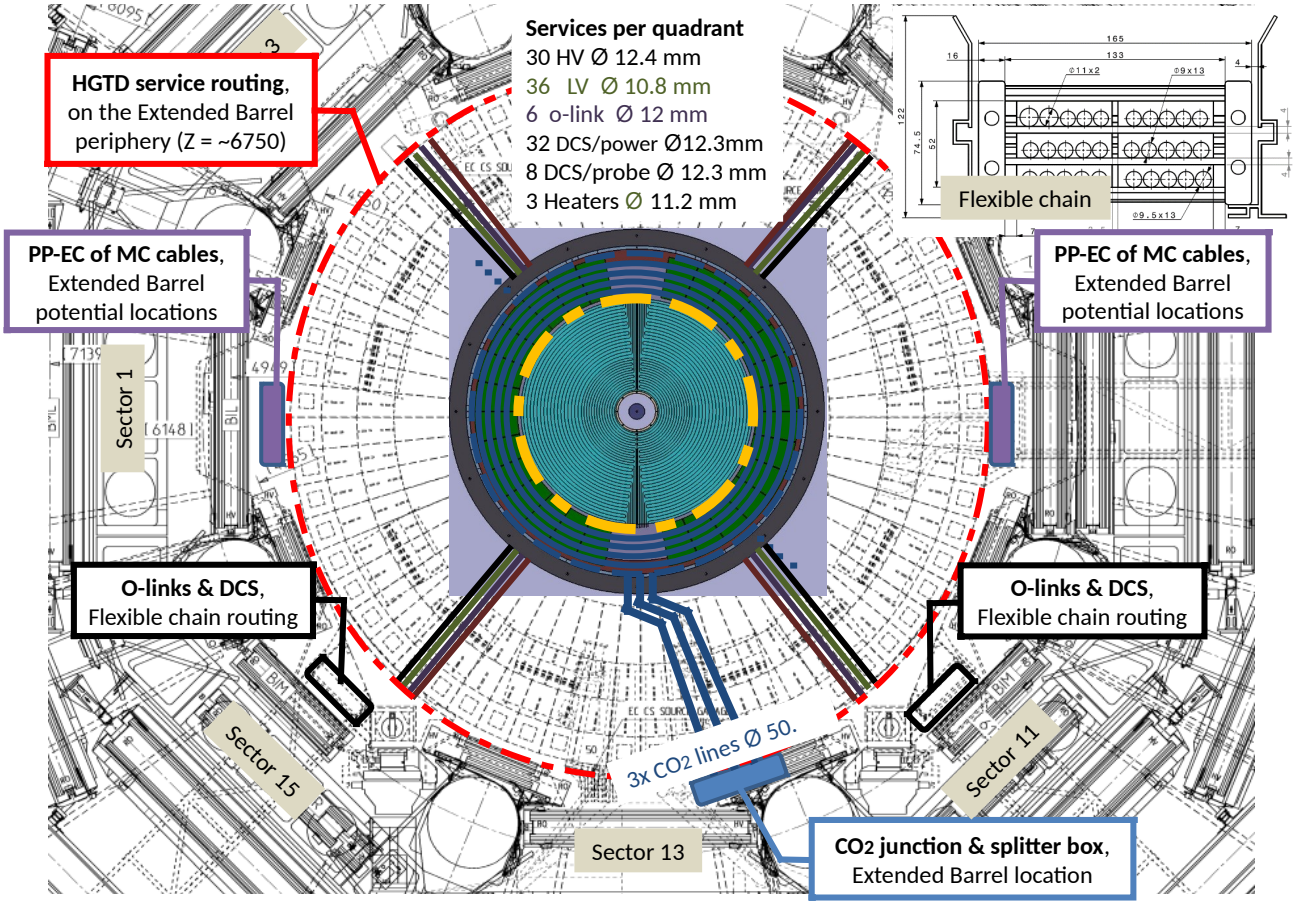


Figure 5.9: Illustrations of the possible path of the HGTD services (red), the cooling transfer lines (blue), multiconductor cables (MC cables, violet) and flexible chain (black) that will contain the DCS links and optical links (*o-links*).

In addition, a mechanics mock-up with a real-size cooling plate, stacking of cables and dummy modules of realistic dimensions will be made available during the first half of 2019 to confirm the overall detector envelope of 75 mm.

6 Organisation, cost and schedule

The HGTD group started as an organised ATLAS upgrade activity in summer 2015 and this new sub-detector proposal was part of the ATLAS Upgrade Scoping Document. The HGTD project is in close communication with ATLAS Technical Coordination and the ITk since the space constraints for the HGTD are very tight and care is needed to avoid interference with the ITk and the routing of its services. The HGTD project includes several activities:

- Sensors
- Electronics
- Luminosity and trigger
- Test beam measurements
- Module assembly
- Detector assembly and integration
- Simulation and physics performance

The work is carried out by roughly 120 physicists and engineers from 20 ATLAS institutes from 11 funding agencies, see Table 6.1. Table 6.2 summarises the involvement of the institutes in the different activities[1].

If approved by LHCC, the R&D in all different areas of the project will need to be intensified, in order to prepare for a Technical Design Report (TDR) in the first quarter of 2019. Dedicated working groups should be reinforced and adapted to the new needs of the project. The details of responsibility and sharing need to be defined in the MoU after the TDR. A preliminary survey of institute interests and of the available person-power have been performed and indicate that the (quite substantial) resources required may be made available.

A preliminary estimate of the core cost[2] of the HGTD is presented in Table 6.3. No core costs needed for the R&D period (mainly sensors and electronics) will be identified for the TDR with a proposed sharing between the HGTD institutes.

[1] Groups from the USA are currently only approved for R&D

[2] The item "Detector readout, dataflow, and network" is considered a TDAQ deliverable but cannot be included in the TDAQ TDR until the HGTD TDR has been reviewed by LHCC/UCG.

Country (funding agency)	Institutes/Universities
	CERN
France	LAL (Orsay), LPNHE (Paris) , OMEGA (Palaiseau)
Germany	JGU (Mainz), JLU (Giessen)
Slovenia	IJS (Ljubljana)
Spain	IFAE (Barcelona)
Sweden	KTH (Stockholm)
Taiwan	AS (Taipei), National Tsing-Hua U
USA	BNL, Ohio State U, SLAC, SMU (Dallas), Stony Brook NY, UC Santa Cruz, U of Iowa
Russia	JINR
Morrocco	Univ. Hassan II Casa Blanca

Table 6.1: Countries, funding agencies and institutes/universities participating in the HGTD project. USA groups approved only for R&D.

Activities	Institutes
Sensors	BNL, CERN, Dubna, IFAE, , JSI, UCSC
Electronics	AS, Tsing-Hua, CERN, Dubna, Giessen, IFAE, Iowa, KTH, LAL, Omega, SLAC, SMU, Stony Brook
Luminosity and trigger	KTH, Ohio State
Test beam measurements	All institutes
Module assembly	CERN, BNL, Dubna, IFAE, Iowa, JSI, LAL, LPNHE, Mainz, Ohio State
Mechanics and integration	CERN, Dubna, LAL, LPNHE
Software and performance	Casa Blanca, CERN, Giessen, IFAE, Iowa, KTH, LAL, LPNHE, SLAC

Table 6.2: Present and expected involvement of the institutes in the different HGTD activities.

The overall ATLAS installation schedule for Long Shutdown 3 provides constraints for the scheduling of the installation of the HGTD since it needs to be integrated into the global ATLAS Phase-II detector upgrade plan. The installation of the HGTD is planned to take up to one month for each side and should take place in June and July 2025, for the A and C endcap side, respectively. While all the mechanical supports, services and the cold vessel need to be installed during these two periods, the detector layers are designed to allow insertion during a winter shutdown in case of delays. This schedule maybe still be subject to modification if required by the installation of other ATLAS detector components.

Figure 6.1 and Table 6.4 give an overview of the schedule foreseen for R&D, prototyping, production and installation of the HGTD. There will be three main phases:

- **2018-2020** R&D
- **2021-2024** Construction
- **2025-2026** Integration, installation and commissioning

Item	Cost (kCHF)
Sensors	1700
Front-end ASICs	730
Bump bonding	900
Module assembly	600
Peripheral on-detector electronics (transition, optical and HV boards, optical links, services)	717
Power supplies and electronics in USA15	2027
Mechanics and integration (cooling support plates, vessel, feedthrough)	405
CO_2 cooling plant and distribution	450
Sub-total HGTD	7529
Detector readout, dataflow, and network	970
Total	**8499**

Table 6.3: Core cost of the HGTD in kCHF.

The main milestones have been identified during the R&D period and are listed in Table 6.5. The dates for the post-TDR milestones are preliminary and will be reassessed when preparing the TDR.

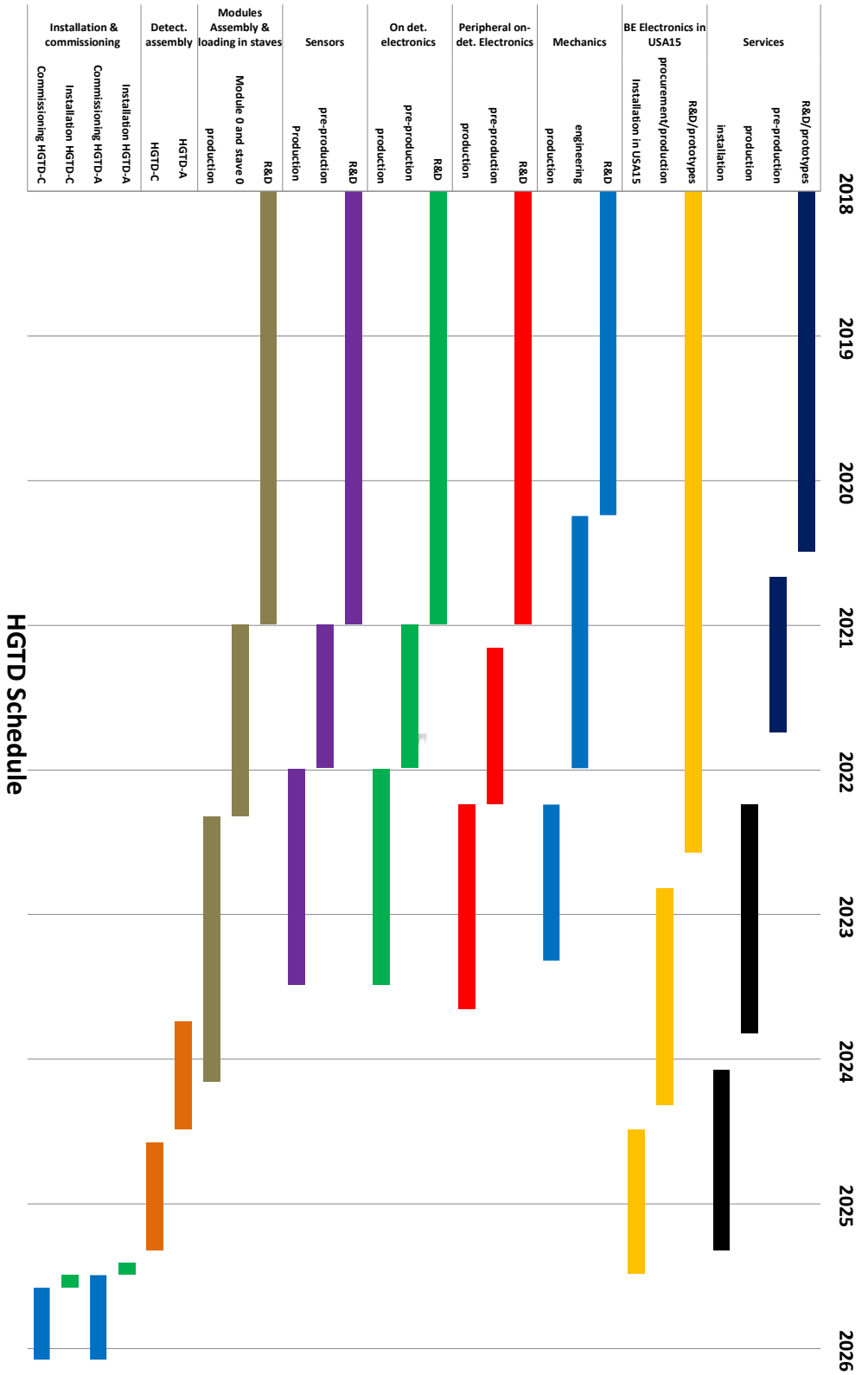


Figure 6.1: Gantt chart showing the schedule of the various activities in the HGTD project.

Main activity	Activity steps	Start	End	Work days
1. Services	R&D/prototypes	01/01/18	30/06/20	651
(cooling, cables, fibres, ...)	Pre-production	01/09/20	30/09/21	281
	Production	01/04/22	30/10/23	412
	Installation	30/01/24	30/04/25	326
2. BE Electronics in USA15	R&D/prototypes	01/01/18	30/07/22	1194
(LV, HV, luminosity board)	Prod./procurement	30/10/22	30/04/24	391
	Installation USA15	01/07/24	30/06/25	260
3. Mechanics	R&D	01/01/18	30/03/20	585
(cooling plates, vessel, ...)	Engineering	01/04/20	30/12/21	456
	Production	01/04/22	30/04/23	281
4. Peripheral on-detector electronics	R&D	01/01/18	30/12/20	781
(Flex, transition, optical	Pre-production	01/03/21	30/03/22	281
and HV boards, DCS, ...)	Production	01/04/22	30/08/23	369
5. On-detector electronics	R&D	01/01/18	30/12/20	781
(ASIC)	Pre-production	01/01/21	30/12/21	259
	Production	01/01/22	30/06/23	389
6. Sensors	R&D	01/01/18	30/12/20	781
(LGAD)	Pre-production	01/01/21	30/12/21	259
	Production	01/01/22	30/06/23	389
7. Modules assembly	R&D	01/01/18	30/12/20	781
and loading in staves	Module0 & Stave0	01/01/21	30/04/22	346
	Production	01/05/22	29/02/24	478
8. Detector assembly	HGTD-A	01/10/23	30/06/24	195
(Mount layers in vessel,	HGTD-C	01/08/24	30/04/25	194
install off-detector elec., ...)				
10. Installation in ATLAS	Install HGTD-A	02/06/25	02/07/25	21
and commissioning	Install HGTD-C	02/07/25	01/08/25	21
	Comm. HGTD-A	03/07/25	01/02/26	152
	Comm. HGTD-C	03/08/25	01/02/26	130

Table 6.4: Schedule of the HGTD project. The number of work days per week is assumed to be five. The dates for the post-TDR milestones are preliminary and will be reassessed when preparing the TDR.

Name	Area	Time	Comment
M1	Modules	Q3 2018	Performance of flex circuits
M2	Software	Q3 2018	Detailed geometry of HGTD in ATLAS software
M3	Services	Q3 2018	Performance of CO_2 cooling system with prototype and dummy stave
M4	Sensors	Q4 2018	Performance of large-size sensors (2×2 cm^2) from HPK/CNM and radiation tolerance performance
M5	Electronics	Q4 2018	Performance complete pixel readout channels with ALTIROC1
M6	Services	Q4 2018	Service routing conceptual design
M7	Electronics	Q1 2019	PDR of first complete ALTIROC chip architecture
M8		Q1 2019	Technical Design Report
M9	Electronics	Q2 2019	Submission of first iteration of ALTIROC
M10	Services	Q2 2019	Feedthough/services connectivity concept and prototype (PDR)
M11	Electronics	Q2 2019	Peripheral on-detector electronics concept and prototype (PDR)
M12	Services	Q3 2019	Design tooling for detector assembly and for final installation
M13	Sensors	Q3 2019	Final sensor specification and vendor qualification (FDR)
M14	Electronics	Q4 2019	Characterisation of first ALTIROC iteration
M15	Modules	Q1 2020	Prototype module assembly (2×2 or 2×4 cm^2)
M16	Electronics	Q2 2020	Submission of ALTIROC second iteration (FDR)
M17	Electronics	Q4 2020	Final validation of ALTIROC ASIC (PRR)
M18	Modules	Q4 2020	Stave 0 demonstrator including peripheral electronics and services

Table 6.5: List of main milestones during the R&D phase. The descriptions of the milestones use acronyms for Preliminary Design Review (PDR), Final Design Review (FDR), and Production Readiness Review (PRR).

7 Conclusions

This document describes a technical proposal for a High-Granularity Timing Detector (HGTD), to be installed in ATLAS during the long shutdown, which starts at the end of 2023 and is expected to last for 30 months, until the start of HL-LHC data-taking in mid-2026. This proposal is the result of two years of active R&D, especially on sensors and front-end electronics, performed since summer 2015 by ∼20 institutes and ∼120 collaborators. The proposal for the HGTD was already included in the ATLAS Phase-II Scoping Document [1].

The HGTD will provide a timing resolution of ∼30 ps for minimum-ionising particles throughout the entire duration of the HL-LHC programme, covering the pseudorapidity region between 2.4 and 4.0. The detector will use the space currently occupied by the so-called Minimum-Bias Trigger Scintillators installed in front of the LAr endcap cryostats on both A and C sides at ±3.5 m from the interaction point. Silicon Low Gain Avalanche Detectors (LGADs) will be used to provide the precision timing measurements. The R&D on the sensor technology and the front-end electronics have demonstrated that this target time resolution is already close to being achieved. A realistic baseline design has been described. An optimisation towards a baseline concept driven by the best compromise between performance and cost is ongoing.

With 30 ps time resolution for charged particles, the HGTD can mitigate the impact of pileup in the association of tracks in the forward region to their respective vertices, compensating for the reduced longitudinal impact parameter resolution of tracks reconstructed by the ITk tracking detector at large pseudorapidities. With this capability, the performance of pileup-jet suppression, b-jet tagging, and lepton isolation in the forward region approaches the same level as in the central region. The rejection of pileup jets improves by a factor of approximately 2 (for a hard-scatter jet efficiency of 98%), the light-jet rejection at a b-jet efficiency of 70% improves by a factor of 1.5, and the lepton isolation efficiency increases by 14%. Several important physics analyses rely on the performance of such objects in the forward region. This document demonstrates that the HGTD can improve the uncertainty on the signal strength determination for VBF-produced Higgs bosons decaying to $H \to WW^*$ by 8% and the signal significance for the $tH(H \to b\bar{b})$ process by 11%. For the measurement of the weak mixing angle, $\sin^2\theta_{\text{eff}}$, an improvement of 11% on the experimental uncertainty is achieved through the improved electron isolation performance in the forward region that the HGTD brings. Many other physics applications are being considered, including precision measurements of the searches for long-lived particles, machine induced non-collision background processes such as beam-gas interactions and beam-halo activity, etc.

Furthermore, the HGTD provides unique capabilities to measure the online and offline luminosity with high accuracy. It can provide a minimum-bias trigger at Level-0 and possibilities for improved pileup mitigation in both the Level-0 and the high-level trigger systems. The improved trigger capability as well as the impact on other physics analyses will be evaluated in greater detail in the Technical Design Report.

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