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Design and Performance of the Fermilab E781 (SELEX) Hardware Scattering Trigger

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Abstract

The design and performance of the Fermilab E781 (SELEX) hardware scattering trigger (HST) are described. This trigger worked by distinguishing beam scattering at small angles ($> 150\mu$rad) from non-interacting beam. Six 50 micron pitch silicon planes grouped in 3 (x,y) stations, two before and one after the target, were used as the detectors. The triggering system involved 1920 channels of readout providing data to the Fast Encoding and Readout System with programmable trigger logic processor (FERS). The overall system was tested successfully at Fermilab during the 1996-97 fixed target run. The encoding time of the readout part of the FERS device was 30 nsec and the processor decision time was 55 nsec. The HST provided an output signal 250 nsec after beam traversal of the target.

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1 Introduction

Fermilab experiment E781 (SELEX), which collected data during the 1996-1997 fixed target run, is designed primarily to study the production and decay of charmed baryons using a 650 GeV/c beam with Σ^- and π^- as the main components [1]. Supplementary parts of the E781 physics program involve the study of $\gamma\pi$ interactions through the scattering of high energy pions from virtual photons in the Coulomb field of the target nucleus. The reactions of interest were $\pi^-\gamma \to \pi^-\gamma$ to determine the pion polarizability, $\pi^-\gamma \to \pi^-\pi^0$ to determine the chiral anomaly amplitude $F_{3\pi}(\gamma \to 3\pi)$, and $\pi^-\gamma \to \pi^-\eta$ as part of a search of hybrid mesons [1][2]. In E781, first level triggering on the produced photon was not possible because the electromagnetic calorimeter was located some 50 meters downstream of the target, and thus could not be placed in coincidence with the beam. Triggering on such very rare processes in high energy, high intensity beams using a hardware processor presents an experimental challenge because the desired final state of one charged outgoing particle must be distinguished from noninteracting beam particles by the measurement of a scattering angle of less than 1 mrad. It was therefore decided to build the Fast Encoding and Readout System with programmable trigger logic processor (FERS) for triggering on events with only one scattered charged particle in the final state.

The design and performance of the Fermilab E781 (SELEX) hardware scattering trigger (HST) are described. The HST provides a fast trigger decision for Primakoff scattering events with gamma rays and a single charged pion emitted at a scattering angle exceeding 150 μrad. SELEX implemented a first level "beam kill" Primakoff trigger, which worked by distinguishing pions with a small scattering angle from non-interacting beam. This trigger employed six (x,y) silicon planes grouped in 3 stations, two before and one after a Pb target. We formed a coincidence between the projections ont the third silicon station of hits in the first two stations, assumin a beam particle, and then vetoed in a square (x,y) window of $\pm$ 3 strips around this projection. The triggering system involved 1920 channels of 50 μ pitch silicon strip detectors providing data to the Fast Encoding and Readout System with programmable trigger logic processor (FERS). The overall system was tested successfully at Fermilab during the 1996-97 fixed target run. The encoding time of the readout part of the FERS device was 30 nsec and the processor decision time was 55 nsec. The HST provided an output signal 250 nsec after beam traversal of the target for a scattering angle greater than 150 μrad.

2 Description of the System

- **Specific features of the FERS processor**

The key features of the processor hardware are the use of:

· fast look-up memories to provide the programmable decision logic;
· fast Quick Logic FPGA (Field Programmable Gate Array) integrated circuits as the core logic elements of the design;
· a special track identifying algorithm to reduce the contribution of noisy channels;
· fast FIFOs as programmable delays and gates;
· a programmable mask to inhibit noisy channels and a programmable test pattern for each channel;
· four 10 bit readout scalers to provide counting characteristics;
· two parallel streams of output data — one, a circular buffer (10 μsec deep in 19 nsec steps) of encoded data, and the other, the latch of encoded data used by the trigger processor in reaching its decision;
· serial readout of gated data from every channel for diagnostic purposes.

- **General hardware configuration**

The main hardware modules of the system together with the silicon detectors and front-end electronics are presented in Fig. 1. They include:

· a 64 channel Special Board (SPB), containing a 64 input latch, a 64 input edge register, and a 64 input priority encoder;
· a Back Plane (BPL) to provide the daisy-chain of SPBs. It contains the final encoder and provides a parallel data stream via a 25 twisted pair cable for subsequent trigger decision and fast readout;
· a Receiver/Digitizer/Latch (RDL) card, containing a receiver and a latch for encoded data from one SPB/BPL assembly, and two synchronizing FIFOs for delay and gating;
· two Programmable Logic Units (PLUs), one each per X- and Y-view, containing look-up memories for the trigger decision;
· a Databus/Trigger Interface (DTI) board as an active back plane for the RDLs and PLUs to provide interfaces to the E781 trigger logic and data acquisition systems.

The system uses the 53 MHz accelerator radio frequency signal (ARF) for the data clock, and the E781 beam particle identification time (T0). The unit is latched by the experiment's common DAQ readout strobe (T2). The entire system occupies four Vector crates.

- **Detectors and front-end electronics**

Six single-sided silicon microstrip planes, each with a pitch of 50 μ and a thickness of 300 μ, are used to measure the X and Y positions of 650 GeV/c beam particles. They are assembled in three XY-stations (SSD1-3) located in the very upstream part of the E781 apparatus. The first two stations are separated by a distance of 1.5 m; the third station is located 2 m downstream from the second station. The Pb target was placed between the second and third SSD stations, 1 m upstream of SSD3. There was a total of 1920 readout channels. The number of Si planes as well as the choice of their location were limited by the desire to minimize material in the E781 incident beam and by the available space in the spectrometer.

The front-end electronics has two stages — 4-channel charge sensitive preamplifier hybrid chips (CERN MSP1) mounted next to the fanout boards on the Si planes, and 16-channel amplifier/discriminator cards (Nanometric N277CD) installed in special crates providing power to each card and a common programmable threshold. The silicon planes and front-end electronics were part of a previous FNAL experiment (E761) [3].

3 Data Handling in the FERS Processor

The block and timing diagram for the FERS processor is shown in Fig. 2 for the X-view planes. The ECL bipolar signals from the N277CD cards are accumulated in the input latches of the SPBs. The first-arriving pulse from a given plane starts a 25 nsec long OR signal, and latched data for all input pulses from this plane arriving within this time interval are reloaded by this OR signal into the edge registers and after that go into the priority encoders on the SPB cards.

The BPL provides encoding for a given plane by analyzing priority codes from the corresponding SPB cards. The registration of a new event is available 50 nsec after the previous event. The BPL generates an 18 bit word with two 9 bit binary codes identifying two strips: the strip containing the first hit (first 'on' strip) encountered counting from 1 to 512 (bottom strip, B) and the first on strip encountered counting from 512 to 1 (top strip, T). There are additional bits H and DV serving as logical flags and indicating that no strips (DV=0), or more than two strips (DV=1, H=1) are on in the given plane. Further logical decisions and definitions ('zero' if no strips are on, 'single' if one strip is on, 'cluster' if a set of adjacent strips are on, or 'many' if a set of strips are on with at least one strip off between them) are made in the RDL modules, and the corresponding logical outputs for all planes go to the programmable decision logic. Total encoding time (SPB encoders plus BPL encoder) is 30 nsec.

The DV signals from all planes (DVX1, DVX2, DVX3) start the programmable logic, which produces a common strobe to latch the data from all the planes (X1T, X1B; X2T, X2B; and X3T, X3B) in the coincidence registers of the RDLs for subsequent use in the look-up memories of the processor. The data coincidence gate has a limit of 50 nsec. The RDL modules also provide a stream of time-sliced data, synchronized with the 53 MHz accelerator radio frequency clock, read out by the experiment's DAQ. This is done using synchronized FIFOs as programmable delays and gates.

The data from the X1 and X2 planes go to four input look-up memories which provide four combinations of top and bottom strips, predicting possible positions of the track in the X3 plane (I1X-I4X). These predictions are compared with the hits in the X3 plane (top and bottom strips X3T and X3B) in the eight final look-up memories and the result of this comparison (BX) is sent to the programmable decision logic. If at least one look-up

finds the difference to be not more than 3 strips, then BX (beam in X-view) is set to 1. Checking all eight combinations for the track candidates helps identify beam tracks in the presence of noise.

The decision logic also has input from the Y-view look-up memories (BY) and inputs for logic signals from all 6 planes. A variety of different algorithms for the decision logic is provided by fast PALs. The common strobe of the coincidence register, delayed by 55 nsec, loads the result into the decision register. The FERS output signal for the trigger logic is a coincidence of the processor decision with a delayed T0 (pretrigger) pulse. The total elapsed time, from the moment of beam (T0) until the time of the E781 data latch decision (T1), was about 250 nsec, and included 40 nsec for the silicon detectors and the front-end electronics, and 60 nsec for the cables.

The FERS processor has readout and downloading interfaces that are connected to the E781 data acquisition system. The block of readout data includes time-sliced data, coincidence register data, look-up memory data, scalers, and various logic signals. A block of different constants can be downloaded into processors and encoders: look-up alignment constants, RDL test patterns, inhibit masks for the hot channels, and test patterns for the encoder latches. The special serial interface is used for downloading communication with the encoders.

4 Results Achieved

The distributions of the difference in X and Y views between the predicted and the measured coordinates in X3 and Y3 for non-interacting beam particles are presented in Fig. 3, and for events triggered by the FERS processor in Fig. 4. The non-interacting beam distribution in Fig. 3 is well contained within ± 2 strips. The threshold for deciding to accept an event as an interaction (± 3 strips) is clearly evident in Fig. 4. The algorithm used rejected an event as a beam particle if both X and Y views had at least one hit within the threshold limit of ± 3 strips — i.e., a beam track definition of BEAM=BEAMX.AND.BEAMY. The rejection factor achieved with such an algorithm is limited by silicon plane noise. This rejection can be improved significantly if one changes this definition to BEAM = BEAMX.OR.BEAMY, but such an algorithm can yield lower acceptance, and possibly modify the angular distribution of scattered particles in physics events. Examination of these and other issues is underway using about $7 \cdot 10^7$ triggers recorded during 6 days of dedicated running.

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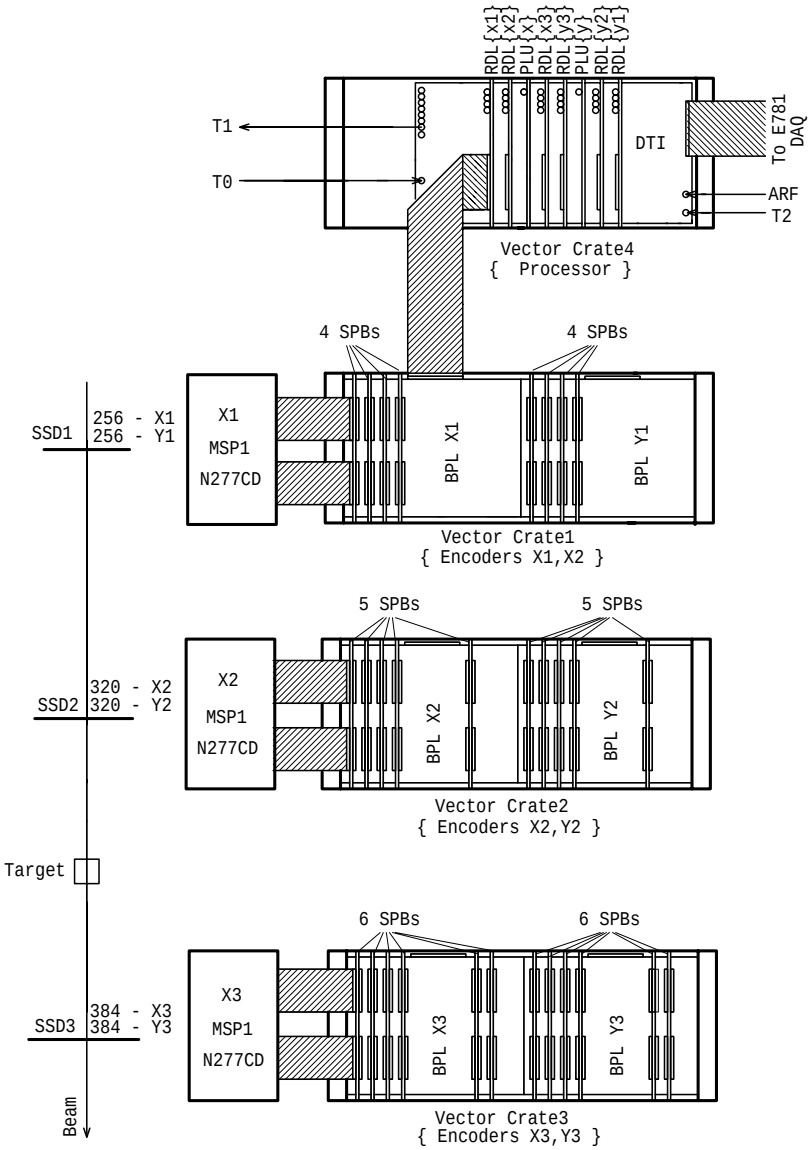

Fig. 1. General hardware configuration for the FERS processor.

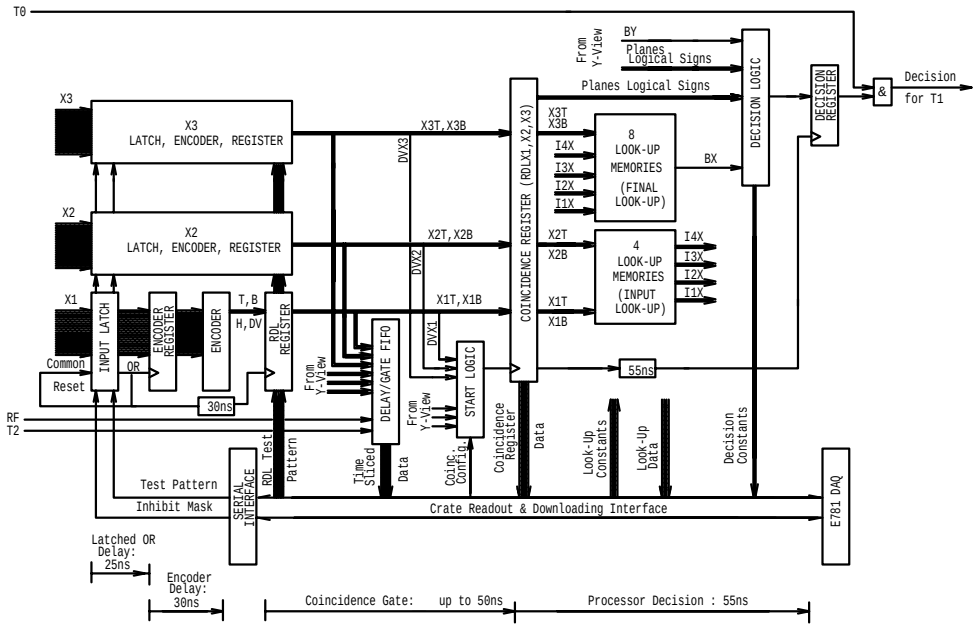

Fig. 2. Block and timing diagram for the FERS processor.

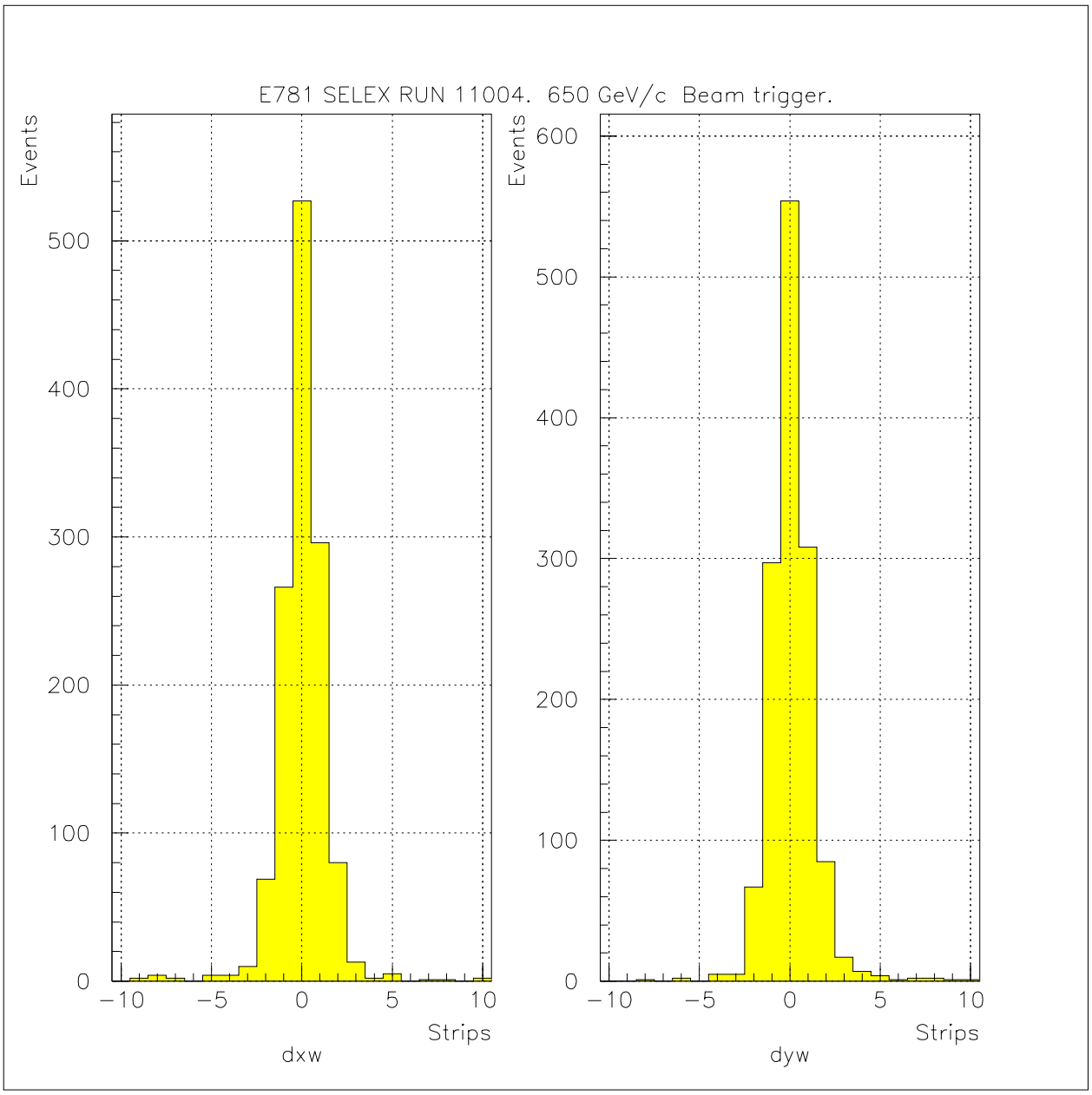

Fig. 3. The difference between the predicted and measured positions (in strips) in X3 and Y3 for non-interacting beam tracks.

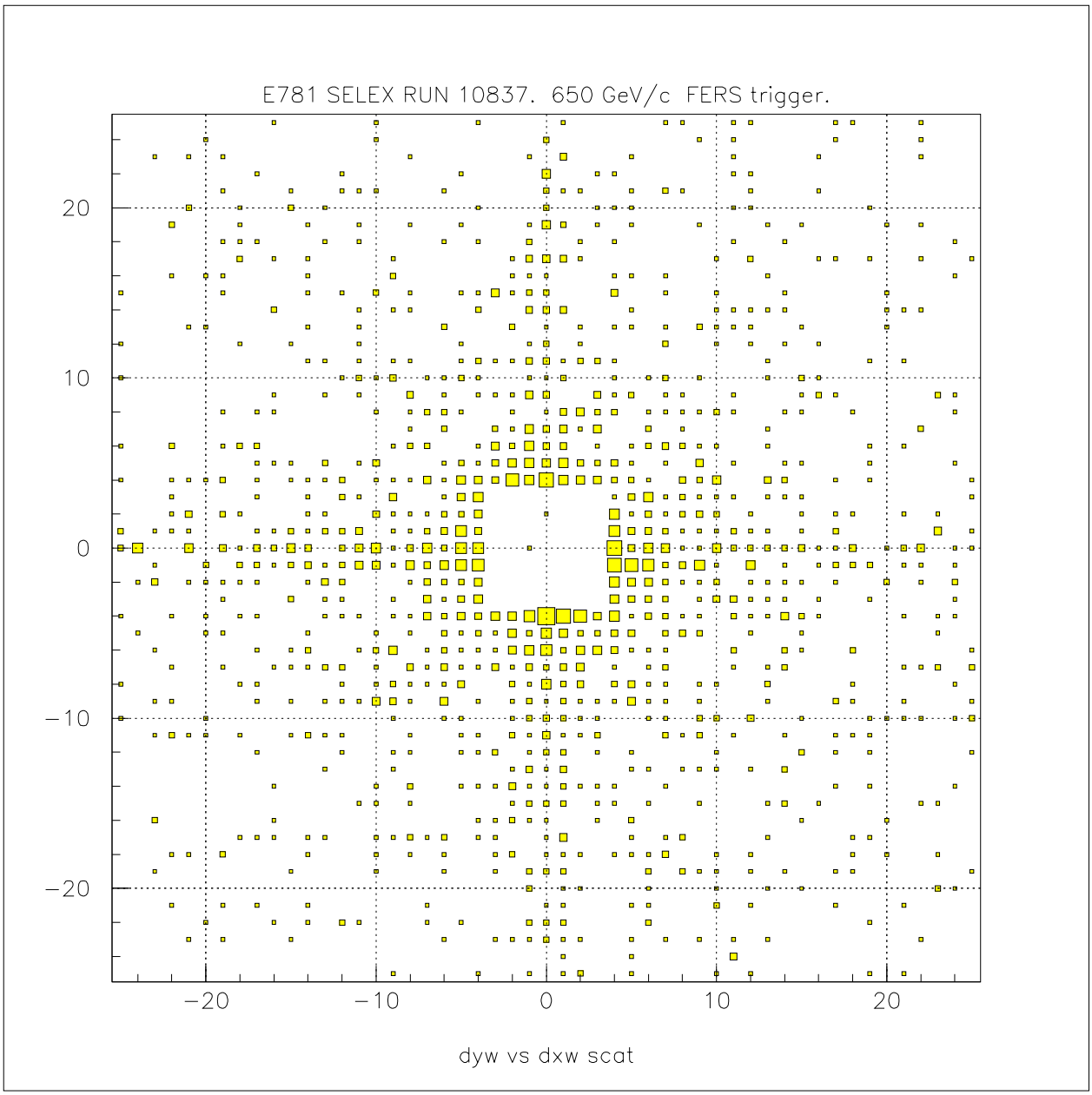

Fig. 4. The difference between the predicted and measured positions (in strips) in Y3 vs. X3 for events triggered by the FERS processor.