PROPOSAL FOR A HYPERON TRIGGER FOR KTEV

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1 Introduction

The study of hyperon decays has been approved as part of the KTeV experiment (see KTeV memo 119 "A proposal for hyperon physics at KTeV"). There are four components of the experiment that are vital for that set of physics topics: a full coverage TRD, a beamhole TRD, a polarizing magnet and a trigger. Construction of the full coverage TRD is underway (see memo 185 "The KTeV TRD design report"), and testing of the beamhole TRD is progressing (memo 197 "Laboratory tests of the beamline TRD"). A magnet that can be used for setting the lambda polarization has been reserved for our use. The subject of this memo is to outline our proposal for the second level triggering for hyperon decays.

2 The proposed trigger module

The trigger for lambda decays in E799-I used a U.Chicago designed Fastbus type board, termed Plotin, whose inputs were a subset of drift chamber signals. A detailed description of how that trigger worked is given in the hyperon proposal. In brief, it analyzed a copy of the central 10 drift chamber wires from each plane of X and X' wires. It searched for a set of hits defining a straight track in the first two drift chambers and in the last two drift chambers, separately. It then determined whether these two track segments corresponded to a single high momentum track in the spectrometer. A physical offset of the fourth drift chamber with respect to the others was

required for biasing the trigger to positive, high-momentum tracks.

For KTeV, new trigger boards would have to be made, since the logic chips used in the Plotin board are no longer manufactured. A new board would have to be made in any case, since the X view now has two beam holes that are separated, not one above the other. The cost of manufacturing new boards is on the order of $10K. We have been investigating the possibility of purchasing off-the-shelf logic modules to replace the Plotin board, at a similar cost.

Our proposal is to use several of the new Xilinx based Lecroy 2366 modules (termed a "universal logic module" or ULM) for a hyperon trigger. A description of this module, which is not in any catalog, is given in the appendix. In brief, it is a single width Camac module, with 59 i/o connections. They are separately selectable to be input or output within groups of 4, except for 3 connections which can be independently selected. To quote from the description:

> Any logic that can be implemented as a synchronous (clocked) state machine may be programmed, subject only to the limitations of the Xilinx 4005 gate array chip (approximately 5000 equivalent gates).

The connections use differential ECL signals. We would use the logic module to make a fast decision based on the logical 'or' of drift chamber hits, specifically to find roads corresponding to stiff tracks in the beam hole region.

3 Inputs and outputs to the trigger

A gate generator, triggered by the level 1 trigger, will create a signal of a fixed length, which will be an input to the logic modules indicating the time during which the drift chamber signals are active. (The level 1 reset signal will be used as a veto to this gate generator.) Other level 2 inputs to the hyperon trigger will be trigger signals from the beam hole TRD and full coverage TRD. These three signals will have to be translated from NIM levels to differential ECL.

The main inputs to the hyperon trigger, as shown in the memo "KTeV Level 0/1/2 Trigger", are copies of the latched signals from the drift chambers. These signals are differential ECL. As shown in figure 1, there is a convenient set of 16 wires from each drift chamber that exactly maps onto the beam region. Using this set of wires, it would be necessary to use at least two Lecroy 2366 modules for each beam hole (4x16=64, which is larger than the 59 i/o connections in a single module). We propose to copy the signals coming in on this set of wires, and distribute an overlapping set of 12 wires to two modules, to ensure total beam coverage. We will thus require a means

of fanning out the drift chamber signals. A good module for this purpose is the Lecroy 4518 delay/fanout. We will need 8 of these devices. We hope to obtain 5 2366 modules, 2 for each beam hole, and 1 for a spare.

The output from each of the 2366 modules will be two differential ECL signals. One will be the level 2 decision from the internal search for straight tracks. The other is a busy signal, generated while the internal search is active. Translation of these signals to NIM will take place, followed by or'ing the result from the two modules associated with each beam hole.

Figure 2 shows the schematic for our proposed trigger. This schematic is for one beam hole only. A summary of the electronic modules needed for the hyperon trigger is as follows:

- 8 Lecroy 4518 ECLine delay/fanout
- 5 Lecroy 2366 Universal logic modules
- 1 Lecroy 4616 ECL-NIM-ECL converter
- 1 Lecroy 222 gate generator
- 1 Lecroy 622 coincidence units
- 1 Lecroy 429A logic fanout

4 Programming the 2366 modules

Figure 3 shows the timing of various signals in the hyperon trigger system, both internal and external to the logic modules. Arrows indicate the flow of the logic.

Currently we have one 2366 module on indefinite loan from Lecroy. Capabilities for programming Xilinx software exist at Fermilab. We hope to test the various programming details of this module in the next year.

5 Conclusion

We feel that the versatility and simplicity of the LeCroy 2366 logic module will allow us to create a Level 2 trigger for hyperons at KTeV, with no need of custom designing a logic board for that purpose. The current price of this module is quite reasonable, considering the cost of redesigning the Plotin trigger system. We intend to continue studies of this trigger scheme using the KTeV Monte Carlo. We reccomend adding the list of electronics modules given in this report to the official "PREP" list.

APPENDIX

Message from Ed Corlett concerning the 2366 module:

From: FNALV::LECROY "Ed Corlett, (708) 386-3628" 13-APR-1994 09:53:43.39
To: RAMBERG
CC: LECROY
Subj: 2366 MODULE

April 13, 1994

Hi Erik,

The 2366 is a new module designed by Richard Sumner who used to be at Univ. of Chicago (ask Bruce Winstein). It is a single width CAMAC module costing $1990 each. Four have been shipped to customers and six are in stock at the factory.

If you can draw a logic diagram of your pattern searching requirement, then the 2366 is the ideal module because this is what you do to program its Xilinx chip. The latching of your inputs should be of no problem.

I have attached a description of the 2366,

Ed

LeCroy model 2366 Universal Logic Module September 22, 1993

The CAMAC 2366 is a general purpose programmable logic module, using state of the art field programmable gate array technology. This CAMAC module can be used as a programmable LeCroy Ecline trigger processor module, among other uses. In addition to a full 24 bit CAMAC interface, there are 59 front panel differential ECL i/o signals, which (with some restrictions) can be independently selected to be either inputs or outputs. This module is also useful as a general purpose controller, as part of a test system or data acquisition system.

The desired logical operations are programmed in a Xilinx 4005

gate array chip. Any logic that can be implemented as a synchronous (clocked) state machine may be programmed, subject only to the limitations of the Xilinx 4005 gate array chip (approximately 5000 equivalent gates). There are 3 clocks available on the board, 40, 20, and 10 MHz, or any of 3 special front panel inputs may be used as a clock. Input and output signals use standard 10124 and 10125 TTL-ECL level translators. Input signals as short as 5 nanoseconds can be latched and synchronized with the internal state machine logic.

The gate array must be programmed after power up, and can be reprogrammed at any time. An onboard EPROM socket may contain a program which is loaded on power up, or reloaded on CAMAC command. The Xilinx chip may also be programmed directly from the CAMAC dataway (the program information is stored in RAM in the Xilinx chip, so there is no limit to the number of times that it can be reprogrammed).

A few basic CAMAC Function codes are implemented in hardware, and are available on power up. These are only used to program the Xilinx chip, and all but one of these functions dissappear after a CAMAC clear operation (F9, C, or Z).

F30	A0-A15	enter programming mode with eprom selected enable all other hardware function codes
F28	A0-A15	select CAMAC programming mode
F25	A0-A15	program Xilinx chip (program pulse lasts until the next S1)
F16	A0-A15	write 8 bits to the Xilinx
F12	A0-A15	test Xilinx READY line (not usually required)
F13	A0-A15	test Xilinx program DONE
F14	A0-A15	test Xilinx INIT line
F9	A0-A15	disable function codes except for F30 (CAMAC C, Z have the same effect)

The Xilinx chip automatically loads itself if an EPROM is

installed on the board. An F30 command followed by an F25 will cause the Xilinx chip to be reset and reloaded from the EPROM.

To load a program from CAMAC, the F30 command is follwed by an F28 and F25. After the Xilinx INIT line is true (test with F14), the data is written 8 bits at a time using F16. F12 tests the Xilinx ready line before each write operation. This is not required unless the CAMAC host is capable of CAMAC operations at a rate greater than 500 kHz. This continues until all data is written and the Xilinx DONE line is true (test with F13). The Xilinx XACT software or any of several third party gate array software packages can be used to prepare the program file. An example basic program is supplied which reads the Xilinx .BIT file and uses standard ESONE CAMAC functions to load the program file into the 2366 module.

The initial program in the EPROM is T2366E (the schematic is included in the manual) This implements a simple divide chain to flash the leds with the 3 internal clocks (40mhz, 20mhz and 10 mhz), a 24 bit read write register and a register which latches the CAMAC F,A,,Z,I,N on every S2. This last register is read by F0, A1. This emulates most of the test portion of the LeCroy 2050 CAMAC dataway display and test module.

A simple basic program which exercises the 2366 is EP2366.bas. It starts by forcing the reload of the Xilinx chip from the eprom (with T2366E), and implements a simple CAMAC system test.

The example program LOAD2366.bas will load an arbitrary xxxx.bit file into the Xilinx chip.

SPECIFICATIONS: 2366 Universal Programmable Logic Module

single width CAMAC module

1 Led indicates N line activity

2 programmable Leds

59 i/o signals on front panel, all are differential ECL

all front panel i/o is to and from the Xilinx chip

input or output is selectable in groups of 4
  inputs are terminated with 112 ohms
  outputs will drive 100 ohm lines

Programmable gate array: Xilinx 4005
  approximately 5000 gates: 196 configurable logic bloocks,
  616 flipflops, 112 i/o blocks, 6272 Ram bits,
  fast carry logic, wide decoding

40 MHz, 20 MHz, and 10 MHz crystal clocks on the board

programmable by optional on board (socketed) Eprom on power up, or
  by CAMAC command to reload from Eprom

programmable via CAMAC, at any time, independent of Eprom.
  Xilinx XACT software system is required for programming
  Uses Xilinx .BIT file for programming information
  Basic CAMAC programming software for IBM compatible included
  11875 CAMAC F16 write operations are required to program
  all logic must be clocked (synchronous logic)

Camac interface:

  programming, 8 bit write only interface
  Test for successful programming

  after programming, all camac control and data lines (N, F,
  A, 24R/W, C, Z, S1, S2, Q, X, L) are available to Xilinx chip

  Only 1 function code is reserved for reprogramming, all
  others are available for the user

Possible Applications:

    trigger logic, digital 48 input majority logic
    trigger or readout controller, pipelined sequential logic
    pulse sequence generator, any arbitrary state machine logic
    fast memory, FIFO or LIFO, 16 bit digital adder

CAMAC interface pin assignments for Xilinx 4005-PGA156

CAMAC NAME	XILINX PIN	CAMAC NAME	XILINX PIN
C	R10	the 24 bit read-write bus	
Z	T9		
I	E14	RW1	T16
N	C5	RW2	T14
S1	T7	RW3	T10
S2	A2	RW4	R9
A1	B4	RW5	T8
A2	A3	RW6	P7
A4	B5	RW7	T3
A8	B6	RW8	P4
F1	A5	RW9	R1
F2	C7	RW10	P2
F4	B7	RW11	P1
F8	A6	RW12	N1
F16	A7	RW13	K3
		RW14	K2
X	G15	RW15	J2
Q	G16	RW16	J3
L	H16	RW17	H1
		RW18	G1
		RW19	F1
enables for bidirectional		RW20	F2
24 bit read write bus		RW21	E3
Re* T11	r1-r24	RW22	C1
Wr1* R11	w1-w8	RW23	B1
Wr2* A8	w9-w24	RW24	A1

Direction for R1-R24, normally +5v, pin T1

40 MHz crystal clock pin B3 (PGCK1)
divide by 2 (20 MHz) pin B16(PGCK2)
divide by 4 (10 MHz) pin T15(PGCK3)

FRONT PANEL

programmable LEDS, top = D14 (red), bottom = C16 (yellow)

Front Panel Input-Output pins:

PAIR NUMBER	A (8)	B (17)	C (17)	D (17)	connector (pairs)
1	F15	R6	B2	J15	
2	E16	T4	C9	J16	
3	F16	R4	B9	K14	
4	G14	R3	A9	K15	
5	P9	N2	C10	K16	
6	T6	M3	B10	L15	
7	R7	L2	A10	L16	
8	T5	L1	B11	M14	
9		K1	A11	M16	
10		J1	C12	N14	
11		G2	B12	N15	
12		G3	B13	P12	
13		E1	A13	P15	
14		E2	A14	P16	
15		C2	C15	R13	
16		D3	D15	T13	
17		R16	B14	T2	

All front panel i/o is selectable as input or output in groups of 4, as indicated below (the 3 clocks inputs are separately selectable). This is accomplished by installing the socketed ECL-TTL or TTL-ECL level converters and the appropriate termination resistor networks. All inputs and outputs are differential ECL. The corresponding Xilinx pins must be programmed as either input or output.

For input only the 10125 ECL to TTL converters and the 56 ohm termnation resistor SIPs are installed. The inputs are properly terminated for twisted pair cable.

For output, only the 10124 TTL to ECL converters and the 390 ohm pull down resistor SIP are installed.

Note that the module will work properly with short cables (but with reduced noise immunity) even if both the input termination SIPs and the output pulldown SIPs are installed.

The logical polarity of any signal is programmable in the Xilinx chip of course. There are a total of 59 i/o signals.

1 16 pin (8 pairs) header:

i/o A 1-4
i/o A 5-8

3 34 pin (17 pairs) headers:

i/o B 1-4
i/o B 5-8
i/o B 9-12
i/o B 13-16
i/o B 17 (can be connected to SGCK1)

i/o C 1-4
i/o C 5-8
i/o C 9-12
i/o C 13-16
i/o C 17 (can be connected to SGCK2)

i/o D 1-4
i/o D 5-8
i/o D 9-12
i/o D 13-16
i/o D 17 (can be connected to SGCK3)

SGCK1, 2 and 3 are Xilinx internal clock distribution networks

It is possible to convert the front panel i/o to bidirectional TTL. This user modification cannot be wholeheartedly recommended, however, since little protection is provided for the Xilinx chip. This method will only work at low speeds (less than 1 MHz) and for very short cable lengths. Deglitching will

be needed at all receivers. The Xilinx pins cannot drive 100 ohm terminated lines. For best results we recommend using the terminated ECL for the cable runs, and converting to TTL at the destination circuit board. This is necessary if high speed performance is required.

To provide TTL connections construct this 16 pin dip header with 4 100 ohm resistors, for each group of 4 to be used as TTL.

Install this header in the 10124 location after removing both resistor packs, and both the 10124 and 10125 chips.

This user modification connects the Xilinx pin directly to the odd numbered pin on the front panel connector. The corresponding even numbered pin is grounded. There is no buffer, ONLY a series resistor to prevent damage to the Xilinx chip.

The Xilinx chip can be programmed for either INPUT, OUTPUT or as a TRISTATE pin.

Please Use With Care!

pin

1	connect to 16
2	connect to 16
3	100 ohm resistor to 7
4	100 ohm resistor to 5
5	100 ohm resistor to 4
6	
7	100 ohm resistor to 3
8	
9	
10	100 ohm resistor to 12
11	100 ohm resistor to 13
12	100 ohm resistor to 10
13	100 ohm resistor to 11
14	connect to 16
15	connect to 16
16	connect to 1,2,14,15 (ground)

note that only 4 100 ohm resistors are required.