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# FAST3 ASIC: an analog front-end with 30 ps resolution, designed to readout thin Low Gain Avalanche Diodes

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Abstract: This contribution presents a new version of the FAST (Fast Amplifier for Silicon detector for Timing) ASICs, called FAST3, and the more significant results from its characterization. The FAST3-*Analog* version is a 16-channel front-end electronic designed for low power consumption, minimal noise, reduced temporal jitter, and a wide charge input range (3–40 fC). Developed in standard 110 nm CMOS technology, the ASIC is optimized to read out LGAD sensors in timing and tracking applications. The FAST3-*Analog* was extensively characterized in the laboratory using a low-jitter pulser, a $\beta$-source, and during a beam test campaign at DESY. Its performance has been evaluated while coupled with LGADs of different active thicknesses (50 and 80 µm) and pixel capacitances (3.8 and 1.8 pF). Characterization results demonstrated the capability of FAST3 to achieve temporal jitter below 25 ps for charges above 10 fC, and to measure the passage time of charged particles through an LGAD, with a temporal precision of approximately 35 ps.

Keywords: Electronic detector readout concepts (solid-state); Analogue electronic circuits; Front-end electronics for detector readout

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## Contents



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## 1 Introduction

The next generation of High Energy Physics (HEP) experiments will operate at significantly higher instantaneous luminosities, leading to increased pile-up, particularly in the tracker detectors. To mitigate these effects, a new generation of tracker detectors (4D-trackers) [1, 2], are anticipated to become widely adopted for use in the challenging environments of future experiments.

Low Gain Avalanche Diode (LGAD) technology [3], in its various declinations (Trench-isolated LGAD [4], Resistive-Silicon Detector [5]), is a strong candidate for the sensor technology of future 4D-trackers. A key advantage of LGAD technology is its ability to measure the time of passage of a charged particle with a temporal precision of about 25–35 ps, depending upon the sensor thickness. For this reason, high-performance read-out electronic with temporal jitter below 20 ps is essential to preserve the excellent temporal resolution of LGADs.

The FAST family of ASICs [6–8] is a front-end electronic suite specifically designed and optimized for LGADs, capable of achieving a temporal resolution below 40 ps, when coupled with them.

## 2 FAST3 ASICs

The FAST3 ASICs [9] have been developed in two versions, referred to *Analog* and *Digital*. FAST3-*Digital* is a 20-channel ASIC featuring a single-stage amplifier and comparator architecture with differential output in LVDS format. FAST3-*Analog* in a 16-channel ASIC with a double-stage amplifier architecture and a single-ended output. FAST3 ASICs are designed in UMC 110 nm CMOS technology and implemented on a $1.5 \times 5\,\mathrm{mm}^2$ chip, operating on a 1.2 V power rail. This manuscript, along with all results presented within, focuses on the FAST3-Analog version.

### 2.1 FAST3-Analog: main characteristics and architecture

The layout of FAST3-*Analog* is shown in figure 1. The 16 channels are arranged along the short side of the ASIC; with inputs positioned at the bottom and the single-ended outputs at the top. The ASIC is designed to handle input charge levels ranging from 3 to 40 fC, corresponding to the typical

charge range generated by LGADs when a Minimum Ionizing Particle (MIP) passes through. The figure of merit of this ASIC is the very low temporal jitter (< 20 ps) for input charges above 8 fC (based on post-layout simulations). This performance is achieved by combining a low RMS Noise, about 1.1 mV, with a high Signal-to-Noise Ratio (SNR > 90 at 8 fC of charge). Table 1 summarizes the main features of FAST3-*Analog*.

A two-stage amplification chain architecture guarantees the FAST3-*Analog* temporal jitter performance. The first stage is a pre-amplifier implemented as a Trans-Impedance Amplifier (TIA) with a broadband design. An RF transistor is integrated at the input stage, with the aim of preserving the high frequencies components of the typical LGAD signal. Two versions of FAST3-*Analog* have been designed in this pre-amplifier, one of which features programmable gain, while the second one works with default parameters. The programmable version uses three configurable bits to set the feedback resistance value ($R_f$), allowing selection among eight $R_f$ values (including a null value that disconnects the channel) obtained by the parallel combination of three resistors (5 kΩ, 15 kΩ and 30 kΩ). The second stage is a buffer, consisting of an operational amplifier in inverter configuration with a Class AB driver at the output node. The buffer stage was implemented to provide: i) a frequency bandwidth of approximately 1 GHz to preserve the first stage signal rise time of 1.5 ns, ii) a low DC gain (∼ 6) to enhance signal amplitude at low charges, and iii) a large output dynamic rage (∼ 800 mV).

The estimated power consumption for this two-stage amplification architecture is 10 mW/ch divided into 2.3 mW/ch for the pre-amplifier stage and 7.7 mW/ch for the buffer stage.

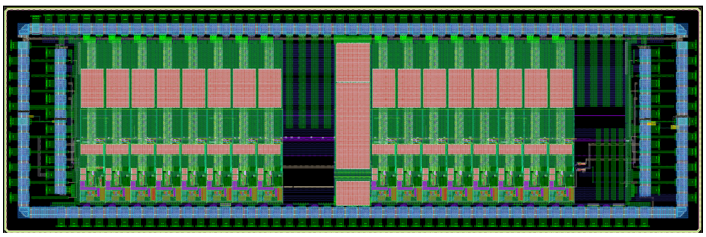

**Figure 1.** Layout of FAST3-*Analog* ASIC. The 16 inputs and single-ended outputs are positioned at the bottom and top, respectively; the lateral pads supply power and controls to the chip.

**Table 1.** Table of specifications of FAST3-*Analog*. The numerical values refer to results obtained in post-layout simulations, with a capacitance of 3.4 pF at the input of the channel.

| | |
|---|---|
| Technology | 110 nm CMOS |
| Chip dimension | $1.5 \times 5\,\text{mm}^2$ |
| Number of channels | 16 |
| Power rail | 1.2 V |
| Power consumption | 2.3 + 7.7 mW/ch |
| Charge input range | 3–40 fC |
| Max voltage output range | 800 mV |
| RMS noise | 1.1 mV |
| Bandwidth | 1 GHz |
| SNR (@$Q$ > 8 fC) | > 93 |
| Temporal jitter (@$Q$ > 8 fC) | < 20 ps |

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## 3 Experimental results

### 3.1 Characterization setups

The characterization of FAST3-*Analog*, both standalone and coupled with LGADs, was conducted with three different measurement setups and using a read-out board where FAST3 and LGAD were attached and wire-bonded, see figure 2 (left).

- *Pulser-setup*: this setup is used to inject charge ($Q$) to the ASIC input to characterize the dynamic range, the gain of the amplification chain, and its temporal jitter. The charge is injected via a capacitor ($C = 0.5$ pF), located on the read-out board. Four capacitors are placed on the board for channels 1, 5, 11, and 16. The pulser setup utilizes the Active Technology PG-1074 pulser, tuned to maintain a constant temporal jitter of 10 ps when injecting a charge $\geq 10$ fC. The output signals from FAST3 were read out by a 4-Channel LeCroy-WaveRunner 9254M oscilloscope, with a frequency bandwidth of 2.5 GHz and a sampling rate of either 20 or 40 GSample/s.

- $\beta$- and *beam test-setup*: these setups were used to measure the temporal resolution ($\sigma_t$) of FAST3-*Analog*, when coupled to an LGAD. For the $\beta$-setup, a $^{90}$Sr-source served as MIP source, while an electron beam of momentum 5 GeV/$c$ was used for the beam test at DESY facility [10]. Both setups utilized a Lecroy-WaveRunner 9254M oscilloscope for data acquisition, with time reference provided by a Photonis Multi-Channel Plate (MCP), with a temporal resolution between 15–20 ps. The setups allowed the characterization of FAST3 coupled to two different LGADs: a 50 µm-thick, $2 \times 2$ pixel-matrix with a pixel capacitance of 3.8 pF (high-$C$ configuration) and an 80 µm-thick single pixel with a capacitance of 1.8 pF (low-$C$ configuration). Since the temporal performance obtained from both setups is fully consistent, we do not distinguish between them in the results presented below.

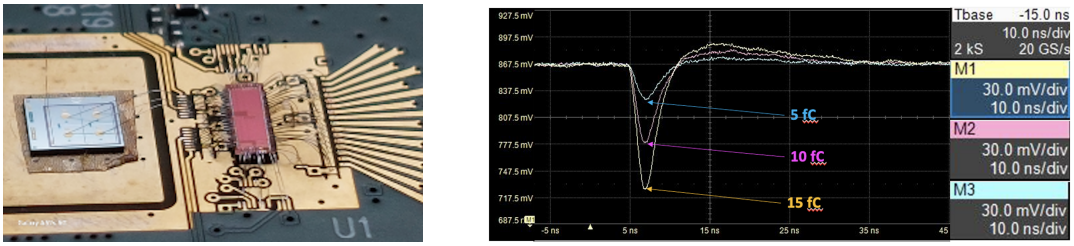


**Figure 2.** Left: FAST3-*Analog* and $2 \times 2$-matrix LGAD attached and wire-bonded to read-out board. Right: typical FAST3-*Analog* output signals generated by the injection of 5 (blue), 10 (magenta) and 15 fC (yellow), through pulser-setup.

### 3.2 FAST3 signal and gain

Typical FAST3 signals generated by the injection of charges (5, 10, and 15 fC) are displayed in the oscilloscope screenshot in figure 2 (right). The FAST3 signal exhibits a leading edge of 1.5 ns, a time duration of 5 ns, and an evident undershoot that becomes more pronounced with larger input charges. This signal shape shows a very good agreement with the expectation from post-layout simulations. The response of FAST3-*Analog*, in terms of output signal amplitude, demonstrates good sensitivity to variations in input charge of the order of fC. Figure 3-left (red markers) shows a linear output dynamic

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range up to 40 fC, with a gain factor of approximately 10 mV/fC and onset of saturation beyond this charge value. The output response is consistent with the simulation predictions (black dashed line).

A notable feature of the FAST3 amplifier chain is the gain response as a function of input capacitance. Figure 3-right shows that for a constant injected charge of 20 fC, the gain decreases as the pixel capacitance at the input of the read-out channel increases.

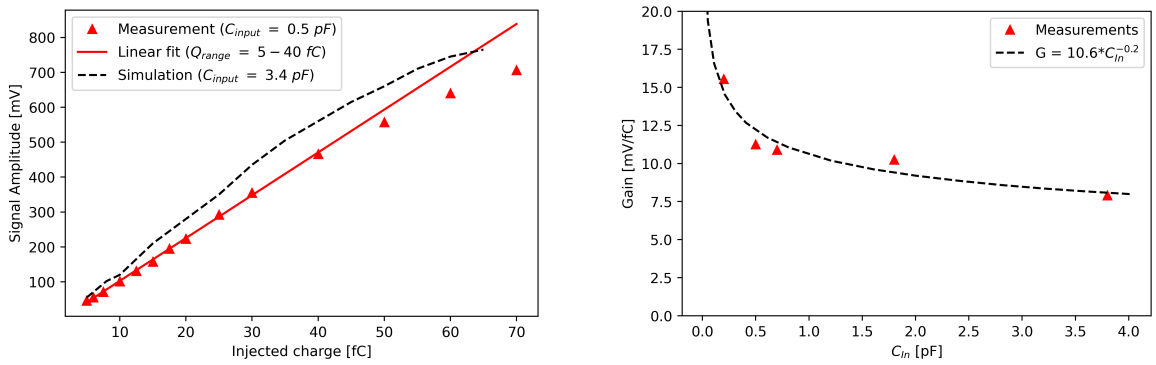


**Figure 3.** Left: evolution of the output signal amplitude as a function of the injected charge: measurements and their linear fit (red markers and line), simulation (black dashed line). The experimental measurements were carried out with an input capacitance of 0.5 pF, while the simulation with 3.4 pF. Right: relationship between amplification factor of the FAST3 channel and the value of the capacitance at the input of the channel.

### 3.3 Temporal performance: jitter and resolution

The primary figure of merit of FAST3 is its temporal jitter. Jitter is measured using the pulser setup and selecting two different frequency BWs on the oscilloscope: 2.5 GHz (full BW) and 500 MHz. To quantify jitter, we used the Constant Fraction Discriminator (CFD) method at the 50% of the leading edge of the signal, referred against the trigger signal provided by the pulser. The measured temporal jitter as a function of the injected charge is shown in figure 4-left. Results indicate that limiting the data acquisition BW to 500 MHz improves the temporal resolution (green markers) and the agreement with post-layout simulation (black dashed line). The temporal performance characterization of FAST3 was completed by extracting the temporal resolution from the two FAST3-LGAD couplings described in section 3.1. Both investigated sensors operate in a range of internal gain 10–60, typical of LGAD technology. The results presented below refer to $\beta$ and beam test data, acquired with a BW limitation of 500 MHz. The analysis of data showed that the pixel capacitance influences the gain of the readout chain (section 3.2), the RMS Noise, and the slew rate of the readout signals. The low-$C$ configuration, when compared with high-$C$ ones, exhibited a slightly higher RMS noise (0.7 mV versus 0.6 mV) and, conversely, higher slew rate values for the same input charge. Overall, differences in gain, noise, and slew rate resulted in comparable SNR values across both configurations and in agreement with post-layout simulation expectations. As shown by $\beta$ data in figure 4-right, both FAST3-LGAD configurations achieved a temporal resolution of 35 ps. On beam test dataset, we achieve a temporal resolution below 40 ps, and the measured values are comparable with those obtained on $\beta$ dataset. These results demonstrate the excellent performance of FAST3-*Analog* in the timing of passage of a charged particle in a thin LGAD.

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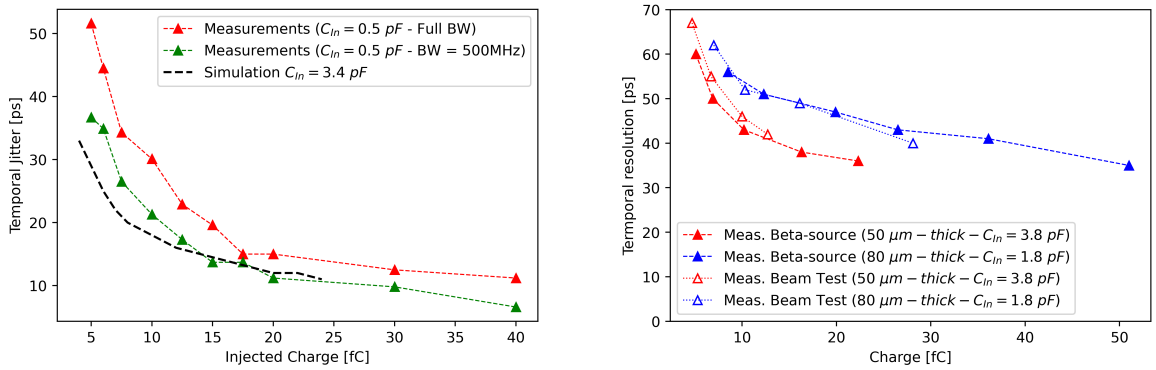


**Figure 4.** Left: temporal jitter as a function of injected charge, measured using the pulse setup with the data acquisition BW of 2.5 GHz (red markers) and 500 MHz (green markers), compared with simulation results. Right: the temporal resolution of FAST3-LGADs with a sensor of active thickness (pixel capacitance) of 80 µm (1.8 pF) (blue markers) and 50 µm (3.8 pF) (red markers). The empty and filled markers refer to beam test and $\beta$ data, respectively.

## 4 Conclusion

FAST3-*Analog* is a low-power, low-noise, 16-channel ASIC optimized to readout LGAD sensors. Designed in 110 nm CMOS technology, the ASIC provides an input/output dynamic range up to 40 fC/800 mV and achieves a temporal jitter below 25 ps. These design specifications have been confirmed through laboratory measurements using a low-jitter pulser setup. The pulser characterization highlighted two critical features of FAST3: i) the optimal temporal jitter is achieved by limiting the frequency BW of the acquisition system to 500 MHz; ii) the pixel capacitance at the input of the ASIC channel influences the gain of the amplification chain (higher capacitance reduces the channel gain). The temporal performance of FAST3, coupled to LGAD, was further evaluated using $\beta$-source and during beam test, confirming the capability of the ASIC to reach a temporal resolution of approximately 35 ps. In conclusion, FAST3-*Analog* is an excellent multi-channel amplifier, suitable for *R & D* activities on LGADs and as front-end electronics in experiments requiring a moderate number of channels and precise time-tracking capabilities.

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