Jinst

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 5, 2025*
REVISED: *March 26, 2026*
ACCEPTED: *April 1, 2026*
PUBLISHED: *April 24, 2026*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS
RETHYMNO, CRETE, GREECE
6–10 OCTOBER 2025

PRISME: a radiation tolerant low power Phase-Locked Loop in a 65 nm technology for precision clocking at EIC

F. Bouyjou,[a,*] **C. Flouzat,**[a] **O. Gevin,**[a] **I. Mandjavidze**[a] **and D. Neyret**[a]

[a] *Université Paris-Saclay, CEA, IRFU,*
91191 Gif-sur-Yvette, France

E-mail: florent.bouyjou@cea.fr

ABSTRACT: The proposed PRISME chip contains a new Phase-Locked Loop IP block for clock signal generation with a jitter lower than 10 ps and a radiation tolerance up to 300 Mrad. To be compatible with a large range of applications at the Electron-Ion Collider and at the Large Hadron Collider, it needs to accept a large input frequency range (80 MHz and 100 MHz), with output frequencies within 1.6–2 GHz. It is designed in TSMC 65 nm technology to allow its integration in future readout ASICs, such as the SALSA chip for readout of micro pattern gaseous detectors. Test results in agreement with simulations are well within the application requirements of the SALSA ASIC. The Phase-Locked Loop occupies an area of 0.07 mm^2 and consumes 6.2 mA from a 1.2 V supply. The output jitter integrated from 5 kHz to 80 MHz is 1.26 ps rms for a frequency division ratio of 20.

KEYWORDS: Analogue electronic circuits; Digital electronic circuits; Radiation-hard electronics

2026 JINST 21 C04066

---

[*] Corresponding author.

https://doi.org/10.1088/1748-0221/21/04/C04066

2026 JINST 21 C04066

Contents

1 Introduction

Many elements in electronics for modern particle physics experiments require very precise, low jitter clock signals, and need to operate in extreme environments. Examples include clock distribution systems, analog and time to digital converters and gigabit serial links [1]. To accept a clock reference of 80 MHz or 100 MHz and be compatible with both the Large Hadron Collider (LHC) and Electron-Ion Collider (EIC) applications, the SALSA chip [2] for micro pattern gaseous detectors (MPGD) readout, needs a wideband Phase-Locked Loop (PLL) rather than a readily available PLL. This new PLL design features a digital control loop, described in section 2, offering a noticeable jitter improvement as illustrated in section 2.1, while requiring little additional area and energy.

2 Proposed wideband low-jitter PLL

A well-made PLL typically shows an in-band noise dominated by the charge pump (CP) and an out-of-band noise dominated by the voltage-controlled oscillator (VCO). A higher CP gain helps to suppress in-band noise more effectively by responding more strongly to PLL phase errors, but makes the PLL more sensitive to spurs from CP injection and mismatch, increasing deterministic jitter. A Track-and-Hold Charge Pump (THCP) can offer a solution to this compromise.

2.1 T/H charge pump

CPs suffer from several imperfections (current mismatch, charge sharing, clock feed-through, and charge injection) causing undesired spurs at the PLL reference frequency. Implementing a THCP [3] can help to mitigate some of the issues associated with increasing of the CP gain. The principle is based on sampling the rising edge of the CKDIV (slowed down in a T/H capacitor CTH) at rising edge of CKREF and storing this voltage proportional to the phase difference, in CTH. An operational transconductance amplifier (OTA) then compares this stored voltage with a fixed control voltage VCM to generate an output current ITHCP proportional to the difference between the two voltages. At the

OTA output, the current is injected into the PLL filter node using a pumping switch closed for a pulse width duration TPW. This approach holds the CP output constant over multiple phases, reducing jitter, noise, up/down current imbalance, and the dead zone inherent to classical CP designs.

2.2 Multi-band VCO implementation

With a reduced VCO gain K_{VCO} to mitigate the higher frequency deviations, the PLL may not be able to cover the required frequency range with a single VCO band. The multi-band VCO architecture switches between different frequency bands. The K_{VCO} is now divided by the number of bands allowing to maintain the desired performance across the entire frequency range [4]. Multiple current sources, controlled by a 7-bit control code, are switched in and out to cover different frequency bands over a wide range, improving the stability and performance of the PLL without significantly compromising the K_{VCO}. The VCO band for the PLL is selected by the automatic frequency control (AFC) block shown in figure 1 which continuously scans the control voltage V_{CTRL} and checks if it reaches saturation levels, below 0.2 V (DN) or above 1 V (UP). If so, it triggers a hysteresis time circuit and if the programmed time is exceeded, it increments or decrements a counter, depending on the region where the signal is saturated, either DN or UP. This shifts the current source to allow the desired band to be reached by the analog proportional part.

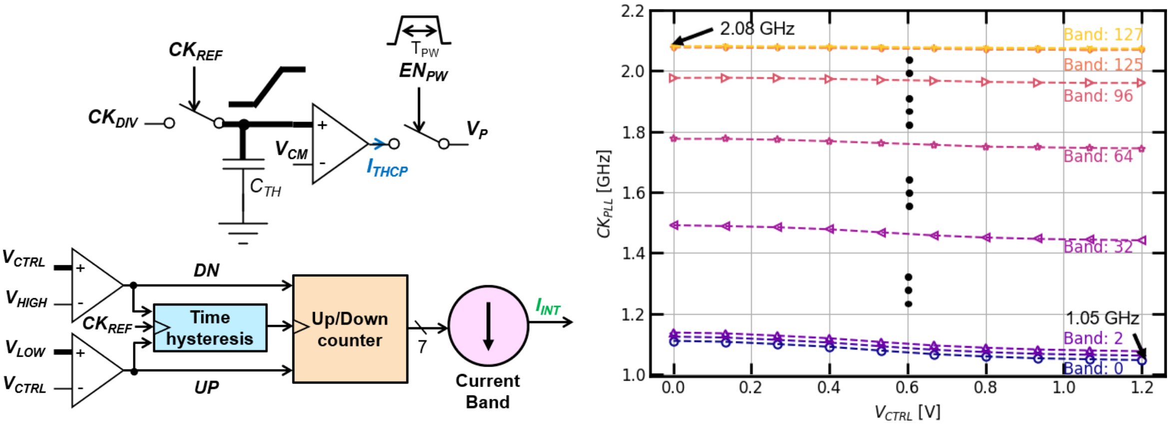

Figure 1. T/H charge pump (top left). Automatic Frequency Control block diagram with 128 bands (bottom left) and the VCO band cover range (right).

This approach enables a wide-range ring VCO suited to CERN and EIC clock domains, with improved frequency tuning linearity and a constant K_{VCO} across the full V_{CTRL} range. The VCO operates from 1 GHz to 2 GHz, covering the frequency range compatible with the EIC (100 MHz = 2 GHz/20) and LHC (80 MHz = 1.6 GHz/20) acquisition systems. The VCO has been optimized over the full frequency band and V_{CTRL} range for low jitter (integration range 500 kHz–10 GHz) in order to achieve few ps rms (see simulations in figure 2).

The K_{VCO} is also verified within the range, and a K_{VCO} drop can be observed from 14 to 2 MHz/V, which will need to be improved in a future iteration in order to achieve a more consistent gain.

2026 JINST 21 C04066

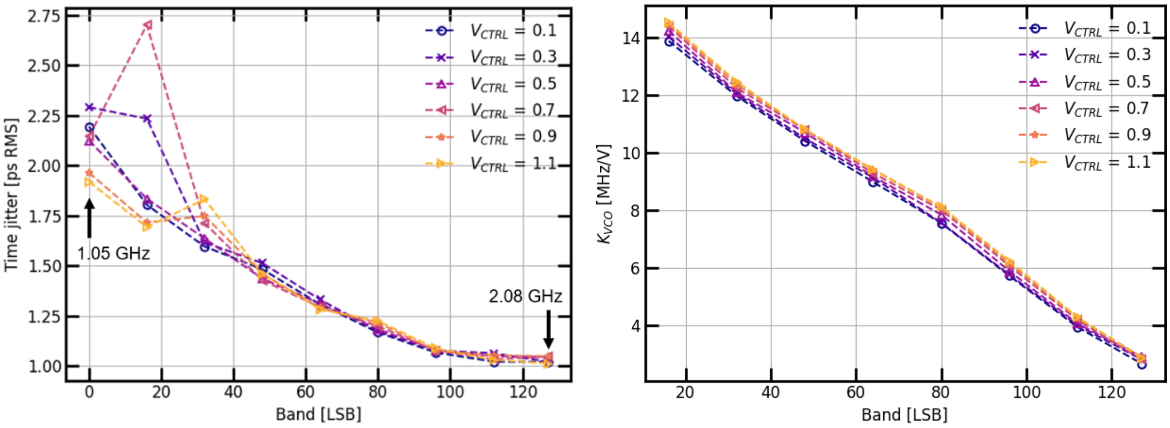

Figure 2. Simulation results of VCO time jitter (integration range 500 kHz–10 GHz) (left) and the VCO gain K_{VCO} throughout the output band range and for multiple VCTRL input voltages (right).

2.3 PLL implementation in PRISMEv1 chip

The block diagram of the proposed PLL is presented in figure 3. The PLL includes a phase detector with a traditional CP, the THCP and the loop filter node (BW = 500 kHz). In THCP mode, the CP is used for the band lock phase. The two modes can be forced independently in order to compare the performances between them. The VCO control is composed of a voltage to current converter (V2I) for the proportional path and the AFC for the integral path. The sum of these two currents provides the operating current of the ring oscillator (CCRO). Finally, a frequency divider by 20 is implemented to create CK_{DIV} and a mode control block is added to shift between CP and THCP configurations with EN_{CP} and EN_{THCP} controlled signals.

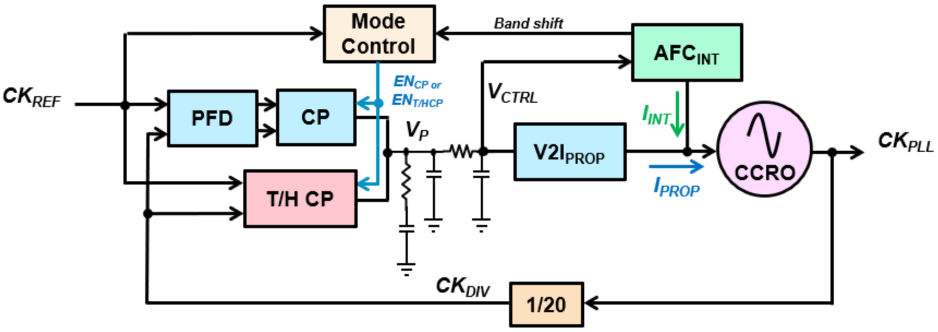

Figure 3. Block diagram of the proposed PLL.

The PLL block is integrated into the PRISMEv1 ASIC designed in TSMC 65 nm CMOS process. Figure 4 shows the block diagram of the PRISMEv1 ASIC, mainly composed by the PLL presented previously and 4 programmable outputs (fanout). The die size dimensions are 1500×1500 μm^2 and the PLL active size is 430×160 μm^2.

The 4 programmable outputs allow fractions of VCO frequency to get out, up to 1 GHz and also phase shifts to be made in steps of ~500 ps according to the VCO frequency. Efforts have been made to harden the design in SEE/SEU by using TMR technique in the PLL. Particular attention has been paid

2026 JINST 21 C04066

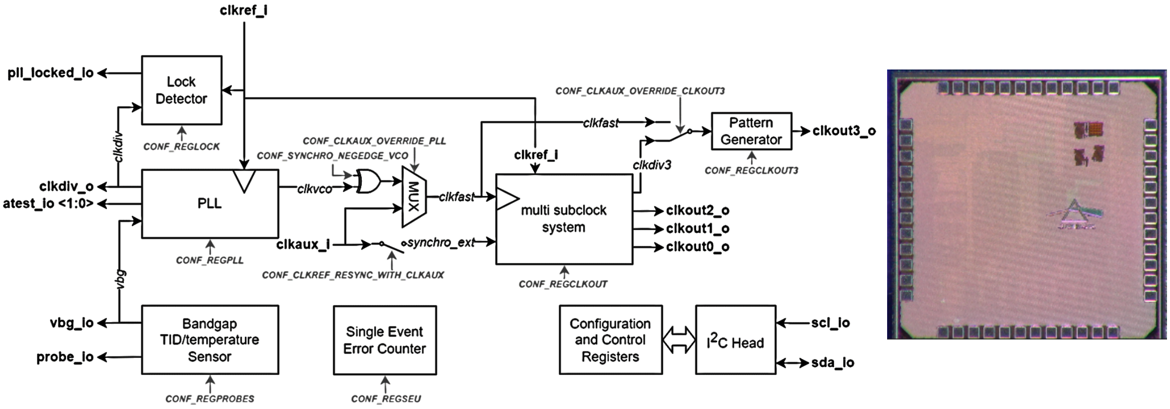

Figure 4. Block diagram of PRISMEv1 ASIC (left) and its micrograph (right).

to the loop counter and AFC blocks to avoid erroneous changing of frequency bands. The PRISMEv1 logic and the I2C circuitry are also triplicated. The CERN radiation hardened RX and TX IPs are used.

3 PRISMEv1 measurement results

For thorough characterization of the PLL, its $\mathrm{CK_{REF}}$ input was fed by a clock from Si5344 evaluation board [5]. The PLL outputs were analyzed using the Tektronix MSO64B 10 GHz 50 GS/s oscilloscope [6]. At power-up, the AFC system reached the desired band without external intervention. Measurements of the PLL noise characteristics at the $\mathrm{CK_{DIV}}$ output show that the PLL VCO covers a wide frequency range from 1.18 to 2.1 GHz [59–105 MHz $\mathrm{CK_{DIV}}$] as shown in figure 5. This range is in good agreement with simulations.

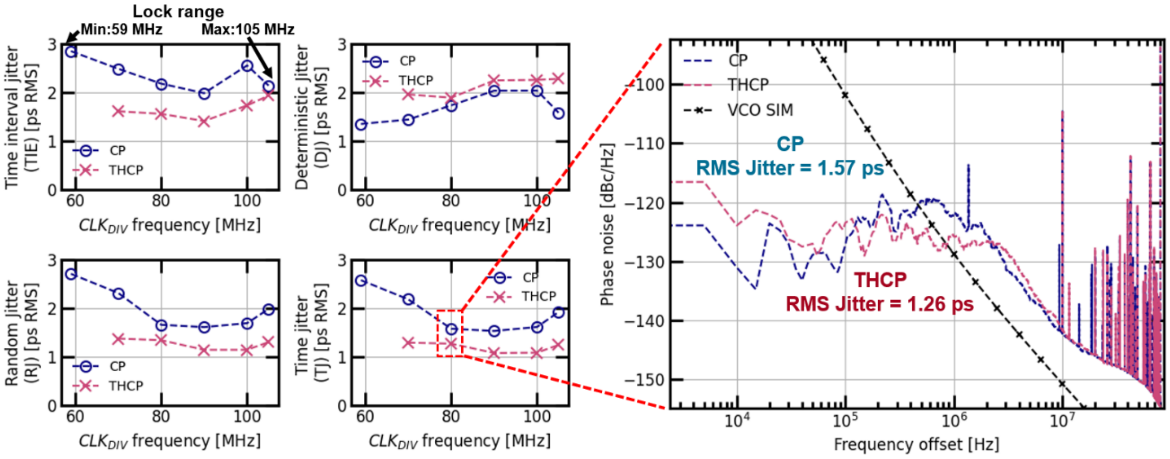

Figure 5. Measured jitter performances (integrated range 5 kHz-$\mathrm{CK_{DIV}}$) over the clock input range.

The PLL performance has been studied over the entire input frequency range (5 kHz-$\mathrm{CK_{DIV}}\,y$). The time interval, random and deterministic jitter components as well as the phase noise were measured. Figure 5 shows that an excellent time jitter from 1.5 to 2.5 ps rms was achieved in CP mode, further reduced by 20% to 1.1 to 1.3 ps rms in THCP mode.

Less than −120 dBc/Hz in-band noise level was measured. In addition, simulation of the VCO phase noise (VCO oscillating at 1.6 GHz i.e. 80 MHz at PLL input) is shown in the figure 5. Figure 6

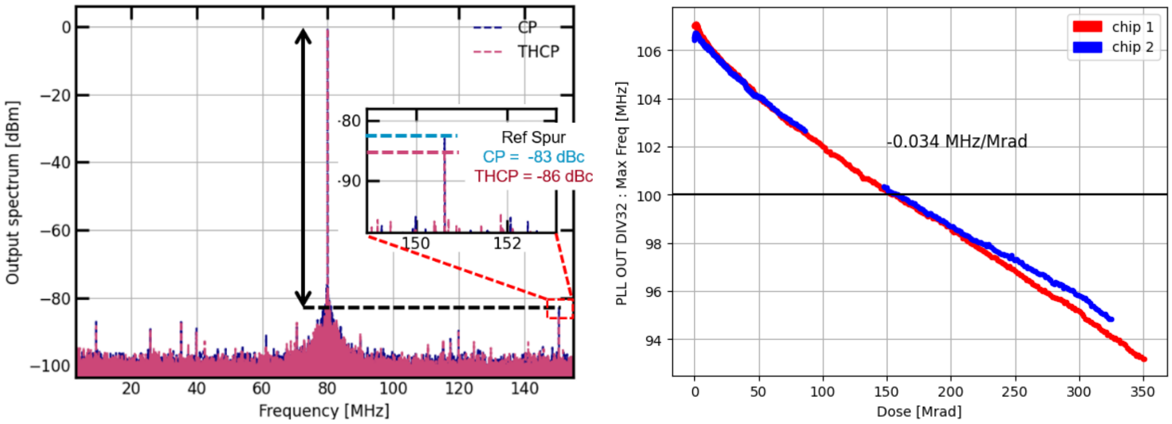

Figure 6. Output spectrum of the proposed PLL at 80 MHz reference frequency for PRISMEv1 (left) and PLL max output frequency of PRISMEv0 chips as function of TID (right).

shows the measured spectral performance of the proposed PLL. The reference spur of the PLL at 80 MHz carrier frequency is −83 dBc for the CP mode and −86 dBc for the THCP mode showing a 3 dBm spur reduction compared to the CP mode.

The power consumption of the PLL is 6.2 mW @ 1.6 GHz. The 1.2 V power consumption of the entire chip is 90.6 mW, including the 4 TX drivers.

The radiation tolerance of the design has been evaluated on a previous version of the PLL – PRISMEv0. The TID measurements performed on two PRISMEv0 chips have shown a decrease of 34 kHz/Mrad of the maximum frequency that the VCO can provide (figure 6). For the targeted reference frequency of 100 MHz, we showed that the PLL VCO can survive the doses of up to 150 Mrad.

Table 1. PRISMEv1-PLL performance summary.

Parameter	Value
Reference-range	59–105 MHz
Output-range	1.18–2.1 GHz
Power	6.2 mW @ 1.6 GHz
Active area	0.07 mm^2
RMS jitter (Int. range)	1.26 ps @ 80 MHz Ref. clock (5 kHz–80 MHz)
Ref. spur	−86 dBc

4 Conclusion

A wide-range, low-noise PLL was developed and validated in the PRISMEv1 chip for EIC and LHC experiments (table 1), implemented in 65 nm process with a 430×160 μm^2 area. The VCO covers 59–105 MHz input tuning range with adjustable current sources, lightens the trade-off between phase noise and power consumption. The measurement results show that the PLL tuning range output is 1.18 to 2.1 GHz, the jitter of the output clock in CP and THCP mode are respectively 1.57 ps@1.6 GHz and 1.26 ps@1.6 GHz and the reference spurs are −83 dBc@1.6 GHz and −86 dBc@1.6 GHz. Beyond the

2026 JINST 21 C04066

PLL core, PRISMEv1 integrates four programmable clock outputs, internal temperature and radiation sensors, and triplicated I^2C slow control. TID measurements on PRISMEv0 (2024) established a 150 Mrad threshold for the VCO; an improved tolerance is anticipated for PRISMEv1, with a TID campaign planned for 2026. The PLL will be integrated into SALSA (See "SALSA: a new versatile ASIC for the readout of MPGD detectors" submitted to JINST proceedings for TWEPP25) to provide clock references for its ADCs, CDR and serial links.

Acknowledgments

The authors would like to thank the European Organization for Nuclear Research (CERN), EP-ESE group for IPs and TID support and the "Generic EIC R&D Program" [7] for having supported this work and for funds.

References

[1] P. Moreira et al., *lpGBT: Low-Power Radiation-Hard Multipurpose High-Speed Transceiver ASIC for High-Energy Physics Experiments*, *IEEE Trans. Nucl. Sci.* **72** (2025) 24.

[2] D. Neyret et al., *SALSA: a new versatile readout chip for MPGD detectors*, 2025 *JINST* **20** C06057 [`arXiv:2501.10237`].

[3] C.-T. Ko, T.-K. Kuan, R.-P. Shen and C.-H. Chang, *A 7-nm FinFET CMOS PLL With 388-fs Jitter and* −80*-dBc Reference Spur Featuring a Track-and-Hold Charge Pump and Automatic Loop Gain Control*, *IEEE J. Solid-State Circuits* **55** (2020) 1043.

[4] W. Zou, D. Ren and X. Zou, *A wideband low-jitter PLL with an optimized Ring-VCO*, *IEICE Electron. Express* **17** (2020) 20190703.

[5] Skyworks Solutions Inc., *Si5344-D-EVB and Si5344 High-Performance Clock Jitter Attenuator, Jitter Cleaner*, `https://www.skyworksinc.com/products/timing/high-performance-jitter-attenuators/si5344`.

[6] *Tektronix MSO64B 6 Series B MSO Mixed Signal Oscilloscope*, `https://www.tek.com/en/products/oscilloscopes/6-series-mso`.

[7] Thomas Jefferson National Accelerator Facility (Jefferson Lab), *Generic EIC-related Detector R&D Program*, `https://www.jlab.org/research/eic_rd_prgm`.

2026 JINST 21 C04066