Published by IOP Publishing for Sissa Medialab

Received: *September 15, 2025*
Revised: *October 30, 2025*
Accepted: *December 13, 2025*
Published: *January 14, 2026*

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

Design, simulation and characterization of the ALICE ITS3 MOSS analog front-end

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Abstract: The upgrade of the ALICE vertex detector (ITS3) with wafer-scale stitched MAPS targets an orthogonal MIP detection efficiency > 99 %, with a fake-hit rate < 0.1 pixel^{-1}s^{-1} and a power budget of 40 mW/cm^2. The MOSS wafer-scale monolithic sensor analog front-end, featuring ~ 0.55mV/e$^-$ gain and < 15 e$^-$ rms noise and threshold dispersion each, was designed, prototyped and measured, confirming these performance targets. Measurement results suggest that the on-chip digital readout signal (strobe) injects noise into the pixel matrix. This effect can be suppressed in future prototypes to further improve the signal-to-noise ratio. In this work, front-end design, simulation and measurement results will be presented together with a discussion on the observed strobe-related effect.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Pixelated detectors and associated VLSI electronics

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https://doi.org/10.1088/1748-0221/21/01/C01011

Contents

1 Introduction

In view of the ALICE Inner Tracking System upgrade (ITS3) at CERN, a prototype monolithic sensor ASIC, the Monolithic Stitched Sensor (MOSS), has been developed [1, 2]. It targets an orthogonal minimum ionizing particle (MIP) detection efficiency greater than 99 %, with a fake-hit rate (FHR) less than 0.1 hits/pixel/s and a power budget of 40 mW/cm^2. Designed in a 65 nm CMOS imaging technology, it uses stitching to cover a large area (25.9 cm × 1.4 cm) within a single die. To minimize the detector material budget (0.09 %X_0 per layer), power and data transmission are integrated on chip. MOSS implements two distinct pixel matrices with different pixel pitches to study the effect of layout density on yield: one with 256 × 256 pixels and a pitch of 22.5 µm; the second one with 320 × 320 pixels and a pitch of 18 µm. Although the matrix geometry differs, the periphery and in-pixel circuitry are identical, and four variants of the front-end using the same circuit topology and different transistor sizes were implemented. Since their performance is similar, only results from one of the variants are reported in this paper.

2 Analog front-end design and simulations

The analog front-end implemented in MOSS is derived from a compact and low power front-end prototyped in the same 65 nm CMOS imaging technology [3]. It continuously resets the collection electrode while amplifying and digitizing the signal induced by the charge released in the sensor. The MOSS front-end is an open-loop voltage amplifier which integrates charge directly on the sensor capacitance. This approach exploits the < 5 fF sensor capacitance efficiently, yielding a signal of tens of mV for a MIP (∼ 600 e$^-$) [4].

The schematic is shown in figure 1. The sensor, represented by the diode D0, is directly coupled to the circuit. The input transistor M1 operates in source-follower configuration to reduce the contribution of its gate-source capacitance to the sensor capacitance, and it is biased by M0 (I_{bias}). Upon a particle hit, the induced current generates a voltage signal $\Delta V = Q/C_{\text{in}}$ on the input capacitance. This signal is replicated on the source of M1 and transferred to M2, which acts as a common-source amplifier. A folded cascode stage (M4) further enhances gain, with biasing provided by M9/M8 (I_{biasn}) and set to 1/10 of the main current I_{bias}. In the first branch, a pMOS level shifter (M3) is inserted to increase the bias voltage of the sensor and improve the operating margins of the input

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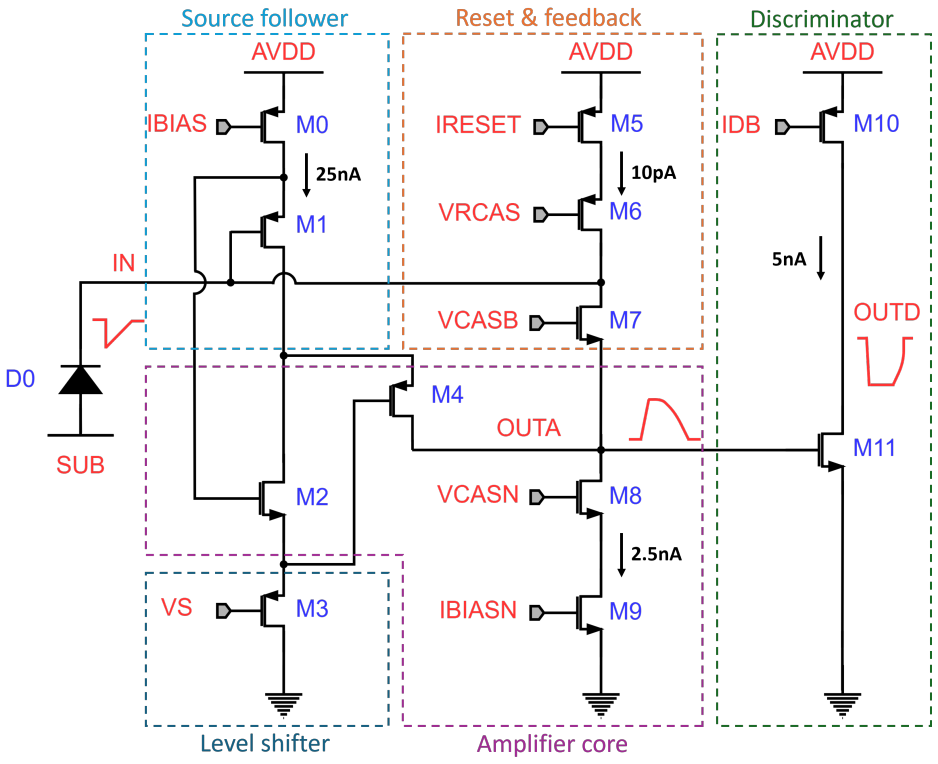

Figure 1. MOSS in-pixel analog front-end.

transistor. Feedback is provided by transistors M5–M7, which adjust the DC operating point of the input node. The same network also compensates for sensor leakage current and resets the electrode after a hit. Because the reset must be sufficiently slow to avoid filtering the high-frequency input signals, I_{reset} is kept small (10 pA), also limiting its shot noise contribution. The analog output (OUTA) is digitized by transistors M10-M11, which constitute the discriminator. In steady state, M10 pulls up the discriminator output OUTD. Upon an input stimulus, the amplifier output rises, turning on M11. If OUTA is sufficiently large, M11 discharges OUTD to the ground and a hit is registered. As a result, the charge threshold is a function of the amplifier gain, its output baseline (set by V_{casb} and I_{reset} biases) and the discriminator bias I_{db}.

To be within the ALICE ITS3 power budget of 40 mW/cm^2, the analog front-end is required to consume less than 30 nA (corresponding to 11 mW/cm^2 in the 18 µm pixel pitch matrix). Since the I_{reset} current is only 10 pA and the discriminator standby current can be set as low as 5 nA, the maximum I_{bias} current allowed is 25 nA. A larger value of this current would be beneficial for the front-end performance in terms of threshold dispersion, noise and response time.

Transistor sizing and layout were optimized iteratively using post-layout simulations, with the goal of minimizing the input equivalent noise charge (ENC) and pixel-to-pixel mismatch. Further improvements can be obtained at the sensor level. In particular, applying a negative voltage to the substrate, the sensor capacitance decreases, hence a larger voltage signal is induced at the input for the same charge. Nominal substrate voltage used in the MOSS chip is −1.2 V and the corresponding sensor capacitance set in simulation is 2 fF. The simulated front-end gain is 0.6 mV/e$^-$ for a 200 e$^-$ input charge (around target threshold). Monte Carlo and transient noise simulations

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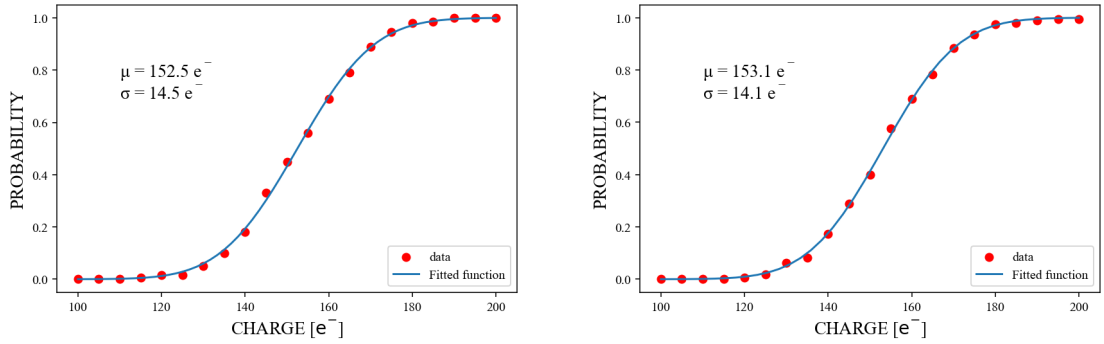
were performed to estimate pixel-to-pixel threshold variation and the ENC. The curves shown in figure 2 report the simulated hit probability as a function of the input charge. For each value of charge 200 runs were performed. Fitting the S-curves with the formula $\frac{1}{2}\left(1+\mathrm{erf}\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right)$ yields the front-end nominal threshold, $\sim 153\,\mathrm{e}^-$, the pixel-to-pixel threshold variation, $14.5\,\mathrm{e}^-$ (figure 2(a)), and the ENC, $14.1\,\mathrm{e}^-$ (figure 2(b)).



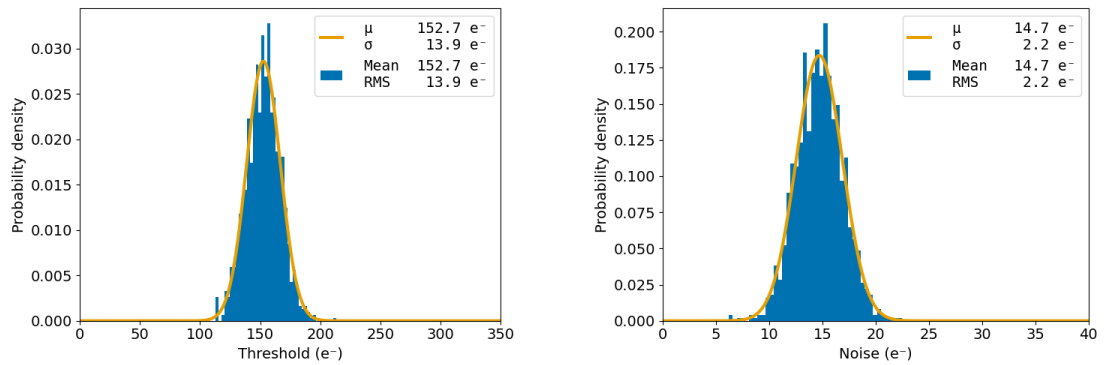
(a) S-curve for simulated transistors' mismatch.

(b) S-curve for simulated transistors' noise.

Figure 2. Simulated mismatch and noise hit probability vs input charge.

3 Measurement results

The MOSS front-end was characterized in laboratory relying on the in-pixel pulsing circuitry, which injects a tunable charge into the collection electrode. The injection capacitance was calibrated measuring time-over-threshold while exposing the chip to a ^{55}Fe source. Threshold and noise were measured for each pixel through charge test injections, and the resulting S-curves were fitted using the same method as in the simulations. The distributions of threshold and noise for a MOSS pixel matrix are reported in figure 3. The measured average threshold is $\sim 153\,\mathrm{e}^-$ with a standard deviation of $13.9\,\mathrm{e}^-$ (figure 3(a)). The measured average noise is $14.7\,\mathrm{e}^-$ (figure 3(b)). These values agree closely with the simulation results.



(a)

(b)

Figure 3. Measured distribution of threshold and ENC.

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FHR was evaluated by repeatedly reading out the pixels without external stimuli, while the efficiency was measured in a 7 GeV/c hadron beam at the CERN PS using a telescope with six reference planes [5]. The results are summarized in figure 4, comparing different radiation levels. The non-irradiated front-end fulfills the ITS3 specifications in terms of detection efficiency larger than 99 % and FHR lower than 0.1 hits/pixel/s over a wide range of thresholds ($\sim 70\,e^-$). This operational margin degrades after irradiating the chip with ionizing and non-ionizing radiation, due respectively to increased front-end and sensor shot noise. However, the tested doses exceed those expected in ITS3 by more than a factor of two, so sufficient operational margins remain.

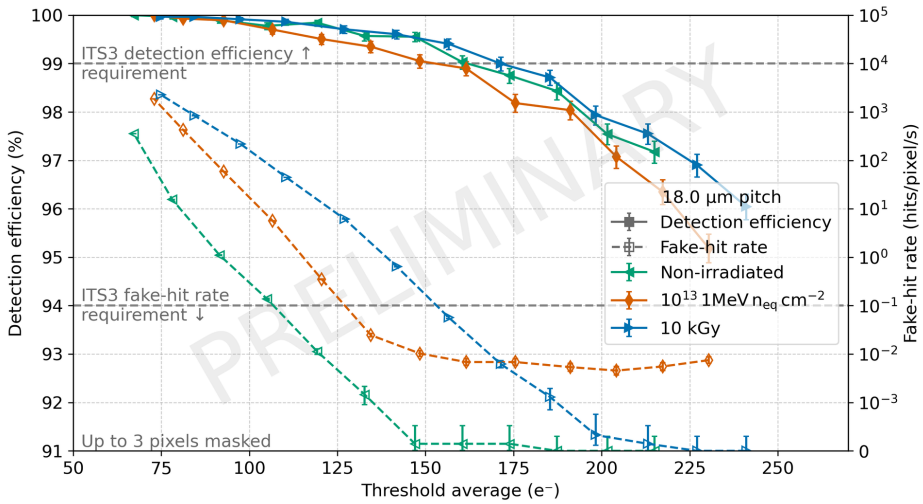

Figure 4. Detection efficiency and FHR as a function of the average charge threshold.

4 Perturbation from on-chip global digital control (strobe)

During characterization, a systematic variation of the measured FHR across the columns of the pixel matrix was observed. Further analysis revealed a dependence of the FHR on the duration of the global digital strobe signal, which defines the sensing window for data acquisition (figure 5(a)). Assuming random noise dominance, the FHR should be independent of strobe length. Figure 5(a) shows a peak in FHR about 2 µs after strobe assertion, consistent with the front-end response time for small charges, indicating noise injection related to the edge of the strobe signal. A spatial trend is also evident: figure 5(b) shows a systematic column dependence of the average threshold variation measured using the on-pixel pulsing circuit, which evolves with the delay between strobe and charge injection. For longer strobe-to-injection delays, the variation of the measured threshold across the columns is reduced. This temporal fading suggests that an edge on the strobe signal causes a dynamic perturbation that relaxes over time. strobe is distributed across the matrix as shown in figure 5(c) and crosses the bias lines (IBIAS, IDB, IRESET, IBIASN, VSHIFT, VCASB, VCASN, VRCAS, the position of the bias generator for each bias is shown at the bottom of figure 5(c)) every two pixel rows. The origin of the perturbation can be traced to capacitive coupling related to these crossings between strobe and the bias lines ($\sim$ 80 aF per crossing).

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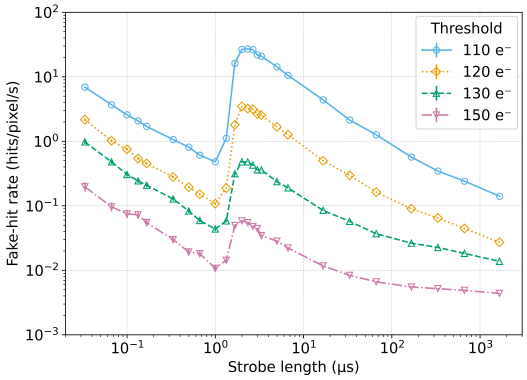
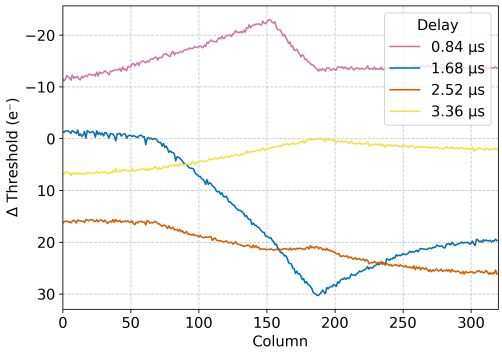
Simulations using a model that includes the extracted parasitic capacitance and resistance of the strobe and of the bias lines across the pixel matrix confirm this mechanism. Figure 5(d) shows the analog output response for different column positions when a strobe is applied at 4 µs (no charge applied to the pixel input). The perturbation amplitude and recovery time depend on the column (in particular, it depends on the distance of the column to each bias generator), consistently with the measured column trend. Although the effect cannot be exactly reproduced in simulation, the evidence indicates that the strobe signal perturbs the front-end via the bias network and is responsible for the apparent FHR increase.

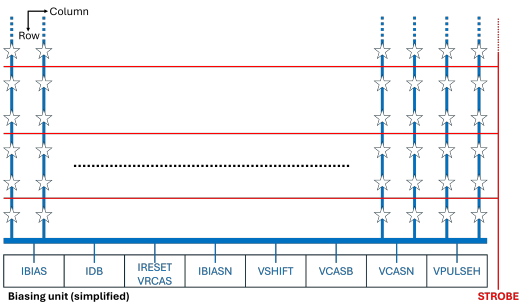
This issue has been addressed in the next prototype, MOSAIX (Monolithic Stitched Active pIXel sensor) [6]. In this design, the global control was changed from a level-based strobe to a short pulse (named frame), whose falling edge counterbalances the noise injected on the rising edge. In addition, the analog and digital domains are completely separated in routing, avoiding any crossings between analog and digital nets and thus suppressing capacitive coupling. The intrinsic front-end performance in terms of FHR is therefore expected to be further improved compared to MOSS.



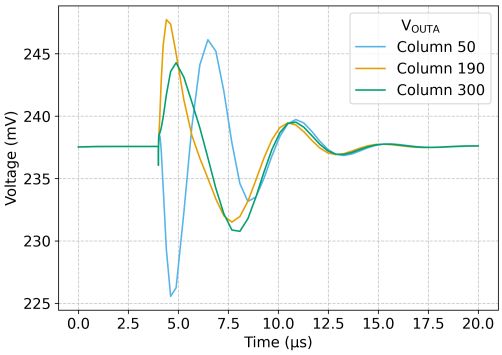
(a) FHR vs Strobe length.



(b) Column profile of threshold variation for different delays between strobe and charge injection. The reference threshold is measured at a delay of 8.8 µs, where the perturbation is recovered.



(c) Strobe and biases distribution. Stars representing pixels.



(d) Simulated front-end analog output with strobe sent at 4 µs.

Figure 5. Strobe effect.

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5 Conclusion

The MOSS analog front-end was designed, simulated, and measured within the framework of the ALICE ITS3 upgrade. Simulations were found to predict front-end performance accurately, both in terms of noise and pixel-to-pixel variation. Beam tests confirm an efficiency above 99 % and FHR below 0.1 hits/pixel/s. A systematic effect linked to the global strobe signal was identified and attributed to capacitive coupling into the bias network, which produced column-dependent perturbations. Design modifications have been implemented in the MOSAIX chip to address this issue. These results demonstrate that the MOSS front-end meets the ITS3 specifications under the required power budget and provide critical input for the final full-scale detector.

Acknowledgments

This work was conducted in the framework of the CERN Experimental Physics Research & Development program (work package 1.2) in collaboration with the ALICE ITS3 project.

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