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Development of a triggerless readout energy measurement and timestamp ASIC for silicon microstrips sensors

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Abstract: The new and second version of ToASt (Torino ASIC for STrip detectors) as a radiation-tolerant readout for silicon microstrips sensors has been produced, and it is now under characterization. It is implemented in a 110 nm commercial CMOS technology, and it is synchronous to a 160 MHz clock. A common time stamp is used to provide both particle time of arrival and particle energy information with the Time over Threshold technique. Triple logic is applied to all configuration registers of the 64 channels and in the global logic circuit for protection against single-event upsets. An enclosed gate layout has been used to protect the analog switches against total ionizing dose leakage.

Keywords: Front-end electronics for detector readout; Radiation-hard electronics

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Contents

1 Introduction

The development of a triggerless readout energy-measuring and timestamp ASIC for silicon microstrip sensors is in the framework of a future experiment dedicated to antiproton physics (PANDA- Antiproton annihilations at Darmstadt) at FAIR (Facility for Antiproton and Ion Research). The PANDA experiment includes a Micro Vertex Detector [1] with double-sided silicon microstrip sensors, and it is triggerless with a delivered clock signal of 160 MHz frequency. It means that a trigger signal generated fast enough to provide the decision to store an event of interest among all the others is absent. Therefore, all data above a fixed threshold at the front-end level is transmitted to the data acquisition system.

The development of a triggerless readout for microstrip sensors indicated the way for the design of a custom integrated circuit named ToASt (Torino ASIC for microStrip detectors) [2], which implements the requirements of the PANDA experiment, summarized in table 1.

Table 1. ToASt specifications.

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max. rate per strip		40	kHz
Input charge	1	40	fC
Charge resolution	8		bit
Noise		≤1500	e^-
Preamp. peaking time	50	100	ns
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Radiation tolerance		20	kGy

The ASIC is a full-size chip with 64 channels and an area of $4.5 \times 3.5\,\text{mm}^2$, with pads on only two opposite sides and power consumption limited to 256 mW for the whole circuit. The ASIC is implemented in a commercial 110 nm UMC CMOS technology. The protection against single-event upsets in the control logic has been implemented using the Triple Modular Redundancy (TMR) technique working with the TMRG tool [3].

2026 JINST 21 C04010

The new and second version of ToASt, named ToASt2, has been designed and produced to improve robustness against Single Event Upset (SEU) and increase tolerance to the Total Ionizing Dose (TID) leakage compared to the first version of ToASt chip [4], which is named ToASt1 in this paper. For the first point, the triplication error in the Verilog code for the TMR layout was corrected, which is the most likely reason for the limited robustness against SEU of ToASt1 [5]. Concerning the second point, previous studies [6] have shown that the technology is insensitive to TID up to 50 kGy, a value higher than the expected one for the environment where ToASt1 would be used; for this reason, no specific techniques were implemented to reduce the effects of TID in ToASt1 [5]. To note that the 20 KGy specification for TID would cover 10 years of the PANDA experiment lifetime. TID tests on ToASt1 demonstrated a different result [7], and therefore, an enclosed gate layout has been implemented in ToASt2 for the n-transistors in all the analog switches, which are the most critical parts due to their shortest gate length, and were absent in ToASt1.

ToASt2 implements the same analogue and digital circuit schemes as the first version of ToASt [2] except for two variations: the bandgap voltage that is generated internally in the chip and the channel DAC's threshold voltage resolution, which is increased from 5 to 6 bits.

In section 2, the description of the ToASt2 integrated circuit is presented. In section 3, some results about the functionalities of the ASIC are shown. In section 4, the results obtained with SEU and TID tests are reported. Conclusions will follow in section 5.

2 ToASt2

ToASt2 features 64 channels each with the same analog chain, which includes a charge sensitive amplifier with selectable input polarity (gain of about 5 mV/fC), p-type or n-type, depending on which side of the double-sided microstrip sensors the chip has to be connected; in addition, a test pulse circuit can be enabled to inject, via an integrated capacitor, a charge at the input of each channel for calibration and debugging purposes. A shaper circuit with adjustable peaking time compensates for the increase in the sensor leakage current due to a long period of irradiation. A current buffer is between the previous part and a second part that includes a Time over Threshold (ToT) stage with a low-frequency baseline holder circuit in feedback. The ToT stage integrates the current pulse from the buffer over a capacitor, which is then discharged by a constant current, generating a triangular-shaped waveform. It feeds two comparators in parallel, which convert this signal into digital signals: the time comparator (TC), which works with a lower threshold, and the energy comparator (EC), which works with a higher threshold. During normal operations, a first-time value, named the Time of Arrival (ToA) of a particle, is stored on the rising edge of the TC. When a second time value is stored on the falling edge of the EC, the time difference provides the ToT, which corresponds to an energy measurement. The event is validated and its information acquired only if an EC rising edge is detected before the TC falling edge; otherwise, the event is discarded. The technique of working with two thresholds reduces both jitter for small signals and the noise-induced events. The time resolution is determined by the time-stamp counter, clocked by the 160 MHz master clock signal. To compensate for variations due to the production process, the ToT discharge current and the two thresholds can be digitally coarse-tuned (at the chip level) and fine-tuned (for each channel) via a configuration interface.

Eight channels are grouped in a region controlled by a Region Control Unit, which polls them for data availability and, to reduce dead time, immediately stores event time stamps and channel address information in a local FIFO. Afterwards, the 8 regions transmit data to a global readout

2026 JINST 21 C04010

unit, which sorts them in 32-bit words. Data are sent out of the chip to two serial links running at 160 Mb/s, and the chip configuration is written via a serial link running at 80 Mb/s. This last one is a bi-directional link; it uploads and downloads the global and local threshold configurations, the ToT discharge current value, and the other configuration parameters. The drivers and receivers work with SLVS (Scalable Low-Voltage Signaling) logic.

To improve robustness against SEU, the TMR technique has been applied to protect the digital logic: two 12-bit registers for configuring each channel, and the sixteen 12-bit registers for the global chip configuration. To avoid risks of double upsets on adjacent elements of a triplicated register, the distance between FF of the same bit is not less than 20 µm. The channel data registers are non-triplicated to limit power consumption. Clock and reset lines are triplicated.

3 Electrical functionalities tests results

Most of ToASt2's electrical functionalities have been tested. The ToT gain linearity has been measured to be less than 1% in the range 2–16 fC. The ToT gain spread between chip channels is large; it can be reduced by the calibration DACs with a fine adjustment (figure 1), to less than 2%.

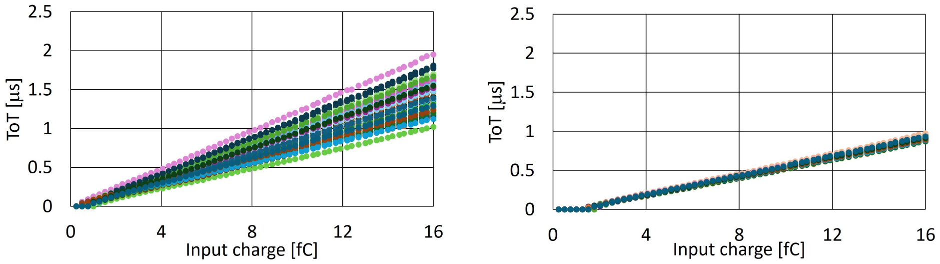

Figure 1. ToT Transfer function before and after the calibration for all the 64 channels of a chip. The right plot shows the result of calibrating the ToT gain spread from the left plot for the 64 channels of a chip. The calibration method minimizes both the spread of slopes of the curves representing the ToT gain and the threshold dispersion. Therefore, in this case, the offset of the right plot does not correspond to the minimum threshold value.

The noise varies from channel to channel within the same chip, and figure 2 shows the results for one of the tested chips with no sensor connected to the channel's input. The measurement was performed by scanning the channel's fine-tuning threshold; therefore, the S-curve can be evaluated. The Equivalent Noise Charge (E.N.C.) values were evaluated with the error function, assuming a Gaussian distribution.

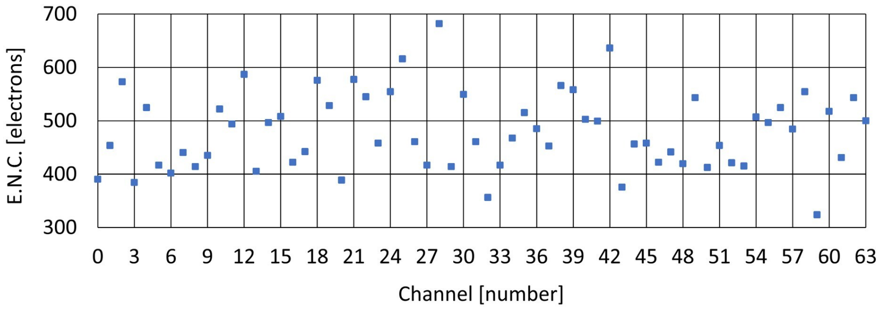

Figure 2. Equivalent Noise Charge values for all the 64 channels of a chip under study.

It is important to note that the yield is 100% after carrying out tests and measurements on 7 chips, for which all channels provide ToT information. In the case of ToASt1, the yield was approximately 60%, as 40% of the chips did not give any output signal. Although the statistic is low, the difference could be due to an improvement in the foundry's production process.

4 SEU and TID tests results

To evaluate the tolerance to SEU, a test was performed at the SIRAD facility (INFN-LNL), where beams of different ions are available. Using the configuration line, the register bits of the chip are written, both for channels and global control. The written values are a balance of 0 and 1 that corresponds to a working point anyway. Under irradiation, the written values are read out, and if one or more upsets are detected, they are recorded, and the registers are rewritten. The SEU cross section is defined as the ratio of the number of upsets to the incident particle fluence divided by the number of bits of the registers under study. This ratio can be reported as a function of LET or E_{dep} by assuming a sensitive volume. In general, the behavior features a sharp threshold below which no upset occurs, and an increase with a saturation region where SEU number remains constant.

With ToASt2, the ion fluxes range from 10^4 up to 10^5 ions/(cm^{2}s) and several ion beams were used: Ag, Ni, Si, Br, Cl. Measurements were performed with the d.u.t (device under test) positioned at 90° with respect to the incident beams; two runs were acquired with a 30° tilt angle of the chip, for Si and Cl. Figure 3 shows the SEU cross section per bit as a function of the deposited energy in an assumed sensitive volume of 1 μm^3 [8] as measured for the channel configuration registers, where the total number of bits is 1536. The fit of the experimental points is performed using a Weibull function; the threshold for upset effects is 1.9 MeV deposited energy. The evaluation of the cross section for a hadronic environment has been done following the reference [8], and it is $\Sigma_{\mathrm{SEU}} = 4.0 \pm 0.4 \cdot 10^{-17}$ cm^2/bit, about two orders of magnitude lower than the value evaluated for ToASt1. No upsets were observed in the global configuration registers, which have a total number of 192 bits. From the analysis of results in the channel registers, events where all the bits of a register are set to zero are identified. This effect could be due to a transient in the LOAD circuit which

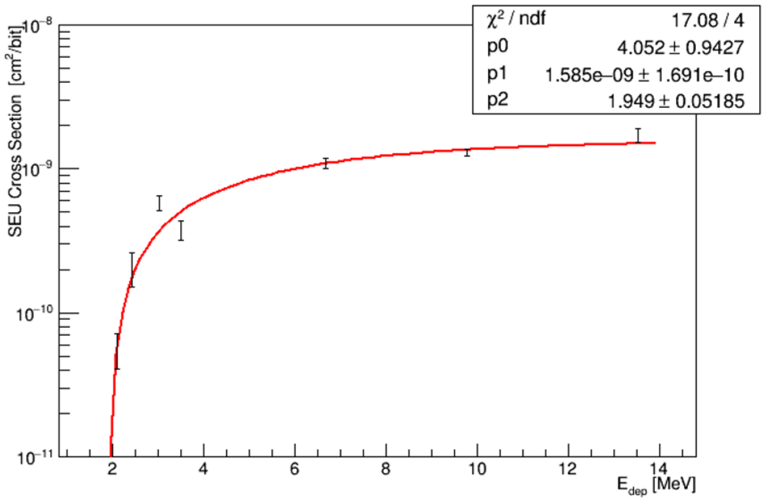

Figure 3. SEU cross section per bit of the channel configuration registers.

2026 JINST 21 C04010

sends the configuration ‘all zero’. The cross section for these transients has been evaluated for a hadronic environment, and it is $\Sigma_{\mathrm{SET}} = 3.9 \pm 0.3 \cdot 10^{-16}\,\mathrm{cm}^2$/register. This type of transient was not detected in the global configuration registers.

The TID test of ToASt2 was performed in the Laboratorio Tecnologico of INFN-Torino using the available X-ray source from the Physics Department of the Torino University and INFN of Torino. Two chips were irradiated, each wire-bonded on its testing board, with two different dose rates: 350 rad/s (Board 3) and 200 rad/s (Board 5). It was observed that all irradiated channels reduce their ToT gain, which drops to 50% around a 6–8 kGy dose and decreases further when the dose increases to 20 kGy. These lower values are recovered to the initial gain values by annealing at room temperature for a few tens of hours, followed at 100°C for hundreds of hours. Figure 4 shows the trend of the ToT gain for channel 35 of board 5 during the irradiation and along the annealing phase.

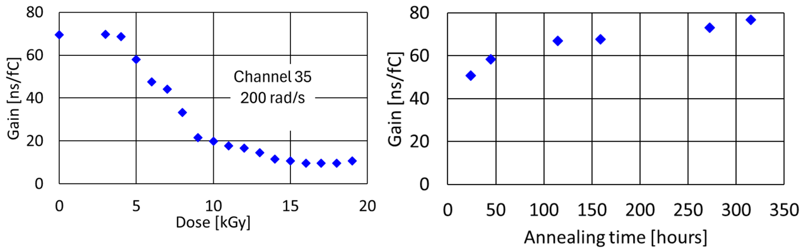

Figure 4. TID test results. On the left, the ToT gain variations of channel 35 during the irradiation of the chip. On the right plot, the ToT gain recovers during the annealing phase.

The analog and digital currents, measured on the power supply of the board, increase by about a few tens % and a few % respectively, and they recover during the annealing phase. The measured variation in the supply current is due to leakage current at the transistors’ edges. This effect has been widely studied and measured for many technologies [9].

5 Conclusions

ToASt2, the second version of triggerless readout for silicon microstrip detectors, was designed and, due to its limited size, produced in an MPW in a commercial CMOS 110 nm. The ASIC was tested for characterization of its electrical functionality and radiation tolerance, for application in the PANDA experiment. Overall, the results meet the project requirements and, as far as the electrical characteristics are evaluated, they are similar to those of ToASt1.

Regarding the radiation tolerance, corrections and changes have been made to the circuit compared to the ASIC ToASt1. Variations of the ToT gain and digital and analog currents were measured during the TID test. However, the dose rate of 200 rad/s is more than two orders of magnitude higher than that expected in the PANDA experiment, and annealing recovers both the decrease in the channel gain and the increase in the current. The tolerance to SEU effects measured for the channel registers is satisfactory, and the effects evaluated as a transient in the LOAD circuit are acceptable, even considering that a project like PANDA implements several thousand of these ASICs.

Acknowledgments

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