Vertex Detector Electronics: L1 Electronics System Issues

LHCb Technical Note

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Abstract

This note describes the application of general requirements to LHCb L1 front-end electronics [1] to the vertex detector L1 electronics, mainly system aspects like initialisation, resets, event identification, data formats and throttling.

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Vertex Detector Electronics: L1 Electronics System Aspects			
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Draft	0	28 Sep 2001	First version
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1 Introduction

The L1 electronics of the LHCb Vertex Detector [2] is a part of the front-end (or read-out) electronics. It receives...

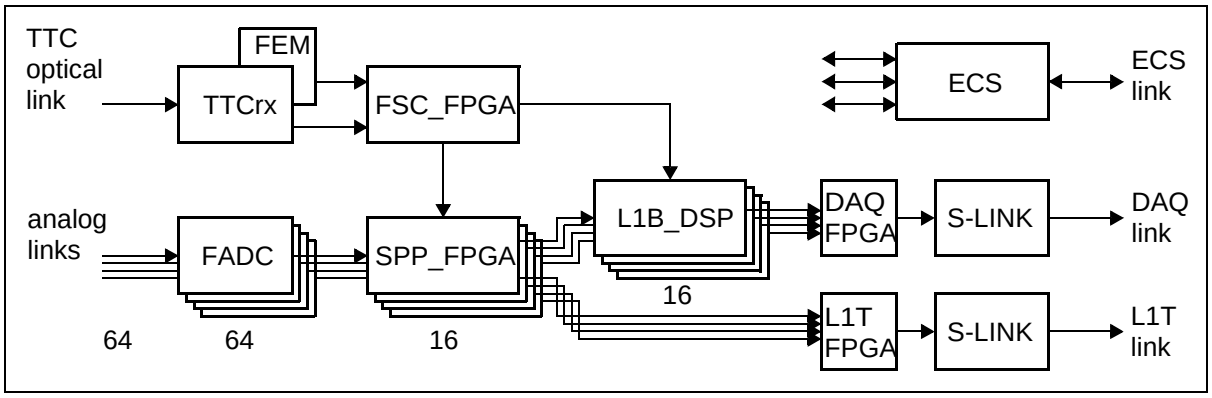


Figure 1

- Analog links, each carries analog information from 32 detector strips, 32 neighbouring strips have to end up on one FE-chip to be able to regroup them in the ODE.
- FADC - 4 channels FADC card with clock phase and voltage reference adjustment per group of 4 channels, hence require one front-end chip to have the same link length from the front-end to the L1 electronics for 4 kinks which shall be grouped together,
- TTCrx - receiver chip of the Timing and Fast Control (TFC) system, which receives clock and commands from the Readout Supervisor,
- FEM - Front-End eMulator,
- FSC_FPGA - Fast and Slow Control FPGA,
- ECS - Experiment Control System interface,
- SPP_FPGA - Synchronisation and level-1 PreProcessor FPGA,
- L1T_FPGA - Level-1 Trigger link control FPGA,
- L1B_DSP - Level-1 Buffer and DSP,
- DAQ_FPGA - DAQ link control FPGA.

2 L1 electronics initialization

2.1 Power-up initialisation

Vertex detector L1 electronics contains a number of components which have to be initialized after power-up. Some of them have an internal power monitoring circuit which automatically starts an initialisation procedure, while others require an external “power-up reset” signal.

VELO L1 electronics boards may require several voltages (e.g. 5.0V, 3.3V, 2.5V, 1.8V) for their operation. They (or some of them) are provided by power supplies via the LHCb standard power backplane in the crate. A power-up reset circuit, which monitors board voltages and generates “power-up reset” signal, may be implemented on each individual L1 electronics board (e.g in the ECS interface on the board). Alternatively, this signal may be generated centrally for all boards in the crate (in the ECS interface of the crate power supply) and sent to all boards via power backplane in the crate.

Following paragraphs describe the power-up initialisation procedure for different components and generation of a board status signal. The power-up initialisation is followed by the software configuration of the board from the LHCb ECS system - loading parameters into internal configuration registers and look-up tables.

2.1.1 TTC interface

After power-up, TTCrx chip automatically goes through a power-on reset delay of 50 ms to allow power supply to stabilize and than goes into initialisation procedure which takes about 50 µs. Internal TTCrx registers are set into default state (see chapter 3 of TTCrx reference manual [3] for details). Upon termination, TTCReady signal goes high. Some parameters in the Control and Configuration registers may be changed after initialisation to standard LHCb values via ECS (e.g. Level 1 Trigger Sequence).

The front-end emulator (FEM) in the L1 electronics is based on the real front-end chip or implemented in the FPGA, using an HDL model of the control logic of the real chip. After power-up all internal registers are automatically set to initial values. There is no “ready” signal from the front-end emulator.

2.1.2 FPGA (Altera APEX 20K)

After power-up, low-to-high transition on nCONFIG pin of APEX 20K device initiates FPGA configuration from EEPROM (EPC2 from Altera) and subsequent initialization [4]. It includes power-on reset delay of max 200 ms, configuration data download time of 390 ms (for 3.3V EPC2 DCLK=5 MHz, APEX 20K200 data size=1950000 bit) plus 40 clock cycles of initialization, 8 ms (for APEX 20K). Total time ~600 ms. All internal registers and state machines are set to initial states. Upon termination, INIT_DONE signal goes high and I/O are switched to user mode from Tri-State.

2.1.3 DSP

DSPs in the L1 electronics require an external power-up signal in order to guarantee a proper DSP initialization. A power-up reset circuit (e.g. TPS3707 from Texas Instruments which monitors DSP power supplies [5]) may be used to generate a DSP_RESET pulse of 200 ms duration. Initialisation takes 50 to 200 ms, depending on the program memory, and includes booting the DSP and loading the program memory from EEPROM. Upon initialization, each DSP set DSP_READY signal high.

2.1.4 ECS interface

ECS interface in L1 electronics requires an external power-up signal which may be generated by a power-up reset circuit on the L1 electronics board (e.g the same as used for DSPs). Initialisation takes ~? ms. Upon initialization, ECS interface sets ECS_READY signal high.

2.1.5 Data Links

Data links to the L1 trigger and DAQ system may require a configuration routine on power-up which might take some time. For example, for the Link Source Card (LSC) of S-LINK it may take maximum 15 s according to the S-LINK specification [6] and depends on the LSC implementation. During this time S-LINK LDOWN# signal will be held low by the LSC. When power-up sequence has been completed, LDOWN# signal will automatically go high.

2.1.6 L1 electronics READY signal generation

Each L1 electronics board contains a circuits which generates a BOARD_READY signal as an “AND” of individual “ready” signals from the board components. This signal is available on the front panel output LEMO connector. It is also accessible by the LHCb ECS system via standard status register on the board (TBD). The maximum delay of the BOARD_READY signal generation after power-on is defined by the component with the longest initialisation time.

2.2 Re-initialisation

Vertex detector L1 electronics may need re-initialisation during running, e.g. FPGA re-configuration with a new design or re-loading program in DSP. Not all components may be re-initialise at the same time. Following paragraphs describe the re-initialisation procedure for different components.

As in the case of power-up initialisation, the re-initialisation is followed by the software configuration of the board from the LHCb ECS system - loading internal configuration registers and look-up tables.

2.2.1 TTC interface

TTCrx chip may be re-initialised by external system either:

- by an active low pulse of ~50 μs on the Reset_b pin of the TTCrx chip,
- by sending an individually addressed (subaddress = 6) RESET command via TTC optical link,
- writing value=5 to the TTCrx status register (address=22) via I2C port of the TTCrx chip.

NB: There is no clock output signals from the TTCrx chip during re-initialisation. Therefore, the external system, which re-initialise TTCx chip, must use separate clock.

The TTCrx chip may be automatically reset by the internal watchdog circuit - how to handle this situation?

The front-end emulator in the L1 electronics may be re-initialised by sending a command to the reset logic in FPGA which controls the front-end emulator reset signal. This command is send by the ECS interface on the board via I2C port of the FPGA.

2.2.2 FPGA

New configuration data for the FPGA are loaded into EEPROM (EPC2 from Altera) before FPGA re-initialisation. EEPROM may be programmed via JTAG port from ECS interface on the board (without affecting board operation). FPGA re-configuration may be initiated by an external system either:

- by generation of an active low signal of (? μs) on the nCONFIG pin of the FPGA,
- by sending a JTAG instruction INIT_CONF to EEPROM via JTAG port. This instruction drives nINIT_CONF pin of the EEPROM that is tied to the nCONFIG pin of the FPGA.

2.2.3 DSP

New program for DSP are loaded into EEPROMs before DSP rebooting. EEPROM may be programmed via parallel port from the ECS interface. DSP rebooting may be initiated by an external system either:

- by generation of an active low signal of on the EXT_RESET pin of the DSP power-up reset circuit,
- by sending a software interrupt via DSP parallel port to initiate software rebooting.

2.2.4 ECS interface

ECS interface on the L1 electronics board may be re-initialised by the central LHCb ECS system. During ECS interface re-initialisation the L1 electronics board is still running.

There is no ECS interface re-initialisation from the L1 electronics board (e.g. from the TTC system).

2.2.5 Data Links

Data links to the L1 trigger and DAQ system (e.g. S-LINK LSCs) may be re-initialised by setting the URESET# low. LSC sets LDOWN# low, initialises (max 15 s) and sets LDOWN# high. The RESET# then may be removed (set high). URESET# signal may be controlled by the link control logic or by the ECS interface on the board.

2.2.6 Re-initialisation from ECS

L1 electronics board re-initialisation may be initiated by the central LHCb ECS system via ECS interface on the board. Components on the board may be re-initialised individually:

- TTCrx chip may be re-initialised via I2C port of the TTCrx chip.
- Front-end emulator may be re-initialised via I2C port of the front-end emulator control FPGA.
- FPGA may be re-initialised via JTAG port of the EEPROM.
- DSPs may be re-initialised via DSP parallel port.
- Data links may be re-initialised via I2C port of the link control FPGA

This provide a flexibility in the board re-initialisation scenarios (e.g. partial board re-configuration). Re-initialisation of the whole L1 electronics board in one go may be achieved by remote switching off and on the power supply in the crate from the central ECS system *(do we need this?)*.

3 L1 electronics resets and event identification

3.1 Resets

Vertex detector L1 electronics must react to LHCb reset signals. They are sent to the L1 electronics (to the TTCrx chip) via the TTC system from the Readout Supervisor (RS) which is controlled by the L0 and L1 trigger systems and the LHCb ECS system.

3.1.1 BCID_Reset - bunch counter reset

The BCID_Reset is used to reset a Bunch Counter in the TTCrx chip, driven by clock (see 3.2.2). It is sent to the TTCrx chip via TTC system broadcast command (CMD<7..0>=xxxxxxx1). The BCID_Reset signal is made available on the output pin of the TTCrx chip (BCntRes) but is not used by the L1 electronics.

3.1.2 L0ID_Reset - L0 event counter reset

The L0ID_Reset is used to reset L0 Event Counter, implemented in the FCS_FPGA, driven by the L0 accept signal (see 3.2.3). It is sent to the TTCrx chip via TTC system broadcast command (CMD<7..0>=xxxxxx1x). The L0ID_Reset signal is made available on the output pin of the TTCrx chip (EvCntRes) to be used by the FCS_FPGA.

3.1.3 L0_Reset - L0 front-end reset

The L0_Reset is used to reset the L0 electronics. In the vertex detector L1 electronics L0_Reset is used only to reset the front-end emulator. It is sent to the TTCrx chip via TTC system broadcast command (CMD<7..0>=01xxx1xx) which is made available on the output broadcast data bus (Brcst<7..2>) of the TTCrx chip accompanied by the strobe (BrcstStr1). This broadcast command is decoded in the FCS_FPGA and generates 2 clock cycles wide reset signal for the front-end emulator. It resets L0 pipeline pointers, L0 derandomizer pointers and stops any running readout process. *(Is L0_Reset always accompanied by the L0ID_Reset? Do we need a L0_Reset counter in the L1 electronics, accessible by ECS?)*

3.1.4 L1ID_Reset - L1 event counter reset

The L1ID_Reset is used to reset L1 Event Counter in the L1 electronics, which counts L1 accepts (see 3.2.4). It is sent to the TTCrx chip via TTC system broadcast command (CMD<7..0>=01x1xxxx) which is made available on the output broadcast data bus (Brcst<7..2>) of the TTCrx chip accompanied by the strobe (BrcstStr1). This broadcast command is decoded in the FCS_FPGA and generates L1ID_Reset signal on the output pin of the FCS_FPGA. It is used to reset the L1 Event Counters in DSP and DAQ_FPGA and to set “resync” flag (R) in the subsequent event, sent to DAQ.

3.1.5 L1_Reset - L1 front-end reset

The L1_Reset is used to reset the control logic (counters, pointers, state machines, error flags) of the L1 electronics without its re-initialisation. Parameters in the internal configuration registers, look-up tables, which are downloaded via ECS system after power-up initialisation or re-initialisation, are not affected by the L1_Reset (e.g. TTCrx configuration). The L1_Reset is always accompanied by the L0_Reset *(and also*

L0ID_Reset and L1ID_Reset? Do we need a L1_Reset counter in the L1 electronics, accessible by ECS?).

It is sent to the TTCrx chip via TTC system broadcast command (CMD<7..0>=01xx1xxx) which is available on the output broadcast data bus (Brcst<7..2>) of the TTCrx chip accompanied by the strobe (BrcstStr1). This broadcast command is decoded in the FCS_FPGA, generates L1_Reset signal on the output pin of the FCS_FPGA and resets internal control logic in the FCS_FPGA.

The L1_Reset signal is used to reset internal control logic (counters, pointers, state machines, error flags) in other FPGAs and to reset the Level 1 Buffer read / write pointers and to restart the DSP algorithm. The front-end emulator is reset by the L0_Reset which is sent together with L1_Reset. The TTCrx chip and the ECS interface on the board are not affected by the L1_Reset.

3.2 Identification tags

Event data fragments (e.g. from the front-end chip, the readout board, etc.) must be tagged with an identifier, which allow synchronisation error detection in the front-end electronics and event assembling.

3.2.1 PCN - Pipeline Column Number

The Pipeline Column Number (PCN) is an 8-bit trigger pointer of the L0 pipeline in the front-end chip. It is driven by clock, stored on L0 accept to be used as a L0 pipeline read pointer and reset by the L0_Reset (see 3.1.3). Its value is attached as a header (two 4 bit words) to the event data from the front-end chip and shall be identical for all event data fragments from the vertex detector front-end chips belonging to the same event.

In the vertex detector L1 electronics identical PCN is generated in the front-end emulator and is made available on the output 4 bit bus, accompanied by the DataValid signal. The PCN is de-multiplexed from two 4-bit words in one 8-bit word in the FSC_FPGA, delayed for the front-end event data latency and sent to the SPP_FPGAs for cross-check with the PCN in the event data fragments from the vertex detector front-end chips. It is also used for the event tagging (see 4).

3.2.2 BCID - Bunch Counter

The Bunch Counter (BCID) is a 12-bit counter available in the TTCrx chip. It is driven by clock and is reset by the BCID_Reset (see 3.1.1). Its value is made available (for each L0 accept) on the output 12 bit bus (BCnt<11..0>) of the TTCrx chip accompanied by the BCntStr signal and shall be identical for all TTCrx chips in the L1 electronics. It is sent to the SPP_FPGAs via the FSC_FPGA and is used for event tagging (see 4) in the L1 buffer. 2 LSBc of the BCID are used for event tagging to the L1 trigger.

3.2.3 L0ID - L0 Event Counter

The L0 Event Counter (L0ID) is a 12-bit counter implemented in the FSC_FPGA. It is driven by the L0 accept signal from the TTCrx chip. It is reset by the L0_Reset and L0ID_Reset signals from the TTCrx chip (see 3.1.2) and from ECS system by writing any data in it. For the first L0 trigger accepted event, L0ID is equal to "1".

It is sent to the SPP_FPGAs and is used for event tagging (see 4). In the L1T_FPGA, L0ID is used for synchronisation of event data fragments from several SPP_FPGAs before transfer to the L1T system. In DSPs, L0ID is used for cross-check with the L0ID from the L1 decision (see 3.2.4).

3.2.4 L1ID - L1 Event Counter

The L1 Event Counter (L1ID) is a 16-bit counter implemented in the DSPs, therefore, there are several L1ID counters on the L1 electronics board. They are incremented by the L1 trigger accept decision (which is generated in the FSC_FPGA upon receiving and decoding of a L1 trigger decision from the TTCrx chip and distributed to the DSPs). They are reset by the L1ID_Reset and L1_Reset signals which are generated in the FCS_FPGA (see 3.1.4) and from ECS system by writing any data in it. For the first event, accepted by the L1 trigger, L1ID is equal to "1". In the DSPs, 16-bit L1ID is used for event tagging (see 4) before data transfer to the DAQ_FPGA.

The L1 trigger decision is sent to the TTCrx chip via TTC system broadcast command CMD<7..0> - CMD<7>=1 defines the L1 decision command, CMD<6..4> specify the L1 trigger type, CMD<3..2> carry two LSB of the L0ID and CMD<1..0>=xx are ignored. This command is made available on the output broadcast data bus (Brcst<7..2>) of the TTCrx chip accompanied by the strobe (BrcstStr1) and is sent to the FSC_FPGA. From the FSC_FPGA, five bits of the L1 decision (CMD<6..2>) are sent to the DSPs together with 11 bit pointer for the accepted event in the L1 buffer. The DSPs cross-check the L0ID<1..0> of the event data from the L1 buffer with the 2 LSB of the L0ID from the L1 decision (CMD<3..2>).

In the DAQ_FPGA, 16-bit L1ID is used for synchronisation of event data fragments from several DSPs. Before transfer to the DAQ system, they are tagged by 32-bit L1ID from the 32-bit L1ID counter in the DAQ_FPGA.

4 Data formats

4.1 L1 Buffer input

Vertex detector L1 electronics receives event data fragments from the front-end chips over analog data links, four analog links per chip, 128 detector channels in total. After digitizing in the FADC, four 8-bit data streams - 32 detector channel amplitudes plus 2 header words of the PCN (see 3.2.1) each - from one front-end chip are sent to the SPP_FPGA.

Event data fragments from 4 analog data links coming from one front-end chip undergo the synchronisation check and concatenated into 32-bit words before transferring to the L1 buffer.

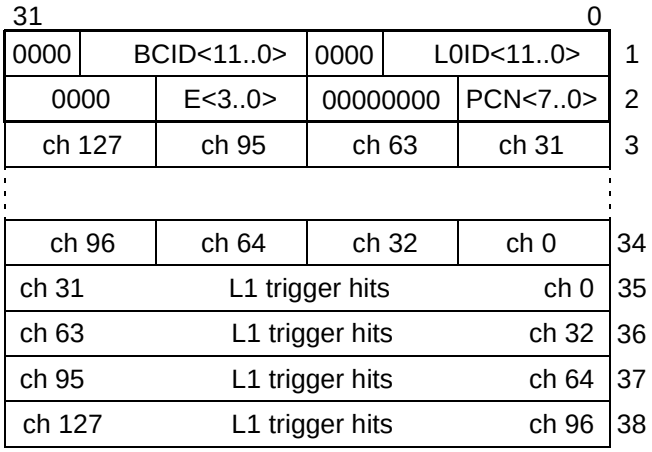
A new common header (two 32-bit words) carries the following information:

- 12-bit L0 Event Counter (L0ID) from the FSC_FPGA,
- 12-bit Bunch Counter (BCID) from the TTCrx chip (via the FSC_FPGA),
- 8-bit Pipeline Column Number (PCN) from the front-end chip event data fragment,
- 4-bit synchronisation error flags (E).

The header is followed by 32 words32-bit wide.

Vertex detector event data from the front-end chips also undergo the preprocessing in the SPP_FPGA for the L1 trigger [7]. Preprocessing algorithm is applied in parallel on each individual event data fragment from one analog data link (32*8 words). After “hit detection” step, the event data fragment is converted into 32*1 words stream where each bit represents a detector channel with an amplitude above a threshold value. Four such streams (from 4 input data links) are converted into four 32 bit “hit” words and appended to the end of the event data, stored in the L1 buffer, for further reference (no hit encoding is performed before the L1 buffer in order to keep the event size constant).

32-bit data format from SPP_FPGA to the L1 buffer is presented below:



The total number of words per event, written into the L1 buffer at 60 MHz, is 38 (~630 ns total write time, well below the 900 ns L0 event spacing). The L1 buffer size is 128K*32 words. 64 words are allocated for each event data in order to simplify event access (an 11 bit pointer is used to access event data). Therefore up to 2K events may be stored in the L1 buffer which satisfies the general L1 electronics requirements.

4.2 L1 Trigger output

4.2.1 From SPP_FPGA to L1T_FPGA

Vertex detector L1 electronics preprocess the event data for the L1 trigger. One SPP_FPGA preprocess the event data from one front-end chip (128 detector channels) - pedestal subtraction, hit detection and cluster encoding. The result of preprocessing is a list of cluster's positions, maximum cluster size is two detector channels, bigger cluster is encoded as several clusters.

For 128 detector channels, 7 bits is enough to encode the position (address) of the cluster. One extra bit indicates the cluster size (one or two channels). The maximum number of clusters which may be found in the SPP_FPGA is 64, assuming all detector channels are above threshold, while the realistic average is 1-2.

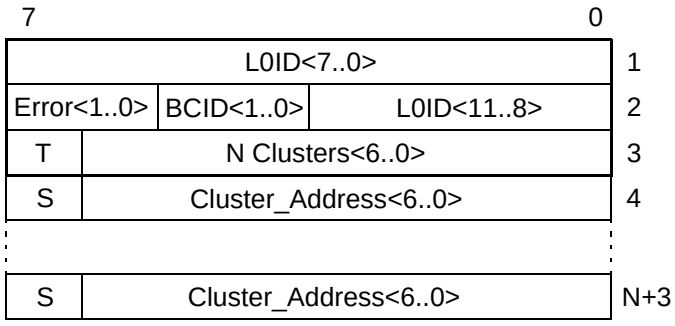
The list of 8-bit cluster addresses is sent to the L1T_FPGA from 16 SPP_FPGAs via 8-bit parallel buses. The number of clusters sent to the L1T_FPGA from each SPP_FPGA is limited (the limit is a 7-bit parameter in the SPP_FPGAs, set by the ECS, the maximum number is 64 per SPP_FPGA therefore, all clusters from certain SPP_FPGA may be sent to the L1T_FPGA and no clusters from other). The other reason for the event truncation may be the time-out during cluster encoding and collection in the SPP_FPGA (the time-out may be switched off). The error flag is set in the case of event truncation.

The header includes the following information:

- 12-bit L0 Event Counter L0ID<11..0> from the FSC_FPGA,
- 2 LSBs of BCID (as required by the RS in the output data format from the L1 trigger),
- 2 bits of error (Error<1..0>, to be defined),
- 7-bit number of L1 trigger clusters found (N, from 0 to 64),
- 1-bit of the SPP_FPGA truncation error flag (T).

The header is followed by N 8-bit words - 7 bit of cluster address plus 1 bit of the cluster size (S="1" - two channel cluster).

8-bit data format from SPP_FPGA to the L1T_FPGA is presented below:



4.2.2 From L1T_FPGA to L1 trigger

In the L1T_FPGA, incoming data from SPP_FPGA are stored in the 8-bit wide 256-word deep FIFOs (standard size of the FIFO block in Altera APEX 20K FPGA) and then collected and written into the 32-bit wide 512-word deep output FIFO. When complete event data from all SPP_FPGAs are assembled in the output FIFO, they are sent to the L1 trigger via the S-LINK.

The total number of detector channels per vertex detector L1 electronics board is 2048, therefore 12 bits are required to encode the position of the cluster (7 bit of the cluster position in the SPP_FPGA, 4 bit of the SPP_FPGA address, 1 bit of the cluster size).

The number of clusters sent to the L1 trigger from each L1 electronics board is limited (the limit is an 8-bit parameter in the L1T_FPGA, set by the ECS, the maximum number is 255 while the realistic average number is around 10, see fig. 13 in [7]. The error flag is set in the case of event truncation.

The event data fragment from the L1 board is embedded in the 32-bit wide Subevent Transport Format (STF) for the L1 trigger [8], which carry the following information:

- 12-bit L0 Event Counter - L0ID<11..0>,
- 2 LSBs of Bunch Counter - BCID<1..0>,
- 16-bit Link ID, LHCb wide number, set by the ECS system in the L1T_FPGA,
- 8-bit L1 electronics board number, set by the ECS system in the L1T_FPGA,
- 2 bits of error (Error<1..0>, to be defined),
- 8-bit total number of clusters (N, from 0 to 255),
- 16 bits of the SPP_FPGA truncation error flags (T flags from the SPP_FPGA),
- 1-bit of the L1T_FPGA global truncation error flag (GT),
- X-bit total size of the STF data block.

Data block of the STF contains M/2 32-bit words, each word carries information about two clusters, for each cluster:

- 7 bit of the cluster position in the SPP_FPGA,
- 4 bit of the SPP_FPGA address,
- 1 bit of the cluster size (S=”1” - two channel cluster).

The exact L1T data format to be discussed with L1T group. In principle 16 bits are available per cluster. One could imagine that rather than transferring the cluster position and cluster size in strip (or channel) numbers, one could transfer them in units of 10 micron (or the detector resolution) in the global reference frame of the VELO, as proposed in [9]. This would allow direct use in the pattern recognition without extra conversions in the L1 trigger. As an example for a R-detectors: maximum radius is 42 mm, this would require 13 bits. Each SPP-FPGA would then have its own LUT to convert the 8 bits (7+1) strip number to the radial position of the strip relative to the origin. The remaining 3 bits would then give the sector number (6 for the micron detector).

4.3 DAQ output

4.3.1 From DSP to DAQ_FPGA

Upon receiving the L1 trigger accept decision from the FSC_FPGA, each DSP increments its 16-bit L1ID counter, transfer 38 words of the event data from the L1 buffer to the DSP internal memory (L1 derandomizer for 16 events) using 11-bit pointer, generated in the FSC_FPGA, and starts processing algorithm:

- zero suppression of the detector data from 128 detector channels (DAQ clusters),
- encoding of the L1 trigger hits, stored in the L1 buffer together with the detector data (L1T clusters), the number of clusters is truncated as in the SPP_FPGA, using the same limit and the truncation error flag (T) is set in the case of event truncation.

The result of the processing is a list of DAQ and L1T clusters. In a special mode without processing (which is set by the ECS system in the DSPs and DAQ_FPGA, indicated by “Z” flag in the data format) no DAQ clusters are sent to the DAQ and the number of clusters found is set to zero. The encoding of the L1 trigger hits is still performed.

To the end of the processed event data a non-processed data for several detector channels are appended (the number of channels is a 8-bit parameter in the DSPs and DAQ_FPGA, set by the ECS, the maximum number is 128). In a special mode without processing, data for all 128 detector channels are appended.

The DSP also follows the pedestal and noise for each of 128 channels. This information is available to the DAQ/ECS systems via ECS interface on the board and is not included in the output data to the DAQ_FPGA.

This list of the DAQ and L1T clusters is preceded by a 5 word header, which contains:

- 16-bit L1ID counter, L1ID<4..0> are used to define an address of the non-processed channels group,
- 12-bit L0ID, 12-bit BCID, 8-bit PCN,
- 4-bit synchronisation error flags (E) from the SPP_FPGA,
- 1-bit “resync” flag (R), which is set upon reset of the L1 Event Counter in DSP (see 3.1.4),
- 1-bit flag (Z), indicating non-processed data,
- 8-bit number of DAQ clusters found (N, from 0 to 255, equal to zero for non-processed data),
- 7-bit number of L1T clusters found (M, from 0 to 64),
- 1 bit of the DSP L1T truncation error flag (T).

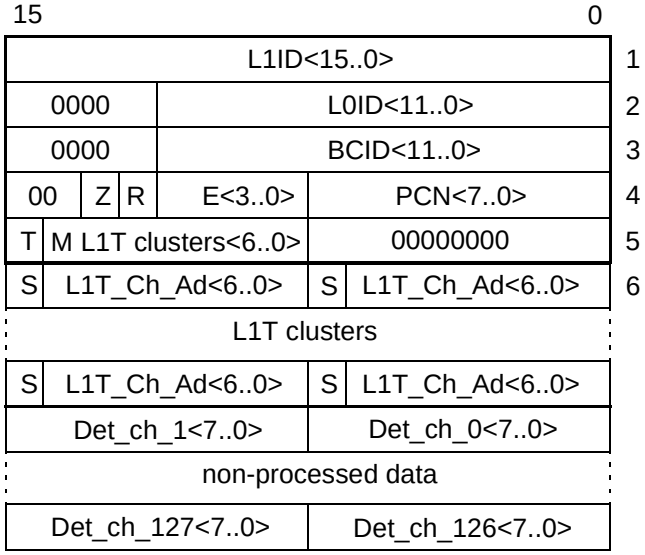
Each DAQ cluster (out of N clusters found) description contains the following information (In a special mode without processing the number of clusters found is set to zero and there are no DAQ clusters information):

- 7-bit address of the first detector channel of the cluster (from 0 to 127),
- 3-bit number of detector channels in the cluster (up to 7 channels),
- up to 7 words of 8-bit cluster data - signal value of every detector channel in the cluster.

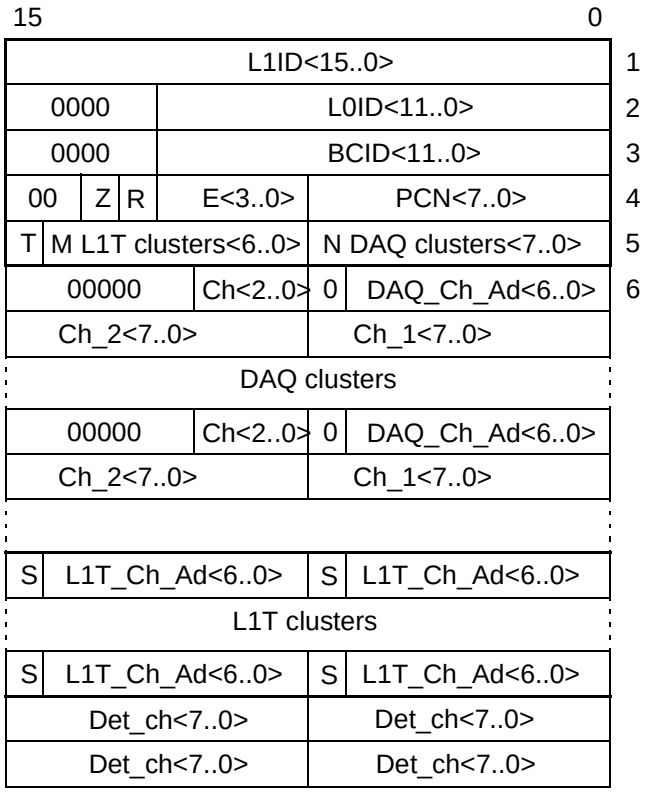
Each L1 trigger hit (out of M hits found) is described by one 8-bit word - 7 bit of cluster address plus 1 bit of the cluster size (S=”1” - two channel cluster).

The non-processed data (e.g. - for 4 detector channels) are appended to the end. The address of the group of 4 channels (address of the first channel in the group) is defined by the L1ID<5..0>. In a special mode without processing, data for all 128 detector channels are appended and L1ID<5..0> are ignored.

16-bit data format from DSPs to the DAQ_FPGA in non processing mode (Z=”1”)



16-bit data format from DSPs to the DAQ_FPGA in processing mode (Z=”0”):



Data are sent from the DSPs to the DAQ_FPGA over 16-bit parallel buses at 40 MHz.

4.3.2 From DAQ_FPGA to DAQ

In the DAQ_FPGA, incoming data from DSPs are stored in the 16-bit wide 128-word deep input FIFOs (standard size of the FIFO block in Altera APEX 20K FPGA) and then collected and written into the 32-bit wide 512-word deep output FIFO. The number if the L1 trigger clusters are truncated as in the L1T_FPGA using the same limit and the global truncation error flag (GT) is set in the case of event truncation

When complete event data from all DSPs are assembled in the output FIFO, they are sent to the DAQ via the S-LINK.

The format of the data, sent to the S-LINK, contain a header with the following information:

- 32-bit L1ID counter, L1ID<4..0> are used to define an address of the non-processed channels group,
- 12-bit L0ID, 12-bit BCID, 8-bit PCN,
- 16 4-bit synchronisation error flags (E) from the SPP_FPGAs, 64 bit in total,
- 1-bit “resync” flag (R), which is set upon reset of the L1 Event Counter in DSP (see 3.1.4),
- 1-bit flag (Z), indicating non-processed data,
- 16-bit Link ID, LHCb wide number, set by the ECS system in the DAQ_FPGA,
- 8-bit L1 electronics board number, set by the ECS system in the DAQ_FPGA,
- 12-bit total number of DAQ clusters found (equal to zero for non-processed data),
- 12-bit total number of L1T clusters found,
- 16 bits of DSPs truncation flags (T flags from the DSPs),
- 1-bit of the DAQ_FPGA global truncation error flag (GT),
- X-bit total size of the of the data block,
- ???

Each DAQ cluster description contains the following information:

- 12-bit address of the first detector channel of the cluster (7-bit address from DSP is extended to 12 bits by adding a 4-bit DSP number),
- 3-bit number of detector channels in the cluster (up to 7 channels),
- up to 7 words of 8-bit cluster data - signal value of every detector channel in the cluster.

Each L1 trigger cluster is described by one 13-bit word:

- 12-bit of the cluster position (7-bit address from DSP is extended to 12 bits by adding a 4-bit DSP number),
- 1 bit of the cluster size (S=”1” - two channel cluster),

The non-processed data are appended to the end. The address of the group of 4 channels from each DSP (address of the first channel in the group) is defined by the L1ID<5..0>. In a special mode without processing, data for all 2K detector channels are appended and L1ID<5..0> are ignored.

Transport data format for the DAQ system is not yet defined.

5 Throttling

5.1 DSPs and DAQ interface

Upon receiving the L1 trigger accept decision, each DSP transfers 38 words of the event data from the L1 buffer to the DSP internal memory (the L1 derandomizer for 16 events) and starts processing algorithm. As soon as the L1 derandomizer is nearly full (there are N events in the derandomizer, N is a 4-bit parameter in the DSP, set by the ECS, default value - 13), the throttle signal is generated by the DSP and sent to the FSC_FPGA.

In the DAQ_FPGA, internal throttles are the full flags from the input FIFOs, which are sent back to the DSPs in order to temporarily stop data transfer from DSP to the DAQ_FPGA. This “back pressure” from the DAQ_FPGA builds up a queue in the DSP output buffer and in the L1 derandomizer and results in the throttle from the DSP to the FSC_FPGA

5.2 No throttle from the L1 trigger preprocessor

Vertex detector L1 electronics preprocess the event data for the L1 trigger. In order to keep with the 900 ns L0 event spacing, the preprocessing in the SPP_FPGA (up to the cluster encoding) is performed in pipeline mode with no dead-time and the cluster encoding and collection uses time-out to truncate event (in addition to the cluster limit, set by ECS, see 4.2.1). The time-out may be switched off.

In the L1T_FPGA, the event data (number of clusters, found in SPP_FPGAs) are also truncated in order to keep data transfer time to the L1 trigger within 900 ns.

Therefore, no throttle signal is generated by the L1 trigger preprocessor and data link.

5.3 L1 electronics board throttle

All individual throttle signals from DSPs on the L1 electronics board are handled in the FSC_FPGA. They can be individually disabled using a control register in the FSC_FPGA, accessible via ECS interface. Each throttle signal is counted, the total number is made available for the ECS system via ECS interface on the L1 electronics board.

A global “OR” of all individual throttles is generated and made available as a NIM signal on the LEMO connector on the front panel and also as a bit in the FSC_FPGA status register.

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