Fermi National Accelerator Laboratory

FERMILAB-Pub-92/251

Field Oxide Radiation Damage Measurements in Silicon Strip Detectors

M. Laakso

Research Institute of High Energy Physics (SEFT)
Helsinki, Finland

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

P. Singh, P.F. Shepard

Department of Physics and Astronomy, University of Pittsburgh

December 1992

Submitted to *Nuclear Instruments and Methods*

Operated by Universities Research Association Inc. under Contract No. DE-AC02-76CHO3000 with the United States Department of Energy

Disclaimer

FERMILAB - Pub - 92/251

FIELD OXIDE RADIATION DAMAGE MEASUREMENTS IN SILICON STRIP DETECTORS

M. Laakso
Particle Detector Group, Fermilab, Batavia, Illinois, USA and
Research Institute for High Energy Physics (SEFT), Helsinki, Finland

P. Singh, P.F. Shepard
Department of Physics and Astronomy,
University of Pittsburgh, Pittsburgh, PA, USA

Abstract

Surface radiation damage in planar processed silicon detectors is caused by radiation generated holes being trapped in the silicon dioxide layers on the detector wafer. We have studied charge trapping in thick (field) oxide layers on detector wafers by irradiating FOXFET biased strip detectors and MOS test capacitors. Special emphasis was put on studying how a negative bias voltage across the oxide during irradiation affects hole trapping. In addition to FOXFET biased detectors, negatively biased field oxide layers may exist on the n-side of double-sided strip detectors with field plate based n-strip separation. The results indicate that charge trapping occurred both close to the Si-SiO_2 interface and in the bulk of the oxide. The charge trapped in the bulk was found to modify the electric field in the oxide in a way that leads to saturation in the amount of charge trapped in the bulk when the flatband/threshold voltage shift equals the voltage applied over the oxide during irradiation. After irradiation only charge trapped close to the interface is annealed by electrons tunneling to the oxide from the n-type bulk.

(Submitted to Nucl. Instr and Meth.)

1. Introduction

Interest in radiation damage in planar processed silicon detectors has been steadily increasing as new proposals for their use in high radiation fields in experiments at Fermilab, LHC and SSC have been presented. Both bulk damage, depending on the fluence of high energy charged and neutral hadrons incident on the detector, and surface damage, depending on total ionization dose to the SiO_2 layer at the surface of the detector [1], have to be considered for successful operation of the detectors in the high radiation environment of hadron colliders. This work concentrates on surface radiation effects on silicon detectors.

In some silicon strip detector designs a normal operation of the device leads to a negative voltage being applied over a thick field oxide layer. Examples of cases like this are 1) detectors with p-strips biased with FOXFET transistors [2],[3] or 2) double-sided strip detectors with strips separated by a field plate structure on top of a field oxide layer [4]. In this paper we report studies on charge trapping in negatively biased field oxides using both FOXFET biased detectors and MOS field oxide test capacitors.

The oxide layers generally used in AC-coupled silicon detectors are much thicker than for example gate oxides in MOS transistors. Typical oxide thicknesses are around 200 nm for insulator oxides in integrated coupling capacitors, 0.5 - 1 μm for passivating (field) oxides on detector wafers and over 1 μm for the insulating oxide between the two metal layers in detectors utilizing double metal crossed electrodes. As a consequence, significant oxide space charge effects can be expected to occur at relatively low (krad) doses of ionizing radiation. Furthermore, most of the literature available about radiation induced charge buildup in oxide layers concentrates on thin (<200 nm) oxide layers used

in MOS integrated circuits [1] rather than on the thicker oxides found on silicon detectors.

The amount of charge trapped in the oxide depends strongly on the direction and magnitude of the electric field in the oxide during irradiation. With no electric field inside the oxide, electrons and holes recombine efficiently after they have been created, and very little charge trapping occurs. With the electric field pointing towards the Si-SiO_2 interface the holes created by radiation are transported to the interface, where most of the hole traps in the oxide are generally located. This leads to strongly enhanced hole trapping with positive gate voltages. With the electric field pointing away from the Si-SiO_2 interface recombination is less efficient than with no electric field present, which tends to increase hole trapping. On the other hand, now the holes are drifted away from the interface, which decreases trapping. Overall the trapping is larger than with zero electric field, but significantly less than with positive gate voltages.

2. Experiments

The detectors used in this study were single sided AC-coupled strip detectors biased with FOXFET transistors with a nominally 1000 nm thick field oxide. The MOS field oxide test capacitors had an area of 5x5 mm^2 and the measured oxide capacitance was ≈ 1300 pF, giving an oxide thickness of ≈ 660 nm. The detectors and test structures were mounted and bonded on PC boards so that devices could be biased during irradiations. The resistivity of the wafers after processing was determined by C-V measurements on the detectors and test diodes and was found to be ≈30 kΩcm, corresponding to an effective doping level of $1.4 \cdot 10^{11}$ cm^{-3}.

The samples were irradiated using a ^{137}Cs source at the University of Pittsburgh. The dose rate varied between 156 krad/h and 274 krad/h for detector irradiations and between 22 krad/h and 51 krad/h for test capacitor irradiations.

The detectors were irradiated with no material between the source and the detectors, whereas the test capacitors were irradiated with a filter consisting of 2.1 mm lead and 0.8 mm aluminum between the source and the detector. The filter was used in order to remove possible low-energy photon contamination in the radiation field [1]. For both cases the dose rate was calibrated with an air-ionization chamber.

The FOXFETs on the detectors were characterized using a HP 4145B programmable source-monitor unit, which was also used for low frequency C-V measurements on the test capacitors. High frequency C-V measurements were made using a HP 4284A LCR meter.

3. Results

We present here results from two different sets of measurements. In the first measurements we studied the behavior of the FOXFET biased detectors as a function of radiation dose. These measurements, which are described in section 3.1., indicated the significance of FOXFET gate bias during irradiation. This effect was verified and studied more thoroughly in the second set of measurements, where MOS test capacitors were irradiated and studied (section 3.2).

3.1. Measurements on detectors

In order to determine oxide charge buildup in the gate (field) oxide of the FOXFETs, we measured the shift in the threshold voltage of the FOXFET as a function of radiation dose. The threshold voltage should in first approximation be a measure of the oxide charge buildup in the gate oxide. During irradiation the FOXFET gate was biased at -9V. First a set of irradiations up to 100 krad was performed. The shift in the threshold voltage as a function of radiation dose can be

seen in fig. 1, where we notice that already at 10 krad a change in the threshold voltage of approximately -10 V is observed, after which the change is much more gradual. After 100 krad there was a 100 day period without irradiations, during which the threshold voltage shift annealed from 14.5 V to 10 V. In consequent irradiations up to 1 Mrad only a few volts increase in the threshold voltage was observed. Saturation effects like this are usually attributed to the effect of trapped charge on the oxide electric field, and have been observed in thin oxides at high (Mrads) doses [1], and in thick oxides at lower doses at low temperatures [5], where radiation generated holes remain essentially immobile after their creation. Assuming that hole trapping occurs also in the bulk of the oxide [6], a saturation due to space charge effects of holes trapped in the bulk can be expected in thick oxides also at room temperature. With negative gate voltages the saturation should occur approximately at threshold or flatband voltage shifts equaling the gate or capacitor bias voltage.

In another study done with the gate electrode floating during irradiations, the shift in threshold voltage has been observed to increase proportional to the square root of the dose up to 1 Mrad, with no noticeable saturation [7]. As expected, the gate biasing during irradiation seems to play a significant role in the charge buildup to the gate oxide.

In addition to charges in the oxide, in humid conditions a layer of negative charge can be present also on top of the oxide leading to instabilities caused by fluctuations in the distribution of this charge [8]. We measured the leakage current of one detector as a function of ambient humidity in order to determine the magnitude of this effect on the leakage current. This was done by monitoring the detector leakage current as the detector enclosure, originally filled with dry nitrogen, was slowly flushed with nitrogen saturated with water vapor. Fig. 2 shows the result of the measurement. As the humidity was increased to over

60%RH, the detector behavior in terms of leakage current became unstable and the leakage current started to increase. This can be explained by the introduction and rearrangement of negative charges on the part of the oxide surface that is not covered with aluminum. When the negative charges appear on the surface they compensate the effect of positive oxide charge and reduce the accumulation layer electron density close to the Si-SiO_2 interface. Further increase in the negative charge leads eventually to surface depletion and consequent increase in the leakage current, as the surface generation becomes added to the bulk leakage current. At high humidity levels (≈90%RH) the leakage current was as much as 20 times greater than the current at dry conditions.

3.2. Measurements on test capacitors

Three test capacitors were available for the study. They were irradiated with 0V (capacitor C1), -8V (C2) and -16V (C3) applied to the gate during irradiation, corresponding to an oxide electric field of 0 V/cm, $-1.2 \cdot 10^5$ V/cm and $-2.4 \cdot 10^5$ V/cm, respectively. The results of a 10 kHz C-V measurement at different doses for capacitor C1 together with a calculated ideal high frequency C-V curve are presented in fig. 3. For the two other capacitors the curves were qualitatively similar. The standard high-frequency measurement frequency of 1 MHz could not be used because of the high resistivity of the wafer causing resistive losses in the undepleted silicon under the capacitor. The shift of the C-V curve and the stretchout caused by interface traps can clearly be seen in fig. 3.

Because of the low measurement frequency some of the interface traps contribute to the capacitance at flatband conditions, so we made a correction to the capacitance value used to determine the flatband voltage. The procedure was to determine the capacitances C_{fb} and C_{inv} corresponding to the flatband condition (surface potential $y_s = 0$) and the onset of strong inversion ($y_s = 2 \cdot y_{bulk}$) from

the theoretical C-V curve, calculated according to [9]. We also determined the theoretical gate voltage stretchout between these two values with no interface traps present. These values are: C_{fb} = 550 pF, C_{inv} = 107 pF and $(V_{fb}-V_{inv})$ = 0.086 V. Then we estimated the interface state density in cm^{-2} was obtained from the measured stretchout between C_{fb} and C_{inv}, using [10]:

$$DN_{it} = \frac{D(V_{fb}-V_{inv})\, e_o e_{SiO2}}{q\, d_{ox}} \qquad (1)$$

where e_o is the vacuum permittivity, e_{SiO2} is the dielectric constant of SiO_2, q = electron charge and d_{ox} = the oxide thickness. This value was converted into interface state density D_{it} (in units of $cm^{-2}eV^{-1}$) by dividing it by the width of the portion of the bandgap between flatbands and strong inversion, which is 0.12 eV in silicon of our resistivity. The interface state capacitance C_{it} was then calculated from [9]:

$$C_{it} = q\, D_{it}\, A \qquad (2)$$

where A is the area of the capacitor. This capacitance was then added to the calculated flatband capacitance, and the same procedure was repeated. After two or three cycles the values were consistent in all the cases.

The flatband voltage as a function of radiation dose for all the three capacitors is plotted in fig. 4. It is clearly observed how the capacitor C3 biased with -16 V during irradiation quickly reaches a flatband shift of ≈ -16 V, whereas the grounded capacitor C1 shows practically no flatband shift at low doses. The capacitor C2 experiences a smaller quick shift at low doses. At high doses the

shape of the flatband voltage shift vs. dose for capacitors C1 and C3 is identical, and similar to the shape of the curve for C2. The interface state densities calculated from the stretchout of C-V curves were found to increase from approximately 10^{11} $cm^{-2}eV^{-1}$ to $2\text{-}3\cdot10^{12}$ $cm^{-2}eV^{-1}$ during irradiation to 100 krad.

After irradiations we observed the annealing of the capacitors with no bias voltages applied. Figure 5. shows the development of flatband voltages for the different capacitors as a function of time after last irradiation. A logarithmic dependence on time, which is characteristic for annealing through electrons tunneling from the n-type bulk to the interface is clearly observed.

We also measured low-frequency thermal equilibrium C-V characteristics of the capacitors. For these measurements we developed a method utilizing the HP4145 parameter analyzer. Conventionally a thermal equilibrium C-V measurement is done using the quasi-static technique [11], where a slow voltage ramp is applied to the measured capacitor, and the current charging the capacitor is recorded. Hence the ratio of the current and the voltage ramp values gives the capacitance. In our method we inject a constant current to the capacitor and record the voltage during charge-up of the capacitor, and obtain the capacitance as the ratio between the current and the derivative of the recorded voltage. By decreasing the current used to charge the capacitor until the shape of the C-V curve no longer changes as a function of the charging current, we conclude that the capacitor is in thermal equilibrium during the measurement. For our capacitance value of ≈1300 pF we used a current of 25 pA, which results in a rate of voltage change of ≈ 20mV/s, which is a typical value for quasi-static measurements. We also checked that the leakage current of the capacitors was small compared with the injected current. Fig. 6. shows the development of the low frequency C-V curve for the capacitor C1 at low doses. The dramatic change in the shape of the curves is caused by the introduction of interface states, whose capacitance at the low

frequency dominates over the depletion region capacitance. For the biased capacitors the low frequency C-V curve becomes completely flat after 2-3 krad. This measurement confirms qualitatively the importance of interface states in the observed flatband voltage shifts presented earlier.

3.3 Discussion of results

Our measured results about the behavior of the threshold/flatband voltage shifts can be explained by a model that takes into account space charge effects of holes trapped in the bulk of the oxide in addition to the oxide charge due to holes trapped close to the interface. Both in the bulk and at the interface the amount of trapped charge depends on the electric field in the trapping region. With a negative gate voltage hole trapping close to the interface occurs only through radiation interactions in the thin region close to the interface, since the holes are swept away from the interface by the electric field caused by the gate voltage V_{gate} during irradiation. In the beginning of the irradiation trapping in the bulk occurs throughout the oxide, as illustrated in fig. 7a. As charge gets trapped in the bulk of the oxide, it modifies the electric field (fig. 7b), leading eventually to a field free region close to the interface (fig. 7c). When this field free region is formed, both trapping at the interface and trapping in the field free region in the bulk are strongly suppressed. As more charge gets trapped in the oxide, the field free region spreads from the interface towards the gate and thus diminishes the active thickness where hole trapping still occurs (fig. 7d). In the end there is a charge sheet close to the gate, which corresponds to $DV_{fb} = V_{gate}$ and an amount of charge trapped in the Si-SiO_2 interface that still increases with radiation as holes created by radiation interactions close to the interface get trapped to the traps available close to the interface. At this point the electric field in the oxide and at the interface is zero for all the capacitors regardless of their biasing, so that with

further irradiations the amount of charge trapped at the interface develops essentially in a similar way as a function of dose, as we observed in the test capacitors. Fluctuations between individual capacitors may be caused by differences in the quality of the interface. These differences may be large even between capacitors from different wafers in the same processing batch. From the logarithmic annealing of flatband shifts as a function of time after irradiation, we can assume that the annealing occurs by tunneling of electrons from the n-type silicon. This suggests that only the charges trapped close to the interface can be annealed. This means that a flatband or threshold voltage shift of $\Delta V = V_{gate}$ can still be observed even after long annealing times, as we observed in the long anneal of the FOXFET detector.

We can also make some quantitative calculations about how the measured results agree with simple theoretical estimates about the amount of charge trapped. From the energy deposited by radiation to silicon dioxide one can easily calculate the amount of charge (electron-hole pairs) created per unit dose, unit area and unit oxide thickness; this turns out to be $\approx 7.6 \cdot 10^{11}$ krad^{-1}cm$^{-2}\mu$m^{-1}. This has to be multiplied by our oxide thickness of 0.66μm and by an estimate for the fraction of charge escaping recombination at an electric field of $2 \cdot 10^5$ V/cm, which is roughly 0.2 [1], to obtain the total amount of charge available for trapping in our biased test capacitors. The calculation gives a result of $\approx 10^{11}$ cm^{-2}krad^{-1}. On the other hand we know that for example in the capacitor C3 the oxide charge after 6 krad is $5.1 \cdot 10^{11}$ cm^{-2}, which gives about $0.9 \cdot 10^{11}$ cm^{-2}krad^{-1}. According to this the trapping fraction for the oxide in question would be close to 1.0, which according to [1] is a reasonable assumption for an unhardened oxide.

4. Conclusions

We have observed electric field dependent hole trapping in negatively biased field oxides in planar processed silicon strip detectors and test structures. The results can be explained by a model that assumes hole trapping in the bulk of the oxide and considers the effect of that space charge on the shape of the electric field in the oxide. The results indicate that hole trapping in the bulk of the oxide occurs in a negatively biased field oxide until the flatband voltage shift caused by the oxide trapped charge equals the gate voltage applied during irradiation. In our measurements with voltages below -20V being applied over a ≈0.7 μm oxide this condition was reached after less than 5 krad of ^{137}Cs photon irradiation. In further irradiations the voltage applied over the oxide had little or no effect on the charge trapping, which occurred presumably at hole traps located close to the Si-SiO_2 interface.

In FOXFET biased strip detectors, where a negative voltage may be applied at the gate/field oxide of the transistor, the effect of charge trapped in the oxide is that of increasing the FOXFET threshold voltage and the voltage drop over the FOXFET at punch-through. From the point of view of FOXFET operation, the threshold voltage shift occurs away from the normal subthreshold working point of the FOXFET, so there is no danger of moving into an undesired operation region as a result of irradiation. The increase in the voltage drop over the FOXFET causes a decrease in the effective bias voltage at the strips, which can be accounted for by increasing the overall bias voltage applied to the detector.

In double-sided strip detectors a negative voltage being applied over a field oxide may be found if a field plate structure is used for the separation of n-side strips. In this case the charge trapped in the oxide in effect compensates the voltage applied to the field plate, and may eventually degrade the strip separation. Furthermore, charge trapped in the bulk rather than at the interface cannot be expected to anneal and will have adverse effects even during slow irradiations,

where annealing during irradiation may be expected to improve the detector lifetime.

By using a design with the field plate on top of a thin oxide layer rather than the field oxide, and by using a good quality oxide the radiation dose at which the oxide charging effects become crucial can be increased significantly.

Acknowledgements

We would like to thank Ray Yarema and Dean Connolly at Fermilab for the use of instruments in their groups, and also Tom Zimmerman at Fermilab for his help with the thermal equilibrium C-V measurements.

References

[1] Ma T.P. Dressendorfer P.V., "Ionizing Radiation Effects in MOS Devices & Circuits", J. Wiley & Sons, 1989.

[2] Allport P. et. al., "FOXFET Biassed Microstrip Detectors", NIM A310 (1991) 155 - 159.

[2] Laakso M. et. al.,"Operation and Radiation Resistance of a FOXFET Biasing Structure for Silicon Strip Detectors", FERMILAB-Conf-92/66, Feb. 1992.

[4] Caccia M. et. al., "A Si Strip Detector with Integrated Coupling Capacitors", NIM A260(1987) 124-131.

[5] Boesch H.E, McGarrity J.M., "Charge Yield and Dose Effects in MOS

Capacitors at 80 K", IEEE Trans. Nucl. Sci, NS-30, 4377, 1983.

[6] Boesch H.E. et. al., "Hole Transport and Trapping in Field Oxides", IEEE Trans. Nucl. Sci. Vol. 32, No. 6, 1985.

[7] Bacchetta, N. et. al., "Radiation Effects on CDF AC-coupled Microstrip Silicon Detectors", Proceedings of the Sixth European Symposium on Semiconductor Detectors, Milano, Italy, Feb. 24.-26., 1992.

[8] Longoni A. et. al., "Instability of the Behaviour of High Resistivity Silicon Detectors due to the Presence of Oxide Charges", NIM A288 (1990), 35-43.

[9] Nicollian E.H., Brews J.R., "MOS Physics and Technology", Wiley, New York, 1982.

[10].Boesch H.E., "Interface-State Generation in Thick SiO_2 Layers", IEEE Trans. Nucl. Sci. Vol. NS-29, No.6, 1446, 1982.

[11] Kuhn M. "A Quasi-Static Technique for MOS C-V and Surface State Measurements", Solid-State Electronics, Vol.13, 873, 1970.

Figure captions:

Figure 1. The threshold voltage shift of the FOXFET as a function of radiation dose. After 100 krad the detector was anncaled for 100 days before the next irradiation.

Figure 2. The leakage current of one detector as a function of time and increasing relative humidity. After 60%RH the leakage current becomes unstable and starts to increase.

Figure 3. CV measurement results of capacitor C1 after different doses. A calculated ideal curve with no oxide charge is also included. The shift in the flatband voltage and stretchout caused by interface states can be clearly observed in the irradiated curves.

Figure 4. Flatband shifts for different capacitors as a function of radiation dose. Note the quick changes at low doses, which are equal to the voltage applied to the gate during irradiation.

Figure 5. Annealing of flatband voltages. Logarithmic dependence on time suggests that the annealing occurs as a tunnel anneal by electrons tunneling to the oxide from the n-side bulk.

Figure 6. Low frequency thermal equilibrium CV measurement for C1 at different doses. The interface state capacitance dominates over depletion region capacitance after irradiation at low frequencies, and causes the curves to become flat.

Figure 7. Schematic of the charge trapping process in the oxide. The electric field inside the oxide is depicted on the left.

a) before irradiation

b) in the beginning of the irradiation, when the flatband voltage shift caused by oxide trapped charge is still less than the gate voltage during irradiation

c) at the point when the flatband shift equals the gate voltage, and the field

free region is formed at the interface

d) the field free region has extended inside the bulk, and electrons and holes recombine efficiently in the shaded area

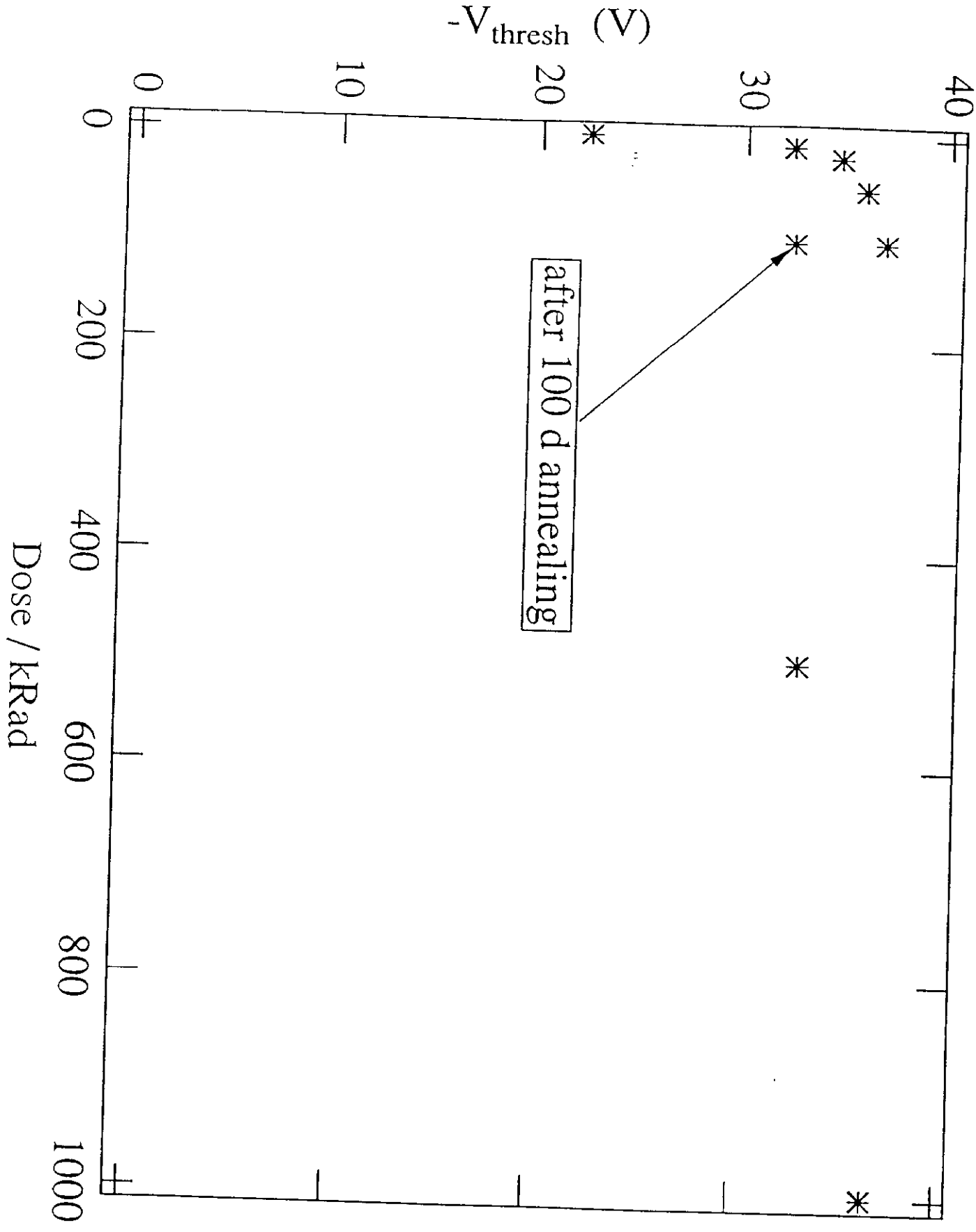

-V thresh (V)
0
10
20
30
40
0
200
400
600
800
1000
Dose / kRad
after 100 d annealing

Figure 1

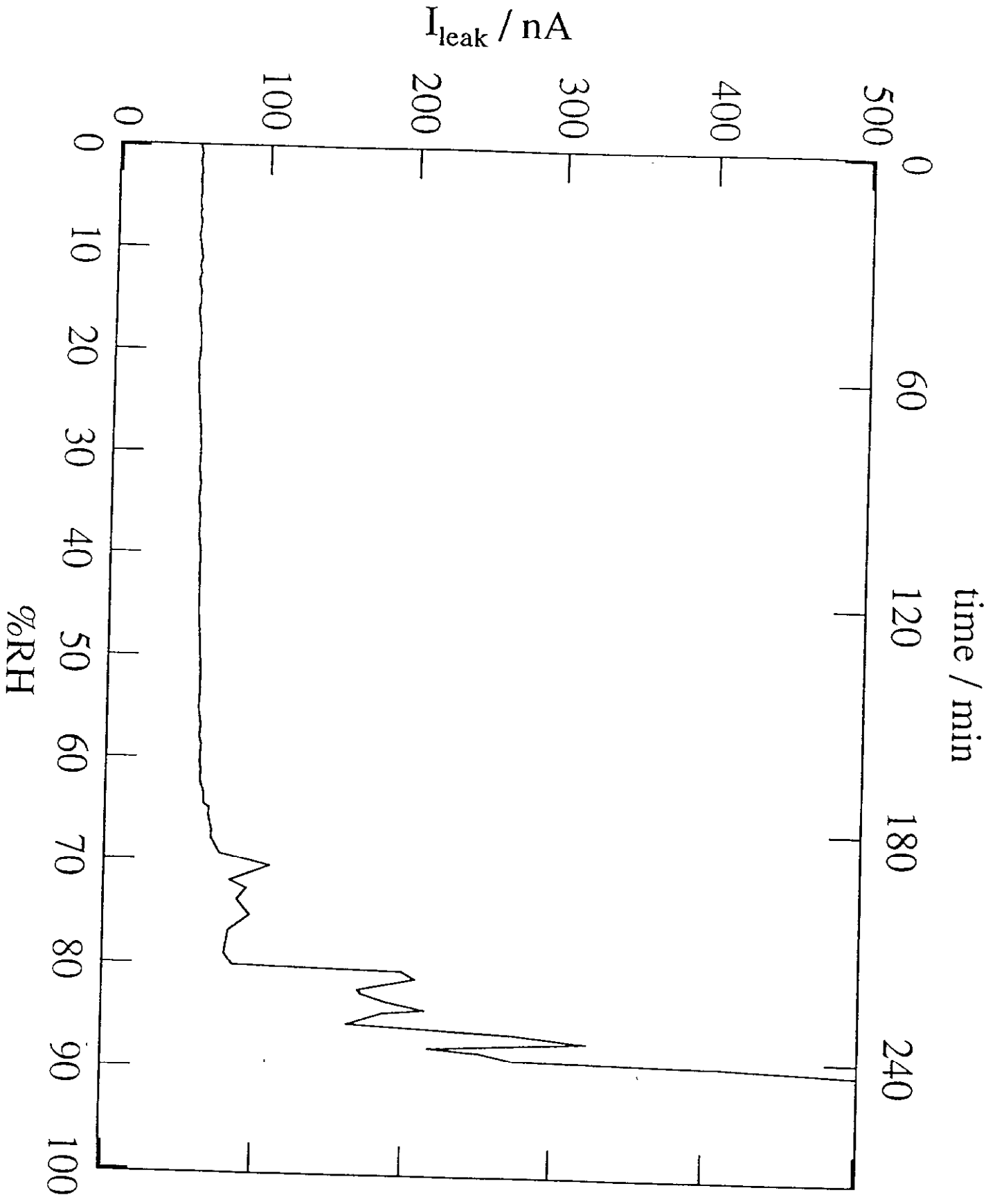

I_{leak} / nA
0
100
200
300
400
500
time / min
0
60
120
180
240
%RH
0
10
20
30
40
50
60
70
80
90
100

Figure 2

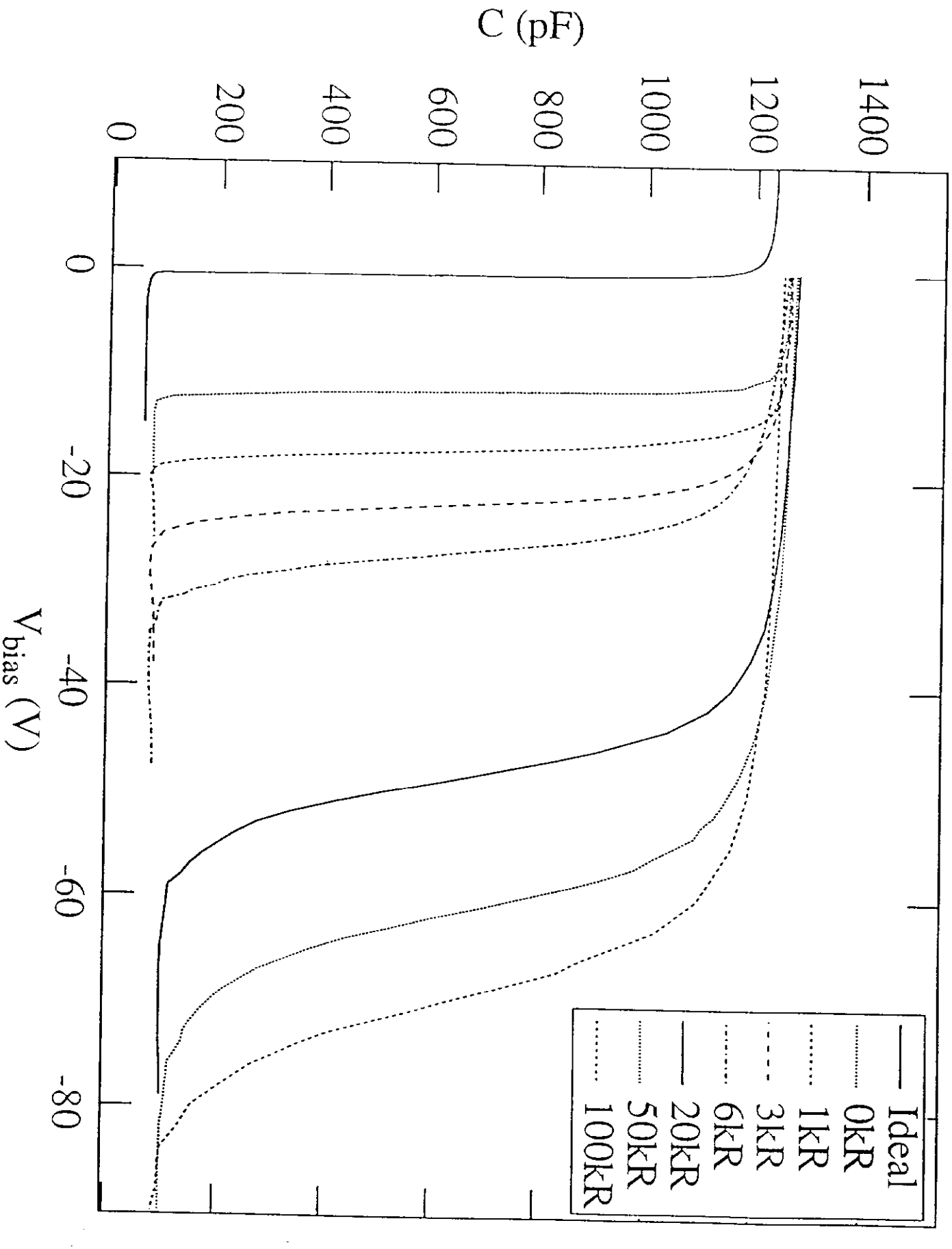

C (pF)
0
200
400
600
800
1000
1200
1400
0
-20
-40
-60
-80
V_{bias} (V)
Ideal
0kR
1kR
3kR
6kR
20kR
50kR
100kR

Figure 3

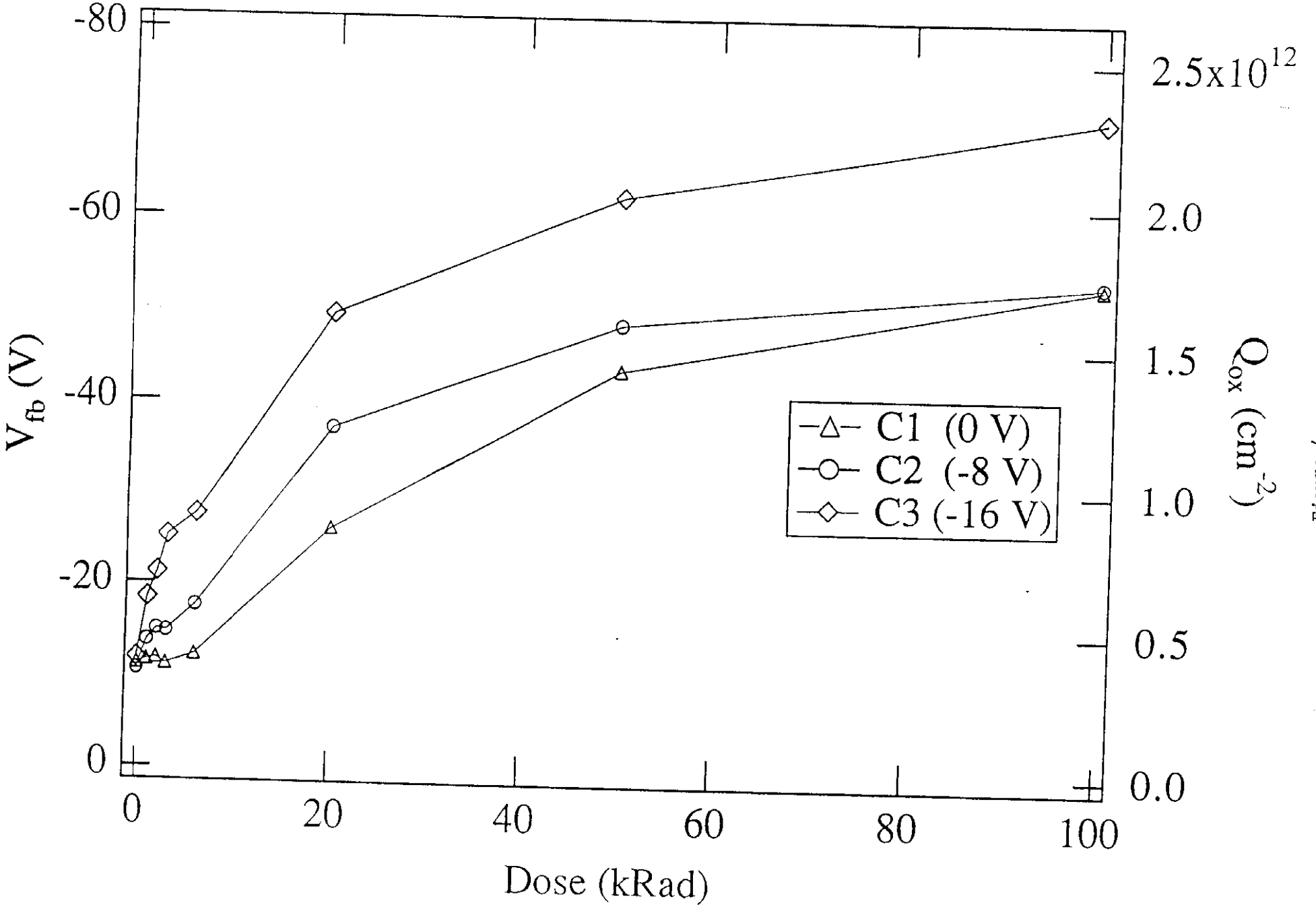

-80
-60
-40
-20
0
V_{fb} (V)
0
20
40
60
80
100
Dose (kRad)
$2.5x10^{12}$
2.0
1.5
1.0
0.5
0.0
Q_{ox} (cm^{-2})
C1 (0 V)
C2 (-8 V)
C3 (-16 V)

Figure 4

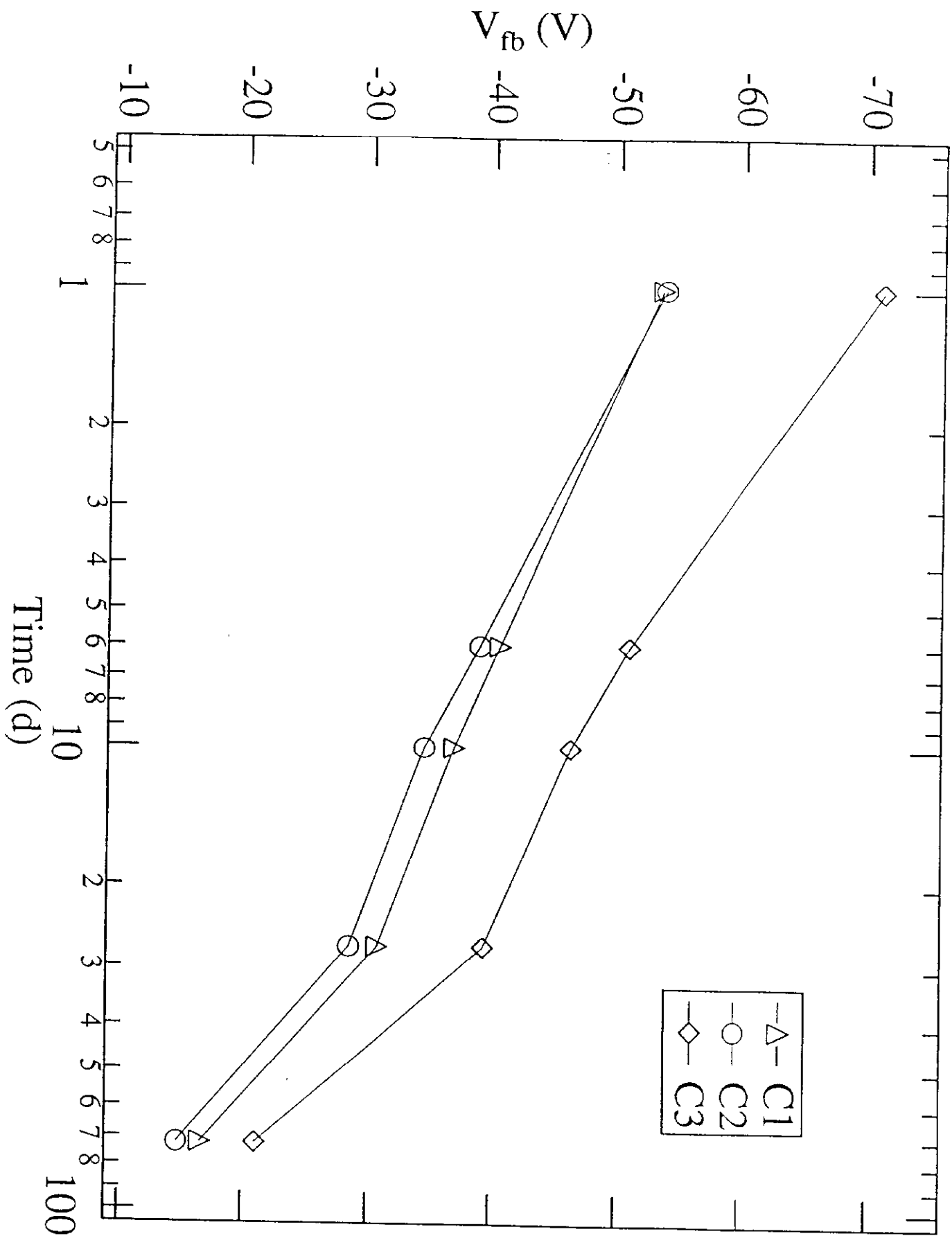


Figure 5

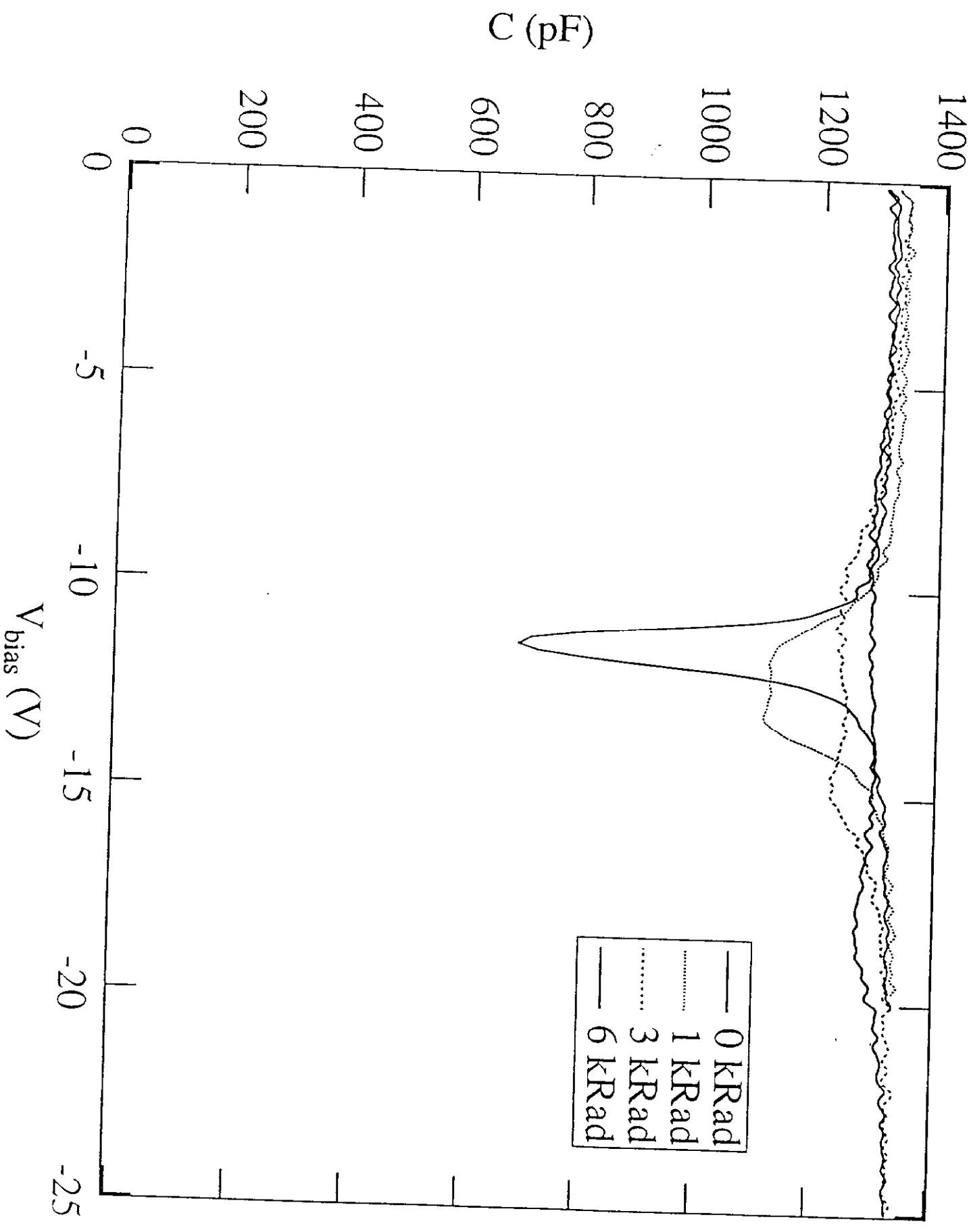
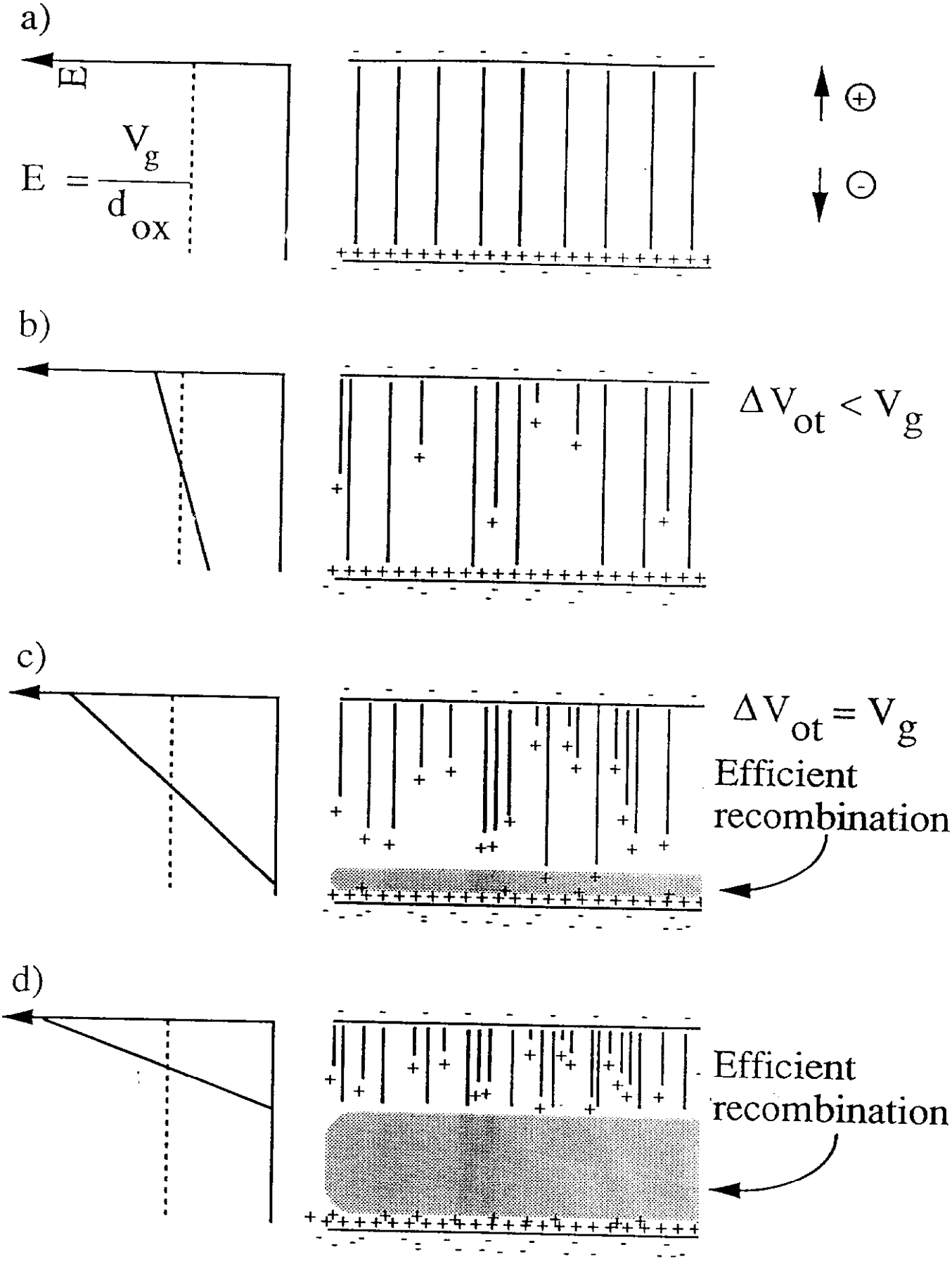

C (pF)
0
200
400
600
800
1000
1200
1400
0
-5
-10
-15
-20
-25
V_{bias} (V)
0 kRad
1 kRad
3 kRad
6 kRad

Figure 6


a)
E
$E = \frac{V_g}{d_{ox}}$
b)
$\Delta V_{ot} < V_g$
c)
$\Delta V_{ot} = V_g$
Efficient recombination
d)
Efficient recombination

16. 7.

Figure 7