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The analog front end for FastRICH: an ASIC for the LHCb RICH detector upgrade

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Abstract: This work presents the analog circuitry of the FastRICH ASIC, a 16-channel ASIC, developed in a 65 nm CMOS technology specifically designed for the RICH detector at LHCb to readout detectors like Photomultiplier Tubes to be used at the LHC Run 4 and Silicon Photomultipliers candidates for Run 5. The front-end (FE) stage has an input impedance below 50 Ω and an input dynamic range from 5 µA to 5 mA with a power consumption of ∼5 mW/channel. The chip includes a Leading Edge Comparator (LED) and a Constant Fraction Discriminator (CFD) for time pick-off and a Time-to-Digital Converter (TDC) for digitization.

Keywords: Analogue electronic circuits; Cherenkov and transition radiation; Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons); Radiation-hard detectors

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1 Introduction

The increase in luminosity during HL-LHC Run 5 causes a challenging rise in particle multiplicity and hit occupancy also for the LHCb Ring Imaging Cherenkov (RICH) subsystem [1]. The increased irradiation level dictates a shift in the electronics from FPGAs to a more radiation-hard ASIC with a time resolution of better than 100 ps in order to keep the high particle identification performance after the Upgrade II [2]. The availability of fast-timing data from the detected Cherenkov photons can be employed to enhance particle identification performance and improve the signal-to-background ratio of the detectors. This work focuses on the analog front-end electronics proposed for a future upgrade of the RICH system with Multi-Anode Photomultiplier Tubes (MAPMTs) in LHC Run 4 and small Silicon Photomultipliers (SiPMs) during Run 5.

2 The FastRICH ASIC

The FastRICH is an ASIC developed in a 65 nm CMOS technology specifically designed for the RICH detector at the LHCb experiment. It builds on the experience with the FastIC ASIC [3, 4], and adapts its architecture, adding specific characteristics required, for the RICH detector. The most significant stages are: (1) a configurable input Front-End stage capable of reading MAPMTs, small SiPMs and Microchannel Plates (MCPs); (2) a Constant Fraction Discriminator (CFD) to minimize time walk variations and avoid the need to send the time-over-threshold (ToT) information to the back-end, reducing the amount of output data; (3) a Time-to-Digital Converter (TDC) to digitize the data; (4) a digital zero suppressed readout circuit; and (5) programmable output links for data transmission.

Figure 1 shows a block diagram of the analog signal path and the TDC of a single channel of the ASIC. The configuration allows using either the positive or negative input stage. The most susceptible analog blocks are designed with Enclosed Layout Transistors (ELT) geometry to minimize the cumulative effects from radiation on the electronics [5]. The aspect ratio of this ELT devices must be designed accordingly at the layout stage to enhance the radiation tolerance [6]. Time-of-Arrival measurement is generated through a CFD. In addition, the ASIC also provides a nonlinear ToT energy signal through a Leading-Edge Discriminator (LED) for calibration purposes. CFD or LED binary output signal will be digitized on-chip by means of a TDC with adjustable time bin, ~25 ps for the high-performance mode or ~50 ps for the low-power mode. The digital circuitry will be implemented

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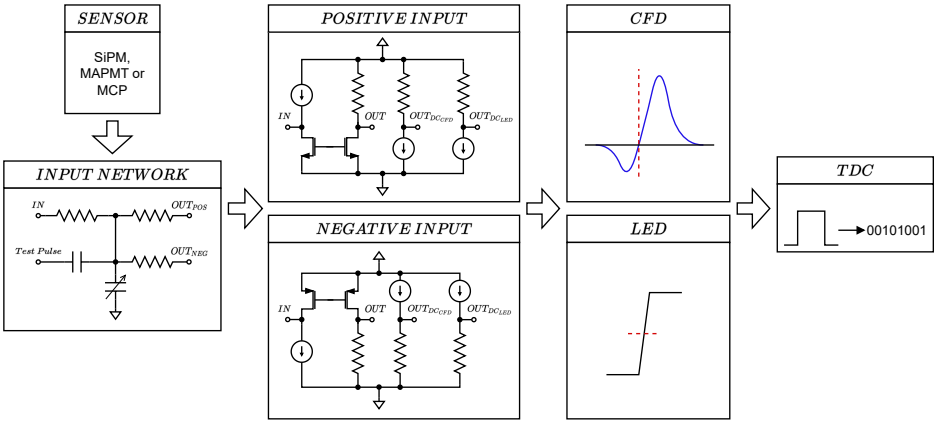

Figure 1. FastRICH ASIC block diagram.

using Triple Modular Redundancy (TMR) to improve radiation tolerance, and therefore the chip is radiation tolerant by design. The power consumption per channel is ~5 mW.

The FastRICH ASIC includes several features aimed at improving data throughput. Cherenkov photons arrive within specific time windows within the 25 ns LHC clock period. A programmable hardware shutter, allows selecting the signals of interest in a timing window that is foreseen to be in the order of a few ns per Bunch Crossing (BX) and filters background and reflected events arriving later. Moreover, the employment of the CFD avoids sending the ToT information and thus reducing the output data bandwidth. Lastly, Data at a given BX is zero-suppressed and encoded in variable-length packets, which will in turn be transmitted by one of 4 independent lpGBT/VTRx-compatible SLVS output links, which provide the chip a total maximum output bandwidth of up to 5.12 Gbps. A framing protocol ensures DC balancing and link self-recovery in case of readout errors. The number of active output links is configurable so that the chip can be optimized to operate in regions in the experiment with different occupancy.

3 Analog front end

The input stage processes the input signal in current mode with an input impedance below 50 Ω and an input dynamic range from 5 µA to 5 mA. It is programmable to work with positive or negative input polarity signals delivered by low capacitance sensors with intrinsic amplification, such as MAPMTs, small area (1×1 mm^2) SiPMs, or MCPs. The FE consists of two complementary (positive and negative polarity) input stages based on a high performance unity gain current mirror with two control feedbacks.

Figure 2 shows the schematic of the positive and negative polarity input stages of the FastRICH ASIC. It consists of a high performance unity gain current mirror with two control feedbacks. A Low Frequency Feedback loop (LFF) adjusts the DC voltage at the input node (IN). The High Frequency Feedback loop (HFF) keeps the input impedance low at high frequencies. This voltage is set at the positive input of OTA1 (V_{ANODE} for the positive polarity, $V_{CATHODE}$ for the negative polarity). Transistor M_4 is a DC voltage Level Shifter that allows increasing input DC voltage, keeping M_2 in saturation. Transistors M_1 and M_6 form a current mirror with a 1:1 ratio. OTA2 regulates M_7 gate voltage and adds a virtual short-circuit between M_1 and M_6 drains. This improves the accuracy of the current copy [7]. Transistor M_3 is a bias transistor that provide the DC bias current for the input branch.

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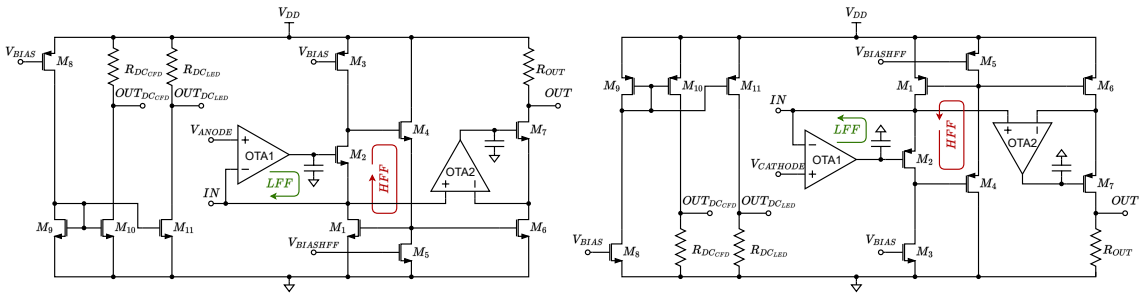

Figure 2. Simplified Positive (left) and Negative (right) input stage circuits.

The output signal of this block is a pseudo-differential voltage signal formed by the pulse at the OUT node and the DC reference signal from OUT_{DC}. The output signal branch features an output resistor (R_{OUT}) to convert the current copied from the input by transistor (M_6) into a voltage (OUT). The resistor value and the DC bias current adjust the DC operating point for the discriminators inputs. Two DC voltages ($OUT_{DC_{CFD}}$ and $OUT_{DC_{LED}}$) present the same value as the baseline voltage of the output signal generated by resistors $R_{DC_{CFD}}$ and $R_{DC_{LED}}$. Since no AC signal current is flowing through the DC output branches, and with the objective of reducing the power consumption of the circuit, $R_{DC_{CFD}}$ and $R_{DC_{LED}}$ values are 8 times larger than R_{OUT} and the DC current flowing through them is 8 times lower, achieving the same DC voltage at nodes $OUT_{DC_{CFD}}$, $OUT_{DC_{LED}}$ and OUT. Resistors R_{OUT}, $R_{DC_{CFD}}$ and $R_{DC_{LED}}$ are adjustable with the objective to compensate for process variations after manufacturing.

With large signals, the current peak at the output node OUT will translate into a voltage drop, moving transistors M_6 and M_7 into the linear region. Therefore, the peak amplitude will not follow a linear behavior. But this drawback does not present a big problem, since the ASIC is focused on Time-of-Arrival detection, thus preserving the shape of the input pulse is not critical. In addition, the expected range of operation is in the order of single photon detection, where the response is linear.

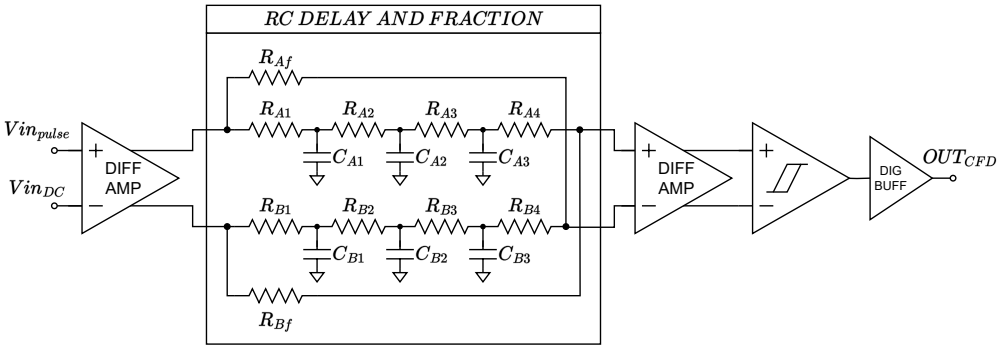

Figure 3. Constant Fraction Discriminator block diagram (left) and RC delay and fraction implementation (right).

The use of CFDs is very effective to reduce the time walk in applications with a reduced dynamic range and a large dispersion on the mean arrival time of the events, for instance, when reading a PMT [8]. Figure 3 shows the block diagram of the CFD, including the implementation of the delay and signal fraction with a cross coupling configuration employing capacitors and resistors. The CFD implemented in the FastRICH is optimized, with fixed component values, for the signal provided by a PMT.

4 Simulation results

Figure 4 shows the transient voltage output for the positive and negative polarity input stages. The positive polarity input stage is tested with a SiPM model, while the negative polarity input stage is tested with a PMT signal.

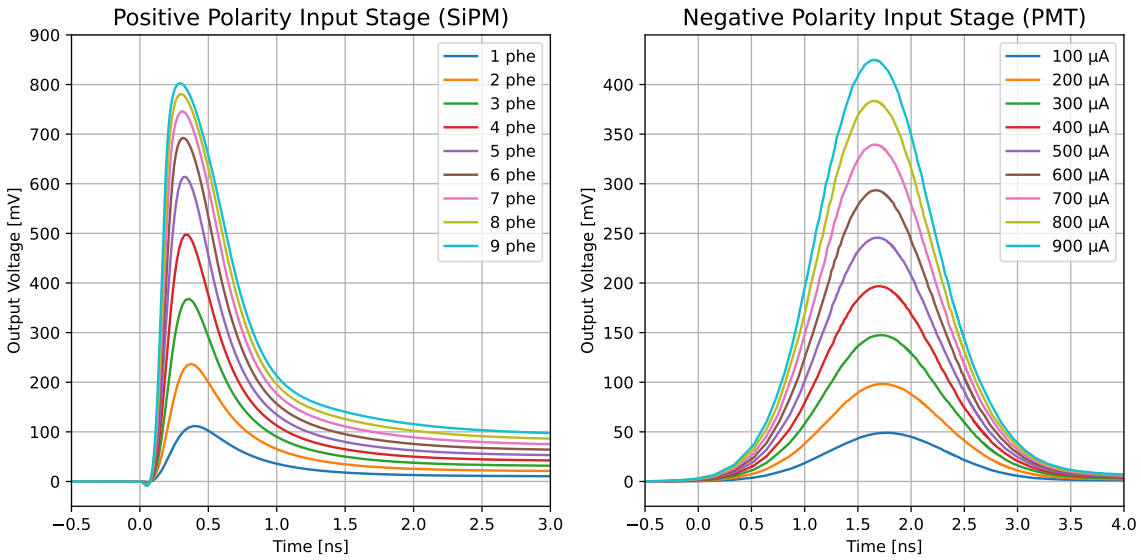

Figure 4. Front End output transient voltage.

Figure 5 shows the results of the evaluation of the linearity of the input stages. The positive polarity input stage output response is linear up to ~0.8 mA of input current amplitude, which corresponds to an output voltage amplitude of ~500 mV. On the other hand, the negative polarity input stage implements a configurable attenuation system that allows for an extended range of operation. Results shown in figure 5 correspond to maximum attenuation for the negative polarity input stage.

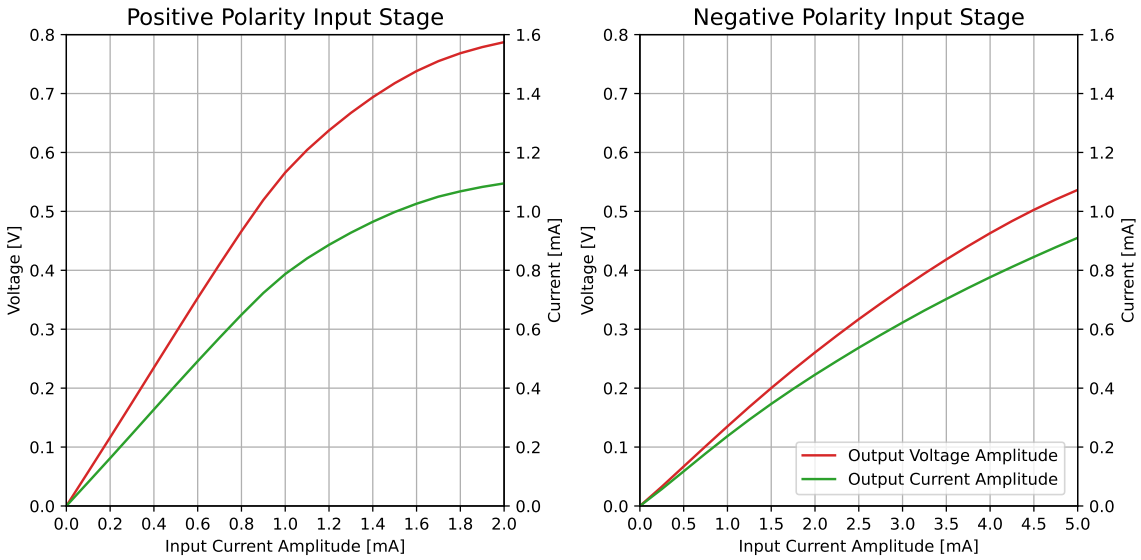

Figure 5. Output voltage and current peak amplitude results for the positive and negative input stages. Negative input stage configured with maximum attenuation to extend the dynamic range.

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Figure 6 displays the differential analog output of the CFD after the RC filter block and the discriminated signal after the Zero-crossing Comparator (ZCC), which provides the time stamp of the arriving photons. Simulations results show a time walk below 70 ps when employing a signal from a PMT. Simulations performed with the LED comparator show that it exhibits a time walk of about 1.6 ns, which is notably larger compared to that of the CFD.

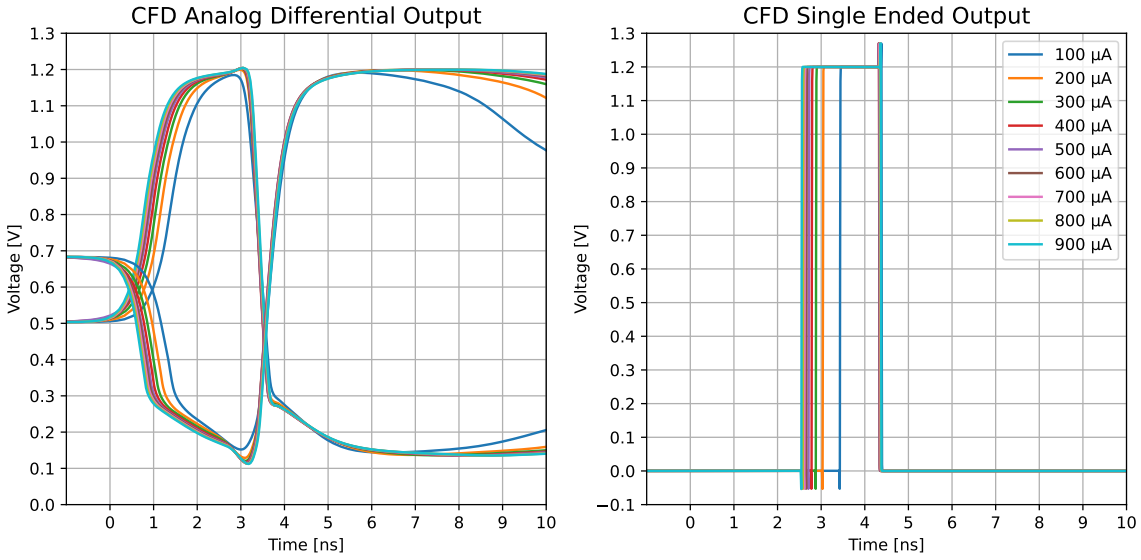

Figure 6. Constant Fraction Discriminator analog differential output (left) and single ended discriminated output (right).

5 Conclusions

The FastRICH ASIC implements the required characteristics to be installed in the LHCb RICH subsystem in the future upgrade of the LHC, such as a CFD and a TDC integrated in the ASIC. It is designed to readout positive and negative polarity signals generated by MAPMTs, small SiPMs and MCPs with 16 channels and a power consumption of ~5 mW per channel. Simulations performed with a signal from a PMT of the implemented CFD show a time walk below 70 ps, improving notably the result of 1.6 ns obtained with the LED.

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