ISBN: 978-3-95450-211-0 doi:10.18429/JACoW-SRF2019-THP029

TOWARDS REAL-TIME DATA PROCESSING USING FPGA TECHNOLOGY FOR HIGH-SPEED DATA ACQUISITION SYSTEM AT MHz REPETITION RATES

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Abstract

Accelerator-based light sources, in particular, those based on linear accelerators, are intrinsically less stable than lasers or other more conventional light sources because of their large scale. In order to achieve optimal data quality, the properties of each light pulse need to be detected and implemented into the analysis of each experiment. Such schemes are of particular advantage in 4th generation light sources based on superconducting radiofrequency (SRF) technology, since here the combination of pulse-resolved detection schemes with high-repetition-rate is particularly fruitful. Implementation of several different purpose-built CMOS linear array detector will enable to perform arrival-time measurements at MHz repetition rates. An architecture based on FPGA technology will allow an online analysis of the measured data at MHz repetition rate and will decrease the amount of data throughput and disk capacity for storing the data by orders of magnitude. In this contribution, we will outline how the pulse-resolved data acquisition scheme of the TELBE user facility shall be upgraded to allow operation at MHz repetition rates and sub-femtosecond timing precision.

INTRODUCTION

Terahertz radiation offers unique control of low-energy excitations in the matter. Fundamental modes such as molecular rotations, lattice vibrations, electron and ion motion or spin precession can be coherently controlled on the ultra-scale, while parasitic electronic excitations are suppressed, because of the low THz photon energy. The main challenges which have impeded the experimental realization are the availability of high field and high repetition rate THz sources, knowledge, and control of the interaction of photoelectrons with THz-field.

Femtosecond level diagnostic and control of sub-picosecond electron bunches is an essential topic in modern accelerator research. At the same time, new quasi-cw linear electron accelerator is the driver of many 4th Generation light sources such as X-ray free electron laser. High duty cycle, high stability, and online pulse to pulse diagnostics of these new accelerators are crucial ingredients to the success of these large scale facilities. A novel THz based online monitor concept is presented that has the potential to give access to pulse information on bunch form, arrival time and energy at high repetition rate and down to sub pC charges [1]. It has been shown that pulse experimentally to pulse arrival time measurements can be used to perform high temporal resolution and dynamic range experiments, removing the influence of synchronization problems between the accelerator and external laser systems.

The rapid evolution of high-speed processors has allowed scientists to reduce the time needed to process data from several hours to a few minutes. Due to the different methods of data processing and the urgent need to increase the resolution, speed of measurement, and get the results in the shortest time, many developers of data acquisition systems are considering Field Programmable Gate Array (FPGA) technology.

The Data Acquisition (DAQ) system presented in this paper is for obtaining time-resolved measurements of various materials, utilizing THz at accelerator-based photon sources as in [2,3]. However, THz-driven phenomena experiments using the method of THz pump-Laser probe have many challenges, namely the instabilities and synchronization with the modern fs laser systems.

This paper organized as follows: first; we will present the current Data Acquisition (DAQ) system at the THz source at the Electron Linac for beams with high Brilliance and low Emittance (TELBE) that is used to measure the electrical and magnetic properties of samples, along with the challenges and limitations. Second; we will explain the signal processing methods we apply to the raw data in the sorted and binned data that is used to obtain the results. Finally, we will present our current development progress on the FPGA-based DAQ system and its prospects.

DAQ SYSTEM AT TELBE

The TELBE facility currently operates two superradiant THz sources, a Coherent Diffraction Radiator (CDR) source and an undulator source. The THz emission characteristics are distinctly different, offering TELBE users the choice to work with either quasi-single-cycle or multi-cycle THz pulse forms, or even both. In the following, fundamental properties of these two sources that are of vital interest for users of the TELBE facility shall be quantitatively compared. Namely, the maximum achievable pulse energy together with the achievable intensity- and timing-stability. The pulse-resolved data acquisition system at TELBE has been used for the pulse-resolved characterization of the CDR source and the undulator source in parallel. Thereby the measurements can be directly compared. The current pulse-to-pulse data acquisition system has an optimal timing resolution of 12 femtosecond Full-Width Half Maximum (FWHM), as determined by the physical properties of its design.

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In order to understand the proposed MHz repetition rate DAQ system in this paper, we will shortly explain the current DAQ system at TELBE: characteristics, challenges, and significant trade-offs.

A pulse-to-pulse DAQ system was developed at TELBE for use at repetition rates of 100 kHz. For each pulse, we record two data channel: the arrival time information of the THz pulse, and the experimental data, which are the laser probe pulses, as shown in Fig. 1.

For each THz pump pulse at a repetition rate of 100 kHz, two laser pulses of duration 100 femtoseconds (fs) are applied to the sample at a repetition rate of 200 kHz with a variable delay between the THz and laser pulses. Depending on the experiment and the sample, a mechanical step delay changes the time the pump and probe pulses arrive at the sample, with 100 thousand THz pulses for each step to improve the Signal-to-Noise Ratio (SNR).

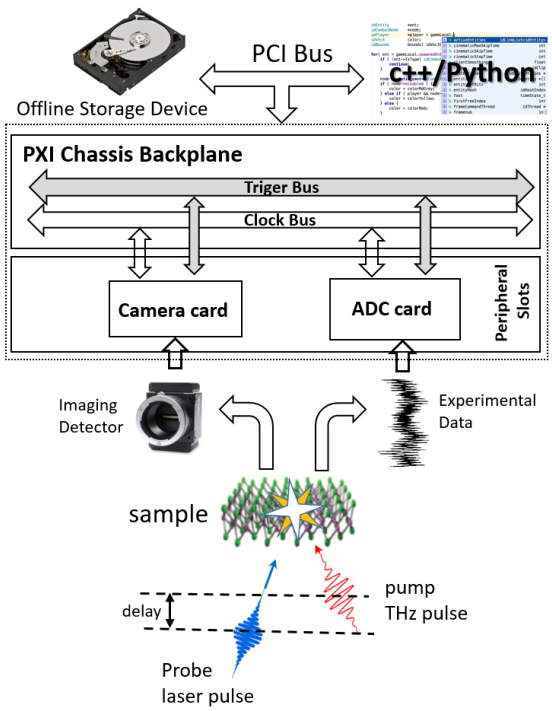

Figure 1: Block diagram for the current DAQ system hardware at TELBE.

The experimental and arrival time raw data are then sent to the offline storage devices for further signal processing and data analysis.

Arrival Time Measurements

Several signal processing operations need to be done on the measured arrival time information to achieve an excellent time resolution and performance accuracy of a few ten fs. For each THz pulse, a signal consists of 2048 pixels as a readout data from an spl2048 camera as in Fig. 2.

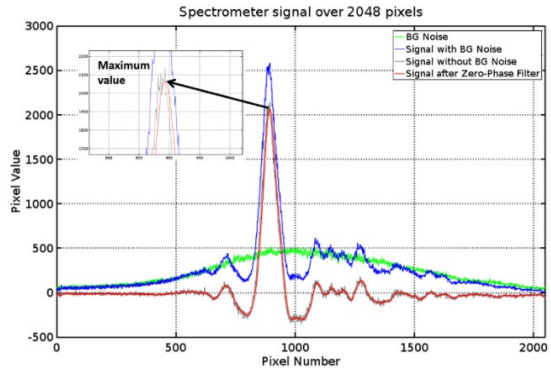

Figure 2: The signal measured by the spL2048 camera for single-shot measurement of THz pulse at TELBE. The repetition rate in these measurements was 100 kHz.

The three signal processing operations are: subtracting the pixels form the background noise, then applying the zero-phase filter on these pixels to reduce noise, and then calculating the location of the peak. Finally, Eq. (1) is used to determine the arrival time of the THz pulse.

$$PD_{ps} = MP_{x\_value} * Pixel_{Width} + DeSP/c. \quad (1)$$

Where PD is the position of data, MP is the maximum point, DeSP is the delay stage position, ps is picosecond, and c is the speed of light in meter per second.

Experimental Data Measurements

After determining the arrival time of each THz pulse in a time resolution of a few ten fs, a further signal processing and calculations need to be done on the measured experimental data. The experimental data are measured using two laser probe detectors which are connected to the 10 MSPS TB-2708 ADC card. Depending on the experiment, one or both values of the two detectors may, and then the mean of the 100 samples measured by the ADC is calculated.

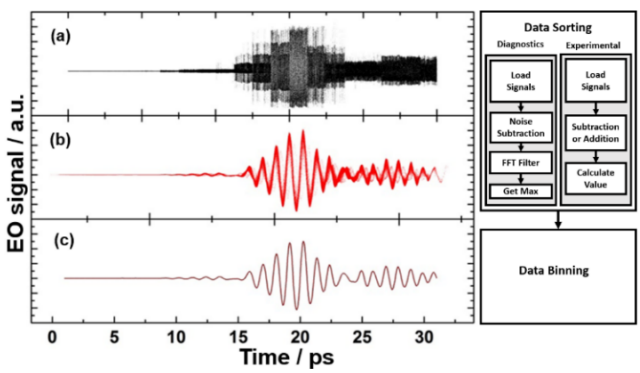

Figure 3: Electro-Optic Signal (EOS) of 0.9 THz pulses: (a) Raw, unsorted data. Timing from delay stage position only, (b) Added arrival time data from pulse-resolved diagnostics, (c) Averaged data in 50 fs wide bins.

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The signal processing of the diagnostics data and the experimental data can be done in parallel as in Fig. 3. However, the data binning, which is the final step of the signal processing in the raw data, is done in series after finishing the signal processing on both of the diagnostics and experimental data. The data averaging is a simple calculation of the data in 50 fs wide bins.

Challenges and Trade-offs

The demand for high SNR and more accurate time resolution has lead in the recent years to enhancements of the sensor technology and ADC architecture. However, increasing the clock rate in the ADC, and thus, the increase in the data acquisition rate, make the task of saving and processing the data more complex. In the current DAQ system at TELBE, the raw data is saved in offline storage devices. Therefore a lot of disk capacity, as well as the very high data throughput, is required to move this raw data to and from the storage devices.

The current DAQ system at TELBE faces the challenge of allocating the required resources to save the long-time scale data of a few weeks at 100 kHz repetition rates of THz pulses. For each day tens of loops are measured. The required disk capacity to store one loop of raw data is 89.7 Gigabytes. Each loop consists of 200 steps, and the raw data comes from two channels: first, the diagnostics data at 100 kHz of THz pulses each takes 2048 pixel every ten µs at 12 bits resolution that results in 82 Gigabytes per Loop. Second, the experimental data that comes from the 10 MSPS ADC card with 12 bits resolution per sample that results in 7.7 Gigabytes per Loop. Interfacing higher speed ADC card or higher frame rate imaging detector will dramatically increase the required resources of memory, channel bandwidths, and disk capacity. Moreover, further signal processing on the raw data is required to load the data again from the storage devices for data sorting and binning analysis.

FPGA-BASED DAQ SYSTEM

In recent years, the rapid development in the reconfigurable processing units, namely the FPGA that contains thousands of embedded Digital Signal Processing (DSP) units make the online data processing more attractive for the developers of high speed DAQ systems. These reconfigurable processing units can perform the required parallel processing to process the data stream from an ADC which can generate vast amounts of raw data. In this paper, we will present our development of improving the repetition rate of our DAQ system using KALYPSO detector version 2.1 as in [4, 5] with interface implemented in High-Flex FPGA board as in Fig. 4.

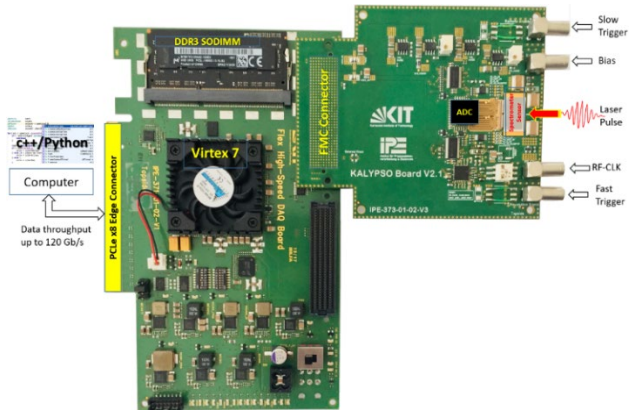

Figure 4: FPGA KALYPSO interface architecture.

Challenges and Trade-offs

The linear array imaging detectors are integrated circuits used for measuring the light intensity [6]. There are two major imagining detectors technologies: the Complementary Metal-Oxide-Semiconductor (CMOS), and the Charge-Coupled Devices (CCD). The imaging detector consists of pixels. The pixel size is an important parameter that affects the SNR because the pixel size is directly propotional to the number of received photons, and that results in less noise. High frame rates can be achieved by massive parallelism. However, the frame rate of the high-speed image sensors is limited by the pixel access time. Therefore, commercially available imaging detectors decrease the number of pixels while increasing the frame rate. In our work at TELBE, we are interested in the monochrome linear array imaging detectors with ultra-high line rate, high SNR, and the maximum number of pixels.

The current linear array imaging detector used at TELBE supports a line rate up to 140 kHz. A total of 2048 pixels can be taken in each frame with pixel size 10 µm x 10 µm. The specifications of the KALYPSO version 2 imaging detector are presented in Table 1.

Table 1: Comparison of the Characteristics of the Image Sensors Used at TELBE

Specification	Basler SPL2048	KALYPSO v2
Number of pixels	2048 pixels	256 pixels
Pixel width	10 µm	50 µm
Pixel height	10 µm	3 mm
Sensor type	CMOS	CCD
Wavelength	400nm - 1µm	300nm - 1µm
Colour	Mono	Mono
Line rate	Up to 140 kHz	Up to 2.7 MHz
Sensor width	20.5 mm	12.8 mm
Pixel bit depth	12 bit (ADC)	12 bit (ADC)

Due to the limitations in the number of pixels supported by high frame rates imaging detectors available today, we decided to use the KALYPSO linear array detector due to

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its unprecedented MHz line rate and 256 pixels. KALYPSO is a front-end ASIC that measure photon energy at the range of visible light as in [4, 5].

FPGA Board and KALYPSO Interface

The High-Flex board as in [7] has VIRTEX XC7VX330T FPGA on it, with almost 2 million of Configurable Logic Blocks (CLBs), 68 Mb of RAM Blocks (BRAM), 4 Gigabyte of DDR3 with 64 lanes at 1866 Mb/s, two High Pin Count FMC connectors, and a PCIe Gen 3 x 16 lanes that enable a full duplex data throughput up to 130 Gb/s. The Printed Circuit Board (PCB) has 16 layer metals stack, and support a picosecond time controlled transmission lines.

The hardware interface between KALYPSO detector and the High-Flex FPGA board is done by FMC connector as in Fig. 4. The KALYPSO detector has two ADS52J90 ADCs that are connected to the imaging sensors, and interfacing with the FPGA by the serial Low Voltage Differential Signalling (LVDS) interface that provide the digital data to the FPGA.

Several ADC signal controls are used to control the data rate and the bit resolution of the ADC chip, and LMK03001C is used to clean the jitter.

Table 2: FPGA Resources Utilized

Resource	Available	Used	Percentage Used
Logic Cells	326,400	67.391	%20.6
SLICEs	51,000	3.850	%7.5
Block RAM 18 Kb	1,500	680	%45.3

Table 2 lists the resources percentages used in VIRTEX-7 FPGA as in Fig. 4. The implemented MHz repetition rate DAQ system causes a significant challenge in allocating suitable computer resources to handle the massive volume of recorded raw data.

FPGA-PC Interface

In order to maximize the throughput of the PCIe connection and minimize the FPGA resources utilization, the data flow, registers, memory organization between the Direct Memory Access (DMA) engine and the Linux Driver for interfacing the front end of KALYPSO detector to the High-Flex FPGA readout are based on the solution provided by the Institute for Data Processing and Electronics, Karlsruhe Institute of Technology (KIT) as in [8].

The DAQ software was written in Python language to control the data flow between the FPGA board and the PC. Also, the software has a Graphical User Interface (GUI) to monitor the signal, and perform some basic mathematical calculations to fit the requirements of the pump-probe experiments at TELBE user facility.

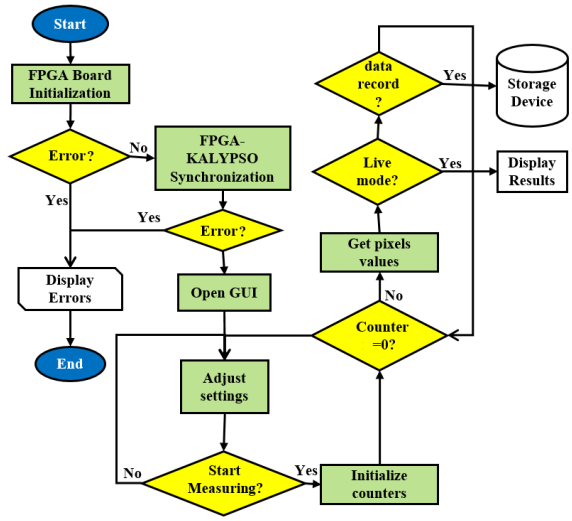

Figure 5: Flow chart of the GUI internal operations for the FPGA-Based DAQ system at TELBE.

The internal operations of the FPGA-PC interface are shown in Fig. 5. The first step is to check the status of the High-Flex FPGA board and the synchronization with the KALYPSO card. If there is no error, then the GUI is enabled for users to adjust the required settings. For MHz frame rate measurements, the GUI automatically adjusts the presentation of data on the user screen.

SYSTEM CHARACTERISTICS AND RESULTS

A practical approach to improve the repetition rate of our DAQ system at TELBE has been presented. In this paper, a pulse-to-pulse FPGA-Based DAQ was developed for use at MHz repetition rates. For each pulse, several data channels can be taken.

Currently, an image file containing the arrival time information is recorded. This data can be used to improve the dynamic range and time resolution in time-resolved experiments. The developed system was characterized throughout this work, and an excellent performance could be established.

The previous DAQ system drawback is the fact that online data sorting and the overall data handling only allow operation with roughly a 25% duty cycle. For every 1 second of data taken at 100 kHz, roughly 3 seconds are required to write the data to storage. However, implementing FPGA architecture is capable of achieving the necessary speed to process data between pulses, as well as improving the transfer rate of data to storage.

The KALYPSO linear array detector is capable of monitoring the arrival time of THz pump pulses at a rate of 2.7 MHz with 256 pixels per frame, and 12-bit resolution per pixel. The data volume increase to 280 Gigabytes per loop, which means a percentage increase of 480 with the comparison to the current DAQ system used at TELBE.

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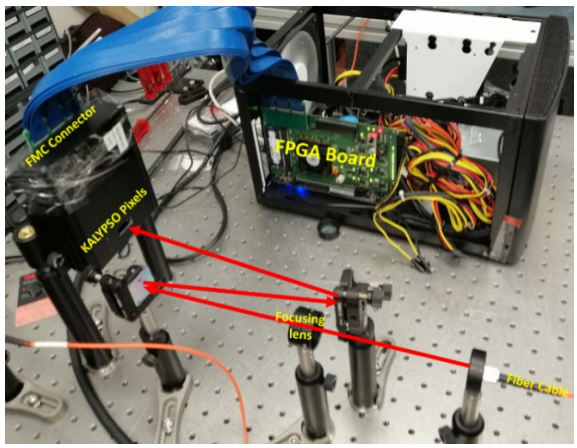

Figure 6: Picture of the FPGA-Based DAQ installed at the EOSD experimental setup at TELBE.

The FPGA-Based DAQ system has been installed at the Electro-optic sampling (EOS) experimental setup at TELBE, as shown in Fig. 6.

The Electro-optic sampling system is most commonly used to measure the time domain form of THz pulses. They work by altering the polarization of a probe beam that propagates through the electro-optic crystal co-linear with a THz pulse. This effect is quasi-simultaneous and can be used to detect signals on femtosecond timescales.

For ZnTe crystal the condition is met for THz pulses by using an 800 nm probe pulse. Another parameter of importance is the group velocity mismatch (GVM). This is the difference in group velocity between the THz pulse and the probe pulse. For instance, in ZnTe using an 800 nm probe, there is a GVM of about 1 ps/mm. That means that while using an 800 nm laser and ZnTe, it is essential to have crystals that are sufficiently thinner than 1 mm or the GVM will cause the setup to be insensitive to higher THz frequencies.

Table 3: SRF Gun and Beam Parameter Values

Parameter	Value
Laser pulse length (rms)	2 ps
Repetition rate	100 kHz
Bunch charge	200 pC
Kinetic energy gun	3.5 MeV
Final beam energy	25.8 MeV

Table 3 lists the beam parameter values used in this experiment. The undulator was tuned to 1 THz, and the beam was guided through the whole beamline. A raw data of 2000 frames at 100 kHz repetition rate, as shown in Fig. 7 has been recorded at TELBE.

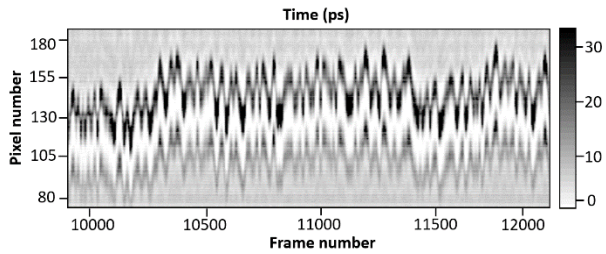

Figure 7: Raw data measurements recorded by the FPGA-Based DAQ System at TELBE.

This massive amount of raw data coming from the linear array detector is a significant challenge, and it requires the allocation of memory capacity and bandwidth, as well as the storage devices. The beam-time at TELBE lasts for an average of two weeks, with 24 hours of continuous measurement. From three to four experiments can be measured per hour, and this results in a raw data volume of hundreds of terabytes

CONCLUSION AND FUTURE WORK

The FPGA-Based DAQ system presented in this paper is for obtaining time-resolved measurements of various materials, utilizing THz at accelerator-based photon sources.

We evaluated the KALYPSO linear array detector as an approach to increase the performance of our DAQ system, which is limited by the speed of the imaging detector that supports a repetition rate of 100 kHz. As future work, the online sorting and binning of raw data shall be implemented inside the FPGA, as well as interfacing ultra-high speed ADC of 500 MSPS to improve the SNR of our experimental data.

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