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The Silicon Vertex Detector of the Belle II Experiment

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Belle II is an experiment taking data at an asymmetric energy e^+e^- collider, SuperKEKB, which is operated at the $\Upsilon(4S)$ resonance energy. The Belle II vertex detector is composed of an inner two-layer pixel detector and an outer four-layer double-sided strip detector (SVD). A deep knowledge of the system has been gained since the start of SVD operation in 2019 by assessing the high-quality and stable reconstruction performance of the detector, which includes that for hit efficiency and signal-to-noise ratio. The good cluster-position resolution is in reasonable agreement with the expectations. The Belle II event time obtained from central drift chamber is replaced with a new method to allow a faster calculation based on the SVD event time T_0 while achieving the same time resolution. Currently the average occupancy of the SVD is still less than 0.5%, which is well below the estimated limit where tracking performance deteriorates. The radiation damage effects on the sensor current and strip noise are measured, and we confirm this damage does not significantly degrade the SVD performance.

KEYWORDS: Silicon strip detector, Vertex detector, Tracking detector, Belle II, Radiation damage

1. Introduction

The Belle II experiment [1], which operates at the SuperKEKB collider [2] in Japan, aims to explore new physics beyond the Standard Model of particle physics based on B meson, tau lepton, and charm particle samples. SuperKEKB is operated at the $\Upsilon(4S)$ resonance energy with asymmetric beam energies of 7 GeV (e^-) and 4 GeV (e^+). The collected data since March 2019 is 424 fb^{-1}, and the achieved peak luminosity is 4.7 × 10^{34} cm^{-2} s^{-1}, which is the world record and more than twice that of KEKB, the predecessor accelerator of SuperKEKB. The target integrated luminosity is 50 ab^{-1}, which is 50 times larger than Belle, the predecessor experiment. The vertex detector (VXD) is composed of two layers of DEPFET pixel detector (PXD [3]) and four layers of double-sided silicon strip detector (DSSD), which is called the silicon vertex detector (SVD [4]). The major missions of the SVD are to extrapolate track trajectories from the drift chamber inward to the PXD, standalone tracking for low momentum tracks, precise vertexing of K_S^0, and particle identification using dE/dx. These proceedings describe the operation and performance of the SVD.

2. The Belle II Silicon Vertex Detector

The SVD consists of four detector layers of DSSDs at radii of 39, 80, 104, and 135 mm. Each detector layer is composed of mechanically and electrically independent sensor modules called ladders as depicted in Fig. 1 (top). Layers contain between seven and 16 ladders. Three types of DSSDs are used for the SVD, small rectangular ones for the innermost detector layer (layer 3), large rectangular ones in the barrel region and trapezoidal ones in slanted forward region for outer detector layers (layers 4 to 6) as illustrated in Fig. 1 (bottom). The details of the DSSDs are summarized in Table. 1. Each ladder has two to five DSSDs depending on the layer, and the total number of DSSDs is 172. DSSDs are made from an *N*-type bulk 6-inch wafer. The full depletion voltage ranges from 20 – 60 V, and we choose the operation voltage to be 100 V. To

provide 2D spatial information, AC coupled strips are designed on the u/P side in parallel to the beam axis, and other AC coupled strips are orthogonally designed on the v/N side that are transverse to the beam axis, which correspond to the r–φ and z axes in the cylindrical coordinate system, respectively.

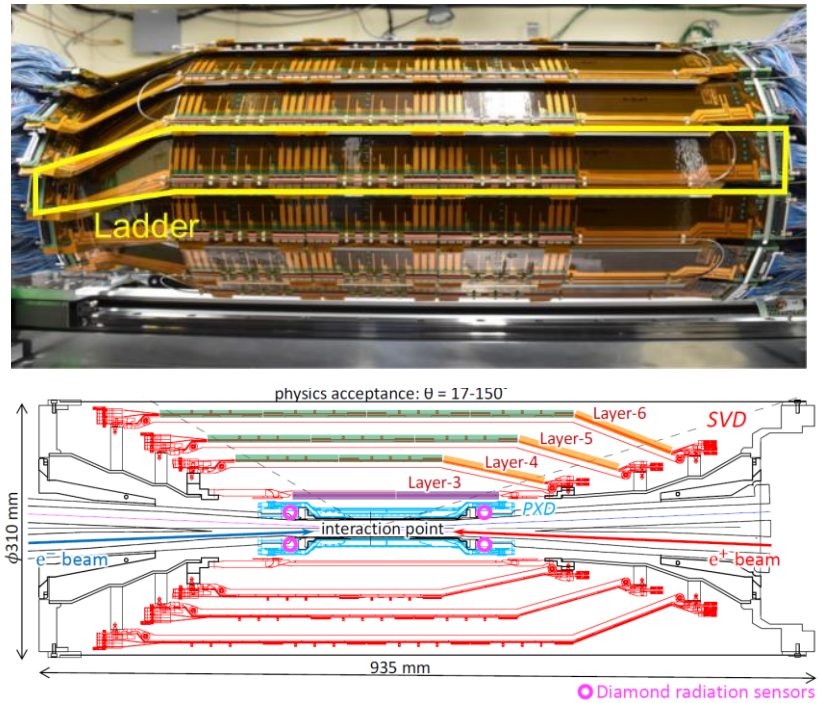

Fig. 1. Fully mounted half cylinder of the SVD (top): the yellow box indicates one ladder. Schematic cross-sectional view of the VXD (bottom): four red layers indicates the SVD, and two blue layers indicate the PXD. The magenta, green, and orange lines indicate small rectangular, large rectangular, and trapezoidal DSSDs for the SVD, respectively. Four diamond sensors (pink circles) are installed on IP beam pipe for radiation monitoring and beam abort system to protect the VXD from damaging beam losses [5].

Tab I. Details of the three types of DSSDs used in the SVD. All sensors have one intermediate floating strip between two readout strips.

	Small rectangular	Large rectangular	Trapezoidal
Sensor active area (mm^2)	122.90 × 38.55	122.90 × 57.52	122.76 × (38.42-57.59)
Number of p-strips	768	768	768
p-strip readout pitch (μm)	50	75	50-75
Number of n-strips	768	512	512
n-strip readout pitch (μm)	160	240	240
Thickness (μm)	320	320	300
Manufacturer	Hamamatsu	Hamamatsu	Micron

The APV25 chip [6] is used to read out signals from groups of 128 strips. The chip is characterized by 50 ns shaping time and radiation hardness up to 100 Mrad to cope with hit rates of 3 MHz/cm^2 and integrated radiation dose up to 0.2 Mrad/year, which meets the requirements for the innermost layer. In SVD, the AVP25 chip is operated with a clock frequency of 31.805 MHz that is only one eighth of the bunch-crossing frequency. Therefore, signal samples stored in the APV25 pipeline are not synchronous with the beam collisions. Thus the chip is operated in its 'multi-peak mode' that reads out multiple consecutive samples to reconstruct the signal-peak height and the hit time. In the present operation, six samples are readout upon the arrival of the Level-1 trigger. When the trigger timing is determined precisely, only three samples are enough to reconstruct the signal shape. So a mixed mode operation, using either three or six samples, is in preparation to reduce the readout time and data size. This change results in a shorter dead time, which will be important once higher luminosities will be delivered.

A novel chip-on-sensor concept, called Origami, is employed. The fast shaping is associated with higher susceptibility to noise, which mainly results from the capacitive load of the amplifier inputs. The APV25 chips are thinned down to 100 μm to reduce material budget and mounted on a flex circuit glued to the top-side of the DSSDs, so chips are placed as close to the sensor as possible, reducing the capacitive load. A flexible fan-out circuit is used to bring bottom-side signals of the DSSDs to the APV25 chips. The flexible circuit is glued to the DSSD bottom-side and bent to the top-side where the APV25 chips are mounted. Only central DSSDs of the layer 4 to 6 are assembled with the Origami concept, while forward and backward DSSDs of the layer 4 to 6, as well as layer 3 DSSDs, are read out by APV25 chips mounted on the end of the sensors instead of the Origami concept. In total ten APV25 chips are mounted for each DSSD. Dual-phase CO_2 at –20°C is used to cool down the APV25 chips. Thin stainless-steel pipes carry the CO_2; these pipes couple to the APV25 chips via thermal conductive rubber. In total, the SVD has approximately 1.2 m^2 of active area and 224,000 readout strips. The average material budget is about 0.7% of a radiation length per layer.

3. SVD Operation and Performance

The SVD has been showing reliable and smooth operation with no major issues since the start of the operation. So far, the total fraction of masked strips due to defects is less than 1%. We had only one temporarily disabled APV25 chip out of 1748 during spring 2019, which was fully recovered after cable reconnection. The hit efficiency is greater than 99% for all sensors. The temperature is stable and calibration constants (pedestals, noise, and gain) are within the expected range, despite radiation damage.

Figure 2 shows the comparisons between the 2020 and 2022 data samples of the signal cluster charge and signal-to-noise ratio (SNR). The signal cluster charge is normalized by the track path length in the silicon to correct for the track's incidence angle. The normalized cluster charge is in good agreement with expectations and similar in all sensors. The distribution of the normalized cluster charge in the u/P side is shown Fig. 2

(left). The most probable value (MPV) of the signal cluster charge agrees with expectation (~24000 e^-) from a minimum ionizing particle (MIP) within 15%, which is the uncertainty in the absolute APV25 gain calibration. The plots show good stability comparing 2020 and 2022 data samples. The cluster SNR is an important figure-of-merit (FOM) to be monitored and is defined as the total cluster charge divided by the quadrature sum of the noise from each strip in the cluster. All the 172 DSSDs have very good performance in the cluster SNR with the MPV ranging from 13 to 30 depending on the incident angle. Figure 2 (right) shows the good stability of the cluster SNR between 2020 and 2022 data samples, while small changes are visible due to an increased noise from the radiation damage (about 20-30% in the layer 3). The SNR is generally higher on the v/N side due to differences in strip length and capacitance. Furthermore, signal charge loss of the 10-30% on the v/N side is observed due to the large pitch and presence of the floating strips.

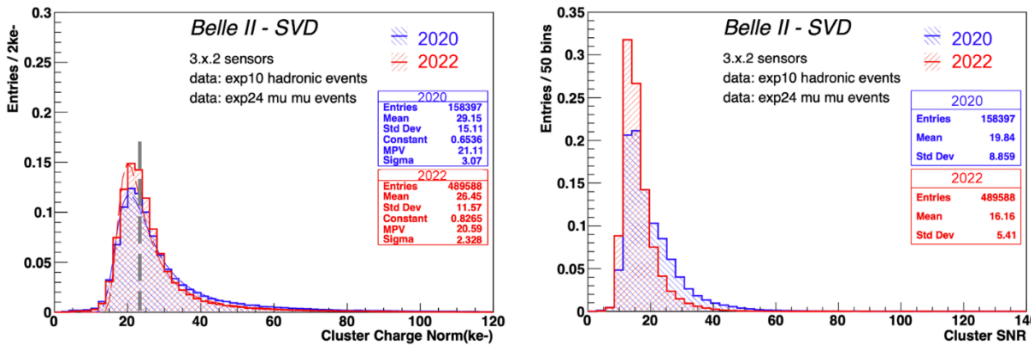

Fig. 2. Comparisons between 2020 and 2022 data samples of the signal cluster charge (left) and cluster SNR (right) in u/P side for one of the Layer 3 sensors. The vertical dashed line in the left plot shows the expected MPV (~24000 e-) for the MIP signal.

The measurement of the cluster position resolution is one of the main FOM for the SVD. We perform the measurement on a di-muon sample ($e^+e^- \to \mu^+\mu^-$) by using the residual of the cluster position with respect to the intercept of the unbiased track extrapolation after subtracting the effect of the track extrapolation uncertainty. The measured cluster position resolution, shown in Fig. 3, has the expected shape as a function of the track incident angle, with values of about 9 μm for the u/P side and 20 μm for the v/N side for the layer 3. Layers 4, 5, and 6 have a u/P-side resolution of 11 μm and v/N-side resolution of 25 μm. The measured resolution for normal incidence is also in fair agreement with the resolution derived from the sensor pitch with the floating strips under the assumption that at normal incidence only one strip is activated. As shown in Fig. 3, the cluster position shows good stability between 2020 and 2022 data samples.

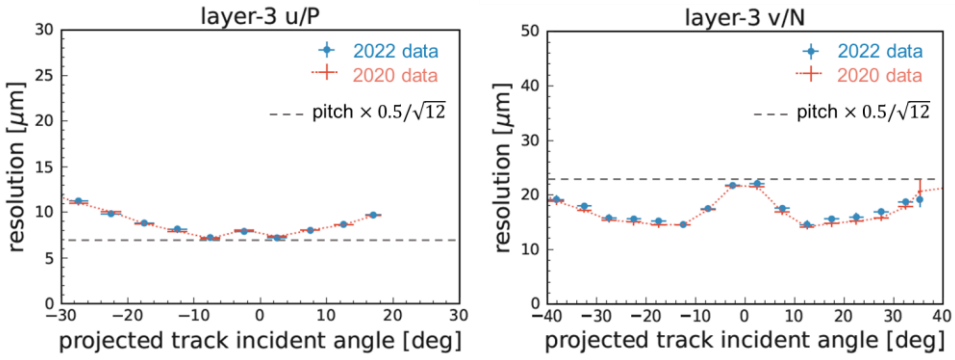

Fig. 3. Cluster position resolution as a function of the track incident angle for the u/P side (left) and v/N side (right) of the layer 3 for the comparison between 2020 and 2022 data.

The hit time resolutions are 2.9 ns for the u/P side and 2.4 ns for the v/N side [7], which are calibrated with respect to the event time provided by the Belle II central drift chamber (CDC). We observe that this good resolution can be used to remove 50% of off-time hit background, which is typically unassociated with the e^+e^- collisions, while keeping signal efficiency above 99% by means of a time cut. While not yet implemented, this will contribute to off-time hit rejection in the future high background running scenarios. The collision time (event T_0) can also be estimated using SVD cluster hit time, as explained in detail in reference [8]. The residuals of the SVD event T_0 compared to the CDC event T_0 for a hadronic data sample are shown in Fig. 4. From the width of the residual distribution, we subtract the known T_0 resolution of the CDC to find the SVD T_0 resolution of 0.8 ns. The computation speed of the SVD event T_0 is about 2000 times faster than the CDC one, which is favorable for fast event reconstruction in the high-level trigger. As a result, event T_0 will be computed using SVD in the future.

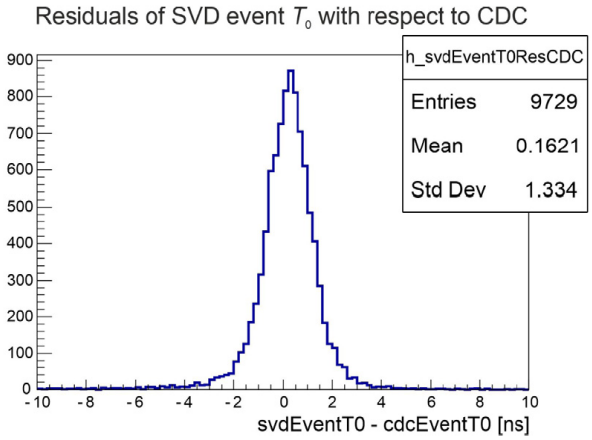

Fig. 4. Residual of SVD T_0 event and CDC T_0 for hadronic events.

4. Beam Background and Radiation Effects

The SVD tracking performance strongly depends on the SVD occupancy, which is correlated with the beam-background level. The current hit occupancy averaged over the layer 3 DSSDs is around 0.5%, which is below our allowed limit. We consider the occupancy limit to be 3% for the current operation from performance studies. It could be relaxed to about 5% by using the hit-time selection to reject background. The expected average hit occupancy at the target luminosity of 6×10^{35} cm^{-2} s^{-1} is about 3% in the layer 3 according to beam-background projections, which are based on scaling with a data-simulation ratio. But this extrapolation is still affected by large uncertainties on the long-term background extrapolation, computed assuming optimal collimator settings, and an even larger unknown from possible machine design changes required to reach the target luminosity. Due to small safety factor and large uncertainties, the VXD upgrade is motivated to improve the tolerance to the hit rates. The technology assessment is currently ongoing.

The integrated dose on the SVD sensors is estimated using the correlation between SVD occupancy and diamond dose, which is measured by diamond sensors mounted on and around VXD [5]. These estimates are based on several assumptions with approximately 50% uncertainty. The total integrated dose on layer 3 mid plane, which is closest to the interaction region, is less than 70 krad since the start of the data taking as shown in Fig. 5. This corresponds to an equivalent 1-MeV neutron fluence of 1.6×10^{11} n_{eq}/cm^2, based on the ratio of neutron fluence to radiation dose of 2.3×10^9 $n_{eq}/cm^2/krad$, taken from MC simulation. The effects of radiation damage are constantly monitored measuring the changes in the leakage current, strip noise, and depletion voltage as a function of the integrated dose. So far, there is no degradation of the SVD performance, while we observed a correlation between the integrated dose and observable effects induced by radiation damage.

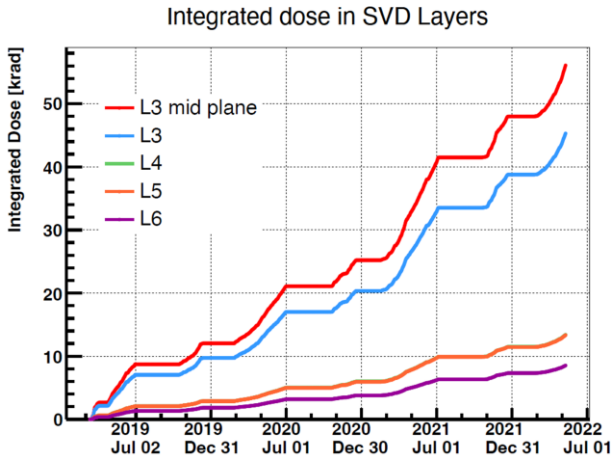

Fig. 5. The estimated integrated dose received by SVD layers.

Increase of measured leakage current due to radiation damage is correlated with the radiation dose based on the NIEL model [9]. Figure 6 shows the linear dependance of one of the layer 3 sensors, and similar linear dependencies are observed for all sensors. The correlation coefficients show the same order of magnitude as BaBar measurement (1 μA/cm^2/Mrad at 20°C) [10]. Because of the fast-shaping time of the APV25 chip, the expected contribution for the strip noise by increased leakage current is very small with respect to the contribution by the main capacitance. Therefore, the SVD performance will not be degraded by the radiation damage even with an integrated dose of up to 6 Mrad, which is three times greater than the expected dose during ten-year operation.

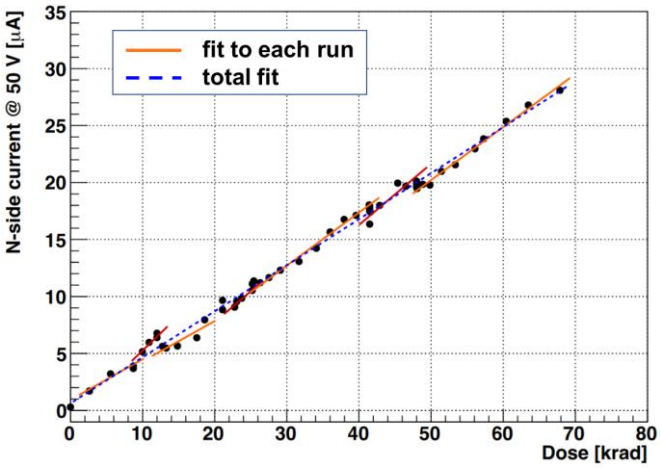

Fig. 6. Linear correlation between integrated dose and leakage current in the one of the layer 3 sensors.

This noise increase is due to the higher interstrip capacitance produced by the increase of the oxide fixed charge density at the Si-SiO2 interface, related to surface radiation damage. The increment in the oxide fixed charge is expected to saturate. The increase in interstrip capacitance is also saturating as a function of the oxide fixed charge, especially on the n/V side, with a non linear dependence. We then expect saturation in the associated noise increase too; this saturation was already reached at about 10 krad on the n/V side and at about 40 krad on the u/P side.

The radiation damage of the silicon sensor is also monitored by measuring the depletion voltage. The full depletion voltage is obtained by scanning the noise as a function of the applied bias voltage. No change in the full depletion voltage is observed after the irradiation, which is consistent with the current integrated dose.

5. Summary

The SVD has been operated with excellent performance since its start in 2019. The cluster charge, cluster signal-to-noise ratio, and position resolution show good stability between 2020 and 2022 data samples. The total integrated dose on the layer 3 sensor that

is the most irradiated is estimated to be less than 70 krad. The effects of radiation damage are observed on the leakage current, strip noise, and depletion voltage, but the SVD performance does not degrade.

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