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# Development of cryogenic CMOS Readout ASICs for the Point-Contact HPGe Detectors for Dark Matter Search and Neutrino Experiments

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**Abstract.** The paper presents the developments of two cryogenic readout ASICs for the point-contact HPGe detectors for dark matter search and neutrino experiments. Extremely low noise readout electronics were demanded and the capability of working at cryogenic temperatures may bring great advantages. The first ASIC was a monolithic CMOS charge sensitive preamplifier with its noise optimized for  $\sim 1$  pF input capacitance. The second ASIC was a waveform recorder based on switched capacitor array. These two ASICs were fabricated in CMOS 350 nm and 180 nm processes respectively. The prototype chips were tested and showed promising results. Both ASICs worked well at low temperature. The preamplifier had achieved ENC of 10.3 electrons with 0.7 pF input capacitance and the SCA chip could run at 9 bit effective resolution and 25 MSPS sampling rate.

## 1. Introduction

The point-contact high purity germanium detector (PC-HPGe) technology has been successfully demonstrated for dark matter search and neutrino-less double beta decay experiments [1-4]. Benefit from the low capacitance ( $\sim 1$  pF) of the small point contact, the equivalent noise charge (ENC) for PC-HPGe can be lowered down to several electrons. Hence low threshold and high energy resolution can be achieved, which are of great importance to the low energy limit and sensitivity for rare event detection.

However extremely low noise readout electronics are demanded. Conventionally JFETs (Junction Field Effect Transistors) are used due to their lower flicker noise [5,6]. As the detector capacitance decreases down to  $\sim 1$  pF the contribution from the flicker noise becomes insignificant. In addition JFETs cannot be mounted very close to the detectors since their optimum working temperature is usually  $\sim 120$  K. Hence the parasitic capacitance of the interconnection cannot be minimized. On the contrary CMOS (Complementary Metal Oxide Semiconductor) transistors can work at 77 K and can be more easily custom designed with highly integration. Several low noise CMOS preamplifier ASICs (Application Specific Integrated Circuits) have been reported both for silicon drift detectors with very small capacitance of 10-100 fF [7,8] and for HPGe detectors with detector capacitance of  $\sim 10$  pF [9,10]. The noise of the preamplifiers for silicon drift detectors could be very low ( $< 10$  e) but they were not optimized for  $\sim 1$  pF detector capacitance. Our previously designed CMOS preamplifier has achieved energy resolution of 512 eV FWHM at 59.5 keV with a 3 pF PC-HPGe detector [11]. It



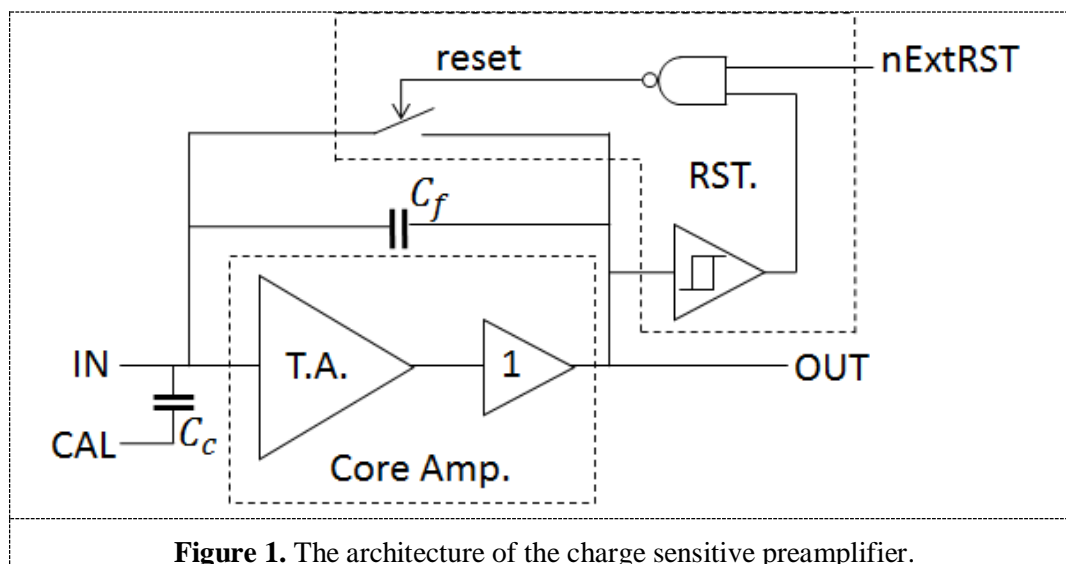
turned out to be very promising and a newly developed ASIC dedicated for smaller capacitance and its test results will be present in this paper.

On the other hand, pulse shape analysis is essential for HPGe detector signal processing [12] and the waveform of the preamplifier output needs to be sampled and stored for further digital signal processing. In current dark matter and neutrino experiments the preamplifier outputs were sent out from the cryostat through 10-meter-long cables and the waveforms were sampled and digitized by room-temperature fast ADCs. In order to reduce the number of the cables as well as cryogenic feedthroughs, a multi-channel SCA (Switched Capacitor Array) ASIC was proposed here to record the signal waveforms of multiple detectors in an analogue way and then to send them out in serial by multiplexing. The SCA structure was adopted due to its simplicity, which in principle could easily work at 77K. A SCA ASIC named CASCA [13] originally developed for gas detectors at room temperature was used for feasibility study. The details of the circuit design and the test results under cryogenic environment will be described in the following sections.

## 2. Circuit design

### 2.1. The CMOS charge sensitive preamplifier ASIC

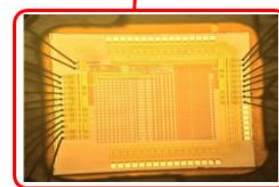
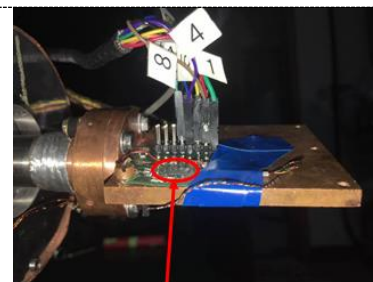
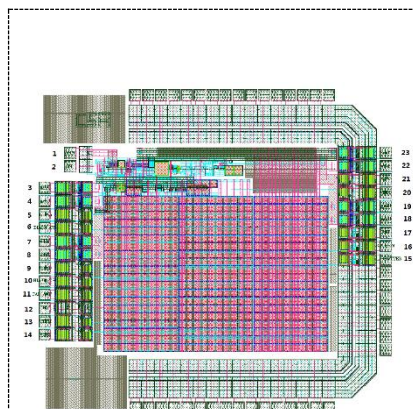
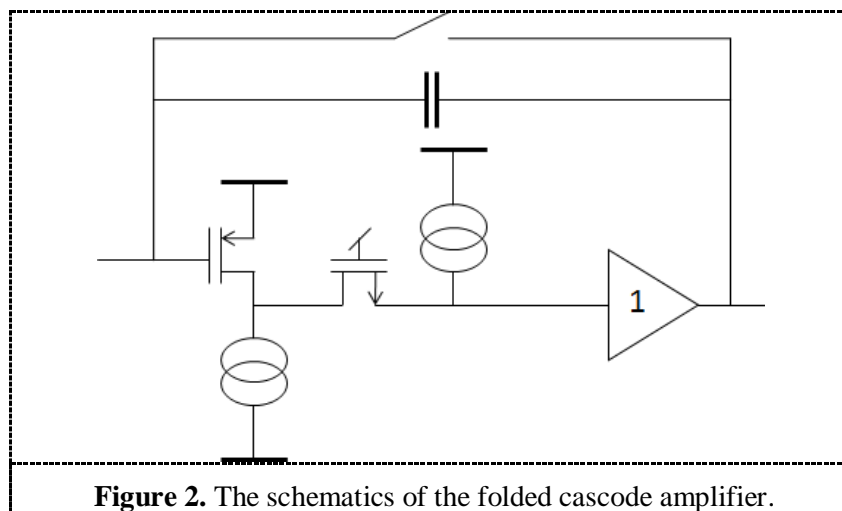
The charge sensitive preamplifier consisted of a core amplifier, providing effective gain and bandwidth, a feedback capacitor and the reset circuits, as shown in Fig.1. The core amplifier has a transconductance amplifier stage and an output stage, which is able to drive ~1 m long cable. The feedback capacitor was 50 fF. A reset switch was used since it had almost zero noise contribution when it was open. The pulse reset signal was generated either by the on-chip window discriminators or externally. A calibration capacitor of 50 fF was also integrated. The chip was implemented in a CMOS 350 nm process. All the circuit simulation was done using the transistor model provided by the manufacturer, which was not valid for such low temperature down to 77 K. Hence the bias currents of all circuit branches can be adjusted through an external resistor.



**2.1.1. The core amplifier.** A traditional folded cascode amplifier structure was adopted for the transconductance amplifier, as shown in Fig.2. A PMOS input transistor was chosen for its lower flicker noise coefficient. The size of the transistor ( $600\ \mu\text{m}/0.35\ \mu\text{m}$ ) was optimized for 1 pF input capacitance and its bias current was 0.8 mA at 77 K. The output stage was designed to drive large negative signals without slew rate limit [14]. The total consumed current of the core amplifier was 2.8 mA.

*2.1.2. The reset circuits.* The minimum sized NMOS and PMOS transistors were used in parallel for the reset switches. Dummy transistors were evenly placed to minimize the charge injection. A resistor was also put in series to the switch transistors to increase the stability of the amplifier and hence to suppress the oscillation during the reset. Two discriminators were used to set the upper and lower thresholds respectively. A pulse reset signal with  $\sim 100$  ns fixed duration was asserted automatically when the output of the preamplifier was out of the range defined by the two thresholds, which can be adjusted externally.

*2.1.3. The chip layout and the test PCB.* The layout of the preamplifier is shown in Fig.3 and the size of the chip is 2.5 mm x 2.3 mm. A test PCB was designed with the die wire bonded on it. The test PCB was mounted on the cold finger of the cryostat, as shown in Fig.4.



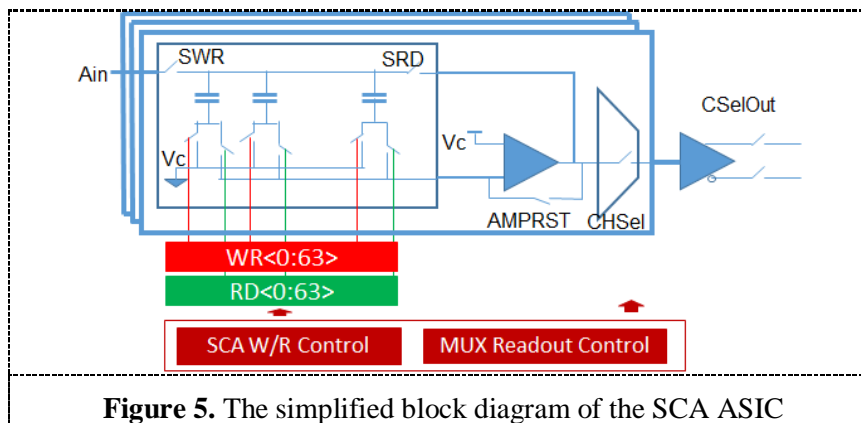
**Figure 4.** The test PCB mounted on the cold finger of the cryostat.

## *2.2. The waveform sampling ASIC based on switched capacitor array*

The simplified block diagram of the SCA ASIC was shown in Fig.5. It consisted of 32 channels of switched capacitor array, a readout amplifier for each channel, a 32:1 multiplexer and a differential output driver. The control logic was also integrated. The chip was fabricated in a CMOS 180 nm

process and was originally developed for time projection chamber gas detectors. Only a short description of working principle and circuits will be introduced below and the detailed circuit design can be found in Ref.13.

During the sampling phase, the write switch  $WR$  of each capacitor was turned on for one clock period in sequence and the input voltage would be stored on the corresponding capacitor. If there was no signal detected, the input signal was continuously sampled on the capacitor cells in a cycling way. There were 64 capacitor cells in total for each channel. Once a trigger asserted, the sampled voltage on the capacitors would be frozen and waited for readout. The readout switch  $RD$  could be selected by the 6 bit address bus. During the readout phase, the selected sampling capacitor was connected as the feedback capacitor of the readout amplifier. The voltage stored was then present at the output of the amplifier, which was sent out channel by channel by multiplexing and was converted to differential current signals. The chip was designed for working at room temperature but it might work at 77 K due to that there were no complex amplifiers and all the bias currents could be externally adjusted.

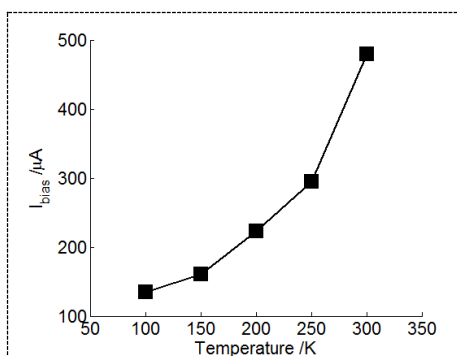


### 3. Test results

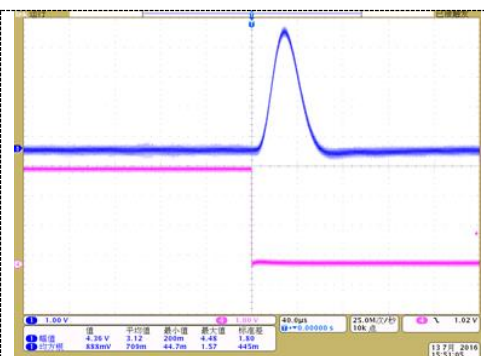
The performance of these two ASICs under cryogenic temperature will be described below.

#### 3.1. The charge sensitive preamplifier

The external bias resistor was set to  $520 \Omega$  and its bias current  $I_{\text{bias}}$  was measured at different temperatures, as shown in Fig.6. The bias currents of all circuit branches in the core amplifier were proportional to the master bias  $I_{\text{bias}}$ . The master bias current had a significant change from  $480 \mu\text{A}$  at  $300 \text{ K}$  to  $135 \mu\text{A}$  at  $100 \text{ K}$  and it was estimate to be about  $100 \mu\text{A}$  at  $77 \text{ K}$ , which was very close to the simulation results.

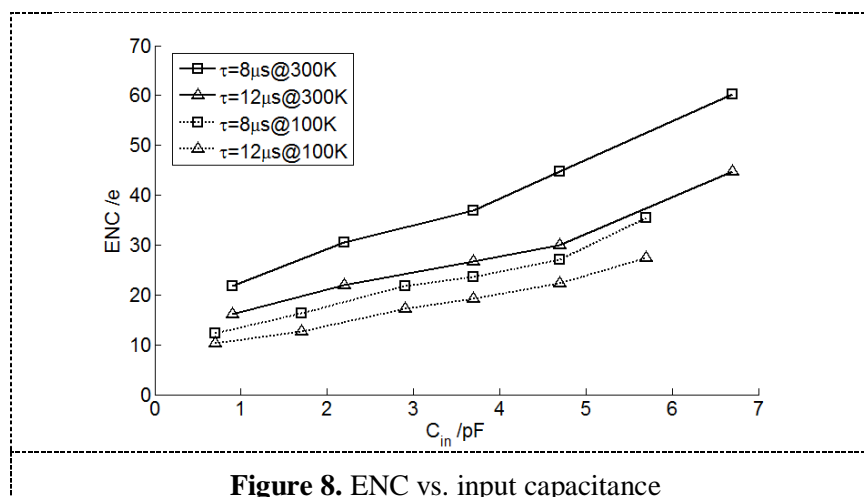


**Figure 6.** The temperature dependence of the bias current.



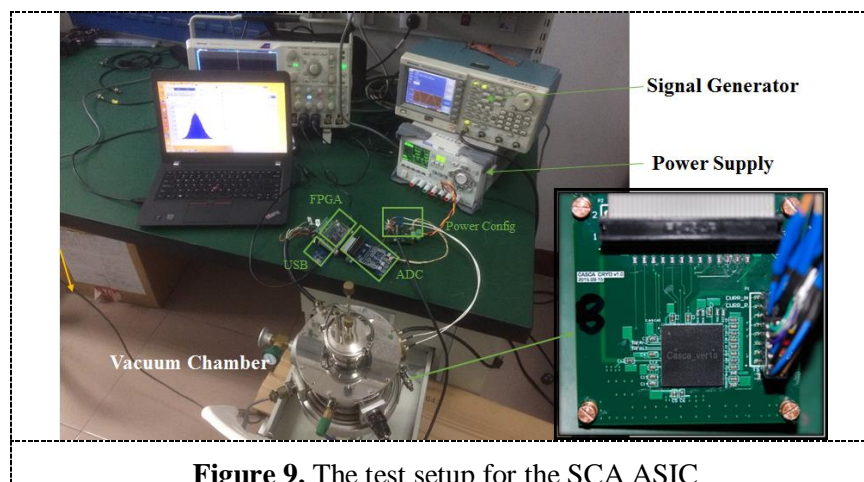
**Figure 7.** The transient signals. Pink: input step pulse; Blue: shaper output

The preamplifier was tested by injecting a step pulse through a calibration capacitor, mimicking the detector signal. The injected signal charge can be calculated by  $C_{cal} \cdot \Delta V$ , where  $C_{cal}$  is the calibration capacitance and  $\Delta V$  is the amplitude of the step pulse. The output of the preamplifier was sent to a commercial spectroscopy amplifier (Canberra 2022) for shaping and noise filtering. The transient signal waveforms were shown in Fig.7. The charge gain  $G = V_{out}/Q_{in}$  of the amplifiers was then derived. The r.m.s standard deviation of the output baseline  $\sigma_{vo}$  was measured by the oscilloscope and the ENC was calculated by  $\sigma_{vo}/G$ . ENC was dependent on the input capacitance and the shaping time and the curves of ENC vs. input capacitance at different shaping time at 300 K and 100 K were shown in Fig.8. The bias currents at different temperature were set to about the same ( $\sim 100 \mu\text{A}$ ). Due to the test setup the temperatures for the noise measurement at 100 K were actually in the range of 90-100 K. The minimum of 10.3 electrons was achieved with 0.7 pF input capacitance at 12  $\mu\text{s}$  shaping time at 100 K.

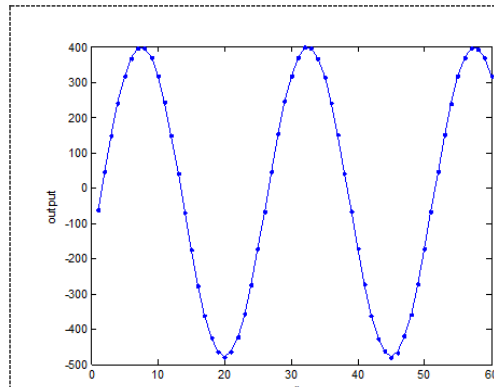


### 3.2. The SCA

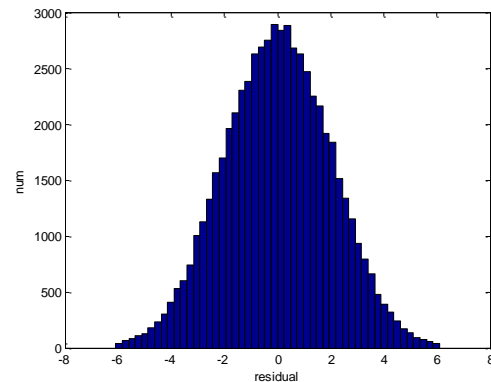
The test setup for the SCA ASIC was shown in Fig.9. The SCA ASIC was put on the cold finger of the cryostat vacuum chamber. The power supply, the output and the control signals including clock and trigger were connected out through  $\sim 1$  m long cables. The control signals were generated by a FPGA evaluation board and the analog output was digitized by an ADC board. The data was acquired through the USB interface to the computer.



A standard dynamic ADC test procedure was conducted to evaluate the SCA waveform sampling performance. A sine signal with 200 kHz frequency and almost full amplitude ( $\sim 1$  V) was sampled and readout by the SCA ASIC. The collected samples were fitted with the sinusoidal function (Fig.10) and then the resolution was estimated from the standard deviation of the residual. An example of residual distribution was shown in Fig.11.



**Figure 10.** Fitting the readout SCA samples with sine waveform.



**Figure 11.** The distribution of the residual.

The dynamic tests were done with sampling frequency up to 25 MSPS at 300 K and 120 K respectively, which was limited by the test setup. In order to adjust the bias current to be the same ( $\sim 50$   $\mu$ A), the external resistor had to be changed from 1.4 k $\Omega$  at 300 K to 118.2  $\Omega$  at 120 K. The r.m.s. standard deviations were measured to be 2.2 mV and 1.9 mV at 300 K and 120 K, corresponding to 8.8 bit and 9 bit effective resolution.

#### 4. Summary

Two ASICs have been developed for PC-HPGe detectors for dark matter search and neutrino experiments. Both ASICs worked well at cryogenic temperature. The CMOS charge sensitive preamplifier had achieved ENC of 10.3 electrons with 0.7 pF input capacitance and the SCA ASIC could run at 9 bit effective resolution and 25 MSPS sampling rate. All these prototype chips cannot fully satisfy the requirements for the experiments. More tests and ASIC developments are undergoing for better noise and resolution performances in the near future.

Our experience with CMOS 350 nm and 180 nm processes showed that simple cascode and operational amplifiers could work easily at 77 K with external bias strategy. However it may need more accurate low temperature transistor model for further optimization.

#### Acknowledgments

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