Total ionizing dose radiation hardness of the ATLAS MDT-ASD and the HP-Agilent 0.5 μm CMOS process

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Abstract

A total ionizing dose (TID) test of the MDT-ASD, the ATLAS MDT front-end chip [12][13] has been performed at the Harvard Cyclotron Lab. The MDT-ASD is an 8-channel drift tube read-out ASIC fabricated in a commercial 0.5μm CMOS process (AMOS14TB). The accumulated TID at the end of the test was 300 krad, delivered by 160 MeV protons at a rate of approximately 70 rad/sec. All 10 irradiated chips retained their full functionality and performance and showed only minuscule and completely insignificant changes in device parameters. As the total accumulated dose is substantially higher than the relevant ATLAS Radiation Tolerance Criteria (RTC_{tid}) [3], the results of this test indicate that MDT-ASD meets the ATLAS TID radiation hardness requirements. In addition, the results of this test correspond well with results of a 30 keV gamma TID irradiation test performed by us on an earlier prototype at the CERN x-ray facility as well as with results of other irradiation test on this process found in literature.

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1. Radiation environment

The MDT-ASD will reside and work in the Muon Spectrometer part of the ATLAS detector and thus will be exposed to the LHC radiation environment. The worst case location for the ATLAS MDT read-out electronics in terms of radiation levels is the middle end-cap (End-cap 2) close to the beam pipe. The Simulated Radiation Levels (SRL_{tid}) and Safety Factors (SF_{tid}) and the resulting Radiation Tolerance Criteria (RTC_{tid}) are defined and issued by the ATLAS Radiation Hardness Assurance Working Group (RHA-WG) [1]. The relevant numbers for the Mezzanine board on which the MDT-ASD resides are given for the End-cap 2 innermost location in Table 1.

Table 1. Excerpt from the ATLAS official Radiation Tolerance Criteria for MDT

Tech	**Simulated Radiation Level**			**Safety Factors**			**Radiation Tolerance Criteria**	
	SRL_{tid} [1]	SRL_{niel}	SRL_{see}	SF_{sim}	SF_{ldr}	SF_{lot}	RTC_{tid} [2]	RTC_{niel}
				tid /niel-see	tid/niel-see	presel/qual	presel/qual	presel/qual
ASIC	62.4	1.63E12	2.67E10	3.5 / 5	5 / 1	2 / 1	2184 / 1092	1.63E13 / 0.8E13

2. ASIC fabrication process

The MDT-ASD is a full-custom mixed signal ASIC which has been designed for and fabricated in a commercial 0.5 μm N-well triple-metal CMOS process named AMOS14TB. The foundry is HP-Agilent. The process has a linear capacitor option consisting of polysilicon over an active N+ diffusion in an N-well (2250 aF/μm²). The process is silicided yielding very low polysilicon and diffusion resistivities. There is a "silicide" block layer available which allows exclusion of silicide over polysilicon but not over diffusion. This feature is used for polysilicon resistors. The nominal operating voltage for this process is 3.3 V.

The MDT-ASD is composed of full-custom analog blocks as well as library standard cells and pads. The design is based on MOSIS scalable CMOS (SCMOS) design rules [11]. These rules are generally more conservative than the process-specific vendor design rules. The minimum well-to-active spacing in MDT-ASD is 3 μm, which results in an increased latchup threshold (see Appendix). No further special radiation hardness improving layout techniques have been employed in the design.

[1] Unit for SRL_{tid} and RTC_{tid}: Gray (Gy) / 10 years. 1 Gy = 100 rad

3. Irradiation facility

The radiation test was done at the Harvard Cyclotron Laboratory at Harvard University, Cambridge, MA. The synchrocyclotron produces an up to 160 MeV proton beam with variable fluence up to 3×10^{10} protons/sec. The beam diameter can be adjusted from 0.1 cm to 30 cm. The calibration system uses a "Faraday cup" and a Keithley electrometer.

For this irradiation test, the beam was set up to deliver $4.41\cdot10^{8}$ protons/cm^2 per Monitor Unit (MU). The calculation of the ionizing dose in Silicon yields 30.21 rad(Si)/MU. A rate of approximately 2.38 MU/sec resulted in a dose rate of ~ 70 rad/sec. Details of the beam calibration and the Si-dose calculation can be inquired from [1].

4. Test setup and online monitoring

The DAQ and monitoring setup allows to run Single Event Effect (SEE) and TID tests simultaneously. The system monitors DC parameters like the on-chip bias generator voltages, pre-amp input levels and LVDS output levels. Also the power consumption of the DUT is monitored to catch Single Event Latchups (SEL). All values are displayed on screen for immediate observation and are also recorded with the proper timing information for offline analysis. For Single Event Upset (SEU) monitoring the system periodically reads all on-chip register contents, compares them to some initial state and re-writes the registers. Every bit flip is recorded and time stamped. The period of this read-write cycle is approximately 3 seconds.

During irradiation the DUT is biased and run under its nominal operating conditions, however there are no signals passed through the analog amplifier chain. The digital part is operated as stated in the last paragraph.

A list of all parameters monitored and recorded during the irradiation test is given below in Table 2.

Table 2. Online monitored DC parameters

Parameter	Name	Comment
Pre-amp bias voltages	Vb1, Vb2, Vb3, Vb4	on-chip bias generator
Pre-amp input DC levels	InA0, InB0, InA1, InB1	2 ch (0, 1) active and dummy input
LVDS output levels	OutA0, OutB0, OutA2, OutB2	2 ch (0, 2) both LVDS polarities
Power consumption	VddASD, VddIn	voltage drop across 10 Ohm sense
Register contents (SEE)	S1 - S106	shift and shadow register contents

5. Analog performance evaluation

All DUTs (10) have been characterized in terms of analog performance parameters before irradiation. To be able to asses the effect of TID radiation on the DUTs, these parameters were compared to measurements on the devices before irradiation as well as to the parameters of a non-irradiated set of devices (5).

The MDT-ASD measures drift time and charge of Muon signals in drift tubes. Hence the relevant parameters are peaking time, timing jitter (noise) and delay of the shaper pulse as well as width and jitter (noise) of the pulse-width encoded Wilkinson ADC output pulse. Radiation induced amplifier gain decrease and noise increase are also meaningful parameters for the estimation of radiation effects in electronic circuits.

6. Results

6.1 DC parameters

The observed changes in DC parameters appeared very similar on all of 10 irradiated devices so only the averages across all DUTs are plotted below (Figure 1). After 300 krad of TID the pre-amp bias voltages dropped between 2% (Vb4) and 5% (Vb3), the pre-amp input DC levels by 3% - 4%. The DC levels of the LVDS output drivers dropped 2% - 3%. The error bars of plots a) and c) of are too small to appear on this scale.

There was no measurable increase in power consumption thus we conclude that no noticeable radiation induced leakage current increase occurred (Figure 1.d). The data of DUTs 1 - 4 were not included in this plot because their irradiation was interrupted and continued the next day, resulting in a discontinuity due to slight changes in supply voltage.

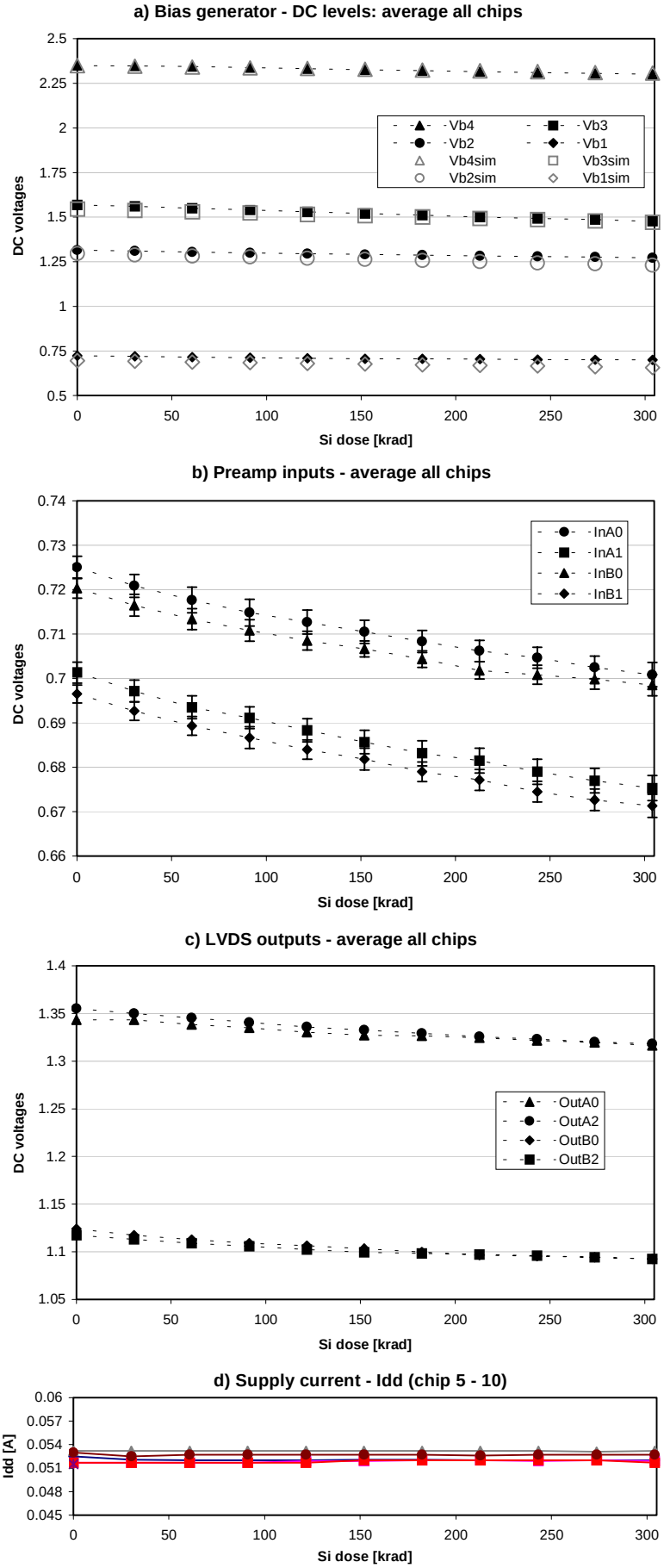

Figure 1. DC parameters vs. TID Si [krad]

6.2 Simulation of device parameters

The shift in threshold voltage of the AMOS14TB MOS transistors as measured by Osborn et. al. [10] could be verified through simulation. The VbXsim data points of the DC bias generator in Figure 1.a) were simulated with Pspice assuming that the threshold voltage of both NMOS and CMOS transistors had to first approximation linearly decreased by ~40 mV at 300 krad TID(Si) as stated in [10] (see also section 11.1).

6.3 Performance parameters

Comparison of measurement data from the 10 irradiated and the 5 non-irradiated DUTs yield the results of Table 3 and Figure 2. The data in the plots are averaged across the respective group of devices. The numbers of Table 3, column 3 in addition are averaged over the input charge range. The "System context/comment"-column correlates the data to the application parameters. It is apparent that the radiation induced performance deterioration is negligible .

Table 3. Performance parameter changes after 300 krad TID

Parameter	MAX change	AVG(input charge) change	System context/comment
Wilkinson pulse width	± 0	± 0	–
Wilkinson width jitter	+ 146 ps r.m.s.	+ 93 ps r.m.s.	< 0.1% of typical pulse
RMS timing error	+ 45 ps r.m.s.	+ 28 ps r.m.s.	3.5% of TDC bin width
Amplifier gain	– 26 mV peak	– 15 mV peak	minus 5%
RMS noise	± 0	± 0	–
Shaper peaking time	– 161 ps	– 153 ps	minus 0.1%

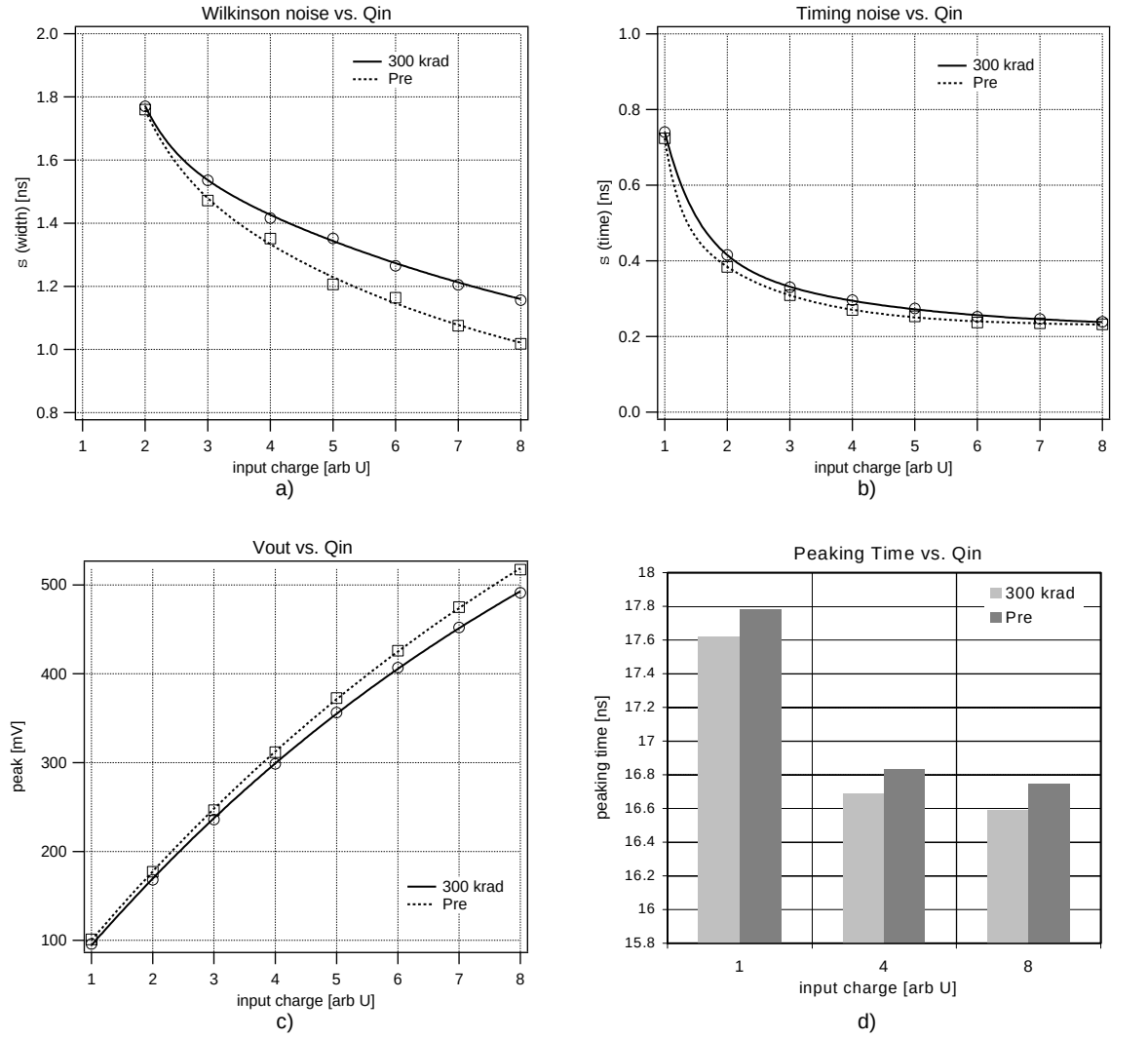

Figure 2. Performance parameters pre and post irradiation (300 krad$_{Si}$ TID); fit functions double-exponential.

7. Comparison with gamma irradiation TID results

An earlier prototype of the MDT-ASD has been irradiated at the CERN X-ray facility. The Seifert X-ray source delivers up to 30 keV gammas at variable dose rate. The TID of 1 Mrad was accumulated in several steps, 10k, 50k, 100k, 300k, 1Mrad, with a dose rate of ~ 170 rad/sec. The temperature during irradiation was controlled (const. 21°C). Electrical measurements were conducted immediately (<15 min) after reaching each radiation step. The DUT was biased at nominal conditions; no signals were passed through the amplifier chains.

The results of this gamma irradiation test are in very good agreement with the results from the cyclotron proton irradiation. Table 4 summarizes the results for both tests, Figure 3 shows sample plots of the two radiation tests (all fit function double-exponential).

Table 4. Comparison gamma and proton irradiation

Parameter	Gamma irradiation (300 krad)	Proton irradiation (300 krad)
Wilkinson width jitter increase	118 ps	91 ps
RMS timing error increase	25 ps	28 ps
Amplifier gain decrease	15.4 mV	15.3 mV

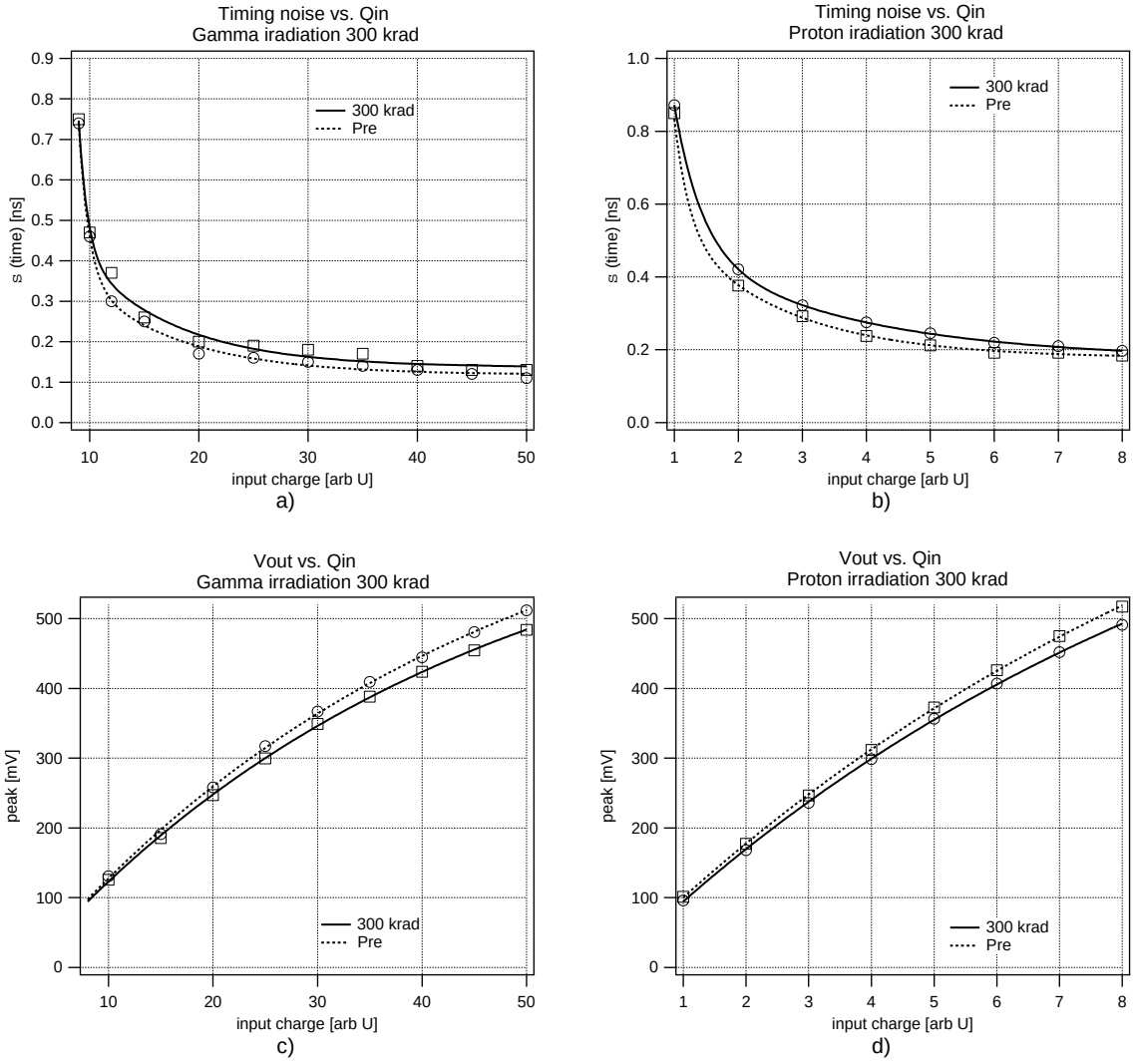

Figure 3. Comparison - gamma and proton irradiation

8. Gamma irradiation effects vs. TID

The plots of Figure 4 and Figure 5 show results of measurements taken after each step of the gamma irradiation described in the previous section (7).
Figure 4 a) shows the RMS timing error, i.e. the sigma of a number of timing measurements of identical input pulses, as a function of input charge before and after 1 Mrad of TID; the fit function is double-exponential. Figure 4 b) shows the averaged (across the input charge range) RMS timing error before and after each irradiation step with an exponential fit.

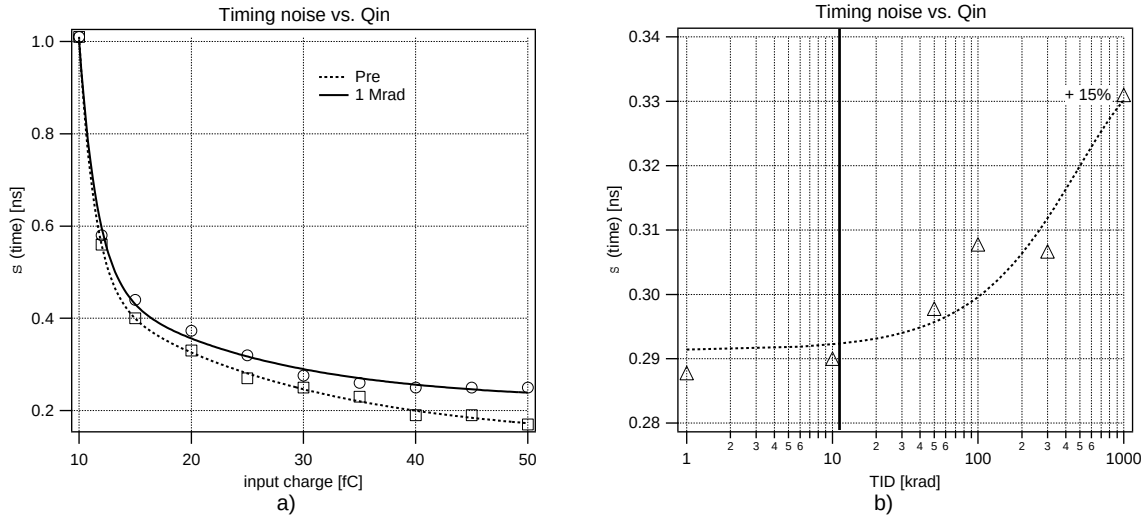

Figure 4. Gamma irradiation - RMS timing error before and after 1 Mrad (a), average vs. dose (b)

Figure 5 a) shows the pulse peak voltage at the analog output (shaper pulse at pad driver) as a function of the input charge after each irradiation step. Figure 5 b) shows the gain of the analog signal chain versus dose normalized to pre-rad values (100 %) with a linear fit.

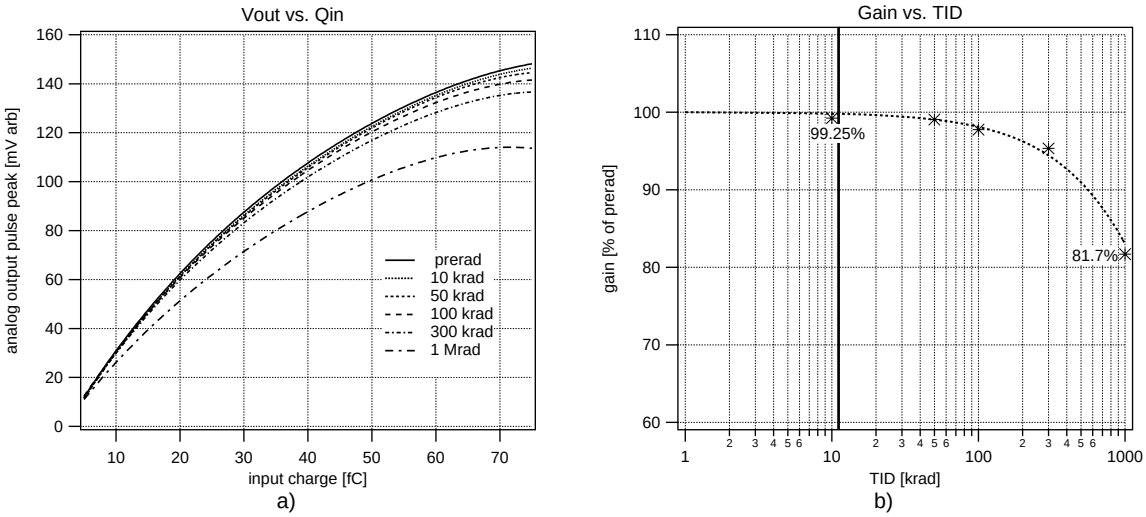

Figure 5. Gamma irradiation - amplifier Vout vs. input charge for each step (a) and average gain vs. dose (b)

Summary of the gamma irradiation results:

- The averaged RMS timing error increases by 7 % after 300 krad TID.
- At 110 krad (1100 Gy), the ATLAS Radiation Tolerance Criterion (RTC_{tid}) for ASIC qualification, the RMS timing error increase is ~ 2%.
- The voltage gain of the complete analog signal chain - pre-amp, gain stage (differential amplifier), shaper (two differential amplifiers), analog pad driver - drops by 5 % after 300 krad TID.
- At 110 krad, the gain drop of the full chain is of the order of 2 %.
- The chip is fully functional after 1 Mrad (>1600 years of ATLAS operation at worst location - Simulated Radiation Level SRL_{tid}) with a gain drop of 18 % and a RMS timing error increase of 15 %.

9. Conclusion

We have performed a total ionizing dose (TID) qualification test of the MDT-ASD. The accumulated TID at the end of the test was 300 krad, delivered by 160 MeV protons at a rate of approximately 70 rad/sec. All 10 irradiated chips retained their full functionality and performance and showed only minuscule and completely insignificant changes in device parameters. As the total accumulated dose is substantially higher than the relevant ATLAS Radiation Tolerance Criteria (RTC_{tid}) [3], the results of this test indicate that MDT-ASD meets the ATLAS TID radiation hardness requirements.

In addition, the results of the test correspond very well with results of a 30 keV gamma TID irradiation test performed by us on the previous MDT-ASD prototype at the CERN x-ray facility as well as with results of other irradiation test on the HP-Agilent AMOS14TB process found in literature.

10. References

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11. Appendix: Additional radiation results for the AMOS14TB process

11.1 Aerospace Corp. TID tests on commercial CMOS processes [10]

Total dose irradiation was performed on AMOS14TB minimum geometry n-channel and p-channel MOSFETS and a 49-stage ring oscillator, using a ^{60}Co gamma source at 50 rad (Si)/sec. The accumulated TID reached 300 krad (Si).

Quote: Good TID radiation tolerance is achieved in the HP 0.5 μm process. The average change in threshold voltage at 100 krad is less than 40 mV for the n-channel and less than 20 mV for the p-channel devices. The normalized change in gate delay at 300 krad is of the order of 1%.

Table 5. HP AMOS14TB total ionizing dose (TID) results

Dose	Vth NMOS	Vth PMOS	Gate delay
100 krad	-40 mV	18 mV	+0.6%
300 krad	-38 mV	43 mV	+1.0%
Post-anneal	0 mV	28 mV	+1.6%

No special radiation-tolerant layout techniques were applied. The HP 0.5μm CMOS process is recommended to be a candidate for (space) missions with a total dose requirement of 100 krad [10].

11.2 ATLAS CSC ASD chip - ^{60}Co irradiation, BNL [8]

The CSC-ASD designed at BNL uses the HP 0.5 μm CMOS process. A ^{60}Co-irradiation was done up to a total dose of 1.055 Mrad (Si).

Summary of the resulting data on power supply current, amplifier gain, noise and time-domain wave-form changes:

a) No radiation induced leakage current.
b) Gain drop: 4.06 -> 3.99 mV/fC (- 1.5 %)
c) Noise increase: 1750 -> 2050 rms e^- ENC (+ 17 %)
d) No shaper pulse shape change

11.3 Aerospace Corp. Single Event Latchup (SEL) tests on commercial CMOS processes [9]

Single event latchup testing was performed with both a single shot laser system and with accelerated heavy ions ranging in effective LET from 5.6 MeV/mg/cm^2 to greater than 120 MeV/mg/cm^2. Figure 6 indicates that the HP 0.5μm devices range in latchup threshold from 63 LET for a 1.5 μm well-to-active spacing to greater 100 LET for a 4.5 μm well-to-active spacing device. HP 0.5μm latchup thresholds improve at the rate of ~12 LET per micron of increased well-to-active spacing. Bias of the HP devices was 3.3 V during both ion and laser testing [9].

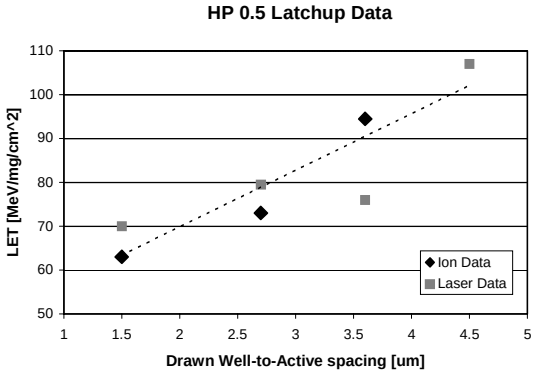

Figure 6. Latchup threshold in LET versus distance between biased N-well and grounded Active regions

The MDT-ASD is designed using SCMOS scalable design rules, which are generally more conservative than the process-specific vendor design rules. The minimum well-to-active spacing in MDT-ASDs is 3 μm, resulting in a 81 LET latchup threshold.

A recent simulation study has shown that the maximum energy deposition occurring with non-negligible probability in the LHC radiation environment will correspond locally to a LET lower than 50 MeVcm^{2}mg^{-1}. This will happen only in the very rare case of a nuclear interaction in tungsten, which is used in certain ICs for connection purposes between metal layers [4][5]. ✌