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Efficient fault-tolerant implementations of non-Clifford gates with reconfigurable atom arrays

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To achieve scalable universal quantum computing, we need to implement a universal set of logical gates fault-tolerantly, for which the main difficulty lies with non-Clifford gates. We demonstrate that several characteristic features of the reconfigurable atom array platform are inherently well-suited for addressing this key challenge, potentially leading to significant advantages in fidelity and efficiency. Specifically, we consider a series of different strategies, including magic state distillation, concatenated code array, and fault-tolerant logical multi-controlled-Z gates, leveraging key platform features such as nonlocal connectivity, parallel gate action, collective mobility, and native multi-controlled-Z gates. Our analysis provides valuable insights into the efficient experimental realization of logical gates, serving as a guide for the full-cycle demonstration of fault-tolerant quantum computation with reconfigurable atom arrays.

The implementation of reliable large-scale quantum computing holds great promise for significant technological advancements but poses substantial challenges in practice, as quantum systems are inherently susceptible to noise and errors. A crucial idea for tackling this problem is quantum error correction (QEC)^{1–3}, wherein the central element is quantum codes that encode the logical information of quantum systems. Logical error rates can be suppressed by the error detection and correction procedure. To implement large-scale general-purpose quantum computation in practice, we further need to be able to execute a universal set of quantum gates at the level of logical qubits fault-tolerantly. The most straightforward fault-tolerant logical gates are those implemented by transversal gates upon codes, which take the form of tensor products of gates acting on disjoint physical subsystems like individual code qubits. Unfortunately, a no-go theorem of Eastin and Knill⁴ states that transversal operators on any nontrivial QEC code cannot be universal, which calls for other approaches for fault-tolerant (FT) logical gates. In general, Clifford gates represent the “easy” part—they can be classically simulated efficiently^{1,5} and are relatively straightforward to protect and implement fault-tolerantly. However, to achieve universal quantum computation, it is necessary to include non-Clifford gates such as T and CCZ gates, which represent the main bottleneck. To address this problem, multiple frameworks have been

proposed and developed, including magic state distillation (MSD)^{6–9}, code concatenation^{10,11}, and code switching^{12,13}.

From a practical viewpoint, the FT implementation of non-Clifford logical gates faces fundamental obstacles when the system architecture or interaction structure is restricted to two spatial dimensions (2D) or lower, which is more feasible in various experimental platforms. In particular, it is well known that for 2D stabilizer codes¹⁴ (such as the surface code^{15–17} which has been a leading candidate for realizing fault tolerance) and even subsystem codes¹⁸, gates that can be implemented transversally or indeed with constant-depth quantum circuits are restricted to the Clifford group. As a result, FT non-Clifford logical gates are expected to be especially difficult to implement due to the necessity of long-range interactions and remain largely unstudied in experiments (The recent seminal work ref. 19 demonstrates the logical CCZ gate on the specific case of $[[8, 3, 2]]$ quantum error-detecting code, yet it does not form a systematic fault-tolerant scheme). Here, we consider the reconfigurable atom array quantum processor, an emerging hardware architecture^{20,21} that enables highly parallel and dynamically all-to-all gates, thereby overcoming the aforementioned geometric locality constraint.

Specifically, we propose and analyze several hardware-efficient schemes for fault-tolerantly implementing non-Clifford gates with reconfigurable atom arrays. The primary ones that we will elaborate on include

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magic state distillation, concatenated code array, and FT logical multi-controlled-Z gates. Remarkably, all of these approaches capitalize on certain characteristic features of the atom array experimental platform, particularly the reconfigurability and parallel efficient control, which enable significant advantages; see Table 1 for a summary. We will describe the implementation methods and analyze their experimental feasibility in detail, from which it will become evident how the native features of the platform are particularly favorable for implementing non-Clifford gates.

Results

Magic state distillation

Magic state distillation (MSD) and injection constitutes a major approach to achieve FT universal logical gates. Roughly speaking, the protocol refers to the procedure of distilling certain non-stabilizer states to arbitrary fidelity from noisy states (which may have suffered from storage error) offline, and

directly “injecting” them into the circuit to realize non-Clifford gates⁶, both steps using only Clifford gates. This method is based on assuming ideal Clifford gates as their fault tolerance can be achieved straightforwardly, and focus on dealing with noisy non-Clifford resources.

Here we consider the T gate (i.e. $T = \exp(-i\pi\sigma^z/8)$), a standard non-Clifford gate that forms a universal gate set together with Clifford gates. It can be implemented with the ancilla $|T\rangle = |0\rangle + e^{i\pi/4}|1\rangle$, as shown in Fig. 1(a). Here, to distill the ancilla, we consider the scheme using the $[[15, 1, 3]]$ quantum Reed–Muller (QRM) code that has transversal logical T . We consider the distillation scheme shown in Fig. 1(b) which consumes 15 noisy ancillae and outputs 1 more accurate ancilla. An EPR pair $(|00\rangle + |11\rangle)/\sqrt{2}$ is prepared and one qubit is encoded into the 15-qubit code. Then a transversal T gate is applied using the input noisy ancillae. Finally, all 15 qubits are measured in the X basis. If any of the four X stabilizers is not satisfied, the output will be discarded, otherwise one may apply a Z operator

Table 1 | Summary of the major schemes for the efficient fault-tolerant implementation of non-Clifford gates considered in this article and the characteristic features of the reconfigurable atom array platform that can significantly enhance their efficiency

	Non-local connectivity	Parallel gate action	Collective mobility	Native multi-controlled-Z
Magic state distillation	✓	✓	✓	
Concatenated code array	✓	✓	✓	
FT multi-controlled-Z codes	✓	✓	✓	✓

The rows correspond to different schemes for fault-tolerant non-Clifford gates, and the columns correspond to features of the reconfigurable atom array platform. Here, non-local connectivity refers to the reconfigurable architecture that allows non-local gates²⁷; parallel gate action refers to the parallel grid illumination that realizes parallel single qubit rotations^{19,47}; collective mobility refers to the transport of multiple qubits via moving 2D acousto-optic deflectors (AOD), which can be used to perform parallel entangling CZ gates in a zone with global Rydberg excitation laser⁴⁸; native multi-controlled-Z refers to the experimental realization of a multi-qubit gate by moving multiple atoms into Rydberg blockade regime, e.g. CCZ by preparing three atoms in the nearest-neighbor blockade regime⁴⁸.

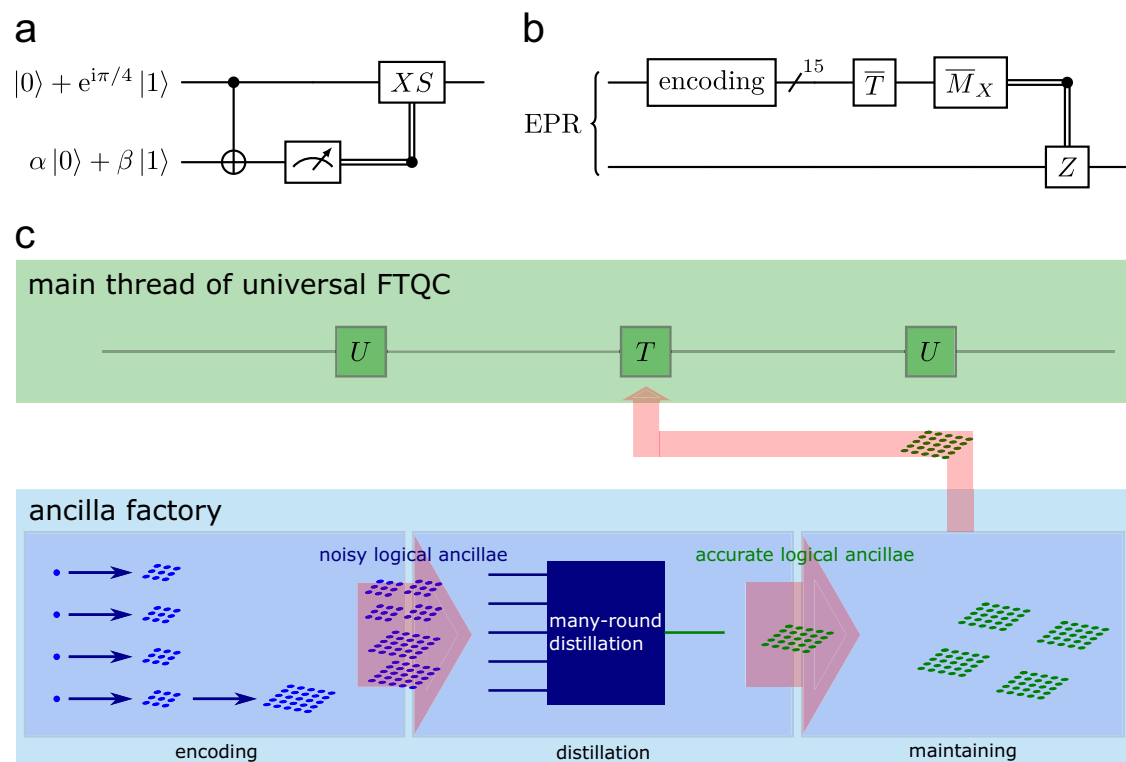


Fig. 1 | Illustration of magic state distillation and its role in universal fault-tolerant quantum computation. a A Clifford circuit for the implementation of a T gate with an ancilla state. Note that the input qubit is destructively measured and the ancillary qubit serves as the output. **b** Illustration of magic state distillation. One qubit of an entangled pair is encoded into the $[[15, 1, 3]]$ quantum Reed–Muller code and a logical T gate is applied via transversal T^* gates. Each T^* gate is implemented using a noisy ancilla. After measurement on the 15-qubit code and a conditioned Z on the

other qubit of the EPR pair, the latter qubit is transformed to a more accurate ancilla. **c** Universal fault-tolerant quantum computation (FTQC) with magic state distillation. The ancilla factory supplies noisy ancillae that are encoded to QEC codes of various sizes and undergo many-round distillation until the desired fidelity is achieved. The produced ancillae are then maintained by standard error correction procedure for quantum memory. When a logical T is required in the main thread of the computation, a good ancilla is moved out from the factory to the computation region.

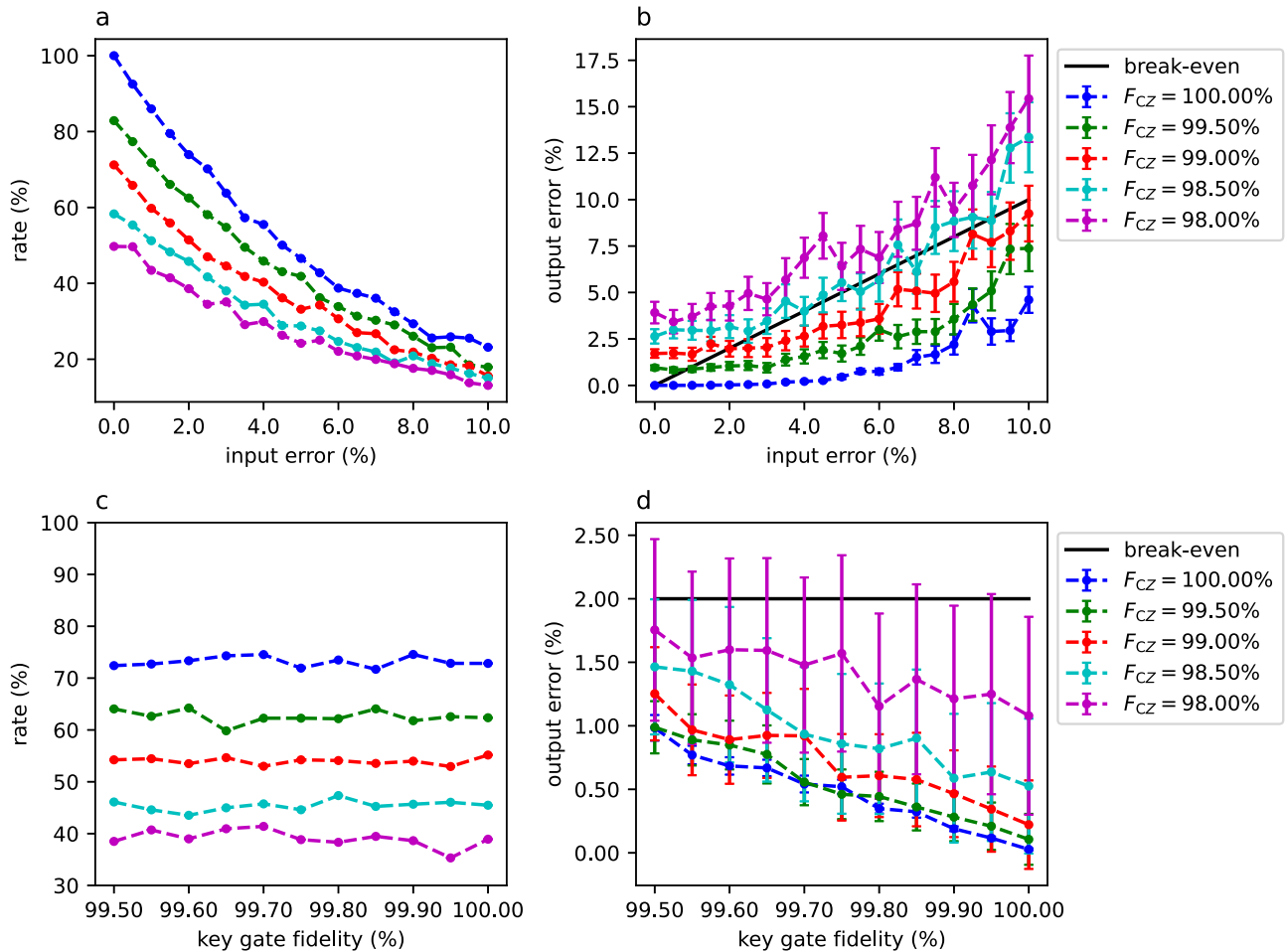


Fig. 2 | Effect of two-qubit gate error on distillation of T gates obtained from Monte Carlo simulation. a, b Rate of successful rounds and output noise as a function of input noise, under different fidelities (F_{CZ} in legend) of two-qubit CZ gates with independent Z errors on each qubit. Break-even condition that output

noise equals to input noise is indicated by the black solid line in **b, c, d** Rate of successful rounds and output noise as a function of key gate fidelity (see main text), under different fidelities of other CZ gates.

conditioned on the product of all X measurements which is exactly the logical \bar{X} measurement (There is an alternative scheme: encode a $|+\rangle = (|0\rangle + |1\rangle)/\sqrt{2}$ to the 15-qubit QRM code, apply a transversal T , and then decode to extract the information in the 15 qubits to one qubit. This scheme uses one less qubit but take twice the number of Clifford gates, which is slower and more sensitive to Clifford errors). See Section "Errors in Clifford gates in magic state distillation" for more details.

Eventually, we would like to carry out magic state distillation on a logical level such that qubits in circuit 1(b) are protected by quantum codes, that is, all the "qubit" in the previous paragraph refers to logical qubit encoded in some codes (for example surface codes). The fault-tolerant universal quantum computation architecture using this logical level distillation is illustrated in Fig. 1(c). A more feasible short-term goal is to distill T ancillae on a physical level, as a demonstration of both the distillation scheme and the experiment techniques.

For physical level distillation, since the $[[15, 1, 3]]$ QRM code is a 3D code, it is inefficient to implement the encoding using local gates in 2D since we need many swap gates for long-range CNOT gates, which not only takes more time but also introduces more errors. The reconfigurability of atom arrays can provide significant advantages. For distillation at the logical level using the surface code, non-local logical CNOT gates between two surface codes are required. Even if lattice surgery techniques²² are used to implement logical CNOT gate locally between adjacent code blocks, the non-locality in the distillation circuit still requires the additional logical swaps,

each using 3 CNOT gates by lattice surgery, making the overhead much larger.

To provide a first estimation of the feasibility of MSD on reconfigurable atomic systems, we consider a simplified error model where independent Z errors can occur on each qubit when applying a CZ gate. This simplification is based on the error analysis on realistic platforms²³. We simulate one distillation round 100 times at different input ancilla noise and CZ gate fidelity. Figure 2a, b reveal the performance of MSD when all CZ gates have the same gate fidelity, which can serve as a reference for near-term experiments. Especially at the state-of-the-art CZ gate fidelity 99.5%²³, one can achieve break-even when the input infidelity is higher than 1% ($\geq 0.75\%$ according to our analytical result). Note that, since 1% is much higher than the error of single-qubit rotation in recent techniques, distillation at the physical level serves more as a proof-of-principle demonstration than a practical procedure.

Figure 2c, d reveals a remarkable observation: when the input noise is 2%, a point at which 99% CZ fidelity achieves break-even (b), only by improving the fidelity of 5 key gates to 99.5% can we achieve break-even when all other CZ gates still have the fidelity of 98%. In fact, our analytic computation shows that the linear dependence of the output error on the CZ error comes totally from the 5 key gates. If these key gates have gate fidelity $(1-q)^2$, (that is, a Z error can occur on each qubit with probability q when applying the gate), while other CZ gates have fidelity $(1-p)^2$, the leading order of the output error is $3.5q$. This linear dependence can be further

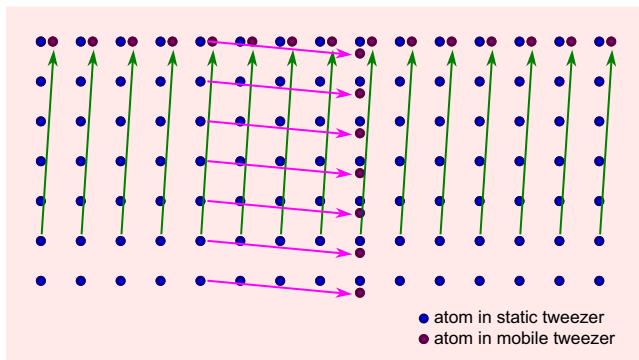


Fig. 3 | Parallel implementation of a universal set of logical gates by code concatenation. A logical qubit is encoded in the $[[7, 1, 3]]$ Steane code concatenated with the $[[15, 1, 3]]$ QRM code forming a 7×15 atom array (dark blue circles) held by an array of static tweezers generated with a spatial light modulator (SLM, red circles), where each row is a 15-qubit code and a physical “qubit” for the 7-qubit code. To apply CNOT gates transversally between two rows, say rows 1 and 6, one can use an array of mobile tweezers generated with AOD to shift one row of atoms to the neighbor sites of the other row (green arrow). One then turns off the tweezers, applies a row of Hadamard gates on the target line, turns on a pulse to apply CZ gates on the atom pairs closer than the Rydberg blockade radius simultaneously, and applies Hadamard gates on the target line again. To apply physical CNOT gates simultaneously between two columns, say columns 5 and 9, one can move one column of atoms to the neighbor of the other (purple arrow). The other operations are similar.

suppressed using a flag protocol^{24,25}; see Section “Errors in Clifford gates in magic state distillation”. Our analysis suggests that, at the fault-tolerant level, costs can be reduced by focusing on the improvement of these key gates, comparing with the former cost analysis where all CZ gates are equally protected.

Concatenated code array

Code concatenation offers another approach to bypass the Eastin-Knill theorem to achieve universal FT gates, which is also particularly fit for the atom array platform. The essential idea is to “combine” different FT gate sets of different codes¹⁰. Consider two codes C_1 and C_2 such that the union of their transversal gate sets is universal. We concatenate these two codes such that each physical qubit in C_1 is encoded as a logical qubit for C_2 . For a small example, we can take C_1 to be the $[[7, 1, 3]]$ Steane code and C_2 the $[[15, 1, 3]]$ QRM code¹⁰. C_1 has transversal gate set $\{H, S, \text{CNOT}\}$ while C_2 has transversal gate set $\{T, \text{CNOT}\}$. We can arrange the physical qubits into a 7×15 array, with each row forming the 15-qubit code while the collection of rows corresponding to the 7-qubit code; see Fig. 3. To implement a logical S or CNOT, we can apply the gate qubit-wise: a qubit-wise S is a logical S^{\dagger} for the 15-qubit code, and a qubit-wise S^{\dagger} is a logical S for the 7-qubit code; similar is the CNOT gate. To implement a logical T, which is not transversal for the 7-qubit code, we need to apply 4 CNOT gates and 1 T gate at the physical level of the 7-qubit code, which are transversal for the 15-qubit code: errors can only propagate within individual columns. To implement a logical H, which is transversal for the 7-qubit code but not transversal for the 15-qubit code, we need to apply a logical H gate, which amounts to 14 CNOT gates and 1 H gate, for each 15-qubit code: errors can only propagate within individual rows²⁶. Both C_1 and C_2 have distance 3 but neither has a transversal universal gate set. Nevertheless, we can implement a universal gate set fault-tolerantly in the concatenated code with an effective distance of 3.

The parallel gate action and the collective mobility features of the atom arrays are ideal for implementing a concatenated code array scheme. For instance, in the logical T and H implementation, CNOT gates between two rows or columns can be performed in parallel via transport-based entangling gates²⁷, see Fig. 3 for details. To demonstrate the experimental feasibility, we give an estimation for the time cost of logical T and H based on the architecture and technology demonstrated

in²⁷, utilizing a system of acoustic optical deflectors (AOD). This system enables a simultaneously movement of an entire row or column of the tweezers array. In the atom arrays, two atoms are separated by roughly 10 μm . Two adjacent sites in static tweezer are separated by less than 2 μm . According to ref. 27, at the length scale of the separation of several atoms, the average moving velocity of atoms is roughly 0.5 m/s under the requirement that fidelity is well preserved. We use this value for estimating the time cost and neglect the acceleration profile that can be tuned for further optimization. The typical moving time is thus at the order of some 20 μs . Besides moving the atoms there are other processes, including the pulse implementing CZ gates, which lasts for roughly 200 ns \ll 20 μs , and transferring between spatial light modulator (SLM) and AOD tweezers which takes roughly 100 ~ 200 μs ¹⁹. Only the last procedure is relevant to our time estimation. For logical T gate, 4 cycles of CNOT gates are needed^{10,26}, involving row movements $R_7(7 \rightarrow 6)$, $R_6(6 \rightarrow 1)$, $R_6(1 \rightarrow 6)$, $R_7(6 \rightarrow 7)$, where $R_i(j \rightarrow k)$ means moving the i th row of atoms from row j to row k , taking roughly 20 μs , 100 μs , 100 μs , 20 μs , respectively, adding up to 0.24 ms for moving only and 0.84 ms with transferring time included (taking transferring time as 150 μs). For logical H gate, 8 cycles of CNOT gates are needed²⁶. In the worst case that after each step columns are moved back to its original position, it takes roughly 3.76 ms to implement the logical H gate, comparing to an order of seconds for the decoherence time of an atom qubit. The time cost can be further reduced by optimizing the moving strategy based on different computational task at a software level, as well as using time-optimal control techniques at a hardware level.

Fault-tolerant logical multi-controlled-Z gates

One advantage of the reconfigurable atom array platform is the natural physical implementation of multi-controlled-Z gates, denoted by $C^m Z$ where m is the number of control qubits, which are non-Clifford when $m \geq 2$. Due to this feature, we are tempted to consider $C^m Z$ gates which are suited to certain important scenarios (e.g., generating hypergraph states²⁸ which are representative many-body entangled magic states²⁹) and generally provide an alternative choice of non-Clifford gates for circuit compilation.

Stabilizer codes based on triorthogonal matrices, such as the $[[15, 1, 3]]$, $[[49, 1, 5]]$, and a family of $[[3k + 8, k, 2]]$ triorthogonal codes, support logical CCZ gates implemented by transversal physical CCZ gates^{7,30}. Additionally, the 3D surface code on the rectified cubic lattice, which exhibits a similar triorthogonal structure, has logical CCZ gates implemented by transversal physical CCZ gates³¹. This concept has been further generalized to the 4D octaplex tessellation, enabling the logical CCCZ gate to be implemented by transversal physical CCCZ gates³². Generally, the D -dimensional toric code permits logical non-Pauli gates from the D -th level of the Clifford hierarchy¹⁴. The duality between color codes and toric codes³³ enables logical $C^{D-1}Z$ gates in the D -dimensional toric code through transversal R_m gates up to a Clifford circuit, where $R_D := \text{diag}(1, \exp(2\pi i/2^D))$, saturating the Bravyi-König bound¹⁴. Furthermore, we consider the D -dimensional $(1, D-1)$ -toric code on the hypercubic tessellation where the physical system consists of one qubit per edge, and the stabilizers are X-star (product of X incident at a vertex) and Z-plaquette (product of Z around a face) terms. It contains 0-dimensional excitations (i.e., particles) and $(D-2)$ -dimensional excitations. As discussed in detail in Section “Fault-tolerant logical $C^{D-1}Z$ gates in D -dimensional toric codes” the logical $C^{D-1}Z$ gates can be implemented fault-tolerantly with a constant-depth circuit of physical $C^{D-1}Z$ gates. This approach has the advantage that the implementation is straightforward and can be generalized directly to higher dimensions, without the need for intricate higher-dimensional rectifications or tessellations. It is worth emphasizing the suitability of high-dimensional codes and multi-controlled-Z gates for the reconfigurable atom array platform. To achieve universality, we may use such codes in code-switching or code concatenation strategies. In this platform, these exotic high-dimensional codes can offer unique implementation advantages and greater flexibility for gate choice, further enhancing their utility in practical quantum computing.

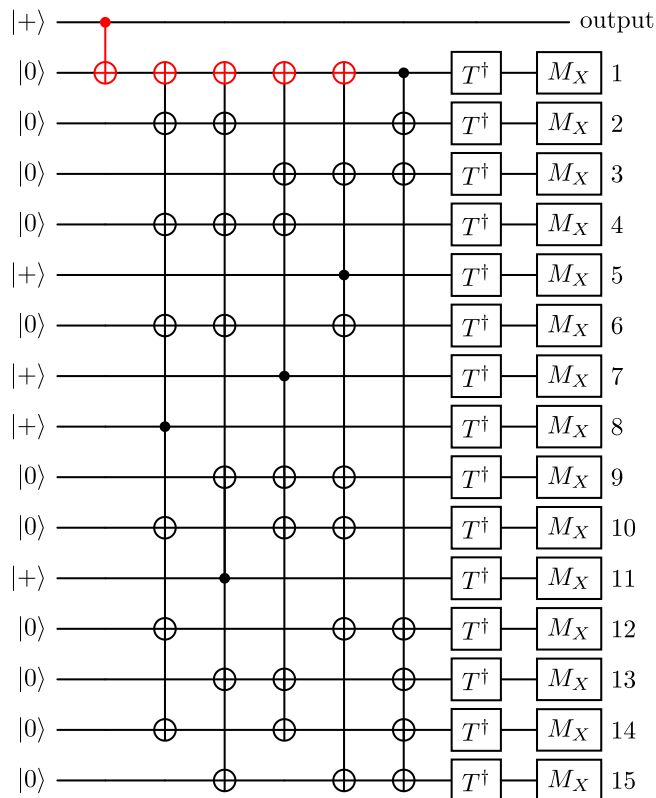


Fig. 4 | Circuit for magic state distillation of T ancilla. The key gates, CNOT between output and qubit 1, CNOT_{8,1}, CNOT_{11,1}, CNOT_{7,1}, CNOT_{5,1} are labelled red.

Discussion

Implementation of non-Clifford gates is costly but indispensable for fault-tolerant universal quantum computation. In this article, we describe how the native features of the reconfigurable atom array platform can lead to unique advantages in fault-tolerantly implementing non-Clifford gates. In particular, we provide detailed analyses for magic state distillation and code concatenation methods. Moreover, motivated by the unique feasibility of multi-controlled-Z gates in this platform, we specifically discuss codes that use them to realize FT logical multi-controlled-Z.

Besides the methods analyzed in detailed in this article, there are other schemes for FT universal gates. A well-established one is code switching^{12,34}, which enables transversal universal gates through gauge fixing. This approach also inevitably involves codes beyond 2D so the reconfigurability of the atom array is again crucial. It could also be worthwhile to further explore the usage of relevant methods such as flag qubits^{24,25} and just-in-time decoding^{35,36}.

On the other hand, it would be valuable to systematically benchmark and compare the resource costs of different approaches for fault tolerance in the reconfigurable atom platform as well as other platforms, in light of the comparison between e.g. MSD and code-switching with color codes³⁷ in the literature. Furthermore, our discussion of the implementation of different types of non-Clifford gates offer flexibility for circuit compilation, opening up further opportunities to optimize the cost of logical quantum computation. Broadly speaking, we consider further investigation into the implementation cost in conjunction with different compilation schemes and features of experimental platforms important and valuable.

There are also various other proposals exploring different aspects of quantum computing with the reconfigurable atom array platform, including converting leakage errors that are dominant on atomic systems to erasure errors³⁸, utilizing the biased error structure introduced by some conversion protocol to achieve better fault-tolerant performance^{39,40}, implementing highly non-local quantum LDPC codes via reconfiguration of atoms⁴¹, and

surface code architectures enhancing logical qubit connectivity by moving atoms⁴². With the rapid advancements of experimental technologies, now is an opportune time to explore and implement different methods which may pave the way for practical quantum computing.

Methods

Errors in Clifford gates in magic state distillation

In this subsection we discuss in some detail the effect of Clifford errors in magic state distillation of T ancilla. We use the $[[15, 1, 3]]$ quantum Reed–Muller code with check matrix

$$H_X = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix},$$

$$H_Z = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}, \quad (1)$$

where each row in H_X defines an X stabilizer which has the identity operator I on sites with 0 while X on sites with 1. For example, the first row in H_X gives the stabilizer $X_1X_3X_5X_7X_9X_{11}X_{13}X_{15}$. Similarly, rows in H_Z define the Z stabilizers. One logical qubit encoded in this code is

$$|\bar{0}\rangle = \prod_{i=1}^4 \frac{I + S_X^i}{\sqrt{2}} |00 \dots 0\rangle, \quad |\bar{1}\rangle = \prod_{i=1}^4 \frac{I + S_X^i}{\sqrt{2}} |11 \dots 1\rangle, \quad (2)$$

where S_X^i is the i th X stabilizer. It is straightforward to verify that

$$T^{\dagger \otimes 15} |\bar{0}\rangle = |\bar{0}\rangle, \quad T^{\dagger \otimes 15} |\bar{1}\rangle = e^{i\pi/4} |\bar{1}\rangle, \quad (3)$$

indicating that this code has a transversal logical T implementation via a bit-wise physical T^\dagger gate.

The detailed circuit for distillation¹⁷ is shown in Fig. 4. The circuit starts from an EPR pair (first two lines), then one of the entangled qubits is encoded into a 15-qubit code, followed by a transversal T gate and X -basis measurement for each qubit in the 15-qubit code. The measurement results are used to calculate four X stabilizers shown in Eq. (1) as well as the logical \bar{X} operator, which is the product of X operators on the 15 qubits. If any of the four stabilizers is not + 1, the output is discarded. Finally a Pauli Z gate may be performed on the output qubit conditioned on the measurement outcome of the logical \bar{X} operator. As discussed in the main text, we consider the major class of error, that is, the Z error on the CZ gates, which is modelled as

$$E(\rho) = CZ((1-p)^2\rho + p(I \otimes Z\rho I \otimes Z + Z \otimes I\rho Z \otimes I) + p^2Z \otimes Z\rho Z \otimes Z)CZ^\dagger. \quad (4)$$

The Choi gate fidelity is $F_{CZ} = (1-p)^2$. A CNOT gate can be obtained from a CZ gate by conjugating an H on the target qubit, which converts the Z error to an X one. In this error model, we see that

- The Z error on the control qubit when entangling the output qubit with qubit 1 will directly come into the final result, yielding a Z error.
- The five X errors on the target qubit 1 will be spread to qubits 1, 2, 3, 12, 13, 14, 15 as $X_1X_2X_3X_{12}X_{13}X_{14}X_{15}$ since $\text{CNOT}(X) \text{CNOT} = XX$. Since $T^\dagger X = e^{-i\pi/4} X T^\dagger$, where the factor is irrelevant while acting an X before measuring X has no effect, this error is equivalent to acting $S^{\otimes 7}$ on the 7 qubits. A straightforward calculation using equation (2) shows that this

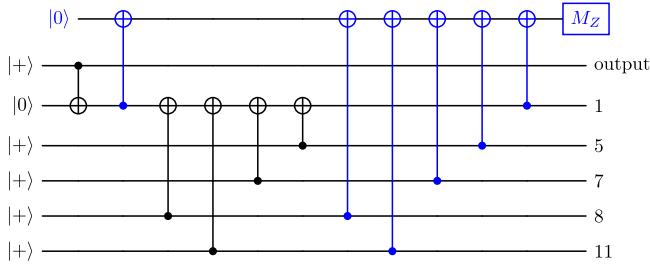


Fig. 5 | Using flag qubit gadgets to detect errors on qubit 1. Here only the relevant gates in the distillation circuit are shown. The flag qubit gadgets are colored blue. If an X error occurs on qubit 1 within the flag qubit gadgets, their corresponding flag qubit will be measured — 1 and this round of distillation should be discarded. However, a Z error on the control qubit (1) of the leftmost blue CNOT gate can be propagated to qubits 1, 5, 7, 8, 11, which is a logical Z operator. As a result, this flag gadget can reduce the linear dependence of the output error from $3.5p$ to $2.5p$.

is a logical S^z gate, which will be teleported to the output qubit. An S^z error with probability q contributes $0.5q$ to the output error.

- Other errors, including those in implementing T^z using noisy ancillae, are not spread, reducing linearly the rate of success while the contribution to the output error is at a higher order. From the first two points, we see that if the gate fidelity is $(1-p)^2$, the output qubit will be found with a Z error at probability p , and an S error at probability $5p$, yielding an output fidelity $1 - 3.5p$. Higher order contribution can come from two-qubit gates other than these 5 key gates.

The effect of measurement error can be converted to that of an error in the preceding T gates, which turns out to be a less serious problem. To see this, let's write down the channel of a projective X measurement⁴³, which maps a quantum register to a pair consisting of the quantum register itself and a classical “record”,

$$M_X(\rho) = (\Pi_+ \rho \Pi_+, +) + (\Pi_- \rho \Pi_-, -). \quad (5)$$

Here $\Pi_{\pm} = (1 \pm X)/2$. A measurement with error rate p can be modelled by

$$M_X^e(\rho; p) = (1-p)[(\Pi_+ \rho \Pi_+, +) + (\Pi_- \rho \Pi_-, -)] + p[(\Pi_+ \rho \Pi_+, -) + (\Pi_- \rho \Pi_-, +)]. \quad (6)$$

Since $\Pi_+ = Z \Pi_- Z$, the measurement error is equivalent to a pair of Z errors correlated in time, happening before and after the projection. However, since we are doing single-qubit measurements so that the measured qubit, after projection, ceases to entangle with any other qubits, the Z error after the projection has no effect on our distillation result. Therefore, the erroneous measurement is equivalent to the channel

$$M_X'(\rho) = M_X((1-p)\rho + pZ\rho Z). \quad (7)$$

This is nothing but a Z error before a perfect measurement. If the T gate error rate is ϵ , while measurement error rate is p , their influence to the distilled state is equivalent to $\epsilon = \epsilon + p$ and $p = 0$. In conclusion, measurement errors, which are dominant in atomic platform, have the same effect as the T gate errors which are designed to be protected in MSD.

We can use a flag gadget to further reduce this linear dependence, see the blue part of Fig. 5. This flag gadget can detect whether there is an error on qubit 1 from CNOT gates between qubit 1 and qubits 5, 7, 8, 11, hence eliminate the contribution to the output error from these four gates. However, error on qubit 1 from the first CNOT between qubit 1 and the flag qubit can contribute linearly to the output error, since this error is propagated by the four following CNOT gates to a logical Z error. Therefore, our flag gadget can reduce the number of key gates to 2 and reduce the output error from $3.5p$ to $2.5p$, where $(1-p)^2$ is the fidelity of the key gates. See Fig. 6 for a numerical simulation.

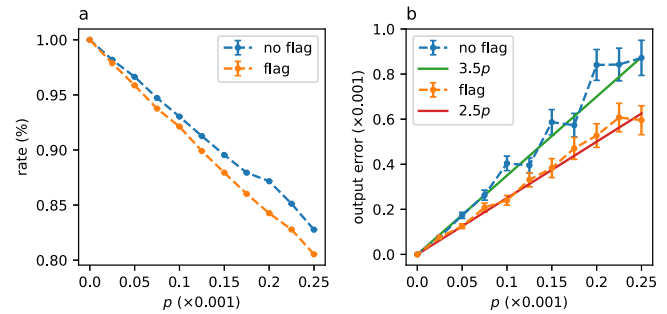


Fig. 6 | Effects of flag gadgets. The rate (a) and output error (b) with and without flag gadgets, with data obtained by 200 rounds Monte Carlo simulation for each point. The input ancillae are accurate. The rate is suppressed linearly with flag since several single CNOT error now contributes linearly to the — 1 flag measurement instead of the output error. The output error shows a behaviour of $3.5p$ and $2.5p$ with or without flag gadget, respectively.

Numerical simulation of MSD

In simulating the errors of Clifford gates in MSD, we randomly introduce rotation errors subject to a proper Gaussian distribution instead of randomly introducing Pauli errors. To see how this works, note that on a density matrix

$$\rho = \frac{1}{2}(I + \rho_x X + \rho_y Y + \rho_z Z), \quad (8)$$

a Pauli Z error with probability p is given by the error channel

$$E(\rho; p) = (1-p)\rho + pZ\rho Z = \frac{1}{2}\left(I + \rho_z Z + (1-2p)(\rho_x X + \rho_y Y)\right). \quad (9)$$

On the other hand, consider a rotation with angular distribution f ,

$$\begin{aligned} R(\rho; f) &= \int d\theta f(\theta) e^{i\theta Z/2} \rho e^{-i\theta Z/2} \\ &= \int d\theta f(\theta) \frac{1}{2}\left(I + \rho_z Z + (\rho_x \cos \theta + \rho_y \sin \theta)X + (\rho_y \cos \theta - \rho_x \sin \theta)Y\right). \end{aligned} \quad (10)$$

If f is an even function, the two channels are the same under the condition

$$\overline{\cos \theta} = 1 - 2p. \quad (11)$$

Specially, if f is a Gaussian distribution with standard deviation σ , the equivalence condition becomes

$$e^{-\sigma^2/2} = \overline{\cos \theta} = 1 - 2p, \quad (12)$$

which reduces to $\sigma = 2\sqrt{p}$ for small error rates.

The advantage of such a simulation procedure is that it converges more quickly than directly simulating random Pauli errors. To simulate a Z error channel with error rate p , one may randomly choose to do nothing with probability $1-p$, or to apply a Z gate with probability p . To see how many rounds are needed to obtain this average output, we need to consider the variance of the output. Actually, in our simulation, there are two possible outputs with probabilities

$$\rho' = \begin{cases} \frac{1}{2}\left(I + \rho_z Z + (\rho_x X + \rho_y Y)\right), & \text{with } 1-p, \\ \frac{1}{2}\left(I + \rho_z Z - (\rho_x X + \rho_y Y)\right), & \text{with } p. \end{cases} \quad (13)$$

The fidelity of these two outputs (that is, their overlap with the input state) are respectively 1 and $(1 + \rho_z^2 - (\rho_x^2 + \rho_y^2))/4$. The average fidelity is $(1 + \rho_z^2 + (1 - 2p)(\rho_x^2 + \rho_y^2))/4$. The variance of the fidelity is $\sqrt{p(1-p)(\rho_x^2 + \rho_y^2)}/2$. On the other hand, one may also simulate the random rotation with a Gaussian distributed angle,

$$F(\rho; \sigma) = \int d\theta \frac{e^{-\theta^2/2\sigma^2}}{\sigma\sqrt{2\pi}} e^{i\theta Z/2} \rho e^{-i\theta Z/2}. \quad (14)$$

For a single θ , the output is

$$\rho' = \frac{1}{2} \left(I + \rho_z Z + (\rho_x \cos \theta + \rho_y \sin \theta) X + (\rho_y \cos \theta - \rho_x \sin \theta) Y \right), \quad (15)$$

corresponding to fidelity $(1 + \rho_z^2 + \cos \theta (\rho_x^2 + \rho_y^2))/4$. The average fidelity is $(1 + \rho_z^2 + e^{-\sigma^2/2} (\rho_x^2 + \rho_y^2))/4$. Now the variance of the fidelity is $(\rho_x^2 + \rho_y^2)(1 - e^{-\sigma^2})/4\sqrt{2}$. For small p , the ratio of the variances between these two sampling procedures is $\sqrt{2p/(1-p)}$. If $p = 0.5\%$, to achieve the same stability, the rotation sampling requires 1/14 of the rounds required by the naive Z sampling. The error bars in our data reflect this variance.

Furthermore, this simulation procedure is more realistic since errors are introduced by fluctuations in the experiments, which are continuously distributed. The stability of the simulation result, which is better than that simulated by introducing discrete Pauli errors, should reflect the real stability when doing the experiments using physical qubits. However, in the ultimate goal of distillation with logical qubits, mid-circuit error-correcting procedure can transfer the errors to discrete Pauli errors, leading to a larger variance in the output fidelity.

Fault-tolerant logical $C^{D-1}Z$ gates in D -dimensional toric codes

This section introduces a simple method for topologically protected FT logical $C^{D-1}Z$ gates in D -dimensional toric codes using physical $C^{D-1}Z$ gates. As an example, we start with two layers of 2D toric codes on the square lattice. One logical \bar{X}_1 gate in the first layer and another logical \bar{Z}_2 in the second layer are

$$\bar{X}_1 = \cdots \begin{array}{|c|c|c|} \hline & & \\ \hline X_1 & X_1 & X_1 \\ \hline & & \\ \hline \end{array} \cdots, \quad \bar{Z}_2 = \cdots \begin{array}{|c|c|c|} \hline & & \\ \hline Z_2 & Z_2 & Z_2 \\ \hline & & \\ \hline \end{array} \cdots \quad (16)$$

The CZ gate between logical qubits in the two different layers of toric codes is

$$\cdots \begin{array}{|c|c|c|} \hline & & \\ \hline 2 & 2 & \\ \hline \text{CZ} & \text{CZ} & \\ \hline 1 & 1 & \\ \hline & & \\ \hline \end{array} \cdots \quad (17)$$

the product of two physical CZ gates on each face, where the labels 1, 2 indicate which layer it acts on. Two CZ gates correspond to two different paths from a corner of a square to the opposite corner.

This construction can be extended to three dimensions. Consider three layers of 3D toric codes. Logical X gates become membrane operators, while logical Z and CZ gates are the same as the 2D toric code. Define logical \bar{X}_3

and logical $\bar{CZ}_{1,2,3}$ as

$$\cdots \begin{array}{|c|c|c|} \hline & & \\ \hline X_3 & X_3 & X_3 \\ \hline & & \\ \hline \end{array} \cdots \quad (18)$$

$$\cdots \begin{array}{|c|c|c|} \hline & & \\ \hline 3 & 3 & \\ \hline \text{CZ} & \text{CZ} & \\ \hline 2 & 2 & \\ \hline & & \\ \hline \end{array} \cdots \quad (19)$$

where logical $\bar{CZ}_{1,2,3}$ is the product of six CCZ gates in each cube. The labels 1, 2, 3 indicate which layer it acts on, and the six CCZ gates represent six paths from one corner to the opposite corner on a cube. One can verify that

$$\bar{CZ}_{1,2,3} \bar{X}_3 \bar{CZ}_{1,2,3} = \bar{X}_3 \bar{CZ}_{1,2}. \quad (20)$$

This construction applies to the D -dimensional hypercube directly, where $C^{D-1}Z$ gates act on the edges of each path from one vertex to the opposite corner. In group cohomology language, the logical $\bar{CZ}_{1,2}$ and $\bar{CZ}_{1,2,3}$ can be expressed by the cocycles $\frac{1}{2}a_1 \cup a_2 \in H^2(\mathbb{Z}_2 \times \mathbb{Z}_2, \mathbb{R}/\mathbb{Z})$ and $\frac{1}{2}a_1 \cup a_2 \cup a_3 \in H^3(\mathbb{Z}_2 \times \mathbb{Z}_2 \times \mathbb{Z}_2, \mathbb{R}/\mathbb{Z})$. In D dimensions, the logical $C^{D-1}Z$ gate corresponds to the cocycle $\frac{1}{2}a_1 \cup a_2 \cup \cdots \cup a_D \in H^D(\mathbb{Z}_2^D, \mathbb{R}/\mathbb{Z})$. The details can be found in refs. 44–46.

Data availability

The simulation data for error analysis of magic state distillation is available at https://github.com/Florestan-Eusebius/error_msd.

Code availability

The codes used for simulating magic state distillation is available at https://github.com/Florestan-Eusebius/error_msd.

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Author contributions

Y.W. (Yifei Wang) led the technical work, with essential contributions from Y.W. (Yixu Wang) and Y.A.C. Y.W., Y.W., Y.A.C., Y.G. and Z.W.L. are responsible for the theoretical content and the writing of the manuscript. W.Z., T.Z., J.H. and W.C. provided advice and insights from experimental perspectives. Y.G. and Z.W.L. conceived and supervised the project. All authors contributed to discussions that led to the completion of this work and approved the final manuscript.

Competing interests

The authors declare no competing interests.

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