Materials for Quantum Technology

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PERSPECTIVE

Quantum Technologies for Engineering: the materials challenge

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Abstract

The materials challenge is often a major hurdle for translating good ideas in science into technologies. This is no different in the arena of quantum technologies which has seen a resurgence of interest in the last decade. This perspective provides a unique insight into the recent collaborative works by research groups in Singapore to surmount key quantum materials and processing bottlenecks that have impeded quantum technologies in the areas of sensing, computing, and communications. We highlight recent important materials related breakthroughs that have made possible novel advancements such as integrated ion traps, light frequency conversion, highly efficient cryogenic contacts to atomically thin quantum devices, and gate defined quantum dots, to name just a few. We also discuss the potential applications and conclude with our perspective on the remaining challenges to be addressed and the prospects enabled by these materials advances for future collaborations and co-developments to advance quantum technologies.

1. Introduction

Significant progress in realizing quantum devices for sensing, computation, and communications has taken place over the last 20 years. Advancement in quantum science has proven the key underlying physics of quantum phenomena such as tunnelling, superposition, and entanglement. Initial quantum algorithms for encoding, factorization, searching, and efficient processing have also been developed for computation. Superconducting circuits [1], trapped ions [2], photonic systems [3], and quantum dots [4, 5] have shown promise towards achieving quantum advantage, or the ability to solve a programmable computational problem that no classical computer can solve in a reasonable amount of time.

Many materials science and processing challenges of implementing practical quantum devices and systems remain unsolved [6]. Among these hard challenges are (1) realizing high-fidelity qubits, (2) solving the scalability problems of realizing several hundreds of qubits working in close proximity and with a practical number of electrical interconnections to the outside world, and (3) miniaturizing the optical sources, detectors, and components which often lead to massively large and non-scalable optical benches, which might be simply described as solving the 'free space optics problem'.

The above challenges represent significant research topics involving both public and private sectors around the world. Different technology approaches based on superconducting circuits, ion traps, solid-state qubits, and photons are actively being pursued to realize scalable quantum computation.

Superconducting qubit approaches are the most pursued with research efforts taking place at Google [1], IBM [7], and Rigetti [8]. While being lithographically scalable and compatible with semiconductor fabrication tools, superconducting qubits need to maintain qubit coherence times compatible with an appropriate quantum processor usually implemented by a classical computer. A recent review paper by Martinis [9] attributes limitations in coherence time to materials loss issues associated with multiple materials interfaces in the superconducting junction structures.

Quantum computing based on ion traps is also being pursued by private entities including Quantinuum [10] (a partnership between Honeywell Quantum Solutions and Cambridge Quantum) and Ion-Q [11]. Significant challenges in ion trapping approaches involve the ability to manipulate, or shuttle, multiple chains of ions with one another. This often requires multiple electrodes to precisely control electrical fields close to the qubit plane. These electrodes and electrical interfaces must also be compatible with multiple free-space lasers and optics are required to address individual ions. The realization of thousands of electrical interconnections on a planar ion trap surface is therefore a fabrication challenge for which three-dimensional integrated circuit processing techniques may be required [12].

Solid-state qubits include those based on semiconductors manipulated electrostatically or optically. Electrostatically gated quantum dots were originally demonstrated in GaAs/AlGaAs heterostructures [12], but more recently Si-based quantum dots [13] have shown longer coherence times and excellent compatibility with silicon-based integrated circuit manufacturing. A significant challenge however lies in realizing sufficiently high and reproducible electron-spin coherence times in the solid-state materials. Silicon-based quantum computing approaches are currently underway at Intel—Delft University [14] and Silicon Quantum Computing [15] in Australia.

Photons have a desirable property for implementing a quantum computer because of their inherent weak interactions with the environment. In realizing a two-qubit gate however photon-photon interactions are weak. Semiconductor chips that support these optical interactions require small optical components such as waveguides, mirrors, and beam splitters limited by the fundamental challenge of their constituent materials [12].

National research funding has been a dominant driver for quantum computing. Europe launched its Quantum Flagship [16] in 2017 in four application domains: communication, computation, simulation, and sensing/metrology. Twenty projects were launched including one to build a quantum computer with up to 100 superconducting qubits and another to realize a fully automated ion-trap quantum computer.

In 2013 the UK has implemented a similar National Quantum Technology Programme [17] to the EU programme above directed towards advancing quantum science and demonstrator platforms in imaging, sensors, and metrology, communications, and computing across 30 universities. The UK has developed a network of quantum technology hubs such as the Networked Quantum Information Technologies (NQIT) hub at Oxford [18]. National facilities and laboratories Quantum Systems Engineering Skills Hubs have been established.

The US National Quantum Initiative [19] began in 2018 to support Quantum Information Science Technology (QIST) in three broad areas: quantum communication, quantum sensing, and quantum computing. The US relies on multiple government agencies including the Department of Energy, Department of Defense, and National Science Foundation to administer funding primarily to academic participants. A materials research example funded by the National Science Foundation is the Quantum Foundry at UC Santa Barbara which has three fundamental research thrusts: natively Entangled Materials, Interfaced Topological States, and Coherent Quantum Interfaces [20].

China has invested USD 987 million through its National Major Project of China [21] directed towards quantum communication, quantum computation, and quantum metrology.

Japan has carried out multiple research initiatives in quantum technologies over the last 30+ years. The most recently announced US $200 million over 10 years initiative known as 'Q-LEAP' [22] covers three pillars of quantum simulation and computing, quantum sensing, and ultrashort pulse lasers. Japan's research innovations have taken place in quantum dots, superconducting qubits, quantum annealing, and optical lattice clocks.

Australia [23], Canada [24], and Russia [25] have all developed similar national efforts to the above countries. Common themes are communications, sensing, computing, and other enabling technologies.

In contrast, Singapore has not invested research resources across these common themes but instead has targeted a selection of bottleneck challenges in quantum computing. In 2017, Singapore launched its Quantum Technologies for Engineering (QTE) programme to address these challenges through leveraging its multidisciplinary materials science and microelectronic materials processing capabilities at the A*STAR Institute of Materials Research and Engineering, A*STAR Institute of Microelectronics, Nanyang Technological University, and National University of Singapore. The programme is focused on addressing the materials challenges for several quantum applications. Following a brief executive summary of the key contributions from this programme in the remainder of this introduction, the subsequent sections will highlight key aspects of each development vis-à-vis the state-of-the-art as appropriate and discuss the outstanding challenges that remain.

To reduce the many wired electrical interconnections which have long been considered a reliability problem, a source of unwanted noise, and a huge area requirement for conventional wire bonding pads, three-dimensional (3D) wafer-scale ion traps based on $^{88}Sr^{+}$ were fabricated in a CMOS-compatible process [26] The use of electrically conducting through-silicon vias (TSVs) has resulted in higher performance Q-factor, high power spectral density, and lower insertion loss. TSVs and CMOS packaging methods have resulted in a 95% area reduction.

Transition metal dichalcogenide (TMDC) materials including MoS_2 and WS_2 are selected as a potential solid-state qubit owing to its valley-protected spin and potential long coherence time, strong spin-orbit coupling, and ability to be realized in a simple electrically gated quantum dot device through conventional planar nanolithographic processing [27]. The use of TMDC materials for implementing solid-state quantum dot qubits is still in early development.

Computational structures implemented by ion traps and quantum dots typically emit photons at visible wavelengths which exhibit significant loss if passed through conventional fibre networks. Ideally one would like to manipulate and move quantum information encoded in light through existing optical fibres as used extensively by the telecommunications industry. The development of frequency converting nonlinear materials based on second harmonic generation (SGH) in (gallium phosphide) GaP have therefore been developed as a 'photonic gearbox' for the generation of quantum states of light (entangled photons and squeezed light) [28–30]. Further design and fabrication methods have realized GaP resonant metasurfaces using SGH for both pulsed and continuous-wave (CW) laser conversion. Additional emplacement of such metasurface devices directly on optical fibre surfaces has eliminated the need for bulk optical components.

A basic tenet of the QTE research strategy has been to remove the significant barriers holding back the technological quantum community, which can be simply described as (1) developing the long-coherence time solid-state materials to solve the qubit scalability problem; (2) solving the massive electrical interconnection and packaging problem through CMOS-compatible materials, processing, and 3D integration; and (3) eliminating the free-space optics problem through SGH materials and direct integration with existing optical fibres.

The relatively short four-year duration of the QTE research programme has laid significant new capabilities which are already contributing to the development of more robust qubits, novel quantum sensors and effective quantum interconnects. Additional materials approaches, processing, and systems integration are continuing in Singapore for the realization of quantum sensing, computing, and communication systems.

2. Materials for engineering solid-state qubits technologies

In quantum computation, a current challenge in hardware is to build several hundreds of very high-quality qubits and operate them with >99.99% fidelity, or to make do with several hundreds of logical qubits comprising noisy (typically <99.99% fidelity) code qubits and a significant number of ancilla qubits to help with error correction. The latter typically requires hardware overheads that amount to the order of 10^8 qubits or more to begin solving useful real-world problems [31, 32]. The technology for this level of scaling is not yet available, and current quantum computers [1, 33] with few to several tens of noisy qubits (<99.9% fidelity) are referred to as noisy intermediate-scale quantum (NISQ) systems. In many recent press releases of advances in quantum computing, the reader is often shown a well-packaged chip appearing not too different from a microchip with more than 10 billion transistors typically packed into our modern mobile phones or computers. Hence, it is not unreasonable to surmise that it should be possible to scale up to the 10^8 qubits in a chip using such microfabrication technologies. Indeed, some qubit platforms [2, 3, 34, 35] have specifically been designed to take advantage of existing scalable technologies. Why then do we not have at least a million qubits today?

The quantum phenomena employed in qubits are unfortunately much less forgiving of environmental disturbances compared to the electrical switching in transistors. Hence the ideal environment for keeping a stable qubit is a well-isolated vacuum. Except for a few types of qubits (e.g., trapped ions or atoms in vacuum), most other qubit options reside in some material environment. Some researchers, therefore, coined the concept of a 'material vacuum' to host a qubit. What this implies is a material environment devoid of inhomogeneous composition, defects, unexpected foreign contaminations, irregular interfaces, and any other factors that can unintentionally interact with the qubit. These are potential sources of decoherence for the qubits and can create variations from qubit to qubit, which make for complex control strategies to run the quantum computer. For a number of qubit platforms that leverage on chip-scale substrates for fast scale-up [2, 3, 34, 35], these materials-related challenges are significant hindrances to progress. Indeed, the recent seminal review by de Leon *et al* highlights that there is an urgent need to rein in materials scientists and engineers now to help solve this materials bottleneck for qubit scale-up, and encourages the exploration of new material options to increase the odds of finding better options for scalable staple qubits [6].

In this context, we chose to focus on solving some of the materials engineering requirements related to (1) trapped ion qubits, which was already relatively mature and with outstanding coherence lifetimes and gate fidelities [2], and (2) explore the new vista of 2D quantum materials for possible new solid-state qubit options [36, 37]. Here, we shall provide a synopsis of the key highlights in these works, the details of which can be found in published reports and the references therein [27, 38].

2.1. Materials engineering for on-chip ion-trap qubits

As a more mature qubit platform, ion-trap qubits could give a quick route towards translational innovation and commercial scale-up, as well as for building training or educational systems [39] However, the realization of multi-qubit surface ion traps faces practical scaling and performance challenges. In a typical ion trap, a few hundred electrodes (DC/RF) are fabricated on the chip [40–43]. The DC trapping potential is supplied by electrodes that are wire bonded to a package. In addition, surface capacitors or external capacitors, bonded on the package, are used to filter RF pickup on the electrode. As a result, the bond pads and capacitors consume the majority of the trap chip area, hence constraining the layout of the DC/RF electrodes. Wire bonds often obstruct the laser access used for ion trapping and qubit manipulation. These limitations have severely impaired scaling required for ion traps arrays. Furthermore, the parasitic capacitance of surface traps results in high dissipation of the RF field delivered to the ion.

A key effort in this program was focused on the development of new material and packaging platform that would mitigate the scalability and noise issues in the conventional surface ion traps. This effort was led by Chuan Seng Tan's team at the Nanyang Technological University, in collaboration with Hong Yu Li's team at the Institute of Microelectronics (A*STAR, Singapore) and Luca Guidoni's team at the Université de Paris. First, the team developed surface ion traps on glass and demonstrated significant improvement in its noise performance. Then the team demonstrated the 3D ion trap using the trans-silicon-via technology that led to a significant reduction of the ion trap area. The developed devices were tested in actual trapping experiments so that $^{88}Sr^+$ ions can be trapped for 30 min [26], while, one $^{88}Sr^+$ ion can be trapped for 12 h [44]

2.1.1. Surface ion traps fabricated on glass substrate

Although the microfabrication involved in creating the planar ion-trap chips relies on standard CMOS silicon processing and packaging technologies, material and size variations in electrodes that form the planar ion-trap architecture could lead to undesirable ion drifts, which in turn contribute to measurement noise that degrades the performance of the quantum register [6]. The team's approach in addressing this challenge was to fabricate ion traps on glass substrates instead of Si. Because of the superior electrical properties of glass, namely ultrastable high electrical resistivity and low dielectric constant, it is reasonable to expect a more efficient and robust conversion of the current, flowing through the electrodes, into the trapping E-field. The team fabricated traps of identical geometry on glass and Si substrates using the conventional CMOS technique and performed a thorough comparison. The ion traps fabricated on glass demonstrated superior parameters compared to those fabricated on Si. In particular, on-glass traps yield the Q factor greater than 900 in comparison to traps fabricated on silicon substrates with Q factors ranging from 20 to 300. The corresponding RF insertion losses were reduced to 0.2 dB for the glass trap, compared to values of 1–4 dB for traps fabricated on Si. The overall performance of the fabricated traps was verified by reliable trapping $^{88}Sr^+$ ions [45].

2.1.2. TSV integrated ion traps

The subsequent effort was focused on decreasing the footprint of ion traps and their parasitic capacitance. Instead of wire bonds, the team used through-silicon vias (TSV) and micro-bumps to deliver the DC/RF signals to the ion trap chips (see figure 1 left). Instead of gold (Au) filled TSVs and AuSn bumps demonstrated by researchers from Georgia Tech and Honeywell [46], Cu-filled TSV and CuSn micro-bump were used for compatibility with the mainstream back-end of line CMOS processes. The fabricated TSV trap demonstrated a remarkably low capacitance between an RF and the central DC electrode of 3 ± 0.2 pF, while that for the wire-bonded trap was 32 ± 2 pF [26]. This also resulted in higher power spectral density of >10 W/MHz and a much lower insertion loss of 0.1 dB at 50 MHz, compared to wire bonded traps with insertion losses of 2.2 dB at 50 MHz. By eliminating wire bonding pads, the team achieved an area reduction of up to 95% for TSV traps as compared to conventional wire-bonding interconnects without compromising the trapping performance. In the future, this approach will provide greater flexibility in managing the circuit complexity concomitant with scaling up the device density. Mastering this materials engineering step for the TSV trap enabled the team to demonstrate the trapping of one $^{88}Sr^+$ ion qubit for 30 min (see figure 1, right), which is sufficient for elementary quantum computing operation [26].

2.1.3. Future directions

As the next step in the development of an integrated platform for ion trapping, the team is looking at the multi-module integration of TSVs, photonics, and planar ion traps [47]. To this end, the team fabricated and characterised (focusing spot size, coupling efficiency, beam profile) multi-wavelength grating couplers for the optical addressing of ion qubits. The grating couplers were integrated into the ring trap structure, which was fabricated on the same chip. The successful integration and optimisation of these components will no doubt require new know-hows in materials interfacing and processing. Such an approach allows relatively straightforward scaling of the number of components for trapping of multiple ions (prototypes for trapping at least eight ions have been fabricated [44]) for scalable multi-qubit quantum computing applications.

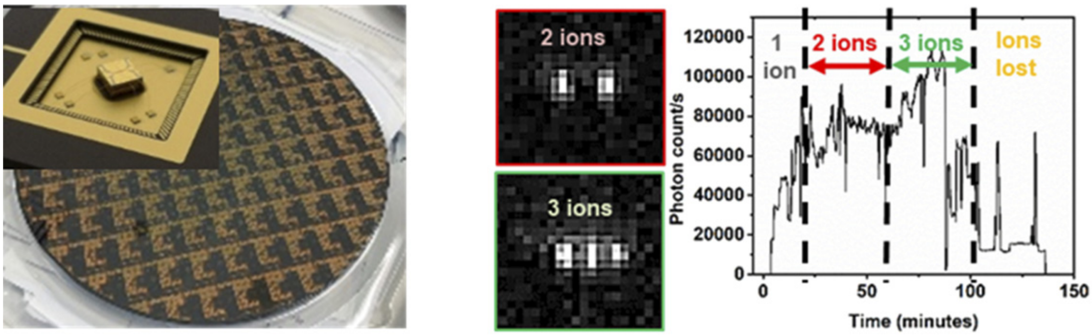

Figure 1. (Left) The TSV ion-trap fabricated on the wafer scale in a CMOS compatible process and (right) the result of the trapping of three ions in the planar trap, fabricated on the glass substrate via CMOS process (courtesy of Prof. S C Tan).

We have thus demonstrated that challenges in the scaling of ion trap systems could be efficiently addressed by co-designing and co-fabricating hybrid electrical-optical interposers entirely based on CMOS technology. This approach will satisfy the requirements (such as footprint, RF dissipation, efficient optical addressing, etc.) that cannot be accomplished with conventional packaging or monolithic integration. If successfully integrated for qubit operations, it will enable true miniaturization and manufacturability of future quantum computers based on the economy of scale, very much like the scaling of silicon electronics as described by Moore's law.

2.2. Materials engineering for spin–valley qubits

In this work, the group of K E Johnson Goh at the Institute of Materials Research and Engineering (A*STAR, Singapore) explored the development of qubits in two-dimensional (2D) quantum materials based on TMDCs such as MoS_2 and WS_2 [27, 38]. Unlike graphene, which lacks an intrinsic bandgap and has negligible spin-orbit coupling, the 2H phase monolayer of such TMDCs possesses an intrinsic direct bandgap with strong spin-orbit coupling and valley-protect spins [48, 49]. Such van der Waals materials possess the natural quantum confinement of carriers in 2D, inherent semiconductor nature without the Moore's law limitations of silicon, and importantly indigenous valley-protected spins for long-lived qubits and strong spin-orbit coupling for fast gate operations. Indeed, these advantages have now spawned a number of novel proposals for new qubit candidates based on 2D TMDCs [37, 50, 51]. The aim is therefore to utilize these advantages in 2D TMDCs, in conjunction with state-of-the-art nanolithography, to build electrically gated quantum dot devices that will act as qubits.

In building up the capabilities for investigating 2D TMDC as a new qubit platform, the strategy was to tackle the dual challenges of materials development and device fabrication simultaneously. The original roadmap of Goh's team determined material development with the co-development of characterisation instrumentation for expedient feedback to be an essential facet of the project in order to enable rapid targeted development [38]. Interestingly, this is also a key recommendation in the recent review by de Leon *et al* [6]. In what follows, we shall briefly describe the materials development and the associated feedback instrumentation, highlighting the key device fabrication steps leading to the first gate-controlled quantum dot demonstration in 2D TMDC using scalable materials, which is recently reported in a research article [52].

The fundamental attraction for using 2D TMDCs as a qubit platform is the coupling of opposite spins to the K and K' valleys at the band edges by virtue of the inversion breaking in the 2D crystal comprising of unit cells with two dissimilar atom types (a transition metal M atom, and two chalcogen X atoms). This unique spin–valley coupling allows for direct access and control of the valley degree of freedom for carrying information since a specific valley may be addressed directly via the spin allowed to occupy the valley (see figure 2 top-left sub-figure). This allows for direct interaction with the valley state through manipulating its coupled spin by external electric, magnetic or electromagnetic (light) fields. In addition, the large spin-orbit interactions in 2D TMDCs imply efficient interactions to external fields, which is attractive for fast device operations. Indeed, these ready attributes of the 2D TMDC semiconductors have motivated the more general field of valleytronics which promises new ultralow-power devices, and the direct bandgap in monolayer TMDC implies opportunities for novel opto-valleytronics applications [48, 49]. For quantum computing, this spin–valley coupling is expected to offer enhanced coherence lifetimes since the scattering of a spin from the K to the K' valley would require a concomitant spin-flip. In other words, a change in the spin–valley state requires spin and valley indices to change simultaneously—akin to a two-factor unlocking security system. While this is seen as advantageous, the manipulation of such spin–valley states has thus far remained predominantly theoretical and viewed as an experimental holy grail. To exploit such spin–valley states inherent in 2D TMDCs [37, 50, 51], the materials processing and device fabrication steps must preserve the 2D crystal ideally in a

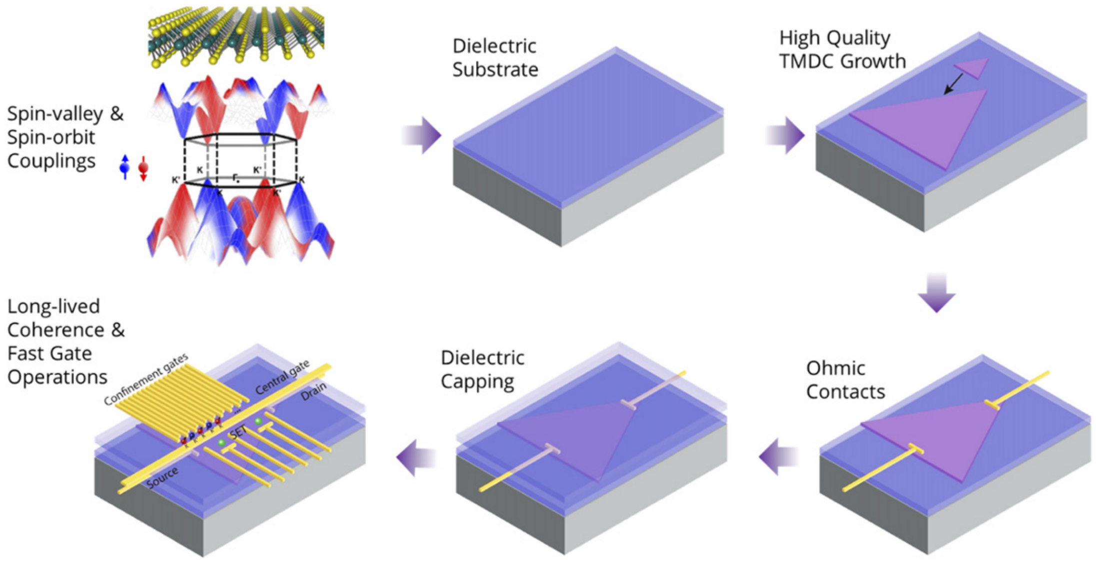

Figure 2. Two-dimensional TMDCs with intrinsic spin–valley and strong spin–orbit coupling offer a platform for realising robust qubits with long coherence lifetimes and fast gate operations. A schematic process showing the key steps towards fabrication spin–valley qubits. Top-left: stick-and-ball representation of a typical 2H TMDC monolayer crystal with corresponding 3D band structure showing K and K' valleys with their allowed spin occupants. Figures courtesy of H Kawai (crystal and band structure) and C P Y Wong (device fabrication schematic).

'material vacuum' with the only access to qubit states via designed control electrodes. This is a material science and engineering challenge.

Amongst the first capabilities built in Goh's labs were two characterisation techniques that specifically allowed us to access the degree of valley selectivity in 2D TMDC materials—circular dichroic photoluminescence, and spin- and angle-resolved photoemission spectroscopy (ARPES) [38, 53, 54]. The presence of such valley selectivity assures the spin–valley coupling/locking remains a feature we can exploit in the material.

The first technique was circular dichroic photoluminescence spectroscopy which enables the use of circularly polarized light of opposite helicity to selectively excite electron–hole pairs (excitons) in either the K or K' valleys of monolayer TMDCs [38]. These measurements provide the degree of valley polarisation, which is a proxy indication of how well spin–valley coupling is maintained in the material. The lack of or low degree of valley polarisation is typically attributed to relaxation pathways because of defects, interfaces and factors that degrade the 'material vacuum' around the 2D TMDC crystal. This technique was used to rapidly screen our TMDC materials (exfoliated or grown) before using them, after lithographic patterning, and after capping with thin dielectric layers. In addition, it was also useful for elucidating the role of defects (within the material, or at contact interfaces) on exciton recombination, and the population exchange between excitons and trions in such 2D TMDCs under the influence of an external electric field, such as those typically experienced in devices under the application of a gate voltage [54].

The second technique developed was ARPES housed in a lab-based system in proximity to our growth systems for rapid materials analysis [38, 53]. This system directly probes the ground state band structure of the 2D TMDC crystal and includes a Mott spin-detector which allows us to discriminate between spin-up and spin-down bands [27, 55]. This is particularly useful for characterising larger crystals and provides a useful indication of the degree of azimuthal disorder in monolayer TMDC films. Such assessments again assure the starting quality of the material before spending effort to fabricate devices, and we have recently shown that it is possible to deduce a ballpark estimate of the carrier mobility from such assessments without having to first fabricate a device [56].

With these materials screening or assessment tools in place, it was then meaningful to establish a materials optimisation cycle to achieve high quality large single crystals on the wafer scale. To that end, we employed the standard chemical vapour deposition (CVD) method for scalable materials development as detailed in references [38, 56–60].

For device fabrication (figure 2), we transferred the CVD grown 2D TMDCs onto standard commercial silicon wafers with high-quality grown oxide to provide the supporting dielectric. Standard electron beam lithography enabled the device patterning and contact metallisation before low temperature atomic layer deposition was applied to cap the 2D TMDC with a high-K dielectric such as HfO_2. Top-gates were subsequently patterned over the dielectric to allow the electrostatic definition of quantum dots which will host the spin–valley qubits, and single-electron transistors for sensing the qubit states. In addition, radiofrequency strip lines may be laid as appropriate to control the qubits. These details are schematically represented in figure 1 and may also be found in other published works [27, 59].

To date, Goh and collaborators have shown the possibility to make efficient metal [59] and ferromagnetic [61] contacts for charge and spin injections into 2D TMDCs, respectively. In particular, the collaboration of Goh's group with Chhowalla's group (Cambridge, UK) exemplifies the leverage afforded by an international collaborative effort to expediently apply the new concept of indium alloy contacts (pioneered in Chhowalla's laboratory) to Goh's quantum devices to achieve record low contact Schottky barriers [59]. These efforts enabled Goh's team to speed up device development culminating in the recently demonstrated gate-controlled quantum dot device in 2D TMDC using scalable materials [62]. While these are encouraging developments, the lack of consistent high-quality large scale 2D TMDCs severely limits reproducibility. In addition, the presence of defects and interface roughness in these devices induces charge noise which compromises the quantum dot performance, as well as augments qubit-to-qubit variations. While the physics background for such devices has been laid, the materials engineering know-how required to obtain consistent high-quality 2D TMDCs remains elusive. Current defect densities and interface traps in CVD grown 2D TMDCs are of the order of 10^{12}–10^{13} cm^{-2}. This limits the carrier mobilities [56, 59] to the order of 10–100 cm^2 V^{-1} s^{-2} which is significantly below the highest mobilities of ∼1000–10 000 cm^2 V^{-1} s^{-2} attained in exfoliated TMDC materials that are well-encapsulated between hBN dielectrics [63, 64]. High quality grown 2D TMDCs are urgently needed and optimised dielectric encapsulation processes that limit the interface traps formed with surrounding dielectrics need to be pursued in a scalable manner. Goh's team recently showed that material interface roughness associated with the dielectric substrate supporting the 2D TMDC can significantly compromise the quantum dot and hence qubit quality [62]. Whilst we do expect valley protection of the spin in these 2D TMDC monolayers, it remains to be seen if isotopic purification of the growth precursors for the TMDC growth and also for the surrounding dielectrics would be required to suppress hyperfine coupling to atoms with non-zero nuclear spins which could decohere the spin-based qubit. Further optimisations and developmental engineering are currently underway to address these open questions and hopefully demonstrate a first qubit on 2D TMDCs.

3. Materials for quantum photonic systems

Solid-state quantum systems are promising candidates for the realization of essential elements of quantum computers, quantum sensors, and quantum communication networks. Several solid-state systems have become useful in this field, including optically active quantum dots, and NV centres in diamond [65, 66] to name a few. Integration of solid-state quantum systems with photonic circuits complements this research and leads to the development of miniaturised, high-performance, and low-cost devices for practical applications.

Currently, there are two broad challenges in the field. The first one is associated with the engineering of solid-state quantum systems themselves. Ideally, the quantum emitter should have a long coherence time, a high and stable emission rate, and the ability to generate photon-photon or spin-photon entangled states [67]. For the trapped ion and NV centre, the challenges lie in the integration and relatively low generation rate. For quantum dots, the challenge is the short coherence time. Silicon carbide (SiC) has the potential to overcome the two challenges with a high generation rate of spin-photon entangled state and long coherence time, but the engineering of quantum emitters in SiC is relatively immature.

The second challenge is associated with integrating quantum emitters with photonic networks. The efficient coupling of single-photon emission into the photonic mode requires accurate positioning or targeted creation of the emitters in proximity (sub 100 nm) to the photonic structure (waveguide or cavity). Furthermore, one has to ensure that the properties of the emitter are not degraded during the fabrication of quantum photonic devices [68, 69]. Numerous techniques have been developed to integrate quantum emitters with photonic structures. They include random dispersion of quantum dots or diamond nanoparticles on the photonic chips [70, 71], targeted creation of the emitters in diamond by irradiation and annealing [72, 73], laser writing of defects in diamond [74], pick and place using an atomic force microscope (AFM) tip [75, 76], to name a few. However, a truly scalable method that would enable efficient interfaces between high-quality quantum emitters and the photonic network is still missing.

The group of Weibo Gao at the Nanyang Technological University (Singapore) was focused on studies of negatively charged silicon-vacancy nitrogen (NV) centres in SiC. NV-centres in SiC combine advantages for both diamond-based NV-centres and quantum dots. Like the case of quantum dot materials, the technique for wafer-size growth and doping technique for opto-electrics is fully developed for SiC, and both epitaxial and bulk materials are available. Furthermore, the colour centres in SiC all show long coherence times [77, 78] similar to NV-centres in diamond. Therefore, the combination of NV-centres and SiC is a good marriage of 'a great material' (fabrication friendly) and 'a great defect' (long coherence time).

Gao's team developed a recipe for creating single NV-centres in SiC via nitrogen ion implantation [79]. The team measured the photon statistics of the emission and proved the creation of single vacancies. Then, the team measured optically detected magnetic resonance to resolve the energy spectrum of the NV-centres, followed by the measurements of Rabi and Ramsey fringe for these defect spin states. With the Ramsey experiment, a dephasing time of 388 ns was resolved, which is comparable to other defects in diamond and di-vacancy in SiC. A much longer coherence time for single NV-centre can be achieved in subsequent experiments on single NV spin manipulation. This would require efforts to realize single NV integration into nanostructures, including solid immersion lenses or nanocavities. This work is ongoing in Gao's group.

Looking at the alternative material systems, Gao's group identified the mechanism of infrared luminescence from Ga^{+} ions implanted in GaN. The infrared luminescence was enhanced by the electron beam irradiation, which implies the conversion of non-luminescent Ga^{+} ions to luminescent neutral Ga atoms. The emission spectra and dynamics were characterized with a time-resolved cathodoluminescence electron microscope. The findings are relevant to the realization of fibre-based quantum cryptography systems, which require telecom range single photons for low-loss transmission through the fibre network [80].

Integration of solid-state quantum emitters with resonant photonic structures has been pursued by several groups in Singapore. The team of Leonid Krivitsky the Institute of Materials Research and Engineering (A*STAR, Singapore) aimed to couple the SiV centres in nano-diamonds with the SiN micro-ring cavities. A critical requirement for achieving this goal is the ability for precise positioning of the nano-diamonds in the close vicinity of the maxima of the optical field in the cavity. By default, the optical field is constrained in the core of the waveguides, and the nano-diamond, positioned at its surface, can only experience a weak evanescent field. To overcome this issue, the team proposed creating a tiny dent (using the focussed ion beam) in the waveguide, which could serve as a pocket for the nano-diamond. As a result, the interaction strength can be significantly enhanced. The nano-diamond was positioned in the pocket using the tip of the AFM. The team achieved the positioning accuracy better than 100 nm, which is sufficient for interfacing the nano-diamond with the nanophotonic cavity [81].

Nanoscale photonic phenomena can be also exploited to enhance the performance of solid-state quantum sensors. Krivitsky's team studied the application of commercially available single-crystal diamond AFM tips for magnetometry. The team discovered that commercial single-crystal diamond AFM tip contains a large concentration of NV and SiV-centres. The optical signal produced by the vacancies can then be used to read out the local magnetic field and temperature. The team modelled the distribution of optical fields in the AFM tip and found that the signal is enhanced due to the combination of the cavity and light guiding effects in the tip. This was confirmed experimentally with the observed $8\times$ improvement in the intensity of the collected fluorescence signal from the AFM tip. These findings open additional exciting applications for commercial diamond AFM tips in nanoscale measurements of magnetic field and temperature [82].

Towards a mature quantum photonic platform, the collective efforts presented here represent significant advances in the development of a scalable on-chip quantum source, which will be the critical component in a large-scale quantum network. This chip will combine multiple SiC spin and photon nodes with microwave carriers and photonic waveguides. Such a chip will be the central element in a large-scale quantum processor, including quantum source, quantum bus, and photon detections. As we advance, the remaining issue that needs to be addressed is the generation of a larger entangled state by photon interference with photons from different nodes, either on a chip or in a distant location. Furthermore, the challenge remains in the integration of the large-scale quantum photonic chips with classical I/O, quantum buses and highly efficient photon detection on chip.

4. Materials for quantum optics

Applications in quantum communications and networking require the transmission of quantum signals, encoded in single photons, through optical fibres for hundreds of kilometres [83]. However, most of the quantum registers, such as trapped ions or quantum dots, emit photons in the visible part of the spectra, which is too lossy to be transmitted through the telecommunication fibre network, optimized for operation in the near-infrared range. Hence significant interest in the quantum optics community is focused on the realization of compact (chip-scale) and efficient ($\sim$10% internal conversion efficiency) devices for frequency conversion, which can be used as 'photonic gearboxes,' see figure 3 (left). These nonlinear devices are also used for the generation of quantum states of light (entangled photons and squeezed light), which are needed for realizing quantum cryptography, metrology, and sensing, see figure 3 (right).

Nonlinear properties of bulk materials can be significantly enhanced using micro- and nanostructures, artificially created via advanced nano-fabrication techniques. This approach allows combining high material nonlinearity, strong field confinement, and a compact footprint to enable the highest efficiency of frequency conversion.

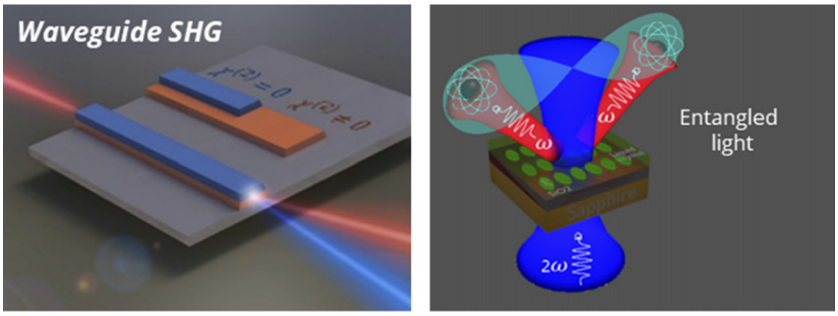

Figure 3. Schematic illustration of light frequency conversion in the waveguided (left) and metasurface (right) optical devices fabricated from GaP and used for SHG and for the generation of entangled light (courtesy of Aravind Padath).

Krivitsky's team focussed on the development of resonant photonic structures made of gallium phosphide (GaP). GaP is an attractive material due to its beneficial optical performance (high nonlinearity, transparency in the broad optical range) and manufacturability considerations. The team bonded GaP film to the low-index Sapphire substrate and then fabricated waveguided (planar) optical devices, see figure 3 (left). Furthermore, since the sapphire substrate is transparent in both visible and IR ranges, the GaP wafers, developed by the team, can be used in the transverse geometry, see figure 3 (right). This approach enables the development of flat nonlinear optical components, known as nonlinear metasurfaces.

As a first step in understanding the nonlinear functionalities in GaP waveguide devices, the team performed a SHG experiment [28]. The effective modal phase matching between the fundamental and converted waves was achieved through the variation of the geometrical parameters of the device. The reported devices exhibited an internal SHG efficiency (0.4% W^{-1} cm^{-2}), which, however, was still an order of magnitude lower than the theoretical estimates (6.1% W^{-1} cm^{-2}). The likely reason for this discrepancy was high optical losses in the waveguide due to the roughness of the top layer of GaP. To circumvent this issue the team, led by Jason Png, came up with an alternative design based on the concept of bound-state-in-continuum (BIC) [84]. This approach obviates the need for nanofabrication of nonlinear material, but requires instead the patterning of a low-refractive-index strip on top of the nonlinear slab. Using GaP as a nonlinear material and the fundamental BIC mode, the team theoretically shown a theoretical conversion efficiency of 1.1×10^4 W^{-1} cm^{-2}. This value is comparable to theoretical estimations obtained for conventional GaP waveguides, yet it is much easier to fabricate. The experimental realization of these devices is underway.

In collaboration with the groups of Arseniy Kuznetsov and Ramon Paniagua, both at the Institute of Materials Research and Engineering (A*STAR, Singapore), the QTE team designed and fabricated GaP resonant metasurfaces for the SHG [30]. The resonant enhancement in metasurfaces is based on the concept of the BIC, which theoretically has an infinite Q factor as the resonant mode is 'trapped' within the structure. The structures are formed by arrays of sub-diffraction ellipse-shaped particles oriented in a specific direction. The disturbance of the symmetry of the particle orientation breaks the symmetry and opens leaky channels for the radiation state to couple light into the resonant states of these structures. Tuning the symmetry of the structure changes the Q-factor, thereby making these structures ideal for both pulsed and CW laser conversion. The team fabricated samples with different mutual orientations of GaP nano-ellipses (5, 10, 20, and 30 degrees). Then the BIC resonance in these structures was used to enhance the efficiency of the SHG process in the 1200 nm wavelength range. As it was expected from the theory, the highest value of the conversion efficiency was observed for the metasurfaces with nearly symmetrical orientation of nano-ellipses (at 5 degrees), as it corresponds to the BIC mode with the highest quality factor. Using these structures, the team demonstrated the record high efficiency of the SHG in dielectric metasurfaces with both CW and femtosecond lasers.

As the next step in the practical adoption of metasurface devices, the group of Nikolai Zheludev at the Nanyang Technological University (Singapore) integrated the metasurface made of amorphous silicon on the tip of the optical fibre. The SHG signal, produced by the metasurface, was directly collected by the fibre, thus eliminating the need for bulk optical components. The metamaterial in the form of a double-chevron array supports a closed-mode resonance at the telecommunication wavelength of 1550 nm and has a quality factor of about 30. The experimentally demonstrated SHG efficiency normalized to intensity and square of interaction length was two orders of magnitude higher than the value demonstrated for a silicon metamaterial [85].

The technical capabilities of the Singapore team in the design and fabrication of nanoscale optical devices attracted strong interest from collaborators who are working on various optical phenomena. In collaboration with the group of Stefan A Maier from the Imperial College London, GaP metasurfaces were used to demonstrate ultrafast optical modulation via the optical Kerr effect and two-photon absorption. The teams showed that a GaP nanodisk yields modulation of reflectivity coefficient of up to ∼40% in the visible and near-IR ranges. The temporal scale of modulation was demonstrated to be between 14 and 66 fs. The demonstrated devices outperformed the state-of-the-art concepts which reached the modulation depths no larger than 0.5% for sub 100 fs optical switching, suggesting GaP nanoantennae as a promising choice for ultrafast all-optical modulation [86].

In collaboration with the group of Mara Chekhova from the Max Planck Institute for the Science of Light, the teams reported the experiment on the generation of correlated photons (biphotons) via spontaneous parametric down-conversion (SPDC) from subwavelength GaP films pumped by a continuous wave visible range laser [29]. The photon pairs generated in lithium niobate and GaP nanofilms demonstrated a high coincidence-to-accidental ratio (∼700–1000) and an extremely broad spectrum (over 500 nm of bandwidth, spanning from 810 nm to 1350 nm), which was further enhanced by a Fabry–Perot effect in the film. This work laid the foundation for the future development of compact SPDC sources based on nonlinear metasurfaces, with the first demonstration published shortly after that work [87].

In collaboration with the group of Gennady Shvets from Cornell University, the team demonstrated a GaP metasurface for highly efficient high harmonic generation (HHG) with a very high damage threshold and low reabsorption. The HHG was driven by strong mid-infrared laser pulses and the HHG signal (up to the ninth harmonic) was observed in the visible and near-IR ranges, with an energy span between 1.3 and 3 eV. The metasurface consisted of domino-like nanostructured elements (nanoantennae) that supported the electrical dipole resonance at the pump wavelength of 3.95 μm. The conversion efficiency was enhanced by the metasurface resonance to the degree that it even allowed the single-shot measurements avoiding damage to the material, thus providing the possibility to study the controllable transition between the perturbative and non-perturbative regimes of light-matter interactions at the nanoscale depending on the pumping conditions [88].

5. Conclusion and perspective

We have given an overview of the recent quantum materials engineering efforts in Singapore. We show the deliberate intent by various groups to address the materials related gap that currently impedes technology translation progress for quantum computing and sensing applications. The key advances highlighted include the co-development of materials processes with their concomitant quality assessment instruments to provide timely feedback for more rapid optimisation cycles, and the exploration of new materials as options for qubits and sensors. Furthermore, the advanced material processing capabilities reveal exciting new functionalities of quantum devices that lead to high fidelity, compact footprint, and potential for mass production.

In the context of quantum computing, new materials processes will be needed to address key challenges of environmental hygiene (reduction of charge and spin noise as relevant), process control, and material interfaces. These will enable high-quality qubits and qubit-to-qubit variations to come within engineering tolerances to make scale-up feasible. It remains unclear if these challenges could be solved for the incumbent qubits, including the small scale NISQ processors that have been engineered into full stacks by the industry. The joint efforts by the teams under C S Tan and H Y Li tackled the materials challenges for ion-trap qubit engineering and showed promising on-chip ion trap lifetimes using a scalable interposer technology. The focus and investments now on quantum materials research and engineering could fortuitously uncover new material options for qubits or related engineering needs which may lead to a faster route to universal gate-based quantum computing. The team under K E J Goh developed the key materials development and qubit fabrication capabilities for spin–valley qubits based on the new 2D TMDC platform and has made key progress in materials screening, device contacts, and quantum dot fabrication.

In the context of quantum sensing and communications, new materials and corresponding processes are the key enablers for devices that can be fabricated at scale and deployed in real applications. W Gao's team developed the techniques for creating colour centers in SiC and single-photon emitters operating at telecommunication wavelengths. L Krivitsky's team developed an integrated GaP photonic platform for efficient light frequency conversion for applications in quantum communications and sensing. The integration of the novel photonic components with optical fibres was demonstrated in groups of N Zheludev and C Soci.

Just a decade ago, quantum devices that exploit superposition and entanglement were mainly in the proof-of-concept stages with primarily laboratory-based demonstrations. The strategic importance of quantum materials engineering targeted at exploiting these effects cannot be overstated. Concerted efforts to leverage the capabilities have accelerated internationally, and this article highlighted the inroads made by various research groups in Singapore in the area of quantum materials engineering. Global developments have been fervent with increasing investments in quantum technologies by both governments and industries alike. Traditionally, the field of quantum technology saw participation mainly from physicists, complexity theorists, engineers and computer scientists, and quantum chemists. Increasingly, the quantum community is acknowledging the need for materials scientists and engineers to join the fold to solve the scale-up problems [4, 6, 89]. It is opportune now for materials experts to make a material impact on quantum engineering.

In conclusion, the significant investments in quantum materials research have provided key insights and made ready a materials technology springboard for the quantum ecosystem to expand and benefit from the new quantum advantages that lie just ahead.

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Data availability statement

No new data were created or analysed in this study.

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