DYNA Ingeniería e Industria	GENERALIZATION OF C++-BASED DSP SOFTWARE FOR VOLTAGE SOURCE REGULATION AND CONTROL OF DIVERSE POWER CONVERTERS IN PARTICLE ACCELERATORS	Electronic technology
RESEARCH ARTICLE	Nagore Pinillos, Louis de Mallac, Serge Pittet, Darjiusz Jakub Zielinski, Edorta Ibarra, Raul Murillo-Garcia, Iñigo Martínez de Alegría	3307.99 Others

GENERALIZATION OF C++-BASED DSP SOFTWARE FOR VOLTAGE SOURCE REGULATION AND CONTROL OF DIVERSE POWER CONVERTERS IN PARTICLE ACCELERATORS

Nagore Pinillos[1], Louis de Mallac [1], Serge Pittet [1], Darjiusz Jakub Zielinski [1], Edorta Ibarra [2], Raul Murillo-Garcia [1], Iñigo Martínez de Alegría [2]

[1] Accelerator Systems Department (SY), Electrical Power Converters Group, CERN, 1211 Geneva (Switzerland)

[2] Universidad del País Vasco (UPV/EHU), 48013 Bilbao (Spain)

DOI: https://doi.org/10.52152/D11247 | Received: 16/abr/2024 • Reviewing: 23/abr/2024 • Accepted: 12/aug/2024

To cite this article: PINILLOS-ZAMORANO, Nagore; De Mallac, Louis; PITTET, Serge; Zielinski, Dariusz Jakub; IBARRA, Edorta; MURILLO-GARCIA, Raul; MARTÍNEZ-DE-ALEGRÍA, Iñigo. GENERALIZATION OF C++-BASED DSP SOFTWARE FOR VOLTAGE SOURCE REGULATION AND CONTROL OF DIVERSE POWER CONVERTERS IN PARTICLE ACCELERATORS. DYNA. March-Abril 2025. Vol. 100, n.2, pp. 137-145. DOI; https://doi.org/10.52152/D11247

ABSTRACT:

Large particle accelerator facilities such as the one at The European Organization for Nuclear Research (CERN) are good examples of complex systems where a large variety of switched power converters coexist to feed the acceleration systems. Over the years, the low-level voltage source regulation software has evolved in a decentralized manner, making it repetitive and difficult to test, debug and maintain. As reliability is of capital importance, this work investigates the similarities between various representative power systems and their converter-specific software, named CANCUN (Cern Acdc Narrow CoNverter), HL-LHC18kA (High Luminosity Large Hadron Collider 18 kA) and RF3kA (Radio-Frequency 3 kA). Then, a C++ coded common control library, herein named RegDspLib, is proposed to make software generalization possible, taking advantage of Object Oriented Programming (OOP). Among the library's features, the re-factorization includes a unified control state machine. The proposal also provides digital signal processor's (DSP) resource utilization reduction. Modifications over the interrupt handling and generalization of pulse width modulation (PWM) modules through parametrization are also investigated. Finally, experimental results showing the correctness of the proposal are presented. All this provides field engineers and researchers valuable information regarding voltage control software standardization, at a power electronics level, in medium-to-large particle acceleration or other complex industrial systems.

Keywords: C++, control, DC/DC converters, inverters, particle accelerators, power electronics converters, power rectifiers

1. INTRODUCTION

High-precision switched power electronics converters are of great importance in modern particle accelerator systems [1]–[8]. They supply electrical energy, directly from the grid or intermediate storage elements, to radio frequency (RF) cavities for charged particle acceleration [8], and to normal [9] or superconducting [10] electromagnets for bending (dipoles), focusing (quadrupoles) and several higher order correctors to control the trajectory of particle beams. These high-precision elements pose tight voltage and current regulation requirements in the parts-per-million (ppm) range [11], [12]. In addition, they must be highly reliable to guarantee the continuous operation of particle accelerators while not jeopardizing their integrity [7], [13]. Thus, the implementation of high-performance measurement and control systems is mandatory, both at the hardware and software levels.

The European Organization for Nuclear Research (CERN), Geneva, Switzerland, is a good example of a highly complex particle accelerator facility with a large amount of powering systems. The Electrical Power Converters group of the Accelerator Systems Department (SY-EPC) has developed more than 5000 power converters over the years. The majority of these converters act as current sources and are composed of three elements: a voltage source (VS), a current measurement system and a Function Generator Controller (FGC) [14], [15]. The FGC provides various services including function generation, current regulation and state control. Around 1500 of these power converters use a proprietary digital control electronics platform named RegFGC3 [6], [16], a control crate for switched mode power converters. Despite most of the software of this embedded converter controller is standardized (such as the code running in the FGC [17]), still, some part remains converter-specific, e.g., the C coded voltage regulation algorithm running in the RegFGC3's digital signal processor (DSP) controller. This possesses a series of drawbacks: code is duplicated, difficult to test, debug and maintain. Thus, its generalization becomes highly desirable.

In this article, the authors propose the generalization of CERN's digitally controlled switched power converters' DSP control software by developing a common control library, herein named RegDspLib. To do so, various steps are followed:

1. Analysis of common features of three representative switched power supply converters, named CANCUN (Cern Acdc Narrow CoNverter), HL-LHC18kA (High Luminosity Large Hadron Collider 18 kA) and RF3kA (Radio-Frequency 3 kA).

2. Unification of converter-specific state machines into a common one, which accounts for all operational and safety requirements.
3. Computational resource/performance analysis, taking the required actions (interrupt handling, task priorities, etc.) to guarantee reliable real-time execution.
4. Re-factorization of the control software from C to C++. Its object oriented programming (OOP) mechanisms [18] ease the expression of common features between converters, deriving code from a common base to a specific power converter in a straightforward fashion.
5. Incorporation of new functions that optimize generic control algorithm execution, such as automatic parameter calculation. Generalization of the pulse width modulation (PWM) related configuration code, understanding the PWM peripherals and accounting for the variety of modulation modes.

A multidisciplinary approach to the problem must be followed, encompassing knowledge in power electronics systems, control theory, digital electronics, and programming.

This work focuses on the generalization of CERN's proprietary power converters' voltage control software. However, authors believe that this proposal and its practical implementation details will be also of great interest to researchers and field engineers working with other medium-to-large particle accelerator systems, or even other kinds of complex industrial facilities where various power conversion architectures coexist.

2.- SWITCHED POWER CONVERTER EXAMPLES AT CERN: ARCHITECTURES AND CONTROL

In this section, three representative 1-, 2- and 4-quadrant power electronics converters, currently operating or under development at CERN, are described to show the variety of powering solutions and their differences and similarities at hardware and control basis.

2.1.- THE CANCUN POWER CONVERTER

The 4-quadrant CANCUN power converter [±20 A to ±100 A, ±30 V to ±75 V] of Fig. 1 is currently in operation, supplying dipoles working as correction magnets at the Booster, Linac3, Linac4, Proton-Synchrotron (PS), Super PS (SPS), Low Energy Ion Ring (LEIR), Isolde and Extra Low Energy Antiproton ring (ELENA) [19]. This is a fast-ramped type of power supply, providing fast output current pulses to the load.

The converter is divided into three main blocks (Fig. 1). First, an input rectification stage supplies the HV-DC link. Then, on the primary side of the isolated DC-DC module, an inverter generates AC voltage to the input of a high-frequency transformer, and galvanic isolation is provided. A rectifier at the secondary generates a low-voltage DC (LV-DC). A 4-quadrant DC/DC output stage, based on full-bridge configuration, feeds the load with the desired output voltage for tracking the load reference current.

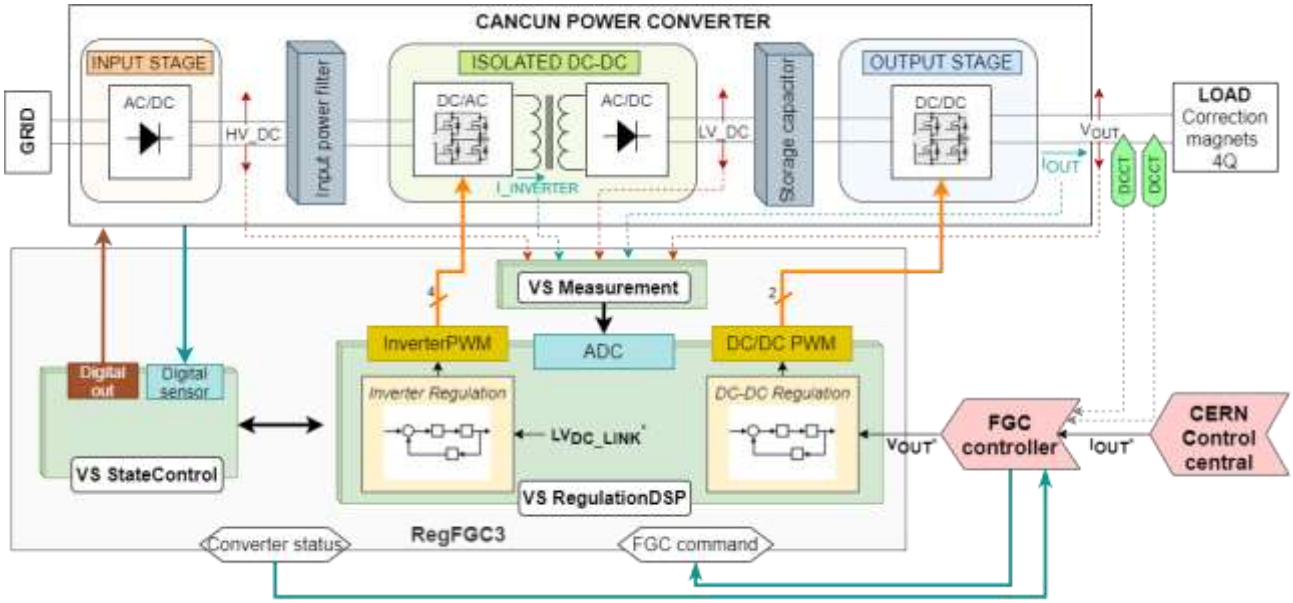

Fig. 1. Block diagram of the CANCUN power converter and its control.

The following hardware elements constitute the control electronics:

(a) The CERN control center (CCC), which commands the dipole magnet's current set-point (Fig. 1).

(b) The RegFGC3 control crate, formed from various electronics boards. For the scope of this work, the relevant boards are:

i. The embedded FGC, which receives the current set-point from CCC (Fig. 1) and two redundant load current measurements from two high precision DC current transducers (DCCT) [20]. It is responsible for managing the current loop through the implementation of an RST algorithm and for outputting the voltage reference. Within the FGC, high-precision Sigma Delta Analog to Digital Converter (ADC) digitization is used to reach ppm requirements. In general, the FGC performs high-level control by diagnosing, controlling, and monitoring the status of the power converter.

ii. The VS StateControl board, containing a Xilinx XC3S700AN Field Programmable Gate Array (FPGA) which monitors and controls the state of the power converter, controls various digital outputs (relays, contactors, etc.), and supervises digital inputs (state of the contactors) through a Finite State Machine (FSM). Both the VS RegulationDSP and the VS StateControl cards work together while receiving commands from and sending the status of the converter to the FGC main controller (Fig. 1).

iii. The VS RegulationDSP control electronics board executes the voltage loop employing a PI-based algorithm. Receives the output voltage reference from the FGC (Fig. 1). It controls the converter's power electronics stages, generating firing pulses through PWM. This hardware block includes a Texas Instruments (TI) TMS320C2834ZFET Digital Signal Processor (DSP) for closed-loop regulation, and also a Xilinx XC3S700AN FPGA, in charge of security and communication duties.

iv. The VS Measurement board provides measurements to the VS RegulationDSP board (voltages, currents and temperatures).

Regarding more specific power electronics control details, the contactors of the first input stage's pre-charge circuit need to be commanded to charge the input power filter at power-up. The output voltage of the second stage inverter is controlled in closed-loop using a PI regulator, and the resulting duty-cycle is phase-shift PWM modulated [21]. The final stage DC-DC converter is closed-loop regulated in current mode (nested outer voltage and inner current PI regulators), and a PWM modulator provides 4-quadrant operation. All closed-loop controllers include their corresponding feed-forward terms and saturation blocks to achieve desired dynamics and performance.

2.2.- THE HL-LHC18kA POWER CONVERTER

The 2-quadrant HL-LHC18kA power converter [2 kA, ±10 V per paralleled sub-converter] (Fig. A within the supplementary material) is currently under development for powering new superconducting large-aperture quadrupole magnet that will be introduced in the future high luminosity (HL) upgrade of the Large Hadron Collider (LHC) [1], [4]. The power system is multi-phase in nature due to the high current levels involved. Here, each sub-converter works with an independent digital regulation board. The control hardware electronics of each paralleled unit will be, in principle, the same as in CANCUN (RegFGC3 crate).

As opposed to CANCUN, HL-LHC18kA is a slow-ramped converter. Here, the load current is initially ramped-up slowly (14.6 A/s), then kept constant for hours, and finally ramped-down, regenerating energy [4]. The CCC sets this current reference. Again, the power supply's output voltage is externally set by the FGC.

The first two stages at each sub-converter will be similar in architecture and control to the ones of CANCUN. However, the LV-DC will supply an intermediate energy storage system based on a large capacity battery pack of 24 V. This will provide a better ride-through capability against grid faults, improving reliability (a high percentage of faults at CERN's power systems are induced by disturbances on the grid [22]). Also, it will allow independent dimensioning of the upstream and downstream converters and will make it possible to recover the up to 42 MJ energy stored in each magnet during ramp-down, achieving better efficiency [4].The main architectural difference with respect to CANCUN lies on the output DC/DC stage of the power converter, which will be composed of eight paralleled 2-quadrant DC/DC converters operating at a high step-down ratio. Their duty-cycles will be determined in closed-loop, and current balance through paralleled units will be actively regulated [4]. Well-known interleaved PWM techniques [4], [23] will be finally applied to minimize output current ripple (Figs. 2(a) and 2(c)) by interleaving the gate pulses of the power semiconductors (Fig. 2(b)) and reach the stringent ppm requirements.

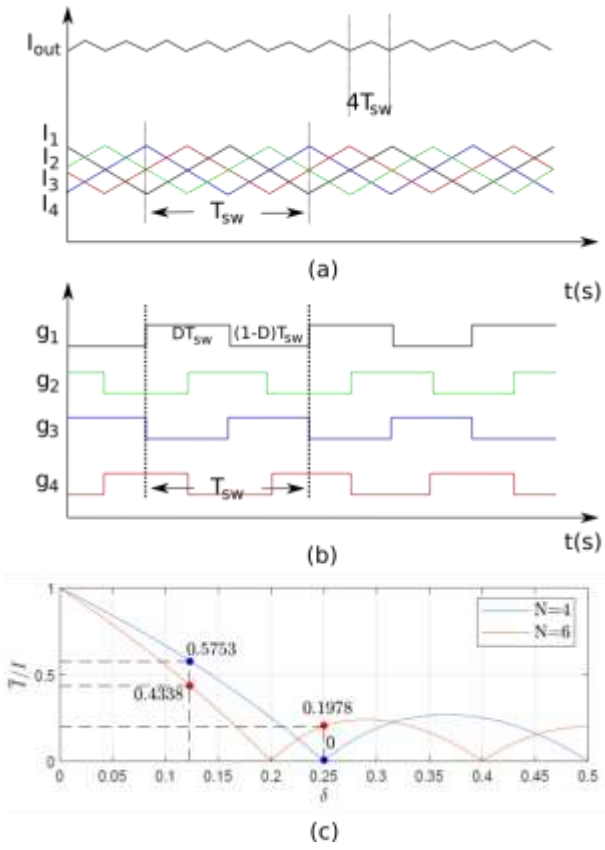

Fig. 2. (a) Qualitative effect of interleaving over total output current ripple; (b) interleaved PWM pulses, and (c) normalized current ripple vs duty-cycle for interleaved DC/DC converters [4].

2.3.- THE RF3kA POWER CONVERTER

The 1-quadrant RF3kA power converter [3 kA, 25 V] (Fig. B within the supplementary material) is also still under development, but it will be soon installed for tuning the Proton Synchrotron (PS) Radiofrequency (RF) cavities. The control hardware electronics are again constituted by the RegFGC3 crate. However, no third power conversion stage is required, as the LV-DC is directly applied to the load. In order to meet the high output current requirements, four paralleled sub-converters are installed. Thus, interleaving PWM techniques are possible for the phase-shift inverter block.

From all this analysis, it becomes clear that the three studied power converters share many of the constituent hardware blocks. However, at control software coding level, differences in the communication signals between the RegFGC3 crate's cards, diverse FSMs, a varying quantity of PWM outputs and modulation schemes, different closed-loop control algorithms, etc. can be found. Their converter-specific software meets the operational requirements, but these independently coded control solutions are not efficient from a programming point of view. Generalizing common features is desired for optimizing coding of the system.

3.- KEY ASPECTS FOR SOFTWARE GENERALIZATION

Within this context, the first steps in the development process of the RegDspLib common control library have involved fine-tuning the original control software to meet C++ refactoring needs. In this section, the main modifications are highlighted, which makes the code more structured and improves the original C code.

3.1.- UNIFIED FINITE STATE MACHINE

In the original control systems of the CANCUN, HL-LHC18kA and RF3kA converters, converter-specific FSMs are distributed and executed within two separated hardware elements of the RegFGC3 cards:

- I) The VS StateControl card (running in an FPGA). Here, the FSM is coded in VHDL. This FSM has control over faults, warnings and some digital signals of the converters.
- II) The VS RegulationDSP card (running in a DSP). Here, the FSM, coded in C, has control over the PWM outputs and the ADCs, as well as over other fault signals.

To ease the implementation of the C++ library, merging the logic of both FSMs into one single element is considered the best option. The proposed new design implies removing the FSM from the VS StateControl card, since writing it in C++ rather than in VHDL is considered more convenient for debugging, verification and maintenance. In consequence, the VS StateControl board will henceforth only be used as a signal interface between the RegFGC3's cards.

Regarding converter-specific functionalities, the states and transitions of the three studied converters are merged into a single FSM. The resultant unified FSM is shown in Fig. 3(a). This modification simplifies the system from a software point of view, making it clearer and easier to understand. For example, when running the CANCUN converter, its basic operation implies going from the precharge state of the HV-DC link capacitor to the enabling of the inverter modulation (BK command), until unblocking the output by enabling the DC-DC stage (IL command), as shown in Fig. 3(a) and experimentally illustrated in section 5.

3.2.- TIMING, INTERRUPT HANDLING AND TASK PRIORITIES

Another point to consider is managing the interrupt-triggering of the digital control. In its initial configuration, a PWM module from the DSP is used as an interrupt source. For example, the regulation loop is triggered upon a flag being generated at 50 kHz frequency for the CANCUN power converter. The interrupt signal is synchronized with the VS Measurement ADC's sampling clock so that the control algorithm execution immediately starts when a new ADC sample is available. During the remaining time allocated for these critical tasks, secondary instructions are executed, such as parameter calculations, protection functions, etc.

Following this configuration, the control algorithm demands 90 % out of the whole interrupt routine period. This makes modifying the regulation software extremely challenging, as seen in the first trials of code generalization. Applying optimization techniques is not sufficient and, in response, the finally proposed solution involves designing a multiple interrupt control system. To do so, DSP's tasks are divided into two interrupts (Fig. 3(b)). First, the original high-priority, high-frequency interrupt, now only containing critical real-time tasks, as the control algorithm. On the other hand, a newly established interrupt operates at a lower priority and frequency. It now accommodates secondary tasks that were previously part of the original interrupt, such as overseeing the converter's protection and managing communication data with the VS StateControl card. Relocation of instructions allows releasing time from the high-priority routine. In this fashion, real-time control is preserved. The next step implies selecting a source for the new interrupt. The lack of available DSP hardware peripherals as an interrupt source leads to triggering the second interrupt by software within the high-priority routine.

As a result of this task segregation, the processor is prevented from overrunning. In addition, tasks originally executed in background outside the interrupt routine (thus not in real-time nor in a deterministic way), will from now on be running within a fixed time-frame. For instance, the period of the lower-priority interrupt is set to 1 ms for the CANCUN converter, maintaining the 10 µs frequency period for the high-priority interrupt, as shown in Fig. 3(b).

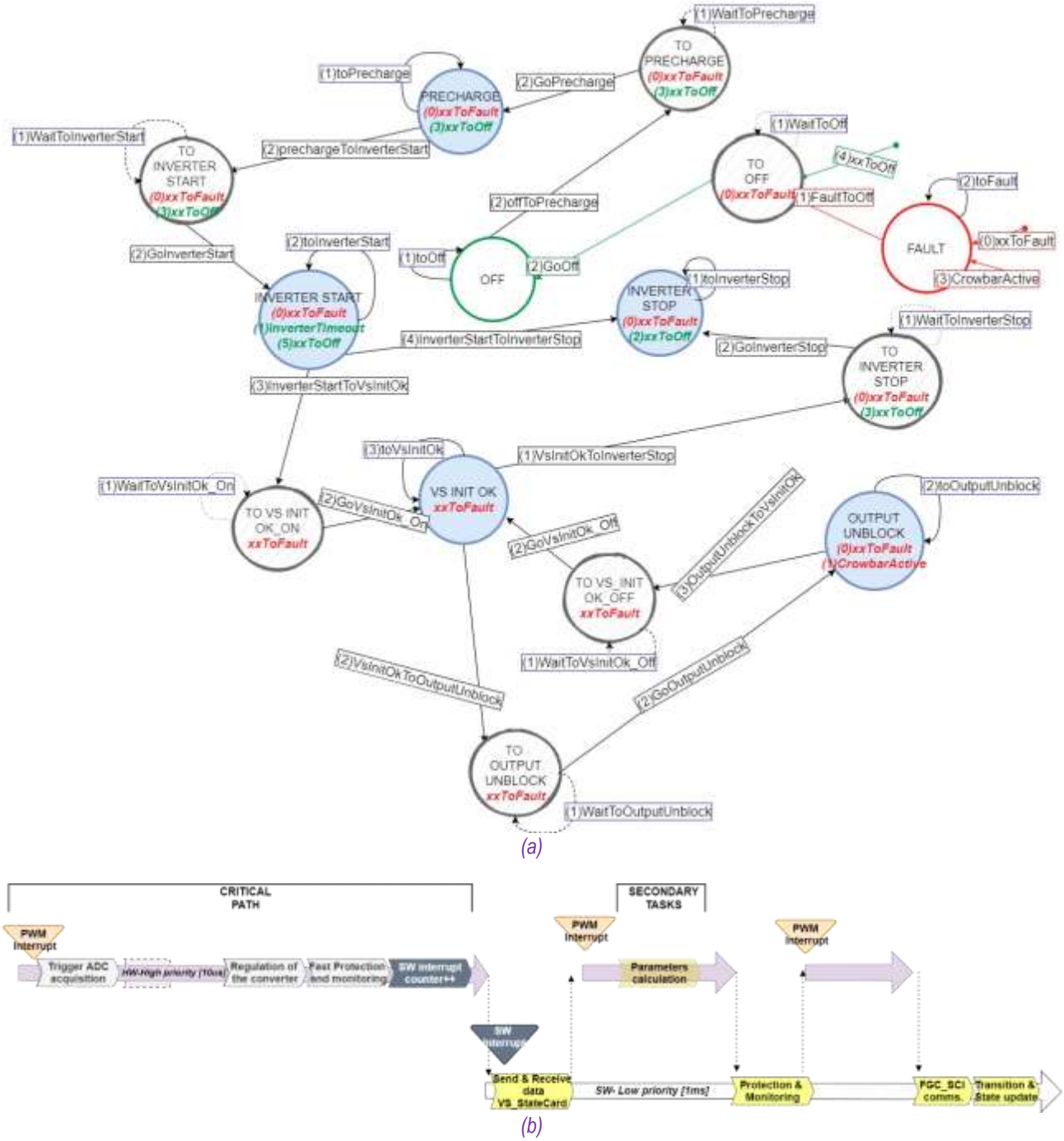

Fig. 3. Software generalization implementation details: (a) Proposed FSM for its implementation in the VS Regulation DSP card; (b) propossed multiple interrupt control system.

4.- IMPLEMENTATION DETAILS OF THE REGDSPLIB IN C++

The following section provides insight into the most relevant features of the proposed, designed and implemented-generalized control software named RegDspLib. For a better understanding, Fig. 4 provides the Unified Modeling Language (UML) Class Diagram of the developed RegDspLib C++ library. The analysis of the existing common features among power converters (section 2) has been vital to reflect them later in the software. The library is developed in C++. Since OOP organizes software around data, its naturality helps to express these relationships between converters.

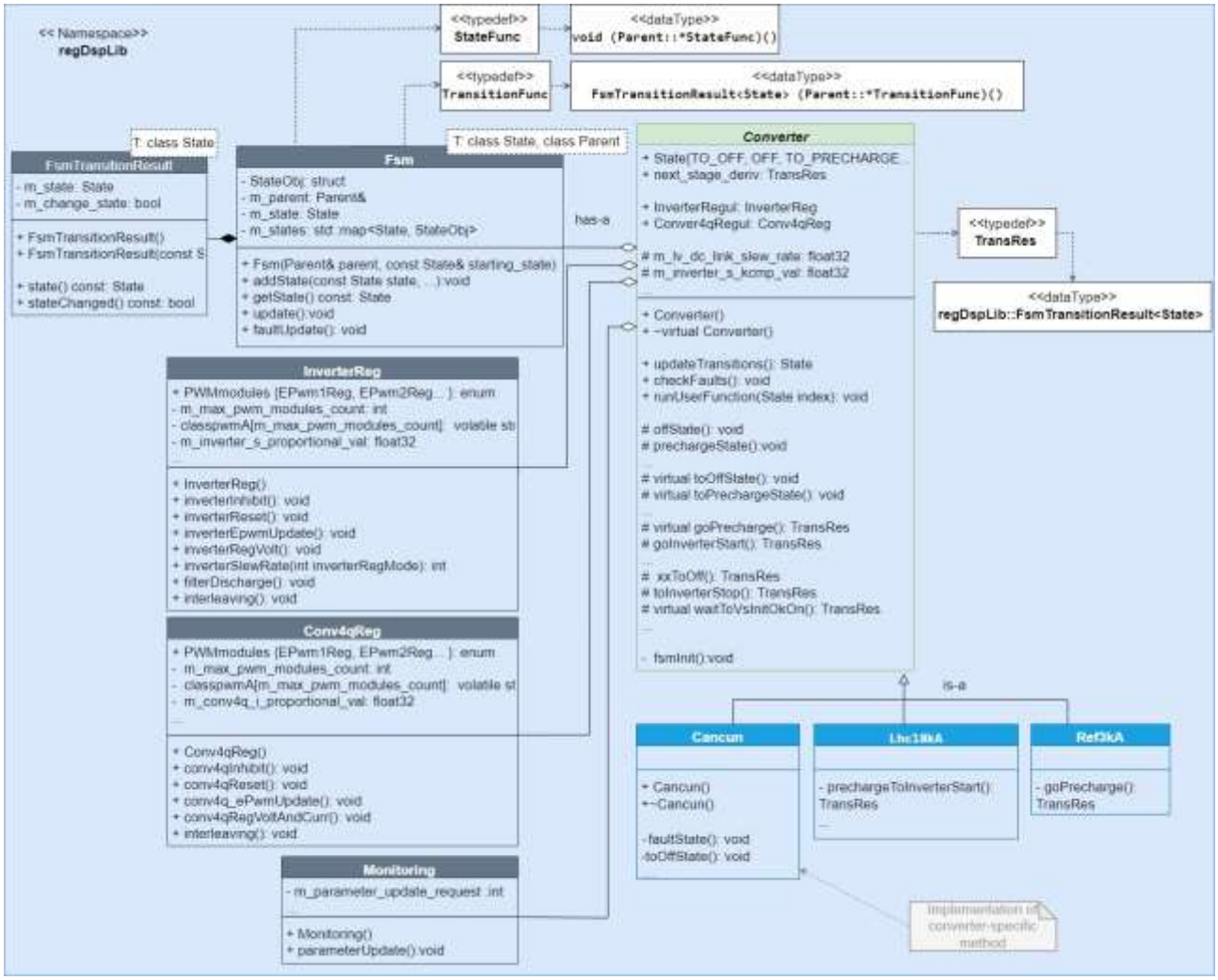

Fig. 4. UML Class Diagram of the proposed RegDspLib C++ library.

4.1.- ESTABLISHING RELATIONSHIP BETWEEN CLASSES THROUGH INHERITANCE

The first and most fundamental step involves the development of CERN's power converter generic concept within the library. This is expressed through a C++ class, from which objects can be instantiated, the building block of OOP. It is denominated "class Converter" and is defined with generic attributes (data) and methods (functions) that describe the behavior of the power converters' control.

The following stage involves setting the relationship between different converters. As in the real world, an idea does not exist in isolation, C++ inheritance mechanisms also provide the ability to relate concepts. Whenever two classes present an "is−a" relationship, the inheritance language mechanism can be used. In this work, the relationship is clear: CANCUN, HL-LHC18kA and RF3kA "are" all Converters. Since a class is used to represent the concept of a power converter, representing CANCUN, HL-LHC18kA and RF3kA without involving the notion of a converter would be missing something essential. Inheritance allows the creation of a new class from

an existing one. The former is named derived class (or child), while the latter is named base class (or parent). For the RegDspLib library, the parent class (Converter) gathers all the commonalities between converters, while the child ones (CANCUN, HL-LHC18kA and RF3kA) inherit them and can have their own additions to cover converter-specific features.

4.2.- PROVIDING LOGIC TO CLASSES: POLYMORPHISM, TEMPLATES AND COMPOSITION

Once a structure is established for the data, the logic is developed through a systematic refactoring process, transitioning the code from C to C++, module by module, while employing OOP mechanisms. This reduces the overall complexity of the program by splitting the code into simpler components.

Beginning with the FSM (section 3.1) and based on the designed standard one (Fig. 3(a)), the original C switch-case statement is refactored into an object. Following the general programming approach, the configured object is an empty machine that needs additional definitions for its states and transitions. However, it provides the behavior and tools needed to create an FSM. Hereby, a polymorphic FSM is created, since the same entity can behave differently in dissimilar scenarios. This allows the creation of a flexible state machine, in which all the implementation is hidden from the user. The states and transitions are defined when used within another class, through composition. This composition mechanism establishes a “has−a” relationship when instantiating the FSM template class (which has types as parameters) inside the class Converter. On their side, each child class can decide what to do in each state, and what conditions need to be met for a transition to occur.

Following this approach, regulation modules are also implemented within the class Converter. Two objects are created for this purpose: one to define the regulation of the DC-DC converter and a second one for the control of the inverter. The different regulation functions of the three power supplies are analyzed to create standard methods that can be encapsulated in the two regulation objects and work for all the converters. Converter-specific variances such as the PI parameters and variable values are configurable through the constructor’s input parameters. Some of the included methods are directly refactored from the original C functions, such as the regulation algorithms, the inhibit and reset methods that force the PWM outputs to either logical '1' or '0', or the update method that calculates the new modulation values after the regulation. On the other hand, some others are built from scratch. These last include, for example, a function that automatically calculates the interleaving phase values for different quantities of the converter’s output modules, or a slew-rate method to slowly increase/decrease the control command.

One of the remarkable aspects of these regulation classes comes from the programmability of which PWM modules of the DSP to use for each converter. As using different peripherals implies configuring different registers, the proposed solution allows selecting any existing PWM module combination through the converter-specific class's constructor. This is possible by using a series of instructions. First, an enum is configured as a regulation class's attribute. This enum's elements corresponds to the 9 PWM modules of the TI DSP, to which a value from “1<<0” to “1<<8” is assigned through left-shift operators. Thereafter, an "or" bitwise operation is carried out between the selected enum’s elements when creating the converter-specific object. The class's constructor executes a series of "if" conditionals and "for" loop iterations, determining which modules are set. Finally, an array of pointers addressing the structure of TI DSP's PWM register is configured. Depending on the result, the corresponding PWM module's register is modified in the regulation algorithm.

The implementation of the RegDspLib library within the control software of several power converters completely modifies the software hierarchy. The common features between converters are clearly reflected in the code, which significantly optimizes the control software if compared with the original configuration.

5.- EXPERIMENTAL VERIFICATION

5.1.- EXPERIMENTAL PLATFORM DESCRIPTION

The experimental verification of the proposed RegDspLib control library was carried out at CERN’s facilities. The CANCUN power converter (Fig.5(a)) was used, which was, by the time of the study, the only converter available in series production. At that moment, only a prototype sub-converter was available for the HL-LHC18kA, while the RF3kA was still under development. The RegFGC3 control electronics crate, described in section 2, was already integrated into the converter rack. In addition, Fig. 5(b) shows the programming board used for loading the RegDspLib software in the power converter. Testing the library was possible using the FGCRun+ software [15] to command the power converter from a laptop through Ethernet.

The CANCUN converter’s output power terminals were connected to an inductive load of 0.16 Ω and 80 mH to emulate the behavior of an electromagnet. The switching frequency of the power inverter at the primary side of the isolated DC/DC stage and at the output

stage 4-quadrant full-bridge were both set to 50 kHz. Interrupts for closed-loop control execution and ADC measurements were the ones previously specified in section 3.2.

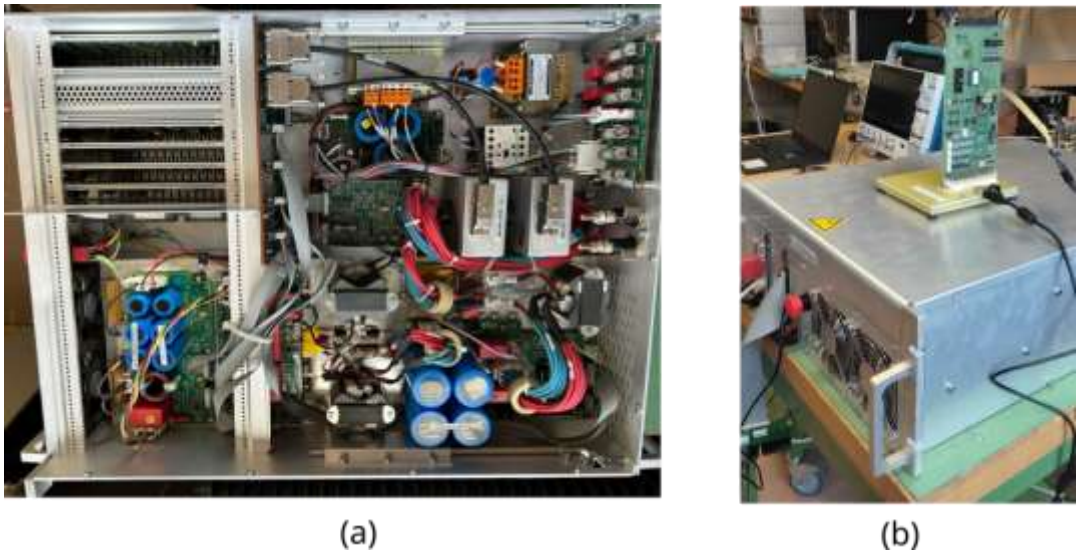

Fig. 5. (a) Detail of the physical CANCUN power converter rack incorporating the RegFC3 control electronics crate; and (b) overview of the experimental setup including the CERN programming board.

5.2.- TIMING RESULTS

Initially, the main objective of the experimental verification was to demonstrate that the newly proposed software and interrupt configuration comply with the execution-time constraints when running it through the whole FSM, i.e., that real-time execution without overruns is guaranteed. A testing card was plugged into the RegFGC3 card. This way, some digital ports were set to logical one during high- and low-priority routines execution for timing monitoring.

Fig. 6 summarizes the obtained time results for the whole interruption routine and FSM execution when operating in OFF, VS INIT OK and OUTPUT UNBLOCK states described in section 3. Table 1 resumes the execution times obtained for both the original software and the implemented RegDspLib library, demonstrating that, in general, time savings are achieved with the proposed software configuration.

Measurement	State	Original software (µs)	RegDspLib library (µs)
Whole interrupt routine execution-time	OFF	7.800	6.946
	VS_INIT_OK	Not measured	7.826
	OUTPUT_UNBLOCK	9.080	9.306
Execution-time of the FSM (task regulation of the converter in Fig. 3(b))	OFF	1.729	0.426
	VS_INIT_OK	1.889	1.226
	OUTPUT_UNBLOCK	2.769	2.746

Table 1. Execution time comparison: original converter-specific code (CANCUN) vs proposed derived code.

5.3.- OPERATIONAL PERFORMANCE OF THE POWER CONVERTER

Finally, and once real-time execution was assessed, the performance of the proposed control software under closed-loop operation was tested. Step-up and step-down commands from 10 A to 15 A (and vice versa) were commanded for the output reference current I_{ref}. A settling-time of T_s = 20 ms was set for the output load current. As expected, according to the experimental tests, the output

current reference tracking and transient responses were almost equal for I_{out} when using the converter-specific (Fig. 7(a)) and the proposed RegDspLib (Fig. 7(b)) codes. Thus, the correct implementation of the library through studying the closed-loop operation of the converter with the new software is confirmed.

6.- CONCLUSIONS

In this work, it has been proven that it is possible to exploit the common features between different particle accelerator switched power electronics converters in order to unify or generalize power converter related voltage control software. In addition, C++ is proven to be an efficient tool to integrate this code. This new approach enhances code maintainability for future modifications and debugging.

Implementing the RegDspLib library yields numerous benefits. By using inheritance, code re-usability and a hierarchical software structure are achieved with a well-established relationship. A generic class is created, defining the basic behavior of a group of power converters, while leaving implementation details to the derived classes (CANCUN, HL-LHC18kA and RF3kA). Accordingly, code becomes more organized and more understandable, while the manpower required for testing the software is minimized.

Several operation modes (1-quadrant,2-quadrant and 4-quadrant), control algorithms, multiple storage mechanisms and PWM techniques are covered. The proposed library does not only put common features together (i.e., the slew rate method) but also adds new functionalities (e.g., automatic interleaving calculation, generic ePWM module configuration within regulation, etc.). Given the generic programming approach followed in the configured library (parent class, generic programming, non-converter-specific interrupt routine, etc.), RegDspLib exhibits the flexibility required to accommodate future control needs for additional families of power converters.

The obtained experimental results are satisfactory in terms of real-time execution of the control software without overruns, achieving some time-saving figures in particular operation conditions (showing an increase of only 2.48 % the execution time for the worst-case scenario, and up to a 24.63 % time-saving for the best-case). The expected regulation performance is obtained for the tested power converter, following the operational requirements of the system and providing the same steady-state and transient responses as with the original converter-specific software.

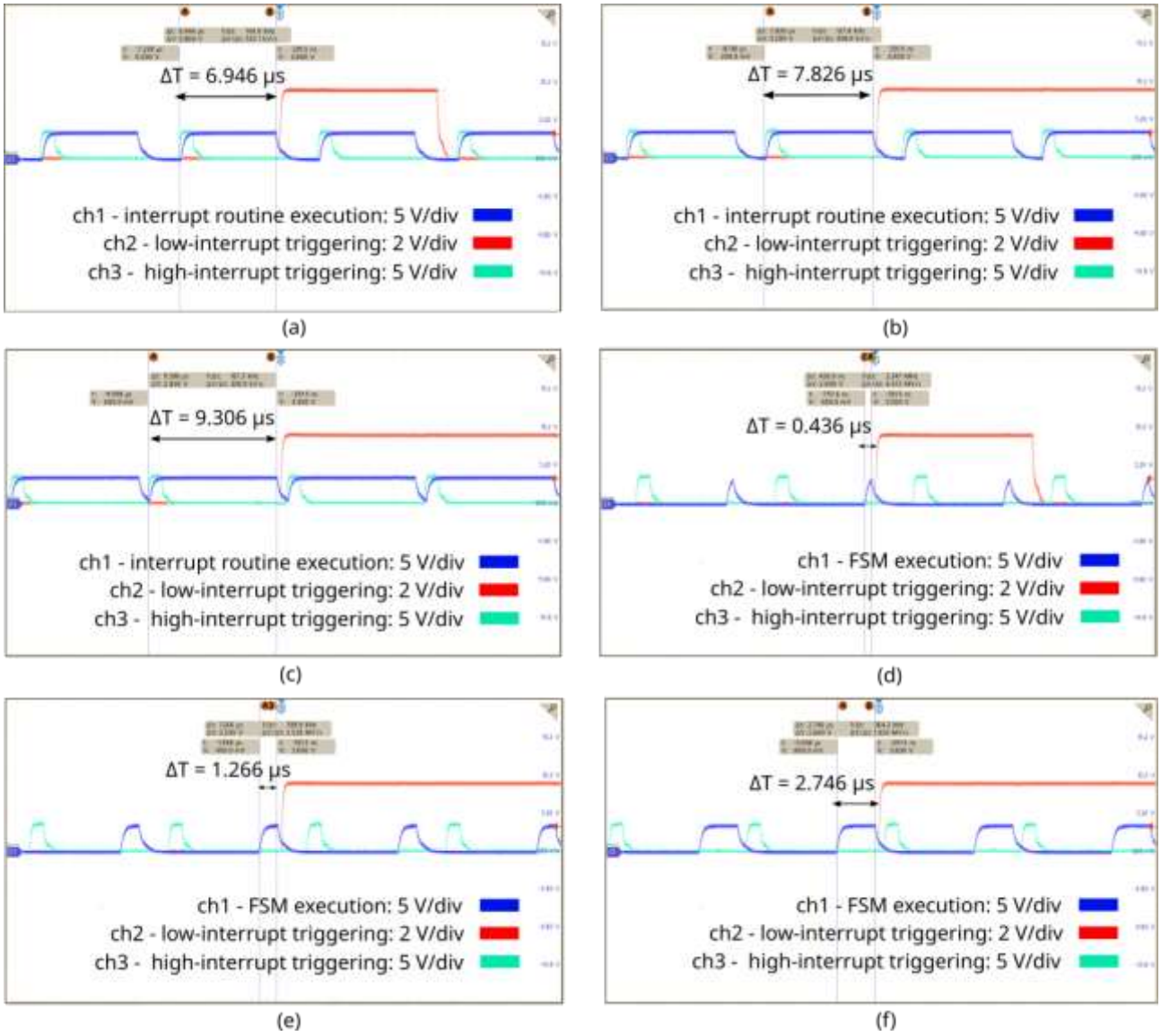

Fig. 6. Timing results (CANCUN): (a) Proposed library's interrupt routine time in OFF state, (b) in VS INIT OK state, and (c) in OUTPUT UNBLOCK state. (d) Detail of FSM execution in OFF state, (e) VS INIT OK state, and (f) OUTPUT UNBLOCK state.

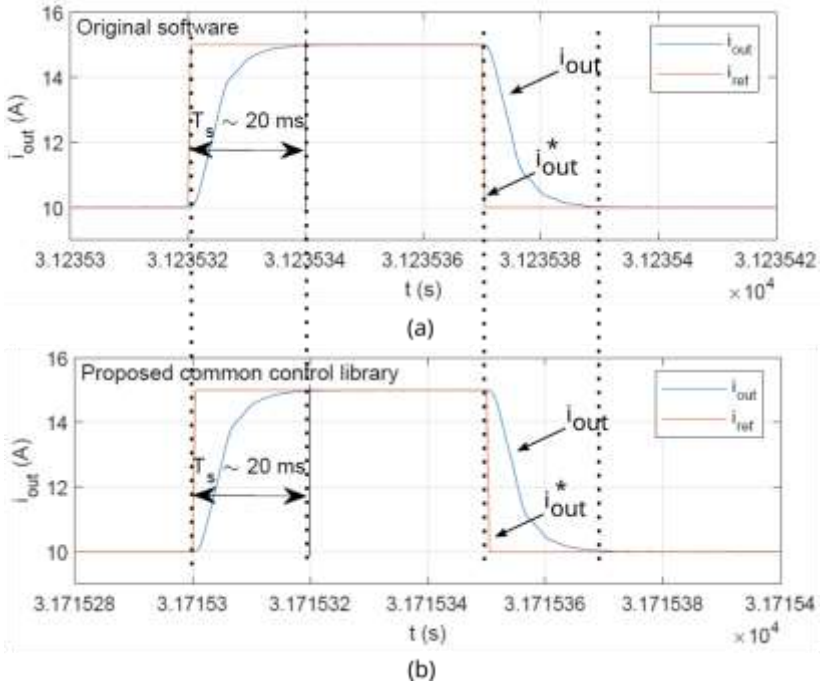

Fig. 7. Output current step response obtained for the CANCUN converter: (a) with the original converter-specific software, and (b) the proposed RegDspLib converter-agnostic software.

ACKNOWLEDGEMENTS

Research supported by the HL-LHC project and by the Government of the Basque Country within the Fund for Research Groups of the Basque University System under Grant IT1440-22

REFERENCES

[1] E. Coulinge, S. Pittet, D. Dujic, "Design optimization of two-quadrant high-current low-voltage power supply," *IEEE Transactions on Power Electronics. 2020.* Vol. 35-10, p. 11602–11611. DOI: 10.1109/TPEL.2020.2988901

[2] A. Srivastava, M. Borage, A. Singh, et al., "Steady-state analysis and design of two-quadrant switch-mode, fast-ramped power converter for electromagnets in particle accelerators," *in Proc. of the National Power Electronics Conference (NPEC)*. 2021, p. 1-6. DOI: 10.1109/NPEC52100.2021.9672504

[3] M. Alderighi, M. Citterio, M. Riva, et al., "Power converters for future LHC experiments," *Journal of Instrumentation.* 2012. Vol. 7, p. 1-15. DOI: 10.1088/1748-0221/7/03/C03012

[4] E. Ibarra, A. Arias, I. Martínez de Alegría, et al., "Digital control of multiphase series capacitor buck converter prototype for the powering of HL-LHC inner triplet magnets," *IEEE Transactions on Industrial Electronics*, 2022. Vol. 69-10, p. 10 014–10 024. DOI: 10.1109/TIE.2021.3120489

[5] S. Rocca, F. Boattini, L. de Paco Soto, "Development of a control strategy for the 18 MW power converter of the CERN PS Booster accelerator," *in Proc. of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*. 2018, p. 1–8. DOI: 10.1109/COMPEL.2018.8460164

[6] S. Carrozza, F. Burini, E. Ferrari, et al., "A new concept of high current power supply for the main cyclotron magnet at TRIUMF," *in Proc. of the International Conference on Cyclotrons and their Applications.* 2016, p. 186-189.

[7] P. Asimakopoulos, K. Papastergiou, T. Thiringer, et al., "IGBT power stack integrity assessment method for high-power magnet supplies," *IEEE Transactions on Power Electronics. 2019.* Vol. 34-11, p. 11228–11 40. DOI: 10.1109/TPEL.2019.2900393

[8] L. De Mallac, D. Aguglia, S. Pittet, "Modular Resonant 25 kV – 8 A Power Converter for Particle Accelerator Application: Realisation and Operation," *in Proc. of the European Conference on Power Electronics and Applications (EPE'21 ECCE Europe).* 2021. p. 1–10. DOI: 10.23919/EPE21ECCEEurope50061.2021.9570439

[9] O. S. Bruning, P. Collier, P. Lebrun, S. Myers, R. Ostojic, "LHC design report vol.1: The LHC main ring," CERN Yellow Reports: Monographs. 2004. DOI: 10.5170/CERN-2004-003-V-1

[10] O. Aberle, I. Bejar Alonso, O. Bruning, P. Fessia, L. Rossi, L. Tavian, M. Zerlauth, "High-Luminosity Large Hadron Collider (HL-LHC): Technical design report", CERN Yellow Reports: Monographs, 2020.

[11] S. Yammine, H. Thiesen, "Modeling and control of the HL-LHC nested magnet circuits at CERN," *in Proc. of the 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019. p. 1-6. DOI: 10.1109/COMPEL.2019.8769677

[12] N. Beev, M. Bastos, M. Martino, D. Valuch, "A metrology-grade digitizer for power converters in the high luminosity large hadron collider," in Proc. of the IEEE International Instrumentation and Measurement Technology Conference (I2MTC), 2022. p. 1-6. DOI: 10.1109/I2MTC48687.2022.9806573

[13] D. Siemaszko, M. Speiser, S. Pittet, "Reliability models applied to a system of power converters in particle accelerators," *in Proc. of the European Power Electronics And Applications Conference (EPE)*, 2011. p. 1-9.

[14] Calcoen, D; King, Q; Semanaz, PF, "Evolution of the CERN Power Converter Function Generator/Controller for Operation in Fast Cycling Accelerators, "*in Proc. of the International Conference on Accelerator and Large Experimental Physics Control Systems.* 2011, pp.939-942.

[15] King, Q, "Development, test and large production of soft switching high current power converters for particle accelerators," *in Proc. of the International Conference on Accelerator and Large Experimental Physics Control Systems*, 2009. pp. 4–6.

[16] R. Murillo-Garcia, "FGC3 ecosystem", *CERN (EPC), EDMS web*. Available: https://edms.cern.ch/ui/file/2771458/2/2021_2771458_TEC_FGC3_ecosystem.pdf

[17] Q. King, K. Lebioda, M. Magrans de Abril, et al., "CCLIBS: The CERN Power Converter Control Libraries," *in Proc. of the International Conference on Accelerator and Large Experimental Physics Control Systems, 2015. pp. 950–953.* DOI: 10.18429/JACoW-ICALEPCS2015-WEPGF106

[18] B. Stroustrup, "The C++ Programming Language, Third Edition," *Addison-Wesley Longman Publishing Co.* 1997.

[19] "CANCUN," 2023, *SY-EPC-LPC's group web page*. [Online]. Available: http://sy-dep-epc-lpc.web.cern.ch/converters/cancun/general.stm

[20] G. Fernqvist, "The measurement challenge of the LHC project," *IEEE Transactions on Instrumentation and Measurement*. 1999. Vol. 48-2, p. 462-466. DOI: 10.1109/19.769628

[21] H. Matsuo, H. Yonemori, Y. Yasaka, "Phase-shift controlled zero current switching high frequency inverter in the MHz frequency range," *in Proc. of the International Power Electronics Conference - ECCE ASIA*. 2010. p. 2830–2835. DOI: 10.1109/IPEC.2010.5543907

[22] F. Bordry, V. Montabonnet, D. Nisbet, et al., "Development, test and large production of soft switching high current power converters for particle accelerators," *in Proc. of the European Conference on Power Electronics and Applications*. 2005. pp. 1–10. DOI: 10.1109/EPE.2005.219231

[23] B. Johnson, P. Krein, "An analytical time-domain expression for the net ripple produced by parallel interleaved converters," *IEEE Transactions on Circuits and Systems II: Express Briefs.* 2017. Vol. 64-3. p. 289–293. DOI: 10.1109/TCSII.2016.2557620

SUPPLEMENTARY MATERIAL

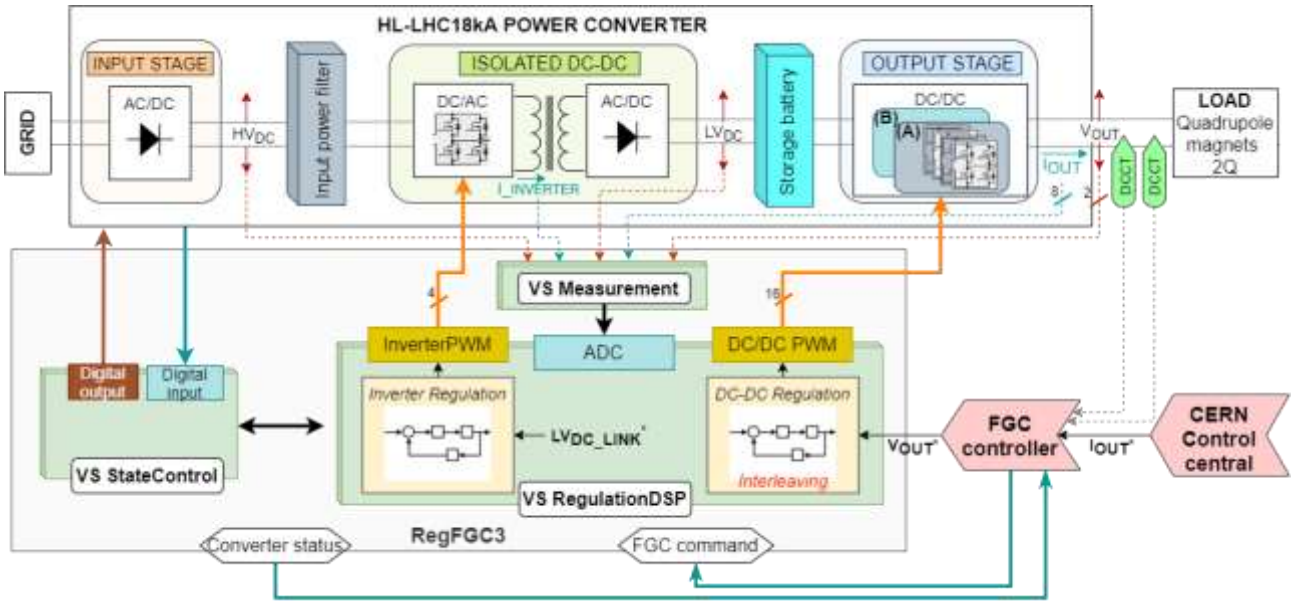

Fig. A. Block diagram of the HL-LHC18kA power converter and its control.

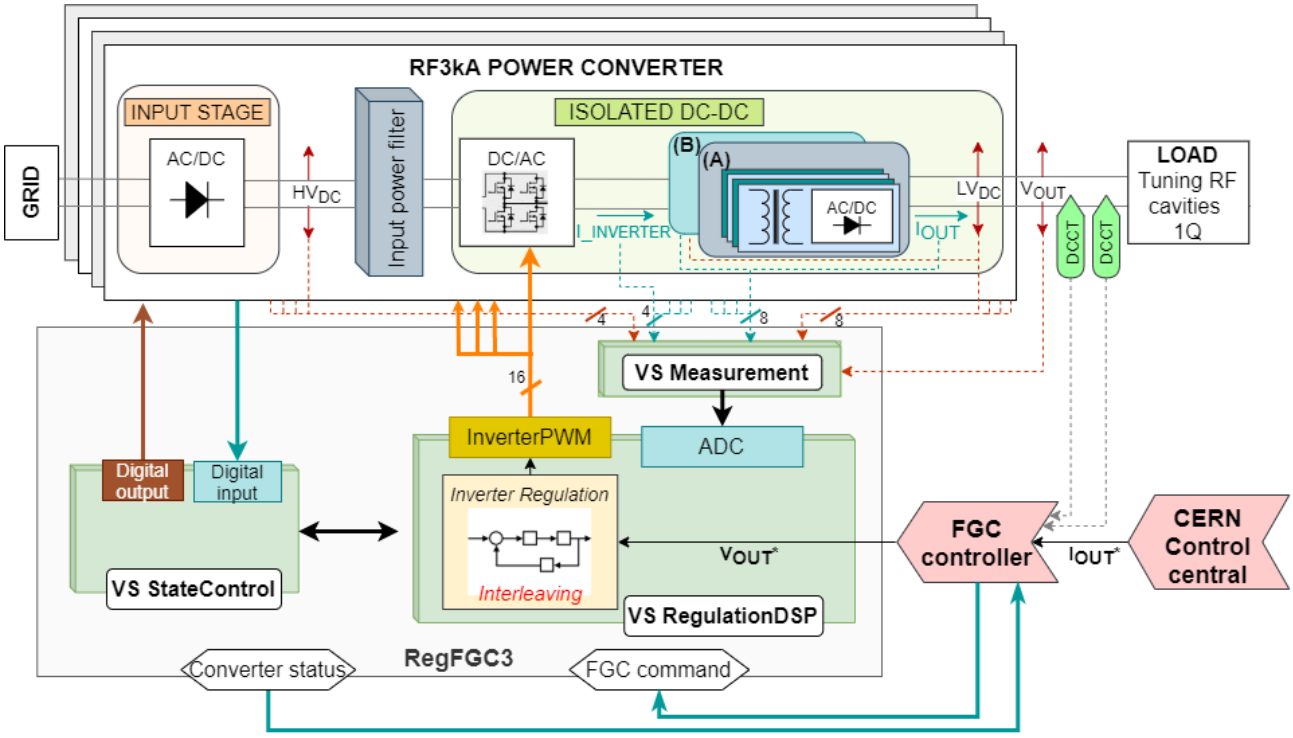

Fig. B. Block diagram of the RF3kA power converter and its control.