DISCRIMINATOR ICS FOR TRACKING AND TIME-OF-FLIGHT DETECTORS

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ABSTRACT

Proceeding from the analysis of the present state of front-end electronics there have been stated the requirements to the parameters of discriminator ICs, being part of the time-processing channels for signals of LHC tracking and time-of-flight detectors.

The structure, contents and basic parameters of new ASICs is described. Among them are:

- two versions of four-channel comparator ICs;
- an eight-channel IC, containing a base line restorer and comparator, supplemented by an "OR" circuit;
- a new ASIC, intended to implement the units of time reference to signals of nanosecond duration and with an amplitude of 5mV..2,5V at an accuracy of tens of picoseconds. It can be used to implement CFD, LED, window and extrapolation discriminators.

1. FOUR-CHANNEL COMPARATOR ICS

Comparators are widely used in the equipment of nuclear physical experiments both in amplitude and, especially, time channels. One may recall the fast comparators for the timing circuits and time spectrometry, economical comparators of the nanosecond range, used in the time processing channels for signals of LHC tracking detectors.

The given section considers comparators for time processing channels, which, as the literary sources show, should meet the following requirements:

Firstly, an extremely large channel number imposes tough restrictions on power consumption which should not exceed 20...30 mV.

Secondly, the comparator should have a low-resistance differential output for connection with a high-resistance differential input of a time to digital converter. Output logic levels should be compatible with small logic step standards, for instance GTL, which are preferable from the viewpoint of speed and consumption.

Thirdly, in order to provide the required accuracy of measurements, the duration of the leading and trailing edges should not exceed 1...3 ns at a capacitance load of each output of about 5 pF relative to ground - a typical value for the printed circuit boards. For the same reason the offset voltage is to be provided in the limits of 1..3 mV.

Fourthly, in order to prevent false triggering it is desirable to have a small (0,5...3 mV) hysteresis.

Besides the enumerated basic requirements, it is useful to be able to control the hysteresis, have at disposal an additional latch function and a base line restoration (BLR) circuit. In a multichannel chip it is expedient also to have a circuit of the "common OR" kind, switched on/off by supply voltage.

With account of the above presented there have been designed and manufactured in Russia three versions of comparator ICs.

The first of them is a 4-cnannel micropower comparator. Each comparator channel is built as a differential circuit with two gain stages and intermediate emitter followers. Output followers are included to reduce output impedance. Internal positive feedback is applied to the input stage, what increases DC gain and provides a hysteresis. The output stage is fed through a separate lead of the positive supply source (+2,0...+3,0 V) and provides the GTL-standard. The main parameters of the comparator are adduced as follows:

Power consumption per channel, mV	18
Supply voltage, V	±3
Offset voltage, mV	3
Built-in hysteresis, mV	2,5
Propagation delay, ns	8
Rise-time, ns	5
Fall-time, ns	7.

The three latter time characteristics for the given comparator and others were measured at the load capacitance of 5 pF, threshold voltage of 30 mV and a signal over threshold overdrive of 50 mV.

The second version of the 4-channel comparator is built similarly to the first one, except the additional circuits controlling the hysteresis and the output logic. The hysteresis is changed in the range of (0...4,5) mV. Depending on the supply voltage of the output stage (separate pin), the output signals may correspond to the GTL, ECL, or TTL standards as needed. Due to the circuit complication, occurred thereat, the power consumption has increased by 30 mW per channel.

Both versions were implemented in limits of a single planar full-custom bipolar process. The chips differ only in their platings.

2. AN EIGHT-CHANNEL IC, CONTAINING A BASE LINE RESTORER AND COMPARATOR.

The given section describes the third version of comparator IC. The 8-channel IC contains in each channel a circuit of base line restoration (BLR) and high speed voltage comparator. The circuit of one channel is shown in fig.1.

The channel is intended for operation from a single-ended signal of positive polarity, taken from the shaper output [1]. The use of the shaping capacitor simultaneously as a DC decoupling one allowed to eliminate the bias voltage originating in the previous stages.

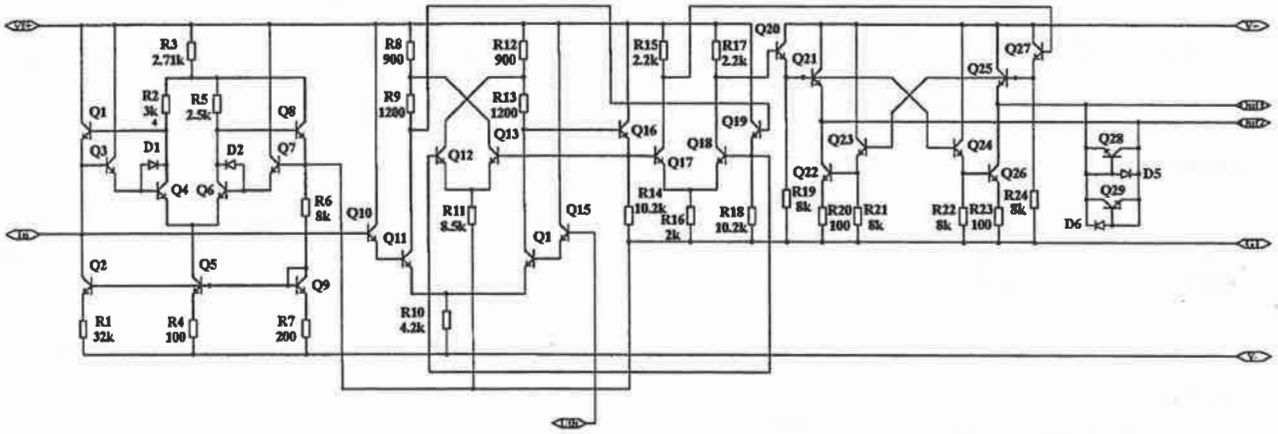

Figure 1: The circuit of one comparator channel

The BLR circuit has a small inherent bias voltage with a small temperature coefficient. Particularly this is achieved by introducing an internal voltage stabilizer (transistors Q6-Q9 and resistors R3, R5-R7). The actually obtained bias voltage of the BLR circuit together with the comparator does not exceed 2-3 mV, what can be neglected in comparison with the standard value of threshold (~10 mV).

The restoration of base line in the designed circuit takes place much faster, than in ASD/BLR designed by Pennsylvania University [2]. The time resolution for pulses of close amplitude makes up < 60 ns (< 100 ns for ASD/BLR). For the worst case (a small pulse superimposed on the tail of a large one) the time resolution makes up < 200 ns (<600 ns for ASD/BLR).

The comparator circuit is built according to the classic circuit with differential input and output. However, some of its peculiarities should be marked.

Since the microwave transistors of the semicustom array have small base current amplification (~35), a Darlington circuit was used at the comparator input in order to reduce the input bias current. The first differential stage has positive feedback, that provides a noise suppressing hysteresis loop (ΔV) about 2 mV wide. The output stage is built as a quasi-push-pull circuit, where the signals of positive polarity are transferred by transistors Q21 and Q25, whereas the ones of negative polarity – by Q22, Q23 and Q24, Q26. The pair of Shottky diodes connected opposed in parallel provides output logic levels of the GTL standard.

The speed of comparator is best of all displayed by the switch-over transients at overdrive levels Vod=5, 20 and 100 mV, presented in fig. 2. Since the comparator output is differential, the duration of transients from logic unity to logic zero and vice versa are, as it should be expected, practically equal. Therefore in fig. 2 there are presented only the plots of transients from logic unity to zero. The corresponding results are tabulated in table 1. Right there are presented also the static parameters of comparator.

Table 1: Basic parameters of the comparator.

V_{od}	T_{del}	t_{01}, t_{10}	V_{off}	I_B	ΔV	$W_{channel}$	U_S	Logic
5 mV	2 ns	0,75 ns	2...3 mV	0,18 μA	2 mV	20 mW	±3 V	GTL
20 mV	3,4 ns	1,1 ns						
100 mV	13,6 ns	5,3 ns						

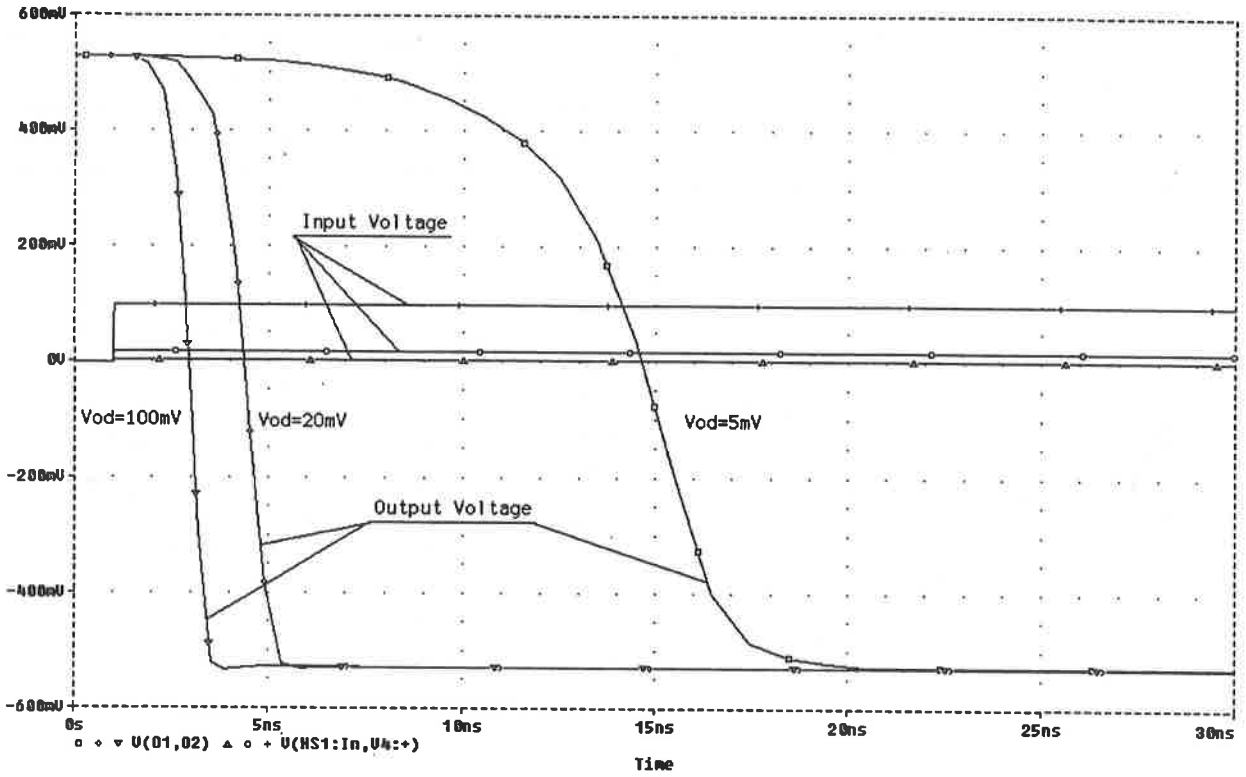

Figure 2: Pulse response of the comparator at different overdrives

The given 8-channel IC contains one more interesting peculiarity – it is added by a circuit implementing the logic OR function for all 8 channels. This, for instance, becomes useful at the stage of calibrating, adjusting multichannel experiments, as well as at choosing useful events. In the given case this has been reached by combining the outputs of eight channels, as shown in fig. 3. The output of the "OR" circuit is implemented as an "open collector" one (Q19), what allows to increase the number of the outputs, combined into on "OR" circuit, directly on the printed circuit board. The circuit is provided by an internal voltage stabilizer and gate with transistors Q21, Q22, which allow to disable the "OR" circuit through its supply voltage in case of necessity.

The 8-channel IC was implemented on the basis of a semicustom bipolar array.

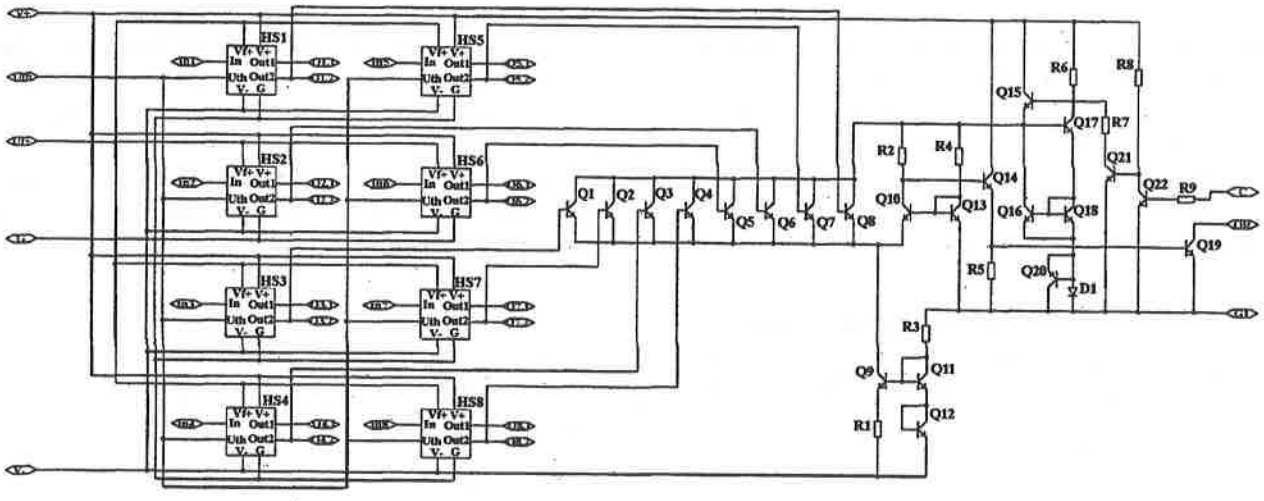

Figure 3: The logic OR circuit inside the IC

3. AN ASIC FOR TIMING DISCRIMINATORS

The LHC multichannel detector systems require an increase of the processing channel number (tens and even hundreds thousand), what inevitably entails a reduction of space, allotted for the electronics of a channel, processing preliminary the signals of a detector, as well as a reduction of power consumption. Requirements are set thereat to preserve or even improve the main precision and energy parameters of electronics, achieved with standard (NIM, CAMAC, VME) units. A success in solving these problems with standard general application ICs appears often extremely difficult.

The structure, contents and basic parameters of a new ASIC, intended to implement the units of time reference to signals of nanosecond duration and with an amplitude of 5mV...2,5V at an accuracy of tens of picoseconds, is described. It can be used to implement CFD, LED, window and extrapolation discriminators.

In the course of design there has been worked out an optimal set of IC components. One chip contains two similar channels of timing discriminators.

The structure of one channel is shown in fig. 4. It is a development of the previous design of the timing discriminator [3]. One channel, along with the most principal cells, namely comparators and D-flip-flops, comprises voltage stabilizers, supply filters, input signal monitoring circuits, buffer amplifiers for driving low-ohmic loads. This all has the purpose of raising the integration scale of the timing discriminator as a whole.

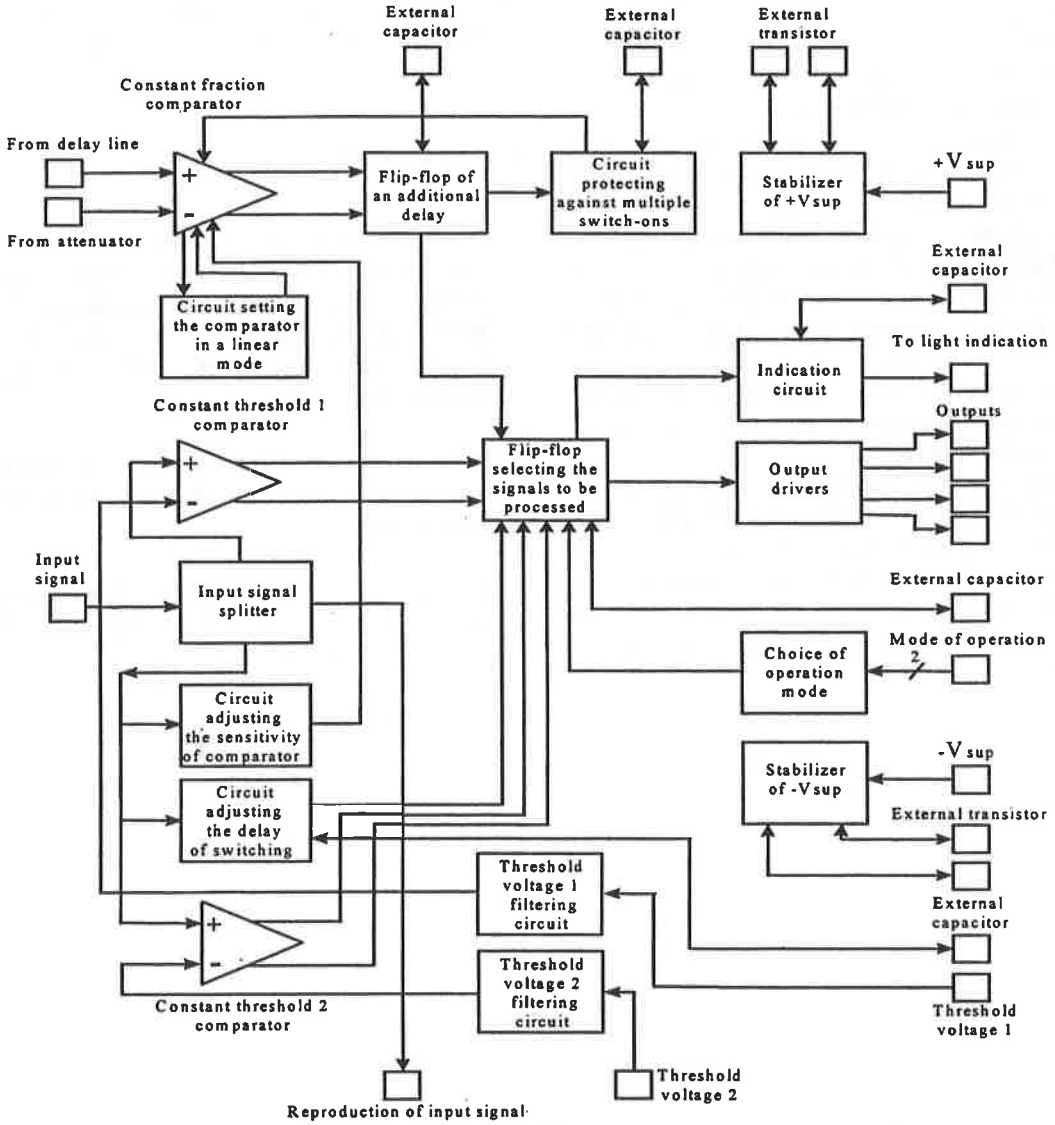

Figure 4: The structure of the timing discriminator channel.

The detectors of multichannel experiments provides differential signal pick up. In this case it is highly important to secure good matching between the main characteristics of the preliminary processing channels (preamps, amplitude and timing discriminators), operating in a differential connection.

Particular attention should be paid to channel characteristics reproducibility and simplicity of their adjustment. Therefore the suggested circuit was supplemented by auxiliary circuits. Among them there are the ones of comparator charge sensitivity compensation and of setting it automatically in the active mode, of excluding false switch-over of the comparator, caused by noise-like signals, as well as of disabling the comparator for a controllable time to prevent its switch-over by spikes in the input signal.

For the user's convenience there has been included a circuit, indicating the mode of IC operation, as well as a digital circuit of event selection having a programmable logic of output signal.

In order to minimize crosstalks between channels and to suppress the supply busses' influence, the circuitry is built according to the differential scheme. The reduction of the internal logic step down to 200 mV not only reduces crosstalk between channels, but essentially raises the economy of the circuit.

Special attention was paid to temperature stability, which had been achieved at the expense of certain circuital complications. This promotes the improvement of characteristics reproducibility from channel to channel.

Such an approach allows to minimize the number of external mounted components and save space in the direct vicinity of the detector.

The first prototype of ASIC is expected to be implemented on the basis of a functionally oriented analog semicustom array, manufactured by a bipolar process.

After testing the IC samples their mounting on a multilayer SMT PCB, measuring 80 * 40 mm. sq., is foreseen as their first applications in time-of-flight measurements.

4. CONCLUSIONS

In this paper the requirements to the parameters of discriminator ICs, being part of the time-processing channels for signals of LHC tracking and time-of-flight detectors, are described.

Also the structure, contents and basic parameters of new ASICs are presented. Among them are two versions of four-channel comparator ICs, an eight-channel IC (comprising a base line restorer and comparator, supplemented by an «OR» circuit) and ASIC for the implementation of the units of time reference to signals of nanosecond duration with amplitudes of 5mV...2,5V (it can be used to implement CFD, LED, window and extrapolation discriminators).

The greatest attention was given to reduction of power consumption, minimizing crosstalks, increasing channel characteristics reproducibility as well as to the simplicity of their adjustment, because these discriminators are intended for using in multichannel experiments.

REFERENCES

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