

10 Gb/s Radiation-Hard VCSEL Array Driver

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We present an R&D program to develop an ASIC that contains a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array driver operating at 10 Gb/s per channel, yielding an aggregated bandwidth of 120 Gb/s. The design of the 10 Gb/s array driver ASIC is based on a prototype ASIC for driving a VCSEL array at 5 Gb/s. We will briefly describe the design of the 5 Gb/s ASIC that was fabricated in a 130 nm CMOS process. Two ASICs were irradiated with 800 MeV protons to a dose of 0.92×10^{15} 1-MeV n_{eq}/cm^2 and remain operational. For the 10 Gb/s VCSEL array driver ASIC, the plan is to fabricate the ASIC in a 65 nm CMOS process. However, at this stage in our R&D we are targeting the fabrication of a four-channel test chip. The circuit design along with the result from a simulation of the extracted layout with parasitic capacitance and inductance will be presented.

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1. Introduction

The Large Hadron Collider (LHC) at CERN (Geneva) is now the highest energy and luminosity collider in the world. To further enhance the physics potential, the LHC will be upgraded to even higher luminosity. The detectors will be upgraded in tandem to fully exploit the new physics potential. The optical data transmission system will thus need to be upgraded to handle the higher data transmission speed.

Commercial VCSEL arrays capable of operation at 10 Gb/s are now readily available. A 12-channel VCSEL array offers a compact and robust solution for data transmission. With individual VCSELs operating at 10 Gb/s, the total aggregated bandwidth is 120 Gb/s per fiber ribbon. In previous studies, these commercial VCSEL arrays have been proven to be sufficiently radiation-hard [1]. Therefore, we will design a VCSEL array driver ASIC with sufficient radiation hardness to survive in challenging HEP deployments.

We will present results from an R&D project to produce a radiation-hard VCSEL driver ASIC capable of 10 Gb/s operation per channel. As a first step in this direction, we have designed a VCSEL array driver ASIC for operation at 5 Gb/s. The prototype ASIC was fabricated in a 130 CMOS process. We will briefly describe the design and present the result after an irradiation with 800 MeV protons to a dose of 0.92×10^{15} 1-MeV n_{eq}/cm^2 . This will be followed by a description of the preliminary design for a 10 Gb/s VCSEL array ASIC. A 4-channel version of the ASIC will first be fabricated in a 65 nm process before expanding to 12 channels. We will present the circuit designs along with results from a simulation of the extracted layout with parasitics included.

2. Results from a 5 Gb/s VCSEL Array Driver

We have successfully designed a VCSEL array driver ASIC to operate at speeds up to 5 Gb/s [2]. The ASIC was fabricated in a 130 nm CMOS process to enhance the radiation-hardness. Each ASIC contains eight low voltage differential signal (LVDS) receivers to receive the data from the front-end electronics [3]. The received LVDS signal is converted in the driver stage into a current sufficient to drive a VCSEL. The amplitude of the modulation current in each driver is controlled via an 8-bit DAC. There is also a single 8-bit DAC to set the bias currents of all channels simultaneously. In addition, there are four spare drivers with associated 8-bit DACs that can receive the LVDS signal from any of the eight LVDS receivers via a switching network. This allows the received LVDS signal to be transmitted via one of the four spare VCSEL channels should a VCSEL in one of inner eight channels become non-operational. To enable operation in case of a failure in the communication link to the receiver array ASIC, we have included a power on reset circuit that sets the modulation current in the VCSEL to 9 mA on top of a bias current of 1 mA upon power up with no signal steering.

The 8-bit DAC and LVDS receiver are designed to operate with a 1.5 V supply and the driver stage is designed to operate with a 2.5 V power supply. A higher supply voltage is required by the output stage to allow sufficient headroom to drive VCSELs which normally have threshold voltages of 2 V or higher.

We have characterized several ASICs. Each ASIC is coupled to a VCSEL array fabricated by ULM with a bandwidth of 10 Gb/s [4]. The performance of the ASIC at 5 Gb/s is satisfactory with bit error rate (BER) of $< 5 \times 10^{-13}$ with all other channels in the ASIC active. We have irradiated two ASICs with 800 MeV protons to a dose of 0.92×10^{15} 1-MeV n_{eq}/cm^2 . Both ASICs were powered during the irradiation. Due to the limited availability of a high-speed optical probe after the test, we evaluated the performance of the driver ASIC using a Finisar Small Form Factor (SFP+) transceiver [5]. This SFP+ transceiver is specified to operate at 10 Gb/s and thus we can use it to probe of the quality of the received optical signal from the VCSEL. This is accomplished by feeding the SFP+ electrical output to a 13 GHz oscilloscope. It should be noted that the use of the SFP+ transceiver improves the vertical eye opening. The transceiver discriminates the optical signal and thus removes amplitude noise by re-shaping the wave fronts. Fig. 1 shows a comparison of the eye diagrams obtained with the SFP+ transceiver before and after the irradiation. It is evident that there is more jitter after the irradiation but the ASIC is still operational with low BER. We plan to do a more detailed characterization with a high bandwidth optical probe.

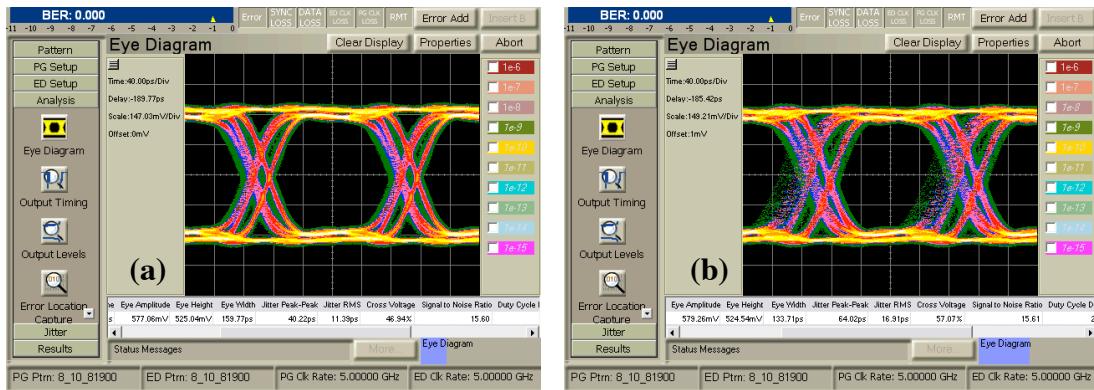


Figure 1: Comparison of the eye diagrams (a) before and (b) after irradiation for a VCSEL channel coupled to a driver ASIC as viewed with a SFP+ transceiver.

3. Preliminary Design of a 10 Gb/s VCSEL Array Driver

We have migrated the design of the 5 Gb/s VCSEL array driver for operation at 10 Gb/s. As a first step, the test chip will have four channels for fabrication in a 65 nm CMOS process. To achieve the maximum possible radiation-hardness, all transistors used will be core transistors. The core transistors have the thinnest gate oxide available in this process. Given this, the supply voltage of the test chip will be 1.2 V. The block diagram of the VCSEL driver is shown in Fig. 2. A simulation of the extracted layout indicates that each channel consumes 35 mA of current, corresponding to a power consumption of 42 mW.

The four channels in the ASIC will have different VCSEL driver and differential receiver topologies. These different topologies will be used to qualify the performance and radiation hardness of the different topologies. We plan to include two versions of CML (current mode logic) receiver along with an LVDS like receiver. For the VCSEL driver, we plan to fabricate

three different versions with modified driver architectures. The fourth channel, containing the LVDS like receiver, will use a copy of the driver from one of the channels containing a CML receiver. The motivation to include an LVDS like receiver is that, while it will likely be inferior from a bandwidth perspective, LVDS requires less power to operate than CML. If we can achieve suitable performance at 10 Gb/s with a lower power design this will of course be beneficial.

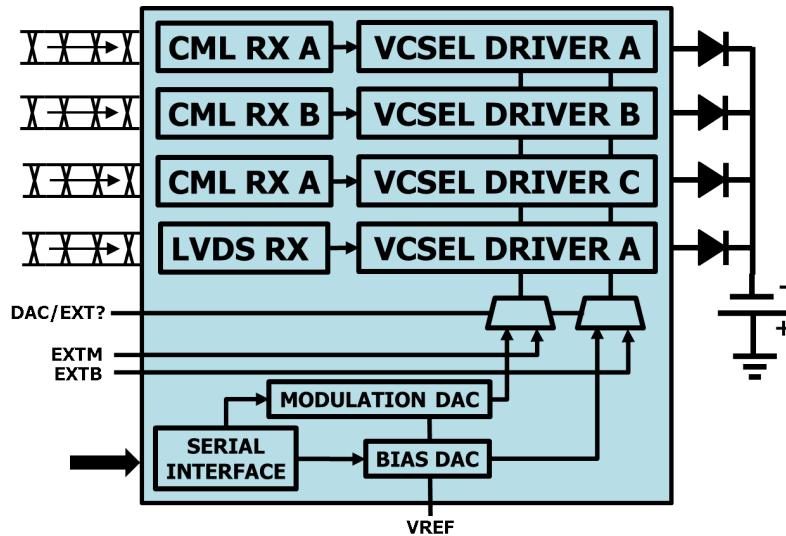


Figure 2: Block diagram of the 10 Gb/s VCSEL array driver with 4 channels.

The CML receiver is a four-stage limiting amplifier as shown in Fig. 3. Each stage is a common mode feedback amplifier with feed forward capacitors on the input differential pair to enhance the higher frequency signal components. The layout is $60 \mu\text{m} \times 30 \mu\text{m}$ with a current consumption of 22 mA, corresponding to a power dissipation of 26 mW. Fig. 4 shows the eye diagram of the extracted layout. The quality of the eye diagram is acceptable but more improvements would enhance the operating margin.

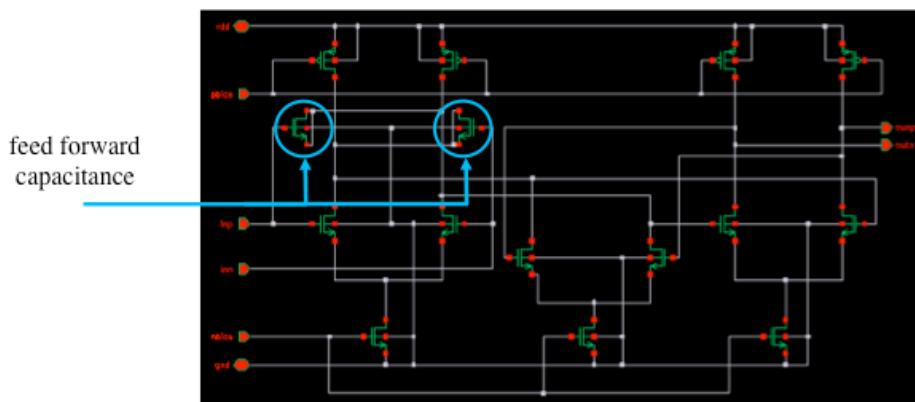


Figure 3: Schematic diagram of the CML driver.

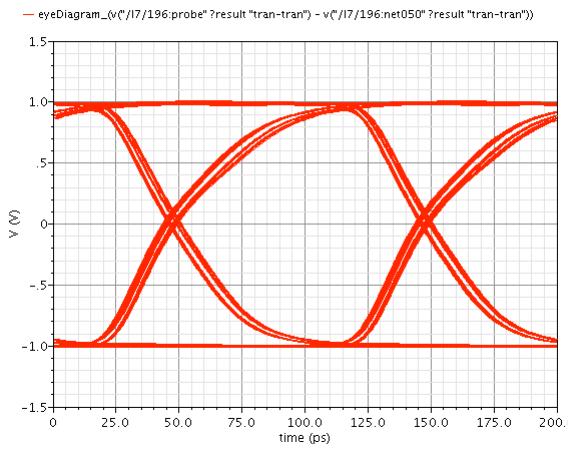


Figure 4: Eye diagram from a simulation of the extracted layout of the CML driver.

In the VCSEL driver, the current in the VCSEL is set by two transistors. One transistor has a constant bias current and the other is biased by a capacitive feed forward of the negative half of the differential input signal as shown in Fig. 5. This produces a pre-emphasis and improves VCSEL current rise/fall times. The layout of the driver is $125 \mu\text{m} \times 125 \mu\text{m}$. The driver consumes 12.5 mA of current or 15 mW of power. The eye diagram from a simulation of the extracted layout including pad, wire-bond, and VCSEL parasitics is shown in Fig. 6. The eye is open but more improvement to the design is needed.

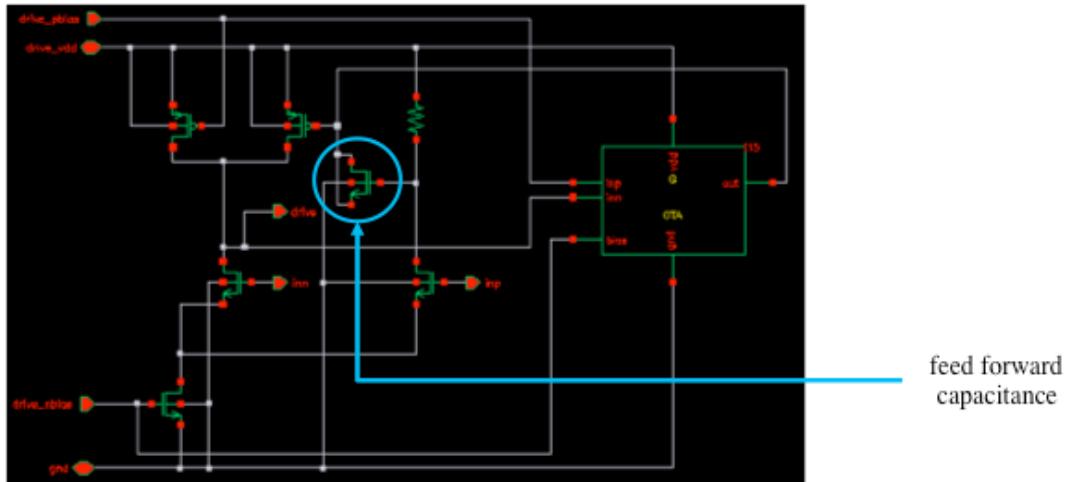


Figure 5: Driver circuit of a VCSEL channel.

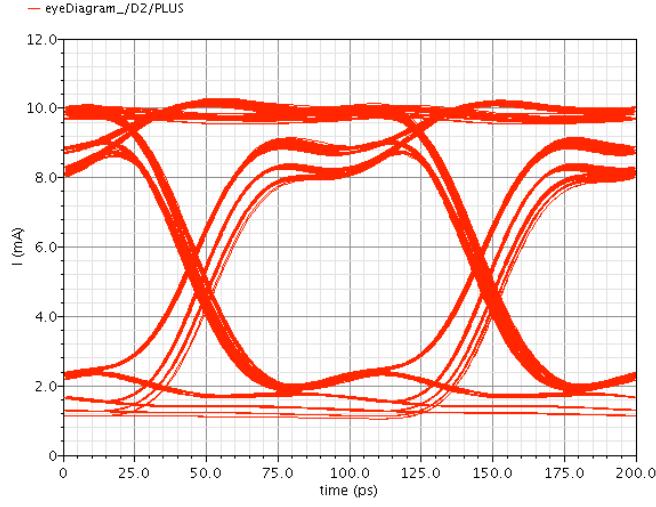


Figure 6: Eye diagram from a simulation of the extracted layout of the driver circuit, including parasitic capacitance and inductance.

The 8-bit DAC is scaled from the design for the 5 Gb/s VCSEL array driver ASIC fabricated in a 130 nm CMOS process. The DAC is used for remotely controlling the VCSEL bias and modulation currents. We plan to use an external reference voltage for this prototype while waiting for the release of a bandgap reference IP (intellectual property) circuit from CERN. The circuit consumes 270 μ A of current. Fig. 7 shows a sweep of the DAC voltage vs time (DAC value). The DAC is not quite linear. However, the performance is quite adequate for our application.

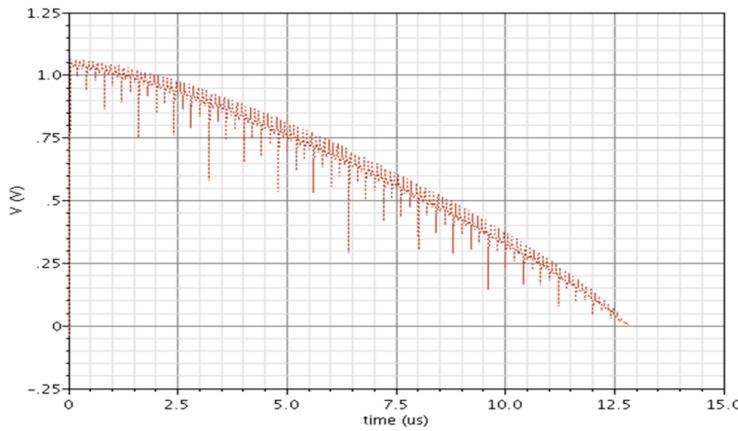


Figure 7: Output voltage of the 8-bit DAC vs time (DAC value).

We are currently improving the various building blocks of the ASIC. The plan is to submit the design for fabrication in early October. The prototype ASIC will be characterized and then irradiated to study the radiation hardness. We anticipate that test results from the four different VCSEL driver channels will guide us in tuning and selecting a preferred topology for the design of a 12-channel ASIC.

4. Conclusions

We present an R&D program to develop an ASIC to operate a 12-channel VCSEL array at 10 Gb/s per channel. The design is an upgraded version of a similar ASIC operating at 5 Gb/s, fabricated in a 130 nm CMOS process. We present the result of the 5 Gb/s VCSEL array driver after irradiation. The ASIC is still operational at 5 Gb/s but with more jitter. We present the various building blocks of the 10 Gb/s design together with results from simulations of the extracted layout including parasitics. More improvements in the design are currently in progress. The plan is to submit a 4-channel test ASIC using a 65 nm CMOS process in October. The result from the prototype ASIC will guide us in the design and fabrication of a 12-channel VCSEL array driver.

Acknowledgments

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References

- [1] A. Nagarkar et al., Study of the Radiation-Hardness of VCSEL & PIN Diodes, PoS (RD11) 036 (2012).
- [2] K.K. Gan et al., Radiation Hard/High-Speed Parallel Optical Links, to be published in the Proceedings of the 9th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, Hiroshima, Japan, September, 2013.
- [3] Due to the requirement of another project, the input has only eight receivers even though the output couples to a 12-channel VCSEL array.
- [4] The VCSEL array used is ULM850-10-TN-N0112U, fabricated by ULM Photonics.
- [5] The SFP+ transceiver used is FTLX8571D3BCL, fabricated by Finisar.