Front-End Electronics Design for the Transition Radiation Detector Prototype in the HERD

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***Abstract*— The high-energy cosmic radiation detection facility (HERD) is a part of the Chinese Cosmic Lighthouse Program in China space station (CSS), which is planned for launch in 2027. The HERD is expected to operate for ten years in orbit, and it will be able to indirectly detect dark matter, measure cosmic rays, and observe high-energy gamma rays. As a subdetector of the HERD, a transition radiation detector (TRD) has the main scientific goal of calibrating the electromagnetic calorimeter (CALO) at the TeV energy range, improving the measurement accuracy of the CALO, and detecting astronomical phenomena of high-energy gamma rays. In this work, we designed the front-end electronics (FEEs) as a standard readout unit for the TRD prototype in the HERD. The FEE uses four SAMPA application-specific integrated circuits (ASICs) for 128 detector signal readouts, realizing a high-speed, low-power, and high-reliability data acquisition system. The FEE receives trigger signals and serial commands from the back-end electronics (BEEs) using the universal asynchronous receiver transmitter (UART) protocol via an RS-422 bus and replies to the BEE, providing appropriate remote environmental and field-programmable gate array (FPGA) status parameters. In addition, the FEE sends detector scientific data and clock signals via a low-voltage differential signaling (LVDS) bus at 80 Mb/s with a dual-channel hot backup. According to the results of the electrical tests on the electronics, the channel's root mean square (rms) noise is less than 1.7 fC, and the linearity is better than 0.2%. In addition, a beam test is performed on the super proton synchrotron (SPS) and proton synchrotron (PS) terminals of the European Organization for Nuclear Research (CERN) to verify the electronic performance of the proposed system. The results show that the proposed FEE can meet the readout requirements of the TRD prototype and can accurately obtain the energy spectrum of muons and electrons.**

***Index Terms*— Front-end electronics (FEEs), high-energy cosmic radiation detection facility (HERD), SAMPA, transition radiation detector (TRD).**

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I. Introduction

THE observational data and results from numerous astronomical studies suggest that dark matter is widely distributed throughout the universe, accounting for approximately 27% of the total mass of matter. It plays a crucial role in matter's origins and the universe's evolution. However, aside from its gravitational effects, human understanding of dark matter remains limited. The detection and study of dark matter particles could potentially lead to breakthroughs in existing physical models, possibly sparking a new revolution in physics. In recent years, numerous international experiments have been conducted to detect dark matter, such as the PAMELA satellite [1], the Fermi satellite [2], the CALET space detector [3], AMS02 experiment [4], and the DAMPE satellite [5]. China also plans to build the next-generation high-energy cosmic radiation detection facility (HERD) experiment to perform related research.

The HERD is planned to be installed on China space station (CSS) for operation starting around 2027 for about ten years [6], [7], [8]. It will be used to serve as a dark matter detector, a cosmic-ray instrument, and an observatory for high-energy gamma rays. It will be the most sensitive experiment for detecting cosmic rays in space [9], [10], [11], [12], [13]. As shown in Fig. 1, the HERD consists of five detectors. Among them, the 3-D imaging calorimeter (CALO) is used for energy reconstruction and identification of electrons and protons; the fiber tracker (FIT) is used for particle tracking [14]; the plastic scintillator detector (PSD) is employed for on-orbit real-time identification of low-energy gamma rays and offline identification of high-energy gamma rays [15]; the silicon charge detector (SCD) is introduced for charge measurements and cosmic rays' trajectory data acquisition [16]; the transition radiation detectors (TRDs) are used for TeV-level absolute energy calibration of high-energy cosmic rays, high-energy X-ray surveys, and gamma-ray burst to monitor [17], [18].

TRD is widely applicable in space high-energy physics experiments. A typical TRD structure consists of a radiator

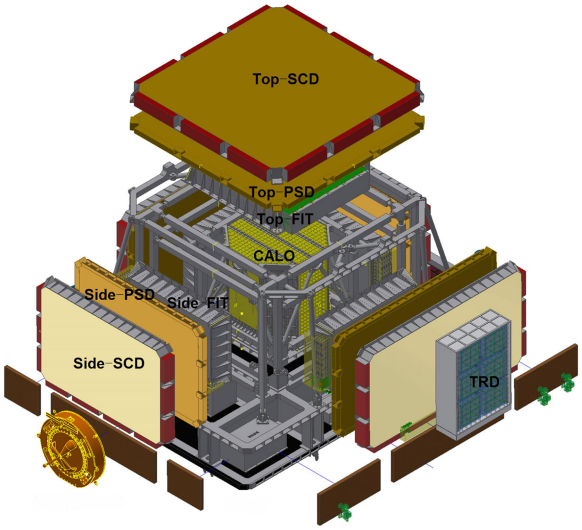

Fig. 1. HERD architecture. The HERD consists of the CALO, the FIT, the PSD, the SCD, and the TRD. TRD is mounted on the side of the HERD.

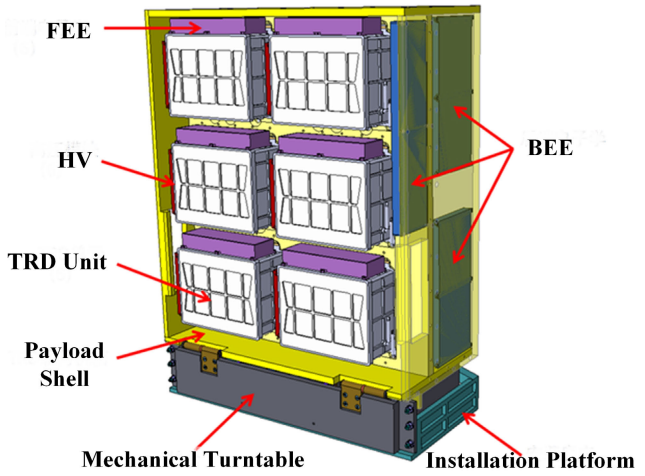

Fig. 2. Architecture of the TRD detection system. The TRD detector has six detector units organized into a 2 × 3 structure.

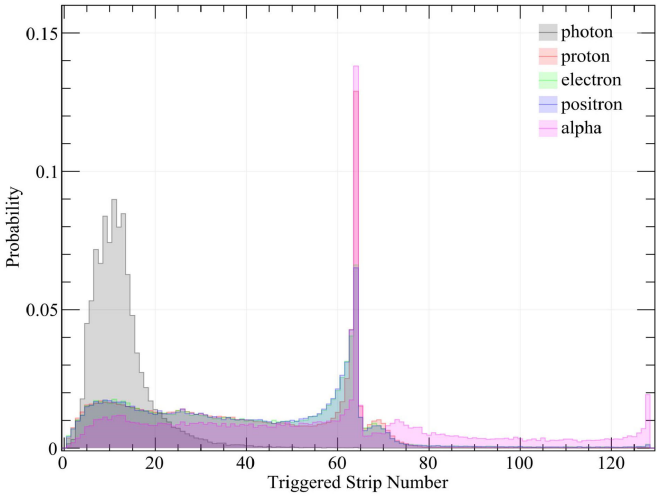

Fig. 3. Distribution of the number of triggered channels for different particles. The number of triggered channels for photons is about 10, and the number of protons and alpha particles is larger than 60.

and a gas X-ray detector. TRD is important in space experiments for studying highly relativistic cosmic rays. They are commonly used for energy measurements of energetic particles and distinguishing between particles with the same energy but different masses [19], [20]. In the early days, TRD was usually carried on balloons for space exploration, such as the Wizard/TS93 [21] and HEAT experiments [22]. They perform energy spectrum measurements of energetic particles by TRD and identify the particles. Recently, TRD has been commonly carried out on satellites and space stations. The PAMELA telescope [23] used TRD to identify particles at relativistic energy; AMS-02 [24], a high-energy physics experiment installed on the International Space Station, improves the accuracy of particle identification by TRD.

The TRD in the HERD experiment used an X-ray gas detector based on double-layer thick gaseous electron multipliers (THGEMs). It ensures that the TRD detector unit can be produced at a low cost and on a large scale. The TRD is mounted on the windward side of the HERD using a mechanical turntable, with an outer envelope size of 1020 × 680 × 300 mm and a total weight of 132.6 kg. As shown in Fig. 2, the TRD has a total of six detector units, laid out in a 2 × 3 configuration, with a total effective geometric detection area of 1800 cm^2. The initial state is an upright posture. High-energy cosmic-ray protons are incident from in front of the TRD. The radiator first converts them into transition radiation (TR) photons. Then, the TR photons enter the gas detection chamber and undergo photoelectric conversion, drift, multiplication, and collection to complete the detection of the TR photon signals to obtain the TR response of effective cosmic-ray proton events triggered by the CALO. The TRD's TR calibration curve on the ground is used to achieve absolute energy calibration of the TeV-level high-energy cosmic rays. Afterward, the TRD is rotated by 90° through the turntable to a lying attitude, with the backside of the detector as an incident surface; the high-energy X-ray photons pass through the metal shell structure and enter the gas detection chamber directly for high-energy X-ray measurements and gamma-ray burst to monitor.

As shown in Fig. 3, the spatial distribution of particles varies along the drift direction in the detector, causing some triggered channels in the detector to be different. The TRD prototype requires 128 channels for the readout of the anode signal. The distribution of the number of photons in triggered channels is concentrated at approximately 10, while the number of protons and alpha-triggered channels is larger than 60. By introducing the triggered channel judgment, the particle identification accuracy can be improved. The readout electronics of the TRD prototype need to have a dynamic range of 100 fC, as well as the detector environmental parameter monitoring function and the triggered channels discrimination function. To this end, this study proposes high-performance and high-reliability front-end electronics (FEE).

In this article, we describe the design and performance testing of the FEE for the TRD prototype. Section II describes the architecture of the TRD system. Section III describes

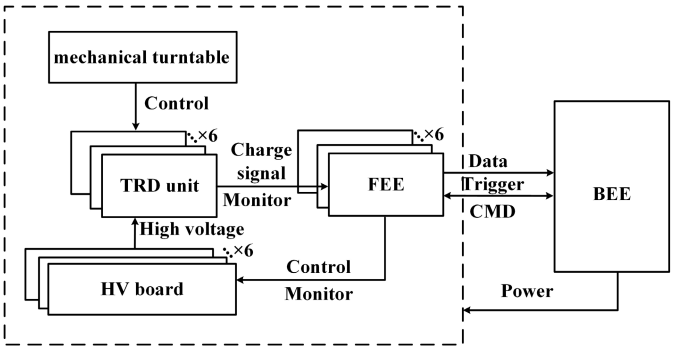

Fig. 4. Block diagram of the TRD system. The TRD system consists of six TRD detector units, six FEEs, a BEE, six high-voltage units, and a mechanical turntable.

the hardware design of FEE and the firmware design of the field-programmable gate array (FPGA). Section IV describes the results of the laboratory and beam performance tests, and Section V provides a summary.

II. Architecture of the TRD System

The architecture of the TRD system is shown in Fig. 4, where it can be seen that the TRD system mainly consists of six TRD detector units, six FEEs, back-end electronics (BEE), six high-voltage units, and a mechanical turntable. The TRD detector unit consists of two parts: a regular radiator and a gas detector based on THGEM. The detector unit completes the conversion of the TR photon signals of high-energy charged particles, the photoelectric conversion of high-efficiency TR photon signals, the multiplication and amplification of high-gain optoelectronic signals, and the readout. The anode of the TRD detector unit produces a direct measurement signal from the ionization of charged particles, and the electrons generated by the ionization process enter the THGEM for amplification through the drift region. The magnitude of which depends on the magnitude of the ionization signal and the gas multiplier. These are affected by the temperature and the internal operating gas of the detector. The TRD is designed as a sealed gas detector, and the FEE is used to monitor the temperature and gas pressure of the detector to ensure its operational stability. The FEE receives the charge signal from the TRD detector unit and performs the amplification, shaping, sampling, and data compression operation on this signal. Each FEE is configured with four SAMPA chips to provide 128 channels of signal readout. The TRD subsystem has a total of 768 channels. The BEE communicates with the six FEEs to configure FEE commands and summarize detector scientific data; it also provides power inputs to the FEE, high-voltage power boards, and the mechanical turntable. In addition, the BEE communicates with the integrated electronics through FC-AE-1553 and MIL-FEESTD-1553B for transmission of control and load data. The mechanical turntable performs attitude switching between the energy calibration mode and the independent observation mode according to the TRD operating mode command. Each high-voltage module is responsible for providing three high-voltage biases for the TRD detector unit: one 5100 V and two 1700 V. The configuration of the high-voltage module and telemetry of its environmental parameters are performed using the FEE.

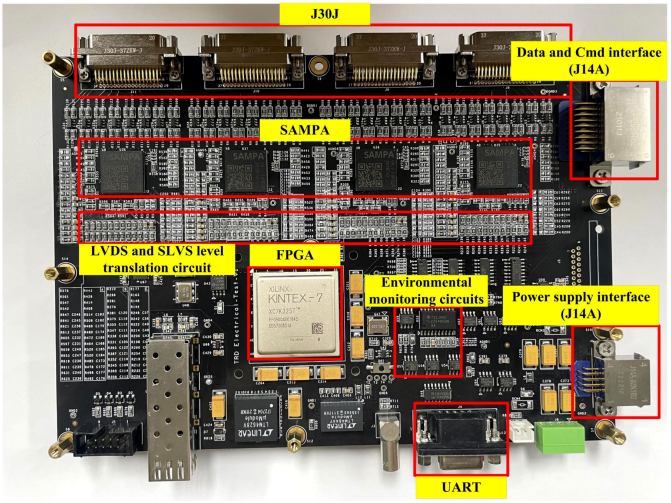

Fig. 5. Picture of the FEE. The power consumption is approximately 6 W. The key modules and interfaces are marked by red rectangular boxes.

III. Architecture of the FEE

A. Hardware Design of the FEE

The picture and block diagram of the FEE are presented in Figs. 5 and 6, respectively. The FEE includes seven circuit modules, including detector interface input circuits, level shifter circuits, an FPGA and its peripheral circuits, SAMPA and its peripheral circuits, power supply circuits, data communication circuits, and environmental parameter monitoring circuits. The FEE uses four SAMPA application-specific integrated circuits (ASICs) for high-speed readout of 128 detector signals, and the detector signals are fed to SAMPA through four J30J-37ZKW-J connectors interface. The SAMPA uses scalable low-voltage signaling (SLVS) levels for communication and configuration links to achieve low-power operation. The FEE designs resistor networks to realize level shifting between the SLVS and the low-voltage differential signaling (LVDS) levels. The FPGA is XC7K325T-2FFG900I from Xilinx, and it is mainly responsible for data processing and transmission, and BEE command parsing. Command configurations, status parameter responses, and trigger signals are transmitted between the FEE and the BEE via an RS-422 bus, and scientific data and clock signals are transmitted via an LVDS bus with a transmission rate of 80 Mb/s. The BEE provides the power of +3.3 and +5 V to the FEE via the J14A-9ZK1B connector. This power is converted by the direct current to direct current (dc–dc) and low-dropout (LDO) chips on the FEE to the appropriate lower voltages used to supply the SAMPA, FPGA, and other components. Furthermore, scientific data, clock signals, and trigger signals are sent in the simplex mode with dual-channel hot backup. Command configuration and environmental parameter replies are sent in the half-duplex mode with a dual-channel hot backup.

The SAMPA is a digital–analog hybrid ASIC developed by the European Organization for Nuclear Research (CERN) for the upgrade of the ALICE time projection Chamber (TPC)

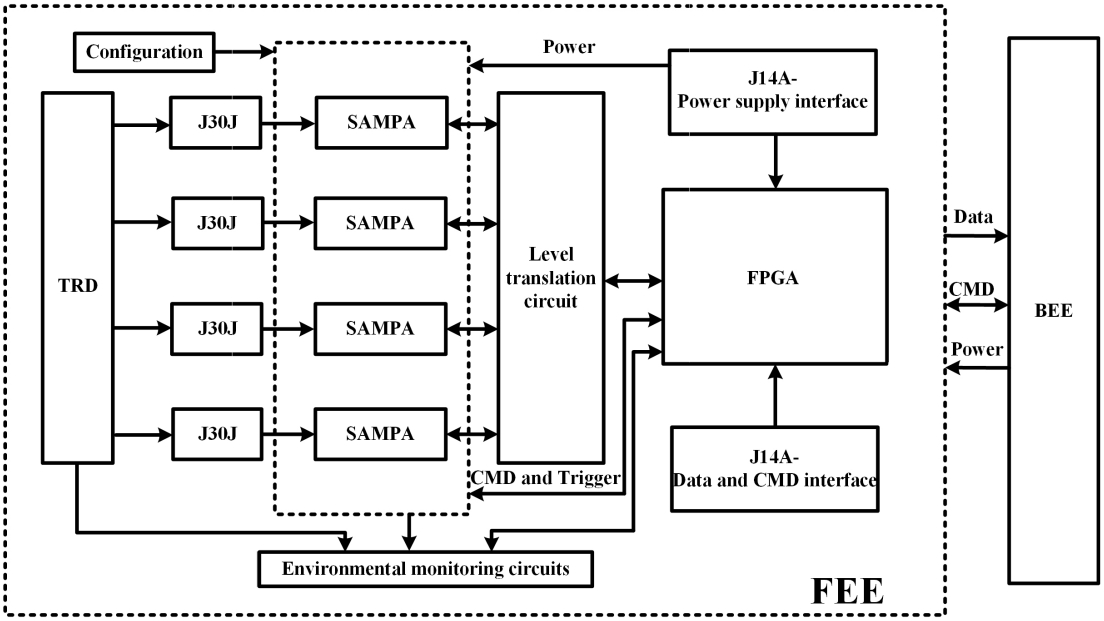

Fig. 6. Block diagram of the FEE. The FEE consists of seven circuit modules, including the detector interface input circuit, the level shifter circuit, the FPGA and its peripheral circuits, the SAMPA and its configuration circuits, the power supply circuit, the data communication circuits, and the environmental parameter monitoring circuits.

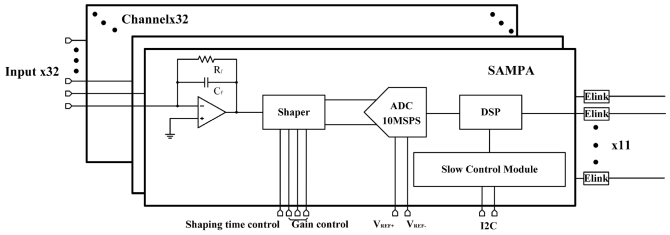

Fig. 7. Block diagram of the SAMPA ASIC consisting of analog and digital parts that are divided by internal ADC. Each SAMPA has 32 analog input channels and the digital signals are transmitted to the FPGA via 11 e-links.

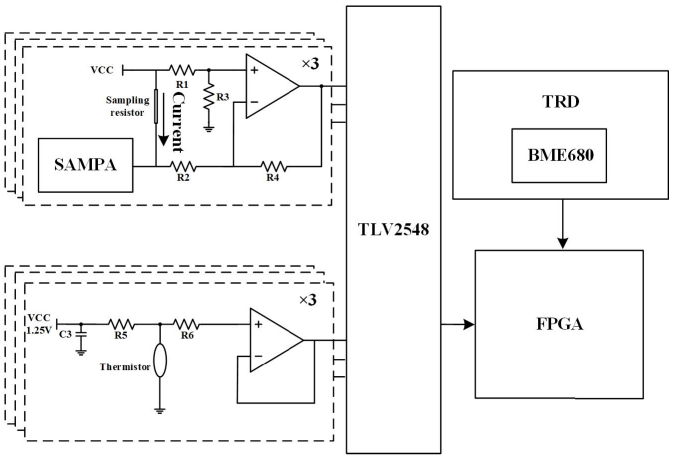

Fig. 8. Design of the FEE and detector environmental parameters monitoring circuit. The circuit is designed using thermistors, sampling resistors, operational amplifiers, and an ADC.

and the ALICE muon Chambers (MCH) [25], [26], [27]. The block diagram of the SAMPA is presented in Fig. 7. It should be noted that the SAMPA's signal charge polarity, gain (4, 20, or 30 mV/fC), and shaping time (160 or 300 ns) can be configured via external pins on the chip. The other configurations of the SAMPA can be configured via the built-in registers. The chip can be divided into two parts, analog and digital, which are divided by a 10-bit ADC: 1) the analog part includes a charge-sensitive amplifier, a semi-Gaussian pulse shaper module, and a noninverting stage; and 2) the digital part consists of a digital signal processor (DSP) and a slow control module [28], [29], [30]. The DSP processed data for 32 channels are read out via 11 e-links. The SAMPA chip can compress the raw data by the DSP, operating in the zero-suppression mode, thus reducing the data transmission stress [31], [32]. In addition, radiation experiments have proved that the chip has strong anti-radiation ability. The performance of the SAMPA chip fulfills application requirements of space exploration [33]. The design of the FEE is based on the SAMPA chip. Four SAMPA can accommodate 128 anode signal readouts and offer a dynamic range of 100 fC.

Furthermore, to prevent sudden changes in the high voltage of the detector, higher transient voltages can be generated by coupling through the detector's PAD to the FEE input. As well as to minimize detector signal input noise. A clamp protection circuit and a filter circuit are designed at the SAMPA input in the FEE. The circuit consists mainly of capacitors, resistors, and diodes. A series resistor is used in the circuit for current limiting, and an electrostatic discharge (ESD) protection diode (NUP4114) provides overvoltage clamping to protect the signal input circuitry of the SAMPA. A 1-MΩ shunt resistor to the ground and a 220-pF series capacitor are used for signal filtering to reduce the noise. The FEE and detector environmental parameter monitoring circuits are designed on the FEE. As shown in Fig. 8, each FEE has three temperature- and three current-monitoring points. The temperature-monitoring

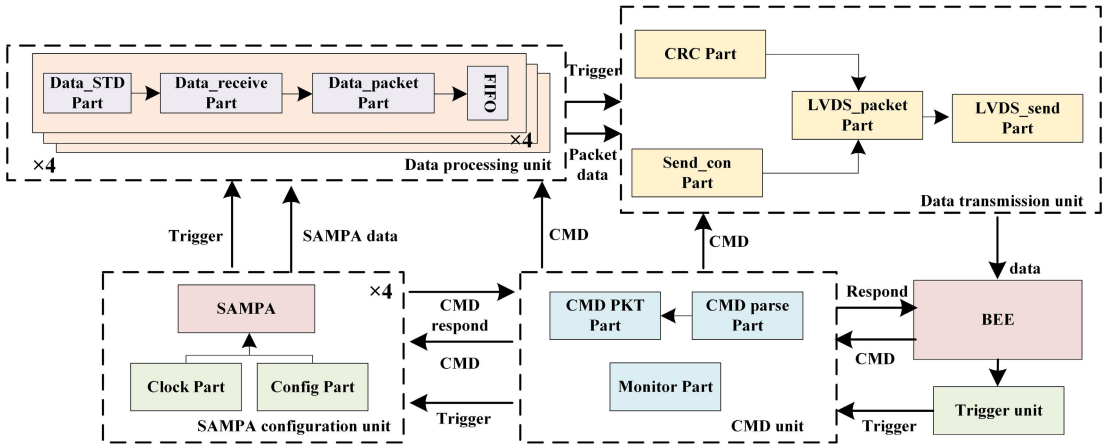

Fig. 9. Architecture of FPGA firmware. It consists of five modules: a trigger unit, a CMD unit, a SAMPA configuration unit, a data-processing unit, and a data transmission unit. It is mainly responsible for processing detector input signals from SAMPA, parsing commands from BEE, data packing, and transmission.

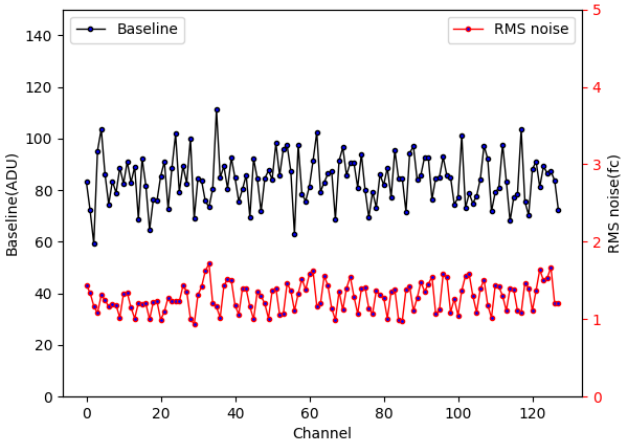

Fig. 10. Baseline and rms noise of 128 channels. The FEE baseline is between 60 and 110 ADC values, and the rms noise is less than 1.7 ADC values (approximately 0.17 fC).

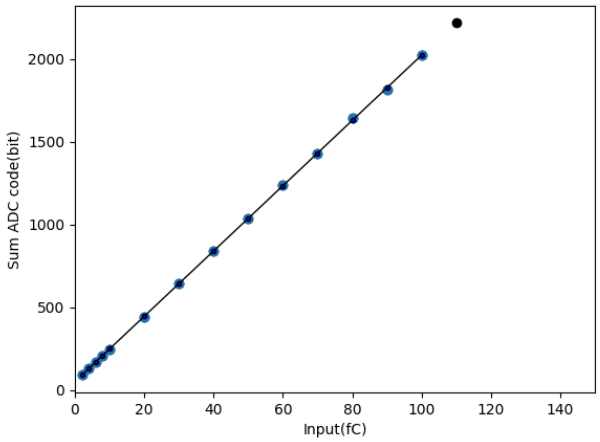

Fig. 11. Result of the linearity test. The linearly fit function $y = 19.71x + 50.44$. Its INL was better than 0.7%.

process is focused on the temperatures of the SAMPA, FPGA, and FEE printed circuit board (PCB). The monitoring is conducted every 16 s, and the circuit is designed using thermistors, operational amplifiers, and an ADC. The current monitoring tracks the three operational currents of the SAMPA, which correspond to the analog voltage of +1.25 V, digital voltage of +1.25 V, and analog voltage of +1.1 V. The three currents are monitored every second, and the circuit mainly consists of current sampling resistors, operational amplifiers, and an ADC. An eight-channel TLV2548 from Texas Instruments is selected for the ADC, and it is controlled and processed by the FPGA. When the FPGA continuously monitors two abnormal currents, it will automatically power down the SAMPA and restart it after a 10-ms interval. The environmental parameters of the detector are monitored by the BME680 chip, which monitors the temperature and air pressure inside the detector and communicates directly with the FPGA through the detector input interface.

B. FPGA Firmware Design of the FEE

The block diagram of the FPGA's firmware architecture is presented in Fig. 9, where it can be seen that it consists of five modules: a trigger unit, a CMD unit, a SAMPA configuration unit, a data-processing unit, and a data transmission unit. When the FEE is operating, the BEE sends the corresponding configuration commands to the FEE via an RS422 bus and then decodes and verifies data integrity at the CMD unit. The command channel can change SAMPA's time window and gain configuration. After determining the command type, the CMD unit sends this information to the corresponding configuration register and replies with a response command. The BEE transmits the trigger signal to FEE via the RS422 bus, and the trigger unit determines whether the trigger pulse level meets the requirement for the width of 400–600 ns to avoid interference signals. In the data-processing unit, the SAMPA receives the trigger signal from the FPGA and controls the transmission process of the entire data link. First, SAMPA's data will have a serial-to-parallel convert operation in this unit, discarded empty packets and invalid synchronization packets, then inserted the start flag bit and FIFO status judgment bit, and finally transmitted to the data transmission unit. The data in the data transmission unit will be inserted and reassembled with CRC check bits to check the reliability of the transmission signal, and the trigger number will be added to facilitate

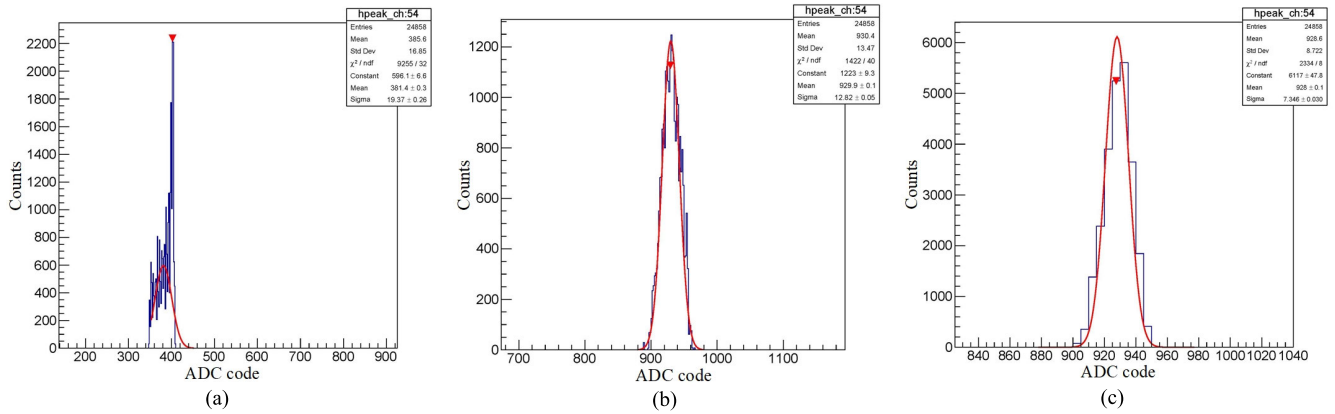

Fig. 12. Pulse height distribution was obtained using (a) peak search method, (b) integrating samples method, and (c) 4th-order semi-Gaussian waveform fitting method in the signal region. The input charge value was 50 fC, and 24858 events were recorded. (b) and (c) Integrating samples method and waveform fitting method performed well, and the amplitude resolution of the waveform fitting method is the best resolution of 2.21%.

the restoration of accurate waveforms during subsequent data analysis.

IV. Performance Measurement

A series of tests were performed to evaluate the functionality and performance of the proposed FEE design. The SAMPA was configured with a dynamic range of 100 fC, a gain of 20 mV/fC, and a data transmission clock frequency of 80 MHz. In the laboratory tests, a signal generator (Tektronix AFG31000) generated a trigger signal for the BEE, which fanned out to the FEE.

A. Baseline Characterization Test

The ionization signal energy on an anode strip has an average ionization value of approximately 0.5 keV, and the TR signal energy on an anode strip is nearly 10 keV. The detector requires the FEE readout signal range that can cover both the ionization signal and the TR photon signal, and the electronics noise that differs by more than one order of magnitude from the ionization signal. When the ionization signal is about 50 ADC code, the noise level should be below five ADC code. The baseline and root mean square (rms) noise of the FEE were tested. The BEE provided the trigger signal at a frequency of 1 kHz. The FEE operated in the raw data mode with a time window of 100 μs. Fig. 10 shows the baseline and the rms noise for 128 FEE channels. The FEE baseline is between 60 and 110 ADC values, and the rms noise is less than 1.7 ADC values (approximately 0.17 fC). The noise level of the FEE meets the requirements of the TRD and improves signal measurement reliability.

B. Channel Linearity Test

The linearity test was performed using a signal generator, which produces voltage pulses from 0 to 10 mV in steps of 2 mV and from 10 to 110 mV in steps of 10 mV, which were converted into corresponding charge pulses by a 1-pF capacitor. The trigger frequency was set to 1 kHz, and the delay time between the signal and the trigger was 1 μs to ensure that the signal was within the reading time window. Fig. 11 shows the results of the linearity test for one channel. Its integral nonlinearity (INL) was better than 0.7%.

C. Pulse Height Distribution Test With Different Methods

To analyze the features extracted from the recorded signals, we used different methods, including the peak search method, the integrating samples method, and the fourth-order semi-Gaussian waveform fitting method, as shown in Fig. 12. The test was performed with a trigger signal having a frequency of 1 kHz, the SAMPA was configured in the zero compression mode, and the SAMPA input equivalent charge was 50 fC. The test yielded a total of 24 858 valid events. As shown in Fig. 12, the peak search method has the worst results among all the methods. This was because the limited number of sampling points in the SAMPA cannot guarantee that the peak value of the waveform is accurately captured. However, both the integrating samples method and the waveform fitting method performed well, and the amplitude resolution of the waveform fitting method is the best resolution of 2.21%.

D. Beam Test of the TRD Prototype

To further verify the performance of the FEE, we performed electron and muon beam tests from August 2023 to September 2023 on the proton synchrotron (PS) and super PS (SPS) accelerator at the CERN. The operating gas of the detector was 95% Ar + 5% C_4H_{10}.The FEE trigger signal was provided by HERD's trigger system, and it was sent to the FEE through the BEE with a trigger rate of about 300 Hz. The test setup is shown in Fig. 13. The test system consists of the TRD detection unit, the FEE, the BEE, and a high-voltage power supply. The particle beam is emitted from the accelerator and hits the detection-sensitive region of the TRD. The charge signal generated by the detector is collected by the FEE and transmitted to the server in real time via the BEE. Fig. 14 shows the test results for 150-GeV electrons and 150-GeV muons. The energy of the TR is proportional to the Lorentz factor (γ) of the incident-charged particle. When γ of the incident particles is 10^3, the energy of the incident particles corresponds exactly to the energy of the photons produced by the TR, and the TR photons tend to be saturated when the incident charged particles are 10^4. The γ of 150-GeV muons is about 1×10^3, which produces TR, while 150-GeV electrons have a γ of about 3×10^5, which is well above the saturation value for the production of TR. This difference is

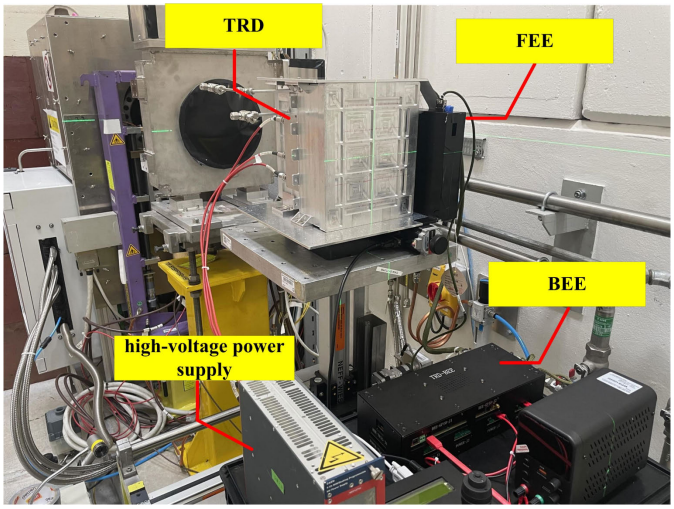

Fig. 13. Beam test system. The test system consists of TRD, FEE, BEE, and a high-voltage power supply.

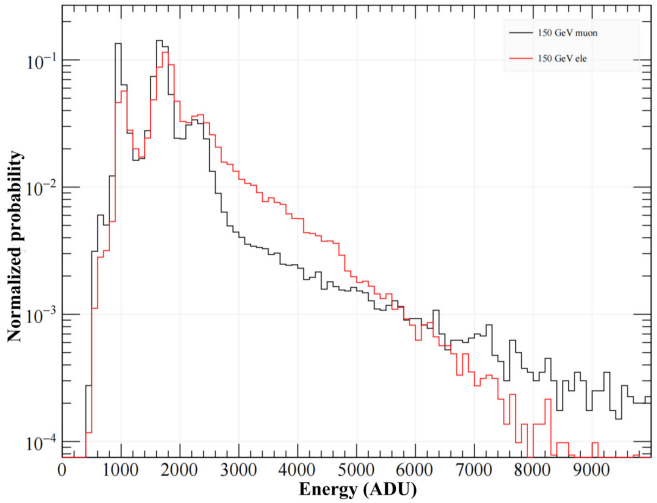

Fig. 14. Energy spectrum of 150-GeV electrons and muons. This difference between the 150-GeV electrons and 150-GeV muons is recognizable from the energy spectrum. This is because the 150-GeV electrons produce TR, and the TR photon produces additional energy.

recognizable from the energy spectrum. In addition, the FEE data transmission was stable and reliable without any data loss during the experiment.

V. Conclusion

In this work, the FEE is designed as a standard readout unit and developed for the prototype of TRD in the HERD. The FEE consists of detector interface input circuits, level shifter circuits, FPGA and its peripheral circuits, SAMPA and its peripheral circuits, power supply circuits, data communication circuits, and environmental parameter-monitoring circuits. The FEE is intended to provide 128 detector signal readouts with a dynamic range of 100 fC. The FEE has a total power consumption of approximately 6 W. The readout system was stable and performed well. The laboratory test results indicate that the rms noise of FEE is less than 1.7 ADC code (approximately 0.17 fC), and the nonlinearity of the readout electronics system is less than 0.7%. When the SAMPA input equivalent charge is 50 fC, the resolution of the FEE is better than 2.21% using the waveform fitting method. In addition, the beam test results with joint TRD demonstrate that the readout system can perform well.

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