VHDL Implementation of Trigger and timing filter for Nuclear Pulse Processing applications

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Introduction

In nuclear pulse processing applications, accurate estimation of arrival time of each individual pulse is required for better understanding of Nuclear events. Usually, time of arrival information is measured by a self-trigger based on a programmable voltage threshold by traditional analog approach. In this approach the trigger is generated as soon as the input signal crosses that threshold [1]. For accelerator-based experiments the fast timing output of the preamplifiers are used to generate the timing signals. Analog processing units such as CFD (Constant fraction discriminators) are used to reduce the jitter. With fast analog to digital converter (ADC), it is possible to implement a digital timing filter so as to avoid these analog processing units. Because of the baseline fluctuation, pulse pile-up, noise, etc. direct digital comparison is not a feasible solution for trigger generation in such application. However, the ability to find desired pulses and discriminating them from the noise is very critical. In fact, missing pulses or false triggers can cause loss of important events, bad pile-up rejection, errors in the statistics and other unwanted effects. Therefore, a digital filter able to reject the noise, cancel the baseline and to measure the timing with high resolution and precision is required for this purpose. In this study digital filter RC-CR-CR is proposed, investigated and implemented to overcome stated shortcomings. This filter is able to reject the high frequency (RC low pass filter), restore the baseline, cancel the low frequency fluctuations (verified by simulation) and transform the input pulses into bipolar signals whose zero crossing (pulse amplitude independent) can be used for the determination of the time stamp [2]. This work includes simulation and hardware implementation of trigger and timing system on a Field programmable gate array(FPGA) kit. A RC-CR^2 filter is implemented on FPGA kit. Whenever a zero is detected at the output of the RC-CR^2 filter, a trigger has been generated. But fluctuation and noise due to combinational logic implemented can cause a false trigger generation. In this work for trigger generation, differences between two tap-ins of the output of the RC-CR^2 filter was taken and compared to a threshold.

Digital RC-CR^2 Filter

The recursive algorithm [2] that converts a digitized exponential pulse x(n) into a bipolar pulse $Y_3(n)$ is given as

$Y_1(n) = 0.15\ x(n) + 0.84\ Y_1(n - 1)$,

Here, $Y_1(n)$ is output of RC filter.

$Y_2(n) = 0.91\ Y_1(n) - 0.91\ Y_1(n-1) + 0.84\ Y_2(n - 1)$,

$Y_3(n) = 0.91\ Y_2(n) - 0.91\ Y_2(n-1) + 0.84\ Y_3\ (n - 1)$.

$Y_3(n)$, bipolar pulse, is the output of RC-CR^2 filter.

Trigger and timing information

For trigger and timing information the $Y_3(n)$ is used. A difference between two proximate samples (separated by 16 samples) is measured. This difference is compared with a threshold value. Whenever threshold value exceeds trigger is generated. This trigger pulse is given to a up counter to measure the timing information.
A simple block diagram of hardware representation of trigger and timing system is depicted in Figure 1.

Simulations and preliminary experimental tests

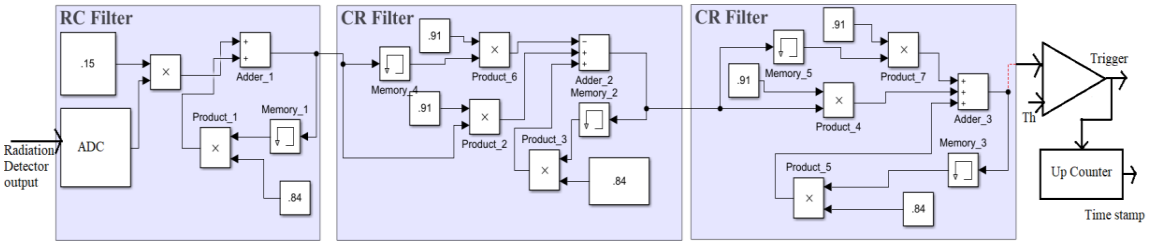

Fig. 1 Block Diagram of Trigger and Timing system

Here simulation is performed on pile-up pulse data acquired from HPGe detector using Cs-137 as the source. Simulation results are shown in Figure 2. On arrival of each pulse, trigger generation and baseline restoration occurred as observed by simulation result.

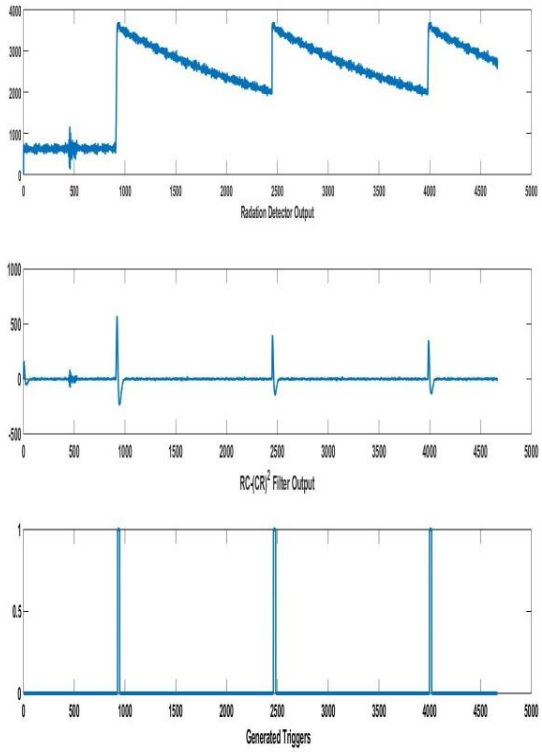

Fig. 2 Simulation on pile-up data

Experiment setup and procedure-: For the hardware implementation, digital conversion of exponentially decaying detector output (generated by arbitrary function generator) by high speed analog to digital converter (ADC) is done. A clock of 50 Mhz is used for this purpose. Filter is implemented on FPGA for fast processing. ADC digitized data is processed in RC_CR^2 filter. Processed data is transferred to computer over Ethernet for observation.

Observation from experiment-:

Processing speed of 50 Mbps achieved. Trigger pulse is observed with 50 ns jitter. Trigger is also generated for pile up data. Input pulse amplitude independent behavior observed.

Conclusion

Efficient algorithms for time stamp measurement of nuclear pulse have been developed and implemented on hardware. This algorithm operates at 50 MHz rate and gives pulse amplitude independent trigger with low jitter. Jitter value of 50 ns is sufficient for many event time stamp applications. Based on this event identification further processing of data for charge, shape etc. can be carried out. For jitter minimization we will use interpolation technique for zero crossing detection in our future work.

References

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