A 128 Channel Analogue Pipeline Chip for MSGC Read-out at LHC

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Abstract

A 128 Channel analogue pipeline chip has been made for the read-out of CMS MSGC detectors at the LHC. Developed from the APV series, it features slow shaping and a deconvolution-type algorithm optimised for MSGC signals. Leakage current compensation has been employed, and leakage current monitoring provides warning of possible MSGC breakdown. The first version of the circuit has been fabricated using Harris AVLSI-RA radiation hard technology.

1. INTRODUCTION

Over the last few years, a series of CMOS chips, the APV circuits [1], has been developed to read out silicon microstrip detectors for the CMS. This architecture has been further developed and modified to optimise it as far as possible for MSGCs whilst minimising the circuit changes required.

The CMS MSGCs have lower capacitance than the silicon strips which has implications on the noise performance, and they are required to be DC coupled to the front-end, so the chip must be immune to leakage currents. MSGC strips are also prone to breakdown causing discharges which may damage the strips and the electronics. Warning must be given so that damage can be avoided. In addition the weights of the deconvolution algorithm have been modified to achieve sufficient timing resolution for the expected MSGC signal shape.

The chip has three modes of operation. One mode, Deconvolution, is used in normal operation when data rates are sufficiently high such that the effects of pile-up are significant. The second, Peak, is used when pile-up is not significant and a larger signal to noise ratio is required. The third, Multi, is a test mode which allows multiple consecutive pipeline columns to be triggered and read out.

Additional features include a dedicated calibration circuit for fine timing resolution, programmable pipeline latency, and an on-chip bias generator, all of which are programmable through a Philips I^2C compatible interface, and apart from the current monitoring outputs the pin-out is fully compatible with the silicon version.

2. CHIP OVERVIEW

The APV-MSGC (figure 1) is an analogue pipeline ASIC intended for read-out of MSGC detectors in the CMS tracker. The architecture of the CMS tracker read-out system is based on analogue processing of data in the detector prior to transmission in analogue form to the DAQ.

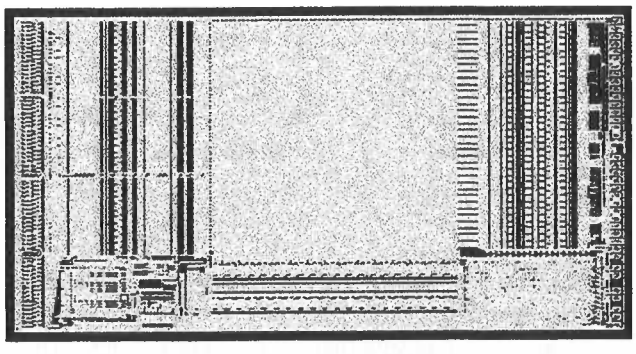

Figure 1 APV-MSGC chip

The chip contains 128 channels of preamplifier and shaper driving a 160 column analogue memory into which samples are written at the LHC 40MHz frequency. The memory always contains a record of the most recent beam crossing that the chip has sensed, and data access mechanisms allow the triggering and queuing of data in the memory for output. Triggered data are then processed with a deconvolution-type filter (APSP) - a switched capacitor network which deconvolves the shaping function of the preamplifier and shaper stages to give a pulse shape with sufficient timing resolution for MSGC signals. Following the APSP, data are held in a further buffer until they can be read out serially through an analogue multiplexer at 20MHz. The APV-MSGC also contains features required for eventual use in CMS including a programmable bias generator, an internal test pulse generation system, and a slow control communication interface.

The APV-MSGC is developed from the APV6 - the silicon microstrip read-out chip - but has been redesigned to optimise it for MSGC signals. To achieve this several modifications have been made to the APV6.

1. Front-end modified to optimise for MSGC capacitance
2. Addition of a leakage current compensation circuit
3. Addition of leakage current monitor circuit to warn potential detector breakdown
4. Additions to bias generator for biasing above circuitry
5. Deconvolution algorithm changed to optimise for MSGC signal shape
6. New mode of operation for reading out consecutive triggers

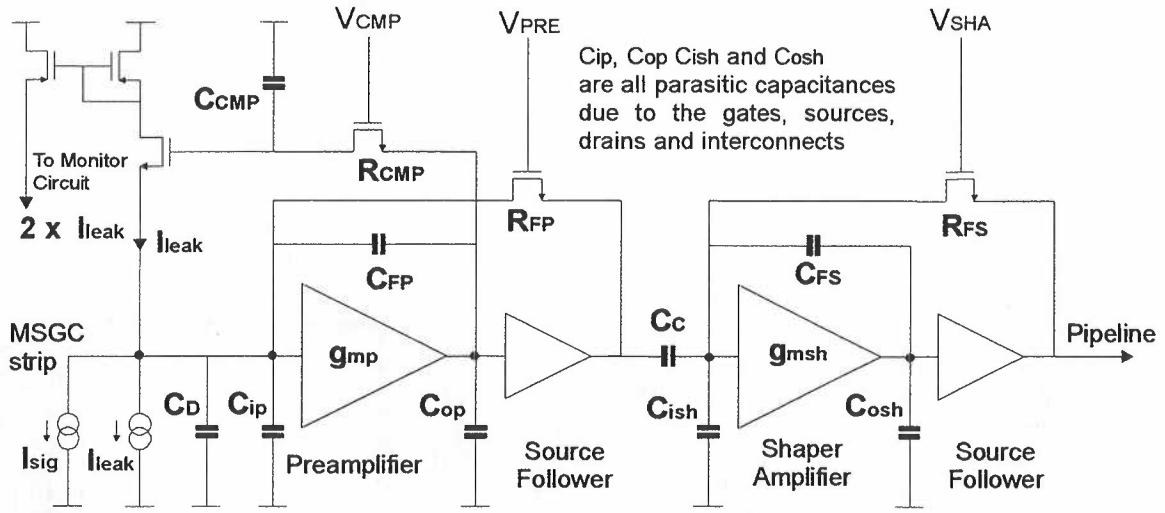

Figure 2 Schematic of Front End

At this stage it was not thought practicable to include a baseline restoration circuit for each channel. This would have been used to ensure that the preamplifier and shaper recovered quickly following saturation by very large signals. Inclusion would have meant increased chip size due to the additional circuitry required in each channel and the modifications necessary to the bias generator.

3. FRONT END

The front-end electronics of the APV-MSGC chip (figure 2) are essentially the same as that for the APV6, but with slight modifications for noise optimisation and pulse shape adjustment, and additional circuitry for detector leakage current compensation and monitoring. In addition the input protection diodes have been increased in size to make them comparable with those found in the PreMux128 - a 128 channel preamplifier-shaper chip which has been extensively used in the characterisation of the MSGC detectors.

3.1 Preamplifier

The preamplifier is a charge amplifier made from a single-ended folded cascode amplifier with a 250fF feedback capacitor and a long channel nfet feedback transistor. The pfet input transistor has a size of 1600/1.4 and is biased at 400μA. Its source is connected to GND to reduce power consumption. The gain of the preamplifier is 15.4mV/silicon MIP (where a silicon MIP = 24000 electrons).

The output is buffered by a source follower which also provides the level shift required for DC stability through the feedback transistor. The feedback transistor also provides a discharge path, in order to avoid pile-up in the preamplifier, and is usually set to give a resistance in the order of 100MΩ

The transimpedance gain of the preamplifier is

$$\frac{V_{out}}{i_{in}}(s) = -\frac{R_{fp}}{\left(1+sC_{fp}R_{fp}\right)\left(1+s\dfrac{\left(C_{fp}+C_{op}\right)\left(C_D+C_{ip}+C_{fp}\right)}{g_{mp}C_{fp}}\right)}$$

3.2 Shaper

The shaper is derived from the same folded cascode amplifier architecture as the preamplifier with a 250fF feedback capacitor but a shorter nfet feedback transistor. The input coupling capacitor is of magnitude 1.8pF. The pfet input transistor has a size of 400/1.4 and is biased at 88 μA.

The voltage gain of the shaper is given by

$$\frac{V_{out}}{V_{in}}(s) = -\frac{sR_{fs}C_c}{\left(1+s\dfrac{R_{fs}C_{fs}}{2}\right)\left(1+s\dfrac{\left(C_{fs}+C_{osh}\right)\left(C_c+C_{ish}+C_{fs}\right)}{g_{msh}C_{fs}}\right)}$$

This is equivalent to a CR-RC shaper with a peaking time

$$t_{peak} = \frac{R_{fs}C_{fs}}{2} = \frac{(C_{fs}+C_{osh})(C_c+C_{ish}+C_{fs})}{g_{msh}C_{fs}}$$

and a peak voltage given by

$$V_{peak} = \frac{2C_c}{eC_{fs}}V_{in} = 5.3 \times V_{in}$$

The total gain due to both the preamplifier and shaper is therefore 81.5mV/Silicon MIP. Perfect CR-RC shaping is not achieved since the output of the preamplifer has a finite rise time (in the order of 10ns). Therefore to achieve an overall peaking time of 50ns, the shaper must be adjusted to have a shaping time of around 40ns.

3.3 Leakage Current Compensation

Current from an MSGC comprises two components - the signal due to ionising particles passing through the chamber, and a DC leakage current. Leakage would

cause a voltage to form across the feedback transistor of the preamplifier. The preamplifier would be able to cope with very small leakage currents, however increasing radiation damage to the MSGC may cause the leakage current to increase to such a point that the preamplifier is pushed out of its optimum operating point. Such a situation is undesirable.

To overcome the problem of leakage current, the preamplifier has been modified to include a *leakage compensation circuit*. This consists of a voltage controlled current source which senses the voltage at the preamplifier output. If a leakage current causes the preamplifier output voltage to change then sufficient current is supplied to the MSGC strip such that none is drawn across the feedback transistor. The circuit has been implemented using an nfet as the current source (figure 2) whose gate is connected directly to the preamplifier output. A long channel nfet forms part of an RC time constant (adjustable using *Vcmp*) that ensures only the leakage current, and not the signal, is compensated.

The sourcing current is mirrored out from the front end to the *leakage current monitoring circuit* which will be described later.

3.4 Noise

By far the largest contribution to the front-end noise comes from the input transistor in the preamplifier. The input transistor is half the size of that in the APV6 since the lower capacitance of the MSGC strips means the transconductance and gate capacitance of the input transistor can be reduced.

4. ANALOGUE PIPELINE

The analogue pipeline buffers data coming from the detectors for sufficient time until the level1 trigger is processed. The trigger latency is 3.2μs equivalent to 128 pipeline columns.

4.1 Analogue Memory

The pipeline consists of an array of 128 X 160 switched capacitor elements. One side of each capacitor connects to VSS and the other to the write and read switches. The capacitor has a size of 250fF.

4.2 Control

The pipeline control is required to have the following functions:

- Sequence the writing of data into the analogue array.
- Mark useful (triggered) data.
- Remember which elements contain triggered data.
- Avoid writing over triggered data until they have been read out.
- Sequence the retrieval of data.

A write pointer continuously circulates the pipeline sampling the shaper output from each channel at intervals of 25ns. A trigger pointer follows behind the write pointer, separated by the trigger latency. When a trigger is received , depending on the mode of operation, either one, or three consecutive columns (figure 3) within the pipeline, are reserved for reading out. Once reserved these columns cannot be overwritten until the data have been read out. Therefore, on their next pass the write and trigger pointers will skip the reserved columns.

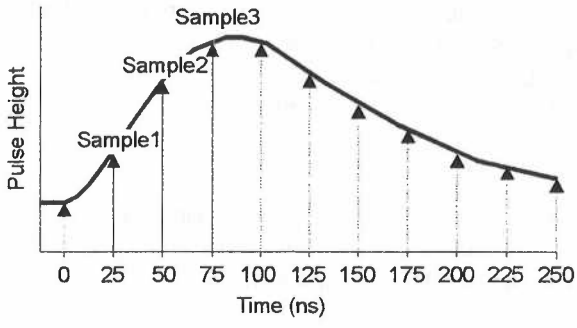

Figure 3 Sampling of shaper output signal.

Columns within the pipeline are grouped in pairs. This was done to reduce the amount of control logic required. The column pairing means that for each column triggered, both it and its pairmate are reserved and *both* are skipped over until the triggered column has been read out. If a number of consecutive column-pairs are reserved in the pipeline then the pointers must skip all of these in one 25ns interval. Each pair introduces a 2ns delay which means only 12 consecutive column pairs can exist before the delay is such that the pointers disappear or are delayed by one clock cycle. The separation between write and trigger pointers is monitored so that if it deviates from the programmed latency an error flag is set.

The addresses of triggered columns are stored in a FIFO which has a depth of 20. Therefore, depending on the mode of operation, either 20 or 6 triggers can be buffered in the pipeline before the FIFO overflows. If an overflow does occur an error flag is set.

5. ANALOGUE PROCESSING

The previous version of this chip, the APV6, was designed for read-out of silicon strip detectors. Signals from silicon strip detectors come as single impulses of current which can be integrated in a charge amplifier and shaped using a CR-RC shaper into a well defined voltage pulse. Deconvolution can then be performed on the sampled signal in order to recover the original impulse signal, thus confining it to one beam crossing interval. In the APV6, this deconvolution was performed using a switched capacitor filter with a three weight algorithm. The weights of the capacitors were determined from theory due to the well defined shape of a CR-RC signal.

Signals from MSGC detectors, however are not so well defined as their silicon counterparts. A simulation study

was undertaken at Imperial College [2] in order to determine the optimum algorithm for processing MSGC signals to give sufficient timing resolution for CMS purposes. Good results were achieved using 50ns CR-RC shaping of the MSGC signal, a sampling interval of 25ns and a three weight signal processing algorithm. This has the advantage that these functions are already implemented on the APV6 chip and minimal effort would be required to convert it for MSGC use. Another advantage in keeping the algorithm logically compatible with the silicon version is that synchronisation is maintained between read-out of silicon strip detectors and MSGC detectors. This reduces the cost and complexity of the data acquisition electronics.

5.1 APSP Weights

The new APSP (Analogue Pulse Shape Processor) uses the three weight deconvolution optimised for MSGC signals (figure 4). The weights are:

weight 1 = -1.202 (applied to sample 1 in figure 3)
weight 2 = 0.172 (applied to sample 2 in figure 3)
weight 3 = 0.858 (applied to sample 3 figure 3)

These have been translated into capacitor weights of

C1 = -2pF
C2 = 0.286pF
C3 = 1.428pF

Capacitor *C1* has been divided into a capacitor of size 1.667pF and a capacitor of size 0.333pF. This is so that the output signals are of roughly equal magnitudes (per MIP) when operating in either Peak or Deconvolution modes. When in Deconvolution mode switch *dec_mode* is closed to give a capacitance of 2pF, and in Peak mode the switch is left open, giving 1.667pF.

5.3 Operation of APSP

In Deconvolution mode, the three samples (figure2) are read in sequence from the pipeline and written onto *C1*, *C2* and *C3* by closing and opening switches *ri1*, *ri2* and *ri3* in turn. They are then simultaneously read out through the amplifier by closing switches *ro* and *ro_dec*. To achieve the negative weight for *C1*, the capacitor is written onto one side and read out from the other.

In Peak mode, the single sample (from the peak of the signal) is read from the pipeline and written onto *C1* by closing and opening switch *ri1*. This is then read back out through the amplifier by closing only switch *ro*.

In both cases the gain for the last read operation is reduced by closing switch *last_cycle*. The resulting voltage is then sampled on a 1.77pF buffer capacitor before it is read out through the analogue multiplexer. There are two buffer capacitors which alternate every read-out cycle. This is so that APSP can process and store a data set while the previous data are still being read out through the multiplexer.

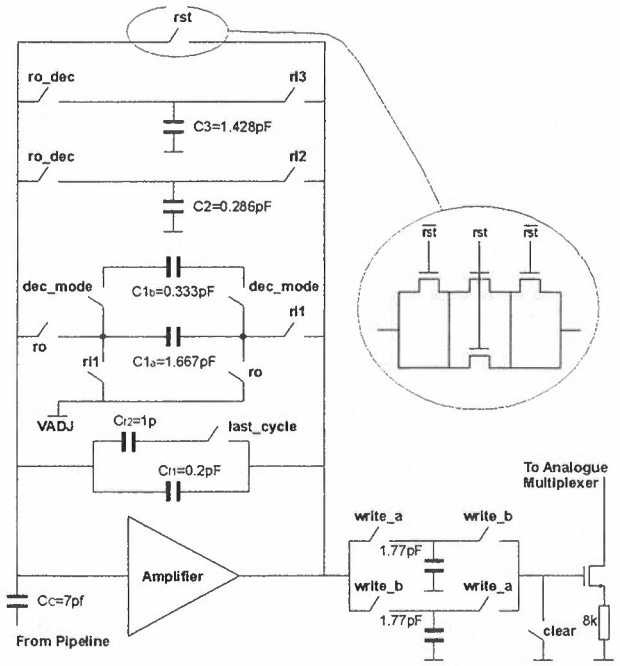

Figure 4 APSP circuit.

A third mode of operation called Multi-mode allows triggering of consecutive pipeline columns and read-out of each sample separately. Modes are selected by programming a dedicated mode register

6. LEAKAGE CURRENT MONITORING

One indication that an MSGC strip is about to break down is a continuous increase in the leakage current of that strip. To avoid a discharge, the power to the faulty strip must be switched off, however, it is not practicable to address each channel individually.

The MSGCs have therefore been arranged into groups of 32 channels, where the power to any one group can be switched off. Within the chip the leakage current to each channel is mirrored out of the front-end by a factor of

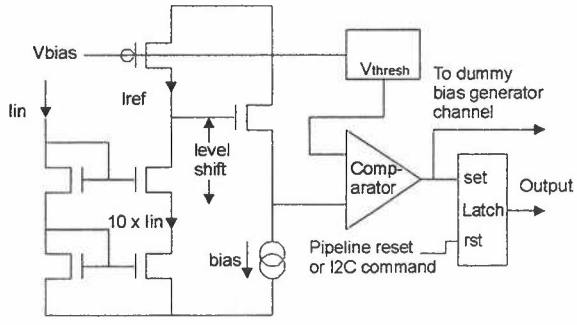

Figure 5 Current Monitoring Circuit

two, and then summed for groups of 32 channels (i.e. for channels 0-31, 32-63, 64-95, 96-127). These four

summed currents then form inputs to current comparators, where they are compared with a reference current (figure 5) which has been programmed using an on-chip register. A latch is set for each of the currents exceeding the reference value. The latched outputs then drive four open-drain output pads which are used to switch off the power to the group of 32 MSGC channels containing the faulty strip. The reference current is defined using one channel of the bias generator programmable over the I^2C interface with 8 bit resolution. The bias generator channel provides a maximum of 127.5uA output current which is mirrored down by a factor of 0.4 to give 51uA. The summed currents are multiplied by a factor of 10 giving a total multiplication factor - from the initial leakage current value - of 20. The leakage monitor range is therefore from 0-2550 nA in steps of 10 nA.

A second channel of the bias generator is used to define a bias current for the monitor circuit electronics and a third channel is used to store information concerning the states of the 4 comparators and latches, which are then accessible over the I^2C interface.

Once any of the latches has been set, it can only be reset by resetting the whole chip, or by using an I^2C command to the bias generator channel.

7. PRELIMINARY TEST RESULTS

Preliminary tests have been carried out at Imperial College. However, the leakage current compensation and monitoring circuits have not yet been fully tested so no results are available for these at present.

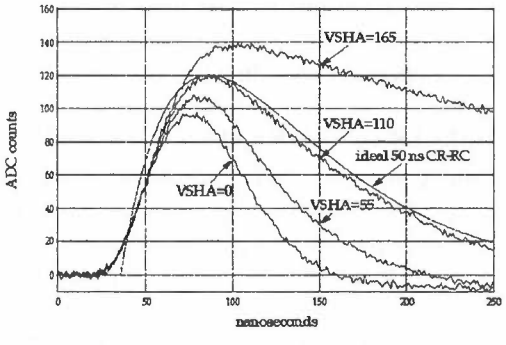

Figure 6 Pulse Shape Adjustment

The pulse shape can be observed at the output of the chip following analogue processing (figure 6). The case when VSHA=110 provides the optimum performance when the signal is closest to the ideal CR-RC shape. For this case the signal is 70μA for a 1MIP input. Adjusting VSHA above and below this value lengthens or shortens the peaking time.

Figure 7 shows the pulse shapes obtained in both peak mode and deconvolution mode. This shows that the deconvolution algorithm is functioning correctly and that the gain in either modes is almost the same.

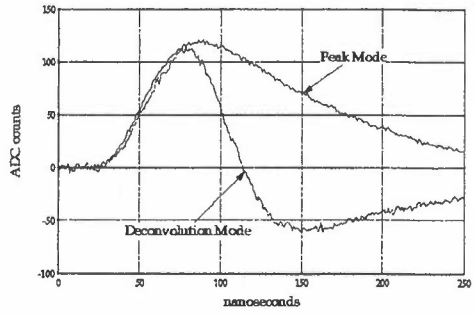

Figure 7 Pulse Shape for Peak and Deconvolution

Figure 8 shows the noise performance in peak mode and in deconvolution mode for varying sizes of input capacitance. The peak mode noise is similar to that in APV6 (510+36/pF) [1], but with a slightly steeper slope. In deconvolution mode however, the intercept is a lot lower than APV6 (1000+46/pF) but the slope is steeper.

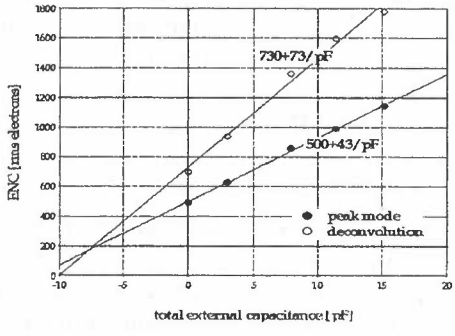

Figure 8 Noise Performance of Analogue Chain

8. CONCLUSIONS

A CMOS mixed signal analogue pipeline has been designed and manufactured. Based on the APV6 it has been optimised for read-out of CMS MSGC detectors, and preliminary test results show the circuit to be working. The next version of the chip will be designed on a 0.25μm process which can be made radiation hard by careful circuit design techniques.

9. ACKNOWLEDGEMENTS

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9. REFERENCES

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[2] Definition of Signal Processing Algorithm for CMS MSGCs, F.G.Sciacca, CMS internal note, May 1997.