Total Ionising Dose effects in the FE-I4 front-end chip of the ATLAS Pixel IBL detector

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ABSTRACT: The ATLAS Pixel Insertable B-Layer (IBL) detector was installed into the ATLAS experiment in 2014 and has been in operation since 2015. During the first year of data taking, an increase of the low-voltage current of the FE-I4 chip was measured. This increase was traced back to radiation damage in the chip. The dependence of the current from the Total Ionising Dose (TID) and temperature has been tested with X-ray irradiations. This paper presents the measurement results and gives a parameterisation of the leakage current and detector operation guidelines.

KEYWORDS: Interaction of radiation with matter; Ionization and excitation processes; Particle tracking detectors; Radiation-hard detectors

Contents

1   The Insertable B-Layer

The ATLAS Insertable B-Layer (IBL) is the innermost layer of the ATLAS pixel detector [1], and was one of the major upgrades to the ATLAS experiment made during the long shutdown of LHC in 2013–2014. It consists of a single cylindrical layer with a radius of 33 mm, covering $|\eta| < 3.0$ of pseudo-rapidity with 14 staves surrounding the new beryllium beam pipe. Each stave is tilted by 14 degrees with respect to the normal incident angle, and is equipped with 32 front-end chips (FE-I4) bonded to 200 μm thick silicon sensors [2]. The FE-I4 is designed in 130 nm CMOS IBM technology, holds around 80 million linear transistors and has a pixel size of $50 \times 250\ \mu m^2$, organised in a matrix of 336×80 pixels. Each individual pixel keeps track of the time-over-threshold (ToT) in counts of an external supplied clock of 40 MHz. The FE-I4 is fed by a common power supply referred to as low-voltage (LV) [3].

2   Observations during operation

After the first months of IBL data-taking in 2015, a significant increase of the LV current and a shift of the calibration parameters Threshold and ToT were measured. The LV currents are read out for a module group of four front-end chips. The low voltage current for one group and the calibration shift are shown in figures 1 and 2. To cope with the calibration parameters shift, the detector was re-tuned regularly in between fills to stay close to the target values. To protect the detector from damage due to the increasing currents, modules were switched off in case they reached the safety limit of 2.8 A. The complete IBL detector was switched off during one LHC fill due to safety concerns regarding the voltage transients on the supplying services.

From previous publications about the leakage current as a function of the total ionising dose (TID) in NMOS transistors [4, 5], it can be concluded that the LV current increase and the shift of tuning parameters are the result of the leakage current increase inside the NMOS transistors of the front-end chip. Ionising radiation generates electron-hole pairs. In SiO_2 holes have relatively low mobility and some of them are trapped in deep trapping centres, where they can remain for a long time. The accumulation of trapped positive charges in the shallow trench isolation (STI) gradually builds an electric field at the edges of the transistors, and this electric field will eventually induce
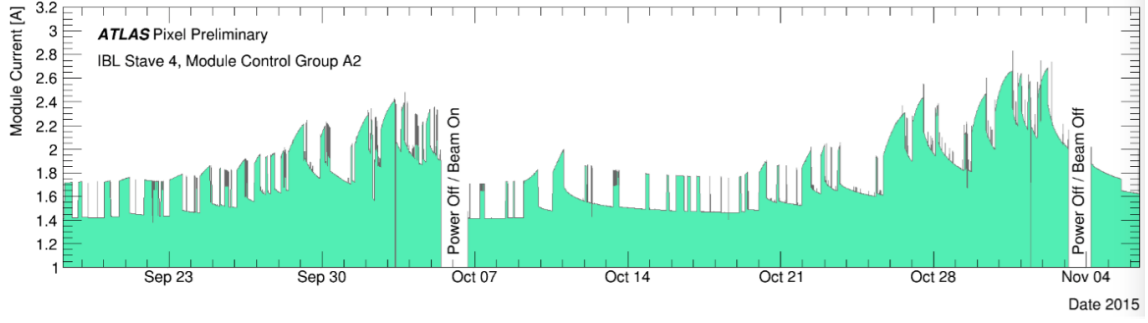
Figure 1. An example of the low-voltage current drift of IBL modules from the middle of September until the beginning of November 2015. The module control group of Stave 4, A2 (4 front-ends) is shown for illustration. There are two levels of the current depending on the configuration of the front-end modules: STANDBY (lower level, not for data taking) and READY (higher level, for data taking). There are two long power-off periods on October 5–6 and November 3–4, plus a short power-off on October 3 and November 1 [6].
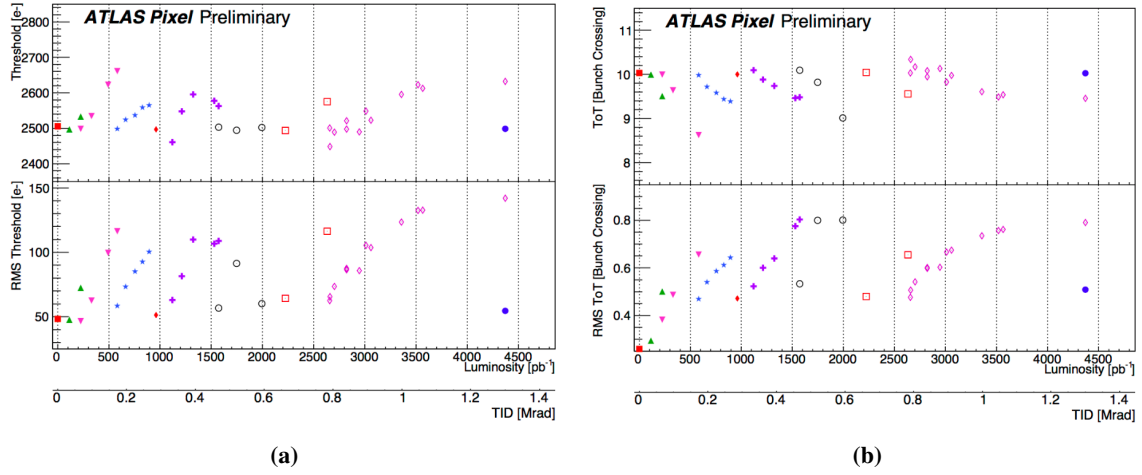

Figure 2. The evolution of the mean and RMS of the measured threshold (a) and ToT (b) over all pixels in the IBL detector as a function of the integrated luminosity and the corresponding total ionising dose (TID) in 2015, as measured in calibration scans. The threshold was tuned to 2500 electrons and the tuning point for the ToT was 10 BC for 16k electrons. Radiation effects caused the measured threshold to drift upwards and the ToT downwards with integrated luminosity. Each colour/symbol series corresponds to a single tuning of the detector.

inversion of the p-doped body of n-channel transistors. This translates in a radiation-induced leakage current channel. However, ionising radiation in the SiO_2 of the STI also leads to the activation of trapping centres at the Si-SiO_2 interface. In NMOS transistors these centres trap electrons. This negative charge can compensate for a part of the positive charge trapped in the bulk of the oxide. The area of the interface traps is located in the yellow marked region in figure 3. Laboratory measurements were set up to investigate the behaviour of the NMOS transistors of the front-end chip and a model was developed to quantify the current trend [8]. The model will be described in section 4.
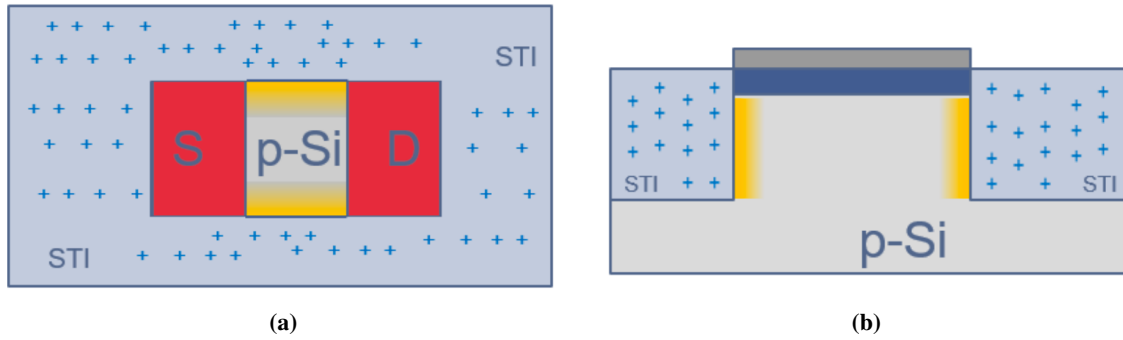
Figure 3. Cross section of an NMOS transistor in top (a) and side view (b). The channel of the parasitic transistor along the STI is indicated in yellow [8].

3 Laboratory measurement results

To quantify the dependency of the current increase on dose rate and temperature, several irradiation and electrical tests were performed. Since the temperature is the only parameter that can be controlled in the operation of the IBL, the main goal was to find a safe operation temperature that would not induce a current increase near the safety limit. For all measurements presented in this paper, two different setups have been used. The first set of measurements has been carried out using a Seifert RP149 X-ray tube [9]. This X-ray tube is equipped with a tungsten target with a peak energy of 10 keV, sealed by a beryllium window of 0.25 mm thickness. In addition, an aluminium filter of 0.15 mm is used to ensure a uniform dose rate in the front end chip. The distance between the tube and the chip was set to 36 cm to achieve a dose rate of 120 krad/h and to 20 cm for a rate of 420 krad/h. A sealed cooling box was designed to ensure a stable temperature during the measurements. The front-end chip was powered using two Keithley 2410 devices.

A second set of measurements has been performed using an XRAD-iR-160 machine [10]. The machine has an adjustable shelf allowing a distance of source to shelf from 10 to 100 cm. The maximum applicable voltage is 160 kV and the maximum current 45 mA. For a dose rate of 120 krad/h the settings were 30 kV and 30 mA at a source to chip distance of 29.4 cm and for 10 krad/h the settings were 30 kV and 10 mA at a distance of 50 cm. An aluminium filter of 0.15 mm thickness is used in addition to a 0.8 mm beryllium window.

A first set of measurements was performed at a fixed dose rate of 120 krad/h for different temperatures to investigate the dependency of the current trend on temperature. The result is shown in figure 4. The increase in the current trend can be explained by the quick trapping of positive charges in the STI oxide, opening a current path which results in an increased LV leakage current. The accumulation of interface traps along the STI partially compensates for the positive space charge in the thin silicon dioxide and therefore increases the channel resistance. As this is a slow process [11] it leads to a delayed decrease of the LV current. In figure 4 we show that a higher temperature results in a lower LV current increase, which we attribute to the faster formation of STI interface traps. Compared to the expected LHC dose rate during collisions of 10 krad/h, the dose rate of 120 krad/h was too high to give realistic results for the expected current increase. Therefore a second set of measurements was performed at 10 krad/h and +5°C as well as 0°C. It is found that an operation temperature of +5°C results in a current increase of about 250 mA, as shown in figure 5.

This would multiply to a current increase of 1 A for one IBL module group, not exceeding the limits for safe operation. It was therefore decided to change the IBL operation temperature to +5°C.

In addition, the shift of the calibration parameters was investigated. The result of the measurement at 0°C is shown in figure 6. The measured parameters follow the same trend as it was seen for the IBL front-end chips and show continuous shifting. Due to this result a frequent retuning of the detector even after longer radiation exposure is recommended. All results of the irradiation measurements have been published on the ATLAS Public Results webpage, see ref. [12].
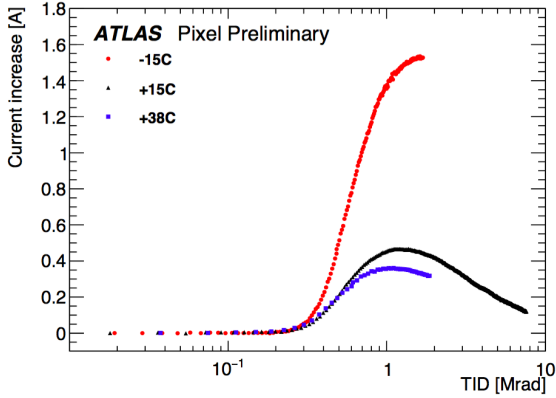
Figure 4. LV current increase of three single front-end chips in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale. Laboratory measurements carried out at 38°C (in blue dots), at 15°C (in black triangles) and at −15°C (in red squares) with a dose rate of 120 krad/h. The LV current of a single front-end chip before irradiation was 400 mA (at 38°C), 360 mA (at 15°C) and 380 mA (at −15°C) [12].
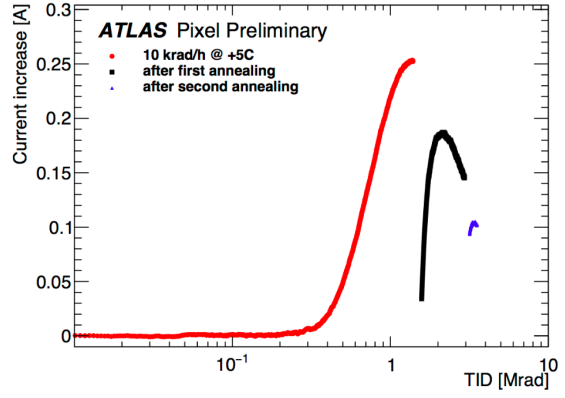
Figure 5. LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale during two consecutive irradiation campaigns. The temperature of the chip was kept at +5°C and the dose rate was 10 krad/h. Between the irradiation steps was a several hour annealing period, resulting in the observed recovery. The LV current of the front-end chip before irradiation was 376 mA [12].
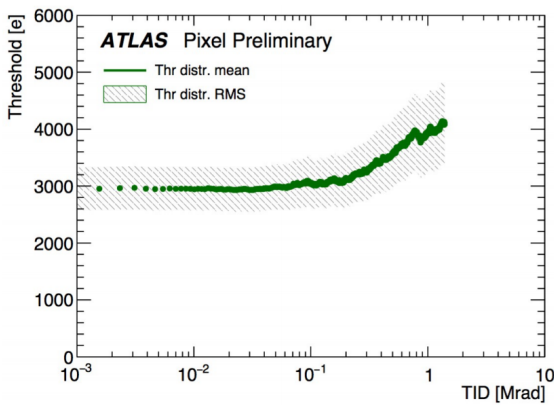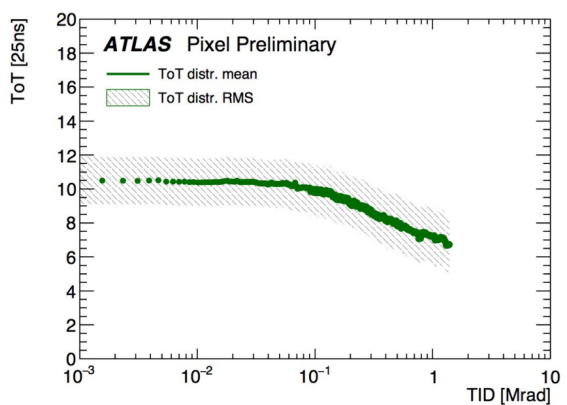
(a)　　　　　　　　　　　　(b)

Figure 6. Trend of the Threshold (a) and ToT (b) parameter shift of a single front-end chip in data taking condition as a function of the total ionising dose (TID). The temperature of the chip was 0°C and the dose rate was 10 krad/h [12].

4 Leakage current parametrisation

The behaviour of the LV current increase can be described using the transfer characteristics of a parasitic transistor, where the current is 0 as long as the gate voltage V_G is smaller than the threshold voltage V_{thr} [8]. In saturation mode, the drain current I_D can be described as a quadratic function with a constant factor K':

$$I_D \approx K' \cdot (V_G - V_{thr})^2 \tag{4.1}$$

The main change of the leakage current in NMOS transistors during irradiation is driven by the number of oxide charges accumulated in the STI and by interface traps activated at the Si-SiO$_2$ interface along the STI. For p-type silicon the STI oxide charges form a conduction channel between source and drain which increases the leakage current. Contrary to that, the interface traps lead to a decrease of leakage current due to the accumulation of fixed negative charges which compensate the positive charges. The gate voltage of parasitic transistors depends on the effective number of charges $N_{eff} = N_{ox} - N_{if}$ and the threshold voltage by the threshold number of charges N_{thr}. Based on this the leakage current can be described as:

$$I_{leak} = I_{leak}^0 + K \cdot (N_{eff} - N_{thr})^2, \tag{4.2}$$

with I_{leak}^0 describing the current consumption before irradiation and a proportionality constant K.

The number of positive charges N_{ox} defines the strength of the electrical field of the space charges in the STI and thereby the channel formation from source to drain. This number increases linearly with TID and decreases exponentially with time due to thermally-activated release of the trapped charges. The trend can be described using:

$$N_{ox}(t) = k_{ox} D \cdot \tau_{ox} \cdot \left(1 - e^{-\frac{t}{\tau_{ox}}}\right), \tag{4.3}$$

with k_{ox} being the number of trapped holes per dose unit, D the dose rate and τ_{ox} the lifetime of oxide charges.

The negative charges get activated by the accumulated positive charges at the interface along the STI. The number of interface traps N_{if} is technology dependent and limited. Due to this, the number of available trapping centres decreases with time and the probability that holes activate new interface traps decreases exponentially. This can be described with:

$$N_{if}(t) = k_{if} D \cdot \tau_{if} \left(1 - e^{-\frac{t}{\tau_{if}}}\right) \tag{4.4}$$

For the resulting leakage current of the front-end chip one has to sum up the current consumption before irradiation and the current increase:

$$I_{leak} = I_{leak}^0 + K \cdot \left[k_{ox} D \cdot \tau_{ox} \cdot \left(1 - e^{-\frac{t}{\tau_{ox}}}\right) - k_{if} D \cdot \tau_{if} \cdot \left(1 - e^{-\frac{t}{\tau_{if}}}\right) - N_{thr}\right]^2 \tag{4.5}$$

This formula was used to predict the maximum current increase in several consecutive measurements. It is assumed that a fit to the first peak of the current results in a maximal value for all following irradiation steps, since the positive charges anneal during the time with beam off while the interface traps stay in place. The result of the fit to data taken at a dose rate of 120 krad/h at 38°C is shown in figure 7. Future measurements will aim for the determination of the parameters k_{if}, k_{ox}, τ_{if} and τ_{ox}. A more detailed derivation of formulas (4.1) to (4.5) can be found in ref. [8].
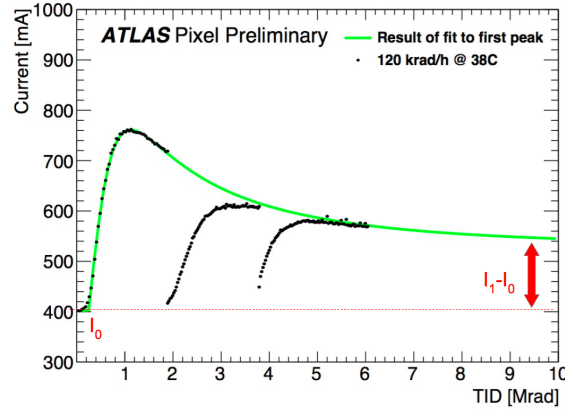
Figure 7. LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose. I_0 shows the current consumption before irradiation and I_1 the current value after the current trend reaches the plateau [12].

5 Summary

During the second half of the year of 2015, an increase of the LV currents of the IBL modules was observed. This observation was of serious concern for the operation of the detector in 2016 due to the expected increased peak luminosity. To ensure the safe operation of the IBL detector, a task force has been installed to investigate the dependence of the current on the TID and temperature. The measurements confirm the hypothesis that the driving factor of the current increase is the radiation induced NMOS transistor leakage current. A measurement was performed at the expected maximum dose rate the LHC would deliver in 2016 and it was found that safe operation of the IBL would be possible at a temperature of $+5°C$. By mid 2016 the front-end chips of IBL accumulated around 9 Mrad and no further increase of the current is expected.

Acknowledgments

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