THÈSE

Pour obtenir le grade de

DOCTEUR de l'UNIVERSITÉ GRENOBLE ALPES
et de l'UNIVERSITE DE SHERBROOKE

École doctorale : Electronique, Electrotechnique, Automatique et Traitement du Signal
Spécialité : Nanoélectronique et Nanotechnologies
Unité de recherche : Laboratoire TIMA

Approche industrielle aux boîtes quantiques dans des dispositifs de silicium sur isolant complètement déplété pour applications en information quantique

Industrial approach to quantum dots in fully-depleted silicon-on-insulator devices for quantum information applications

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Thèse soutenue publiquement le **14 décembre 2022**, devant le jury composé de :

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I am among those who think that science has great beauty.
A scientist in his laboratory is not only a technician;
he is also a child placed before natural phenomena
which impress him like a fairy tale.

Marie Curie

Never half-ass two things.
Whole-ass one thing.

Ron Swanson

Résumé

La mise en œuvre des qubits de spin électronique à base de boîtes quantiques réalisés en utilisant une technologie avancée de métal-oxyde-semiconducteur complémentaire (en anglais: CMOS ou *Complementary Metal-Oxide-Semiconductor*) fonctionnant à des températures cryogéniques permet d'envisager la fabrication industrielle reproductible et à haut rendement de systèmes de qubits de spin à grande échelle. Le développement d'une architecture de boîtes quantiques à base de silicium fabriquées en utilisant exclusivement des techniques de fabrication industrielle CMOS constitue une étape majeure dans cette direction. Dans cette thèse, le potentiel de la technologie UTBB (en anglais: *Ultra-Thin Body and Buried oxide*) silicium sur isolant complétement déplété (en anglais: FD-SOI ou *Fully Depleted Silicon-On-Insulator*) 28 nm de STMicroelectronics (Crolles, France) a été étudié pour la mise en œuvre de boîtes quantiques bien définies, capables de réaliser des systèmes de qubit de spin. Dans ce contexte, des mesures d'effet Hall ont été réalisées sur des microstructures FD-SOI à 4.2 K afin de déterminer la qualité du nœud technologique pour les applications de boîtes quantiques. De plus, un flot du processus d'intégration, optimisé pour la mise en œuvre de dispositifs quantiques utilisant exclusivement des méthodes de fonderie de silicium pour la production de masse est présenté, en se concentrant sur la réduction des risques de fabrication et des délais d'exécution globaux. Enfin, deux géométries différentes de dispositifs à boîtes quantiques FD-SOI de 28 nm ont été conçues et leurs performances ont été étudiées à 1.4 K. Dans le cadre d'une collaboration entre Nanoacademic Technologies, Institut quantique et STMicroelectronics, un modèle QTCAD (en anglais: *Quantum Technology Computer-Aided Design*) en 3D a été développé pour la modélisation de dispositifs à boîtes quantiques FD-SOI. Ainsi, en complément de la caractérisation expérimentale des structures de test via des mesures de transport et de spectroscopie de blocage de Coulomb, leur performance est modélisée et analysée à l'aide du logiciel QTCAD. Les résultats présentés ici démontrent les avantages de la technologie FD-SOI par rapport à d'autres approches pour les applications de calcul quantique, ainsi que les limites identifiées du nœud 28 nm dans ce contexte. Ce travail ouvre la voie à la mise en œuvre des nouvelles générations de dispositifs à boîtes quantiques FD-SOI basées sur des nœuds technologiques inférieurs.

Abstract

Electron spin qubits based on quantum dots implemented using advanced Complementary Metal-Oxide-Semiconductor (CMOS) technology functional at cryogenic temperatures promise to enable reproducible high-yield industrial manufacturing of large-scale spin qubit systems. A milestone in this direction is to develop a silicon-based quantum dot structure fabricated using exclusively CMOS industrial manufacturing techniques. In this thesis, the potential of the industry-standard process 28 nm Ultra-Thin Body and Buried oxide (UTBB) Fully Depleted Silicon-On-Insulator (FD-SOI) technology of STMicroelectronics (Crolles, France) was investigated for the implementation of well-defined quantum dots capable to realize spin qubit systems. In this context, Hall effect measurements were performed on FD-SOI microstructures at 4.2 K to determine the quality of the technology node for quantum dot applications. Moreover, an optimized integration process flow for the implementation of quantum devices, using exclusively mass-production silicon-foundry methods is presented, focusing on reducing manufacturing risks and overall turnaround times. Finally, two different geometries of 28 nm FD-SOI quantum dot devices were conceived, and their performance was studied at 1.4 K. In the framework of a collaboration between Nanoacademic Technologies, Institut quantique, and STMicroelectronics, a 3D Quantum Technology Computer-Aided Design (QTCAD) model was developed for FD-SOI quantum dot device modeling. Therefore, along with the experimental characterization of the test structures via transport and Coulomb blockade spectroscopy measurements, their performance is modeled and analyzed using the QTCAD software. The results reported here demonstrate the advantages of the FD-SOI technology over other approaches for quantum computing applications, as well as the identified limitations of the 28 nm node in this context. This work paves the way for the implementation of the next generations of FD-SOI quantum dot devices based on lower technology nodes.

Acknowledgements

First of all, I would like to express my deepest gratitude to my PhD supervisor and co-supervisors, Dr. Philippe Galy, Prof. Michel Pioro-Ladriere, and Prof. Salvador Mir, as well as to my PhD advisor Dr. Manuel J. Barragan, for their guidance, support, trust, and encouragement throughout the entirety of my PhD journey. Their unwavering belief in my abilities and constant push to excel has been invaluable. I am deeply grateful for the opportunity I have had to work with such experts from diverse domains. All the opportunities they offered me helped me not only to develop my skills and expertise in such a broad field but also to grow as a person. Thank you Philippe for being so supportive and always available to talk and help me, even during my 2.5 years in Canada. Thank you for being so kind and asking me at each one of our weekly meetings about my health and my family's health throughout the years of the pandemic and lockdowns. Thank you Salvador for all the fruitful conversations and thorough comments emphasizing on the details that allowed me to develop my scientific way of thinking. Thank you also for your valuable help and comments with re-reading in detail the entire manuscript of my thesis when I completed it. Thank you Manuel for your guidance and the analytical and pedagogical way you answered all my questions about engineering and microelectronics at the beginning of my PhD. I also greatly appreciate our discussions and your advice on career options. Thank you Michel, for your generosity, optimism and constant motivation. Thank you also from the bottom of my heart for working with me in the lab intensively almost every day with me when my ESD-damaged devices almost drove me crazy, or for finding the time to simply have a coffee and a chat when I was very affected by the challenges of this project. I will stand on this last point to thank you for being so caring and for reminding me all along our work together that success in the longterm does not come by numerous burnouts but by not neglecting our personal life. This realization was a major shift for me and is the one of the main reasons that makes me want to continue research and for that I am deeply grateful to you.

I would like to express my immense gratitude to Thomas Bédécarrats for helping me to understand so many new concepts in electrical engineering at the beginning of my PhD and especially for his priceless support during my first tape-out in STMicroelectronics. I would also like to express my sincere gratitude to Ryan H. Foote for all his tremendous help and invaluable support during almost all the time that I spent in Institut quantique, which allowed me to overcome some of the most difficult challenges. Your broad knowledge is so impressive and you are so enthusiastic that it is really inspiring to work and discuss science with you. I have learnt so much and you have helped me to improve in so many areas, such as how to design and conduct my experiments, my writing and presentation

skills, just to name a few.

At this point, I would like to express my gratefulness to the members of my thesis committee, Prof. Philippe Dollfus, Prof. Andrew Dzurak, Prof. Patrick Fournier, Prof. Skandar Basrour and Dr. Louis Huttin for taking the time to review my manuscript and for their insightful feedback and kind words about my work.

I would also like to thank my PhD follow-up committees, Prof. Skandar Basrour (again) and Prof. Sylvain Bourdel from Université Grenoble Alpes, and Prof. René Côté and Prof. Louis Taillefer from Université de Sherbrooke, for their guidance and valuable feedback on my work which allowed me to evolve, as well as to overcome certain obstacles.

I would like to express my warmest thank you to all the people who participated in this research project and contributed to the data presented in this thesis. I would like to especially express my sincere gratitude to Dr. Felix Beaudoin and Dr. Pericles Philippopoulos from Nanoacademic Technologies for their collaboration on the QTCAD device simulations. I am deeply grateful for all the valuable advice and fruitful conversations that allowed me to understand my data, your quick response to my questions, and the trainings on QTCAD either remotely or in person. The experience of working with such excellent professionals like yourselves has taught me so much. Finally, I specifically would like to thank Dr. Pericles Philippopoulos for performing the QTCAD simulations on the second generation of the quantum dot device by himself while I was busy writing my thesis, thus helping to complete this particular study.

I would also like to express my gratitude to all my colleagues for all the support they provided me with during these four years. I would like to thank my colleagues from STMicroelectronics and more specifically, Philippe Cathelin for all the scientific conversations, Gaëlle Masseboeuf for the training in C2M software, Clément Charbuillet for the IT support, Christian Gardin for the numerous discussions on OFDEC simulations and for validating my design for fabrication despite the design rules violations, Franck Arnaud for his support on my layout and MPW fabrication, Alexis Poulin and Kevin Tournon for their support in sample packaging, and Nicolas Guitar for the training in TCAD Process software. In addition, I would like to thank Mamadou Diallo from TIMA for his support in my first layout design. Finally, I would like to thank Prof. Dominique Drouin from Université de Sherbrooke for his support throughout this thesis, Dany Lachance-Quirion for all the valuable lessons I learned from him, even though we did not work together for a long time, Michael Lacerte for all technical support and various trainings in the laboratory, Christian Lupien for his support during my measurements and all productive discussions that allowed me to overcome so many challenges, and Bobby Rivard and Stéphane Pelletier for the excellent organisation and the on-time delivery of the liquid helium I needed daily.

I would also like to express my warmest thank you to all the people that brightened up my working days, with who I shared lunch and coffee breaks, in France or in Canada, and some of whom became dear friends. In particular, I would like to thank, from STMicroelectronics and TIMA, Joao Henrique Quintino Palhares, Giovani Crasby Britton Orozco, Louise De Conti, Mohammed Tmimi, Renan Lethiecq, Valérian Cincon, Geoffrey Delahaye, Tarun Chawla, Thomas Capelli, Guillaume Tochou, Franck Sabatier, Dayana

Pino Monroy, Raphael Guillaume, Florian Voineau, David Gaidioz, Romane Dumont, Imadeddine Bendjeddou, Sana Ibrahim, Ankush Mamgain, Ayoub Naoui and Mohamed Khalil Bouchoucha. I would also like to thank, from Institut quantique, Marc-Antoine Roux, Sara Turcotte, Zhiren Wang, Sophie Rochette, Julien Camirand-Lemyre, Mathieu Moras, Pierre Lefloïc, Amélie Lacroix, Joffrey Rivard, Claude Rohrbacher, Martin Schnee, Samuel Desrosiers, Jessica Lemieux, Laurine Marian, Maxime Tremblay, Jean-Olivier Simoneau, Alexandre Rousseau, Marie-Eve Boulanger, Clément Godfrin, Benjamin Bureau, Pierre-Olivier Downey, Clément Girod, Chloé-Aminata Gauvin-Ndiaye, Agustin Di Paolo, Maxime Lapointe Major, Camille le Calonnec, Vishnu Narayanan, Charles Paradis, Maxime Plourde and Nouédyn Baspin.

I am so grateful for all the support and encouragement of my family. Without all your love and support I would not have made it. Mom, thank you for making the impossible possible and for teaching me to be strong. Dad, when I started this project, I was reading scientific papers next to your bed in the hospital. I am so happy that you are still with us today. Thank your being there for me in the way that you can. I also thank from the bottom of my heart my brothers and sister I never had, my cousins. Harry, Poppy and Menios, you helped me go through some of the hardest times.

I am also profoundly thankful for all the amazing and unforgettable people from Greece, France, and Canada, whose presence has made my life more beautiful during these four years. Eva, Konstantina and Alkistis, you are a constant source of inspiration for me, in your own personal way. Katerina, our conversations helped me put my thoughts in order and find peace of mind. Panos, your music always helps me to concentrate when I am working. Antonis, of all the exciting adventures we shared together, thank you most of all for making last summer in Athens so much more fun by being my writing partner while I was writing my thesis. Dorina and Nikolas, although we all live in different countries now, you are forever in my heart my family from Grenoble. Nikos, thank you for making me discover new places in the (any) city. Sebastien, Alexia, Jovian, Suzy, Romy and Martina, thank you for all the hikes, drinks, game nights, horse riding in the mountains, last year's COVID-themed international Christmas dinner (yayyy), travelling and all the beautiful memories. Nefeli, Andreas, Sofia, thank you for the fun movie and pizza nights. Georges, thank you for this wonderful friendship and your brilliant idea to surprise me with an improvised lasagna/birthday cake for my birthday in the first week of the very first lockdown. Matthieu, thank you for your kindness and generosity. Loïc, thank you for reminding me that enjoying life should come naturally and easily. Thank you also, Jose, Michael, Mirenia, Nikolas, Irene, Chryssa, Hugo, Dimitris, Sofia, Giorgios, Theano, Christoforos, Christina, Romeo, Titiksha, Jorge, Wanda, Ulysses, Adela, Kimberly, Renato, Raphael, Camille, Quentin, Valentine, Jessica, Eloïse, Benoît, Pierre-Emmanuel, Antonio, Elyssa, Alessandro, Virginie, Noé, Viktoriia, Anthony, Giverny and Sophie, for all the wonderful moments we shared.

Lastly, I will end by thanking my life partner with whom I share the same curiosity and passion for constant learning and personal growth. Merci, mon Luca. Thank you for understanding me like no one else and for standing by my side in every one of my choices, even when it is not easy. Thank you for your unconditional support, from the very beginning of this journey till the very end, no matter what.

Contents

Abbreviations

IC	Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
ESR	Electron Spin Resonance
SET	Single Electron Transistor
FD-SOI	Fully Depleted Silicon-On-Insulator
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
UTBB	Ultra-Thin Body and Buried oxide
SOI	Silicon-On-Insulator
CMP	Chemical Mechanical Polishing
BOX	Buried OXide
LVT	Low Threshold Voltage
RVT	Regular Threshold Voltage
SG	Standard Gate oxide
EG	Extended Gate oxide
EOT	Equivalent Oxide Thickness
LDD	Lightly Doped Drain
STI	Shallow Trench Isolation
BEOL	Back-End-Of-Line
VIA	Vertical Interconnect Access
BG	Back Gate
S	Source
D	Drain
I/O	Input/Output
ESD	Electro-Static Discharge
FEOL	Front-End-Of-Line
LVS	Layout Versus Schematic
DRC	Design Rules Check
DRM	Design Rules Manual
GAGS	Gds Acceptance Gating Script
OFDEC	Optical Friendly DEsign Check
C2M	CAD-to-Mask
CAD	Computer-Aided Design
FEM	Finite Element Modeling
TCAD	Technology Computer-Aided Design
QTCAD	Quantum TCAD

MPW	Multi-Project Wafer
FOUP	Front Opening Unified Pod
TEM	Transmission Electron Microscopy
FLGA	Fine pitch Land Grid Array
PCB	Printed Circuit Board
SEM	Scanning Electron Microscope
2DEG	Two-dimensional electron gas
VTI	Variable Temperature Insert
SMU	Source-Measurement Unit
FIB	Focused Ion Beam
FGT	Front Gate Top
FGB	Front Gate Bottom
DOS	Density Of States
QD	Quantum Dot
RET	Resolution Enhancement Techniques
NA	Numerical Aperture
OPC	Optical Proximity Correction
STEM	Scanning Transmission Electron Microscope

Introduction 1

1.1 Limits of microelectronics

In 1965, Gordon Moore, co-founder of Intel, would publish one of the most famous papers ever written about the evolution of the microelectronics industry in the world. In this seminal paper [1], he predicted that the number of transistors in a dense Integrated Circuit (IC) would double every year, and in 1975, he revised his prediction to doubling every two years [2]. Moore's prediction evolved into Moore's law, describing an exponential growth in computing power (Figure 1.1). Thereby, the improvements in processor speed revolutionized information technology and transformed governments, industry, societies and culture.

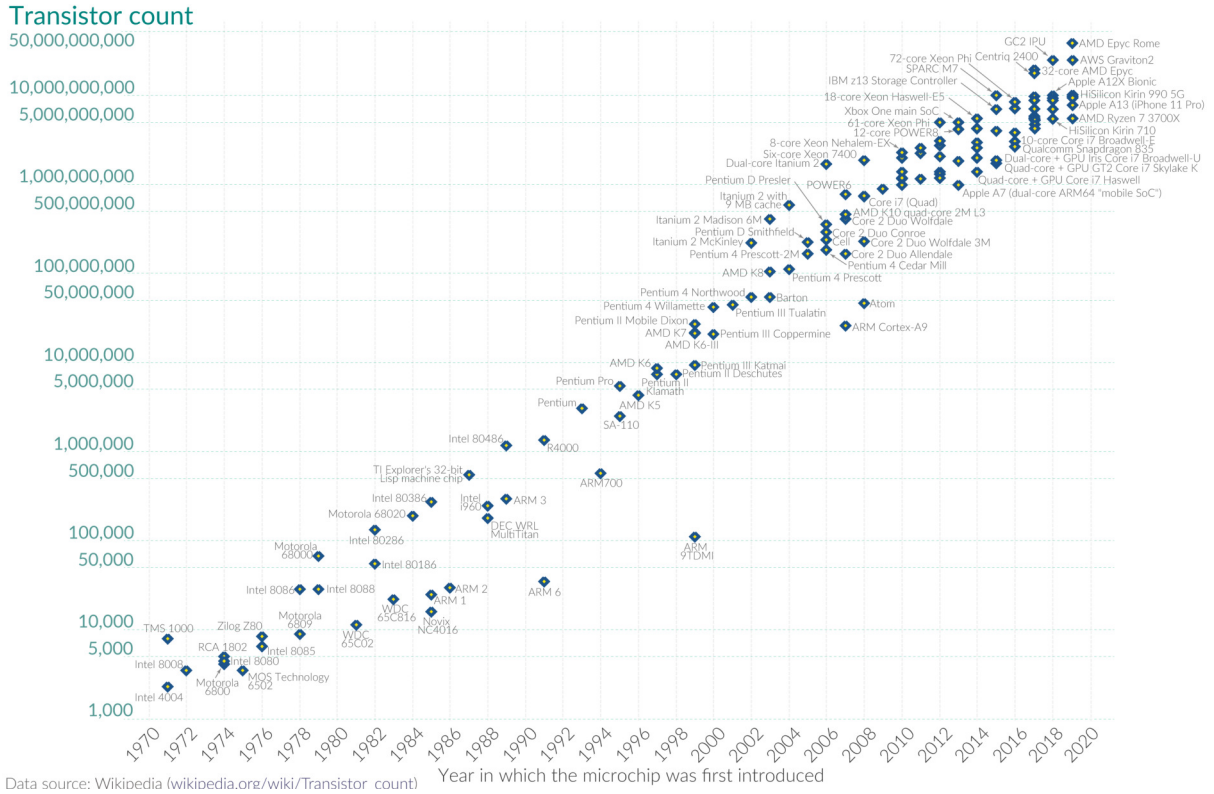

Figure 1.1 – Transistor density on integrated circuits versus calendar year. Image taken from ourworldindata website[1].

However, it is estimated that miniaturization of semiconductor technologies will face technical limitations as transistors approach the size of atoms. Based on Moore's statements from his publication, as long as the minimum device sizes are not limited by fundamental considerations as the electron charge or the atomic structure of matter, "there is no present reason to expect a change in the trend". Until now, technological innovations, driven by the needs of societies in today's generations, permitted to scale down foundry-fabricated transistor dimensions to only a few tens times the size of a silicon atom, i.e. 0.2 nm [3].

Intel, Samsung, and TSMC are currently the major world-leading companies in the semiconductor technology. Intel's 14 nm technology is currently used for mass production[2] and its 7 nm node is expected to be introduced by 2023. Since 2019, the 5 nm process tools of Samsung and TSMC are available to potential customers for 300 mm chip mass production. In addition, commercial chip volume manufacturing using 3 nm fabrication processes has started only very recently by Samsung[3] and TSMC[4], whereas both have promised to start production based on the 2 nm technology node by 2025.

With Complementary Metal-Oxide-Semiconductor (CMOS) technology scaling to smaller and smaller dimensions close to the size of a silicon atom, soon purely quantum effects, such as energy quantization or quantum tunneling, will therefore degrade the proper performance of the device and a decrease, or a plateau, in computational power might be noted soon.

1.2 Quantum computing era

Instead of considering quantum effects as an issue that needs to be tackled, the principles of quantum mechanics could be leveraged to process information. Indeed, quantum computing, based on Alan Turing's legacy, the Turing machine [4], first considered in Richard Feynman's paper published in 1982 [5] and then established by David Deutsch in 1985 [6], harnesses the properties of quantum mechanics and promises to revolutionize several scientific and technological fields. Today, small-scale quantum processors are being used to run quantum algorithms and demonstrate the potential of future large-scale systems [6, 7]. Compared to its classical counterpart, a quantum computer guarantees an exponential improvement in calculation times and promises to solve computation problems considered notoriously difficult even for today's most powerful supercomputers [8, 9].

The most known examples of these unsolvable problems include integer factorization, combinatorial optimization problems, and simulation of quantum systems. Shor's quantum algorithm [10] was introduced in 1994 as an answer to the first challenge, by presenting an efficient way to find the prime factors of an integer and made a big impact

[1] https://ourworldindata.org/technological-change

[2] https://www.intel.ca/content/www/ca/en/silicon-innovations/intel-14nm-technology.html

[3] https://semiconductor.samsung.com/newsroom/news/samsung-begins-chip-production-\using-3nm-process-technology-with-gaa-architecture/

[4] https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm

on present cryptography [11, 12]. Grover's quantum algorithm, developped in 1996, introduced a novel way to search through unstructured data [13], with broad applications in various fields, such as machine learning, artificial intelligence, software engineering or applied mathematics [14]. Last, several studies to date are focused on the development of quantum algorithms for analysing and predicting the properties of nature, with broad applications including drug discovery and design [15], novel methodologies for medicine development [16] or optimization of energy consumption [17].

The building block of a classical computer is a bit which can take two discrete values, either 0 or 1. In the proposal of a quantum computer, quantum information is encoded in the so-called quantum bit or qubit, which exploits the principles of quantum mechanics, such as states superposition or quantum entanglement, to perform quantum computation operations using quantum algorithms. The state of a single qubit is described by a two-dimensional quantum state vector $|\Psi\rangle$ which in the two-dimensional complex Hilbert space is writen as

$$|\Psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \tag{1.1}$$

where the complex numbers $|\alpha|^2$ and $|\beta|^2$ are the probabilities for the qubit to be in the $|0\rangle$ state or the $|1\rangle$ state, respectively, satisfying $|\alpha|^2 + |\beta|^2 = 1$.

By translating these coefficients to the two angles θ and ϕ, a single-qubit quantum state can be represented as a three-dimensional real-valued vector. This new representation can be visualized in Figure 1.2. In the framework of this so-called Bloch sphere [18], the state of a single qubit is described by $|\Psi\rangle = cos\frac{\theta}{2}\,|0\rangle + e^{i\phi}sin\frac{\theta}{2}\,|1\rangle$ and corresponds to a single point on the spherical surface.

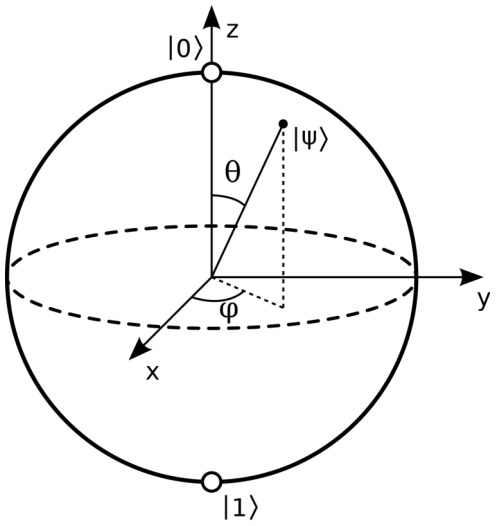

Figure 1.2 – The quantum state $|\Psi\rangle$ of a single qubit depicted on a Bloch sphere. Image taken from wikipedia website[5].

In 2000, David P. DiVincenzo proposed the main requirements for the physical implementation of the hardware needed by a quantum computer. These are known as the

[5]hrefhttp://en.wikipedia.org/wiki/

DiVincenzo's criteria [19], and are the following:

1. A scalable physical system with well characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state
3. Long relevant decoherence times, with respect to the gate operation time
4. A "universal" set of quantum gates
5. A qubit-specific measurement capability

1.3 Silicon spin qubits

Even though no full-fledged quantum computer has not been realized yet, several physical systems are currently explored for the realization of a quantum processor, such as superconducting circuits [20, 21], trapped ions [22, 23], optical lattices [24] and many more. Each approach focuses on fulfilling DiVincenzo's criteria and aims to provide a robust device able to process quantum information reliably. Among the most promising candidates, silicon spin qubits have attracted a wide interest [25].

The spin-based qubit architecture was first proposed in two seminal papers in 1998 in two different approaches [26, 27]. In a system based on the first approach, quantum information is encoded in the states of individual spins of electrons or holes confined in quantum dots hosted in semiconductor nanostructures [28]. In a system based on the second approach though, information is encoded in the states of individual spins of electrons or nuclei of dopant atoms introduced in the semiconductor devices [29, 30, 31, 32]. In such systems, there are two spin states in total, which are commonly referred to as 'spin up' and 'spin down'. Thus, such two-level systems are ideal for quantum information processing and the two states of a single qubit $|0\rangle$ and $|1\rangle$ are implemented by the spin orientation.

An example of a silicon spin qubit device is illustrated in Figure 1.3. The structure depicted here was fabricated on isotopically purified ^{28}Si and is presented in [33]. The design of the device has been simplified in the schematic shown here for illustration purposes. In this approach, the confinement is achieved by forming a quantum dot at the Si/SiO_2 interface via electrostatic gates patterned on the top side of the structure. Moreover, additional gate electrodes serve to control the tunnel barrier between the quantum dot and its nearby environment. More specifically, when the device is appropriately biased, a 2DEG is formed in the silicon channel and electrons tunnel through the potential barriers. Then, by controlling carefully the voltages applied to the gates, a single electron is trapped in the quantum dot and is exploited for the implementation of a single qubit.

In this particular example, the manipulation of the qubit state is achieved by Electron Spin Resonance (ESR) pulses generated by an external applied magnetic field. In this manner, due to the Zeeman effect, the energy levels of the confined electron are separated into the two spin states, which are used as the two qubit states. In general, this energy

splitting is at the range of a few and tens of gigahertz. Hence, by applying an oscillating magnetic field, via a co-integrated microwave antenna close to the qubit, with a frequency corresponding to this energy difference, quantum computation operations are performed on the qubit. In addition, a Single Electron Transistor (SET) device is used for charge sensing, and is integrated close to the quantum dot and capacitively coupled to it. The SET is a sensitive electronic device which is able to detect single electron changes in the dot occupancy.

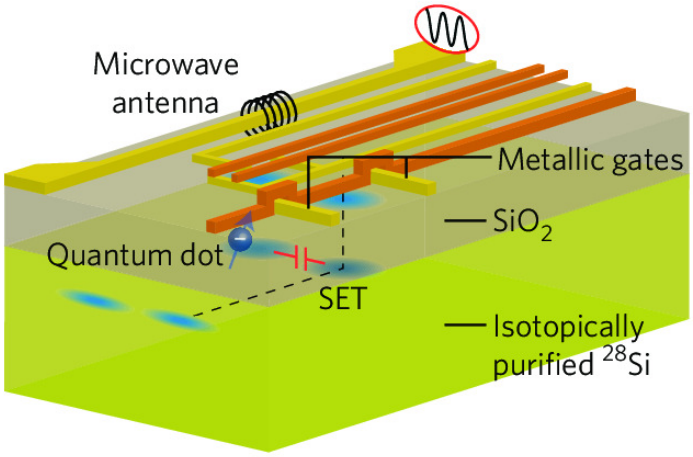

Figure 1.3 – Schematic representation of a silicon-based spin-qubit device fabricated on isotopically purified ^{28}Si presented in [33]. The gate patterns are simplified in the schematic for narrative purposes. A single electron is confined in a quantum dot, formed at the Si/SiO_2 interface and controlled by metal top-gates, depicted in yellow and orange, which are isolated between them. Readout of the charge state of the dot is performed by a top-gate SET. Electrons are manipulated by ESR pulses generated from a microwave antenna. Image adapted from [34].

Reference [35] is an excellent review to introduce spin-based qubits and their advantages comparing to other candidate technologies for quantum information processing. Indeed, silicon spin-based qubits rise to the top thanks to three main advantages: high operating temperatures, small footprint, and long coherence times. More specifically, most energy scales in both atomic and artificial systems are large enough to allow for operations at a few kelvin, which turns to be a high temperature for most solid-state qubits. Operation of a spin-based quantum processor at such temperatures would reduce significantly the complexity of the control and measurement system. In addition, strong carrier confinement is required so that the lowest orbital energy levels are well isolated from higher-energy electronic states, resulting in small dimensions for silicon qubit devices, compared to other alternatives, which makes them similar in size to the transistors composing today's classical computer chips, allowing to envision dense arrays of spin qubits. Last but not least, natural silicon can be isotopically purified to ^{28}Si eliminating nuclear spin, which causes decoherence to the electron spins, and resulting in significantly improved qubit coherence time [36, 37].

As presented in Figure 1.4, the state-of-the-art of the coherence of a single electron spin confined in a ^{28}Si structure attained tens of milliseconds [33]. Moreover, the highest

reported single-qubit fidelity in silicon is 99.96% [38]. The fidelity is a metric widely used to express the quality of the control obtained over the qubit state and is targeted to be higher than 99% in quantum computing systems. In order to achieve a universal gate set and satisfy one of DiVincenzo's criteria, the operation of two or more qubits together is necessary. Recently it has been demonstrated that two-qubit operation can be performed with a fidelity of $(99.65 \pm 0.15)\%$ [39, 40, 41]. Furthermore, the remarkable technological breakthrough of the experimental demonstration of a spin qubit device operating at 1.5 K reported a few years ago permits to envision device performance at much higher temperatures than other solid-state qubits that require a sub-kelvin environment [42].

Finally, the most striking feature of this technology is the ability that it offers to exploit the advanced mass-production processes from the field of microelectronics that have undergone a decades-long trajectory of development and standardization. In combination with the recent demonstration of a six-qubit quantum processor [43], the CMOS compatibility paves promising avenues not only for the accelerated improvement of single-qubit architectures, but also for scaling up to larger numbers of qubits [35, 44, 45, 46]. For more information on the key advantages of semiconductor spin qubits in general, the reader is referred to [47, 48, 49].

1.4 Scaling up challenges

The CMOS compatibility permits to envision the mass-production of spin qubit devices in silicon foundry facilities of modern computer industries [50, 51, 52]. Fabrication yield and qubit uniformity are expected to benefit from industrial efforts to manufacture quantum dot arrays using the well-matured processes and techniques from the microelectronics industry [53]. In the remainder of the section, the discussion is focused on gate-defined quantum dot qubits in CMOS structures, which is more relevant than other approaches to the work presented in this thesis.

CMOS quantum dot qubits

The first CMOS-based hole qubit device is presented in Figure 1.5 [54]. The structure was manufactured using non-standard process methods. Manipulation of the energy landscape in the device was realized through the manipulation of the electrostatic potential formed in the silicon substrate using gate electrodes.

Despite the aforementioned milestones that have been achieved with small-scale qubit structures in silicon, scalable qubit architectures that could enable future quantum computers still remain an issue. In fact, qubit-to-qubit interactions can only occur between the closest neighboring qubits and can currently occur in a range of a few tens of nanometres. The implementation of large-scale quantum computing systems requires qubit connectivity over much larger distances. To this end, linear and bilinear arrays of quantum dots are being explored [44, 45, 53, 55, 56], but no standard-process CMOS technology platforms exist today that could deliver such a 2D gate array design using exclusively industrial

methods.

Finally, in order to accelerate the evolution marked in qubit performance, device modeling leading to optimized fabrication processes and faster overall turnaround times is also necessary. To date, different empirical simulation tools exist which have only been used though for the interpretation of experimental data in order to analyze different qubit parameters [57, 58, 59].

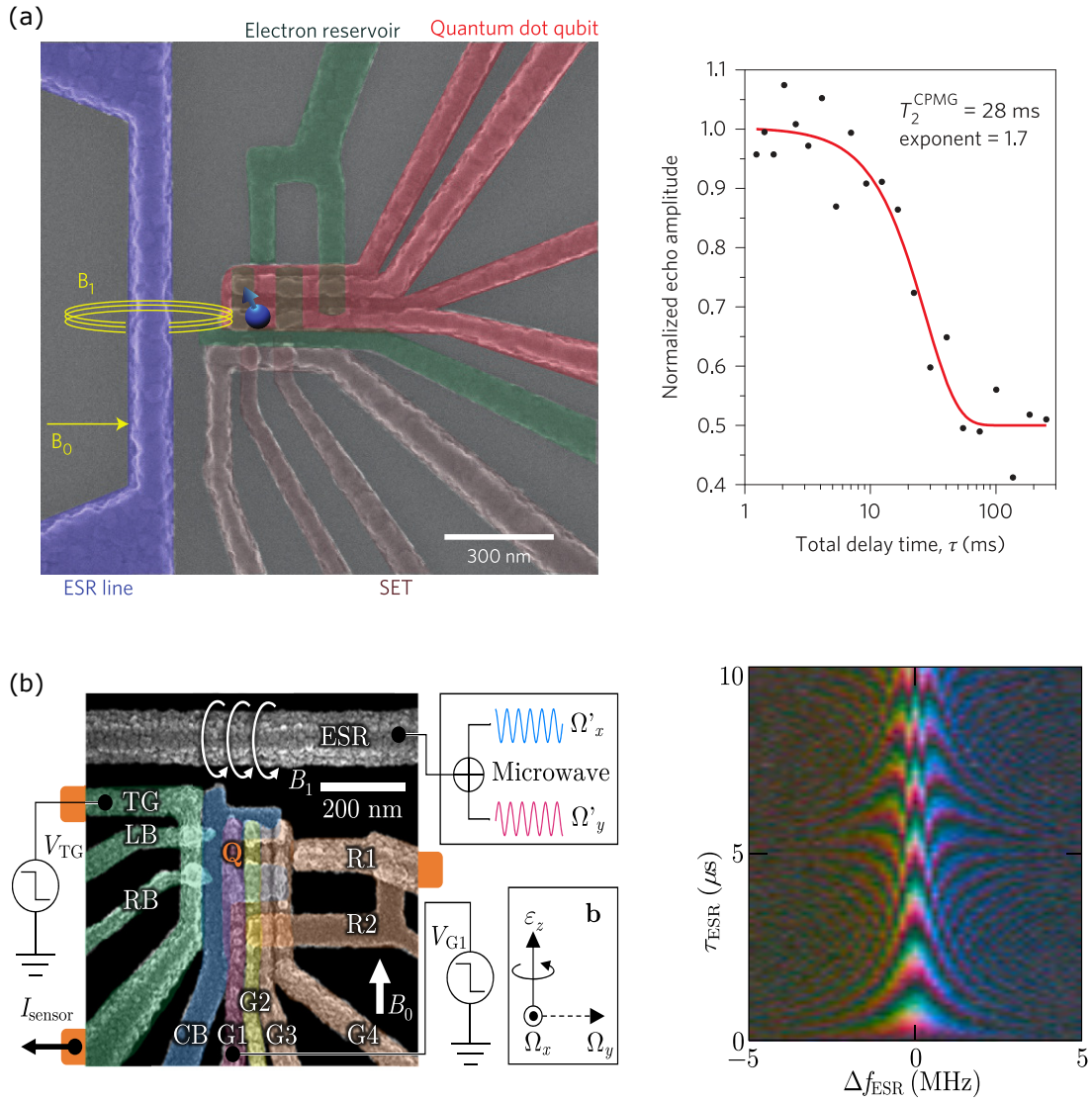

Figure 1.4 – (a) Coherence time of a single quantum dot qubit reaching tens of milliseconds. Image adapted from [33]. (b) Single-qubit control fidelity exceeding 99.96% in a quantum dot spin qubit architecture. Image adapted from [38].

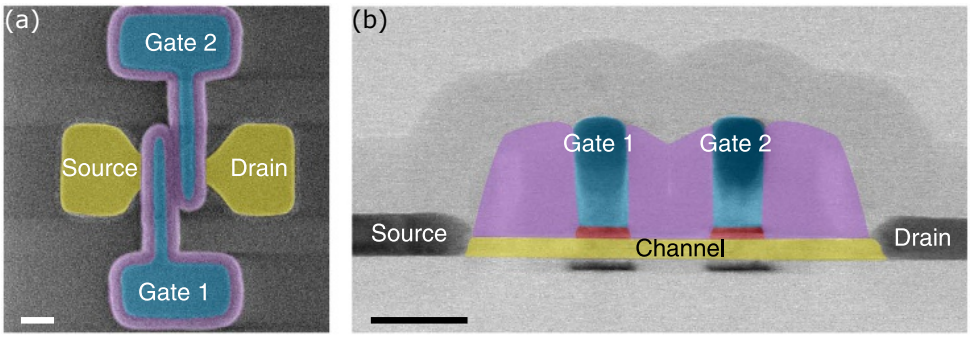

Figure 1.5 – (a) False-colored top-view and (b) cross-section of the first CMOS hole spin qubit device. Image taken from [54].

Co-integration with control electronics

In contrast to solid-state qubits which are in most cases operated at cryogenic temperatures approaching the absolute zero, conventional electronics used to initialize, manipulate and readout their state produce a lot of heat and thus need to be kept outside of the cryogenic system and far from the qubit. Moreover, a large-scale quantum computer will eventually need millions of qubits with massive yet very precise control electronics for the manipulation and readout of each qubit and this brute-force approach will no longer be practical. The heat and noise introduced by current room-temperature rack-mounted instruments and few metres long filtered and thermally anchored connecting cables will rapidly be a major issue.

Moreover, extremely high performance is required from the control electronics in terms of bandwidth, fast response times, and noise, in order to ensure accuracy and speed in the manipulation and readout of the qubits [60]. Solutions to this crucial engineering challenge and wiring bottleneck for the closer integration or, even better, on-chip co-integration of classical control and readout electronics with qubit systems have been explored [61, 62, 63, 64, 65]. In fact, the CMOS compatibility permits for closer, or even on-chip, co-integration of spin qubit platforms with the readout and control circuitry fabricated based on standard-process CMOS technology optimized for cryogenic-temperature operation, namely cryo-CMOS, leading to a more compact quantum processor [66, 67, 68, 69, 70]. In this way, a drastic reduction of the complex interconnections between the cryogenic system and the room-temperature measurement electronics can result in enhanced compactness and reliability.

1.5 Academic and industrial landscape

The global effort driving research and development in quantum sciences and technologies is continuously increasing with current investments reaching nearly USD 30 billion worldwide in 2022[6]. More specifically, Australia has invested AUD 130 million through

[6] https://qureca.com/overview-on-quantum-initiatives-worldwide-update-2022

federal funding in two centres of excellence conducting world-leading research in quantum information, i.e. the Australian Research Council Centre of Excellence for Engineered Quantum Systems and the Centre of Excellence for Quantum Computation and Communication Technology of the University of New South Wales [71]. The Netherlands has invested EUR 135 million in QuTech, the quantum technology institute of the TU Delft, and TNO (Netherlands Organisation for Applied Scientific Research)[7]. The UK has invested more than GBP 1 billion and has established a National Quantum Computing Centre[8] [72]. The European Commission allocated EUR 1 billion of funding to launch the European Quantum Flagship[9]. The French government recently launched an investment plan worth EUR 1.8 billion in quantum technologies[10]. The Canadian government has invested almost CAD 1.4 billion to date and has launched a National Quantum Strategy to accelerate innovation and commercialisation in quantum technologies [73]. The US government established the National Quantum Initiative Act with a USD 1.2 billion budget which will go to institutes such as the National Institute of Standards and Technology (NIST), in order to accelerate the growth of quantum technologies by collaborating with academic institutions and private industry [74].

A few more of these main research centres and institutions participating in the international effort towards a compact spin-based quantum processors are the University of Tokyo in Japan, Harvard University in the United States, and the MOS-Quito project, a European project focused on developing CMOS-based spin qubits which was completed a few years ago. This list is not exhaustive and contains only some of the main programs and efforts in the global ecosystem. Major contributions have also come from spin qubits research groups at CEA-Leti and CNRS in France, Princeton University, Quantum Information Science and Technology at Sandia National Laboratories in the US.

Moreover, several industry leaders in modern computer technology are now participating in the race for quantum supremacy[11]. For instance, IBM is currently exploring qubit systems based on silicon quantum dots, despite the fact that their approach to quantum computers is mainly focused on superconducting qubits [75]. Also, Hitachi Cambridge Laboratory and HRL Laboratories are focused on the study of silicon quantum dot qubits [76, 77]. Moreover, Intel is collaborating with QuTech and is not only focused on developing spin qubits, but also on their co-integration with control electronics (Figure 1.6(a)). Their work on the latter involved the implementation and characterization of a CMOS control electronics architecture operating at 3 K while being coupled to a 20 mK qubit [78, 79]. In fact, the first version of this compact cryo-CMOS control chip, illustrated in Figure 1.6 (b) and code-named Horse Ridge, was used for single-qubit readout with a fidelity of 97%.

[7] https://www.delta.tudelft.nl
[8] https://www.gov.uk/government/news
[9] https://qt.eu/about-quantum-flagship/introduction-to-the-quantum-flagship
[10] https://www.lemonde.fr/politique/article/2021/01/21
[11] https://physicsworld.com/a/silicon-spin-qubits-manufactured-on-an-industrial-scale

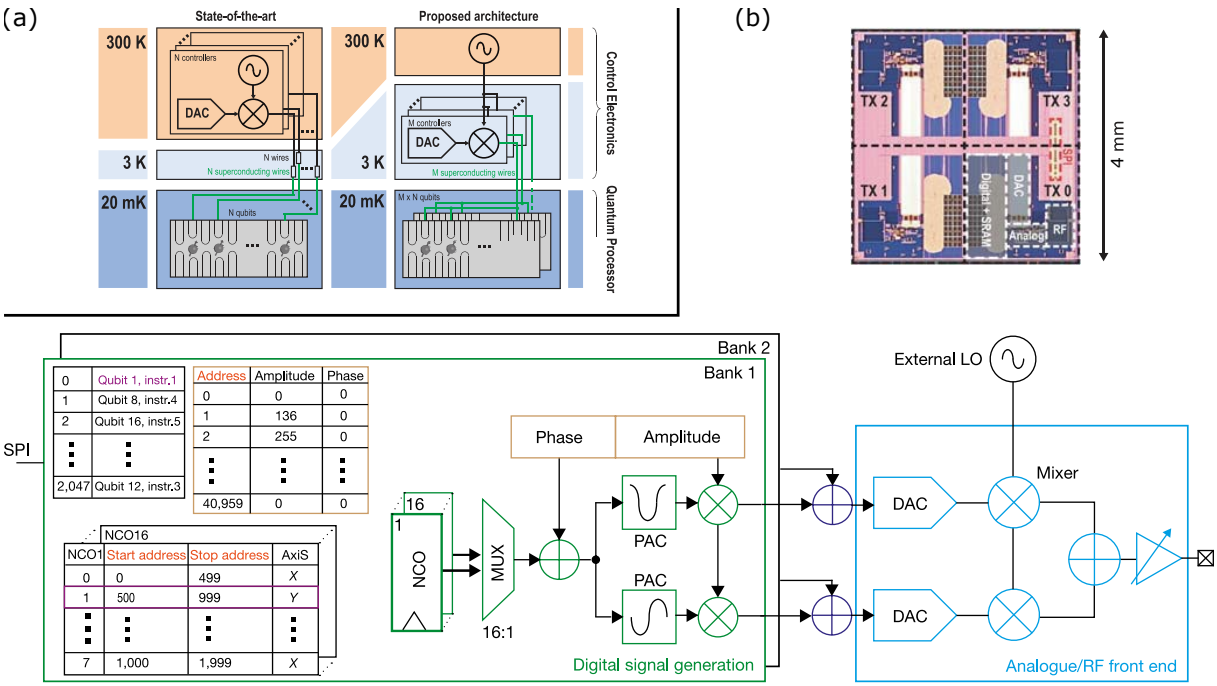

Figure 1.6 – (a) Scalable qubit controller exhibiting a wide frequency and output power range suitable for multiple qubit technologies proposed by [78]. Image taken from [78]. (b) Cryogenic CMOS control chip operating at 3 K, designed to manipulate and readout silicon quantum dot qubits at 20 mK. Image taken from [79].

In addition, Intel and QuTech recently achieved an important milestone by demonstrating the first spin qubit using all-optical lithography techniques [80]. The qubit device, presented in Figure 1.7, was fabricated on a 300 mm wafer that demonstrated a fabrication yield of up to 98%, with only two devices not fully functioning. In parallel, several other quantum computing start-up companies and R&D centers are focused on silicon-based quantum hardware including Photonic Inc. in Canada[81, 82], Equal1 Laboratories in Ireland and in the US[83, 84], Quantum Motion in the UK[85, 86], Imec in Belgium [87], Silicon Quantum Computing [88, 89], and, the newly founded start-up companies, Diraq in Australia and Siquance in France.

1.6 Bridging the gap: STMicroelectronics' approach

In the meantime, the microelectronics industry continues to grow and revenues from semiconductor manufacturing have reached hundreds of billions of dollars worldwide over the last few years[12]. In this context, two of the world leaders in the semiconductor sector, STMicroelectronics and GlobalFoundries Inc., are teaming up to build a 300 mm silicon manufacturing facility in France[13], adjacent to STMicroelectronics' existing 300 mm fa-

[12] https://www.semiconductors.org/policies/tax/market-data/?type=post

[13] https://www.lemonde.fr/economie/article/2022/07/11/semi-conducteurs-globalfoundries-et-stmicroelectronics-annoncent-la-construction-d-une-usine-a-grenoble_6134256_3234.html

cility in Crolles[14]. The project has leveraged multi-billion euro collaborative investments including significant financial support from the French government, and this jointly operated facility targets to reach full capacity by 2026, with production of up to 620000 wafers per year. It is indeed a prosperous time for microelectronics industry and all this interest will lead to improvements in materials, manufacturing equipment and processes which could drastically benefit quantum computing hardware research, and more specifically the development of high-quality CMOS-based spin qubit systems.

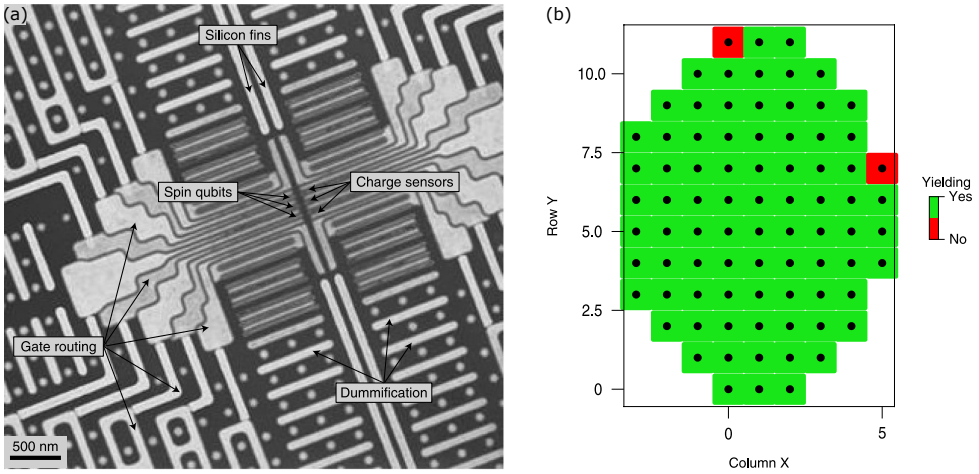

Figure 1.7 – (a) First industrially fabricated quantum dot spin qubit using all-optical fabrication methods. (b) Reported fabrication device yield up to 98%. Image taken from [79].

The development of a scalable quantum dot architecture that can be integrated into industrial manufacturing processes is of major importance for the realization of large-scale high-performance quantum processors. In this perspective, this study is focused on evaluating the potential of different architectures designed and fabricated using the industry-standard process 28 nm Fully Depleted Silicon-On-Insulator (FD-SOI) technology, which has already demonstrated functional operation at cryogenic temperatures [90, 91, 92, 93, 94], managing to combine the advantages of the current state-of-the-art quantum dot architectures and the mass-production industry techniques.

The purpose of this PhD thesis is to continue the investigation that started in 2015 in the framework of the collaboration between STMicroelectronics and Institut quantique of the Université de Sherbrooke. Aiming to explore industrial architectures for the implementation of quantum-dot single spin qubits, a modified Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) structure was characterized at cryogenic temperatures, demonstrating improved maximal carrier mobility, power dissipation and sub-threshold swing compared to room temperature operation [95, 96, 97]. In Figure 1.8, the I-V characteristic curve is shown in the case of transistor operation both at 20 mK and room temperature. This measurement permitted to characterize the technology platform fabricated using exclusively industrial techniques at deep cryogenic temperatures, allowing to

[14] https://www.lemonde.fr/economie/article/2022/09/18/en-france-un-investissement-historique-de-16-milliards-d-euros-dans-la-filiere-electronique_6142152_3234.html

envision co-integration of a CMOS-based qubit architecture with its control block technology.

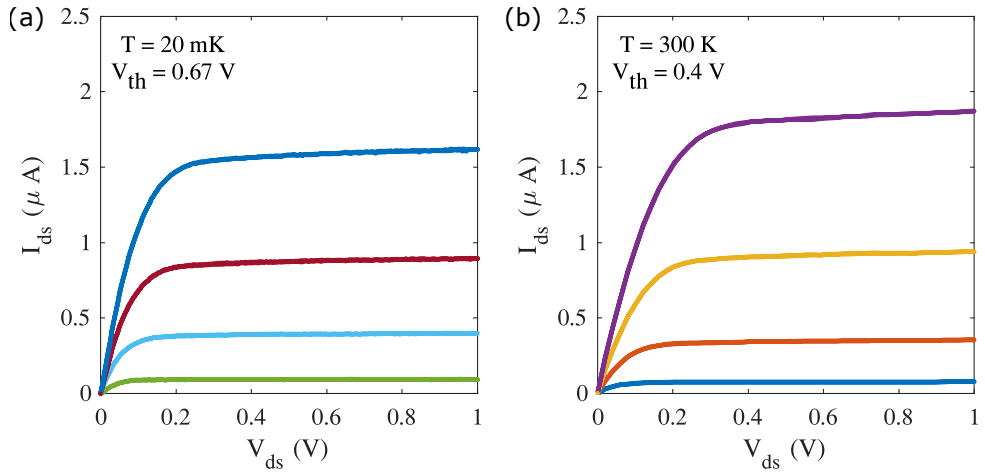

Figure 1.8 – Cryogenic temperature characterization of a modified transistor device fabricated using STMicroelectronics' industry-standard CMOS fabrication processes. (a) I-V characteristic extracted at 20 mK for different values of the voltage applied to the gate varying from 0.65 V0.65 V to 0.85 V by steps of 50 mV. (b) I-V characteristic extracted at 300 K for different values of the voltage applied to the gate varying from 0.5 V to 0.8 V by steps of 100 mV. Image taken from [95].

The electrostatic formation and control of silicon quantum dots in a 300 mm industry-standard process nanostructure was tested next, demonstrating much higher reproducibility in the transport properties compared to devices manufactured in academic laboratories [96, 98]. Moreover, the first steps towards the implementation of linear and matrix array quantum dot architectures with vertical gate access were achieved [98]. Therefore, the study presented in the following chapters is focused on improving the performance of this first generation of the gate-defined quantum dot devices, designed to implement electron spin qubits in silicon and fabricated using state-of-the-art mass-production methods from the field of microelectronics.

1.7 Thesis outline

The remainder of the thesis is divided into five chapters.

In Chapter 2, the main characteristics of the technology node used for the design and fabrication of the devices developed in this work are presented. An optimized integration process flow for the implementation of quantum devices in FD-SOI, using exclusively mass-production silicon-foundry methods is presented, focusing on reducing manufacturing risks and overall turnaround times.

In Chapter 3, a summary of the theoretical and experimental aspects is given related to the characterization of single quantum dots hosted in FD-SOI nanostructures. The

measurement circuits and methods for the characterization of the samples at room and cryogenic temperatures via electrical transport and differential conductance measurements are presented.

In Chapter 4, the experimental data collected from measuring Hall effect FD-SOI microstructures, sharing the same substrate with the quantum dots, at 4.2 K are reported. Aiming to determine the quality of the technology node for quantum dot applications, the electron density and mobility were extracted at 4.2 K through individual or combined activation of the front and back gate of the samples.

In Chapter 5, the numerical data of the cryogenic temperature simulation of the electrical and quantum behavior of the first generation quantum dot device are presented. Proceeding to a comparison with the measurement data resulted from the characterization of the same device at the same temperature, i.e. 1.4 K, the simulations permit to explain unexpected experimental observations. The study of the first generation of quantum dot devices developed in this thesis resulted in valuable insight for the geometry and bias conditions required for reaching the few-electron regime.

In Chapter 6, the investigation of a second generation of quantum dot devices, based on the previous findings, is discussed. The optical, geometrical and quantum simulations performed on the conceived device design are presented. Optical inspection and characterization of the samples demonstrate the advantages of the FD-SOI technology over other approaches for quantum information applications, as well as the identified limitations of the 28 nm node in this context. This work paves the way for the implementation of the next generations of FD-SOI quantum dot devices based on lower technology nodes.

Chapter 1 Introduction

Technology and integration flow 2

Contents

In this chapter, the integration methods used to realize the microstructures and nanodevices studied in this work are presented. First, the 300 mm industry-standard process technology platform used for the physical implementation of the devices using mass production techniques is introduced. A thorough overview of the integration process flow is also provided. Although this flow was initially developed based on the technology node used in this study, there is potential for application to other technology platforms. It was continuously improved throughout this study and was optimized for short R&D cycles in the industrial context, paving the way for a large-scale spin-based qubit processor integration with a full CMOS process.

2.1 28 nm UTBB FD-SOI technology

The devices in this work were designed and fabricated using STMicroelectronics' 28 nm Ultra-Thin Body and Buried oxide (UTBB) FD-SOI foundry-level technology [99, 100, 101, 102]. In this section, a typical 28 nm UTBB FD-SOI MOSFET is chosen as an example in order to discuss the main characteristics of the technology platform.

First, the SOI wafer is fabricated using the Smart Cut technology which was invented and patented in CEA-Leti and is now used for commercial mass-production of SOI wafers in Soitec [103, 104]. Based on hydrogen ion implantation and wafer bonding techniques, this method is used to first define a single thin monocrystalline layer on the top side of a wafer and then transfer it to another substrate. An overview of the process flow leading to the fabrication of an SOI wafer based on the Smart Cut technique is illustrated in Figure 2.1.

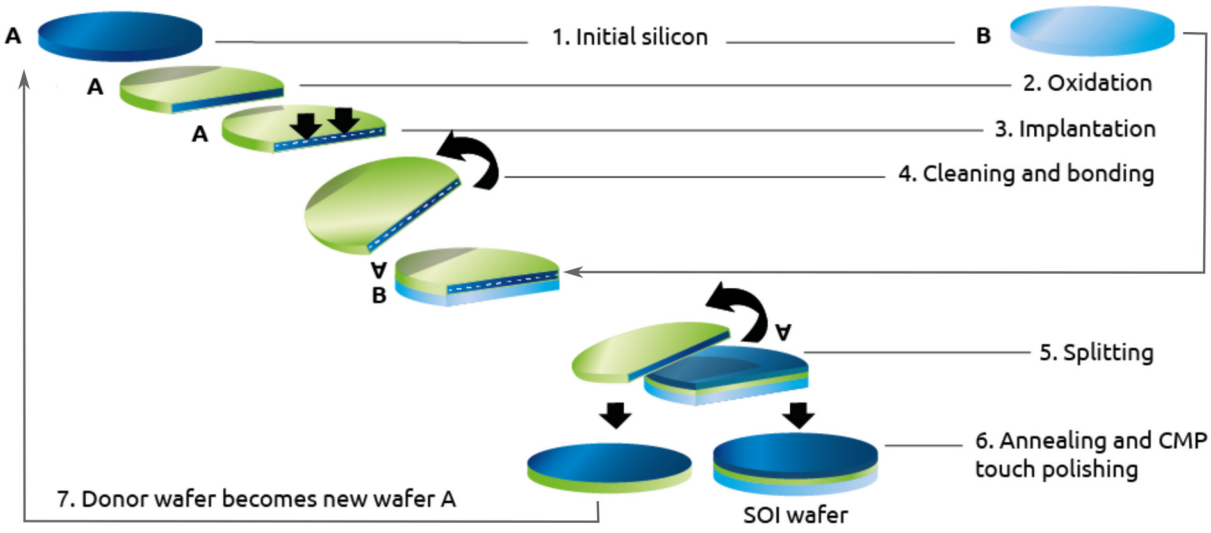

Figure 2.1 – Schematic representation of the process flow of the Smart Cut technique employed for the manufacture of SOI wafers. Image taken from the official website of Soitec.

The procedure starts with two bulk silicon wafers, wafer A or donor wafer, and wafer B. The process could also be carried out using isotopically purified silicon-28, a very

promising candidate for the physical implementation of spin qubits due to its purification of excess nuclear spin (See Introduction). The upper side of the wafer A is then oxidized creating an insulating layer with an adjustable thickness corresponding to the thickness of the Buried OXide (BOX) layer of the final SOI wafer. The wafer A is thereafter subjected to a process of hydrogen ion implantation at a controlled depth below its surface depending on the implantation energy. The resulting surface roughness is a key parameter that determines the effectiveness of the back bias control and variability. Once cleaned, the wafer A is flipped over and placed on top of wafer B before both undergo a two-phase heat treatment. During the first phase, the wafer A is divided into the two parts separated by the horizontal plane defined by the implantation depth of the previous step, resulting in the creation of an SOI layer on top of wafer B. The unused part of the wafer A is recycled and will be used in a future SOI fabrication cycle. The connection between this SOI layer and wafer B is reinforced through the second phase of heat treatment. In the end, the final stages involving annealing, and Chemical Mechanical Polishing (CMP) ensure the uniformity of the newly fabricated SOI wafer, whose silicon layer thickness is adjusted to be only a few tens of nanometres by the hydrogen ion implantation energy of the previous step, leading to the key feature of FD-SOI technology, the full depletion of the silicon channel.

Like all transistors, an FD-SOI transistor has four terminals: the source, drain, gate, and back plane. Thanks to the presence of the BOX, the latter can be considered as a back gate. By polarizing the top and back gate appropriately, the conduction channel is activated allowing current to flow through the structure between the source and the drain. A typical FD-SOI transistor fabricated with a standard process manufacturing flow is operated at temperatures ranging from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. Table 2.1 summarizes the main characteristics of the STMicroelectronics' 28 nm UTBB FD-SOI technology node [101, 105]. More precisely, the undoped silicon channel and the BOX are 7 nm and 25 nm thick respectively, hence the name Ultra Thin Body and BOX technology. In addition, the 28 nm process refers to the minimum gate width of an FD-SOI MOSFET and is used as a basic unit of measurement in IC design for the given technology.

The FD-SOI alternative addresses some of the limitations that have arisen in bulk CMOS technology as the device dimensions decrease in smaller technology nodes [106, 107, 108, 109]. For instance, thanks to the BOX layer, a better electrostatic control is achieved over the channel and the leakage currents between the different regions are reduced [110]. A more elaborate discussion on the subject of FD-SOI solution and the problems appearing in bulk technologies that it manages to tackle can be found in [111]. In the remainder of the section, a brief overview of the main features of STMicroelectronics' 28 nm FD-SOI technology is provided.

The source, drain and back plane are either n-doped or p-doped. The doping in the back place modifies the transistor threshold voltage V_{th} accordingly, which is defined as the gate voltage at which the device turns on and is a key parameter of the transistor [112, 113, 114, 115]. There are therefore two FD-SOI MOSFET options: the Low Threshold Voltage (LVT) and the Regular Threshold Voltage (RVT) transistor. In the first option, the back plane, source, and drain regions undergo the same type of doping, while in the second option, the doping in the back plane is opposite to the one in the source and drain. Furthermore, for the applications of interest, there are two gate oxide options: the

Operation	EOT	Major advantage	Major disadvantage
LVT	SG	reduced switching time	increased leakage current
RVT	EG	reduced leakage current	increased switching time

Table 2.1 – Main characteristics of STMicroelectronics' 28 nm UTBB FD-SOI technology node, suitable for the integration of quantum devices.

thin oxide or Standard Gate oxide (SG) option and the thick oxide or Extended Gate oxide (EG) option. A thin-oxide transistor contains a SiO_2 layer and a high-k dielectric HfO_2 layer with a total Equivalent Oxide Thickness (EOT) of 1.1 nm, leading to enhanced gate control over the conduction channel, but also to increased leakage currents flowing between the gate, the ohmic contacts, and the channel due to a larger number of charge carriers tunneling through the lower potential barrier imposed by the thin gate oxide. On the other hand, a transistor with a thick oxide metal gate consists of a SiO_2 layer and a high-k dielectric HfO_2 layer with a total EOT of 3.4 nm, leading to significantly reduced leakage currents but also to weakened gate-to-channel control.

In Figure 2.2, a cross-sectional and top view of the structure of an RVT N-MOS thick-oxide FD-SOI MOSFET are illustrated depicting the different layers composing the device. The source and drain regions are n-doped and are epitaxially grown leading to reduced access resistance. Spacers are used to limit the source/drain extensions, also known as Lightly Doped Drain (LDD) extensions, under the gate. The top gate stack is composed of polysilicon and titanium nitride and is deposited over the high-k thick oxide layer. Electrostatic access to the p-doped back plane is ensured thanks to the oxide trenches created using the Shallow Trench Isolation (STI) technique, which also permits isolation of the transistor from any adjacent device. Electrostatic access to the back plane is achieved through a hybrid area formed by removing the BOX from a specific region of the substrate [116], isolated from the transistor thanks to the STI technique. On top of the source, drain, and top gate, silicide is deposited to reduce access resistance and prepare the ground for the following metallic interconnections. The resulting device is surrounded by field oxide, which is an ensemble of different oxide types (mostly SiO_2). Finally, the transistor is electrically connected to the rest of the circuit and the aluminium bonding pads via several Back-End-Of-Line (BEOL) layers, consisting of copper horizontal lines and vias (vertical interconnect access) of different sizes encapsulated by TiN barriers to limit propagation into the field oxide. The type of BEOL routing scheme, e.g. a stack of eight, ten or eleven metal layers, is selected according to the system requirements.

Comparing to bulk technology, the UTBB FD-SOI technology has several advantages [117, 118, 119]. First of all, the ultra-thin silicon film drastically prevents the occurrence of undesired short-channel effects in the transistor, which arise when the gate length becomes too small and lead to a significant loss of gate-to-channel control and are detrimental to the proper operation of the transistor [120, 121, 122, 123, 124, 125]. In addition, the ultra-thin BOX allows the structure to be completely isolated from the back plane and substrate resulting in lower source and drain capacitances, reduced leakage currents flowing from the source and drain areas to the rest of the device, and protection against latch-up issues occurring when a high current flows unexpectedly through the device due to an unwanted short circuit between the supply lines [126]. Furthermore, the absence of impurities in

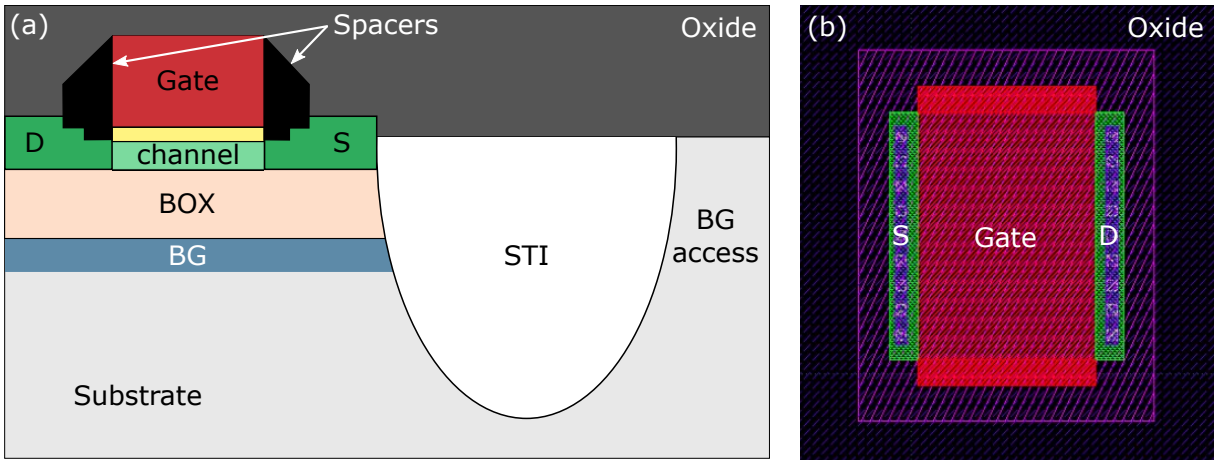

Figure 2.2 – (a) Cross-sectional schematic of a 28 nm UTBB FD-SOI MOSFET illustrating the spacers in black, the BOX in light orange, the gate oxide in yellow, and the different layers composing the four terminals of the transistor: the gate in red, the back gate (BG) in blue, the source (S), and the drain (D) in dark green. (b) Design layout of a typical RVT thick-oxide 28 nm UTBB FD-SOI MOSFET based on the STMicroelectronics' design rules. The thick-oxide option is defined by the purple layer in the layout. The pink squares represent the contacts between the active region and the first interconnect layer, which is depicted in blue.

the channel guarantees high performance and reproducibilty of the device. Finally, the BOX layer permits to significantly reduce device self-heating [127, 128, 129], whereas the epitaxially raised source and drain regions decrease thermal resistance.

2.2 Integration flow

The purpose of this section is to provide a detailed overview of the final version of the fabrication process flow used for the physical implementation of quantum devices and circuits, which was developed during this work and was the result of the application of multiple steps of verification and correction. The following chapters are focused on presenting the numerical and experimental results of this work in detail.

In Figure 2.3, the individual steps leading to the fabrication of quantum devices enclosed inside an IC package are shown, along with their connection to each other. Each block of this diagram corresponds to an individual process flow step. The average turnaround time required to develop and characterize an FD-SOI quantum system based on the proposed workflow here is approximately one calendar year, also including estimated delays due to any revisions and corrections that may have occurred in order to satisfy the specifications. In the remainder of this section, each process step is discussed in detail.

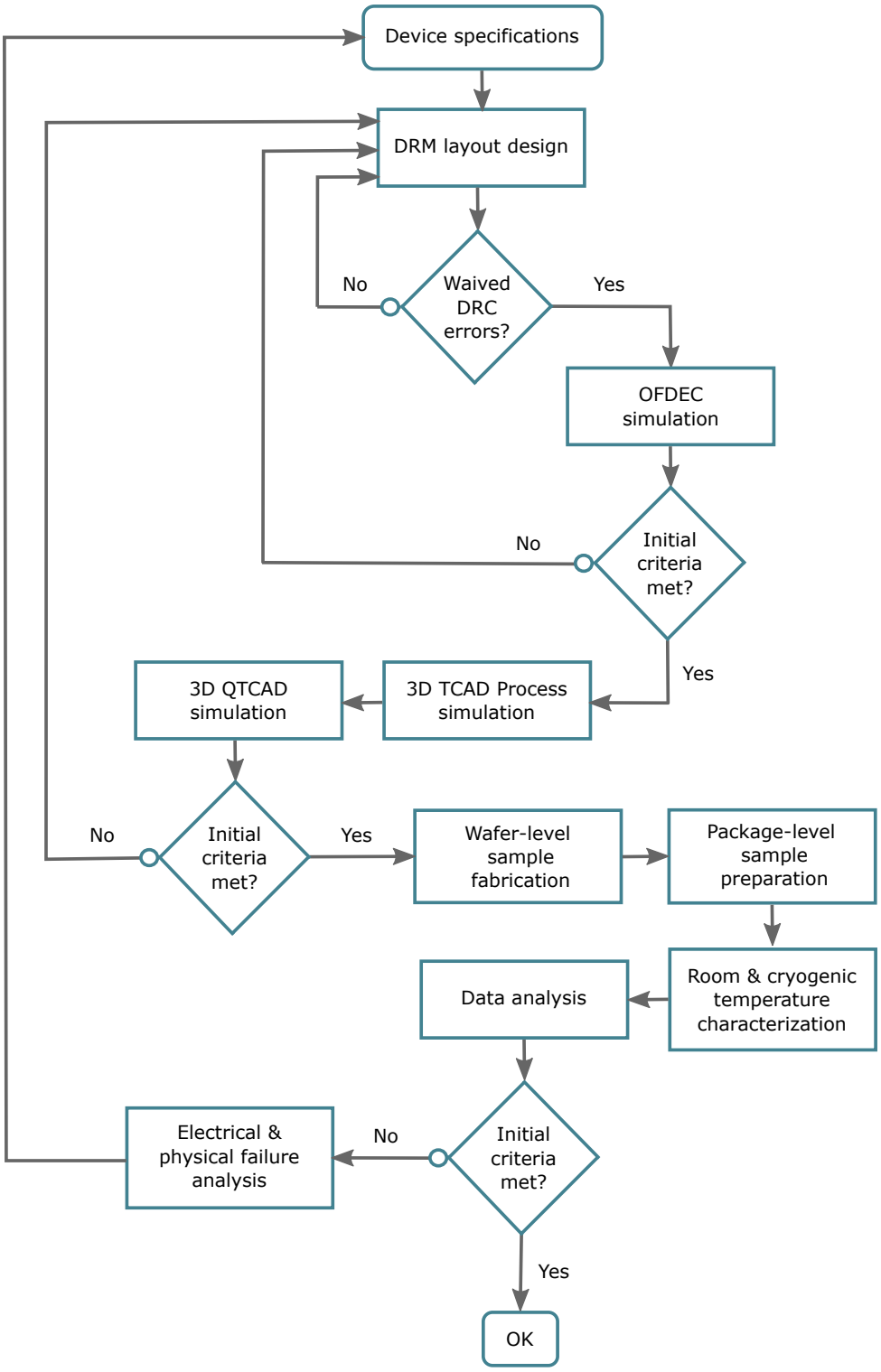

Figure 2.3 – Proposed workflow diagram representing step by step the individual tasks involved in the integration of quantum devices and circuits. Each task is linked to another via an arrow showing how those tasks are related to each other and how the various processes flow through the different stages of the system implementation giving a brief summary of the whole process.

Once the topology of the new device is well defined, the analysis continues for the remaining chip components, including the metal interconnections, bonding pads, and the Input/Output (I/O) protection ring used as an interface between the bonding pads and the chip core. The I/O ring from [130] was used as a basis for the circuit proposed here which consists of diodes designed to protect the fabricated devices from Electro-Static Discharge (ESD) effects [131] and a grid of BEOL metal connections intended to connect the devices to the bonding pads. An ESD event is able to produce hot carrier degradation and melting and can cause significant damage to the oxides, junctions, metals, and even the plastic of the IC package [132, 133, 134, 135, 136, 137, 138, 139, 140]. Notice that other components, such as transistors, can be used to protect the devices against ESD [141, 142].

An ESD stress episode is caused by contact between two electrically charged objects and occurs unexpectedly and instantaneously when an electrostatic discharge occurs between the two. Depending on the nature of charged objects involved in the event, three main ESD types are identified, namely human body ESD, machine ESD and charged device ESD, while the current intensity varies widely from one type to another. For instance, in the different cases of human body and charged device ESD incidents, the current corresponding to a 1 kV discharge ranges from 1 A to 10 A and the duration of the event from 100 ns to 1 ns, respectively [142].

To explain how the I/O ring assists to protect the chip core from ESD problems, the operating principle of a diode is recalled. More specifically, a diode is a unidirectional two-terminal electical device consisting of a p-doped region and an n-doped region that allows electrical current to flow when the proper biasing conditions are applied (Figure 2.4) [143, 144, 145]. The working principle of the diode is based on the difference in energy band levels between these two regions, which generates an electric potential barrier that prevents charge carriers from flowing through the diode. When a forward bias is applied to the diode, the barrier accross the device is reduced. After a certain voltage difference, called the diode threshold voltage, the current starts flowing from the p-doped to the n-doped region. However, at high forward bias voltages, the mobility of the carrier is decreased. On the contrary, a reverse bias applied to the diode increases the barrier potential that blocks electric transport through the diode. At very large reverse bias voltages, above a value called breakdown voltage, a breakdown of the diode occurs leading to a large current flowing through the device, if the current is not limited, causing critical damage to the diode [146, 147].

Therefore, in order to protect the test structures from ESD stress events, the diode is operated in reverse bias regime with respect to the chip core and forward bias regime with respect to ESD-induced current. To this end, the diode threshold voltage is adjusted to meet the performance requirements of the future device by carefully selecting the design and dimensions of the fabricated diode. In order to fabricate on the same wafer the bulk diodes and the FD-SOI quantum devices close to each other, the diodes are placed in a hybrid bulk region of the substrate that allows power dissipation to be achieved. In general, diodes generate noise, but this is expected to be drastically reduced at cryogenic temperatures. However, at the time of writing this thesis, no diode fabricated using STMicroelectronics' technology has yet been characterized at such low temperatures.

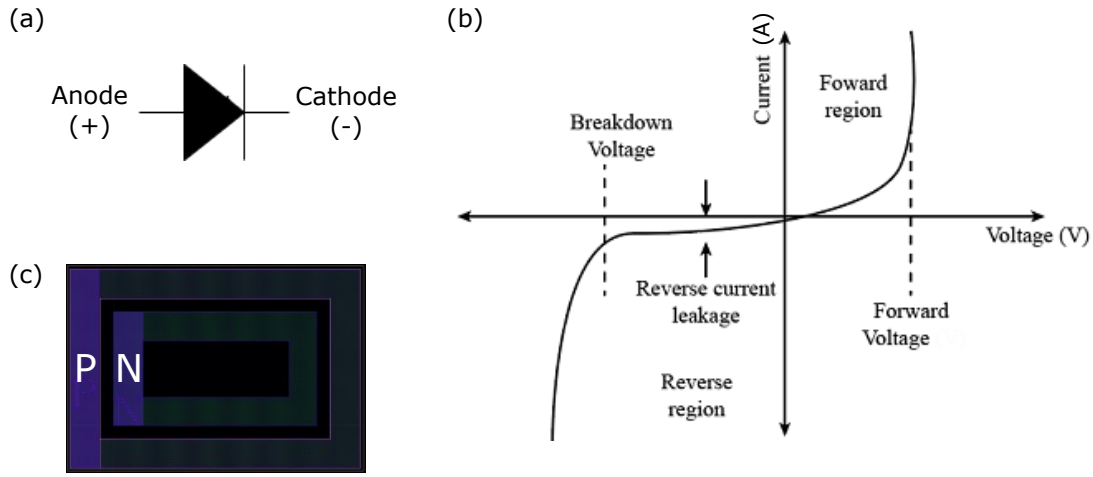

Figure 2.4 – (a) Schematic representation of a pn-junction diode. (b) I-V characteristic curve of a pn-junction diode showing the different regions of operation. Image adapted from [147]. (c) Clamp diode layout designed to limit the applied voltage on the test chip by providing protection against ESD stress events. The diode is designed in hybrid bulk and consists of a p-doped and n-doped region.

2.2.1 Test chip design

Once the specifications of the new system have been defined, the next step is to design the final test-chip layout that meets both the standard-process technology and cryogenic measurement requirements, including the Front-End-Of-Line (FEOL) and BEOL components, i.e. the individual bulk and FD-SOI devices comprising the final circuit and the metal routing scheme, respectively. Based on the requirements of the fabricated system, the appropriate FD-SOI technology options and materials are selected ensuring FEOL and BEOL compatibility. In addition, the design of the final test chip is appropriately tailored to facilitate the subsequent wire-bonding and packaging processes, along with the electrical measurements to be performed on the eventually fabricated samples. To complete the design process of CMOS systems, tiling is performed by automatically adding supplementary layers in every region of the test chip aiming to improve manufacturing feasability.

Next, validation of the final layout is carried out using the Layout Versus Schematic (LVS) verification and Design Rules Check (DRC) software tools. More specifically, based on the STMicroelectronics' Design Rules Manual (DRM), the first validation method permits to verify the agreement of the circuit layout with the corresponding schematic, ensuring the right connectivity and grounding of all the elements of the circuit. Nevertheless, as a quantum dot device schematic does not exist today in the inventory of CMOS designing tools, this step was only performed for the rest of the chip components. The second method is then employed to analyze the circuit layout based on the geometric constraints imposed by the DRM and to identify any violations of the design rules. In contrast to the mandatory correction of LVS errors ensuring the proper connectivity between the individual parts of the fabricated circuit, the design in some R&D projects may be accepted with certain DRC errors depending on their importance and impact. To

this end, these faults shall be documented and submitted as a special error exemption request to the STMicroelectronics process fabrication team. Attention shall be paid when examining the request and errors may only be accepted on an exceptional basis for the specific fabrication run taking place at STMicroelectronics in Crolles, France.

Moreover, by executing an internal STMicroelectronics' rule verification method, more rigorous than DRC, called Gds Acceptance Gating Script (GAGS), the final verification of the design is assured. The purpose of GAGS is to ensure that the omitted DRC violations do not compromise the success of the entire manufacturing process due to, for example, lift-off issues. In general, it is required that the submitted design layouts are free of DRC errors, but any GAGS violations are strictly prohibited.

Care was taken in the course of this thesis to develop a BEOL design tackling the antenna issues that occurred in the first-generation devices. In general, antenna violations are introduced in the fabricated chip by long metal lines, along with large contact, and via areas exceeding the maximum ratio defined by the DRM rules of a metal layer area to the area of the connected gates. Then, in the etching process occurring during sample fabrication, electrical charge is accumulated on the interconnect layers which could lead to a high voltage spike damaging eventually the gates connected to these layers. To fix the antenna violations, two techniques were employed in this work: reducing the contact and via areas, and routing to higher metal layers. Using the latter, the long interconnect is divided and hence the collected charge will not discharge through the gate. Also, longer metal lines are allowed by the DRM as we move on to higher metal layers.

In Figure 2.5, the design layout used to build the last generation of the test chips conceived in this study is illustrated. The layout was designed using the software Cadence Virtuoso based to a large extent on the design rules defined by the DRM of STMicroelectronics 28 nm UTBB FD-SOI technology and was composed of separate quantum devices connected with BEOL layers to the bonding pads of the I/O ring surrounding the structures. The ring also included bulk diodes intended to protect the devices from ESD stress events. Additionally, decoupling capacitors were included in the chip intended to compensate for parasitic effects in the device caused by the bonding wires. Moreover, the seal ring encircling the entire chip was designed to provide additional protection during wafer sewing, but also against moisture penetration and chemical contamination.

2.2.2 OFDEC simulation software

In order to simulate the optical lithography process and predict the wafer printing output concerning the dimensional characteristics of the future device, optical simulations are performed next using the Optical Friendly DEsign Check (OFDEC) software, an STMicroelectronics' internal calibrated simulation model. The software is commonly used to ensure that the output result matches the design and to adjust also the design of the masks that are used during the fabrication process. The optical lithography numerical results play a critical role in the risk assessment and decision making processes regarding the unavoidable DRC errors and their potential omission.

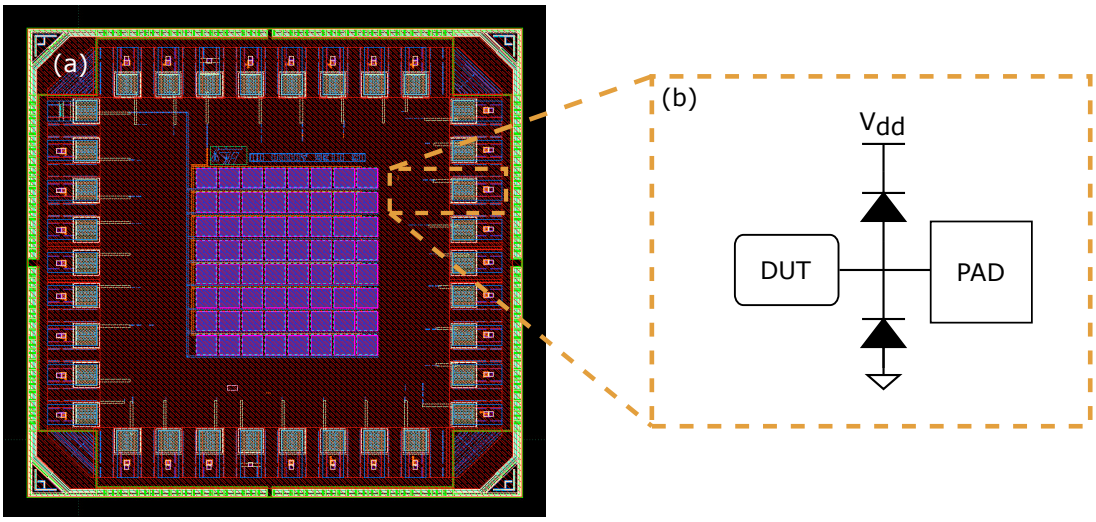

Figure 2.5 – (a) Layout of the last generation test chip developed in this work consisting of several quantum devices enclosed by a seal ring and a pad ring coupled to diodes. BEOL metal interconnect layers were designed to route the devices to the bonding pads. Decoupling capacitors were added in the middle of the chip to balance the parasitic effects due to the bonding wires. (b) Generic schematic of the electrical circuit showing the connection of the test-structure to the bonding pads, which were protected by diodes in case of ESD issues.

The first step of the optical simulation of the system involves the analysis and generation of the corresponding mask layout using STMicroelectronics' in-house CAD-to-Mask (C2M) tool based on the design layout used to manufacture the devices, together with the substrate and technology specifications. During this process, each Computer-Aided Design (CAD) layer is translated into a single photomask design. The photolithography diffraction pattern is then estimated based on the C2M photomask layout using the OFDEC software to estimate the wafer printed device features and critical dimensions. In case that the OFDEC results show a defective design, the device layout is modified appropriately and the OFDEC simulations are repeated. This optimization loop is repeated as many times as necessary until two conditions are achieved. The first condition is mandatory for all STMicroelectronics' designers and non-negotiable and requires that DRC violations must not risk harming the entire fabrication run. The second one is not mandatory though and depends mostly on each designer, as it indicates that the violations should not jeopardize the proper operation of the fabricated device.

Due to the challenging small critical dimensions of the device developed in this work, leading to significant violations of STMicroelectronics' DRM (See Chapter 6), the interest for the OFDEC calculations was focused on the regions of the conductive channel, the high-k oxide metal stack gates, and the contacts with the first interconnection layer, as these layers were the most sensitive and complex from a fabrication point of view. Nevertheless, to date at the time of writing this manuscript, the OFDEC simulation model has not been calibrated in the case of such DRM violations resulting in such small critical dimensions reaching the limits of the 28 nm FD-SOI technology. Figure 2.6 shows an example of one of the OFDEC simulated nanostructures studied here illustrating the

conduction channel in yellow color, the top gates in purple and the field oxide in black. The design layout is depicted with rectangular contours while the modeled device is presented using solid shapes. In contrast to Figure 2.6 (a) which shows the successful simulated printing of the layout on the modeled wafer demonstrating the distinguishable features of the gates individually, Figure 2.6 (b) illustrates the simulation of an unsuccessful printing of merged gates due to a modification of the spacing between them in the layout. In Chapter 6, the OFDEC simulation results are presented in detail, along with the geometry of the fabricated device.

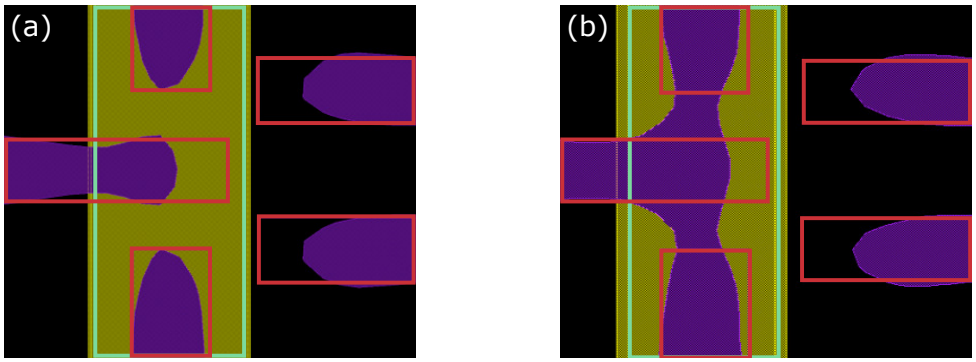

Figure 2.6 – Top view of the simulated OFDEC device focusing on the conduction channel (in yellow), the gates (in purple) and the field oxide (in black) surrounding the device. The layout of the designed device is shown with rectangular outlines: the gates in red and the channel in light green (see Figure 2.2). (a) Despite the DRC violations, the device is simulated to be successfully printed on the wafer. (b) Due to a change in the gate pitch, the photolithography simulation results indicate that the desired design has failed to be printed and the gates are merged together over the channel.

2.2.3 TCAD Process simulation software

After the implementation of any corrections to the design layout that might have arisen following the OFDEC simulations, the next step is to model the topology of the structure using the Finite Element Modeling (FEM) Technology Computer Aided Design (TCAD) Sentaurus Process software developed by Synopsys[1] [148]. At this stage, each step of STMicroelectronics standard FD-SOI manufacturing process is simulated permitting to visualize the structure geometry in 2D and/or 3D before their actual fabrication and to estimate the critical dimensions of the device along with the doping profile in the structure. The TCAD Process simulation results of this work are based on a calibrated STMicroelectronics model used to simulate the fabrication process flow applicable to the case of the 28 nm UTBB FD-SOI technology, which is adapted and optimized for DRM applications and does not anticipate certain design rule violations.

[1] https://www.synopsys.com/silicon/tcad/process-simulation.html

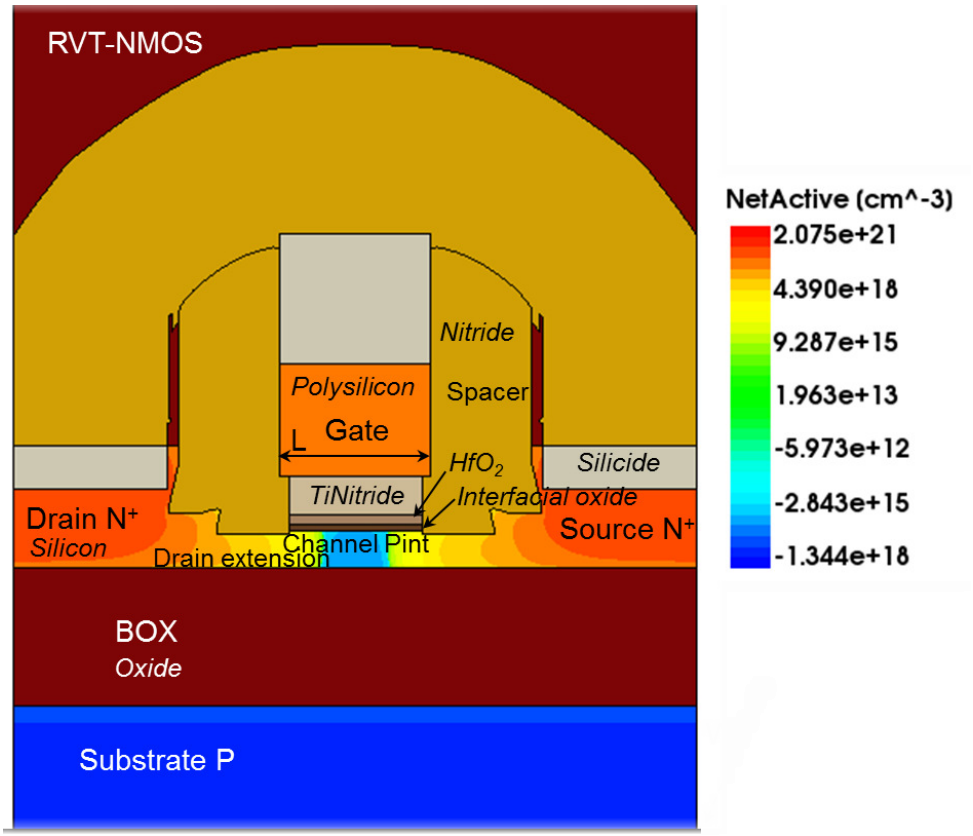

Figure 2.7 – Typical FD-SOI n-type MOSFET modeled in 2D using the TCAD Process simulation tool. The mesh of the device has been generated using the automatic adaptive grid technique. The colorbar shows the doping concentration in the transistor.

The TCAD Process modeling of the fabrication process flow of a conventional 28 nm FD-SOI MOSFET is explained here as an example. In Figure 2.7, the resulting 2D TCAD Process model in the case of an n-type transistor is illustrated. The geometry of the structure is first defined and the mesh is then automatically generated by dividing the structure into a non-uniform grid of nodes based on the final layout used for the actual fabrication of the transistor. Using the automatic adaptive mesh feature of the software, no manual refinement of the mesh is required and only the improvement criteria per region are specified depending on the desired level of accuracy. If needed in a future simulation step, the mesh is further refined ensuring the appropriate refinement conditions in the region of interest.

The physical parameters and models at each grid node are next defined and calculated. The simulation is implemented by executing a sequence of commands corresponding to the individual fabrication steps, including ion implantation, diffusion, oxidation, etching, layer deposition, photolithography, and silicidation. A general overview of the fabrication process is presented in detail in the remainder of the section without revealing though additional information concerning the fabrication parameters such as critical dimensions, layer thickness, annealing time, etc. for confidentiality reasons.

2.2.4 QTCAD simulation software

Following the validation of the device geometry via the TCAD Process simulations and any corrections on the layout that may arise, the next step in the workflow is to model the test-structure using the Quantum TCAD (QTCAD) simulation tool[2]. Achieving convergence at very low temperatures which is still an unsolved problem for classical TCAD software [58, 149, 150], this FEM software developed by Nanoacademic Technologies Inc. allows the simulation of the electrical and quantum behavior of the fabricated device at cryogenic temperatures prior to actual fabrication.

In the framework of the collaboration between Nanoacademic Technologies, Institut quantique and STMicroelectronics, a QTCAD model suitable for the simulation of 28 nm UTBB FD-SOI quantum devices at cryogenic temperatures was developed. This model was finalized in the last year of this PhD project and, therefore, the QTCAD software was used to model the structures that had been already fabricated and measured a few years ago, permitting to understand better unexpected experimental observations. Nevertheless, in the fabrication process flow proposed here, it is suggested that these simulations are performed after the TCAD Process simulations and before the actual fabrication of the device. This sequence allows not only to predict the performance of the future test structure and implement any design changes that may be necessary, but also to compare a set of designed devices without having to wait for the completion of the long fabrication cycles and series of cryogenic measurements.

To perform a QTCAD simulation, the 3D geometry of the nanostructure must be generated again. To do so, either the automatic adaptive mesh method [151] is employed by importing the geometry directly from the layout of the device, or the FEM mesh generating tool Gmsh [152] is used, and then the resulting mesh file is imported into QTCAD. All simulations are defined and launched using QTCAD Python API. Next, the different domains of the regions are defined, along with the materials and doping levels. The electrodes and ohmic contacts are also specified. In all simulations isothermal conditions are assumed with a uniform temperature of a few kelvin or millikelvin imposed across the device. The top gates and ohmic contacts set Dirichlet boundary conditions on the electrostatic potential, whereas the BEOL interconnections to the bonding pads are not included in the simulation. Finally, a set of equations describing the electrical and quantum mechanisms are specified and solved at each node of the mesh.

In Chapters 5 and 6, the QTCAD mathematical and physical models used for the investigation of the behavior of the quantum dot devices of this work are presented in detail. In short, the simulation procedure followed in this work starts by the electrostatic calculation at 1.4 K by solving the non-linear Poisson equation, permitting to estimate the conduction band edge profile across the device demonstrating potential wells in specific regions. These simulations are also exploited to explain experimental measurements of charge stability diagrams for transport activation. Bound states in the structure are then investigated by solving the single-electron effective-mass Schrödinger equation in the regions of the calculated potential wells. Finally, the many-body Schrödinger equation is solved in order to calculate the theoretical location of Coulomb blockade peaks

[2] https://docs.nanoacademic.com/qtcad/introduction/

corresponding to few-electron states in side-gate activated quantum dots.

2.2.5 MPW fabrication

After the completion of the simulations and incorporation of any design changes that may have been introduced, the final layout is submitted for manufacturing to the STMicroelectronics' Multi-Project Wafer (MPW) fabrication run of interest, along with the DRC and GAGS analysis results. In IC design, the final product of the design process, including the C2M and OFDEC analysis, is known as tape-out. During this work, six tape-outs have been submitted to a total of three MPW runs. All samples were fabricated on a 300 mm diameter SOI wafer (Figure 2.8) in the STMicroelectronics' $10^4\,m^2$ surface area and ISO 4 class clean room in Crolles, France. The production process runs 24 hours a day and 7 days a week. Human interaction is minimized thanks to an automatized transport system located on the ceiling allowing the transfer of wafer lots from one manufacturing stage to another along rails. The wafers are always carried in Front Opening Unified Pods (FOUPs) ensuring safe transport in a controlled environment. Articulated robotic arms lower the wafers vertically once they reach their destination. Machines fixed to the floor are used to perform various different tasks such as resin application, metal layer deposition by lithography, etc. Clean room operators and technicians monitor the whole process and their responsibilities consist mainly of visually inspecting the wafers, constantly supervising the proper functioning of the equipment systems, identifying and resolving any kind of problems that may arise. However, despite the automatisation of a great number of manufacturing steps, the final inspection of the fabricated wafers is only partially carried out by vision tools and is always performed by an operator.

The entire process of creating a silicon wafer with functional devices and circuits consists of several steps such as photolithography (exposure and development), etching, CMP, thermal treatment, implantation, metrology, process corrections etc. For instance, the manufacturing process in the case of the 28 nm FD-SOI technology consists of approximately 900 operations, depending on the design. As an example, a brief overview of the main stages of the front-end fabrication of a 28 nm FD-SOI n-type MOSFET (Figure 2.9 (a)) is given next. The procedure begins with an SOI substrate with a 25 nm BOX and a 7 nm active silicon layer. The STI trenches are formed first via etching. Next, back plane implantation is realized by introducing either As or P dopants for n-type implantation and In or B for p-type. The isolated active device regions are formed by photolithography and dry etching, followed by the creation of the gate consisting of SiO_2 and HfO_2 for the thick oxide layers, TiN and polysilicon layers for the metal stack using the appropriate photomask set. In the case of the 28 nm FD-SOI technology, the optical lithography process is realized using the 193 nm immersion scanner, fabricated by ASML. The first spacer is formed by Si_3N_4 uniform deposition everywhere and then by dry etching, acting as a protective mask for the active region during source and drain implantation. Next, the LDD regions of source and drain extensions are formed by opening a window on the mask in both the source and drain areas, followed by As or P implantation. A second spacer is then formed in the same manner as the first, permitting to obtain elevated source and drain regions for reduced series resistance. Implantation of As or P in the source and drain follows the same procedure as LDD, but with a higher dose and energy than before, and

rapid thermal annealing is used afterwards to activate the dopants. In the end, metal silicide is formed on top of the source, drain, and gate regions, and the back-end fabrication process begins.

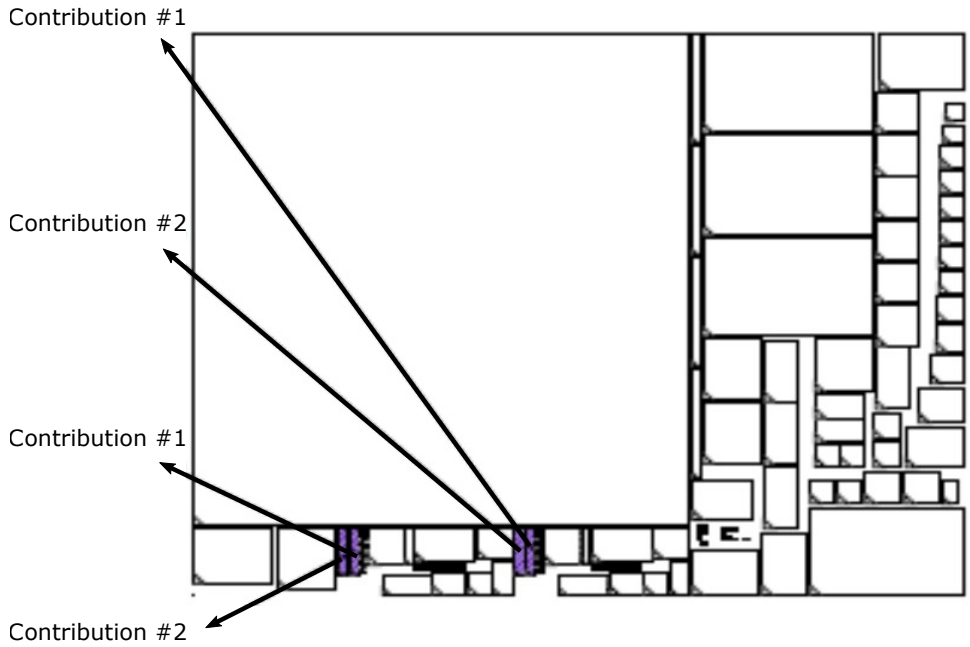

Figure 2.8 – Wafer floorplan top view from one of the three MPW fabrication runs of this work. Two of the contributions conceptualized during this project, duplicated on the wafer and surrounded by several devices and circuits (white rectangulars), are depicted with purple.

In order to integrate a bulk device on a bulk substrate starting from an SOI wafer, the hybrid 28 nm FD-SOI/bulk approach is used. Figure 2.9 (b) illustrates a hybrid system fabricated in STMicroelectronics, composed by an FD-SOI device located next to a bulk structure isolated from each other thanks to an STI trench. The bulk region is created by identifying the area of interest on the SOI substrate and etching away the ultra-thin silicon layer along with the BOX layer in order to create an opening to the silicon bulk substrate underneath.

2.2.6 Sample preparation

After the completion of the MPW manufacturing cycle, the wafers are delivered to the designers. As all the measurements presented in the following chapters were carried out at Institut quantique, the samples were prepared at STMicroelectronics for shipment without performing any wafer-scale characterization measurement. During this project, the average time between design submission and shipment of the prepared samples was approximately one calendar year.

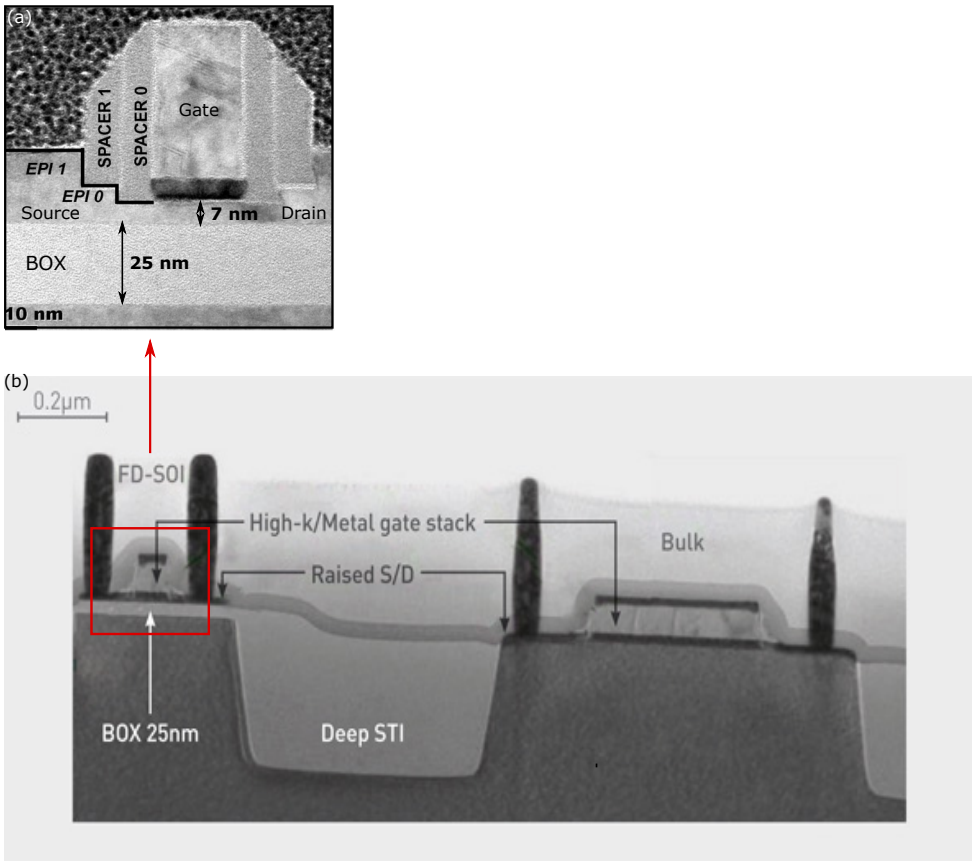

Figure 2.9 – (a) TEM image of a standard-process n-type 28 nm FD-SOI MOSFET fabricated in a STMicroelectronics MPW production run. The two spacers and the different regions of the BOX, gate, and epitaxially grown source and drain are distinguished. Image adapted from [102]. (b) TEM image of a hybrid FDSOI/bulk system. The main FD-SOI characteristics are visible, except for the bulk area where the BOX has been removed. Image adapted from [153].

Throughout the sample preparation process, care is always taken when handling and manipulating the samples, assuring protection from ESD-induced stress damages. The wafers were diced at STMicroelectronics into individual dies of a few millimetres squared surface area containing several micro- and nano-devices and half of the dies were placed in an electrostatic dissipative Gel-Pak box while the other half were enclosed inside an IC package, a method widely used in the microelectronics field.

To package the samples, a Fine pitch Land Grid Array (FLGA) package was chosen. This $9.0 \times 9.0 \times 0.8$ mm-body, 65-land and 0.5 mm-pitch package is fabricated by STMicroelectronics and is commonly used for IC applications. In Figure 2.10, the FLGA electrical circuit is shown, consisting of a Printed Circuit Board (PCB) on a laminate substrate with plastic overmolded encapsulation. Based on a two-level interconnection system, the sample is placed in the center of the package and is wire-bonded with gold wires to the bonding fingers which are then connected to the lands of the package directly on the PCB. In the end, the package is filled with epoxy resin ensuring good stabilisation of the entire content.

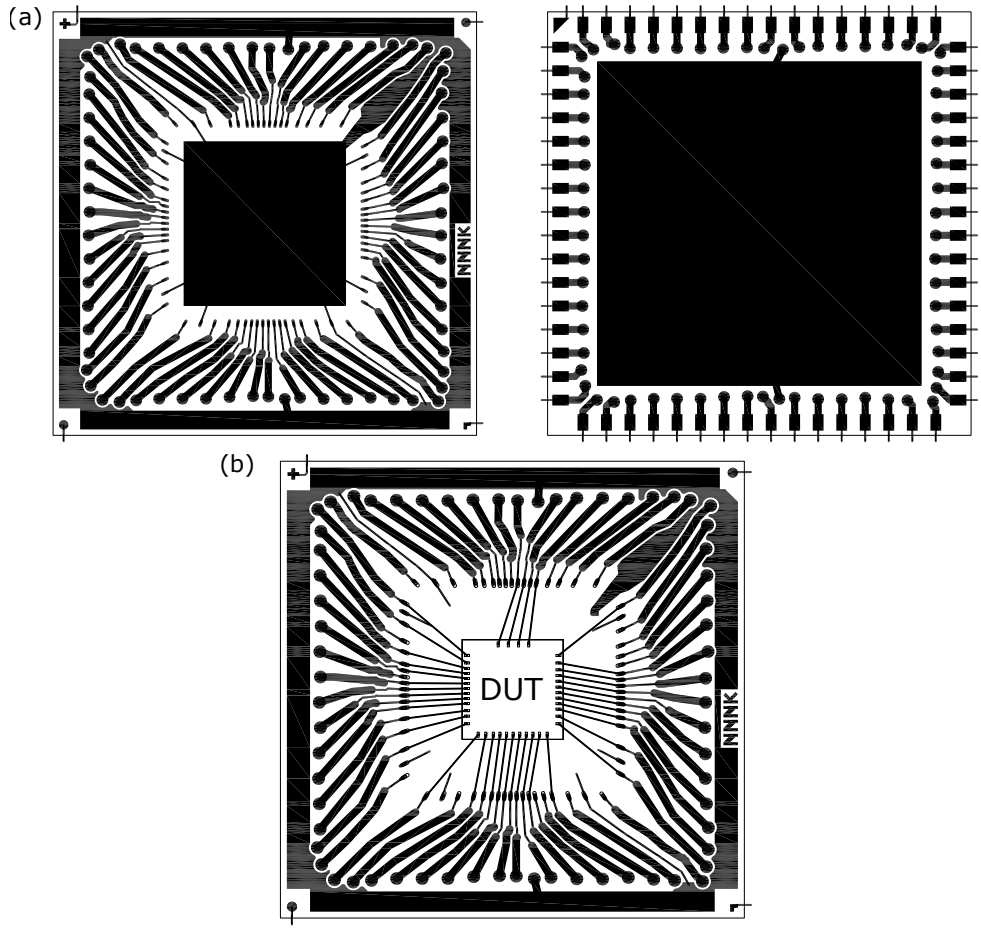

Figure 2.10 – (a) Top view (left) and bottom view (right) schematic of the interior of an FLGA package used to connect the fabricated samples to the measurement equipment typically used in microelectronics. The bonding fingers and connecting lands are visible. (b) Schematic representation of an installed sample in the packaging. The device under test is wire-bonded to the bonding fingers which are connected to the package lands via a network of PCB lines.

2.2.7 Sample characterization

After being prepared, the Gel-Pak box and FLGA packages containing the fabricated samples were shipped from STMicroelectronics to Institut quantique. In the following chapter, the characterization methods and the experimental circuits that permitted to perform room and low temperature measurements on the fabricated samples employing a cryogenic probing system and a variable temperature inset cryostat are discussed in detail. In general, the average processing time required for characterization of a single sample is one month.

In order to measure the packaged samples, a homemade 64-pin interposer constructed at Institut quantique was used as a solderless interface routing between the test-structure and the measurement equipment (Figure 2.11) [154]. The interposer contact system, widely used in today's advanced semiconductor products, is based on the mechanical com-

pression under pressure of the packaged die enabling contact with the interposer PCB. This was a critical milestone achieved during this project, as such a solderless interconnection system allowed to completely avoid the method of wire-bonding in the university laboratory, a process that proved to be quite challenging due to the small dimensions of the device and due to several problems caused by ESD.

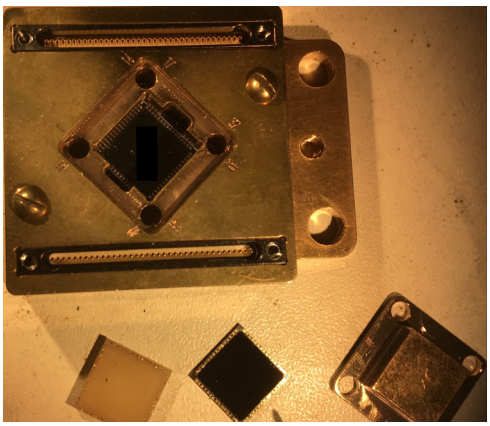

Figure 2.11 – 64-pin homemade interposer [154] served as an interface routing method between FLGA-packaged samples and measurement equipment, leading to significantly reduced ESD-induced issues and improved workflow turnaround times.

2.2.8 Data analysis

Following the sample characterization, the extracted experimental data are analyzed and evaluated. Compared to the numerical data calculated with the simulation tools previously presented, a quantitative agreement is expected between theory and experiment. It is worth noting that the simulation of the device performance at cryogenic temperatures is limited, as the cryogenic temperature sample characterization is realized out of the standard temperature range of operation of the 28 nm FD-SOI technology which is −40 °C at the lowest.

2.2.9 Failure analysis

If the analyzed experimental data deviate significantly from the numerical data indicating that the initial specifications are not met, a complete investigation of the device is essential in order to identify the root cause of the failure. The choice of the methods used for this analysis is decided depending on the nature of the issue at hand. In this work, a physical analysis of the device is selected for the inspection of the test structures failing to fulfill the requirements, as the identified fabrication risks are mostly related to the contour of the gates via OFDEC simulations. More specifically, a cross-sectional and top-view imaging analysis are used to study the geometry and physical characteristics of the fabricated device.

The fabricated samples are prepared for the failure analysis in STMicroelectronics by

selective removal of the top layers through a milling process. Then, electron microscope imaging techniques, such as Scanning Electron Microscope (SEM) and Transmission Electron Microscope (TEM), are used to inspect the top view and cross section of the structure respectively and to verify the fabricated device dimensions. Finally, the extracted microscope images are compared to the design layout and any differences that may have arisen are recorded. In Figure 2.12, an example of an unsuccessful attempt to fabricate a gate-based quantum dot device is shown, where the top gates designed to control the formation of the electron reservoirs and the quantum dot were merged with each other during the manufacturing process.

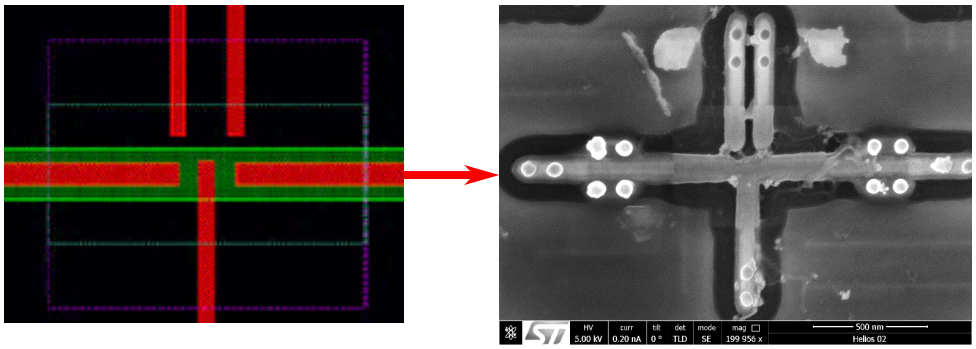

Figure 2.12 – SEM top-view image as part of the failure analysis performed on an unsuccessfully fabricated quantum dot device demonstrating the unwanted connection of the top gates with each other. The initial design of the device showing three separate top gates is given on the side for comparison.

2.2.10 Optimization loop

The numerical and experimental results, as well as the failure analysis, allow to identify solutions in order to overcome the challenges that may have arisen by implementing changes in the design of future test-structures and repeating from the beginning the process flow proposed here for the physical implementation of improved and more robust FD-SOI quantum devices.

2.3 Chapter summary

In this chapter, the main characteristics of STMicroelectronics' 28 nm UTBB FD-SOI technology have been presented. In addition, the crystallization of a dedicated process flow for the physical implementation of quantum devices and circuits is reported here. The proposed workflow leads to reduced risks and optimized turnaround times using standard-process CMOS mass-production methods, widely used in the field of microelectronics. Starting from defining the device specifications, the design of the test chip layout is realized next, followed by the simulation of the device using three different simulation tools for optical, geometrical, and quantum modeling. After the fabrication of the device on a 300 mm MPW using deep UV photolithography, the chip is put inside an IC package

and the samples are characterized at cryogenic temperatures. Finally, an optimization loop ends the process providing valuable feedback for the next generation of quantum devices, based on the experimental data and any failure analysis that may occur on the fabricated samples.

Characterization methods for quantum dot systems

3

Contents

In order to understand the numerical and experimental results presented in the remainder of the thesis, an overview of the key concepts related to quantum dots defined in silicon nanostructures for the realization of spin qubits and the characterization of their performance is presented in this chapter. In the first section, the operating principles of a 2DEG and single quantum dot formed in a semiconductor device are first discussed. Then, the model used to describe the quantum dot is described, followed by the coupling regime of the dot with the electron reservoirs. The Coulomb blockade occurring in quantum dot devices is presented, along with the main principles of the transport mechanisms through the system. In the second section, the cryogenic measurement systems and the experimental setups are first presented. Next, the methods used for evaluation of the performance of the fabricated quantum dot devices are detailed. Finally, the structure of the rest of the thesis is outlined.

3.1 Background

The aspects that describe the behaviour of single quantum dots hosted in semiconducting nanostructures are introduced in this section in order to facilitate the understanding of the research carried out in this work. The discussion is mostly restricted to the regime of weak tunnel coupling between the dot and the nearby charge carrier reservoirs, as this is most relevant to the scope of the study. Today, several books and reviews exist giving a thorough account of the physical principles governing the operation of solid-state devices whose length is smaller than the electron mean free path, and in quantum transport in semiconductor nanostructures to which the reader is referred for more information [155, 156, 157, 158, 159].

3.1.1 2D electron gas model

A two-dimensional electron gas (2DEG) is a region defined via a strong electrostatic confinement at the interface between two semiconductor layers, e.g. a GaAs-AlGaAs heterostructure, or at the interface between a semiconductor and an insulator, e.g. a silicon-inversion layer with a SiO_2 layer playing the role of the insulator. Electrons in such regions are confined in the third spatial dimension and can only move in a plane, described by a stationary wave with certain allowed wave numbers k. A gate electrode deposited on the top semiconductor layer is used to control the surface density n_s of the 2DEG. According to the definition of a parallel plate capacitor

$$C = \epsilon_0 \epsilon_r \frac{A}{t}, \tag{3.1}$$

where ϵ_0, ϵ_r are the vacuum electric permittivity, and material relative permittivity respectively, A the surface area, and t the thickness. The 2DEG density n_s depends linearly from the electrostatic potential V_G applied to the gate electrode

$$n_s = \frac{\epsilon}{et} V_G, \tag{3.2}$$

where e is the elementary charge. In the case of a SiO_2 layer, $\epsilon = 3.9\epsilon_0$.

The energy of non-interacting electrons in the conduction band is given by

$$E(k) = \frac{\hbar^2 k^2}{2m^*}, \tag{3.3}$$

where m^* is the effective mass.[1]

In the case of a laterally confined 2DEG, e.g. in a narrow channel, Equation 3.3 describes only the kinetic energy of a free electron having a momentum $\hbar k$. Due to the spatial confinement, the conduction band edge is separated into a sequence of one-dimensional subbands with minima at the energy levels E_n for $n = 1, 2, ...$ Then, in zero magnetic field, the total energy $E_n(k)$ describing the electron is given by

$$E_n(k) = E_n + \frac{\hbar^2 k^2}{2m^*}. \tag{3.4}$$

3.1.2 Single quantum dot

A single semiconductor quantum dot is a zero-dimensional submicron region defined electrostatically in a 2DEG, containing therefore charge carriers confined in all three spatial dimensions. The size of the dot, or island as it is also called, is comparable to the Fermi wavelength[2], leading to quantization of energy in this area. This behavior is similar to an atomic system and, for this reason, the quantum dots are also called artificial atoms [161].

Several different ways are employed today in order to define a quantum dot in a solid-state structure, such as vertical quantum dots [161] or self-assembled quantum dots [162, 163, 164, 165] and this study focuses on laterally defined quantum dots. The island is coupled to charge reservoirs via potential tunnel barriers. The realization of holes confinement in the quantum dot [54, 166, 167] is equally possible as the confinement of electrons by selecting the doping of the source and drain appropriately. This work is focused on electron confinement in quantum dots and, for this reason, an electron system is considered in the remainder of the discussion.

3.1.3 Constant interaction model

The simplest model considered for modeling a quantum dot system is the constant interaction model [168]. In this model, the quantized energy levels of the dot due to the spatial confinement, and the Coulomb repulsion between the electrons are taken into account, along with the energy required to overcome it and add a new electron into the island. The

[1] In silicon, it's $m^* = 0.19m_e$ indicating that m^* is smaller than the free electron mass m_e, due to interactions occurring with the lattice potential. [25]

[2] In the case of semiconductors, the Fermi wavelength is approximately 50-100 nm.[160]

Coulomb interaction is assumed to be constant and independent of the number N of electrons populating the dot. In this context, the constant capacitance $C = C_S + C_D + C_G$ is used to describe the whole capacitance associated to the dot, where C_S, C_D, and C_G are the capacitances corresponding to the source, drain and gate, respectively.

The equivalent circuit shown in Figure 3.1 illustrates a small island representing a single quantum dot coupled to the two leads of the source (S) and drain (D) through tunnel barriers which are described by a tunnel coupling Γ and a capacitance C in parallel. The dot is also capacitively coupled to an electrostatic gate, designed to control the electron occupancy in the island. This feature is explained from the classical electrostatics by recalling the definition of capacitance $C = Q/V$ as the amount of charge Q stored in any one of the plates of a plate capacitor when a voltage difference V is applied between them. The number of electrons on the island is an integer number N and electron exchange occurs between the dot and the electron reservoirs of the source and drain.

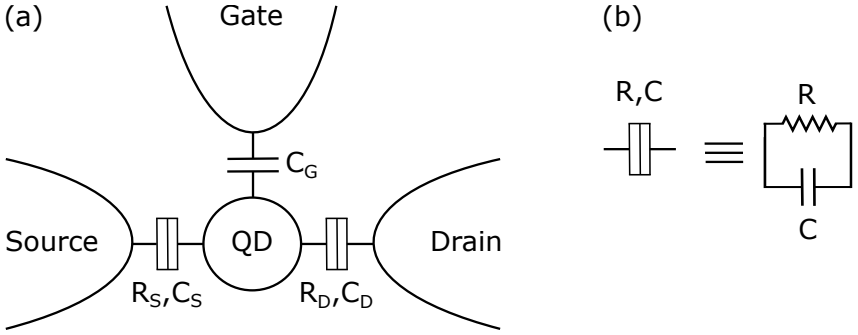

Figure 3.1 – (a) Electrical schematic of a single quantum dot coupled through tunnel barriers to the source and drain reservoirs. A gate electrode is used to control the dot electron occupancy. (b) Electrical symbol of a tunnel barrier, described by a resistance R and a capacitor C.

Any second order effects are not considered in this model, and the single-particle energy spectrum is assumed to be independent from any interactions between the charge carriers. Therefore, the total energy $E(N)$ describing the quantum dot containing N electrons is given by

$$E(N) = \sum_{n=1}^{N} E_n + \frac{e^2(N - N_0) - C_G V_G - C_S V_S - C_D V_S}{2C}, \tag{3.5}$$

where $N = N_0$ for $V_G = 0$, e the elementary charge, and V_S, V_D, V_G the voltages applied to the source, drain, and gate respectively. The first term stands for the summary of the confinement energy of each electron when N electrons are loaded into n dot energy levels in total. The second energy term is used to express the electrostatic energy of the quantum dot and is analyzed in detail in the remainder of the section.

Depending on the system and the model that is used to describe it, the energy term E_n has different definitions. For instance, if the confinement in the dot is modeled by the potential of an harmonic oscillator, the confinement energy is then expressed by the

relation

$$E_{\mathrm{n}} = \left(n + \frac{1}{2}\right)\hbar\omega, \tag{3.6}$$

where n and ω are the quantized energy levels in the quantum dot and the angular frequency.

3.1.4 Weak coupling regime

The quantum dot is coupled to the source and drain reservoirs by a tunnel coupling rate Γ. Two regimes are distinguished based on this definition; the weak coupling regime $k_{\mathrm{B}}T \gg \hbar\Gamma$, and the strong coupling regime $k_{\mathrm{B}}T \lesssim \hbar\Gamma$ [169, 170, 171]. The first regime is explained here as it is more relevant to the results presented in the remainder of the thesis.

Therefore, in the weakly coupling regime, electronic transport through a quantum dot structure is governed by the Coulomb repulsion occurring between charge carriers. This effect leads to single-electron charging effects and the dot occupancy can be controlled via the capacitive coupling with the gate electrode.

3.1.5 Coulomb blockade effect

The electrochemical potentials of the source and drain, μ_{S} and μ_{D} respectively, depend on the source-drain bias V_{ds}, while the electrochemical potential of the quantum dot μ_N changes as a function of the voltage V_{G} applied on the gate. Only when the electrochemical potential of the dot lies between the potentials of the source and drain, i.e. $\mu_{\mathrm{S}} > \mu_{\mathrm{N}} > \mu_{\mathrm{D}}$, transport across the structure is allowed and electrons tunnel through the quantum dot in sequencies of one. Otherwise, i.e. $\mu_{\mathrm{N}} < \mu_{\mathrm{D}}$ and $\mu_{\mathrm{N+1}} > \mu_{\mathrm{S}}$, transport in the system is blocked and the system is then said to be in Coulomb blockade [172, 173, 174, 175, 176]. In Figure 3.2 (a) and (b), considering that both the source and drain reservoirs are connected to the same electrical potential and their electrochemical potentials are in equilibrium ($\mu_{\mathrm{S}} = \mu_{\mathrm{D}}$), an example of blocked and permitted transport through a single quantum dot structure is illustrated.

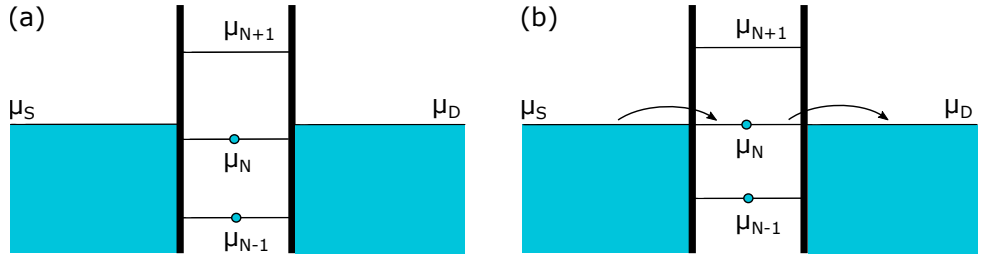

Figure 3.2 – Energy diagram of a single quantum dot system in the Coulomb blockade regime. Two tunnel barriers connect the quantum dot with the source and drain electron reservoirs. (a) The transport through the system is blocked. The next unoccupied energy level in the dot lies higher than the electrochemical potential of the source, so that $\mu_{\mathrm{N}} < \mu_{\mathrm{D}}$ and $\mu_{\mathrm{N+1}} > \mu_{\mathrm{S}}$, and as a result no electron can tunnel through the dot. The system is in Coulomb blockade. (b) The transport through the system is activated. The electrochemical potential of the quantum dot is between the electrochemical potential of the source and drain, so that $\mu_{\mathrm{S}} > \mu_{\mathrm{N}} > \mu_{\mathrm{D}}$, and electrons tunnel through the dot one by one.

Energy scales

Two energy scales are associated to the system of a quantum dot [169]. First, the classical charging energy E_{C} is defined as the energy needed to overcome the Coulomb repulsion between two electrons loaded into the dot. It ranges from a few μeV to several meV and is given by the formula

$$E_{\mathrm{C}} = \frac{e^2}{C}, \tag{3.7}$$

showing that the charging energy E_{C} is inversely proportional to the capacitance C corresponding to the dot. The definition of a parallel plate capacitor (Equation 3.1) indicates that any reduction realized to the dot size leads to a decrease in the dot capacitance C, resulting to an increase in the charging energy E_{C}. Finally, the second energy scale associated to a quantum dot system is the quantum mechanical confinement energy E_{n}, due to the spatial confinement in the quantum dot region.

Coulomb blockade peaks

At a small V_{ds} bias, oscillations are observed in the current I or the conductance G in the structure as a function of the voltage V_{G} applied to the gate, whenever the electrochemical potential of the dot μ_{N} lies between the electrochemical potentials μ_{S} and μ_{D}. These oscillations are called Coulomb blockade peaks. Between Coulomb peaks, transport is blocked due to the Coulomb blockade effect, and at each peak, the number of electrons loaded into the dot is modified by one. For quantum dots with constant charging energy E_{C}, a sequence of regularly spaced peaks in current or conductance is exhibited, as shown

in Figure 3.3.[3]

In the low bias regime, the source-drain voltage difference V_{ds} is low compared to energy level spacing in the dot and the charging energy E_C. When applying a larger bias V_{ds}, the Coulomb peaks become wider, as more than one quantum dot energy levels are now inside the bias window. In addition, if the tunneling resistance R is chosen to be greater than the quantum of resistance h/e^2, the number N of electrons on the island can be then treated as a strictly defined classical variable.

In order to observe the Coulomb blockade effect, apart from the requirement of the small bias voltage, one more criterion has to be met. More specifically, the sum of the charging energy E_C and the confinement energy E_n must be greater than the thermal energy: $E_C, E_n > k_B T$ with k_B the Boltzmann constant and T the temperature [168]. For this reason, Coulomb blockade measurements are carried out at cryogenic temperatures below a few K, leading to an energy level spacing inside the island much larger than the thermal energy. Any thermal excitations are thus avoided and discreet energy levels become distinguishable permitting transport to occur by resonant tunneling through the quantum dot. Furthermore, since both E_C and E_n increase when the dimensions of the quantum dot decrease, the smallest island possible is aimed.

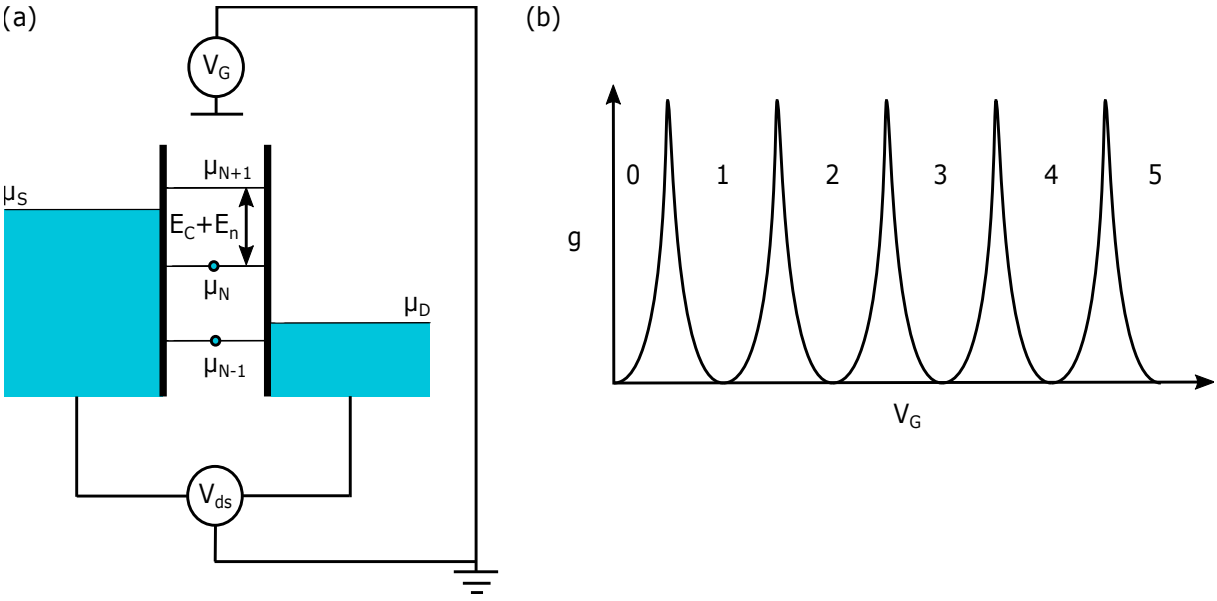

Figure 3.3 – (a) Energy diagram for a single quantum dot system in the Coulomb blockade regime when a small V_{ds} bias is applied permitting to obtain a small bias window. The energy levels of the dot are controlled by the voltage V_G applied to the gate electrode. (b) Measured conductance as a function of the voltage V_G applied to the gate showing Coulomb blockade peaks. At each peak the number of electrons N loaded into the dot changes by one, whereas in between transport is blocked due to the Coulomb blockade effect.

[3] Coulomb oscillations occurring in a realistic semiconductor device are not periodic and lead to Coulomb peaks without identical heights.

Lever arm

The expression of the electrostatic energy of the dot (Equation 3.5) gives rise to the definition of the lever arm, a metric for the capacitive coupling of the gate, expressed as

$$\alpha_i \equiv \frac{C_i}{C}, \tag{3.8}$$

where C_i is the capacitance associated with a single electrode or contact.

Therefore, the resulting voltage difference applied to the dot is given by

$$V_{\text{dot}} = \sum_i \alpha_i V_i, \tag{3.9}$$

where V_i is the voltage applied to each gate or contact, explaining how the gate bias V_G can thus be used to shift the electrostatic energy in the region of the quantum dot for $C_G >> C_d, C_s$.

Addition energy

The electrochemical potential of the quantum dot is therefore defined as the energy required to add one additional electron and is expressed by

$$\mu(N) = E(N) - E(N-1). \tag{3.10}$$

In the framework of the constant interaction model, Equation 3.10 becomes

$$\mu(N) = \sum_{n=1}^{N} E_n + \left(N - \frac{1}{2}\right) E_C - e \sum_i \alpha_i V_i. \tag{3.11}$$

Therefore, the electrostatic potential difference between consecutive dot energy levels $\Delta\mu(N)$ equals to the addition energy required to add a single electron into the quantum dot. For fixed voltages applied to the gates and contacts of the system, $\Delta\mu(N)$ is given by the relation

$$\begin{aligned} \Delta\mu(N) = \mu(N) - \mu(N-1) &= E_N - E_{N\text{-}1} + E_C \\ &= E_C + E_n, \end{aligned} \tag{3.12}$$

As illustrated in Figure 3.3, when a single μ_N level lies within the source-drain bias window defined by the difference $\mu_S - \mu_D$, single electron transport occurs with typical Coulomb peaks.

3.1.6 Coulomb blockade diamonds

As illustrated in Figure 3.4, the measurement of the current I or conductance G as a function of both the V_{ds} and V_{G} biases allows to obtain the diagram of bias spectroscopy or Coulomb blockade spectroscopy as it is also called. The resulting stability diagram demonstrates diamond-shaped regions (shown in shaded blue), inside of which the transport through the quantum dot is blocked due to the Coulomb blockade effect, and the nano-island is occupied by a constant number N of electrons. Whenever the dot energy levels μ_{N} fall within the bias window defined by the source and drain electrochemical potentials difference,μ_{S} and μ_{D} respectively, the number of electrons populating the quantum dot is modified, and conductance or current peaks are observed. The height of a single Coulomb diamond equals the charging energy E_{C}.

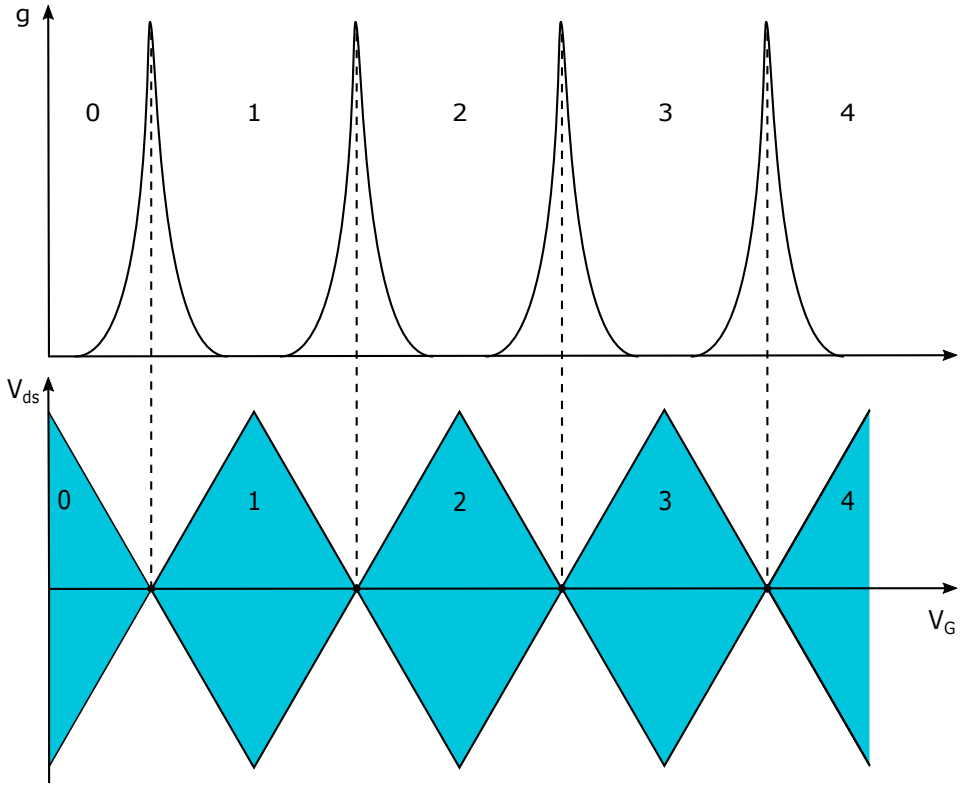

Figure 3.4 – Coulomb blockade diamonds. The transport is blocked inside the diamond-shaped areas depicted in shaded blue. In these areas, the number of electrons N populating the quantum dot is constant. At constant V_{ds} bias, following a linecut along the V_{G}-axis Coulomb peaks are demonstrated occurring in the conductance at the points where the electron dot occupancy change. In this particular example, this happens at the degeneracy points where adjacent Coulomb diamonds touch (depicted with black dots).

In Figure 3.5, an example of electron transport through a single quantum dot system is presented, demonstrating the Coulomb blockade regime. In this particular example, the occupancy of the dot remains stable at a single loaded electron, and electronic transport through the system is blocked. A schematic of the energy diagram of the system, consisting of the dot connected to the source and drain electron reservoirs, is also depicted on the side,

corresponding to different areas of the Coulomb diamond. There are four cases identified here. Case (i) corresponds to the degeneracy point where two adjacent diamonds touch,

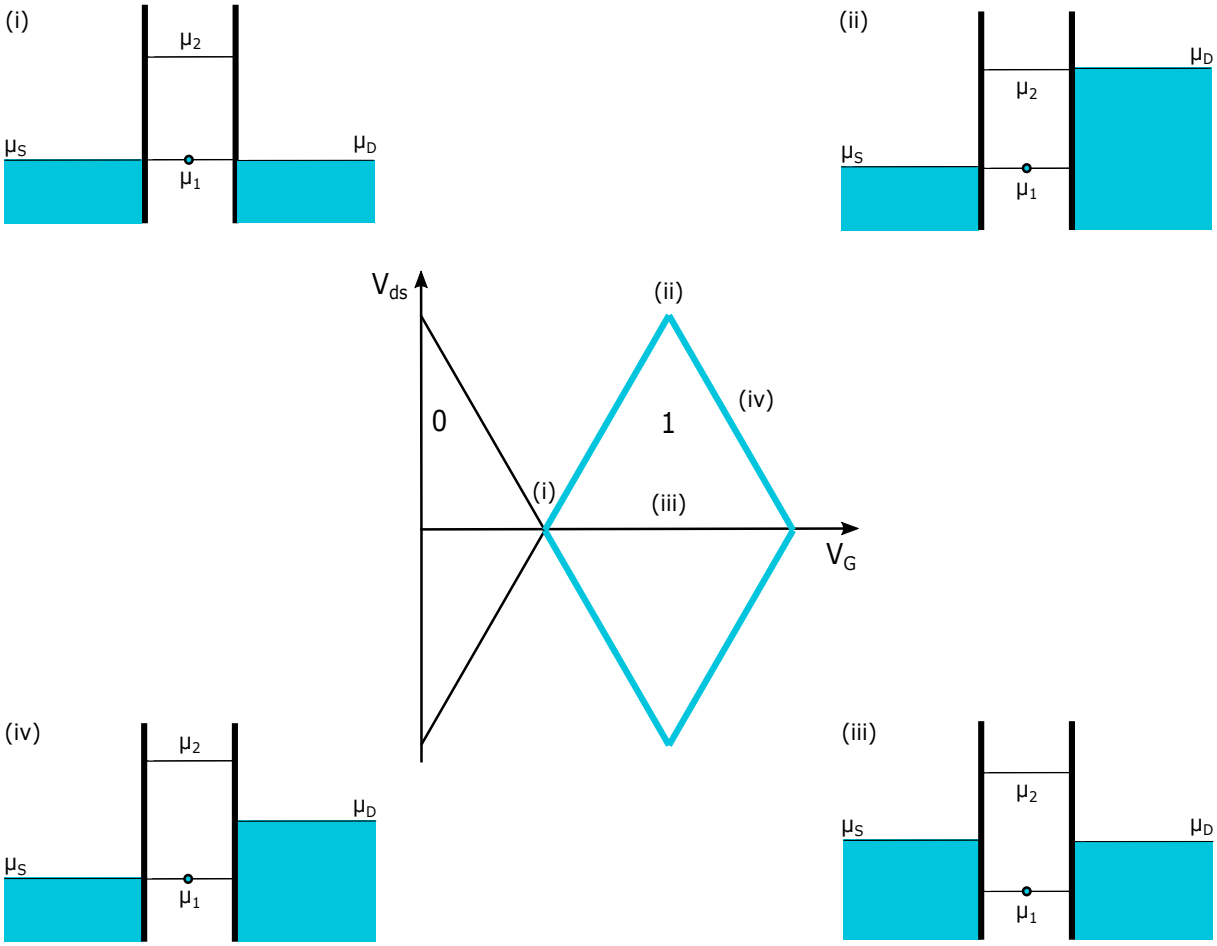

Figure 3.5 – The diamond-shaped regions correspond to different charge states of the quantum dot system. The energy diagram of the dot coupled to the source and drain reservoirs is illustrated at various key areas of the diamond on the side of the diagram. Electronic transport is blocked in each case identified here, and the number of electrons inside the blue shaded diamond remains stable and equal to one. (i) Degeneracy point between two adjacent diamonds. The electrochemical potential of the quantum dot, μ_1, is aligned with the electrochemical potentials of the source and drain reservoirs, μ_S and μ_D respectively. (ii) Top of the diamond. The quantum dot level μ_1 is aligned with the electrochemical potential of the source μ_S while the level μ_2 is aligned with the potential of the drain μ_D. (iii) Center of the diamond. The electrochemical potentials of the source and drain reservoirs μ_S and μ_D are aligned with each other and lie between the dot levels μ_1 and μ_2. (iv) Middle of one of the edges of the diamond. The electrochemical potential of the drain μ_D is aligned with the dot level μ_1.

and the electrochemical potential of the dot μ_1 is aligned with the potentials of the source and drain reservoirs μ_S and μ_D. Case (ii) corresponds to the top of the diamond depicted in shaded blue, and the dot level μ_1 is aligned with the potential of the source reservoir μ_S, whereas the dot level μ_2 is aligned with the potential of the drain reservoir μ_D. Case (iii)

corresponds to the region at the center of the diamond, and the electrochemical potentials of the source and drain reservoirs μ_S and μ_D are aligned with each other and lie in the middle of the distance separating the dot levels μ_1 and μ_2, with μ_2 being unoccupied. Case (iv) corresponds to the middle of one of the diamond edges, and the electrochemical potential of the dot μ_1 is aligned with the potential of the drain reservoir μ_D, while the electrochemical potential of the dot μ_1 is aligned with the potential of the source μ_S lies in the middle of the distance separating the dot levels μ_1 and μ_2.

3.1.7 Sequential tunneling transport

By applying the appropriate source-drain voltage difference, the electrochemical potentials in the leads are adjusted and the current flowing through the system can be derived. Although in theoretical studies, symmetrical biasing conditions are typically assumed, in experimental measurements, it is more usual for the Vds bias to be fully applied to the source electrode while the drain is connected to the ground, or the inverse. In this section, the theoretical background for the many-body and out-of-equilibrium statistical physics of transport in a quantum dot system is provided and the equations that are solved in the remainder of this thesis to calculate properties of the current flowing through the simulated quantum dots are described.

Considering that the quantum dot is coupled to the source and drain reservoirs, at zero magnetic field, the system is described by the Hamiltonian

$$H = H_{\text{dot}} + H_{\text{r}} + H_{\text{c}}, \tag{3.13}$$

where H_{dot} the Hamiltonian describing the quantum dot, H_r both the source and drain reservoirs, H_c the coupling between the dot and the reservoirs. In second quantization, these Hamiltonians are given by [177]

$$H_{\text{dot}} = \sum_{i\sigma} \epsilon_{i\sigma} c^+_{i\sigma} c_{i\sigma} + \frac{1}{2} \sum_{ijkl,\sigma\sigma'} V_{ijlk} c^+_{i\sigma} c^+_{j\sigma'} c_{k\sigma'} c_{l\sigma}, \tag{3.14}$$

$$H_{\text{r}} = \sum_{\boldsymbol{k}L\sigma} \epsilon_{\boldsymbol{k}L} c^+_{\boldsymbol{k}L} c_{\boldsymbol{k}L}, \tag{3.15}$$

$$H_{\text{c}} = \sum_{k,q} \left(t_{\boldsymbol{k}L,i\sigma} c^+_{\boldsymbol{k}L} c_{i\sigma} + t^*_{\boldsymbol{k}L,i\sigma} c_{\boldsymbol{k}L} c^+_{i\sigma} \right). \tag{3.16}$$

In the above equations, the operator c_α is used to describe the desctruction of an electron in the state α, which is a collective index that simultaneously labels all degress of freedom of an electron in the quantum dot or in one of the reservoirs. In the case of the quantum dot, these degrees of freedom are single-electron orbital and spin indices: $\alpha \to i\sigma$. In the case of the reservoirs, these degrees of freedom are the wavevector $\boldsymbol{k}$ and the index L which stands for "lead" (either S for the source or D for the drain): $\alpha \to \boldsymbol{k}L$.

Moreover, $\epsilon_{\boldsymbol{k}L}$ is the energy of a reservoir electron eigenstate labeled by $\boldsymbol{k}L$ and $t_{\boldsymbol{k}L,i\sigma}$ which represents the tunneling matrix element between $i\sigma$ and $\boldsymbol{k}L$, the single-electron

eigenstates of the quantum dot and lead L respectively, defined by the properties of the barriers, such as thickness, etc. Finally, $\epsilon_{i\sigma}$ stands for the single-electron energy, and V_{ijlk} for the matrix elements of the Coulomb interaction given by

$$V_{ijlk} = \int d\boldsymbol{r}_1 \int d\boldsymbol{r}_2 F_i^*(\boldsymbol{r}_1) F_j^*(\boldsymbol{r}_2) \frac{q^2}{4\pi\epsilon|\boldsymbol{r}_1 - \boldsymbol{r}_2|} F_k(\boldsymbol{r}_1) F_l(\boldsymbol{r}_1), \tag{3.17}$$

where integration is realized over all space and $F_i(\boldsymbol{r})$ represents the i-th single-electron wavefunction. More specifically, $\epsilon_{i\sigma}$ and $F_i(\boldsymbol{r})$ are the eigenenergies and eigenfunctions, i.e. envelope functions, resulting from the single-electron effective Schrödinger's equation given by

$$V(\boldsymbol{r})\psi(\boldsymbol{r}) - \frac{\hbar^2}{2}\nabla \cdot [M_{\mathrm{e}}^{(-1)} \cdot \nabla\psi(\boldsymbol{r})] = E\psi(\boldsymbol{r}), \tag{3.18}$$

where $V(\boldsymbol{r})$ is the electron confinement potential and $\boldsymbol{M}_{\mathrm{e}}^{-1}$ is the inverse effective mass tensor.

From the master equation, transport through the quantum dot is described by [177]

$$\frac{dp_{\mathrm{m}}}{dt} = -p_{\mathrm{m}} \sum_{n \neq m} \gamma_{\mathrm{nm}} + \sum_{n \neq m} p_{\mathrm{n}} \gamma_{\mathrm{nm}} = 0, \tag{3.19}$$

$$\gamma_{\mathrm{nm}} = \Gamma^{\mathrm{S}}(n \to m) + \Gamma^{\mathrm{D}}(n \to m), \tag{3.20}$$

where n and m are indices that span all the many-body eigenstates α_{N} of H_{dot}. Within the first order approach described above, the tunneling rate $\Gamma^{\mathrm{L}}(n \to m) \neq 0$, if and only if n and m are within subspaces that differ by one electron. In the approach described here, the non-equilibrium statistics of the quantum dot is captured by the occupancy probabilities p_{m}, i.e. the probability of finding the system in the charge state m. Assuming steady state behavior, the time derivative of each p_{m} is set to zero in the master equation (second equality in Equation 3.19), which then reduces to a system of linear equations. The expression of the current arising from electrons entering the quantum dot from the source can be written in terms of the total tunneling rates as

$$I^{\mathrm{S}} = -e \sum_{\alpha\beta} p_\alpha [\Gamma^{\mathrm{S}}(\alpha_{\mathrm{N}} \to \beta_{\mathrm{N+1}}) - \Gamma^{\mathrm{S}}(\alpha_{\mathrm{N}} \to \beta_{\mathrm{N\text{-}1}})]. \tag{3.21}$$

Due to charge conservation, $I^{\mathrm{S}} + I^{\mathrm{D}} = 0$, where I^{D} is the current arising from electrons entering the quantum dot from the drain reservoir.

3.2 Experimental aspects

In the first part of this section, the cryogenic systems used to cool down the samples are presented. Then, the measurement circuits are detailed, along with the wiring of the refrigerator used to connect the samples to room-temperature electronics, and the associated instrumentation. Finally, the methodology employed to investigate the proper performance of the fabricated devices and to identify a functional device is explained.

3.2.1 Cryogenic measurement systems

As the study of the behavior of electrostatically defined quantum dots needs to be carried out at cryogenic temperatures, the individual components and the entire experimental setup were chosen to be functional at very low temperatures. More specifically, for the realization of the experiments that are discussed in the following chapters, mainly two measurement systems were used in order to attain the cryogenic temperatures required for the accurate study of quantum dots, i.e. a top-loading Variable Temperature Insert (VTI) cryogenic system and a high-vacuum cryogenic probing system.

High-vacuum cryogenic probing system

For the initial tests performed on the quantum dot devices at room and low temperatures, the 4.2 K base temperature cryogenic probe station CPX-VF manufactured by Lakeshore Cryotronics Inc. was used. The samples were mounted onto the grounded metallic plate and silver conductive adhesive paste was chosen to glue them permitting for thermal and electrical connection to the sample holder.

In Figure 3.6 (a), a simplified schematic representation of the probing system is shown illustrating an overall view of the main components of the probing system. The system was installed onto a vibration isolation system, i.e. a floating table whose top is free to move both vertically and horizontally thanks to a continuous flow of compressed air (Model TMC CleanBench Lab Table 63-500). Moreover, a turbo vacuum pumping system (Model Agilent TPS-compact) permits to carry out the experiments in a 10^{-6} Torr vacuum environment providing the required thermal insulation for the cryogenic refrigeration system and eliminating the possibility of sample contamination. Also, a light source (Model Techniquip 21AC illuminator) and a microscope system (Model Qioptiq Optem Fusion) make possible monitoring the samples located on the sample stage throughout the whole experimental process using a computer monitor.

In Figure 3.6 (c), a general outlook of the major components of the refrigerating system is presented. Depending on the demands of the experiment, one or even a few samples were characterized per day. Their cooldown to 4.2 K was accomplished via a liquid-helium continuous flow from a storage dewar into the probing system through a transfer line with a flow rate which was controlled by the dewar head valve and the probe station needle valve. In addition, the sample stage was protected from heating effects due to radiation from warmer stages by the radiation and second shields. A full thermal cycle was completed in a few hours and co-integrated temperature controllers (Model 336) permitted to obtain control over the temperature of the sample, magnet, radiation shield, and second shield stages. Furthermore, the probing system was equipped with a superconducting coil which can be used to apply magnetic fields up to 8 T perpendicular to the sample orientation.

Moreover, the probing system was equipped with six probes in total which can be used for signals ranging from DC to microwave. In order to secure the sample from any additional heating effects due to radiation or heat conduction from the warmer probes, the probe tips were thermally anchored to the cold stages while the probe arms were

equipped with radiation shields. During the measurements, standard ZN50R BeCu and W DC probes with a 25 µm or 10 µm tip radius were used to electrically connect the room temperature measurement equipment to the samples. The contact resistance of the probes was 0.96 Ω, 0.7 Ω, and 0.6 Ω in the case of 25 µm BeCu, 25 µm W, and 10 µm BeCu probe tips respectively, taking into account both the probe contact and the arm resistance (0.5-0.7 Ω approximately).

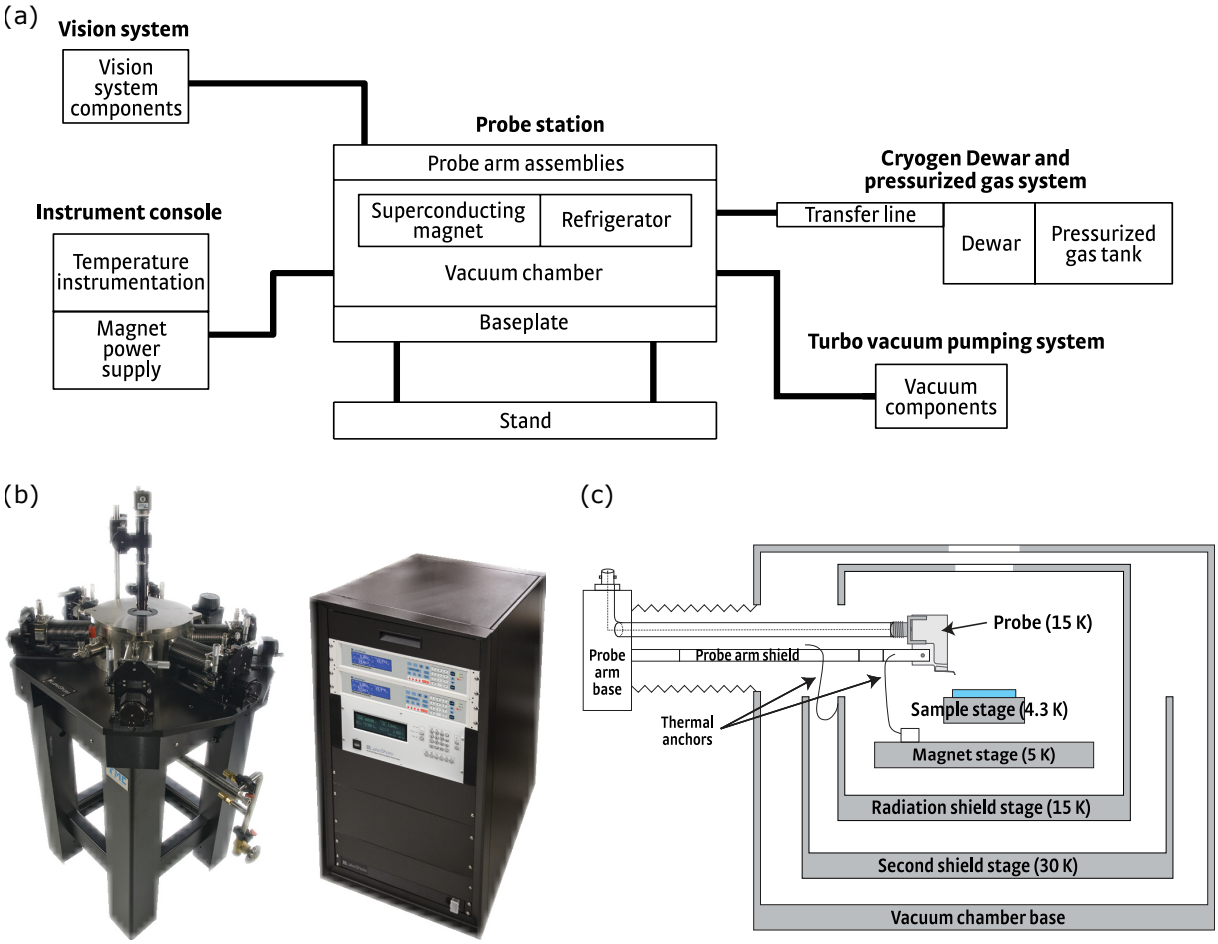

Figure 3.6 – High-vacuum cryogenic probing system. Image adapted and taken from the official website of Lakeshore Cryotronics Inc. (a) Main components of the probe station. (b) Probing system used for sample characterization at room and low temperatures. (c) Main structure of the cryogenic refrigeration system.

Variable Temperature Insert cryogenic system

Despite the fact that the vast majority of high precision studies carried out on qubit systems in academic research laboratories is realized at a temperature of approximately 10 mK achieved usually using a dilution refrigerator, the VTI cryostat was selected for the characterization of the quantum dot devices of this work thanks to its short turnaround time, comparing to other deep cryogenic alternative solutions. In fact, a VTI full thermal cycle is performed in a few hours, which is significantly shorter than the 24-48 hours cycle

of the dilution refrigerator. As the purpose of this work was to explore the capability of this standard-process technology platform to provide gate-defined quantum dots, the interest was focused on the characterization of a maximum possible number of samples, and not on the observation of certain quantum effects with high precision which requires deep cryogenic temperatures.

The VTI cryostat (Model 8TM-SVM-35-SMAG) manufactured by Janis Research Co. that was used, can achieve a base temperature of approximately 1.4 K. One single sample could be loaded onto the system at once, and a full thermal cycle was completed in a few hours. More precisely, the cryostat was used either to realize measurements at fixed temperatures or to perform thermal cycles on the same measured sample between 1.4 K and 300 K, characterized by an uncertainty of a few millikelvin at the lowest temperatures, and of a few kelvins at the highest, with a regulated step thanks to a temperature controller (Model Lakeshore 336). In addition, the cryostat was equipped with a superconducting coil (Model 80-400-010L) able to generate magnetic fields up to 8 T.

In Figure 3.7, a schematic cross-section of the VTI cryostat is shown consisting of two coaxial reservoirs filled with liquid nitrogen, and liquid helium respectively, separated by an intermediate vacuum region permitting to eliminate the conductive heat load due to any gases. More precisely, the helium reservoir was surrounded by the nitrogen reservoir allowing to reduce any thermal load into the first caused by radiations. Also, additional radiation shields help reducing the radiational heat load into the helium reservoir. Moreover, the space surrounding the cryogenic reservoirs was evacuated using the evacuation valve, which served also as a safety pressure relief valve in case of an internal leak incident.

The refrigeration system of the VTI was based on an exchange gas mechanism with the measured sample located inside a column of exchange gas. More precisely, the sample was fixed to the lowest end of the sample positioner which was inserted into the sample tube located in the center of the system. The latter was enclosed inside a vacuum isolation tube permitting to reduce any heat load from the outer parts of the cryostat. Liquid helium was drawn from the reservoir and was channeled to the sample tube through a vaporizer located at the bottom of the sample tube. The flow was regulated by the needle valve. Then, the liquid helium was evaporated to a sub-atmospheric pressure using a pumping station (Model 15RVP), leading to an additional cooling of the sample tube down to 1.4 K approximately. In addition, a temperature sensor placed close to the sample permitted to extract the sample temperature. Last, control over the temperature in the inner tube was obtained using heaters located both at the bottom of the sample tube and on the probe, just above the sample.

3.2.2 Measurement circuits

In this section, each of the experimental setups used both for the electrical characterization of the samples and Coulomb blockade spectroscopy measurements, discussed in the following chapters, is presented along with the instrumentation used during the experimental procedures.

Protection from ESD

Protection from ESD events was one of the biggest challenges of this work. The chips containing the samples were stored in a box filled with anti-static foam during transfer, whereas the packaged chips were enclosed into an electrostatic dissipative plastic container. In order to minimize the risks of any occurring ESD events that could eventually cause significant damage to the structures in a non-reversible way, several precautions were considered, such as grounding oneself during sample handling with wrist and ankle bracelets. In general, safe manipulation of the samples requires always careful preparation and much attention.

Due to the ESD risks involved during wire-bonding of the samples, the procedure was optimized by being entirely performed at STMicroelectronics using industry-standard techniques. In this context, the dies were wire-bonded to their package with gold wires disposing a diameter of a few micrometers. Attentive and optimal selection of the dimensions and location of the device bonding pads was executed, permitting to avoid passing wires over others, and to control their curvature and proper orientation. Furthermore, the aforementioned solderless connection method, i.e. the interposer based on the principle of direct contact, used to connect the samples to their measurement setup, allowed to completely avoid wire-bonding in the laboratory environment.

Last, the sample holder was grounded so that each new connection was automatically grounded. In general, each component of the experimental setup was carefully grounded with respect to the ground of the building eliminating the appearance of ground loops. In addition, before connection to the sample, every part of the measurement setup was examined very carefully using an electrometer allowing to measure static electricity. In case of high measured static electricity, the inspection of the grounding of the setup and its individual components was repeated, until an acceptable measurement was observed.

Lock-in amplifier measurements

A widely used technique to maximize the signal-to-noise ratio is the application of a small AC signal of a given frequency to an ohmic contact or gate using a synchronous detection amplifier or, as it is also called, a lock-in amplifier. Based on a homodyne detection scheme and low-pass filtering, the response of the device is then measured, with respect to a periodic signal reference with the same frequency, thus eliminating the noise contributions of the other frequencies. In short, the lock-in measurement reads signals in a defined frequency band around the frequency of the reference signal, and rejects the rest.

An optimization process is first performed permitting to properly select the reference frequency and amplitude producing the less noisy signal. The frequency is chosen to be compatible with the phenomenon to be observed, to avoid sources of major noise, e.g. harmonics of 60 Hz[4], and to minimize the signal-to-noise ratio. In brief, a higher

[4]In the U.S., Canada, and other countries where a standard line voltage is of 110-120 V, the frequency standard is 60 Hz, leading to severe and undesired 60 Hz interference on electrical signals. Source: https:

frequency is preferred as it allows for measurement averaging over a large number of cycles in less integration time. The amplitude of the excitation signal is chosen large enough to maximize the signal, and its exact value depends on the phenomena under examination.

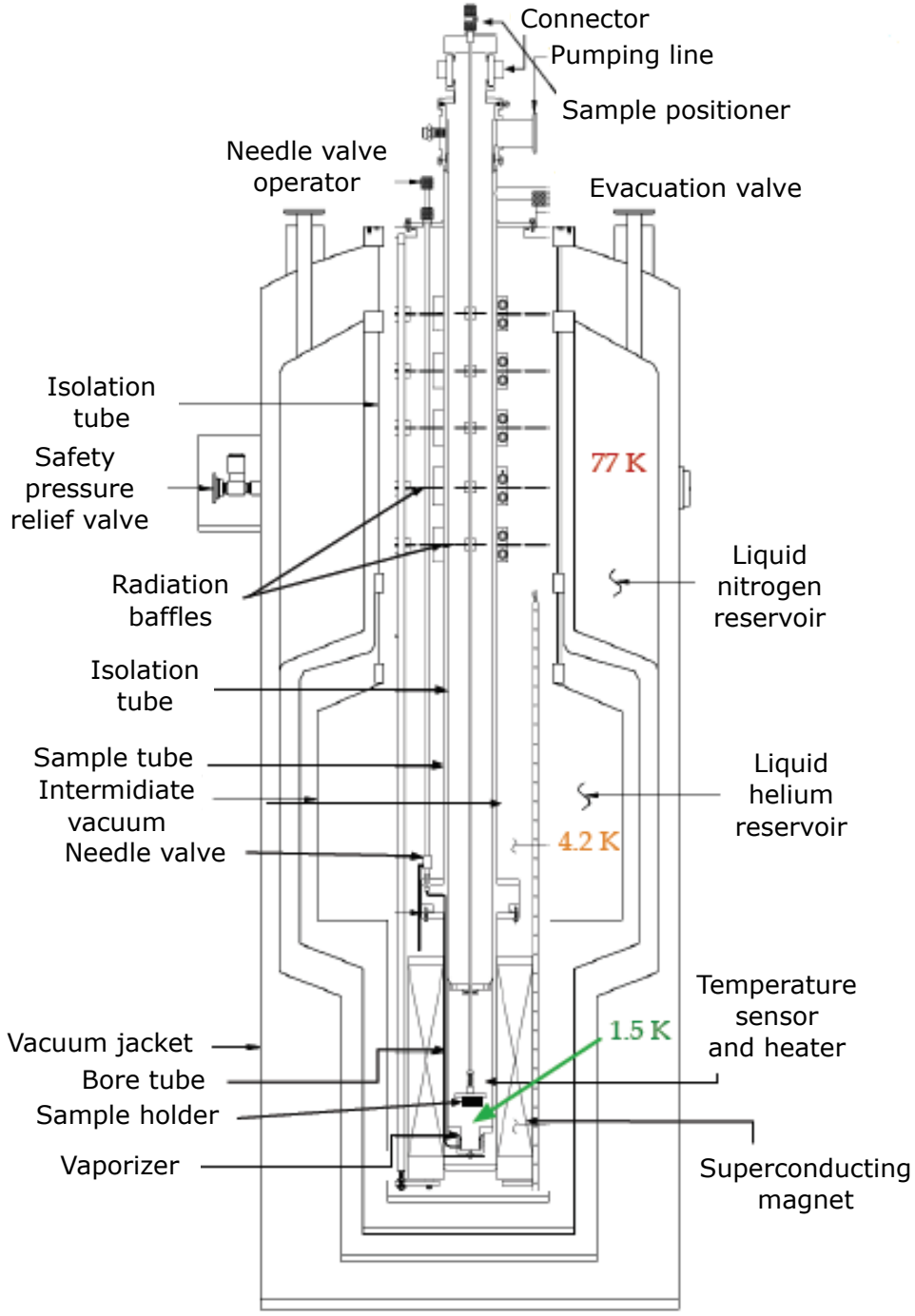

Figure 3.7 – Cross-section schematic of the VTI cryostat manufactured by Janis Research Co. Figure adapted from [96, 98].

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Experimental setup

In order to characterize the quantum dot devices presented in the remainder of the thesis, DC transport and differential conductance measurements were performed for initial characterization and Coulomb blockade spectroscopy, respectively. To this end, the measurement equipement included a lock-in amplifier, a Source-Measurement Unit (SMU), and a bias-DAC. In the remainder of this subsection, each experimental setup used is discussed.

The VTI cryostat was used to cool the packaged chips down to 1.4 K, while a DC-line probe was used to electrically connect the base-temperature sample to the room-temperature instruments. Signal filtering is provided by the coaxial cables and junction boxes, including Π filters. Every chip contained a single quantum dot device wire-bonded to the package (Figure 3.8 (a)). In Figure 3.8 (b), one of the packaged sample is connected to the PCB containing the interposer. Next, as depicted in Figure 3.8 (c), the PCB is mounted onto the VTI probe.

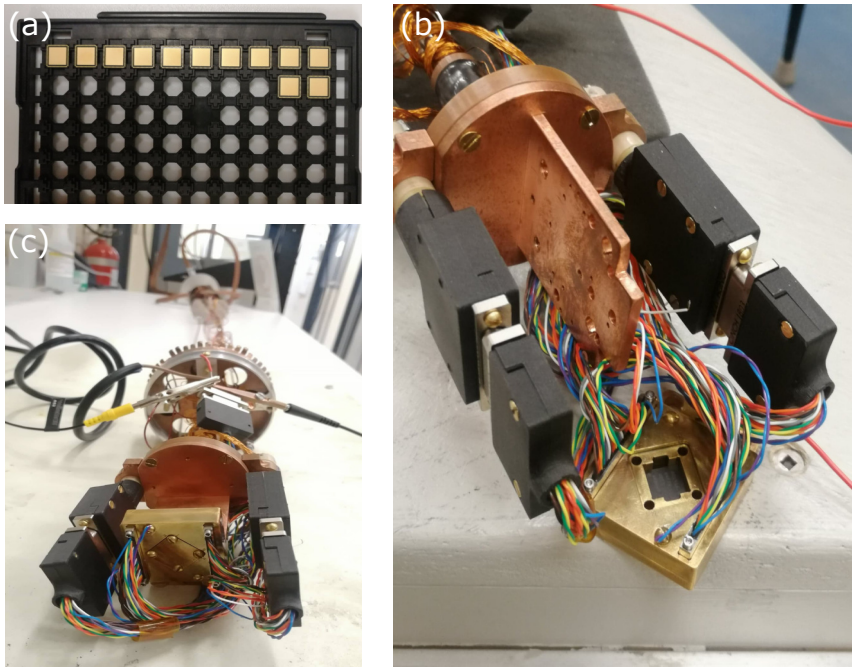


Figure 3.8 – (a) Packaged quantum dot dies enclosed into an electrostatic dissipative plastic container used for sample transportation and storage. (b) Packaged quantum dot sample placed onto the interposer-based PCB which is connected to the VTI measurement probe. (c) The interposer-PCB system containing the quantum dot sample is tightly closed and mounted onto the VTI measurement probe.

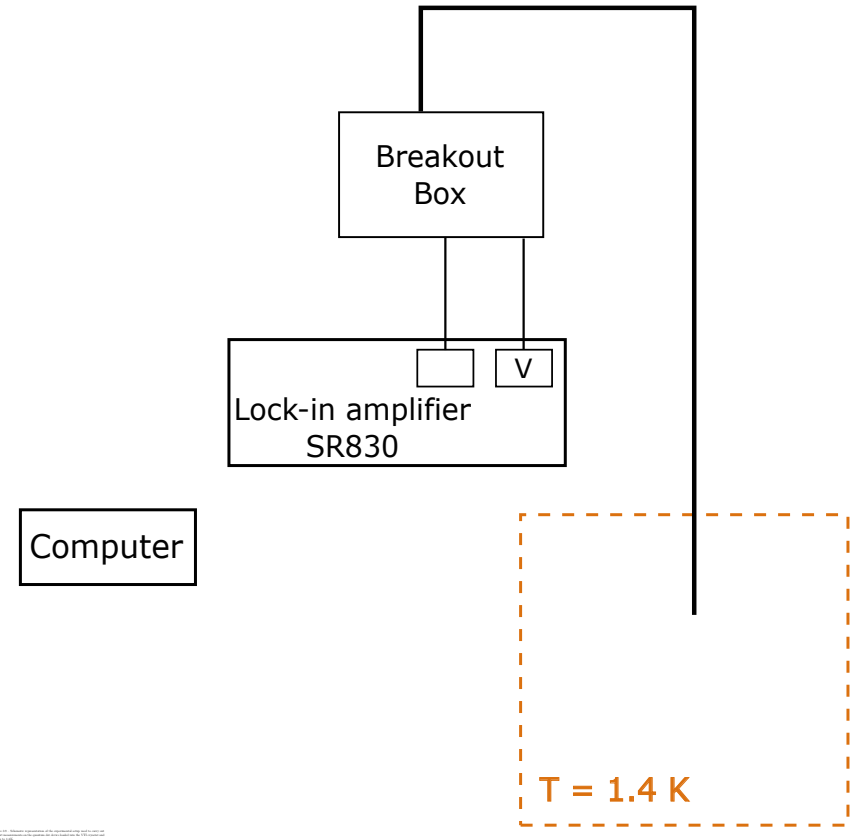
DC transport measurements

During the preliminary measurements, such as continuity and leakage current measurements, voltage signals are applied and read using separate channels of an SMU, which allow a signal to be applied and read on the same terminal (Model E5270B by Agilent

Technologies). In Figure 3.9, the complete measurement circuit used to carry out DC transport measurements is depicted. The application and read-out of voltage signals on the various gates and contacts of the device was achieved using the separate channels of either the aforementioned SMU or the synchronous amplifier (Model SR830 by Stanford Research Systems). In case that more SMU channels were needed, a supplementary unit (Model Keithley 2400 from Tektronix Inc.) was used.

Coulomb blockade spectroscopy

In Figure 3.10, a complete schematic of the measurement circuit used for the realization of the Coulomb blockade spectroscopy is illustrated. The experimental setup consisted of a VI-IV Bias-DAC, and a lock-in amplifier (Model SR830). Various voltage sources of the bias DAC were used to apply independent DC voltage signals to the ohmic contacts and gates controlling the electrostatic formation of the electron reservoirs and the quantum dot.



voltage sources. In parallel, the AC part v_{ds} is applied to the source using a lock-in amplifier with a reference signal of a 17.7 Hz frequency. In the end, a bias-tee is used to combine these two signals. The application of V_{ds} induces the DC current I_{ds} in the device, while the application of v_{ds} gives rise to the AC current i_{ds}. The differential conductance, or transconductance, is the derivative of the current flowing through the channel as a function of the bias voltage, and is given by

$$g = \frac{\partial I_{ds}}{\partial V_{ds}} \simeq \frac{i_{ds}}{v_{ds}}, \tag{3.22}$$

as the signal v_{ds} is small comparing to V_{ds}. Differential conductance measurements carried out on the samples allow to better visualize the excitation levels of the system, comparing to electronic transport measurements [169, 178]. Finally, the same lock-in amplifier is used to read the output voltage at the drain, allowing to measure the output differential conductance g.

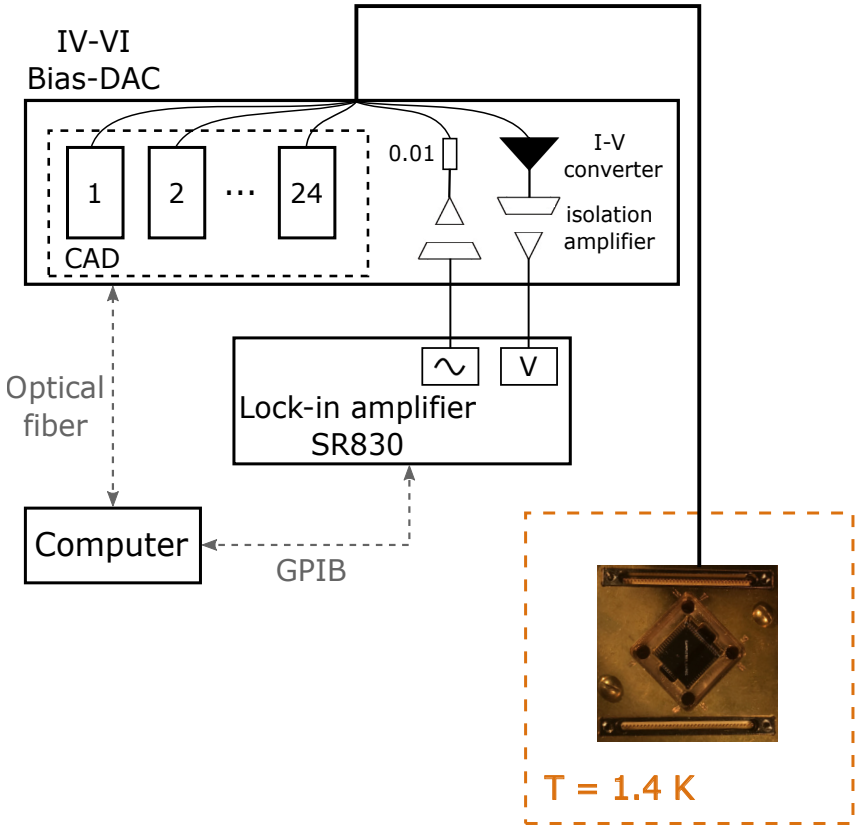


Figure 3.10 – Schematic representation of the measurement circuit used to characterize the quantum dot device at 1.4 K by performing Coulomb blockade spectroscopy measurements.

The transport of electrons between the dot and the regions of the source and drain can be experimentally measured and gives a valuable insight on the occupancy conditions in the dot. The voltages applied on the gate electrodes are the main variables allowing to control the charge configuration in the quantum dot. Each gate is distinctly coupled to the quantum dot, and this coupling can vary depending on the overall state of the device.

In order to measure transport through a quantum dot system, the formation of tunnel barriers opaque enough to form the dot is required, yet low enough to allow transport to be measured experimentally through the device. This condition can be achieved by using gate electrodes to tune the potential barriers. Then, the coupling of each gate is parameterized by the capacitance C_i or more conveniently by the lever arm α_i. Finally, Coulomb blockade spectroscopy performed by measuring the conductance or current through the system versus the source-drain bias and the voltage applied on the gate controlling the dot occupancy gives rise to Coulomb diamonds, from the shape and size of which the properties of the dot can be precised. Examples of measured Coulomb diamonds are shown in Figure 3.11.

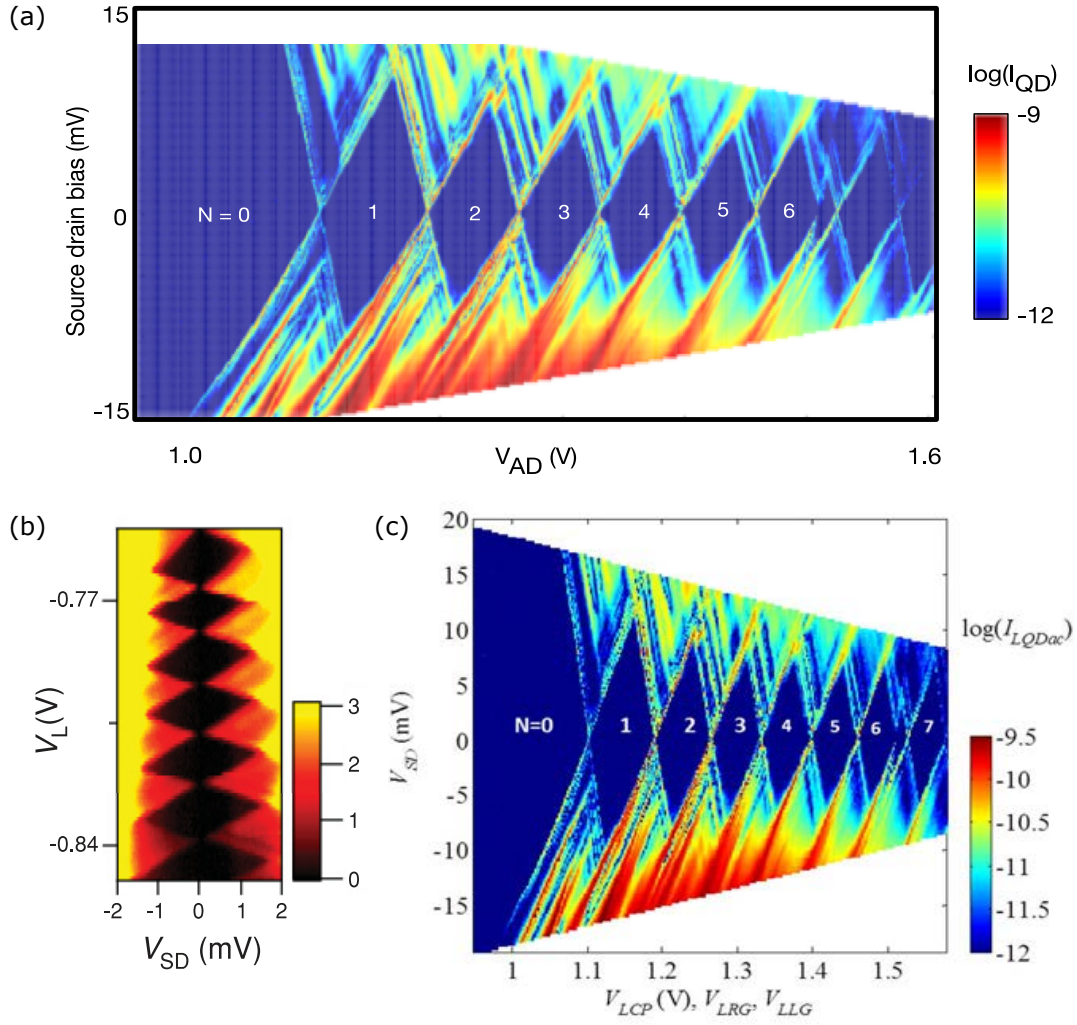


Figure 3.11 – (a) Experimental demonstration of Coulomb diamonds in a MOS quantum dot in the few-electron regime. Image taken from [179]. (b) Coulomb diamond measurement through a single quantum dot in the many-electron regime formed in a Si/SiGe heterostructure. Image taken from [180]. (c) Measured Coulomb diamonds demonstrated in a MOS single quantum dot in the few-electron regime. Image taken from [181].

3.2.3 Device investigation methodology

In the course of this thesis, a protocol was developed summarizing the initial characterization steps performed on the quantum dot device, intended to verify the proper functionality of the device. More precisely, the purpose of these tests is to accomplish a first exploration of the samples and to verify their proper operation before carrying out more elaborate experiments, e.g. Coulomb blockade spectroscopy. A brief outline of this characterization method is presented in Table 3.1. The first step involves the execution of continuity and leakage current tests on every gate and ohmic contact of the device. As a next step, the drain, source, top, and back gate are polarized appropriately, and the current flowing through the channel is measured. Their proper operation is investigated verifying that the key characteristics describing the 28 nm FD-SOI technology node are observed. In this section, the individual initial characterization steps are detailed one by one.

	Characterization steps
1	Continuity and leakage current tests
2	Channel activation using the top gate
3	Channel activation using the back gate
4	Channel activation using both the back and top gate

Table 3.1 – Outline of the characterization methods allowing to evaluate the technology and to investigate the behavior of the fabricated quantum dot devices

Continuity and leakage current test

The first step of the sample evaluation method involves the examination of the presence or absence of leakage current between the ohmic contacts, gates, and conduction channels. These leakage currents appear usually due to material defects, device architecture failure during fabrication or wire-bonding deficiencies and can eventually limit the performance of the device or even serious and irreversible device damage. Therefore, this is a critical step permitting to evaluate the design and fabrication efficiency of the structure. The measurements are initially executed at room temperature, and are repeated when the sample is cooled down. Actually, several of these leakage currents are temperature-dependent and a cryogenic system is thus used to determine the origin of these currents, if any observed.

Therefore, a voltage sweep is performed from $-10\,\mathrm{mV}$ to $10\,\mathrm{mV}$ on a specific gate or contact with a step of $1\,\mathrm{mV}$ or smaller, with the rest of the device grounded. A compliance current of $10\,\mathrm{nA}$ is applied throughout the measurement ensuring that the resulting current cannot cause any damage on the structure. The current flowing through the silicon channel is measured, and the corresponding resistance is extracted with respect to the ground. The process is repeated for every gate or contact. The value of the measured resistance provides a valuable insight concerning the nature of the leakage. Indeed, it permits to identify between which device elements the leakage current occurs, and at which level exactly, i.e. at the level of the structure, wires used for wire-bonding, or interposer.

Depending on the device, experimental setup, and temperature of the measurement, a measured resistance between 50 and 100 kΩ corresponds to a small leakage current under the acceptable limit. Otherwise, a resistance in the order of a few kilo-ohms or less indicates that the leakage can be harmful to the device. In the case of a detected leakage current above the tolerable limit, the measurement is repeated with the adjacent contacts or gates floating, in an attempt to identify its origin. For the technology used for the fabrication of the devices presented in this thesis, the value of 100 pA/μm^2 is the average leakage current in a device occurring at room temperature [182]. It is noted that given the temperature dependence of these currents, a measured leakage current above the acceptable limit at room temperature might become minor at cryogenic temperatures. Moreover, an unexpected short circuit or leak is not always an issue. For instance, In case that this leak is identified towards another gate or contact that can be set to float without endangering the device operation.

Channel activation using the top gate

Once a potentially functional device is identified, the verification test focus next on the activation of the conduction channel via the top gate, aiming to verify the proper performance of the source, drain, and gate. This characterization is initially executed at room temperature and is repeated when the sample is at base temperature.

Therefore, a DC voltage signal, e.g. 100 mV, is applied to the source, while the drain is grounded. The back gate is also grounded. A voltage sweep is performed on the top gate, respecting the supply voltage range specified by the technology design rules, namely from 0 V to 1.8 V, with a step of a few millivolts. The current flowing through the channel is measured and the value of the threshold voltage V_{th} of the device is extracted. The typical transistor characteristic I-V curve is plotted. In the case of the technology option used in this study, the V_{th} value is approximately 700 mV at room temperature [182].

Channel activation using the back gate

The process is then repeated with the back gate activated this time, at room and base temperature. Therefore, a DC voltage signal, e.g. 100 mV, is applied to the source, with the drain grounded. For a grounded top gate, the voltage applied to the back gate is ranged from 0 V to 8 V with a step of a few millivolts. The current flowing through the silicon channel is measured and the value of the threshold voltage of the device is extracted. For the technology used here, this is not a common device operation, as the back gate is polarized usually in combination with the top gate.

Channel activation using the back and top gate

A combination of the two previous characterization processes is performed to activate the silicon channel. Therefore, a DC voltage signal, e.g. 100 mV, is applied on the source, with the drain grounded. For different top gate voltage values, the voltage applied to the

back gate is ranged from 0 V to 8 V with a step of a few millivolts. The current flowing through the device is measured, permitiing to extract the value of the threshold voltage. Depending on the technology options and the back gate bias, the latter is expected to vary by several tens or a few hundreds of millivolts at room temperature [182].

Hall effect measurements at cryogenic temperatures

4

Contents

The characterization of carrier density and mobility plays a crucial role in the development of high quality quantum dot devices and the improvement of design models for quantum computing applications [183, 184]. The Hall effect is a widely used method for material characterization [185, 186, 187] and for defining key semiconductor parameters such as the aforementioned quantities, which can provide valuable feedback to quantum dot integration [188, 189]. In this chapter, the results of this work are presented on the investigation of the Hall effect, demonstrated in industry-standard process 28 nm FD-SOI microstructures. The Hall effect is measured at cryogenic temperatures aiming to evaluate the 28 nm FD-SOI technology in terms of versatility and utility for quantum dot applications. In the first section, the geometry of the devices is explained. In the second section, the measurement circuit is detailed, along with the experimental methods that allowed to extract the electron density and mobility of the structures. In the third section, the experimental results and following analysis are discussed.

It is worth noting that, although several existing studies have investigated the behavior and performance of FD-SOI Hall sensors [190, 191, 192, 193, 194, 195] and the definition of low-temperature carrier densities and mobilities in FD-SOI devices [196, 197, 198], to date and to the best of the author's knowledge, this study presents for the first time experimental data collected from the characterization of 28 nm FD-SOI microstructures with Hall effect measurement methods at 4.2 K.

4.1 Background

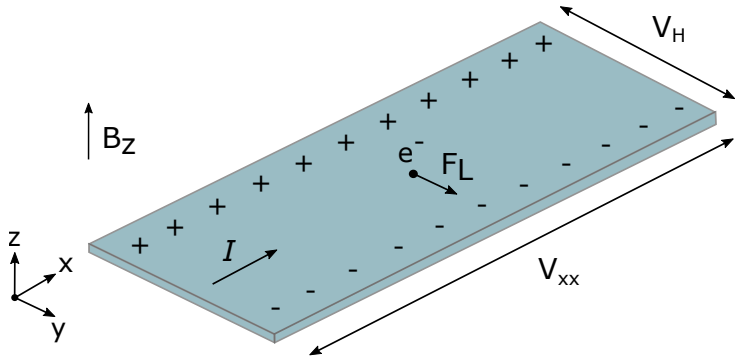


Figure 4.1 – Manifestation of the Hall effect in a bar-shaped n-type semiconducting structure. A constant current I flows through the device in the x-direction. In the presence of an external magnetic field B_z, the Lorentz force F_L forces the moving electrons to migrate to one side of the structure. The resulting voltage difference is known as the Hall voltage.

A bar-shaped structure is used to study the Hall effect, also referred to as Hall bar for short (Figure 4.1) [199, 200, 201]. In such an n-type semiconducting structure, the majority carriers are electrons characterized by a bulk density n and a mobility μ. Considering a constant current I flowing through the structure along the x-axis, and in the presence of an external magnetic field perpendicular to the xy-plane $\boldsymbol{B} \equiv B_z$, the Lorentz force experienced by a moving electron in the y-direction causes it to deviate from its x-direction.

This negative charge carrier deflection to one side of the semiconductor leaves an excess of holes on the other side giving rise to an electric field $\boldsymbol{E}$ in the y-axis. As a result, in the equilibrium, a voltage difference is produced across the structure which is known as the Hall voltage V_{H}, given by

$$V_H = -\frac{IB_{\mathrm{z}}}{en_{\mathrm{s}}}, \tag{4.1}$$

where e is the elementary charge and n_{s} the sheet electron density. In the case of bulk materials, the bulk density is related to the sheet density via $n = n_{\mathrm{s}}/t$, where t the channel thickness.

4.2 Presentation of the device

In order to characterize the FD-SOI technology in terms of material quality, n-doped and p-doped Hall bar structures were designed and fabricated with mass-production process techniques. The devices were based on the same STMicroelectronics' technology used for the quantum dot structures of this work, i.e. the thick-gate-oxide Regular V_{th} option of the 28 nm UTBB FD-SOI technology. Apart some exceptions, the same flow process, conceived for the physical implementation of the quantum dot devices, is used for the manufacturing of the Hall bars. In fact, since the dimensions of the micrometre-sized devices did not violate the design rules and all the GAGS rules were respected, no modeling is performed before the realization of the structures via the TCAD Process simulation tool. In addition, as this work was focused on the study of the demonstration of the classical Hall effect, no QTCAD simulation of the device is performed.

As shown in Figure 4.2 (a), the studied Hall effect microstructures consist of six terminals. The ohmic contacts are depicted with green color, the polysilicon gate with red, and the electrostatic access to the back gate with gray. The blue rectangular layer indicates the region area where the silicide and the doping were blocked during the fabrication of the device. The same design is used for the physical implementation both of the n-doped and p-doped Hall bars. The only difference between these two is the doping of the ohmic contacts and the back plane, which are n-doped and p-doped respectively, and vice versa. In Figure 4.2 (b), an SEM image of an n-doped Hall effect microstructure is illustrated. Several extra tiles and dummies, added during fabrication, are visible here, filling up the empty space around the structure. A Focused Ion Beam (FIB) deprocessing technique [202, 203, 204] was employed in order to remove the upper metal, via, and oxide layers until the contact-polysilicon level was reached. The use of the FIB method over such a large area in this micrometer-sized structure led to a noticeable curtaining effect, i.e. an apparent surface roughness in the direction normal to the FIB ion beam axis due to ion-solid interaction [205, 206]. The device dimensions given here are indicative and have been obtained via STMicroelectronics calibrated tools. Taking under consideration the measurement inaccuracy and material degradation due to the electron beam, a 5% uncertainty of dimensional measurements is estimated.

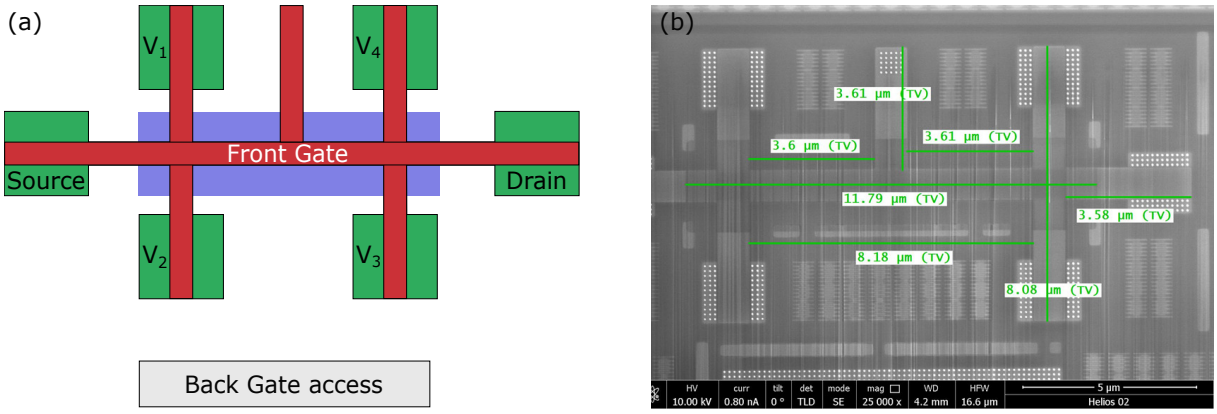


Figure 4.2 – (a) Schematic representation of the Hall bar microstructure designed and fabricated for the classical Hall effect measurements. The only difference between the n-doped and p-doped Hall bars is the doping of the ohmic contacts and the back plane. The ratio of length over width of the silicon channel of the device was designed to be approximately equal to 10. (b) SEM image showing one of the fabricated n-doped Hall bar. A 5% uncertainty in the device dimensions was evaluated. The upper layers were removed via a FIB deprocessing technique permitting to reveal the polysilicon and contact layers. The added tiles during the fabrication process are distinguishable around the manufactured structure. The six ohmic contacts, the electrostatic access to the back gate, and the front gate are visible, as well as the contacts to the first metal layer.

4.3 Experimental setup

In order to measure the material properties of the investigated samples, a four-terminal sensing characterization is performed using lock-in amplifier AC measurement techniques. Once the initial sample examination and device characterization steps (see Chapter 3) were carried out, i.e. the leakage current test and the measurement of the transistor I-V characteristic, both the longitudinal and transverse Hall voltages were measured using a lock-in amplifier.

To protect the samples from ESD issues, the diced chips containing the Hall effect devices were transferred in an electrostatic dissipative Gel-Pak box, as depicted in Figure 4.3 (a). The high-vacuum liquid-helium cryogenic probe station was used to cool the Hall bars down to the base temperature of 4.2 K. A combination of tungsten and BeCu DC probes were used to electrically connect the samples to the room temperature instruments (Figure 4.4 (c)). As shown in Figure 4.3 (b), six Hall bar chips were glued down at the same time to a metallic plate and then mounted onto the probe station chamber. Silver conductive adhesive paste was used to glue the samples allowing for thermal and electrical connection to the sample holder. In Figure 4.3 (c), a microscope image of a die loaded into the cryogenic chamber is shown. The dies were diced from an MPW wafer and our contributions were located in the middle of the chip. Each chip contained two Hall bar structures, one n-doped and one p-doped, sharing the same substrate with the quantum dot devices that are discussed in the following chapters.

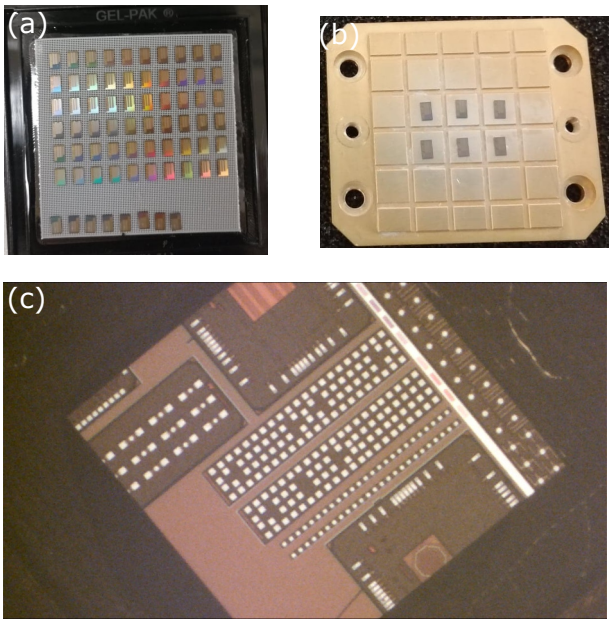


Figure 4.3 – (a) Electrostatic dissipative Gel-Pak box containing Hall bar dies destined for carrier density and mobility measurements. Each die includes two Hall effect microstructures, one n-doped and one p-doped. (c) Microscope image of a die mounted onto the high-vacuum cryogenic probe station. The Hall bars are located in the middle of the chip and the bonding pads are visible.

In order to characterize the manufactured Hall bars, the Hall resistance $R_{\mathrm{H}} \equiv R_{\mathrm{xy}} = V_{\mathrm{xy}}/I$ and the longitudinal resistance $R_{\mathrm{xx}} = V_{\mathrm{xx}}/I$ are measured in a perpendicular magnetic field $B \equiv B_{\mathrm{z}}$ at the temperature of 4.2 K. In Figures 4.4 (a) and (b), a simplified schematic representation of the experimental setups is illustrated, used for the measurement of the resistance R_{H} and the longitudinal resistance R_{xx}, respectively. Two separate SMU channels were used as voltage sources to activate the conduction channel by applying voltage signals V_{FG} and V_{BG} to the front and back gate, respectively, without exceeding the nominal supply voltage range of the technology. Furthermore, a lock-in amplifier was used in series with an 1 MΩ resistor to circulate a current I between the source and the drain of the device through the silicon channel. The reference voltage signal applied by the lock-in amplifier had an amplitude equal to 1 V and a frequency of 90.9 Hz. The same amplifier was also used to measure the input voltage of the device V_{in}. The current flowing through the sample was then estimated by

$$I = \frac{\Delta V}{R} = \frac{1\,\mathrm{V} - V_{in}}{1\,\mathrm{M\Omega}} \approx 1\,\mu\mathrm{A}, \tag{4.2}$$

with V_{in} in the order of a few nanovolts.

As illustrated in Figure 4.4 (a), the Hall voltage V_{H} corresponds to the difference between the voltages V_4 and V_3. A second lock-in amplifier frequency-synchronized with the first one was connected to V_4 and V_3 in order to measure the transverse voltage difference. Moreover, as presented in Figure 4.4 (b), the longitudinal voltage corresponds to the voltage difference between the ohmic contacts V_4 and V_1. Thus, for this measurement, the second amplifier was connected to the ohmic contacts V_4 and V_1. Then, a magnetic field

B was applied via the superconducting magnet of the probe station. The orientation of the external magnetic field was perpendicular to the orientation of the device ($B \equiv B_z$).

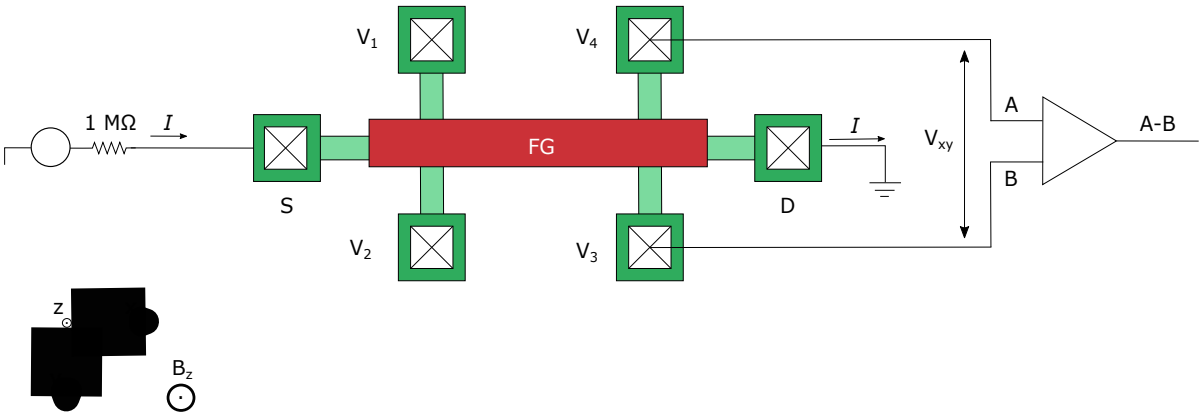
4.4 Hall effect measurements

Four n-doped and four p-doped Hall bar samples were measured in total. However, in this section, we will present and discuss our results on the characterization of the n-doped Hall effect structures only. The unexpected experimental data collected from the characterization of the four p-doped microstructures indicated that further experiments and analysis are required in order to gain a better understanding over the behavior of these devices. This supplementary study unfortunately exceeds the timeline of this PhD project and will be carried out in the future.

Approximately one day was required for a full measurement cycle per sample. The first step towards the Hall bar characterization was to confirm the absence of any short circuit and leakage current between the gates, the conduction channel, and the ohmic contacts. Therefore, continuity and leakage current investigation tests were performed on every ohmic contact and gate of the device, following the same methodology used for the exploration of a quantum dot device. The measurements were initially performed at room temperature and were repeated at base temperature.

The following step was to verify that the typical features defining an FD-SOI structure were demonstrated by extracting its I-V characteristic curve. To do so, the structure was operated as a typical MOSFET and electronic transport measurements were carried out using three separate SMU channels as voltage sources. Voltage signals are applied to the source, the front, and back gate for a grounded drain and floating ohmic contacts V_1, V_2, V_3, and V_4. As an example, the measured I-V characteristic curve of one of the four n-doped samples that were characterized in total, i.e. Sample #1, is presented in Figure 4.5 (a). At 4.2 K, a voltage sweep is performed on the front gate for a fixed voltage of 1 V applied to the source, for different voltages applied to the back gate. Indeed, the measured current I_{ds} is in the expected order of magnitude for the chosen electric configuration realized on an FD-SOI structure measured at low temperatures [95, 198]. In addition, for a grounded back gate, the threshold voltage V_{th} of the device is identified approximately at 800 mV which is in the voltage range for a 28 nm FD-SOI EG structure operated at cryogenic temperatures [95, 197, 198]. Furthermore, a double electrostatic control is observed over the conduction channel by the front and the back gate, and the V_{th} modification by the back gate is efficient. The current-voltage curve is also plotted in a logarithmic scale (Figure 4.5 (b)) permitting to confirm the absence of any leakage current in the structure. In conclusion, the I-V characteristic measurement allowed to verify the accurate performance of the structure demonstrating the main technology characteristics.

(a)



(b)

(c)

(c)]

Once a functional device was identified, the Hall effect was measured using the experimental setup configuration presented in Figure 4.4. The temperature was fixed at 4.2 K and the ohmic contact V_2 was kept floating throughout the whole experimental process. The aforementioned applied current I of approximately 1 µA was imposed to flow from the source to the grounded drain through the channel. Then, the superconducting magnet was activated and an external magnetic field B_z was applied perpendicular to the xy-plane of the Hall structure.

First, the Hall resistance $R_H \equiv R_{xy} = (V_4 - V_3)/I_{ds}$ was measured as a function of the external magnetic field B_z for two circuit configurations. As a first step, a sweep was performed on the magnetic field from −1 T to 1 T, and the resistance was measured for different voltages applied on the front gate while the back gate was grounded. As a second step, a sweep was performed on the magnetic field from −1 T to 1 T, and the resistance was measured for a fixed voltage of 1 V applied on the front gate and a voltage step performed on the back gate. In Figure 4.6, the experimental results in the case of Sample #1 are presented, demonstrating the dependence of the Hall resistance from V_{FG} and V_{BG}, and confirming its double control by the front and the back gate.

It was observed that the Hall effect manifests itself by the presence of a voltage difference between the ohmic contacts V_4 and V_3. The Hall resistance R_H increases linearly with the magnetic field as predicted by the Hall effect. Also, more positive voltages applied on the gates lead to a more negative slope due to an increase in the electron density n and the electron mobility μ. Although the modification of the transerve resistance is possible by both the front and the back gate, the front gate appears to have a stronger effect than the back gate.

Next, one of the material properties of the n-doped microstructure, namely the sheet electron density n_s, is estimated based on the following equation

$$R_H = -\frac{B_z}{en_s}. \tag{4.3}$$

A linear regression of R_H is used to extract and determine the sheet density n_s. Apart from the density, the slope of R_H as a function of B_z allows to determine also the sign of the charge carriers. In this case, given the fact that the type of the majority charge carriers is already known, the absolute value of the Equation 4.3 was considered for the calculation of n_s instead. In Figure 4.7, the estimated densities in the case of the four measured n-doped Hall effect structures are summarized and presented as a function of the voltage V_{FG} applied to the front gate for a grounded back gate and as a function the voltage V_{BG} applied to the back gate for 1 V to the front gate.

It was observed that the density n_s increases approximately linearly between $2 \cdot 10^{12}$ cm^{-2} and $6 \cdot 10^{12}$ cm^{-2} more or less as a function of the voltage V_{FG} applied to the front gate varying from 1 V to 1.5 V and for 0 V applied on the back gate. Furthermore, it is noticed that the density n_s rises approximately linearly between $2.5 \cdot 10^{12}$ cm^{-2} and $3.5 \cdot 10^{12}$ cm^{-2} roughly for a voltage V_{BG} applied on the back gate varying from 0.4 V to 2 V and a voltage V_{FG} fixed at 1 V on the front gate. This observation confirms that the modification of the voltage V_{FG} has a higher impact on the electron density comparing to V_{BG}, and also that using the FD-SOI technology a double control over the electron

density is achieved by combining V_{FG} and V_{BG}. Finally, the good reproducibility of the experimental data demonstrates the high yield of the device fabrication using exclusively industrial methods.

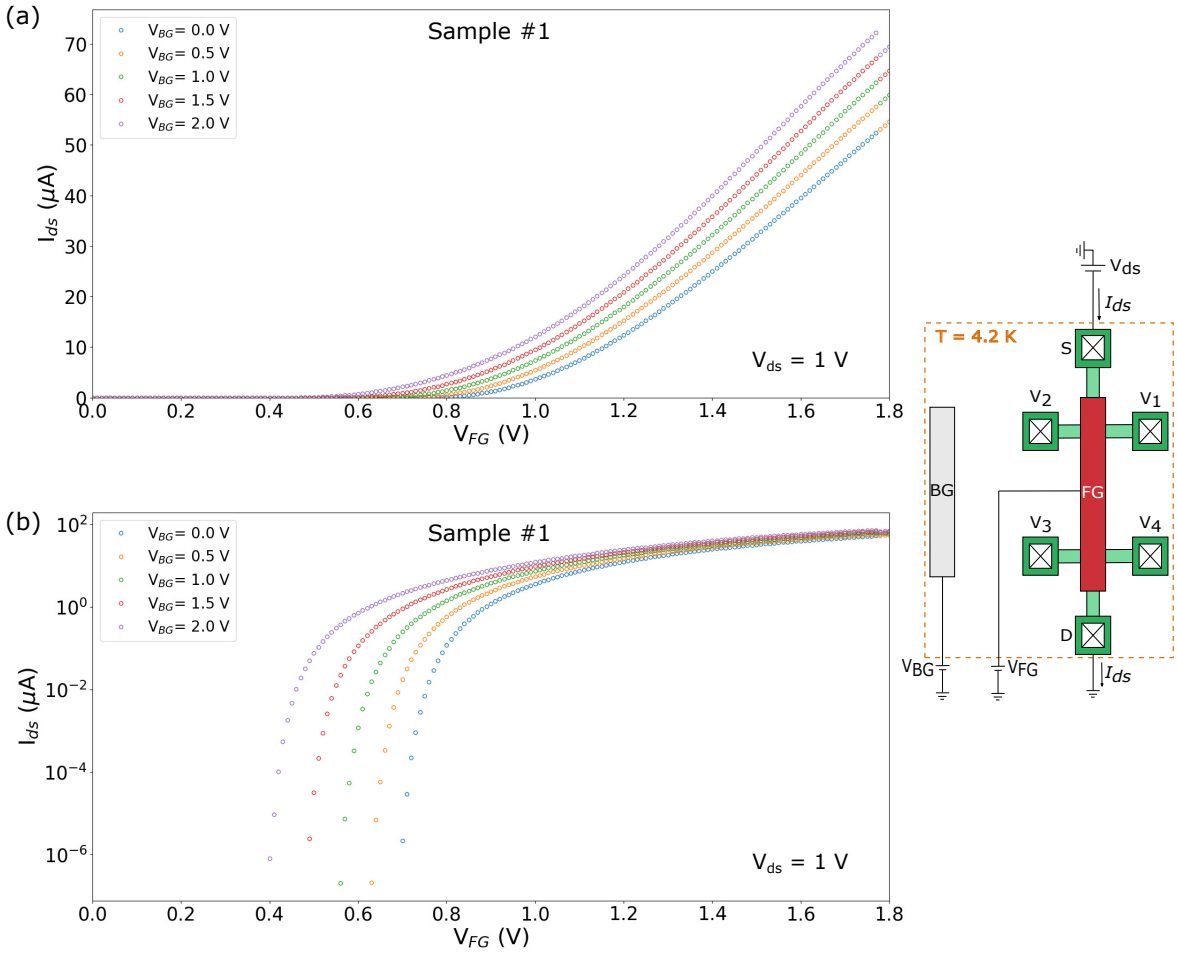


Figure 4.5 – (a) I-V characteristic curve of the Sample #1 from the four measured n-doped Hall effect microstructures operated as a typical FD-SOI MOSFET at 4.2 K. The drain was grounded while the ohmic contacts V_1, V_2, V_3, and V_4 were floating. The current was measured for a voltage sweep performed on the front gate and a voltage step on the back gate. A threshold voltage V_{th} of 800 mV was observed for 0 V on the back gate. When more positive voltages were applied to the back gate, V_{th} was decreased. (b) I-V characteristic curve of the same device plotted in a logarithmic scale confirming the absence of any leakage current in the structure.

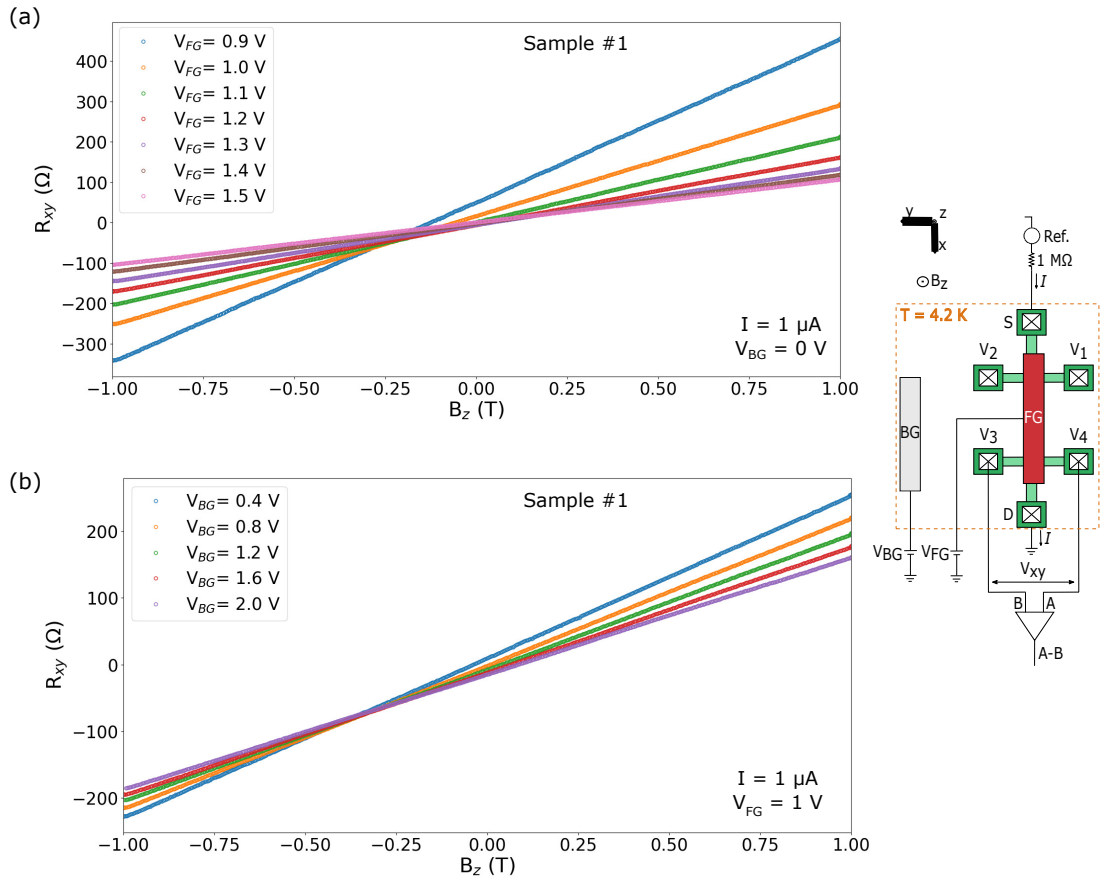


Figure 4.6 – The Hall resistance $R_H \equiv R_{xy} = (V_4 - V_3)/I$ of the Sample #1 from the four measured n-doped Hall effect microstructures was measured at 4.2 K as a function of the external magnetic field B_z using AC measurement techniques. The measurement was repeated for a 1 μA current I applied to the source, and for different voltages applied to (a) the front gate V_{FG} and 0 V to the back gate, and (b) the back gate V_{BG} when 1 V was applied to the front gate. The modification of the resistance R_H is observed by altering the voltages V_{FG} and V_{BG} independently or both at the same time.

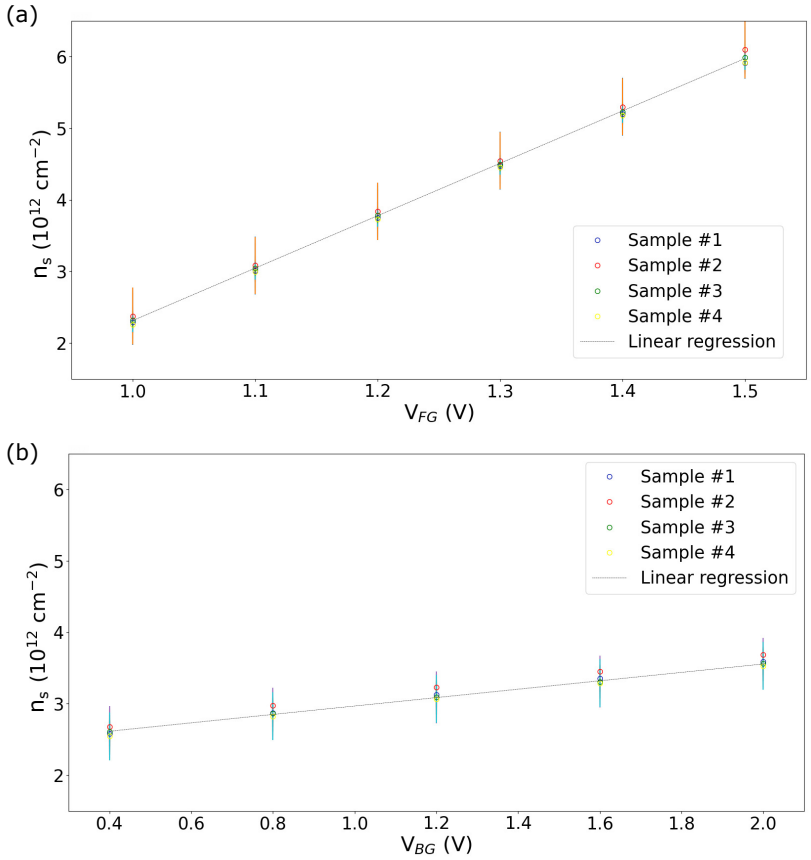


Figure 4.7 – Measured electron density $n_s = |B_z/eR_H|$ of the four n-doped Hall bar samples at 4.2 K as a function of (a) the voltage V_{FG} applied to the front gate and 0 V applied to the back gate, and (b) the voltage V_{BG} applied to the back gate for 1 V applied to the front gate.

The longitudinal resistance $R_{xx} = (V_4 - V_1)/I$ was measured next as a function of the external magnetic field B_z. First, a sweep was performed on the magnetic field from −0.1 T to 0.1 T for certain voltage values applied to the front gate and a grounded back gate. Then, the measurement was repeated for certain back gate biases and a fixed voltage of 1 V applied to the front gate. In Figure 4.9, the experimental data of the measured R_{xx} in the case of Sample #1 are presented, showing the dependence of the longitudinal resistance from both the voltages V_{FG} and V_{BG}, either separately or both together.

It is observed that the resistance R_{xx} decreases when the voltage applied both to the front and back gate is increased due to an increase in the electron density n and the electron mobility μ. Furthermore, it is noticed that, similar to the case of the transverse resistance R_H, the front gate appears to have a stronger impact on the modification of the longitudinal resistance R_{xx}, comparing to the back gate.

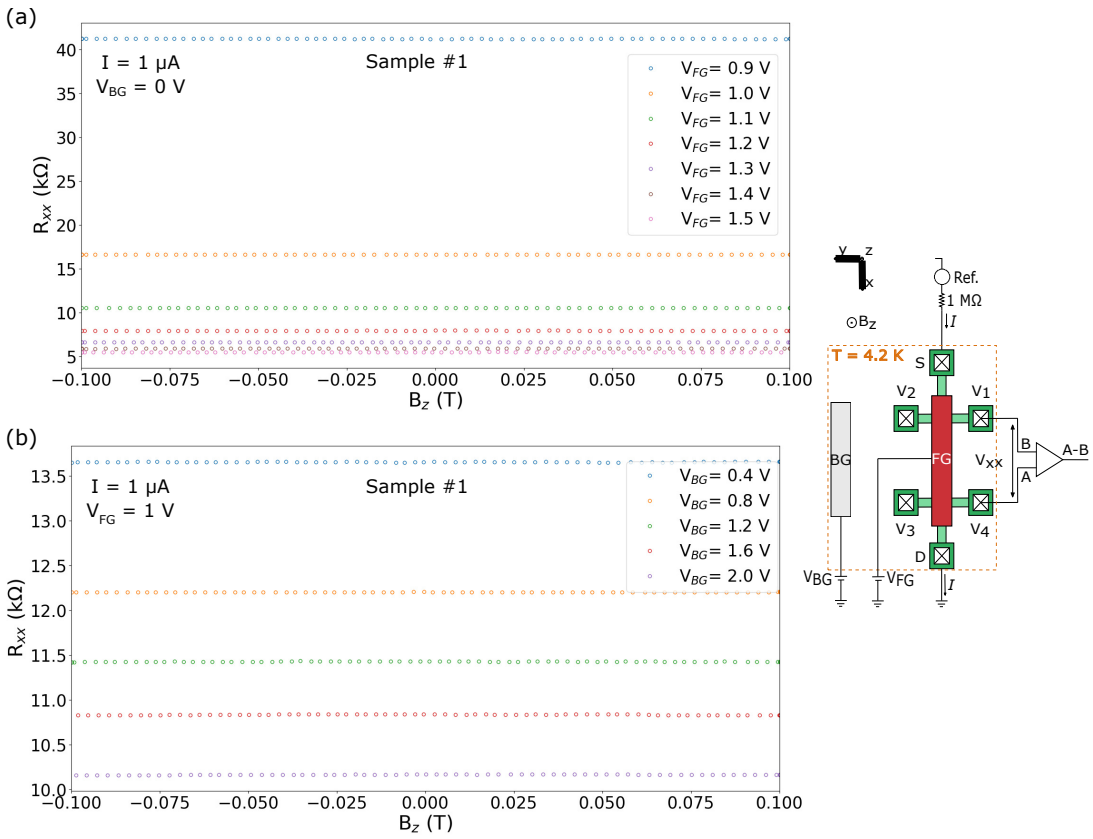


Figure 4.8 – Longitudinal resistance $R_{xx} = (V_4 - V_3)/I$ of the Sample #1 of the four measured n-doped Hall bar samples at 4.2 K as a function of the perpendicular magnetic field B_z. The measurement was repeated for an applied current I of approximately 1 µA on the source and for different voltage values applied to (a) the front gate V_{FG} for a grounded back gate, and (b) the back gate V_{BG} for 1 V fixed on the front gate, demonstrating the impact of both V_{FG} and V_{BG} over R_{xx}.

Last, the electron density n_s permitted to calculate the electron mobility μ of the microstructures. More specifically, the electron mobility μ is related both to the electron density n_s and the longitudinal resistance R_{xx} at zero magnetic field, i.e. $B_z = 0$ T , according to the formula

$$\mu = \frac{l}{w e n_{2D} R_{xx}(0)}, \tag{4.4}$$

where l and w are the length and width of the conduction channel, respectively. In Figure 4.9, the estimated electron mobilities μ are summarized corresponding to the four measured n-doped Hall bar samples.

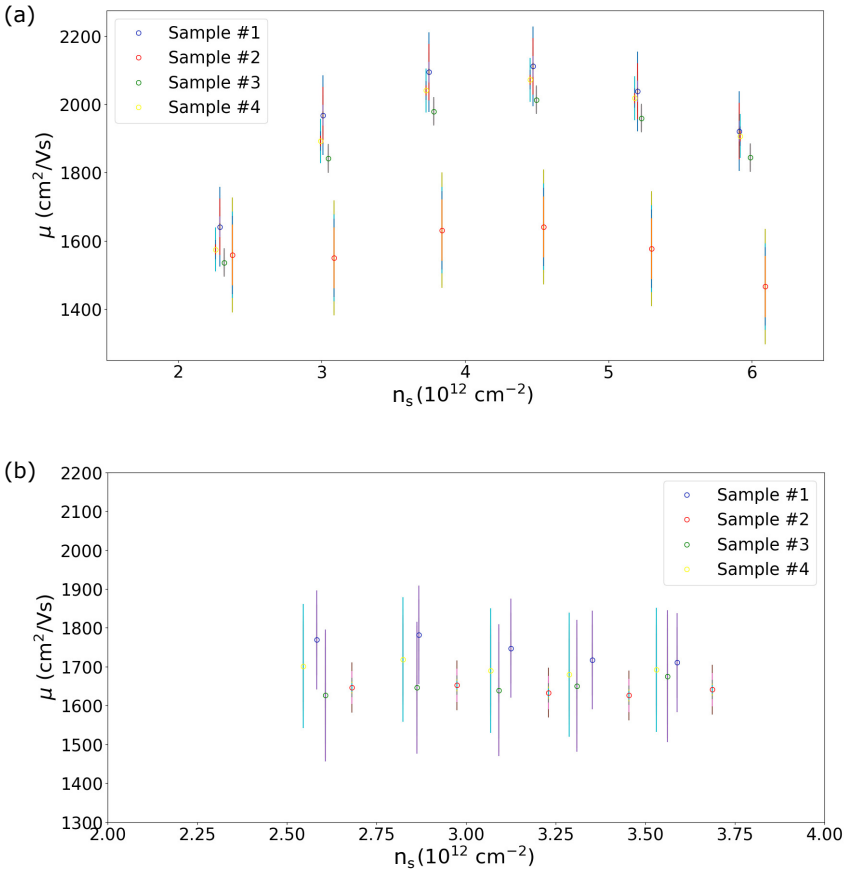


Figure 4.9 – Measured mobility μ of the four n-doped Hall bar samples at 4.2 K as a function of the sheet electron mobility n_s for different voltages applied on (a) the front gate and 0 V applied on the back gate, and (b) the back gate and a fixed voltage of 1 V on the front gate.

Although, in general, the highest mobilities are reported for a device operating in the linear regime, the Hall bars were operated in the saturation regime in these measurements. Since the purpose of this experiment was primarily to evaluate the effect of the front gate alone on the mobility, this regime is more appropriate for doing so, leading however to reduced electron mobilities expected for a device operated in the saturation regime due to the conduction channel pinch-off. By raising the voltage V_{FG} applied to the front gate, which leads to larger electron densities, it is recorded that the electron mobility increases, starting from the value of 1600 $cm^2/(Vs)$ cm^2/Vs approximately. Moreover, after reaching its highest value at almost 2000 cm^2/Vs corresponding to a density of $4{\cdot}10^{12}$ cm^{-2}, the mobility decreases ending up to almost its initial value. As the electron density continues to increase, scattering effects caused by, for instance, trapped oxide charges in the Si/SiO_2 interface (See Chapter 5), further limit electron mobility.

On the other hand, any modification of the back gate bias was not observed to have a remarkable impact on the electron mobility variability. More precisely, the mobility remains almost constant at 1700 cm^2/Vs, whereas the electron density increases. This observation is not surprising, as the back gate is mostly used for V_{th} modulation and its effect over the channel is limited due to the much larger distance between these two com-

pared to the front gate [207]. During the measurement of the electron density, although the impact of the back gate bias over the latter is apparent, a smaller impact is witnessed comparing to the front gate bias. Comparing to the first measured point in Figure 4.9(a) at 1600 cm^2/Vs approximately, which corresponds to 0 V applied to the back gate and 1 V to the front gate, the mobility is increased to almost 1700 cm^2/Vs in Figure 4.9(b). Thus, despite the fact that the effect of the V_{BG} bias on the electron density was observed, higher voltage values might allow to observe a significant variation on the electron mobility. However, such high voltages exceed the technology supply voltage limits and risk to damage the device.

4.5 Chapter summary

In summary, the cryogenic-temperature measurement of Hall effect microstructures intended for the characterization of the technology was presented in this chapter. This was the first time, to date and to our knowledge, that the electron density n and mobility μ were reported for the case of industry-standard process 28 nm FD-SOI Hall bars measured at 4.2 K. Double control of the electron density was achieved through both the front and back gate. More precisely, a linear increase in the density n_s was recorded in the range of approximately $2 \cdot 10^{12}$ cm^{-2} and $6 \cdot 10^{12}$ cm^{-2} when the V_{FG} bias was increased to more positive values and the back gate was grounded. Additionally, a less strong impact of the back gate bias on the electron density was reported, as it was expected, due to the much larger distance of the voltage application region from the conduction channel compared to the front gate. Indeed, a linear increase of the density n_s in the range of roughly $2.5 \cdot 10^{12}$ cm^{-2} and $3.5 \cdot 10^{12}$ cm^{-2} was observed, as the V_{BG} bias was increased to more positive values for a fixed voltage V_{FG} of 1 V. Therefore, it was shown that the back gate can be used in addition to the front gate in order to modify and control the electron density. This feature of double control over the electron density, thanks to the back gate, distinguishes the FD-SOI Hall bar structures from competitive technology platforms offering more flexibility to their operation. In addition, for a device operating in the saturation regime, an electron mobility in the range of 1400 cm^2/Vs and 2200 cm^2/Vs was recorded versus the electron density and the V_{FG} bias for a grounded back gate. When the back gate was activated, an increase in the mobility was observed. However, when the V_{BG} was modified and for a fixed V_{FG} bias at 1 V, the mobility remained almost constant at around 1700 cm^2/Vs, indicating that higher voltages V_{BG} might be required for the inspection of its dependence from the back gate.

Understanding conditions for the few-electron regime

5

Contents

In order to define a high-quality qubit platform suitable for quantum computing applications, it is crucial to reduce the quantum dot occupancy down to the single-electron level. In this chapter, the numerical computations using the 3D QTCAD software to model the first-generation quantum dot device at 1.4 K are demonstrated along with experimental observations. Together, these computations and observations shed light on the required gate biasing and device geometry conditions to attain the single-electron regime for electronic transport tunneling through side-gate activated corner quantum dots in the device.

In the first section, the geometry of the device is presented, along with the particular characteristics of the technology. In the second section, the 3D QTCAD model used to simulate the first-generation quantum dot device is discussed. In the third section, electrostatic calculations and experimental observations demonstrating activation of transport through the nanostructure using the back gate alone are presented. In the fourth section, experimental and numerical evidence of the formation of side-gate activated corner dots in the conduction channel of the device is reported. In the last section, numerical computations and experimental data of Coulomb blockade spectroscopy performed on the split-gate device are demonstrated and the necessary conditions to achieve single-electron tunneling in this particular architecture are discussed.

It is noted that the device was fabricated and characterized before the development of the QTCAD modeling tool. In fact, the results presented in this chapter are the result of a collaboration between Université de Sherbrooke, Université Grenoble Alpes, STMicroelectronics, and Nanoacademic Technologies Inc. The experimental data presented here, along with the measurement equipment and methods, are presented in detail in [96].

5.1 Presentation of the device

For the quantum dot devices developed in this study, free electrons are strongly confined to the interface between Si and SiO_2 in the FD-SOI structure forming a 2DEG. Confinement in the other two dimensions is accomplished by locally depleting the 2DEG using gate electrodes. The resulting structure is weakly coupled to the ohmic contacts of source and drain by tunnel barriers, connecting the device to the measurement equipment.

The first generation of the quantum dot architecture developed in this study was based on the split-gate architecture [179] and was designed and fabricated using the thick-gate-oxide Regular V_{th} option of the technology. The design of this structure contained a few DRC errors which were selectively waived before the generation of the tape-out used for fabrication in STMicroelectronics. The majority of these errors were due to overall shape of the structure, but the design did not contain however any error in the most important technology design rules, i.e. the GAGS rules.

A cross-section and top-view of the quantum dot device are shown in Figure 5.1 (a) and (b) respectively. The device has the same technology characteristics as a typical 28 nm UTBB FD-SOI n-type MOSFET. More precisely, the source and drain were epitaxially grown and were n-doped regions forming the ohmic contacts. Spacers were used to limit

the source/drain extensions under the gates. The top gates were made of polysilicon, and the back plane was p-doped. In the case that the polysilicon gates were designed above the channel, i.e. FGT, FGB, and G2, they were built on top of a gate oxide layer. Otherwise, they were fabricated on top of the field oxide surrounding the device. Electrical contact to the back gate was made between STI trenches filled with oxide. A lateral access to the back gate is illustrated in Figure 5.1 (a) for simplicity. In the end of the fabrication process, silicide was deposited almost everywhere on top of the source, drain and gates, excluding the region over the channel where the quantum dot was expected to be formed. [1]

This split-gate device was intended for the realization of transport measurements. For this reason, the G2 gate was designed to control the quantum dot potential in the silicon channel and splits the front gate in two parts: Front Gate Top (FGT) and Front Gate Bottom (FGB). A positive voltage on both parts of the front gate was used to form the 2DEG at their interface with the silicon oxide to create both the source and drain reservoirs. The role of this separation between the two parts of the front gate was to form the tunnel barriers between the electron reservoirs and the quantum dot which were characterized each by a tunneling rate.

In Figure 5.1 (c), the schematic representation of the electrostatic potential profile expected for the designed structure is presented. The two additional lateral gates G1 and G3 were initially designed to obtain extra control over the tunnel barriers characterized by the tunnel rates Γ_1 and Γ_2 between the electron reservoirs and the quantum dot by controlling their heights and widths. In the remainder of the chapter, it is presented that, instead, they led to the formation of corner dots at the interface of the active region and the field oxide.

5.2 QTCAD model for the split-gate device

The quantum dot device was modeled using the QTCAD simulation tool allowing to simulate its electrical and quantum behavior at cryogenic temperatures. The theoretical models employed for the QTCAD simulations are presented briefly in this section. A more detailed presentation of the mathematical and physical models can be found in [151].

The 3D geometry of the quantum dot structure was defined via the FEM mesh generating tool Gmsh [152] which offers manual fine tuning of the mesh. A first-order mesh containing 2.5 million nodes was generated. Local mesh refinements were manually implemented in areas of fast potential variations allowing to improve precision and convergence. Once the different materials and regions were defined, the electrodes and the doping were specified.

[1] For confidentiality reasons, no further information on the exact dimensions of the device is provided here.

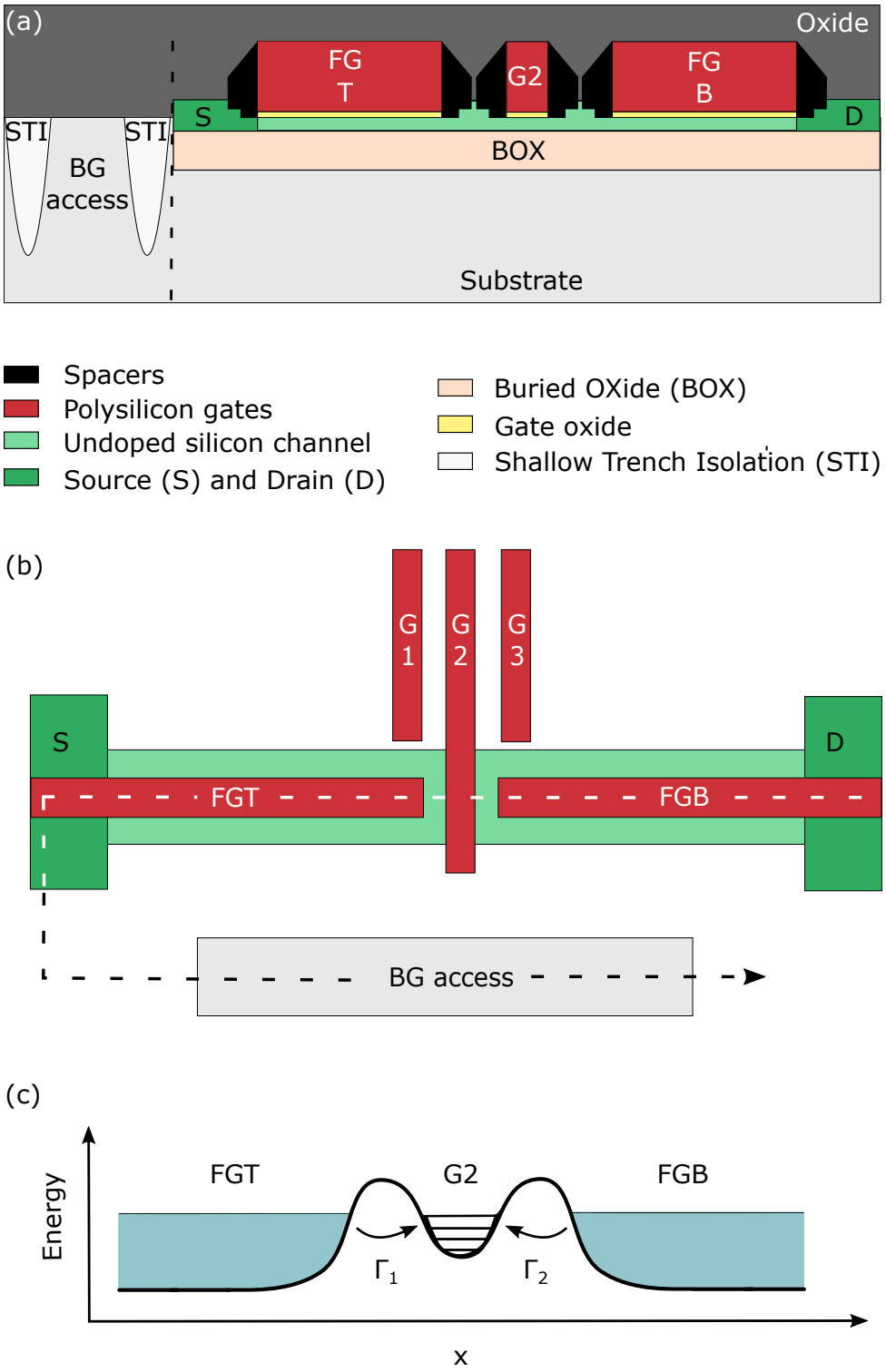


Figure 5.1 – (a) Schematic showing the cross-section of the split-gate device. (b) Schematic showing the top view of the split-gate device, consisting of the source (S), drain (D), front gate splitted into two parts (FGT and FGB), back gate (BG), and gate G2. Two gaps between the gates FGT, G2 and FGB define two tunnel barriers characterized by the tunnel rates Γ_1 and Γ_2. The lateral gates G1 and G3 were designed to manipulate these tunnel barriers. (c) Schematic of the expected electrostatic potential profile in the device. The two tunnel barriers separate the quantum dot from the electron reservoirs which were expected to form under the gate G2, and the gates FGT and FGB, respectively.

In Figure 5.2, the resulting 3D CAD model is shown without displaying the mesh. Isothermal conditions were assumed in all simulations with a uniform temperature of 1.4 K imposed throughout the device. The following Dirichlet boundary conditions on the electrostatic potential were considered: gate (metal-insulator) boundary conditions were imposed at the polysilicon gates (surfaces shown in red color in Figure 5.2) and Ohmic contacts were considered at the source and drain (surfaces shown in dark green in Figure 5.2), and bottom of the BOX (bottom surface in Figure 5.2). All simulations were executed on the Niagara cluster of Compute Canada[2].

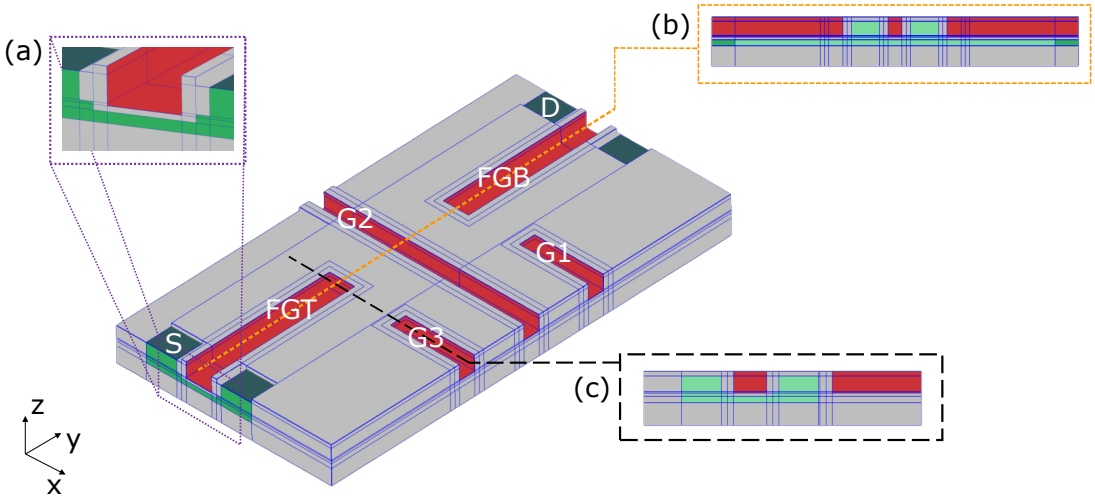


Figure 5.2 – 3D CAD model used to simulate the FD-SOI nanostructure from the layout used for the actual fabrication of the device via Gmsh and the QTCAD software. The device was used to form electrostatically defined quantum dots under the electrodes. (a) Cross section along the x-axis presenting the silicon channel (in pale green), source, drain, spacers, and high-k metal gate stack (in red). The darkest green shade indicates surfaces to which Ohmic boundary conditions are applied in the simulations. (b) Cross-section along the y-axis illustrating the two parts of the front gate (in red), gate G2 (in red), and channel grown on the BOX (in gray). (c) Cross-section along the x-axis illustrating the channel, the front gate lying on the silicon film and the G3 gate located on the field oxide (in gray).

Assuming thermodynamic equilibrium throughout the device, the non-linear Poisson equation [57] was solved self-consistently, yielding the electric potential and the classical charge distribution that corresponds, according to the statistical physics of semiconductors, to:

$$\varepsilon \triangle\varphi = -q(p - n + N_+ - N_-), \tag{5.1}$$

where φ, ε, q, p, n, N_+, N_- stand for the electric potential, the dielectric permittivity of the medium, the elementary electric charge, and the hole, electron, ionized donor, and ionized acceptor densities, respectively. In the framework of the Thomas–Fermi approach [208, 209], and assuming a 3D isotropic and quadratic band model [155], the carrier

[2] https://www.computecanada.ca/home/

densities in electron and hole reservoirs are given respectively by

$$n = N_{\mathrm{c}} F_{1/2} \frac{E_{\mathrm{F}} - E_{\mathrm{C}}}{k_{\mathrm{B}} T}, \tag{5.2}$$

and

$$p = N_{\mathrm{v}} F_{1/2} \frac{E_{\mathrm{V}} - E_{\mathrm{F}}}{k_{\mathrm{B}} T}, \tag{5.3}$$

where E_{C} refers to the conduction band edge, E_{V} the valence band edge, E_{F} the Fermi level, T the temperature, k_{B} the Boltzmann constant, and $F_{1/2}$ the complete Fermi–Dirac integral of order $1/2$.

The electron and hole effective Density Of States (DOS) are given respectively by

$$N_{\mathrm{c}} = \frac{g_{\mathrm{c}} \left(\frac{2 m_{\mathrm{c}} k_{\mathrm{B}} T}{\pi \hbar^2} \right)^{3/2}}{8}, \tag{5.4}$$

and

$$N_{\mathrm{v}} = \frac{g_{\mathrm{v}} \left(\frac{2 m_{\mathrm{v}} k_{\mathrm{B}} T}{\pi \hbar^2} \right)^{3/2}}{8}, \tag{5.5}$$

where $\hbar$ is the reduced Planck's constant, m_{c} and m_{v} the electron and hole DOS effective mass, and g_{c} and g_{v} is the total electron and hole band degeneracy, respectively, including both spin and valley degrees of freedom. The band edges are linked to the electric potential via $E_{\mathrm{C}} = -q(\varphi - \varphi_{\mathrm{ref}}) - \chi$ and $E_{\mathrm{V}} = E_{\mathrm{C}} - E_{\mathrm{g}}$, with χ and E_{g} the electron affinity and band-gap, respectively, and φ_{ref} an arbitrary reference potential [57].

In Figure 5.3, a linecut of the conduction band edge E_{C}, taken following a linecut located along the y-axis in the middle of the front gate (see Figure 5.2) and at 1 Å above the BOX, is plotted for different voltages applied on the G2 gate and the back gate. More precisely, for the calculation shown in Figure 5.3 (a), the conduction band edge was computed as a function of the voltage V_{G2}. The rest of the gates were grounded, leading to the fact that no transport was calculated through the device. Indeed, the entire conduction band edge was estimated to be at a higher energy level than the Fermi level. By modifying however the voltage applied on the G2 gate, it was observed that the potential tunnel barrier formed in the middle of the channel was altered. In particular, by applying a more positive bias, it was possible to lower the barrier approaching the Fermi level.

In Figure 5.3 (b), the calculation of the conduction band edge as a function of the voltage V_{BG} is presented. With the rest of the gates grounded and for low voltages applied on the back gate ($V_{\mathrm{BG}} = 3\,\mathrm{V}$ in the diagram), no transport was computed in the device. Nevertheless, it was possible to activate the conduction channel only with the back gate. Indeed, by applying larger biases ($V_{\mathrm{BG}} = 4\,\mathrm{V}$ and $V_{\mathrm{BG}} = 5\,\mathrm{V}$ in the diagram), the whole conduction band edge was forced below the Fermi level.

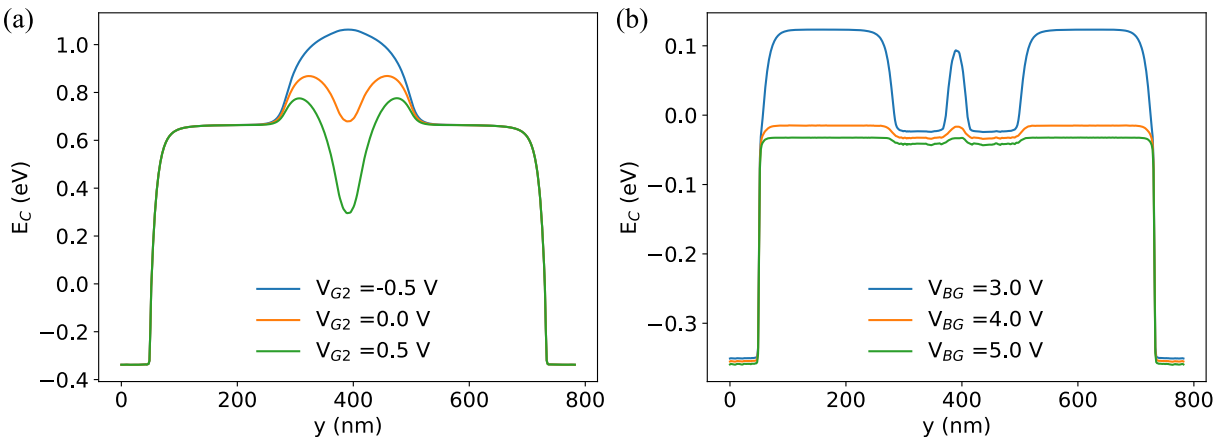


Figure 5.3 – Simulated conduction band profile using the simulation tool QTCAD at 1 Å from the BOX into the silicon film along the y-axis parallel to the transport (see Figure 5.2). A 2DEG at the Si/SiO_2 interface was observed, along with an ability to tune the potential barrier height by applying the appropriate voltages to G2 and the back gate. (a) A voltage sweep was performed on the gate G2 with all the other gates grounded. (b) A voltage sweep was performed on the back gate with all the other gates grounded. The zero of energy corresponds to the Fermi level.

5.3 Back gate transport activation

The formation of a single electrostatic quantum dot under the gate G2 was not observed experimentally. Nevertheless, this gate could be used to regulate the tunnel barrier when the back gate was polarized appropriately to activate the conduction channel with the rest of the gates grounded, as shown by the simulation results in Figure 5.3 (b). In the remainder of the section, experimental data demonstrating channel activation under this electrical configuration are presented, along with their confirmation by QTCAD simulations at 1.4 K.

Specifically, the transport current flowing through the channel was measured versus the voltage to the G2 gate and the back gate [96]. The measurement results are presented in the diagram in Figure 5.4, in which two regimes can be identified. In the first regime, located in the region above the black dashed line, for higher voltages applied to G2, a conduction channel is formed in the device by biasing the back gate alone. In the second regime, below this black line, the G2 gate serves as a tunnel barrier requiring the application of a voltage on the back gate to overcome it and to activate transport. Moreover, it is noticeable that an increase in the voltage applied on the back gate leads to a decrease in this tunnel barrier inducing transport for lower voltages on G2.

The QTCAD simulations, represented by the red and blue dots in Figure 5.4, are in good agreement with the experimentally observed performance of the device. Indeed, the slope of the oblique line marking the distinct regions of activated and blocked transport is almost identical in the calculations and the measurements. In order to compare the two slopes, the numerical data have been shifted compared to the experimental results so that the two corner turn-on points, indicated by a white circle in Figure 5.4, overlap. This

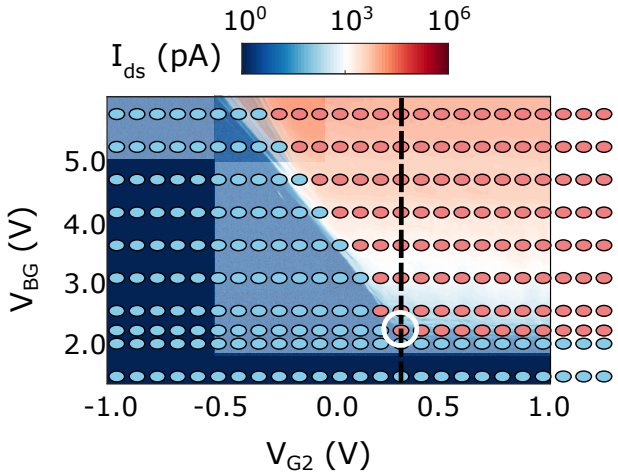


Figure 5.4 – Comparison between numerical calculations using QTCAD and experimental measurements of current flowing through the conduction channel as a function of V_{BG} and V_{G2} at 1.4 K. The black dashed line separates the diagram into two regions showing the two different regimes of current activation in the channel. Density plot: experimentally measured current for a non-activated (blue region) and activated (red region) channel [96]. In the dark blue region, the current is artificially set to zero to reduce the measurement time. The blue dots correspond to numerical calculations of the band diagram predicting blocked transport, and the red dots to numerical calculations predicting allowed transport. In the characterized structure, a corner turn-on point is identified at $(V_{G2}\ ,\ V_{BG}) = (0.34\ ,\ 2.24)$ V (white circle). In the simulated device, it is identified at $(V_{G2},\ V_{BG}) = (0.0\ ,\ 3.7)$ V. The numerical data have been shifted in the V_{G2} and V_{BG} axes by 0.34 V and −1.46 V respectively, so that these two turn-on points fit together revealing an almost identical slope of the inclined line separating the discrete regions of activated and blocked transport in theory and experiment.

stems from the fact that the numerical model does not consider surface charges trapped at the gate oxide interfaces, resulting in an offset between the simulated and the measured corner turn-on point. In fact, these offsets can potentially be used to assess the magnitude of the charge trap density.

5.4 Side-gate activated corner quantum dots

An analysis performed on both the numerical and experimental data showed that side-gate corner quantum dots [210] could be formed in front of G1 and G3 when these lateral gates are polarized positively. Specifically, at low voltage and without back gate biasing, the large spacing between the FGT, G2 and FGB gates leads to large tunnel barriers and thus does not allow transport to be measured experimentally without exceeding the polysilicon gates nominal supply voltage (1.8 V) of this technology and inducing a significant leakage current between the gates and the channel. However, since the distance of G1 and G3 from the channel is larger than for G2, it is possible to apply voltages much higher than 1.8 V on them before the generated leakage current towards the channel causes a problem.

Therefore, when a voltage of the order of 10 V is applied to G1 and G3, the additional potential forces the conduction band under the Fermi level and forms a conduction channel. Reference [96] reports current measurements in the Coulomb blockade regime as a function of the V_{G1} and V_{G3} biases which enabled a triangulation analysis suggesting the formation of quantum dots near G1 and G3 (Figure 5.5 (c)). The electrostatic triangulation technique is used to identify the quantum dot location in the device based on the transition slopes of measured stability diagrams generated by different combinations of electrode potentials.

While the triangulation technique is described in [96], it is also summarized here for completeness. After collecting current measurement for each pair of electrode potentials (among FGT, FGB, G1, G2, and G3), the relative slope of transitions in each charge stability diagram was extracted. In the double-dot charge stability diagram for each electrode pair, along a line parallel to a charge transition, the quantum dot charge is constant, giving:

$$\Delta Q = C_i \Delta V_i + C_j \Delta V_j = 0, \tag{5.6}$$

which results in:

$$\alpha = \frac{C_i}{C_j} = -\frac{\Delta V_j}{\Delta V_i}, \tag{5.7}$$

where α is the relative lever arm of gate i with respect to gate j, $\Delta V_{i,j}$ the variations in gate voltage in a transition, and $C_{i,j}$ the gate capacitances.

In parallel, a simple approximate electrostatic model was used in [96] to calculate the electrostatic potential in a 2D model of the device, without taking into account the shielding effects, quantum confinement and 3D geometry of the active region and the gates. For each pair of gates, this model enabled to identify curves in space, called equi-lever arm curves, along which gate bias increments lead to a change in potential that is equal to the measured lever arm ratio. The regions with the same ratio $\alpha_{theo} = \alpha_{exp}$ are shown in Figure 5.5 (c). An uncertainty of $\pm 30\%$ is identified nevertheless to these lever-arm curves, considering the inaccuracy of the theoretical model and of the extraction of the relative lever arms. The regions that maximize the number of overlaps between the equi-lever arm curves (shown in blue in Figure 5.5 (c)) indicate that the most probable location of the quantum dots is between the gates G1-FGT and G3-FGB on both sides of the G2 gate.

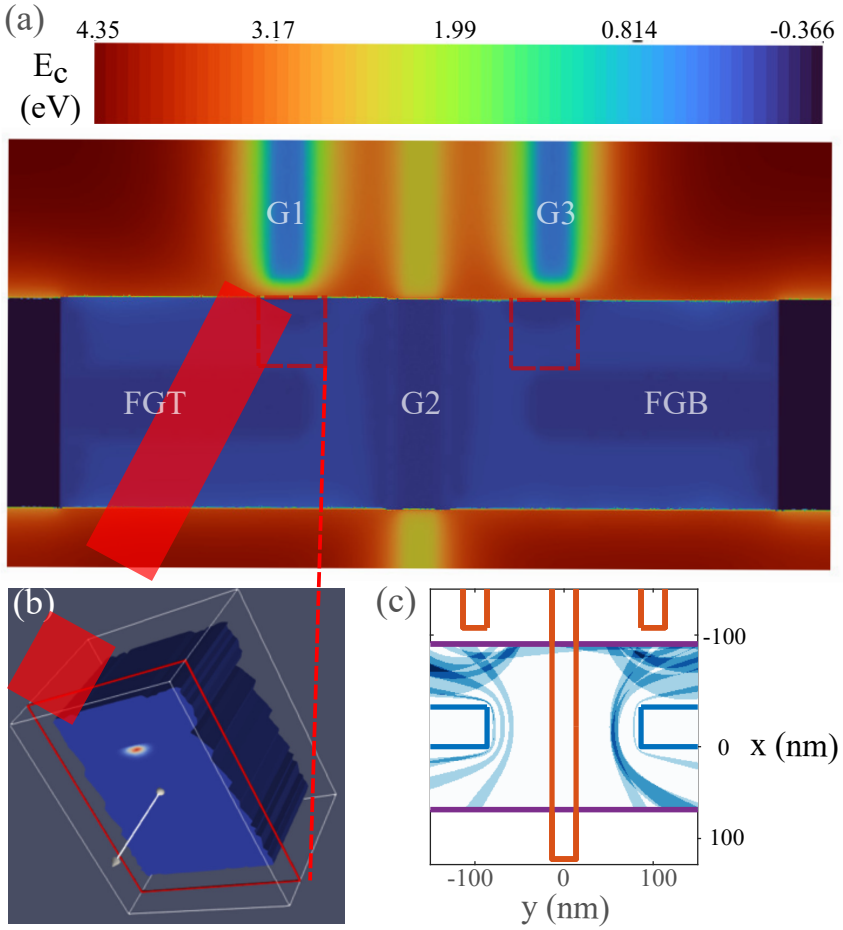


Figure 5.5 – Numerical calculation and exploitation of the experimental results indicating the presence of side-gate activated corner quantum dots in front of G1 and G3. Fixed voltages were applied to the gates: $V_{\mathrm{FGT}} = V_{\mathrm{FGB}} = 843\,\mathrm{mV}$, $V_{\mathrm{G2}} = 1.7\,\mathrm{V}$, $V_{\mathrm{BG}} = 0\,\mathrm{V}$, $V_{\mathrm{G1}} = V_{\mathrm{G3}} = 4\,\mathrm{V}$. (a) Numerical calculation of the conduction band edge using QTCAD. The arrows and roman numerals indicate the sequential tunneling transport model employed in the simulations presented in Figure 5.7. (b) Numerical calculation of the ground state of single electrons in front of G1 using QTCAD. (c) Figure taken from [96]. Lever arm analysis which allowed to estimate the position of the two quantum dots using an electrostatic triangulation technique. Every equi-lever-arm area (shown in blue) corresponds to the condition $\alpha_{theo} = \alpha_{exp}$ś30% for a single pair of V_{G1} and V_{G3} biases, where $\alpha - theo$ was calculated using a coarse electrostatic model (see main text) and α_{exp} was extracted from experimental charge stability diagrams. The most probable quantum-dot locations are at the intersection of equi-lever arm areas, indicated with red circles.

QTCAD simulations predicted the appearance of side-gate activated corner dots at positions that are compatible with the positions indicated by the analysis of the measurement results. More precisely, Figure 5.5 (a) shows the numerically calculated conduction band edge profile over a slice along the xy-plane, 1 nm below the interface between the channel and the gate oxides. The band edge displays clear energy-potential minima in front of G1 and G3 forming potential wells in the corner of the silicon channel. To investigate the existence of bound states in these minima, the time-independent single-electron

effective-mass Schrödinger's equation is solved numerically

$$V(\boldsymbol{r})\psi(\boldsymbol{r}) - \frac{\hbar^2}{2}\nabla \cdot [M_e^{(-1)} \cdot \nabla\psi(\boldsymbol{r})] = E\psi(\boldsymbol{r}), \tag{5.8}$$

where $V(\boldsymbol{r}) = E_{\mathrm{C}}$ is the electron confinement potential and $\boldsymbol{M}_{\mathrm{e}}^{-1}$ is the inverse effective mass tensor. Eigenenergies and eigenfunctions, i.e. envelope functions, of this equation are given by ϵ and $F(\boldsymbol{r})$, respectively. Assuming that the valley degeneracy is completely lifted by strong quantum confinement along the z-direction and by the sharp band-edge discontinuity at the Si/SiO_2 interface [211, 212, 213], the inverse effective mass tensor corresponding to the $\pm\boldsymbol{z}$ valleys: $[[\frac{1}{m_{\mathrm{t}}}, 0, 0], [0, \frac{1}{m_{\mathrm{t}}}, 0], [0, 0, \frac{1}{m_{\mathrm{l}}}]]$, where $m_{\mathrm{t}} = 0.19m_{\mathrm{e}}$ and $m_{\mathrm{l}} = 0.916m_{\mathrm{e}}$ are the transverse and longitudinal silicon effective masses, respectively. The numerical solution of Equation 5.8 resulted in bound eigenstates localized near the top edge of the channel in front of G1 and G3 (Figure 5.5 (b)), thus corroborating the results of the analysis performed on the experimental data indicating the existence of side-gate activated corner dots at these areas.

5.5 Requirements for the few-electron regime

To investigate the transport mechanism based on electron tunneling through the two side-gate activated corner dots, sequential tunneling simulations using QTCAD many-body and master equation solvers were compared to transport measurement results. Therefore, based on experimental observations, a transport model was postulated in which an electron sequentially undergoes the tunneling events that follow: (i) tunneling from the source reservoir (below gate FGT) to the dot QD1 (in front of G1), (ii) tunneling from QD1 to the 2DEG island created under G2, (iii) tunneling from the island below G2 to QD3 (in front of G3), (iv) tunneling from QD3 to the drain reservoir (below gate FGB) (see Figure 5.5 (a)). Because of the depth and width of the corresponding potential well (see Figure 5.5 (a)), the region below G2 behaves more like an additional electron reservoir (akin to the source and drain) than as a quantum dot.

In Figure 5.7 (c), experimental measurements of charge stability diagram are shown at strong $\mathrm{V_{G1}} = V_{\mathrm{G3}}$ biases near 10 V [96]. The width of the Coulomb diamonds along the V_{ds} axis indicates a charging energy of ∼5 meV that is almost independent of $V_{\mathrm{G1}} = V_{\mathrm{G3}}$, suggesting that the uncoupled quantum dots formed in front of G1 and G3 are both in the many-electron regime under these bias conditions. Importantly, for these quantum dots, the single-electron regime was never observed experimentally. Because quantum computing applications typically require single electrons, QTCAD was used to investigate conditions for the single electron regime to be achieved. To do so, a simplified scenario was considered in which transport may be modeled separately for a single quantum dot. Focusing on QD1, the 2DEG formed below FGT was modeled as the source, whereas the 2DEG formed below G2, QD3, along with the quantum dot in front of G3, and the 2DEG under FGB were modeled as a single effective drain. To investigate the onset of the single electron regime, the many-body Hamiltonian was first diagonalized (See Chapter 3), using the first $n_{\mathrm{states}} = 3$ eigensolutions of Equation 5.8 as a spin-degenerate set of basis states. For QD1, the chemical potentials are estimated by the definition of the quantum

dot chemical potential: $\{-0.416, -0.387, -0.351, -0.327, -0.292, -0.272\}$ eV, leading to charging energies whose order of magnitude is comparable to the experimental observation demonstrating transport in the many-electron regime (5-10 meV). The electrical configuration on the simulated device was the following: V_{G1}=V_{G3}= 4 V, V_{G2}= 1.7 V, V_{FGT}=V_{FGB}= 843 mV, and V_{BG}= 0 V.

The single-electron regime is achieved when only the chemical potential $\mu(1)$ lies below the Fermi energy set by the source and drain. To find the gate bias V_{G1} that leads to the few-electron regime, the lever arm α of this gate over the quantum dot is estimated. Considering N=1, α is calculated by computing the single-electron ground energy of QD1 as a function of V_{G1} by successively solving the non-linear Poisson and Schrödinger's equation and taking a linear fit. In Figure 5.6, the estimated single-electron energy spectrum of QD1 is presented, showing different energy states as a function of the V_{G1} bias (solid color lines). The linear regression to the ground-state energy is also plotted in the figure (dashed black line), which gives $\alpha = 0.2$ eV/V. Using this lever arm value, the positions of the Coulomb peaks are estimated by solving for each value of N for V_{G1} the equation:

$$\mu(N) = \mu_0(N) - q\alpha(V_{G1} - V_{ref}), \tag{5.9}$$

where μ_0 is the dot chemical potential with $V_{G1} = V_{ref}$, with V_{ref}= 4 V being a reference G1 bias, and where a linear behavior with respect to the gate bias is assumed, as well as a single lever arm α for all chemical potentials of interest. For the current structure, these Coulomb peak positions were $\{1.92, 2.07, 2.25, 2.37, 2.54, 2.64\}$ V.

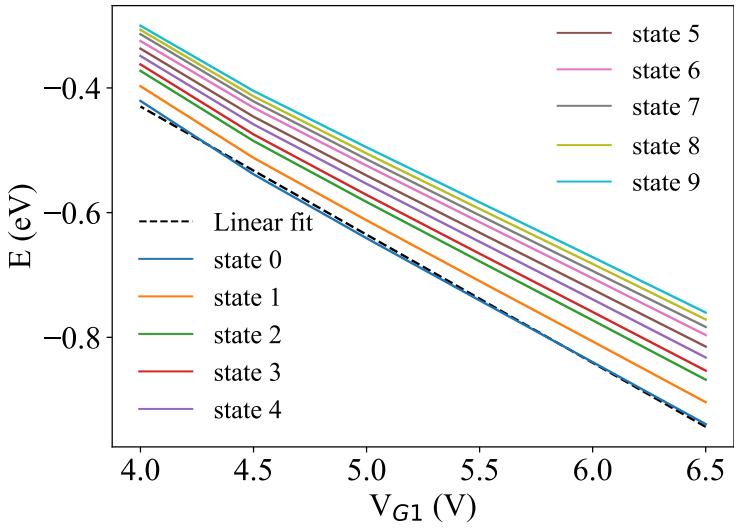


Figure 5.6 – Energy spectrum calculated in QD1 as a function of the voltage applied on the G1 gate, plotted for various energy states (solid colored lines). By fitting the ground-state energy as a function of the voltage applied to gate G1, a lever arm $\alpha = 0.2\,\mathrm{eV/V}$ (dashed black line) was estimated. As seen from the figure, all other energy levels have a similar behavior as a function of the voltage applied to gate G1. This similarity justifies the use of a single lever-arm value for the entire many-body spectrum of QD1 (See 5.9).

In Figure 5.7 (a), the numerical calculation of the Coulomb blockade diamonds is presented displaying the differential conductance, resulting from the solution of the master equation at 1.4 K. Moreover, in Figure 5.7 (b), the estimated current at a V_{ds} bias of 1 mV is illustrated (corresponding to the horizontal dashed white line in Figure 5.7 (a)). The position of the peaks displayed in Figure 5.7 (b) matches the calculation described above based on the dot chemical potentials and lever arm, allowing us to associate Coulomb diamonds and spacings between peaks to bias configurations leading to N electrons occupying the quantum dot. From this analysis, the single-electron regime is achieved for QD1 at $V_{\mathrm{G1}} \approx 2\,\mathrm{V}$.

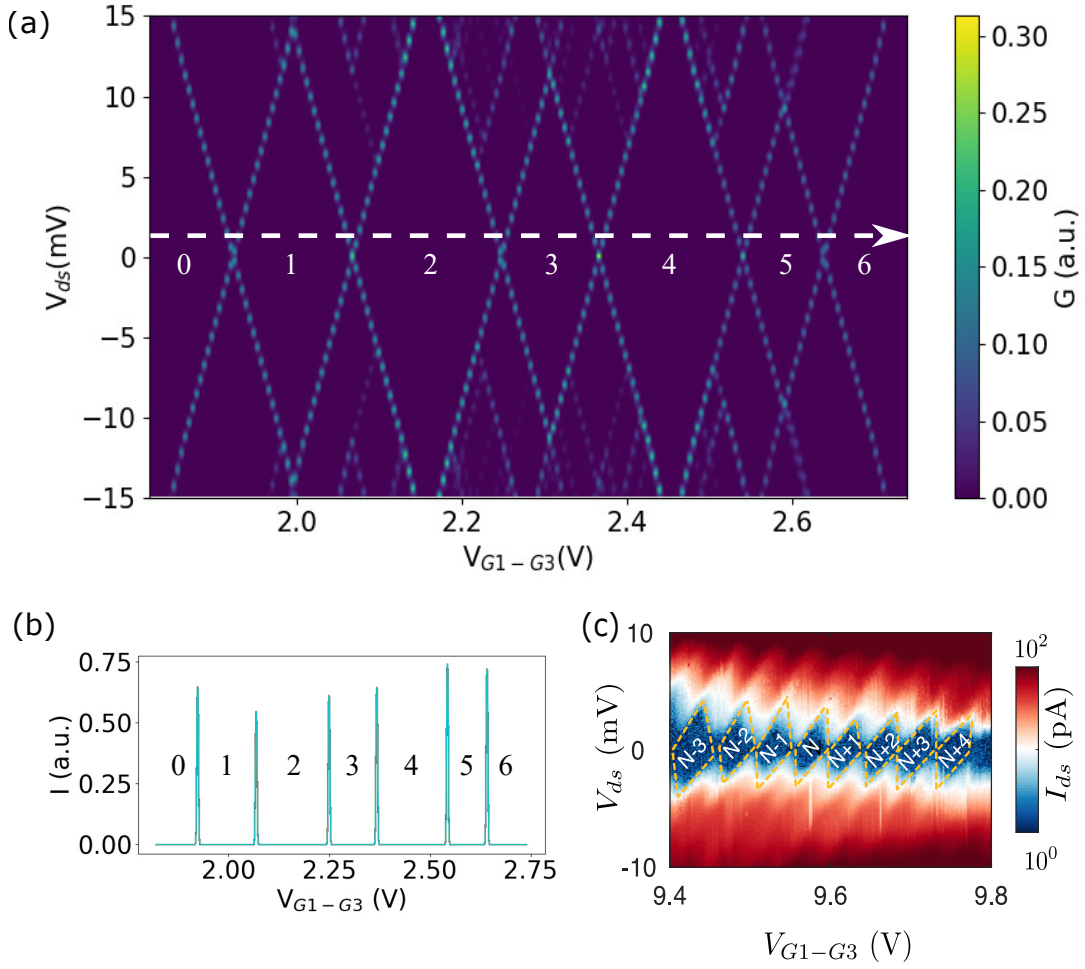


Figure 5.7 – Comparison between numerical calculations and experimental measurements of Coulomb blockade spectroscopy performed on the split-gate device at 1.4 K. The parameters of the electrical configuration of the device are the following: $V_{\mathrm{FGT}} = V_{\mathrm{FGB}} = 843\,\mathrm{mV}$, $V_{\mathrm{G2}} = 1.9\,\mathrm{V}$, and $V_{\mathrm{BG}} = 0\,\mathrm{V}$. (a) Calculated Coulomb diamonds corresponding to QD1 using QTCAD. (b) Coulomb blockade oscillations estimated using QTCAD for a low bias of $V_{\mathrm{ds}} = 1\,\mathrm{mV}$ as a function of the $V_{\mathrm{G1\text{-}G3}}$ voltage applied simultaneously to the lateral gates G1 and G3, corresponding to the single quantum dot QD1. (c) Measured Coulomb diamonds corresponding to QD1 as a function of the $V_{\mathrm{G1\text{-}G3}}$ voltage indicating a charging energy E_{C} of approximately 5-10 meV corresponding to a single quantum dot in the large-electron number regime.

Studying the tunnel barriers formed between the quantum dots and the electron reservoirs (Figure 5.8) permitted to gain useful insights into experimental conditions required to achieve the single-electron regime. Although a single electron may in principle be loaded onto the side-gate activated corner dots in front of G1 and G3 for sufficiently low gate bias, the tunnel barriers between the dots and reservoirs were too high (roughly 100 meV) and too wide (roughly 50 nm) to allow transport current to be measured (see, e.g., the blue line in Figure 5.8). Consequently, the single-electron regime could not be observed at the experimental gate bias of 2 V at which the single-electron regime was expected based on the simulations. In contrast, for large gate biases, simulations showed that the barrier heights and widths may be dramatically reduced (see, e.g., the red line in Figure 5.8). However, such biases would lead to many electrons being loaded into the device, consistent with experimental observations.

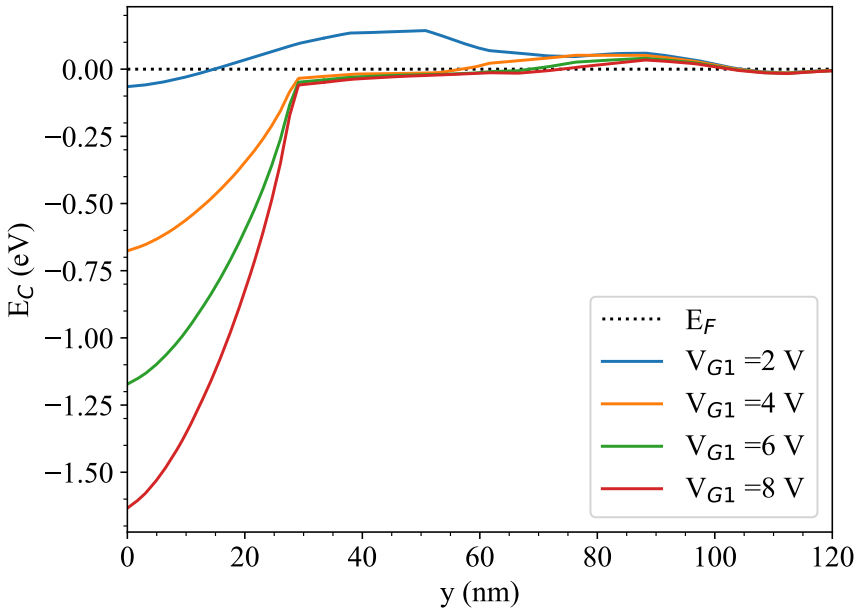


Figure 5.8 – Estimated conduction band profile using QTCAD at 1.4 K. The linecuts presented here were acquired at 1 Å below the top gate oxide, in the silicon film along the white arrow (ii) in Figure 5.5 (a). The ability to adjust the height of the potential barrier by modifying the V_{G1} bias is observed. The zero of E_C corresponds to the Fermi level. The parameters of the electrical configuration of the device were the following: $V_{FGT} = V_{FGB} = 843$ mV, $V_{G2} = 1.9$ V, and $V_{BG} = 0$ V.

5.6 Chapter summary

In this chapter, the simulation of the first generation of the split-gate quantum dot device developed in this study at cryogenic temperatures with the QTCAD simulation tool was presented. Electrostatic simulations performed at 1.4 K confirmed the experimental observation of channel activation by the combined action of the gate G2 and the back gate. In addition, effective-mass Schrödinger calculations verified the experimental data indicating the electrostatic formation of quantum dots near the gates G1 and G3, and

elucidated their side-gate activated corner dot nature. Last, transport simulations clarified the reason why the single-electron regime was not observed experimentally for these dots indicating that narrower and lower potential barriers are required. These results provide an essential insight into the transport mechanisms occurring in the split-gate device and the requirements on gate bias and device geometry conditions to overcome the observed limitations, thus paving the way towards the realization of a next generation of quantum dot devices with reduced critical dimensions.

Exploration of the limits of the 28 nm node

6

Contents

In this chapter, the study and evaluation of the second generation of the split-gate architecture is discussed. In the first section, the challenges to overcome set by the limitations of the technology node are detailed. In the second section, the design is presented and the modifications compared to the design of the first generation of devices are detailed. In the third section, the numerical calculations using the OFDEC and TCAD Process tools that led to the selection of critical dimensions are explained. In the fourth section, the QTCAD simulation results obtained after modeling the nanostructure at 1.4 K are presented. In the fifth section, the physical analysis performed on the fabricated structure is discussed. Last, in the sixth section, the experimental characterization of the device at 1.4 K is presented.

6.1 Physical limits of the 28 nm node

The design of the second generation of the split-gate device is primarly based on the requirements that emerged from the study conducted on the first generation. Such requirements involve lower tunnel barriers between the reservoirs and the dot achieved by reducing the distance between the corresponding gates. This was expected to lead to the experimental measurement of electronic transport tunneling through a single well-defined quantum dot formed in the conduction channel underneath an electrostatic gate able to control the dot potential. To this end, various approaches aiming to reduce the pitch in the new device were tested focusing mostly on improving the resolution of the lithographic process.

As depicted in Figure 6.1, a generic photolithographic system consists of a light source, a condenser lens, a photomask, and an objective lens, used in order to transfer the design from the layout to the silicon wafer [214, 215, 216]. The half pitch is defined as the resolution of the optical system which is described by the equation:

$$R = k_1 \cdot \frac{\lambda}{NA}, \tag{6.1}$$

where λ is the wavelength of the light, k_1 a coefficient summarizing process-related factors, and NA the numerical aperture of the objective lens used in the optical lithography process defined as $NA = n\sin\theta$ with n the refractive index of the medium between the lens and the wafer ($n \approx 1$ for air) and θ is half the angular aperture of the lens.

Several Resolution Enhancement Techniques (RET) [217, 218, 219, 220] exist enabling the photolithographic printing of small features using small technology nodes such as 28 nm FD-SOI. The STMicroelectronics' optical lithography-based fabrication process is fixed for the ensemble of MPW contributions, sharing the same wafer, and is optimized by employing advanced double-patterning steps [221, 222] and various RETs focusing on each resolution parameter. For instance, the numerical aperture NA is increased by using larger lenses and the immersion lithography technique [223, 224, 225, 226] allows to increase the refractive index n by interposing water between the exposure tool's projection lens and the wafer instead of air. Also, another solution to reduce the k_1 factor involves the modification of resist properties [227, 228, 229].

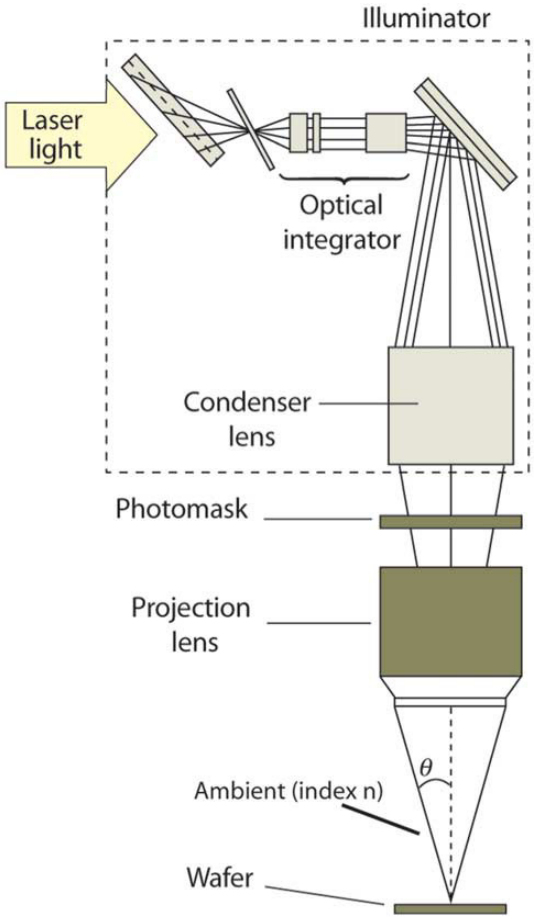


Figure 6.1 – Typical optical lithographic system. Figure taken from [230].

Another widely used RET is the Optical Proximity Correction (OPC) technique, which is applied to the mask design allowing to reduce the k_1 factor [231, 232, 233, 234]. This method implies the presence or absence of adjacent features (proximity) and/or the design of fragmented edges on the feature of interest with each segment being offset so that the target patterns can be printed robustly. During the course of this thesis, several design proposals were developed using additional OPC approaches to the ones already used during the fabrication process at STMicroelectronics, aiming to reduce the distance between the polysilicon gates. The layouts were then simulated and evaluated using the OFDEC software. However, none of them were accepted for MPW fabrication at STMicroelectronics due to the risks or the cost involved, so they are not discussed here in detail. More specifically, one of these approaches attempted a similar technique to the OPC for photomask fabrication and suggested adding polysilicon dummies in the device layout that would not eventually get printed onto the wafer but their presence on the mask design would modify the diffraction pattern by compensating for the pattern transfer error. This solution was rejected because it bore a lift-off risk that could jeopardize the rest of the MPW contributions. Another proposal implied the design of sophisticated fragmented edges on the gates which would help printing robustly the gate features. It was rejected as it required an elaborate maskset layout which was expensive and time-consuming to produce and would not be used for any other project in STMicroelectronics.

No.	Worst-case scenario	Root cause
1	Missing contact	Blocked silicide
2	Merged gates	Reduced gap

Table 6.1 – Main risks for the fabrication of the second-generation split-gate device due to the design rules violations.

In the end, none of the proposed OPC methods could be applied to the design of the masks used in the fabrication for the second generation of the split-gate device. As a result, a more agressive approach was adopted at the new design. The critical dimensions were reduced until the ideal for quantum transport gap between the top gates was achieved. Nevertheless, as the pitch in the first-generation split-gate device was defined by the design rules, its further reduction led to DRM violations. The limits of the technology were reached and several DRC and GAGS errors were unavoidable. As a result, certain risks were risen concerning the physical characteristics and performance of the fabricated device. The absence of silicide in the dot region set up the risk of a missing contact between the DOT gate and the first BEOL layer [235, 236]. In addition, the smaller gaps between the FGT, FGB, and DOT gates bring up the risk of all these gates to merge together. Table 6.1 summarizes these risks.

6.2 Presentation of the device

The design of the second-generation quantum dot device is shown in Figure 6.2. The main features of the thick-gate-oxide RVT option of the 28 nm UTBB FD-SOI technology are identifiable, namely the epitaxially grown source and drain forming the ohmic contacts, spacers, top polysilicon gates, and back gate in the back plane. In the case where the polysilicon gates are designed over the channel, i.e. FGT, FGB, and DOT, they are built on top of a gate oxide layer. Otherwise, they are fabricated on top of the field oxide surrounding the device. The region indicated by a purple rectangular layer in Figure 6.2 (b) was excluded during fabrication from silicide deposition and ion implantation ensuring the inert condition of the silicon channel for the area where the quantum dot is expected to form. In the remainder of this section, the modifications made to the design are presented compared to the first-generation device.

To begin with, the width of the conduction channel was reduced to be the same as the FGT, DOT, and FGB gates in order to eliminate the possibility of the generation of corner quantum dots activated by the side gates. In this way, the probability of forming a single well-defined dot under the DOT gate is increased. Second, the square DOT gate is an improved version of the prolonged rectangular G2 gate that appeared in the first-generation quantum dot device. Like G2, this gate is designed to control the electrostatic potential of the quantum dot that is expected to form under this gate and splits the front gate into the two parts FGT and FGB. Vertical access to the DOT gate is assured via the multiple BEOL layers, allowing to envision scalable 2D and 3D split-gate architectures capable of hosting a larger number of quantum dots. In addition, the square shape of the gate was chosen carefully. It is the minimum possible polysilicon area allowed by the

design rules of this particular technology, in order to form the smallest possible quantum dot and, at the same time, to allow technical integration of the contact connecting the polysilicon gate to the first BEOL layer. Finally, the number of lateral gates was increased to four offering stronger symmetrical control over the tunnel barriers created due to the separation between FGT, DOT, and FGB.

In Figure 6.2 (c), the schematic representation of the expected electrostatic potential profile is presented in the designed quantum dot device. The application of a positive voltage to both parts of the front gate leads to the creation of a 2DEG at their interface with the gate oxide forming the electron reservoirs. The tunneling barriers between the reservoirs and the quantum dot were expected to be characterized by the tunneling rates Γ_1 and Γ_2 and to depend on the critical dimensions of the device.

6.3 Precision of the gate pitch

In view of such important design rules violations, there was an important risk of a non-proper transfer of the intended pattern onto the wafer. This was indeed the case here. In the remainder of this chapter, the work done to first avoid this from happening and then to overcome this challenge is detailed.

First, several variations on the critical dimensions and pitch were investigated by simulating the proposed structure using the OFDEC optical lithography simulation tool. Focusing on the most challenging part of the device for fabrication, i.e. the region where the quantum dot was expected to form, Figure 6.3 (a) shows the OFDEC modeled polysilicon gates and conduction channel (right) based on the final version of the device layout used for the MPW manufacturing run (left). The outline of the layout design is displayed on top of the simulated device for comparison. The modeled conduction channel is depicted in yellow color, the polysilicon gates in purple, and the contact to the first metal layer in pink. The modeled field oxide is depicted in black.

For each simulated element, several variations of certain photolithographic parameters were tested in these simulations resulting in various critical dimensions and feature widths which are depicted as a set of overlapping contours. The simulations showed that the square contact was photolithographically transferred onto the wafer as a circular pattern, which was expected. In addition, the transfer of the channel pattern from the mask onto the simulated wafer ended up to be almost identical to the layout, which was also expected. Moreover, the simulated features of the gates were altered comparing to the layout, resulting in wider gates with rounded corners. Corner rounding and line shortening is generally expected in photolithography and such an error amount in the pattern transferred onto the wafer was within the acceptable limits of features infidelity. The most important result of these simulations was that the gates were not fused with one another and that the gaps between FGT, FGB, and DOT were in the desired range, i.e. 20-50 nm, depending on the optical lithography parameters.[1]

[1] For confidentiality reasons, no further information on the critical dimensions of the device is provided here.

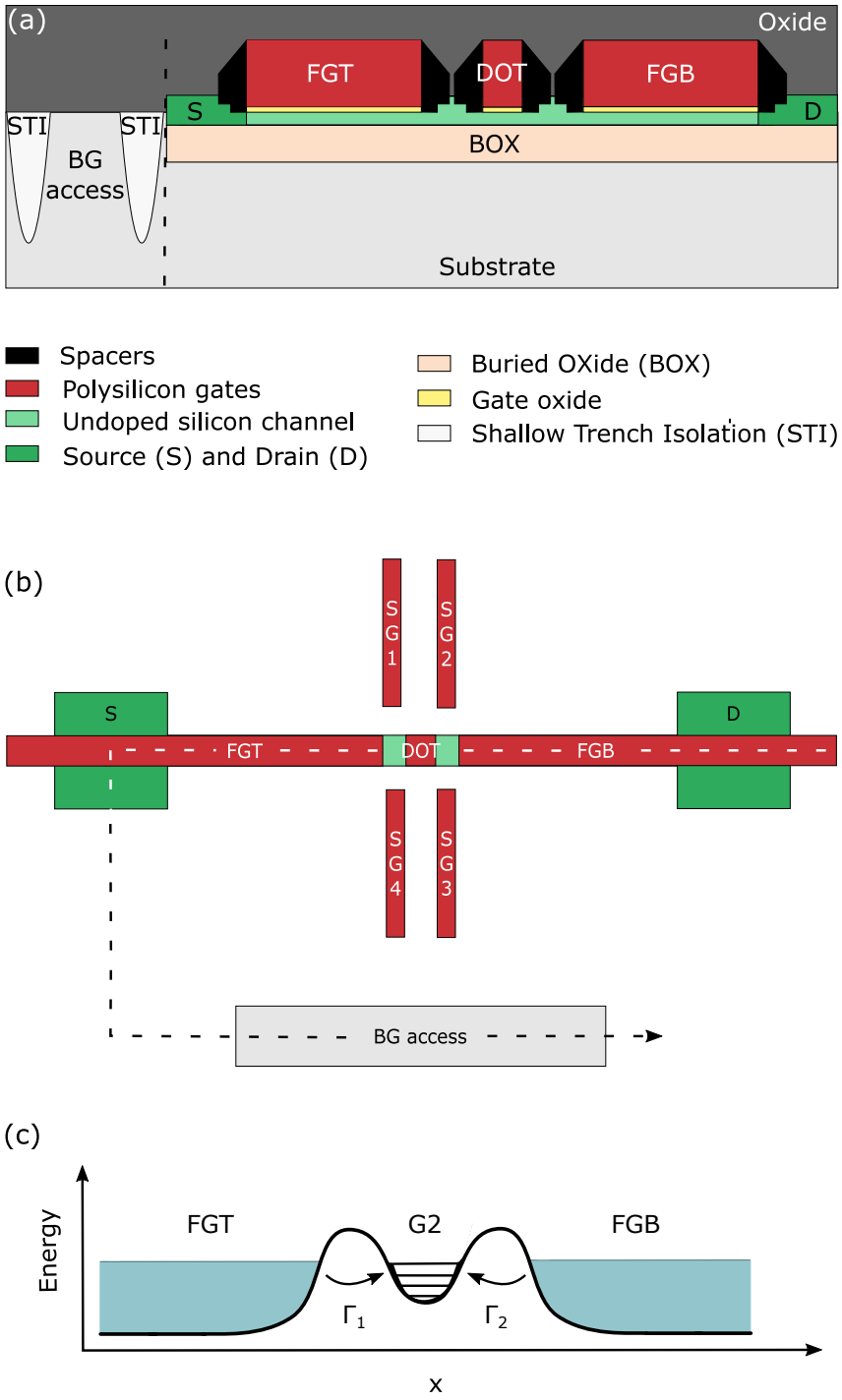


Figure 6.2 – (a) Schematic showing the cross-section of the second generation of the split-gate device. A lateral access to the back gate is illustrated following the linecut in Figure 6.2 (b) for simplicity. (b) Schematic of the the top view of the device. It consists of the n-doped Source (S) and Drain (D), the splitted front gate (Front Gate Top (FGT) and Front Gate Bottom (FGB)), the Back Gate (BG), and the DOT gate. Four lateral gates, SG1, SG2, SG3, and SG4, were designed to manipulate the tunnel barriers. (c) Expected electrostatic potential profile in the second generation of the split-gate architecture. The electron reservoirs were designed to be formed under FGT and FGB, and the quantum dot under DOT. The in-between gaps were designed to form the two tunnel barriers, characterized by the tunnel rates Γ_1 and Γ_2.

A number of technical constraints, however, makes it difficult to achieve these results on silicon. For each one of STMicroelectronics' mass-production runs based on different technology processes, the ensemble of photolithography parameters and manufacturing specifications, such as resist thickness, exposure dose, depth of focus, etc, have been optimized through years of R&D optimization loops and are now fixed to certain values. As a single multi-project wafer is shared between several R&D and customer projects, the latter occupy most of the substrate and dictate the choice of the fabrication parameters. Moreover, the STMicroelectronics' 28 nm FD-SOI model that was used for the OFDEC simulations presented here is only calibrated to compensate for the pattern transfer error based on small deviations from the DRM and is not optimized to estimate with high accuracy the diffraction pattern of such small critical dimensions, almost exceeding the technology limits. As a result, a high risk existed of obtaining a continuous merged top gate instead of three separate ones, despite the encouraging simulation results.

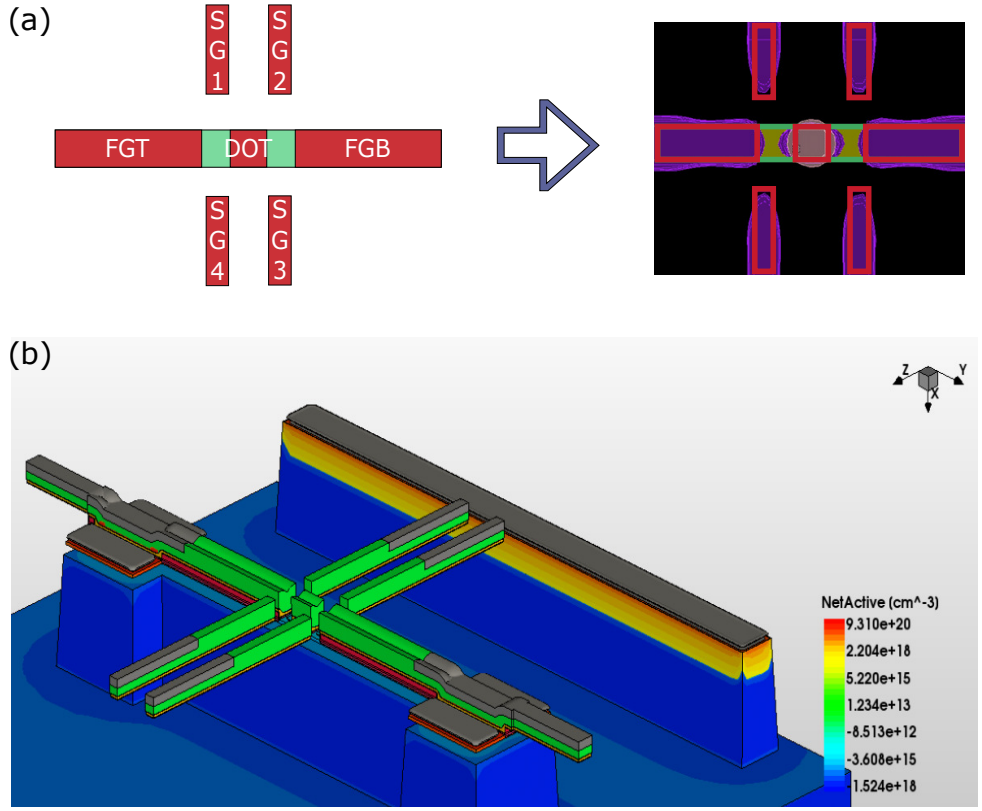


Figure 6.3 – (a) Optical simulation of the split-gate device using the OFDEC software. Left: device layout focusing on the most difficult region for fabrication. Right: simulated features printed onto the wafer. (b) Quantum dot device modeled using the 3D TCAD Process simulation tool based on the layout used for MPW fabrication of the nanostructure.

However, the OFDEC simulations permitted to verify the absence of risks for the adjacent MPW contributions which allowed the acceptance of the design for fabrication at STMicroelectronics, despite the GAGS errors. In spite the fact that the latter are never overlooked, careful inspection and interpretation of the numerical predictions led

to the conclusion that the adjacent circuits and devices were not endangered due to these violations.

After the finalization of the layout following the OFDEC simulations, the structure was simulated using the Synopsys Sentaurus 3D TCAD Process software [148] in order to obtain the 3D geometry and doping profile before the actual fabrication of the device. The various copper interconnect layers routing the device to the bonding pads were not considered during the simulations. Figure 6.3 (b) illustrates the simulated structure showing the carrier concentration varying in the different regions of the device. For a better visibility over the structure, the modeled oxide and nitride layers, namely the BOX, STI, and spacers, were excluded from the 3D topology presented in the figure. The simulated silicide layer is depicted in gray confirming that its deposition was indeed blocked in the desired region. Also, the gate metal stack is slightly n-doped (green and yellow), as it is required for the fabrication of the top gates. Moreover, the channel is undoped, the ohmic contacts are heavily n-doped (red), and the back plane is p-doped (blue). However, the implantation blocking in the region where the quantum dot was expected to form is not taken into account during the simulation. The TCAD Process model is optimized for simulating 28 nm FD-SOI devices that were designed based on STMicroelectronics' DRM and do not consider such design rules errors.

Nevertheless, despite the encouraging results of the OFDEC simulations, it was proven in the process that the device failed to fulfill the initial requirements. Both the physical analysis and characterisation of the device led to the conclusion that the fabrication of the target pattern using the 28 nm FD-SOI technology was unsuccessful and the FGT, DOT, and FGB gates merged with each other. The analysis and characterisation results are discussed in the remainder of the chapter.

6.4 QTCAD device simulation

In this section, the simulated performance of the second-generation split-gate device using the QTCAD software is presented. The structure was modeled via the QTCAD adaptive meshing technique, presented for the simulation of the first-generation quantum dot device in [151], by generating automatically a mesh with approximately $7 \cdot 10^5$ nodes based on the device layout that was used for the MPW fabrication run at STMicroelectronics. Isothermal conditions were assumed in all simulations with a uniform temperature of 1.4 K imposed throughout the device.

First, the effect of the side gates on the transport activation in the conduction channel was explored by electrostatic simulations. Hence, the non-linear Poisson's equation was solved and the conduction band edge was calculated for various voltage differences applied to the side gates SG2 and SG3 simultaneously following a linecut located along the device, near the edge of the channel and in front of the side gates SG4 and SG3 and at 0.1 nm below the top gate oxides. The voltages applied to the rest of the gates are fixed to 1 V on the two parts of the front gate, 1.2 V to the DOT, 8 V to the other two side gates, and 0 V to the back gate. Figure 6.4 shows the numerical calculation of the electrostatic potential profile of the device revealing that the side gates were able to control and modify the tunnel

barriers. The additional potential generated by the side gates forced the conduction band under the Fermi level, identified at the zero of energy, and formed a conduction channel. Since the side gates were not designed to be located above the channel, it was possible to perform these calculations by applying to them voltages that exceed the upper bias limit set by the technology.

Next, in order to investigate the formation of a single quantum dot under the DOT gate, the 3D single-electron effective-mass Schrödinger's equation was solved inside the quantum dot region defined by the energy-potential minimum under the DOT between the two tunnel barriers depicted in Figure 6.4. The solution resulted in bound eigenstates of single electrons localized under the DOT, considering a fourfold degeneracy of z-valley.

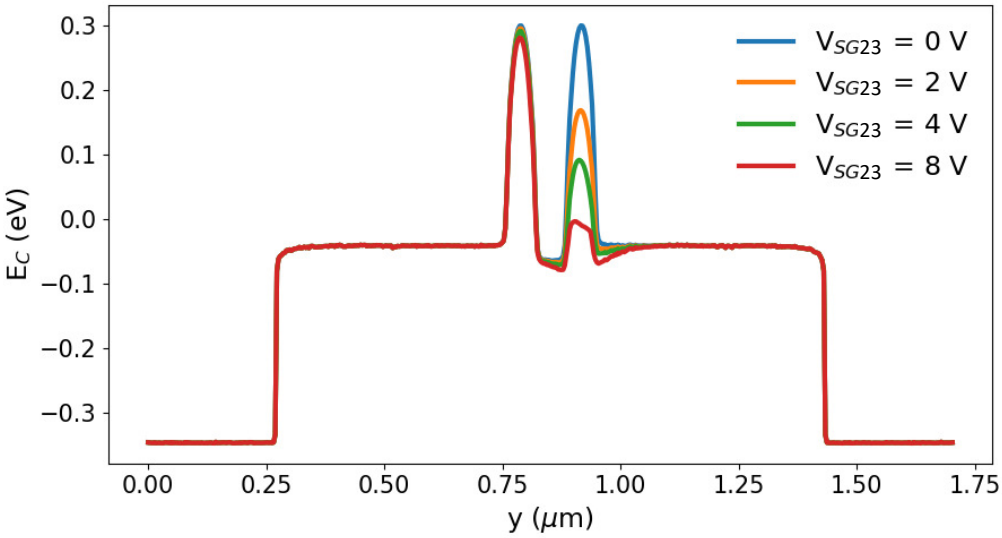


Figure 6.4 – Simulated conduction band edge using the QTCAD simulation software. Linecut taken at 1 Å below the top gate oxide into the conduction channel parallel to the transport. A 2DEG at the Si/SiO_2 interface is observed, along with the ability to tune the potential barrier height by applying the appropriate voltages to the lateral gates. A voltage sweep is performed on the gate SG3 and SG4 simultaneously with the back gate grounded. The voltage applied to the gates FGT and FGB is equal to 1 V, to the rest of the side gates 8 V, and to the DOT gate 1.2 V. The zero of energy corresponds to the Fermi level.

The non-linear Poisson equation was first solved over a range of V_{DOT} biases, for a fixed voltage applied to the rest of the device. The single-electron Schrödinger equation was solved next to extract the quantum dot eigenergies. Figure 6.5 shows these calculated energy levels as a function of the voltage applied on the DOT. Indeed, as expected in the framework of the constant interaction model, a modification in the gate bias controlling the occupancy of the dot brings a modification in the entire energy spectrum calculated in the dot region. A linear fit of the ground state energy was performed then, whose slope corresponded to the lever arm. The latter was estimated to be approximately 0.8 eV/V which is close to the value of 1, corresponding to ideal capacitive coupling. In correspondence with the eigenergies, the single-electron eigenstates were also calculated numerically

in the dot region. Slices from the 3D density plot of the first two, i.e. the ground state and the first excited state, are presented in Figure 6.6. In conclusion, the QTCAD calculations permitted to verify that the formation and eventual control of a gate-defined single quantum dot is possible in the second generation of the split-gate device with the designed geometry and dimensions.

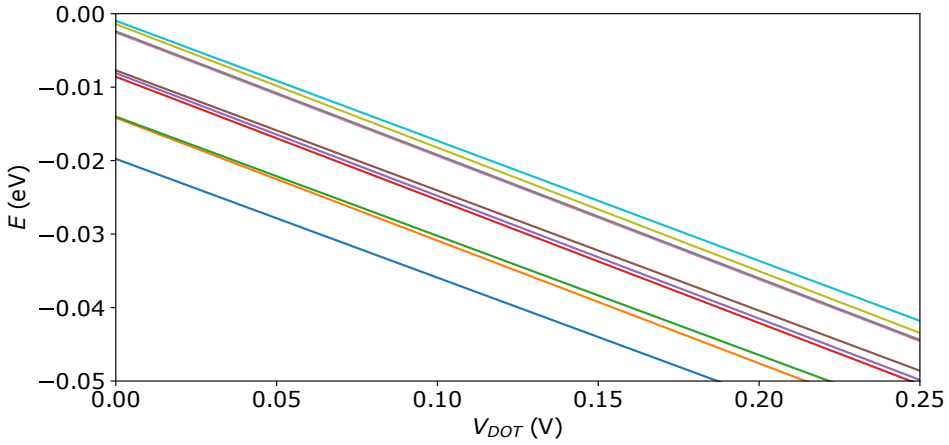


Figure 6.5 – Numerical calculation of the quantum dot energy levels as a function of the voltage applied to the DOT gate. A linear fit is applied on the ground state in order to calculate the lever arm of the DOT gate bias V_{DOT} over the eigenenergies in the dot. Its value is estimated to be approximately 0.8 eV / V.

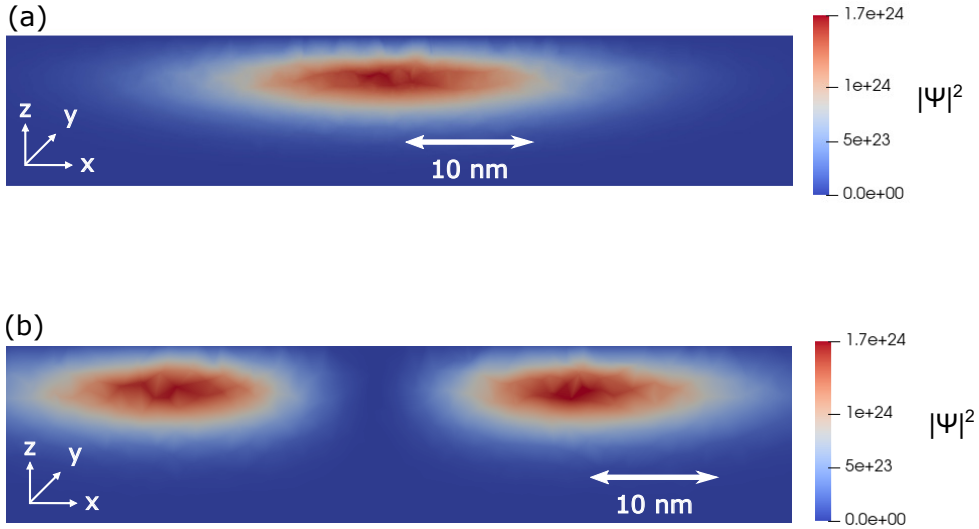


Figure 6.6 – (a) Density plot of the ground state wavefunction of a single electron. A slice was taken in the xz-plane in the middle of the region under the DOT gate. (b) Density plot of the first excited state wavefunction of a single electron. A slice was taken in the xz-plane in the middle of the area under the DOT region. The back gate is grounded, and fixed voltages are applied on the rest of the gates: $V_{\mathrm{FGT}} = V_{\mathrm{FGB}} = 1\mathrm{V}$, $V_{\mathrm{SG1}} = V_{\mathrm{SG2}} = V_{\mathrm{SG3}} = V_{\mathrm{SG4}} = 5V$, and $V_{\mathrm{DOT}} = 0.8\mathrm{V}$.

6.5 Device physical analysis

In view of the limitations of the OFDEC software and the fabrication risks (Table 6.1), it was essential to assess the construction quality of the quantum dot device. To this end, a physical analysis was performed on the device and permitted to demonstrate that, despite the merged gates, the first risk was successfully avoided. In this section, the results of the analysis are presented.

In order to verify the physical characteristics of the device, a cross-section and top-view analysis were performed on the fabricated and un-packaged samples by conducting microscope dimensional measurements. TEM and Scanning Transmission Electron Microscope (STEM) imaging techniques were employed respectively on dies that had not been measured before. The results of the cross-section dimensional analysis are shown in Figure 6.7. A milling process was applied to the sample to remove the unwanted top layers until the contact/polysilicon level was reached. More precisely, a dual-beam technique, based on the combined action of an SEM and FIB technique [202, 203, 204], was employed to identify and prepare the regions of interest for the TEM cross-section analysis. Once the sample was prepared, TEM images were taken with a spatial resolution of 0.5 nm focusing on different regions of the device. The dimensions displayed here are indicative and were measured using STMicroelectronics' calibrated equipment. An uncertainty inferior to 5% is estimated to these values due to material degradation and systematic measurement inaccuracy.

The TEM image shown in the center of Figure 6.7 has been taken along the entire length of the device at the position and direction indicated with the black dashed arrow depicted in the schematic. The individual layers composing the structure are distinguished. Multiple magnified images were taken to better understand their dimensions focusing on different areas. More specifically, in inset (i), it is demonstrated from bottom to top: the thickness of the ensemble of channel, high-k dielectrics, polysilicon, and silicide, along with the thickness of the contacts, and the first copper interconnect layer. In (ii), indicated from bottom to top: the thickness of the BOX, channel, high-k gate metal stack, and polysilicon, together with the length of the contact. The length of this BEOL metal is also illustrated, along with the distance between contacts. In (iii), demonstrated from bottom to top: the thickness of the high-k dielectrics, polysilicon, silicide, passivation layer, and the length of the contact. Finally, in (iv), the thickness of the aforementioned ensemble, the back plane, the STI trenches, and the BOX.

The high-resolution cross-sectional examination of the second-generation quantum dot device revealed that all the individual nanometer-sized features composing a 28 nm FD-SOI structure, i.e. the high-k metal gate stack, polysilicon gates, silicide, BOX, silicon film, and back plane, were fabricated defect-free with the proper dimensions. In addition, this structural analysis showed that despite the challenges imposed by the design rule violations, the contact between the DOT gate and the first copper layer was created in spite of the silicide being blocked in this area. Nevertheless, the critical dimensions of the device could not be evaluated with this imaging method and therefore a top-view imaging approach was used next.

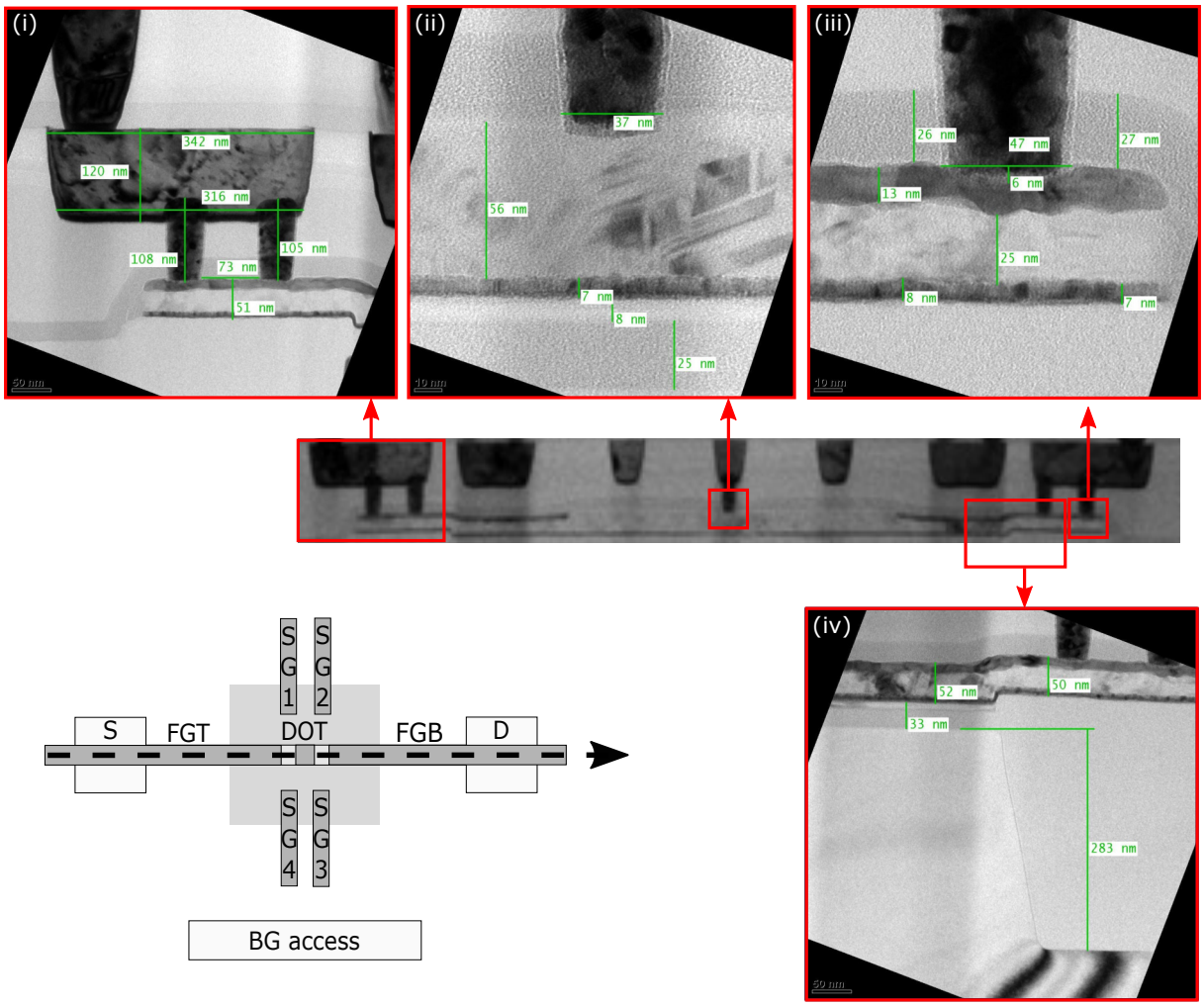


Figure 6.7 – TEM analysis conducted on the fabricated second-generation split-gate device taken along the dashed arrow depicted on the schematic. A dual-beam FIB method was employed to remove the top BEOL layers.

It is worth noting that an SEM-based top-view analysis was attempted first. A FIB-based parallel deprocessing technique [237, 238] was applied to the fabricated samples in order to remove the field oxide, and interconnect layers and achieve the polysilicon/active level. However, the procedure was terminated without success. A breakdown of the device was observed at every sample when the desired level was reached, as shown in Figure 6.8. The access to the back gate is visible, but the rest of the device has been completely destroyed resulting in the individual regions no longer being identifiable. After careful inspection, it was concluded that the root cause of this failure was due to an ESD stress event induced during the deprocessing procedure, which also introduced this pronounced surface roughness that can be seen in the image here; again demonstrating the fragile nature of the samples.

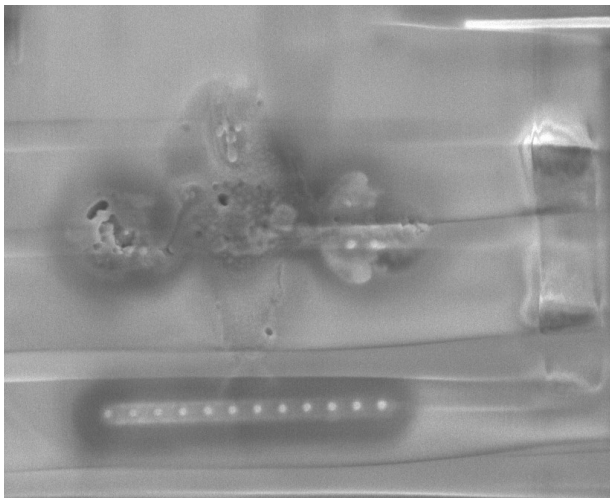


Figure 6.8 – SEM image of the second-generation fabricated split-gate device demonstrating a typical example of structure deterioration due to an ESD stress event caused during the device restoration process.

Hence, the STEM imaging technique was selected to complete the failure analysis conducted on the split-gate device [239, 240, 241]. A FIB-based parallel recovery technique was used to remove the upper layers, ensuring the metallization of the specimen throughout the thin-film coating process. This additional metallic layer enabled better grounding conditions to be achieved and thereby to eliminate any ESD issues. The TEM cross-section technique was then employed to prepare the sample for the subsequent imaging analysis.

At this stage, several STEM images were acquired with a spatial resolution of 0.5 nm focusing on different device regions of interest. In Figure 6.9, the measured critical dimensions of the top view of the fabricated quantum dot device are shown. A $\pm 5\%$ error was introduced in the values presented here due to material degradation and systematic measurement inaccuracy.

In particular, the top view of the fabricated quantum dot device is presented in the center of Figure 6.9. The ohmic contacts, the access to the back gate and the various gates, as well as their contacts with the first interconnect layer, can be seen here. In the insets of the figure, magnified STEM images are shown highlighting different parts of the structure, namely: (i) the two lateral gates on the left side, (ii) the region in the center of the device where the quantum dot was expected to form, (iii) the other two lateral gates on the right side, and (iv) the region of the drain.

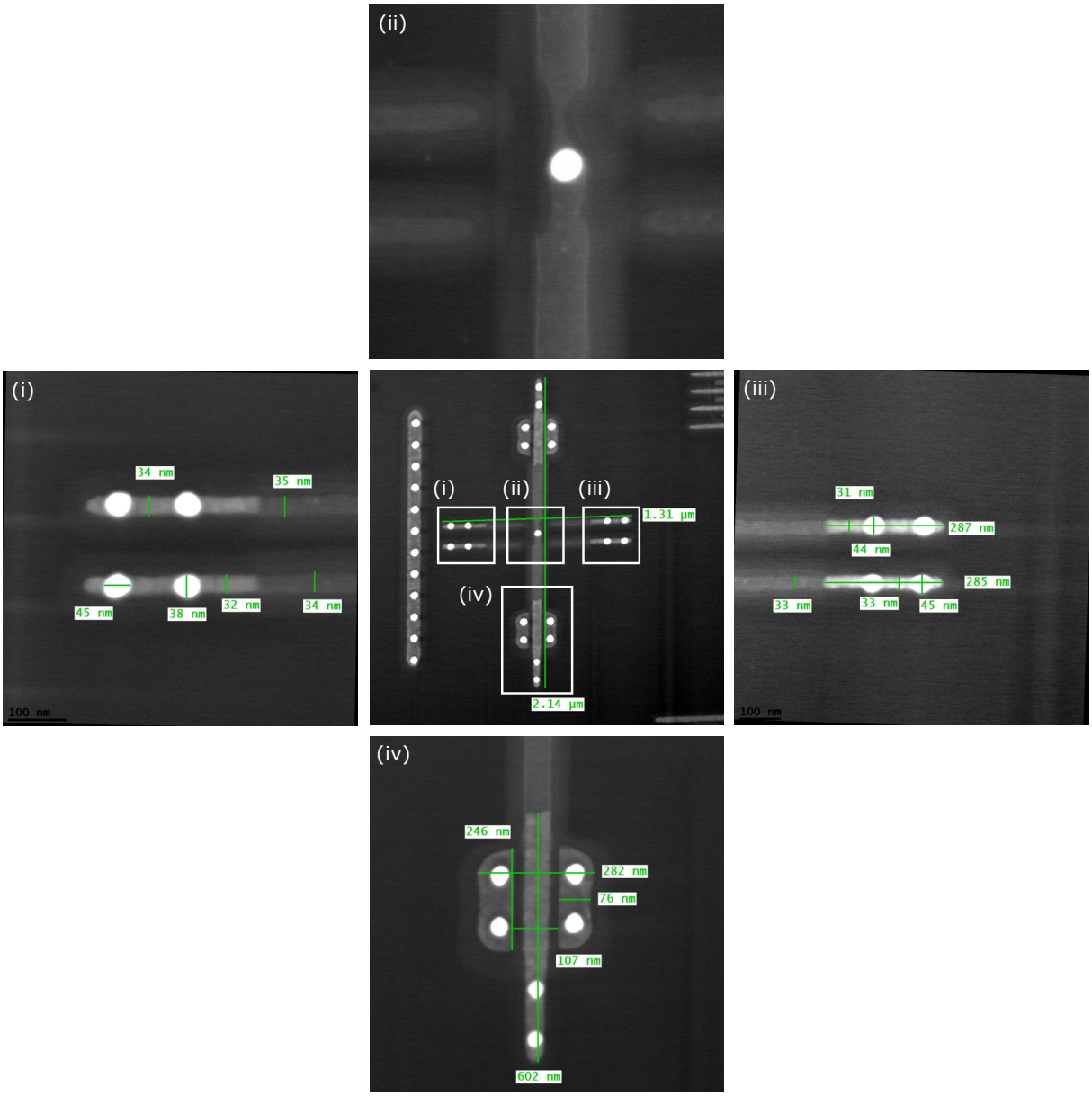


Figure 6.9 – STEM analysis performed on the second-generation fabricated split-gate device indicating that the top FGT, FGB, and DOT gates are merged with one another. A dual-beam FIB deprocessing technique was used to remove the upper layers.

The top-view inspection of the second-generation quantum dot device showed that the target pitch between the polysilicon gates designed to form the electron reservoirs and quantum dot was not reached. In fact, these three gates were fused together (Figure 6.9 (ii)), confirming the risk predictions of the OFDEC simulations. However, the pattern of the rest of the features of the device was successfully transferred to the wafer through the photolithographic process. Indeed, despite the DRC errors in the design, all the other parts were fabricated without defects, attaining the expected shape and dimensions predicted by the optical simulations. In particular, the condition to prevent silicide deposition in the cental region was met during fabrication, also achieving the contact formation on top of the DOT gate (inset (ii)). In addition, the side gates were printed correctly without

merging together despite their short distance. Also, the silicon film was correctly printed despite its narrow size. Last, the construction of the drain, source, and back gate was successful, along with the formation of all the contacts to the first interconnect layer.

In view of the overall results of the failure analysis, it became clear that due to the GAGS violations and the limitations of the OFDEC software, a reliable prediction of the eventual lithographically printed pattern was not possible. Undoubtedly, the design of the second generation of the split-gate architecture tested the limits of the 28 nm FD-SOI technology and the fabrication of the device demonstrated the desired pattern could not be successfully printed onto the wafer. However, as can be seen in Figure 6.9 (ii), the width of the merged gates varies, meaning that there is a significant variability concerning the exact shape of the device.

6.6 Device characterization

The results of the failure analysis that showed that the top gates FGT, DOT, and FGB are merged together were confirmed by the characterization of the samples. Twenty quantum dot samples were inspected in total, containing un-packaged and packaged dies. Based on the measurement protocol developed in this work, the first step towards the characterization of the device was to examine every contact and electrode of the sample for short circuits and leakage currents. These preliminary electrical characterisation tests were performed initially at room temperature and were repeated once base temperature was reached in the cryogenic system.

Indeed, during the initial investigation performed on every second-generation split-gate sample in the course of this study, a continuity was observed between the three polysilicon gates designed to form the electron reservoirs and the quantum dot. More specifically, a resistance in the range of 150 kΩ was measured between the gates, instead of a resistance in the order of a few megaohms, which is the expected value corresponding to separate electrodes. To compare with the theoretical resistance values from STMicroelectronics' DRM, the sheet resistance of the merged top gates, along with the resistance of the active region, were calculated based on the relation

$$R = \frac{\rho L}{wt}, \tag{6.2}$$

where L the gate length, t the gate thickness, w the gate width, and ρ the resistivity. For this calculation, it is noted that the exact dimensions and shape of the merged gates were estimated in approximation based on a combination of the STEM dimensional analysis and the device layout used for fabrication. For the sheet resistance of the merged top gates, this value was found to be $R_{\text{poly}} = 99.8\,\text{k}\Omega$, indicating a continuity between the polysilicon gates. For the active area, $R_{\text{active}} = 11\,\text{M}\Omega$. The latter is in agreement with the measured longitudinal resistance R_{xx} of the n-doped Hall bars presented in Chapter 4.

Nevertheless, in spite of the detected fabrication defect, the device was still usable. In this context, the characterization of the device was pursued and the rest of the gates and

ohmic contacts were inspected in order to confirm their proper functionality based on the characteristics of the 28 nm FD-SOI technology. Due to the fusion of the gates, it was possible to operate the device as a typical MOSFET and to measure its I-V characteristic curve for different bias conditions. As an example, the I-V characteristic curve of one of the characterized samples, namely Sample #1, is presented in Figure 6.10. The measurement was realized both at room and low temperature. The current flowing through the channel was measured when a voltage sweep was performed on the merged FG and DOT gates for a fixed voltage of 1 V applied to the source and a voltage step performed on the back gate. The drain and lateral gates were grounded. Indeed, at room temperature, the measured current I_{ds} was in the expected range for the given electronic configuration in an FD-SOI structure. Also, when the back gate was grounded, the threshold voltage V_{th} was identified at approximately 400 mV which was the expected value for the thick-oxide option. Moreover, a double electrostatic control over the conduction channel was observed using both the top and back gate, and the V_{th} modification by altering the V_{BG} voltage in the range of 250 mV and 500 mV was observed. In conclusion, the I-V characteristic measurement allowed to verify the accurate performance of the FD-SOI nanostructure at room temperature.

When the I-V measurement was repeated at 1.4 K, Coulomb blockade oscillations were observed (Figure 6.10 (b)) whose height and width varied as a function of the V_{FG} and V_{BG} bias voltages. In addition, the accurate performance of the FD-SOI device was verified at low temperature. Dual electrostatic control over the channel by the front and back gate was observed and, in fact, the activation of the back gate was able to shift the threshold voltage by 500 mV to lower V_{FG} values. However, it was observed that transport through the device was activated only after exceeding the polysilicon gates nominal supply voltage, i.e. 1.8 V, risking to damage the device due to the increased leakage currents.

In order to investigate further the origin and nature of these oscillations along with the different regimes of operation of the device, the current flowing through the device is measured as a function of the voltage $V_{FG\text{-}DOT}$ applied to the merged FG and DOT gates, and the voltage V_{BG} applied to the back gate. The drain and lateral gates are grounded, while an AC bias voltage signal v_{ds} is applied to the source with a fixed amplitude of 100 µV and a frequency of 17.7 Hz. In Figure 6.11, the resulting stability diagram is plotted over a large range of operation for both gates. Such experimental data require a lot of time to get selected, and as this first transport measurement was realized for investigative purposes, the resolution of the stability diagram presented here is low.

Different regimes of operation are distinguished in this large stability diagram demonstrating channel activation and tunnel barrier formation in the device. More specifically, for back gate biases lower than 4 V approximately, transport is not activated even when the maximum operating voltage, indicated by STMicroelectronics' DRM in the case of the technology used for the sample fabrication in this work, is applied to the top gate, i.e. 1.8 V. On the contrary, for higher V_{BG} values than 4 V approximately, the top merged gates act as a tunnel barrier which can be overcome when the voltage applied to the back gate is increased allowing for transport in the conduction channel to be activated. In addition, this tunnel barrier is inversely proportional to the increase of the back gate bias, leading to channel activation for lower biases on the merged gates and higher voltages on the back gate. Moreover, a set of almost parallel lines are visible in the blocked-transport

region, on the left of the oblique transition line separating this area from the activated-transport area. In order to better understand the provenance of these lines in current, higher resolution stability diagrams were extracted.

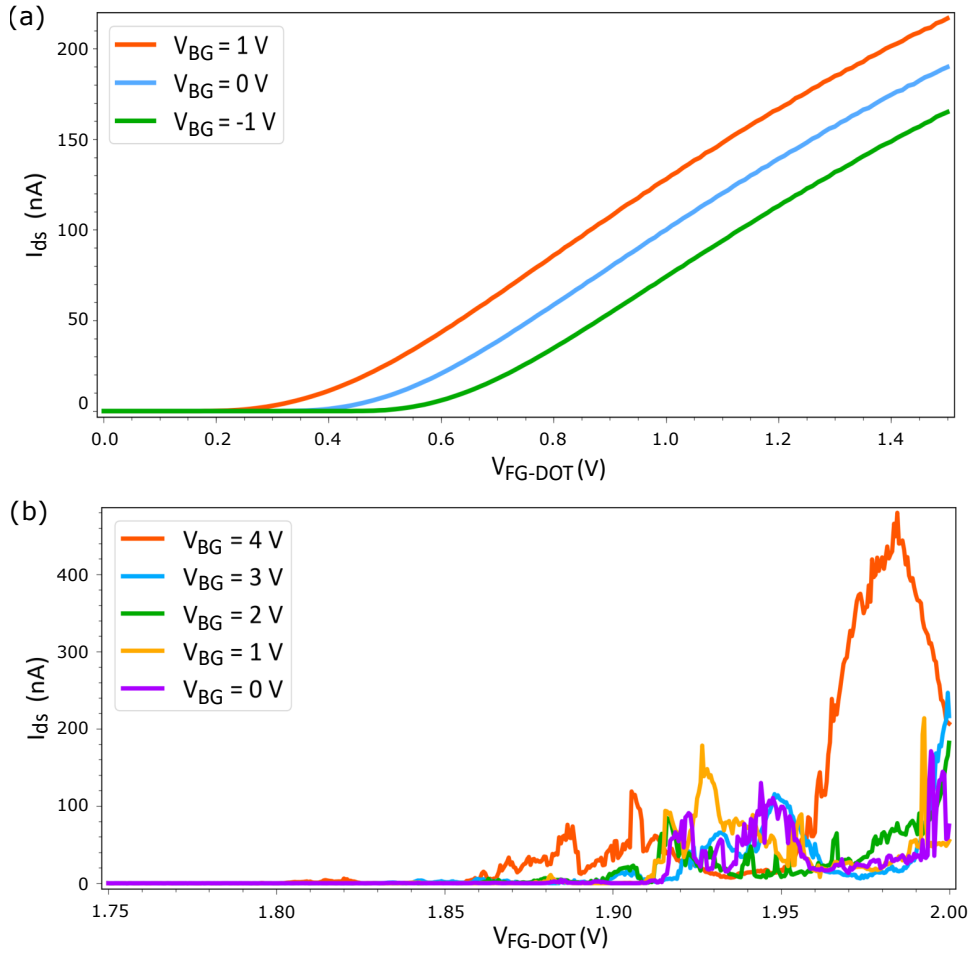


Figure 6.10 – (a) I-V characteristic curve of the second-generation device operated as a typical FD-SOI MOSFET at room temperature. The drain and the side gates were grounded. The current was measured versus the voltage applied on the merged FG and DOT gates, and the voltage on the back gate. A threshold voltage V_{th} of 400 mV was observed for 0 V on BG which was decreased for more positive V_{BG} values and increased for more negative values. (b) I-V characteristic curve at 1.4 K for the same device electrical configuration as previously. Transport is activated for voltages superior to the polysilicon gates nominal supply voltage (1.8 V). Coulomb blockade oscillations of different heights and widths are visible.

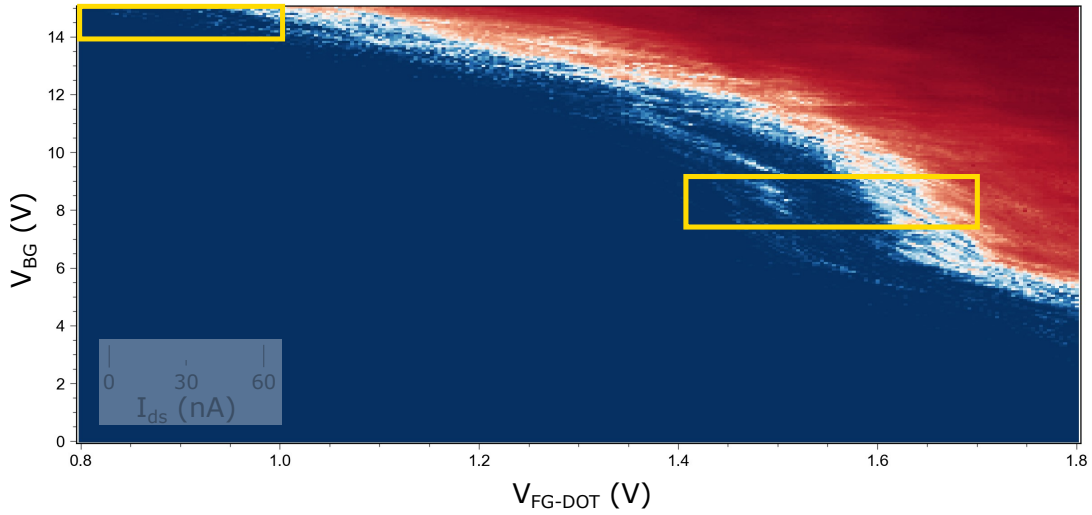


Figure 6.11 – Low-resolution stability diagram as a function of the voltages V_{BG} and $V_{FG\text{-}DOT}$ applied to the back and top merged gates showing different regimes of transport activation in the devices. The drain and the side gates are grounded. Two regions of interest are identified (shown in yellow), in which the transport measurement is repeated (See Figure 6.12).

Two regions of particular interest are identified at the top left corner, and in the middle of the diagram (shown with yellow in Figure 6.11). The transport measurement is repeated with higher resolution in these areas with the same electrical configuration for the rest of the gates and contacts of the device as previously. The measured stability diagrams are presented in Figure 6.12. In Figure 6.12 (a), it is observed that for higher back gate biases, the current lines are diagonal with respect to both V_{BG} and $V_{FG\text{-}DOT}$ axes and the spacing between them increases, indicating almost equal dependence on both the back and top merged gates. On the contrary, in the stability diagram shown in Figure 6.12 (b), the line separation is smaller and their orientation is different. For back gate biases close to 9 V, the lines become almost vertical to the V_{BG} axis, presenting a strong dependence on the back gate. After the manifestation of a kink, their orientation changes to a more diagonal to both axes, indicating dependence on both biases V_{BG} and $V_{FG\text{-}DOT}$.

Following a linecut parallel to the $V_{FG\text{-}DOT}$-axis for a given V_{BG} value, these lines correspond to the appearance of oscillations in the measured current. In fact, these oscillations resemble to the appearance of Coulomb blockade oscillations in the case of transport through a quantum dot. However, in Figure 6.12 (b), several line slopes are distinguishable, indicating the presence of more than a single quantum dot in the channel. Also, the line separation is increased for higher back gate biases, demonstrating a higher confinement in this region.

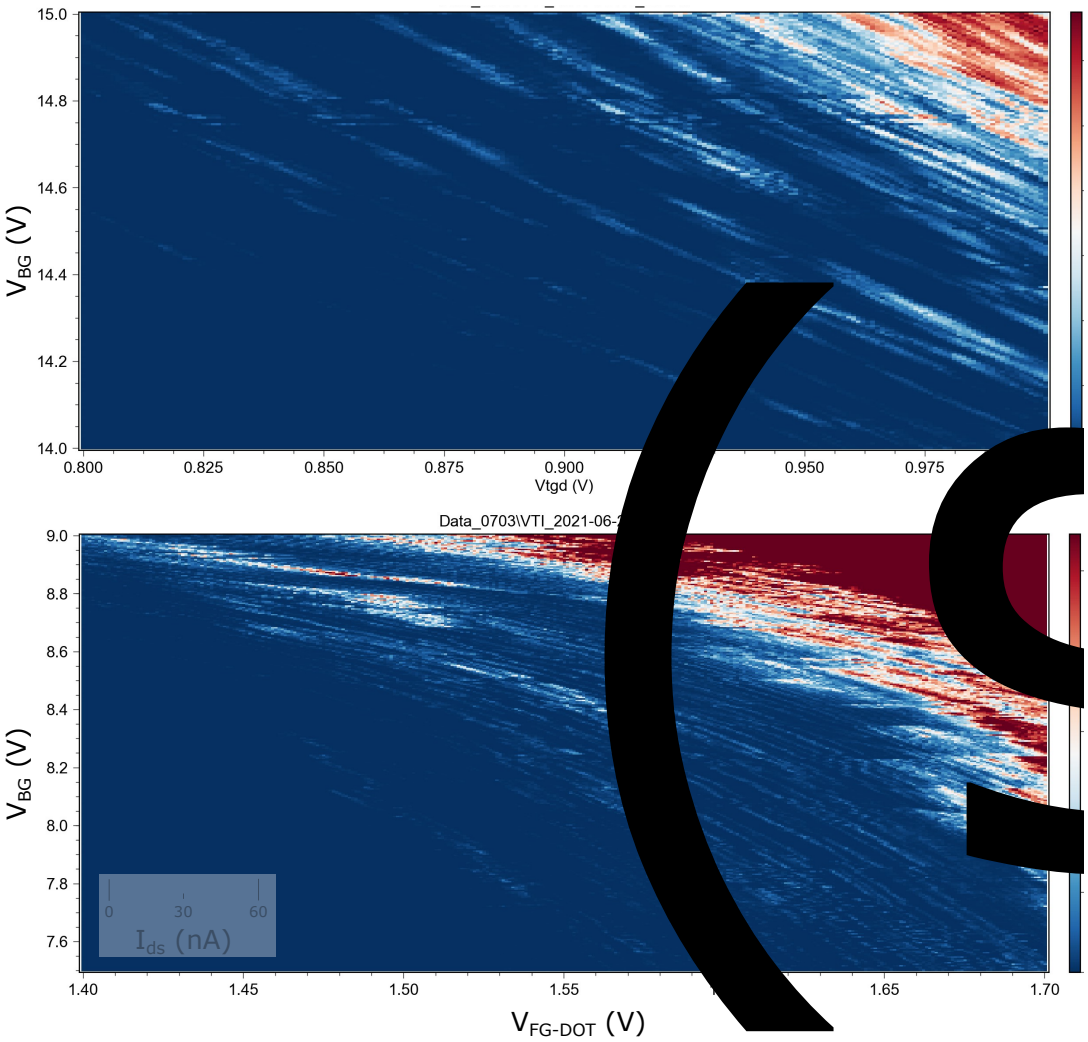


Figure 6.12 – Measurement of the current flowing through the device as a function of the voltages V_{BG} and $V_{FG\text{-}DOT}$ applied to the back and front merged gates, respectively, showing different regimes of channel activation. The drain and the side gates are grounded. (a) Transport measurement focusing on the region indicated with a yellow rectangular in the top left corner in Figure 6.11. (b) Transport measurement focusing on the region indicated with a yellow rectangular in the middle of Figure 6.11.

In order to identify the origin of the oscillations and to understand the performance of the device, Coulomb blockade spectroscopy was carried out next. However, the results were very noisy. No matter the resolution of the measurement, the limits of the Coulomb diamonds could not be identified and the characterization could not be pursued any further. For this reason, the experimental data are not presented here. In addition, the measurement results were not reproducible even when repeating the same measurement on the same device. It was discovered that the electrostatic profile was unstable and it would change significantly when the bias conditions would change. Therefore, the necessary conditions for activation and pinch-off of the channel remained undefined for this structure. In fact, the results were not reproducible for any other device characterized in the framework of this work. Last but not least, the extremely high voltages applied to

the back gate jeopardize the device. Indeed, such operation conditions have never been explored before and the eventual impact on the device remains unknown.

Due to the fusion of the top gates, their final form in the fabricated device resembles more to a disordered quantum wire than to a quantum dot island coupled to the electron reservoirs [242, 243, 244, 245, 246]. Reference [247] reports experimental observations of conductance oscillations as a function of the gate voltage from measurements performed on a narrow and unintentionally disordered channel in a silicon inversion layer, similar to the ones presented here. However, due to the impossibility to reproduce the results, no further study could be realized.

It is also worth noting that despite all careful precautions taken to avoid ESD issues, a short circuit was observed between the ohmic contacts and the front gate in 80% of the characterized samples, indicating that the nanostructures experienced irreversible damage due to electrostatic failure making impossible their operation. To address this issue, the antenna errors at the interconnect copper level were corrected in the design of the developed test chip (See Chapter 2), and the dedicated I/O ring for ESD protection is coupled to the structures.

6.7 Chapter summary

In this chapter, the exploration of the second generation of the split-gate architecture was presented. The constraints imposed by the technology node currently in use were discussed and the implementation risks of the device design, which occur if these limits are reached, were detailed. The geometry of the updated structure was analyzed, and the new features compared to the first generation were listed. The numerical results of the optical lithography and TCAD Process simulations that helped to determine the critical dimensions of the device were presented. QTCAD electrostatic simulations performed at 1.4 K on the device design permitted to precise the necessary bias conditions for channel activation and tunnel barrier modification. In addition, effective-mass Schrödinger calculations predicted the electrostatic formation of a single quantum dot under the DOT gate. In parallel, TEM and STEM-based optical investigation performed on the fabricated samples allowed the assessment of the manufacturing risks revealing that the top gates merged together during fabrication. Last, characterization of the device at room and cryogenic temperature confirmed these observations. Despite the gates fusion, the device was fully functional and Coulomb oscillations were observed, indicating the case of transport in a disordered wire instead of transport through a quantum dot island.

Conclusion and perspectives 7

Chapter 7 Conclusion and perspectives

The goal of this thesis was to investigate the potential of the standard-process 28 nm FD-SOI technology for the implementation of well-defined quantum dot spin qubit systems. In this context, Hall effect measurements were realized in 28 nm FD-SOI Hall bars at cryogenic temperatures, permitting to measure electron density and mobility. In addition, two different geometries of 28 nm FD-SOI quantum dot devices, both based on the split-gate architecture, were studied.

In Chapter 1, a brief overview of the current status of microelectronics industry, as well as the main concepts underlying quantum computing, were presented. The issue of the probable saturation of computation power in the next years was raised, along with the possible solution proposed by the emerging field of quantum computation. The advantages and progress of silicon-based spin qubits over quantum hardware alternatives were discussed next. An emphasis was placed on their CMOS compatibility, which allows to envision the exploitation of the well-matured mass-production methods from the silicon foundry industry for the fabrication of large-scale spin qubit systems. Focusing on the latter, the present challenges encountered for scaling up to large qubit numbers were presented and the importance of control and readout electronics co-integration with the qubit system is highlighted. A brief overview of the current academic and industrial landscape of the global effort in implementing an efficient quantum computer was then presented. Last, located at the interface of academia and industry, the contributions that resulted from the collaboration of Institut quantique and STMicroelectronics were identified, along with the issues that this work targets to tackle. The correspondence between the results presented in this thesis with the challenges of CMOS large-scale quantum computing was explained. Finally, the structure of the remainder of the thesis was outlined.

In Chapter 2, STMicroelectonics' standard-process 28 nm UTBB FD-SOI planar technology, used for the realization of the microstructures and nanodevices developed in this thesis, was presented, along with the different technology options that this node provides. In addition, a dedicated integration process flow for the implementation of quantum nanostructures using mass-production methods was developed and optimized throughout this study, aiming to reduce device fabrication risk and improve turnaround times. In short, as it is indicated in the proposed workflow, once the specifications of the future device are defined, the layout is then designed and tested whether it conforms to the standard-process technology design rules. Optical, geometrical and quantum simulations are performed on the test structure next using OFDEC, 3D TCAD Process, and 3D QTCAD, playing a significant role in finalizing the design. The resulting tape-out is sent for fabrication on a 300 mm multi-project wafer using photolithography at a wavelength of 193 nm in the deep UV with water immersion lenses. In fact, due to the several device ESD and latch-up issues encountered during this work, the proposed test chip design includes a seal ring, a pad ring coupled to pn-junction diodes, and a few decoupling capacitors that are added to compensate the bonding-wire parasitic effects. After fabrication, the wafer is diced, and the samples are enclosed in an IC package. Their room and cryogenic temperature characterization is realized using a direct-contact interposer. Finally, the simulation and measurement data analysis, together with a failure analysis if necessary, result in valuable feedback that is used as a basis for the implementation of the next generation of quantum devices.

In Chapter 3, an overview of the key concepts related to single quantum dots in silicon nanostructures and their performance characterization was presented. The working principle of a 2DEG and a single quantum dot was explained, as well as the constant interaction model which is used to model quantum dot systems. The weak coupling regime was also introduced, which is more relevant to the results of this thesis. The Coulomb blockade effect due to Coulomb repulsion, resulting in Coulomb blockade diamonds in the measured current or conductance across the device, was then explained, along with the sequential tunneling transport through the quantum dot. The cryogenic systems were presented next, followed by an explanation of the complete experimental setups used for the different measurements performed on the quantum dot devices. Finally, the methodology used to consistently and efficiently characterize the FD-SOI nanodevices developed in this work was described.

In Chapter 4, the cryogenic temperature characterization of Hall effect microstructures was presented, aiming to address the quality of the technology node for quantum dot applications. This is the first time, to date and to the writer's knowledge, that the electron density n_s and mobility μ of standard foundry-level 28 nm FD-SOI Hall bars at 4.2 K is measured. Double electrostatic control over the electron density n_s was achieved using both the front and back gate. More precisely, a linear increase in the density n_s was recorded in the range of approximately $2 \cdot 10^{12}$ cm^{-2} and $6 \cdot 10^{12}$ cm^{-2} when the V_{FG} bias was increased to more positive values with the back gate grounded. In addition, a less stronger impact of the back gate bias over the electron density n_s was observed. Indeed, a linear increase of the density n_s in the range of roughly $2.5 \cdot 10^{12}$ cm^{-2} and $3.5 \cdot 10^{12}$ cm^{-2} was observed, as the V_{BG} bias was increased to more positive values for a fixed voltage V_{FG} to the front gate at 1 V. It was therefore demonstrated that the back gate can be used in addition to the front gate to alter and control the electron density of the structure. This feature of double control over the electron density, due to the back gate, distinguishes the FD-SOI Hall bar structures from competitive technologies offering additional flexibility to their operation. In addition, for a device operating in the saturation regime, an electron mobility in the range of 1400 cm^2/Vs and 2200 cm^2/Vs was recorded versus the electron density n_s and the front gate bias V_{FG} with the back gate grounded. An increase in the mobility μ was observed when the back gate is polarized. Nevertheless, with a voltage of 1 V fixed at the front gate, any modification on the back gate bias V_{BG} did not lead to a significant change in the mobility, which remained almost constant at around 1700 cm^2/Vs. As a possible follow-up of this investigation, higher V_{BG} biases should be pursued for the inspection of the mobility dependence from the back gate, exceeding though the voltage limits imposed by the technology. Moreover, the Hall effect should be investigated at lower temperatures than 4.2 K, more relevant to quantum dot operations. Lastly, although the design presented in this chapter was initially realized for the study of the Hall effect for the characterization of the technology platform, it could be extended to magnetic Hall effect sensing applications.

In Chapter 5, the simulation results of the first generation split-gate device using the QTCAD modeling tool at 1.4 K were presented, and were compared to the experimental data collected from the characterization of the same device at 1.4 K. Using the Gmsh mesh generating tool, the 3D geometry of the structure was first defined and the device was then modeled with the QTCAD software. The resolution of the non-linear Poisson

equation resulted to the calculation of the conduction band profile in the device, explaining the unexpected experimental observation of channel activation using only the G2 and back gate for the rest of the gates and contacts grounded. The electrical configuration with the lateral gates activated and the back gate grounded was explored next. In these bias conditions, the non-linear Poisson equation was solved again and the conduction band profile was estimated, demonstrating energy minima in front of the gates G1 and G3. Focusing on these regions, the resolution of the effective-mass Schrödinger equation led to the numerical estimation of single electron bound eigenstates. These calculations indicate the electrostatic formation of single quantum dots in these areas and corroborate the results of the triangulation analysis carried out on the experimental data. Addressing transport through one of these side gate activated corner quantum dots, the master equation was solved to calculate the theoretical position of Coulomb blockade peaks corresponding to few-electron states, revealing the required gate bias and device geometry conditions to load a single electron into one of the dots. Finally, further analysis on the simulated tunnel barriers clarified the reason why the few-electron regime was not observed experimentally in this device, showing that narrower and lower barriers should be designed in the future.

Finally, in Chapter 6, the investigation of the second generation quantum dot device, based on the split gate architecture, was presented. Following the findings of the investigation of the first generation of the quantum dot device studied here, the constraints imposed by the 28 nm FD-SOI technology for the implementation of higher-quality quantum dot devices suitable for quantum computing applications were discussed. The implementation risks of the device design, which occur if these limits are reached, were detailed and enumerated. The geometry of the updated structure was analyzed, explaining the new features compared to the first generation and their importance. The numerical results using the OFDEC and 3D TCAD Process simulation tools were presented and the way in which they helped to determine the critical dimensions of the device is detailed. Next, QTCAD electrostatic simulations performed at 1.4 K by importing the device layout via the adaptive mesh tool permitted to precise the necessary bias conditions for channel activation and tunnel barrier modification, demonstrating that barrier control is possible through the side gates. In addition, effective-mass Schrödinger calculations permitted to estimate single-electron wavefunctions under the DOT gate, thus predicting the electrostatic formation of a single quantum dot at the desired region. However, TEM and STEM-based optical investigation performed on the fabricated samples allowed the assessment of the manufacturing risks revealing that the top gates merged with each other during the fabrication of the samples. Finally, continuity measurements performed on the device at both room and cryogenic temperatures confirmed the dimensional analysis observations demonstrating that the gates DOT, FGB, and FGT were all merged together. Despite the gates fusion, the device was characterized following the inspection methodology and was found to be fully functional. Coulomb oscillations were observed, indicating transport through a disordered wire instead of transport through a quantum dot, which was expected. Nevertheless, due to the random shape of the merged gates, the results presented in this chapter were not reproducible and the analysis was therefore not pursued on a larger amount of samples.

It is also worth noting that several of the devices and circuits that were conceived was not fabricated on time and thus could not be characterized. This was due to the long manufacturing cycle delays involved in industry-standard MPW processes. One of these uncharacterized circuits is of particular interest for co-integration and scaling up to larger number of quantum dots. More precisely, a prototype of 1D linear arrays of single quantum dots coupled to n-doped source and drain reservoirs is fabricated on the same technological platform with a capacitance bridge, conceived and designed for read-out by Ryan H. Foote from Institut quantique. The wafer was actually fabricated in the end of this project and measurements will be carried out in the future by the Ph.D. student taking over this project.

The outcome of this work has shown that the FD-SOI technology has a great potential for quantum information applications. Based on the valuable feedback from the investigation performed on the first generation of FD-SOI quantum dot devices, a new topology was conceived. The fabrication of a smaller pitch between the top polysilicon gates is required in order to form a well-defined and reproducible single quantum dot. The QTCAD simulations have shone light on the working principle of such a system. The promising results obtained from the QTCAD quantum and transport simulations of the second generation quantum dot devices demonstrated that this geometry is able to confine a single electron and implement a spin qubit. The updated test structure reached however the physical and technical limits of the 28 nm FD-SOI technology. For the fabrication of this design, certain design rule violations and manufacturing risks were unavoidable. The fabrication though of such a device, based exclusively on industry-standard process methods, was realized for the first time in STMicroelectronics and tested the limits of the 28 nm node. Despite the partial resulting success on avoiding the manufacturing risks that was reported, it was demonstrated by optical inspection and electrical characterization carried out on the samples, that the 28 nm technology node is not suitable for the 300 mm MPW realization of well-defined quantum dot spin qubits using only foundry-level techniques. The results reported in this thesis demonstrate the strengths of the FD-SOI technology, along with the identified limitations of the 28 nm node, and prepare the ground for the implementation of the next generation of quantum dot devices designed and fabricated using smaller industry-standard process UTBB FD-SOI technology nodes. The integration process flow presented in Chapter 2 can be extended for the realization of FD-SOI quantum dot devices based on smaller technology nodes, such as 22 nm, 18 nm and the soon-to-be-developed, 10 nm UTBB FD-SOI. In fact, the 18 nm process uses the same fabrication equipment as the 28 nm node and is currently under development at STMicroelecronics targeting full production by 2024.

Patents and publications

Journal papers

- Interpretation of 28 nm FD-SOI quantum dot transport data taken at 1.4 K using 3D Quantum TCAD simulations. **I. Kriekouki**, F. Beaudoin, P. Philippopoulos, C. Zhou, J. Camirand Lemyre, S. Rochette, S. Mir, M. Barragan, M. Pioro-Ladriere and P. Galy. *Solid-State Electronics* **194**, 108355, 2022

- Robust technology computer-aided design of gated quantum dots at cryogenic temperature. F. Beaudoin, P. Philippopoulos, C. Zhou, **I. Kriekouki**, M. Pioro-Ladriere, H. Guo and P. Galy. *Applied Physics Letters* **120**, 264001, 2022

- Understanding conditions for the few-electron regime in 28 nm FD-SOI quantum dots: interpretation of experimental data with 3D quantum TCAD simulations. **I. Kriekouki**, F. Beaudoin, P. Philippopoulos, C. Zhou, J. Camirand Lemyre, S. Rochette, C. Rohrbacher, S. Mir, M. J. Barragan, M. Pioro-Ladriere and P. Galy (in press)

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Patent

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