An Accurate Ultra-low Current Measurement ASIC for Ionization Chamber Readout

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by

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Declaration

I, Sarath Kundumattathil Mohanan, hereby declare that the thesis is written independently and without making use of aids other than those indicated. Any part of the content that is taken up from other sources are marked and properly acknowledged. The produced or any other version of the thesis is not previously submitted to another university.

The thesis work was conducted from 2018 to 2021 under the supervision of Prof. Dr. rer. nat. Ullrich R. Pfeiffer at the University of Wuppertal and Dr.Hamza Boukabache at CERN. This work was fully funded under the Doctoral Student Program of CERN.

Wuppertal, August 2021

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List of Abbreviations

Abbreviation	Meaning
ACCURATE	Atto to miCro CoURAnt meTEr
AD	Antiproton factory
ADC	Analog to digital convertor
ALICE	A Large Ion Collider Experiment
AMS	Austriamicrosystems
ARCON	ARea CONtroller
ASIC	Application specific integrated circuit
ATLAS	A Toroidal LHC Apparatus
BIC	Beam interlock controller
BIS	Beam interlock system
BJT	Bipolar junction transistor
BLM	Beam loss monitor
CB	Charge balancing
CC	Current conveyor
CERN	European Organization for Nuclear Research
CFC	Current to frequency conversion
CHUV	Lausanne university hospital
CLEAR	CERN Linear Electron Accelerator for Research
CMOS	Complementary metal-oxide-semiconductor
CMS	Compact Muon Solenoid
COTS	Commercial off-the-shelf
CPU	Central processing unit
CROME	CERN Radiation Monitoring Electronics
DAC	Digital to analog convertor
DC	Direct current
DRC	Desing rule check
DSM	Direct slope measurement
ESD	Electrostatic discharge
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference

FC	Folded Cascode
FCC	Future Circular Collider
FDSOI	Fully depleted silicon-on-insulator
FET	Field-effect transistor
FIFO	First-in first-out
FPGA	Field-programmable gate array
GPIB	General Purpose Interface Bus
I2C	Inter integrated circuit
IC	Integrated circuit
IHP	Leibniz Institute for High Performance Microelectronics
IO	Input-output
IRA	Institute of radio physics
JFET	Junction field-effect transistor
LEIR	Low energy ion ring
LHC	Large hadron collider
LHCb	LHC-beauty
LINAC	Linear accelerator
LSB	Least significant bit
LVS	Layout vs schematic
MATLAB	Matrix laboratory
MEMS	Microelectromechanical systems
MIM	Metal-insulator-metal
MPS	Machine protection system
NMOS	N-type metal-oxide-semiconductor FET
OPAMP	Operational amplifier
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PLC	Programmable logic controller
PMOS	P-type metal-oxide-semiconductor FET
PPS	Personal protection system
PS	Proton synchrotron
PSAIF	Proton Synchrotron - Antiproton collector Irradiation Facility
PSB	Proton synchrotron booster
RAMSES	RAdiation Monitoring System for the Environment and Safety
REMUS	Radiation and Environment Monitoring Unified Supervision
RC	Reset counting
RF	Radio frequency
RP	Radiation protection
RTL	Register-transfer level
SAR	Successive-approximation-register
SCADA	Supervisory Control and Data Acquisition

SIL	Safety integrity level
SoC	System-on-a-chip
SPI	Serial peripheral interface
SPS	Super proton synchrotron
SRAM	Static random-access memory
TIA	Transimpedance amplifier
TSMC	Taiwan Semiconductor Manufacturing Company
UART	Universal Asynchronous Receiver Transmitter
USB	Universal serial bus
UTOPIA	Ultra-low picoammeter
VHDL	Very High Speed Integrated Circuits Hardware Description Language

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Publications

1. **S. K. Mohanan**, H. Boukabache, D. Perrin, and U. R. Pfeiffer, "Comparative Analysis of Ultra-Low Current Measurement Topologies with Implementation in 130 nm Technology", IEEE Access, vol. 9,pp. 63 855–63 864, 2021
2. **S. K. Mohanan**, H. Boukabache, D. Perrin, and U. Pfeiffer, "Femtoampere sensitive current measurement ASIC in 22 nm technology", in 2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), IEEE, Oct. 2019, pp. 1–3
3. **S. K. Mohanan**, H. Boukabache, D. Perrin, and U. Pfeiffer, "Towards the next generation of CERN radiation monitoring front end ASICs", in Topical Workshop on Electronics for Particle Physics (TWEPP), 2021
4. **S. K. Mohanan**, H. Boukabache, V.Cruchet, D. Perrin, S.roesler, and U. Pfeiffer, "An Ultra Low Current Measurement Mixed-Signal ASIC for Radiation Monitoring Using Ionisation Chambers", IEEE Sensors Journal,vol. 22,pp. 2142–2150, 2021
5. K.Ceesay-Seitz, **S. K. Mohanan**, H. Boukabache, and D. Perrin, "Formal Property Verification of the Digital Section of an Ultra-Low Current Digitizer ASIC", in The Design and Verification Conference and Exhibition Europe (DVCon Europe), 2021

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Contributions of Others

1. The thesis presents the design of a current measurement ASIC to be used as the front-end of ionisation chambers. The ASIC was designed in line with the ASIC development program taken up by the Radiation Protection group at CERN. The first two ASICs in this program - UTOPIA 1 and UTOPIA 2 was designed by a previous colleague Evgenia Voulgari. The ASICs presented in this thesis - ACCURATE, forms the next generation of the UTOPIA ASICs. The various circuit blocks designed for UTOPIA in AMS 350 nm technology were redesigned in GF 22FDX and TSMC 130 nm technology and used in this thesis.
2. The IO pads with ESD cells and custom standard cells used in ACCURATE 1 and ACCURATE 2 were designed by Stephano Michelis and Giacomo Ripamonti of EP-ESE-ME section of CERN.
3. The verification of the digital logic of ACCURATE 2M was done by my colleague - Katharina Ceesay-Seitz.
4. The ASICs were bonded by Florentina Manolescu of the bond lab at CERN.
5. The test board for ACCURATE 2M and its MATLAB test scripts were designed by Vassili Cruchet.

The research not included in the above list has been conducted by myself.

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Abstract

CERN houses one of the most sophisticated pieces of machinery ever built by humans to carry out cutting-edge research in the field of particle physics. The experiments carried out at CERN can generate different kinds of ionizing radiation as a side effect. Using dedicated radiation monitors, the radiation protection (RP) group ensures that the generated radiation is contained within the allowable limit and thrusts to minimize the exposure which ensures the safety of the personnel and surrounding habitants. Ionization chambers are the most used sensors for continuous radiation monitoring for RP. This thesis explains the design, development, and characterization of an application specific integrated circuit (ASIC) that aims to replace the existing discrete component-based front end of ionization chambers used at CERN.

The presented research started with the in-depth characterization of the first-generation ASICs designed in the RP group - UTOPIA. Measurements with pulsed radiation fields exposed the limitation of UTOPIA for efficient collection of charge pulses necessitating the need for a redesign with architectural modification. Apart from capacitating the analog front end for improved charge measurement, integrating the digital data processing section into the ASIC to create a mixed-signal, single-chip solution was also envisaged. UTOPIA ASICs were designed in AMS 350 nm technology which exhibited femtoampere leakages which were vital in achieving the ultra-low current measurement capability. The main hurdle faced in designing the second generation of the ASIC – ACCURATE, was identifying a suitable long-term replacement for the proven 350 nm node. A detailed literature review ascertained that no design is reported in technology nodes of 130 nm or finer that achieves femtoampere sensitivity and attains the dynamic range from femtoampere to microampere. Test structures made in 22FDX of GLOBALFOUNDRIES and TSMC 130 nm technology established techniques and architectures to attain the required dynamic range and sensitivity.

Design of ACCURATE 2, which is the main focus of the research, is presented in detail. An architecture combining two current measurement methods, charge balancing current to frequency conversion and direct slope measurement method, was designed. It also incorporates all the digital logic along with the analog section to process the generated data and provide data storage and eventual transfer to an external system through a serial interface. The ASIC is successful in achieving a remarkable sensitivity of 200 aA and demonstrated a wide dynamic range from around -6 fA to -20 µA. The use of thick gate transistors in the leakage critical analog path, optimal feedback capacitance and three stepped progressive charge balancing with 500 fC,

1 pC, and 4 pC charge paths helped in achieving this performance. Prudent floorplanning utilizing Deep N-Well structures to minimize noise coupling along with guard rings and path length matching helped in attaining the sensitivity even with the mixed signal version. The ASIC occupies an area of 3.52 mm^2 and reports a total power consumption of 17.4 mW.

Characterization with the continuous current generated by different kinds of ionization chambers when exposed to radiation sources demonstrated the dose rate measurement of the ASIC from 5 µSv/h to 7.4 Sv/h. Dynamic characterization with pulsed radiation established the improvement of around 16% more charge collection by ACCURATE 2 compared with UTOPIA 2 for a charge pulse of 100 nC. The reason for the limitation in charge collection for charges above tens of nanocoulombs was identified to be caused by saturation of OTA with the high influx of charges beyond that could be compensated by the charge balancing block. The improvement achievable by increasing the time constant of the charge collection path was demonstrated.

The designed ASIC thus improves the sensitivity, dynamic range and charge measurement efficiency of the existing systems and offers a first of its kind mixed-signal single chip solution for ionization chamber frontends. The ASIC can also be employed in applications such as biosensor readouts and device characterization which demands similar performance levels.

ACCURATE 2 must be upgraded from a prototype to a certified reliable unit for the next generation of radiation monitors for CERN. The path culminating in ACCURATE 3 with different improvements and modifications is also laid out.

Zusammenfassung

Das CERN, die Europäische Organisation für Kernforschung, beherbergt eine der ausgeklügeltsten Anlagen, die je von Menschen gebaut wurden und betreibt Spitzenforschung auf dem Gebiet der Teilchenphysik. Die am CERN durchgeführten Experimente können verschiedene Arten von ionisierender Strahlung als Nebenprodukt erzeugen. Mit Hilfe von speziellen Strahlungsmonitoren stellt die Strahlenschutzgruppe (Radiation Protection Group, RP) sicher, dass die erzeugte Strahlung innerhalb der zulässigen Grenzen bleibt. Sie bemüht sich, die Exposition von Personen zu minimieren, um die Sicherheit des Personals und der Bewohner der umliegenden Gebiete, zu gewährleisten. Ionisationskammern sind die von der RP am häufigsten verwendeten Sensoren zur Messung der Strahlungsniveaus. Diese Arbeit beschreibt den Entwurf, die Entwicklung und die Charakterisierung eines ASICs, das das bestehende, auf diskreten Komponenten basierende Frontend der Ionisationskammern am CERN ersetzen soll.

Die Forschungsarbeiten begannen mit der eingehenden Charakterisierung der ASICs der ersten Generation - UTOPIA -, die in der Strahlenschutzgruppe entwickelt wurden. Messungen mit gepulsten Strahlungsfeldern zeigten die Grenzen von UTOPIA bei der effizienten Erfassung von Ladungspulsen auf, so dass ein Neuentwurf mit architektonischen Änderungen erforderlich wurde. Das analoge Frontend sollte mit einer verbesserten Fähigkeit zur Ladungsmessung ausgestattet werden. Darüberhinaus wurde auch die Integration der digitalen Datenverarbeitung in das ASIC ins Auge gefasst, um eine Mixed-Signal Lösung in einem einzigen integrierten Chip zu ermöglichen. Die UTOPIA-ASICs wurden in der AMS-350 nm-Technologie entwickelt. Diese wies Leckströme im Femtoampere-Bereich auf, was für die Erzielung der Messfähigkeit von extrem geringen Strömen entscheidend war. Die größte Hürde bei der Entwicklung der zweiten Generation des ASICs - ACCURATE - war die Suche nach einem geeigneten langfristigen Ersatz für die bewährte 350 nm-Technologie. Eine ausführliche Literaturrecherche ergab, dass für Technologieknoten von 130 nm oder feiner kein Design bekannt ist, das eine Femtoampere-Sensitivität und einen Dynamikbereich von Femtoampere bis Mikroampere erreicht. Basierend auf Teststrukturen, die in der 22FDX Technologie von GLOBALFOUNDRIES und in der 130 nm Technologie von TSMC entworfen wurden, konnten Techniken und Architekturen entwickelt werden, die den geforderten Dynamikbereich und die geforderte Sensitivität erreichen.

Das Schaltungsdesign von ACCURATE 2, das den Schwerpunkt der Forschung bildet, wird im Detail vorgestellt. Es wurde eine Architektur entwickelt, die zwei Strommessmethoden kombiniert, nämlich die Strom-Frequenz-Wandlung mit Ladungsausgleich und die Methode der direkten Steigungsmessung. Zusätzlich zu der analogen Schaltung umfasst das Design auch die gesamte digitale Logik, welche die erzeugten Daten verarbeitet, und eine Möglichkeit zur Datenspeicherung und eventuellen Übertragung an ein externes System über eine serielle Schnittstelle bietet. Das ASIC erreicht eine bemerkenswerte Sensitivität von 200 aA und demonstriert einen weiten Dynamikbereich von etwa -6 fA bis -20 µA. Der Verbesserungen wurden durch die Nutzung von Transistoren mit dickem Gate-Oxid, die optimale Auslegung der Rückkopplungskapazität, sowie eine Architektur mit dreistufigem Ladungsausgleich mit unterschiedlichen Ladungsmengen (500 fC, 1 pC, und 4 pC) erreicht. Durch ein detailliertes Floorplanning, die Integration von Deep N-Well Strukturen zur Minimierung der Rauschkopplung ins Substrat und den Abgleich von Pfadlängen konnte die Sensitivität selbst in der Mixed-Signal-Version beibehalten werden. Das ASIC nimmt eine Fläche von 3,52 mm^2 ein und hat eine Gesamtleistungsaufnahme von 17,4 mW.

Bei der Charakterisierung mit Gleichstrom, der von verschiedenen Arten von Ionisationskammern durch Bestrahlung mit Strahlungsquellen erzeugt wurde, zeigte die Dosisleistungsmessung des ASICs 5 µSv/h bis 7,4 Sv/h. Bei der dynamischen Charakterisierung mit gepulster Strahlung wurde festgestellt, dass ACCURATE 2 im Vergleich zu UTOPIA bei einem Ladungspuls von 100 nC etwa 16% mehr Ladungen sammelt. Es wurde identifiziert, dass Ladungsmengen über zehn Nanocoulomb zu einer Sättigung des OTAs führen, welche durch den Ladundsausgleich nicht kompensiert werden können. Durch eine Erhöhung der Zeitkonstante in dem Pfad zur Ladungsakkumulation konnte diesbezüglich eine Verbesserung nachgewiesen werden. Der entworfene ASIC verbessert somit die Empfindlichkeit, den Dynamikbereich und die Effizienz der Ladungsmessung im Vergleich zu den bestehenden Systemen und ist die erste vollständig integrierte Mixed-Signal-Lösung für die Ionisationskammersensorik. Der ASIC kann auch in Anwendungen mit ähnlichen Leistungsanforderungen eingesetzt werden, wie zum Beispiel in der Biosensorik und in der hochpräzisen Messtechnik. Um den entworfenen ASIC für die nächste Generation von CERN´s Strahlungsmessgeräten verwenden zu können, muss es von einem Protoypen in ein zuverlässiges und zertifiziertes Bauteil überführt werden. Abschließend wird der Weg zur Entwicklung von ACCURATE 3 mit verschiedenen Verbesserungen und Modifikationen dargelegt.

Chapter 1

Introduction

CERN, the European Organization for Nuclear Research, is a unique research facility designed to understand the basic constituents of matter by colliding particles traveling at a high speed. A series of accelerators have been built at CERN to push the particles to almost the speed of light. An overview of the accelerator complex at CERN is shown in Fig. 1.1.

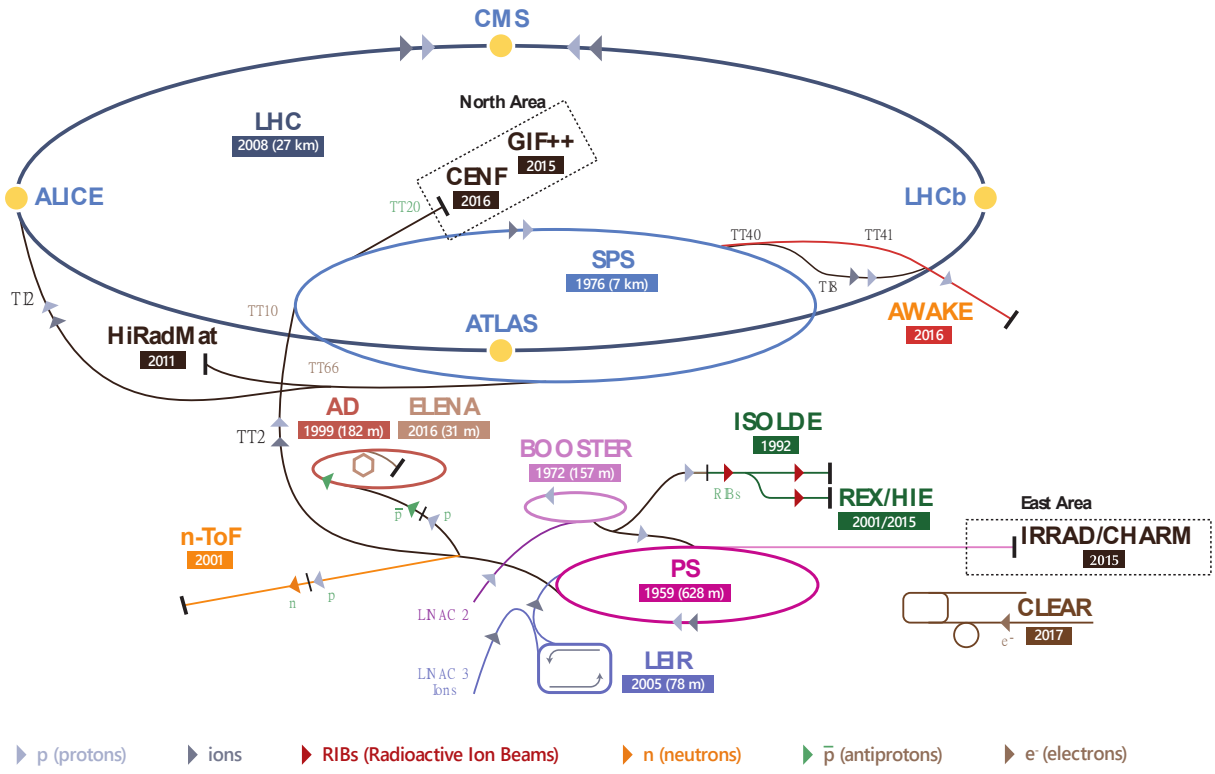

Figure 1.1: CERN's Accelerator Complex [1]

CERN accelerates protons and ions in its accelerators. The path of the protons starts from a bottle of hydrogen from which the protons are extracted and fed to LINAC 2, the first accelerator. Here, the protons are accelerated to an energy of 50 MeV. The beam then traverses the proton synchrotron booster (PSB) where the beam energy level increases to 1.4 GeV, the

proton synchrotron (PS) pushing the energy further to 25 GeV, and the super proton synchrotron (SPS) with a target energy of 450 GeV, before reaching the large hadron collider (LHC). The final energy level achieved in the LHC is 6.5 TeV. The ions make their journey from vaporized lead through LINAC 3 and the low energy ion ring (LEIR) before entering the PS. There are two beam pipes for the LHC, where the beams travel in opposite directions. The beams are made to collide in four detectors – ALICE, ATLAS, CMS, and LHCb. The total energy at these collision points equals 13 TeV.

1.1 Need for radiation monitoring

When the particle beams collide or when they hit a target, different kinds of ionizing radiation are created, as shown in Fig. 1.2. This created secondary field, called stray radiation, is different from the ionizing radiation observed in the nuclear industry in terms of composition, energies, and temporal dynamics. The energy of the created radiation is reduced to a great extent by the shielding provided around such facilities thus containing the radiation within the beam tunnel. Hence, when the accelerators are on, access to the tunnel or experimental area is forbidden. The ambient dose equivalent in these areas is monitored. Depending on the collision energy, the material around the collision area or the target might be activated, resulting in stray radiation even after the accelerators have been switched off. Using dedicated monitors, the level of radiation in all of the risk areas is continuously monitored and only when the levels are below the safety threshold is access re-enabled.

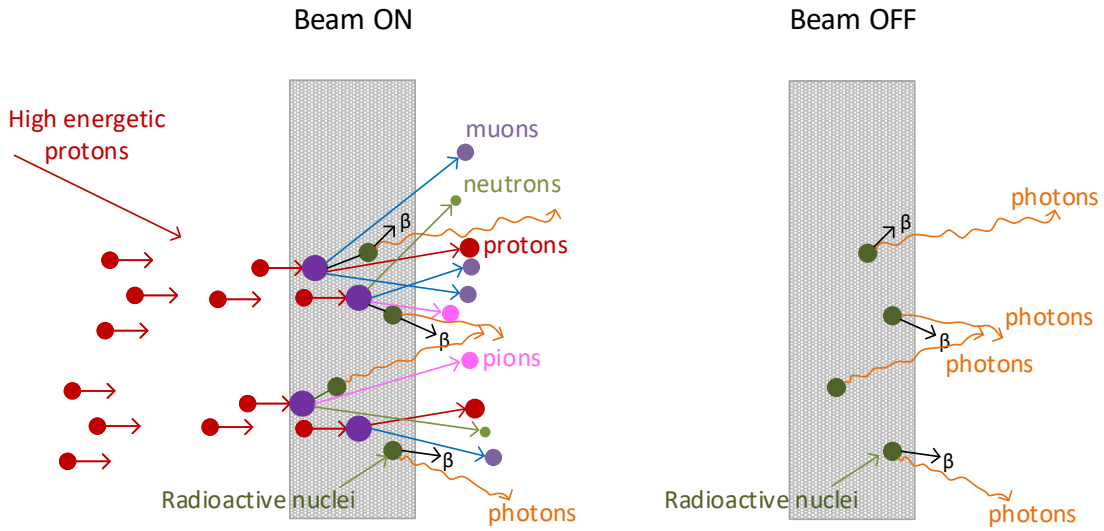

Figure 1.2: Creation of radiation by particle accelerators [2]

For each facility of the accelerator complex and experiments at CERN, there exists a very complex network of interconnected systems that offer various levels of protection. The three main objectives of these systems are: 1. Protecting people from different threats such as radiation exposure, 2. protecting the environment, and 3. protecting the machine [3]. A highly reliable

personal protection system (PPS) is entrusted with the responsibility of protecting the people operating the experiments and in the vicinity.

For the sophisticated accelerators to which damage should be avoided at all costs due to their inherent complexity and the magnitude of the energy involved, the use of a machine protection system (MPS) is also of paramount importance. Specifically, in the case of LHC, a SIL3 (safety integrity level) classified MPS [4] protects the LHC and the associated systems. The main objectives of the MPS are to protect the machine, protect the beam, and provide evidence [5]. The heart of the MPS is a beam interlock system (BIS). In the event of an incident that necessitates the beam being aborted, the beam interlock system communicates with the beam dump system and the beam will be safely directed to a dump. For the LHC, as many as around 10000 electronic channels could request a beam dump [6]. The architecture of the beam interlock system for the LHC is described in detail in [5]. The beam interlock system comprises 16 beam interlock controllers (BIC) which act as the backbone for protecting the LHC against any beam loss related damage. Each BIC can receive up to 14 signals from various systems [7]. One of the main protection systems that interfaces with the BIS is comprised of the beam loss monitors (BLMs) [8], [9]. Some 3600 detectors of the BLM system are installed along the cryostats of the LHC machine and at other critical locations where protons are lost from the beam and hit surrounding material. Beam losses are prone to occur at collimation, injection, and extraction points, as well as along the beam pipes. Any event that could lead to high radiation is immediately detected by the BLMs and the BIS interlock is triggered immediately.

While the beam loss monitors act as the first line of defense protecting against unintentional radiation, separate radiation monitors from the radiation protection (RP) group are also installed close to the LHC ring as well as at various crucial points. The main objective of the RP radiation monitors is to provide protection to people rather than the machine itself. Thus, it is part of the PPS and not the MPS. The operational philosophy of the LHC keeps the PPS and MPS systems separate. However, all radiation events are recorded by the RP radiation monitors and appropriate alarms are raised when the threshold is exceeded.

In the case of other complexes, such as the SPS, RP radiation monitors are interfaced also to the beam interlock system. Thus, apart from generating alarms and recording events, they can interrupt the beam through the BIS. A block diagram of the path from the radiation monitor to the SPS BIS [10] is shown in Fig. 1.3.

The interlock signals from different radiation monitors are collected in a junction box which then redirects the interlock to the BIS through a user interface. The junction interface also allows different logic operations on the received interlocks. Apart from the scenario where the measured radiation field is above the set threshold, if any of the systems are not powered or not in the right operational mode, an interlock signal is triggered according to the fail-safe operating principle.

The radiation protection system thus ensures a safe environment for the people working on site and for the general public by protecting against any unjustified exposure to ionizing radiation.

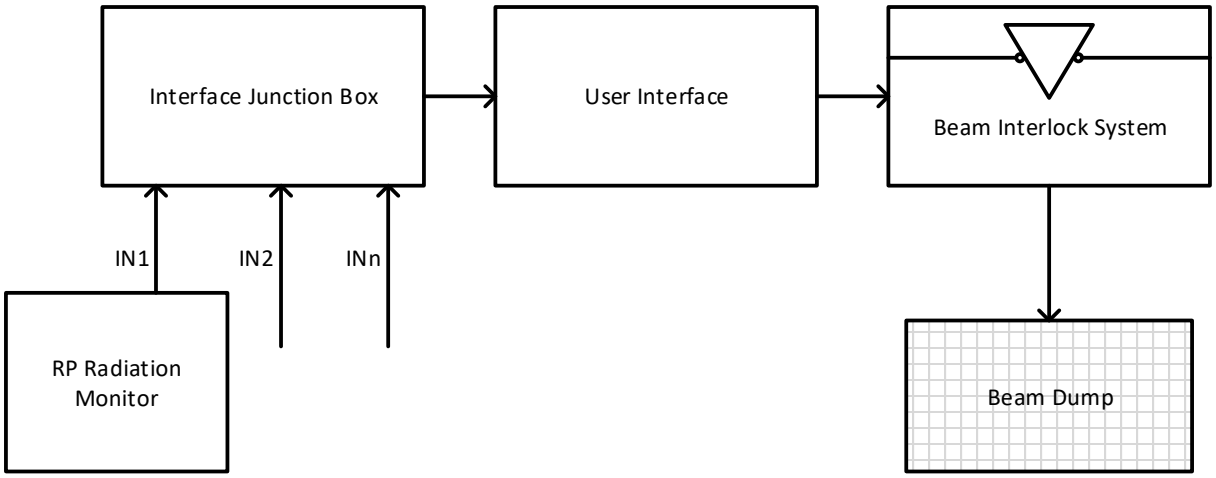

Figure 1.3: SPS BIS interface

The three main functionalities of the system are detection and measurement of radiation levels, generating alarms and interlocks, and finally logging the recorded data for the long term.

1.2 Radiation monitoring system

The typical components of a radiation monitoring system are shown in Fig. 1.4. The ionizing radiation is detected by an ionization chamber which produces a current proportional to the received radiation dose rate.

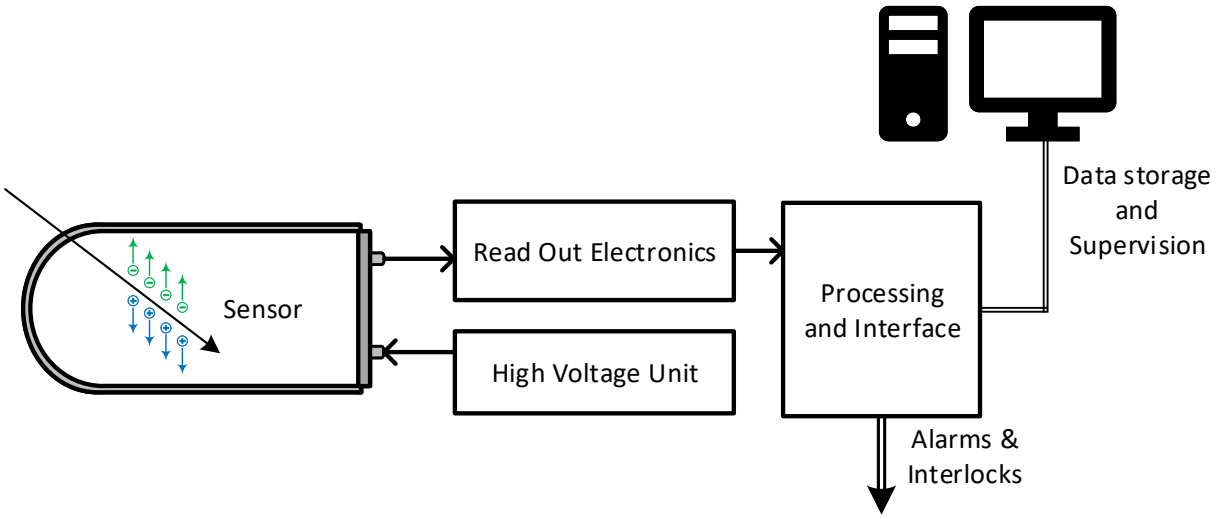

Figure 1.4: Radiation monitoring system

In order to bias the sensor, a high voltage generation unit generates the required voltage depending on the type of chamber used. The generated current is measured by a front-end electronics system. The readout unit converts the current into a digital format which is further processed by a digital section. The processing unit transfers the measured data to a supervision

system and to storage. Depending on the set thresholds and measured dose rate, alarms or interlocks could be generated by the processing system.

1.2.1 Ionization chambers

Ionization chambers are the ubiquitous choice of sensor in radiation monitoring as they are sensitive to different kinds of particles. The chamber is filled with gas and has two electrodes – an anode and a cathode. The gas gets ionized by incident radiation generating electron–ion pairs. The anode which forms the collecting electrode receives the electrons and is connected to the readout electronics. The cathode is applied with the high voltage which determines the region of operation of the chamber.

There are four characteristic regions for a gas filled detector [11] depending on the applied voltage. The first one is a recombination region, where the applied voltage is not high enough and hence the majority of the generated electron–ion pairs are lost by recombination. As the voltage increases beyond a certain threshold, the electric field is high enough to have a significant amount of charge collection by the chamber. This region, called the ionization chamber region, is characterized by a constant charge generation by the chamber for a defined range of applied voltage. As the name suggests, this is the most favorable region of operation for the ionization chamber. The third region of operation is the proportional region, where the generated charges are proportional to the applied voltage. After this region, any increase in the applied voltage places the chamber in the Geiger–Muller region, which is the favored regime for Geiger–Muller counters. For the ionization chambers used at CERN, each chamber is characterized at dedicated facilities and the voltage range to be used in the ionization chamber region for maximum efficiency is determined.

Different kinds of ionization chambers are used at CERN depending on the environment. The three main types are explained further.

1.2.1.1 Centronic IG32

IG32 is argon filled with at a pressure of 3.1 bar. The electrode arrangement follows alternate anode and cathode combs along the center of the chamber, thus allowing for faster collection of charges. The typical dose rates encountered for this chamber are from 1 µSv/h to 1 Sv/h. The nominal bias voltage is -1500 V.

1.2.1.2 PTW PMI T32006

The PMI is a plastic ionization chamber manufactured by PTW-Freiburg specifically for CERN. The construction details of the chamber are shown in Fig. 1.5. It is filled with air at 1 atmospheric pressure. Since these plastic chambers will not be activated by the created radiation, they are installed inside the tunnel for monitoring the radiation dose when the beam is on and to record the residual dose when the accelerators are stopped. The chamber is biased usually with a voltage of -400 V. The PMI chambers are used for measuring doses from 0.5 µSv/h to 10 Sv/h.

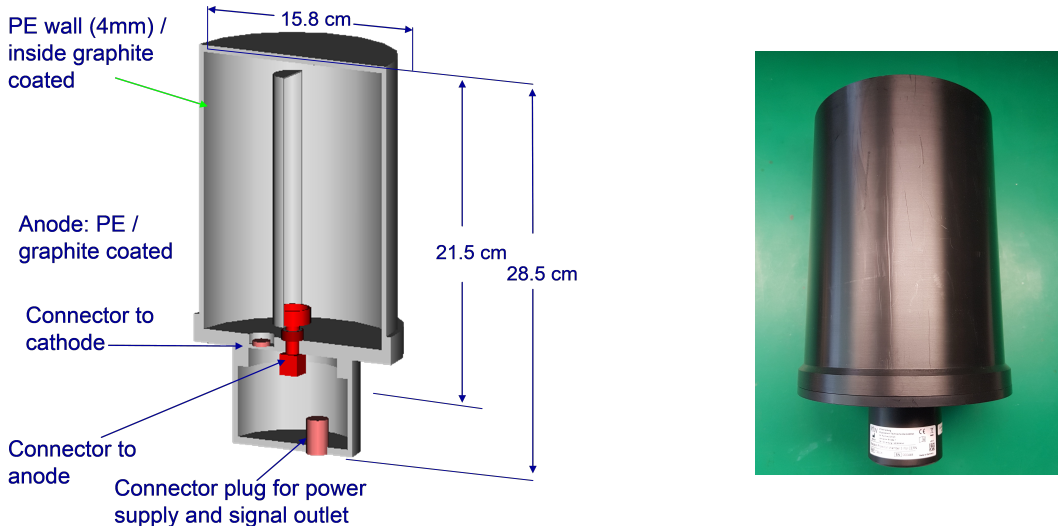

Figure 1.5: PTW PMI T32006 chamber [12]

1.2.1.3 Centronic IG5

IG chambers are steel shelled detectors manufactured by Centronic limited. The internal structure is shown in Fig. 1.6. Depending on the radiation field, either Hydrogen filled (IG5 H20) or Argon filled (IG5 A20) chamber is used. Both chambers have a volume of 5.2 l pressurized at 20 bars. The electrodes are arranged in the center of the chamber and along the envelope. They are used for dose rate measurements from 50 nSv/h to 0.1 Sv/h and are normally biased with a voltage of -1000 V.

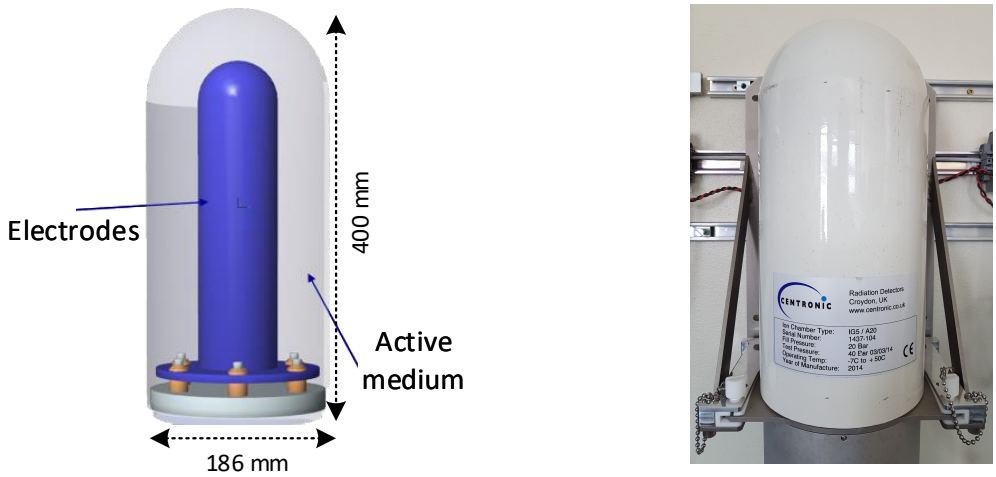

Figure 1.6: IG5 chamber [12]

It is thus clear that the range of current generated by these ionization chambers varies a lot. The current generated by the IG5 H20 chamber, when used for detection of neutrons, can be as low as

a few femtoamperes [13]. The radiation expected by the PMI chambers could be of the order of 10 Sv/h, resulting in a current of around 250 nA. An IG5 A20 chamber, when exposed to a similar radiation dose, can generate currents higher than 10 µA. Also, another requirement specifies the capability of measuring charges up to 500 nC within a pulse of milliseconds duration. The pulse width of the output of the ionization chamber depends on the time constant of the interface circuit. The output pulse of a typical chamber, when observed with an oscilloscope with characteristic impedance, exhibited pulse widths of 50 to 100 ms with the majority of the charge concentrated in the initial few milliseconds. Hence, the peak current could also be beyond 10 µA. The measurement electronics should be able to cater to this wide dynamic range from femtoamperes to tens of microamperes.

1.3 Motivation for the research and thesis organization

The unavailability of commercial products which would demonstrate this dynamic range was the driving force for undertaking in-house development of radiation monitoring systems. The various systems developed in the RP group of CERN are explained in Chapter 2. The legacy systems and the latest generation of installed radiation monitors are all based on discrete components. The management of such a complex system with thousands of components is a herculean task and there is often an unavoidable risk of obsolescence of the components. The solution currently applied is the procurement and storage of components that would be required in the foreseeable future. The solution, although temporarily helping to mitigate the obsolescence problem, nonetheless renders any fault repair or upgrade cumbersome. Hence, an application specific integrated circuit (ASIC) development program was initiated in the group.

This thesis starts with the characterization of an ASIC developed in this program by a previous colleague. From different field tests, the need to upgrade the ASIC was evident. A direct upgrade of the ASIC was unfortunately not feasible due to the unavailability of the technology used for the design of the chip. Hence, a detailed technology evaluation to find a potential new technology node for the future version of the ASIC was necessary. A literature review presented in Chapter 3 reveals that the majority of the research work carried out in the ultra-low current measurement systems discusses the implementation in technology nodes of 350 nm or higher. Also, no reported work demonstrates the required dynamic range and attains a sensitivity of 1 fA. Since the technology nodes available for the design of a future system at CERN were 130 nm or lower, a suitable candidate had to be found in these finer technology nodes and their achievable sensitivity had to be evaluated.

Chapters 4 and 5 explain the research carried out in this direction and establishes the techniques and architectures for designing a low current measurement system in finer technology nodes. GLOBALFOUNDRIES 22FDX and TSMC 130 nm were the chosen technologies for in-depth study. The various leakage currents that affect the ultra-low current measurement system in the analyzed technologies were determined. In this doctoral research, two technology demonstration ASICs were designed and characterized. Chapter 5 delves deeper into the different non-idealities

that affect various low-current measurement topologies. A detailed comparative analysis to find out which method performs better in different current ranges is also carried out.

From the results of the studies of these two prototype versions, a third version of the ASIC was designed. This version has two variants – an analog only one and a mixed-signal one. The analog version attains a wide dynamic range using two different current measurement methods. With the mixed-signal version, the analog and digital sections are combined to make a single chip solution for the front end of the ionization chambers. The different techniques employed to minimize the impact of the noisy digital section on the sensitive analog nodes are explained. The design of this version of the ASIC, which is the central objective of the thesis, is presented in Chapter 6.

The performance of the designed ASICs in different scenarios was extensively studied. The methodologies adopted and the results of the characterization are summarized in Chapter 7. Measurement results with different types of ionization chambers subjected to varying dose rates and fields are presented. The influence of temperature and humidity on the measurements is analyzed and explained in this chapter. The stability of the two current measurement methods with variation in temperature is studied and demonstrated. The performance of the ASIC with a pulsed radiation field was experimentally determined and it was shown to be much superior to its predecessor, which was one of the driving goals for carrying out this research. The conclusion of the thesis and the direction for the future is presented in the final chapter.

The thesis thus addresses the central research question of:

How can a mixed-signal current measurement ASIC with sub-femtoampere sensitivity and 9-decade dynamic range be designed in technology node of 130 nm?

Additionally, the questions addressed are:

- What are the circuit topologies that could be used for ultra-low current measurement and simultaneously achieve a wide dynamic range? What are the effects of different non-linearities on these methodologies?
- How do leakage currents vary across different technology nodes and what is the influence of temperature and humidity on them?
- What should be factored in while designing a mixed-signal system with a hypersensitive analog front end?
- How is radiation detection performed with ionization chambers, and how are the front-end electronics interfaced to these sensors?
- How do ionization chambers respond to pulsed radiation, and what are the factors to be considered while designing the front end for measuring resulting pulsed currents?

Chapter 2

Radiation Monitors at CERN

An extensive network of about 800 ionizing radiation monitors covers CERN's various accelerators and experimental facilities, to protect staff, the general public, and the environment from unwarranted radiation exposure. The responsibility for radiation protection and monitoring is shouldered by different systems. The most widely used radiation monitoring system that has been in operation since 1985 is ARCON (ARea CONtroller) [14]. The next generation, which has been operating since 2004, is RAMSES (RAdiation Monitoring System for the Environment and Safety). Both these systems are now being replaced by the state-of-the-art system – CROME (CERN radiation monitoring electronics). ARCON and CROME were developed in house while RAMSES is a commercial off-the-shelf (COTS) system. All the systems are based on discrete components. The radiation monitors interface to a supervisory control and data acquisition (SCADA) system for data logging. The supervision system is called REMUS (radiation and environment monitoring unified supervision) [15].

This chapter explains the architecture of the readout section of these systems before getting into the details of an ASIC which was developed to have an in-house solution for a radiation monitoring system, avoiding dependency on COTS systems and components. The ASIC, named UTOPIA (ultra low picoammeter) and designed in the AMS 350 nm technology, has a functionality equivalent to the readout section of other systems. There are two versions of this ASIC. The digital section and the details of the static and dynamic characterization of the second version of the ASIC, UTOPIA 2, are presented in detail.

2.1 ARCON

ARCON is the first-generation radiation monitoring system deployed at CERN [14]. It is based on a transimpedance amplifier front end converting the current from the ionization chamber into a voltage. The system architecture of ARCON is depicted in Fig. 2.1. The generated voltage is filtered and fed to a voltage-to-frequency converter circuit. The counts, which are generated

proportional to the voltage, are sent out as a digital word. The system also includes a high voltage generation section to provide the appropriate bias voltage to the ionization chamber.

Each ARCON counter card can accommodate up to 16 channels and an ARCON can have up to four of these counter input cards, allowing up to 64 channels to be processed. The programmable logic implementing the multiplexing sends the data to a controller which converts the digital counts into a dose rate. The value thus measured is passed onto a supervision system. The controller can generate alarms depending on the set thresholds. ARCON adopts a centralized architecture where a single controller interfaced to different channels is the point of interface for the supervision and the alarm unit.

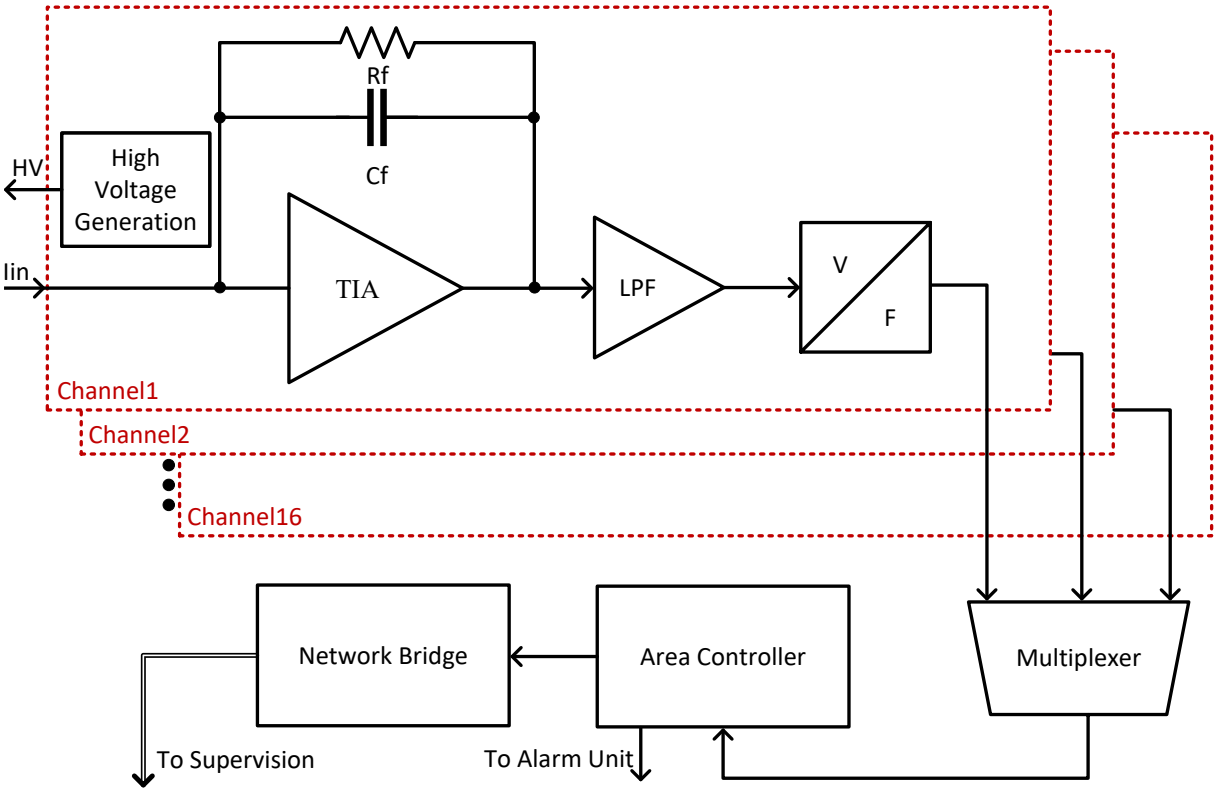

Figure 2.1: ARCON system

2.2 RAMSES

With the expansion of the experimental facilities, ARCON was assisted by RAMSES [15]. The architecture of the system is shown in Fig. 2.2 .The system consists of two channels in a single unit, where the second dummy channel is for leakage compensation. In the input path from the ionization chamber, a series resistor is included to increase the time constant of charge collection. Both the channels employ the current to frequency conversion (CFC) principle [16], and the difference between their outputs is digitized by an analog to digital convertor (ADC) and comparators. The digital output is processed by a CPU that interfaces with a monitoring station through a field bus. The interface to supervision is through the programmable logic

controller (PLC) based monitoring station. The CPU interacts directly with the alarm unit. Up to eight such channels can be interfaced to a single monitoring station.

Compared to ARCON, RAMSES is a federated system with each channel having its own CPU and interface to the alarm unit. The channels, however, do not interact directly with the supervision. Each monitoring station thus acts as an independent unit. They are also equipped with temporary data storage provisions before transmitting to the supervision.

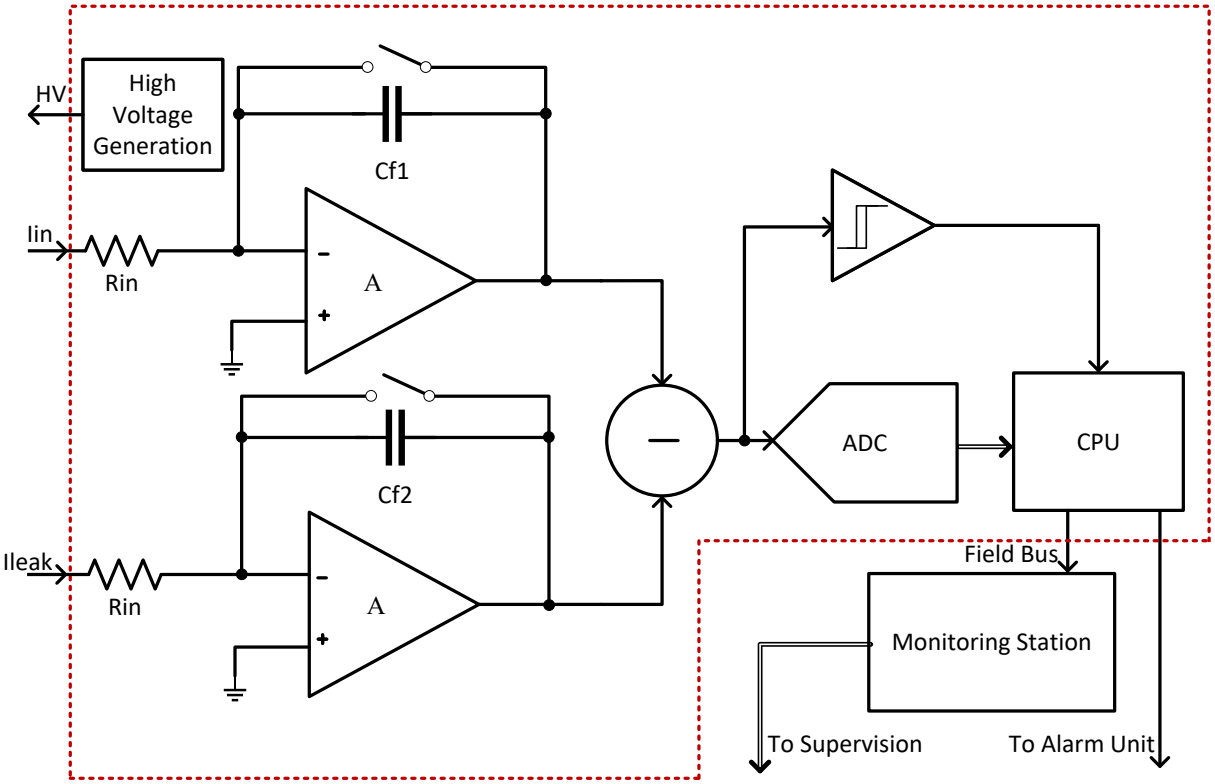

Figure 2.2: RAMSES system

2.3 CROME

The latest generation of the radiation monitoring system is CROME, which started its era of operation in 2021 by replacing ARCON. The system architecture of CROME is shown in Fig. 2.3.

CFC with reset counting is the current measurement principle of CROME. The input current is integrated and fed through a driver to an ADC. The initial voltage at the start of the integration cycle and the final voltage at which the reset is applied are measured by the ADC. The problem of overshoot associated with the reset counting method is tackled by the ADC measurement. Three comparators with progressively higher thresholds generate outputs which are handled by the digital section. A reset pulse of predefined duration is generated depending on the comparator outputs. The current calculations are carried out by a Zynq system-on-a-chip (SoC) module. Temperature compensation based on the temperature data read by an on-board sensor [17], dose rate calculation, and averaging over a defined interval are all handled by the SoC.

The interface to the supervision is also provided through an application software in the SoC. CROME demonstrates a totally modular architecture, with each unit acting as an independent entity with its own processor, a direct interface to the alarm unit, and a network interface to the supervision.

There are around 3000 discrete components in each of the CROME systems. The sheer number of components makes the system extremely complex. The difficulties faced in the maintenance and upgrade of such a system are sourcing all the components, mitigating their obsolescence, and difficult identification in the event of unexpected failures.

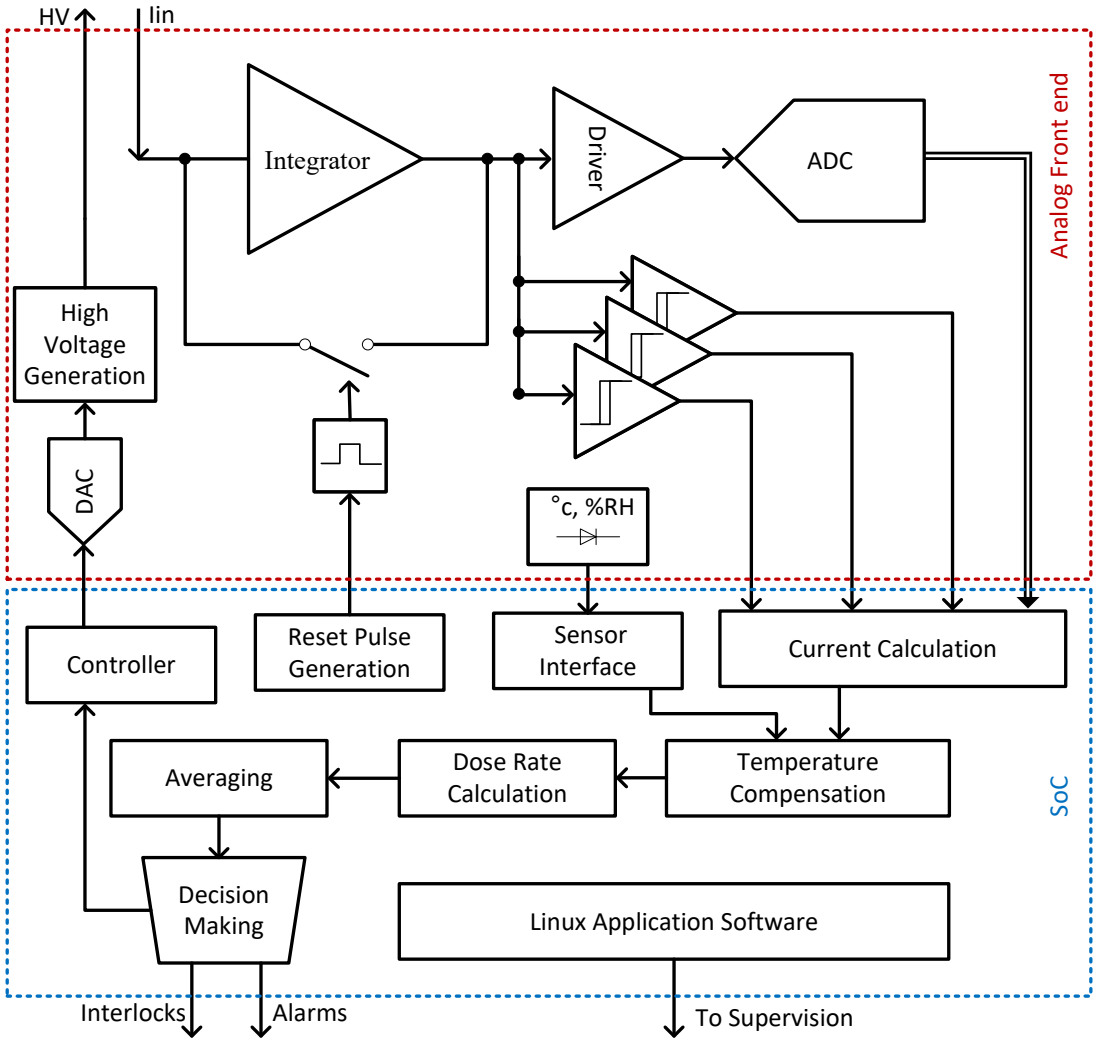

Figure 2.3: CROME architecture

An ASIC development program was undertaken by the radiation protection group at CERN to design the future front end of radiation monitors. The goals were to consolidate the functionalities currently demonstrated by the legacy systems into a single chip along with achieving the best possible performance. The development, which started in 2013, resulted in a series of ASIC developments with different goals.

2.4 UTOPIA

The first ASIC that was developed in the radiation protection (RP) group is UTOPIA 1. This development aimed to evaluate the various leakage currents associated with a typical ultra-low current measurement front end and to establish ways to minimize them. The second generation of the ASIC, named UTOPIA 2, implemented the findings of its predecessor. The ASIC was able to achieve a remarkable dynamic range of nine decades from -1 fA to -5 µA . The design of both the UTOPIA ASICs was successfully carried out by a previous colleague, Dr. Evgenia Voulgari, and the results are published in [18]–[21].

UTOPIA 2 is based on an asynchronous CFC architecture based on charge balancing. There is a primary channel for current measurement and a secondary channel for leakage current compensation. The first channel consists of a feedback capacitor of 1 pF and two charge injection branches generating charges of 100 fC and 400 fC. The feedback capacitance of the second channel is 100 fF and the charge generation block generates 100 fC. The pulses corresponding to charge injection are sent out to an external FPGA.

2.4.1 Static characterization of UTOPIA 2

This research started with studying UTOPIA system and developing the firmware and software for extensively characterising the ASIC. The firmware was developed in VHDL targeting the Zybo board based on the Z-7010 FPGA from Xilinx. The block diagram of the developed FPGA firmware is shown in Fig. 2.4.

The charge pulse corresponding to 100 fC, called Discharge, and that for 400 fC, called Weight, are the two main outputs from channel 1 that are processed in the FPGA. The latter also receives a few other error signals and generates some control signals primarily aimed at calibration. For channel 2, depending on the polarity of the leakage current determined by the comp_op2 and comp_on2 signals, control signals are generated to select the polarity of the charge to be injected for leakage compensation. The number of charge injection pulses is counted by both of the channel interface modules, resulting in different counts that are multiplexed and sent out through a UART interface. An I2C interface module programs two digital to analog convertors (DACs) on an external board to generate various voltages for the chip. The temperature on board is also read through the same I2C interface. The temperature and humidity read by this module are multiplexed along with the various counts to be sent out serially. The generated data is received by a MATLAB-based software through a serial port.

The ASIC was extensively characterized with static currents generated by the current sources Keithley 263 and 6430. Using a MATLAB based characterization software, the various performance metrics of the ASIC were determined. The ASIC showed excellent linearity in the current range from -1 fA to -5 µA. The input leakage current of the whole measurement system was found to be around -50 fA. This was mainly due to the input electrostatic discharge (ESD) diodes.

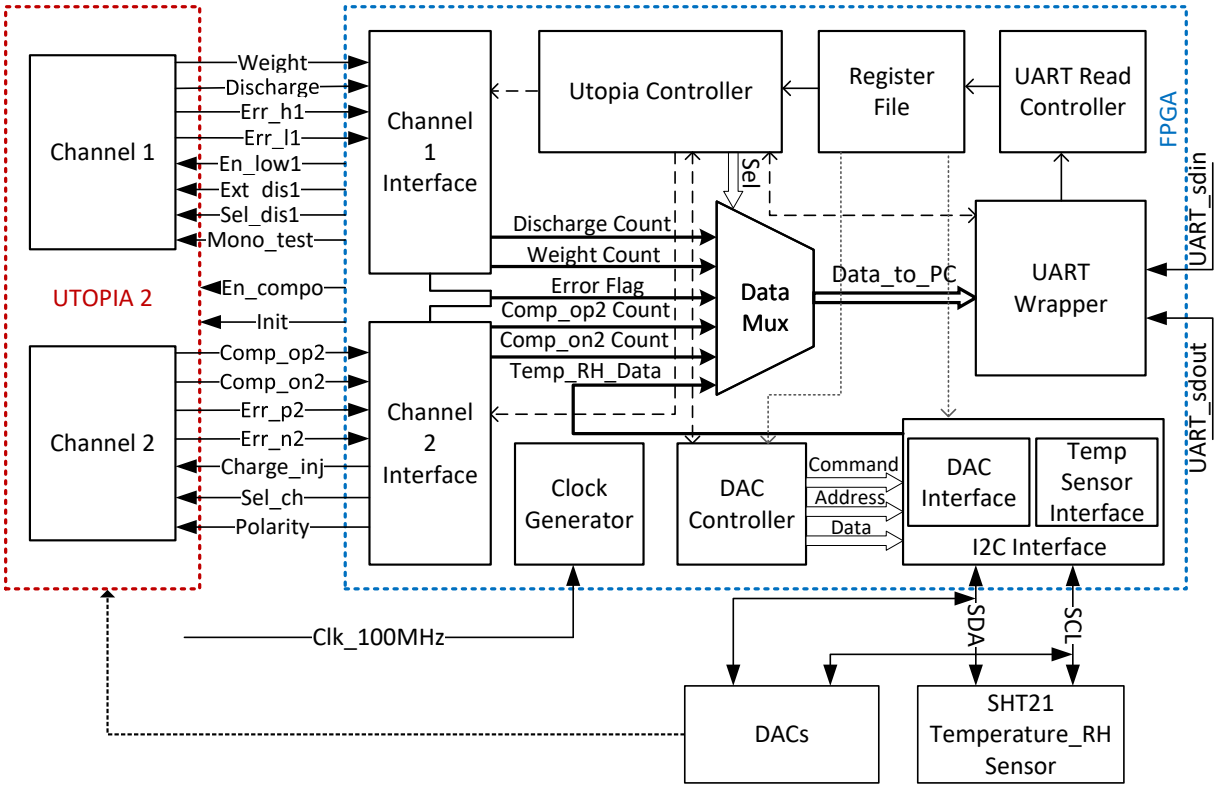

Figure 2.4: UTOPIA 2 FPGA architecture

The time window for accurate measurement in different current ranges were determined as follows:

Table 2.1: Current measurement time of UTOPIA 2

Current range	Measurement time	Error %
−1 fA to −10 fA	200 s	±20%
−10 fA to −50 fA	50 s	±2%
−50 fA to −500 fA	10 s	±2%
−500 fA to −5 pA	1 s	±2%
−5 pA to −5 µA	0.1 s	±2%

As the input current increases, less time is required to collect a sufficient number of counts to obtain the required accuracy.

2.4.2 Dynamic laboratory characterization of UTOPIA 2

The bandwidth requirements of radiation monitors are often very relaxed as the ionization chambers themselves are meant to measure the total ionization dose. The charges generated by an ionization event are accumulated and transferred to the front-end electronics. Especially in the case of environmental monitoring, the generated current is practically a DC for the majority of the measurement time under normal conditions. Hence, the results obtained in the static characterization hold good. However, in applications such as hadron therapy environments or

near particle accelerators, the encountered radiation field is pulsed and the width of the pulse varies with application. The output current pulse from the ionization chamber is a stretched version of the input radiation pulse, with the width depending on the time constant of the discharge path. Most of the charges are delivered in the first few milliseconds followed by an exponentially decreasing discharge. Hence, dynamic characterization of the front-end ASIC was imperative to assess its response to pulsed currents and different input current profiles.

Spectre simulations helped in determining the performance of UTOPIA 2 with pulsed inputs. The chip was simulated to correctly measure pulsed currents. The minimum pulse width of the input current for accurate current measurement was interesting to determine.

The time required by the comparator to generate a pulse is

$$t = \frac{\Delta V.C_f}{I_{\text{det}}}. \tag{2.1}$$

For -5 µA input current, the time to integrate a voltage of 0.1 V on a 1 pF capacitor is 20 ns. However, this value is arrived at by assuming that the voltage at the input terminal of the OTA (Vin) will not move significantly compared to the common-mode voltage Vcm. There is a dynamic offset due to the limited gain of the OTA. Hence, Vin does not remain constant and adds to the integration time.

The difference is more pronounced at the higher end of the dynamic range. The results of cadence simulation are shown in Fig. 2.5. The integration time is calculated as the time difference between the falling edge of the input current pulse and the rising edge of the comparator. Thus, for an input current of -5 µA, the integration time is 25 ns instead of 20 ns. The difference between the ideal and simulated integration times decreases with the magnitude of the input current. The above simulation time is obtained by feeding the pulse directly to the ASIC. Adding an input resistance of 200 Ω and capacitance of 10 pF, to emulate an application environment with the chamber and the cable, already delays the response and for the case of -5 µA, the integration time rises to 33 ns.

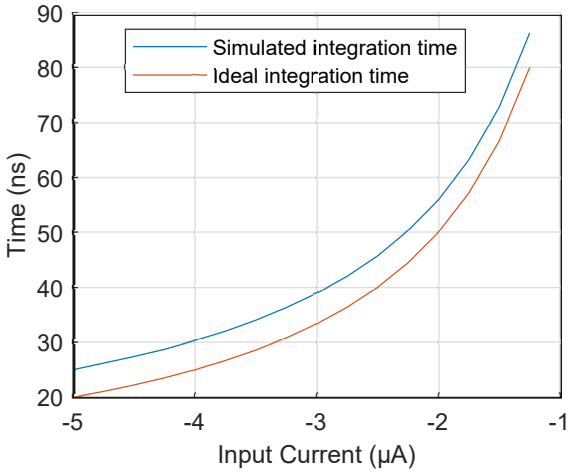

Figure 2.5: Simulation output - Integration time for different input currents

2.4.2.1 Laboratory characterization with pulsed currents

To determine the performance of UTOPIA 2 in a pulsed radiation field, the first measurements were done by injecting pulsed currents. The measurement set-up used is shown in Fig. 2.6.

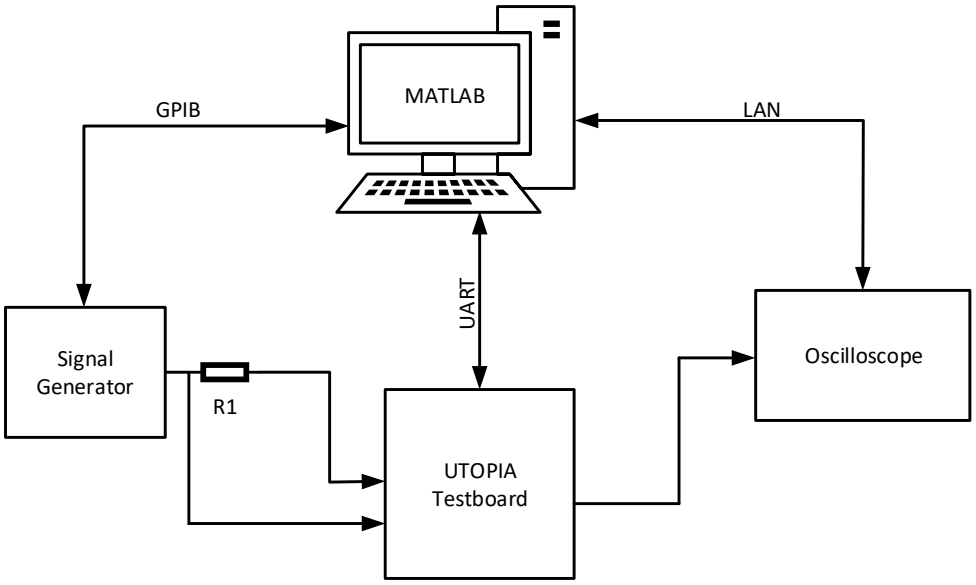

Figure 2.6: Laboratory set-up for pulsed current measurement with UTOPIA 2

A data acquisition environment was created in MATLAB. Voltage pulses were generated using a signal generator from TTi (TG5021A). The instrument was controlled from MATLAB using the GPIB interface. The generated pulses were fed through a precision resistor R1. The value of the resistor used was 1 MΩ or 100 MΩ, depending on the desired range of current. The voltage waveform thus gets converted into current and was injected into the ASIC.

For low frequency input signals, the output from the ASIC was captured using an FPGA. The counts generated by the ASIC corresponding to the input current were counted in a 40 ms interval in the FPGA and then transferred to the test PC using a UART link. For high frequency current pulses, the communication channel through FPGA was not fast enough to transfer the measured data due to bandwidth limitations. So, for this scenario, the output pulses from the ASIC were directly sampled by a high-speed oscilloscope (LeCroy HDO6104). The oscilloscope can sample up to 2.5 GHz and has a data buffer length of up to 50 mega samples.

The captured data from the oscilloscope was transferred to MATLAB using an Ethernet link. The counting of pulses and conversion to equivalent charge were carried out in MATLAB. To affirm the functionality of the chip in a pulsed environment, the quanta of charge injected was compared to that measured by the chip. The FPGA also generated the reset signal based on the input from the signal generator to reset the integration operation of the chip. When the signal generator is powered off or when the output signal level is 0, the common mode voltage generates a current of around -1.4 µA. So, with the 1MΩ resistor, this was the minimum current injected into the chip. During the positive cycle of the input voltage waveform, when the voltage was above Vcm this generated a positive current. The OTA would then integrate in the negative direction. A voltage mismatch at the level even of microvolts generated nanoampere currents that would further affect the measurement values. So, with this set-up, it was impossible to generate zero current.

To circumvent this issue, the voltage waveform that was used to generate the current was also fed into the FPGA. The input buffer of the FPGA was configured as LVCMOS33. Also, the input pins had a diode tied to the ground to suppress negative voltages. The captured voltage waveform in the FPGA was routed to the ASIC as the reset signal to the feedback capacitor. Thus, the OTA remains in reset in the positive cycle of the input pulse and integrates the current supplied in the negative cycle of the input.

An input pulse of 1 Hz frequency and an ON current of -5 µA was injected. The pulse width was swept from 5 µs to 10 ns. The results of the measurement are shown in Fig. 2.7. An input frequency of 1 Hz was chosen to have a similar frequency to the LHC super cycle.

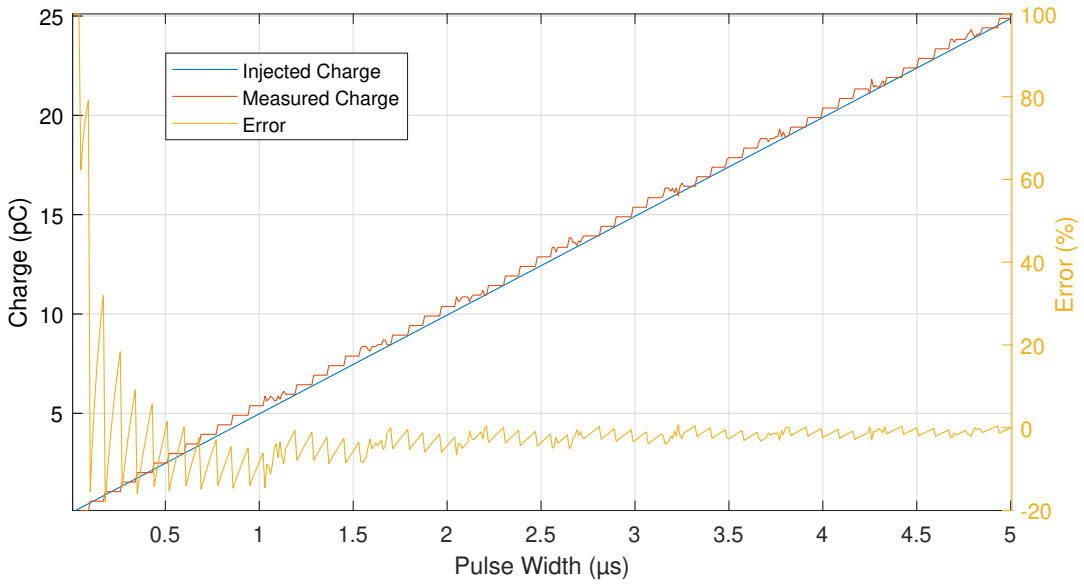

Figure 2.7: Charge measurement by UTOPIA 2 for a pulse of 1 Hz frequency, current of -5 µA, and width varied from 10 ns to 5 µs

The measured charge closely follows the injected charge for a major part of the measured spectrum. The error plot shows the percentage error in the measured charge with respect to the injected charge. The error percentage is close to zero for a pulse width of up to 1 µs. The minimum quantum of measured charge is 100 fC, hence, the effect of quantization is seen in the measured charge waveform. The chip measures the injected charge until a pulse width of 50 ns. This is more than the simulated value of 25 ns. This is attributed to the capacitive and resistive path to the input from the output of the signal generator. The number of complete charge injections reduces with a decrease in the pulse width, resulting in a more erroneous charge measurement.

An exponential wave that closely resembles the output of an ionization chamber was also injected to observe the performance. The results captured are shown in Fig. 2.8. The maximum current in each pulse was 50 nA. It was found that the ASIC can successfully collect all the injected charges in this scenario too.

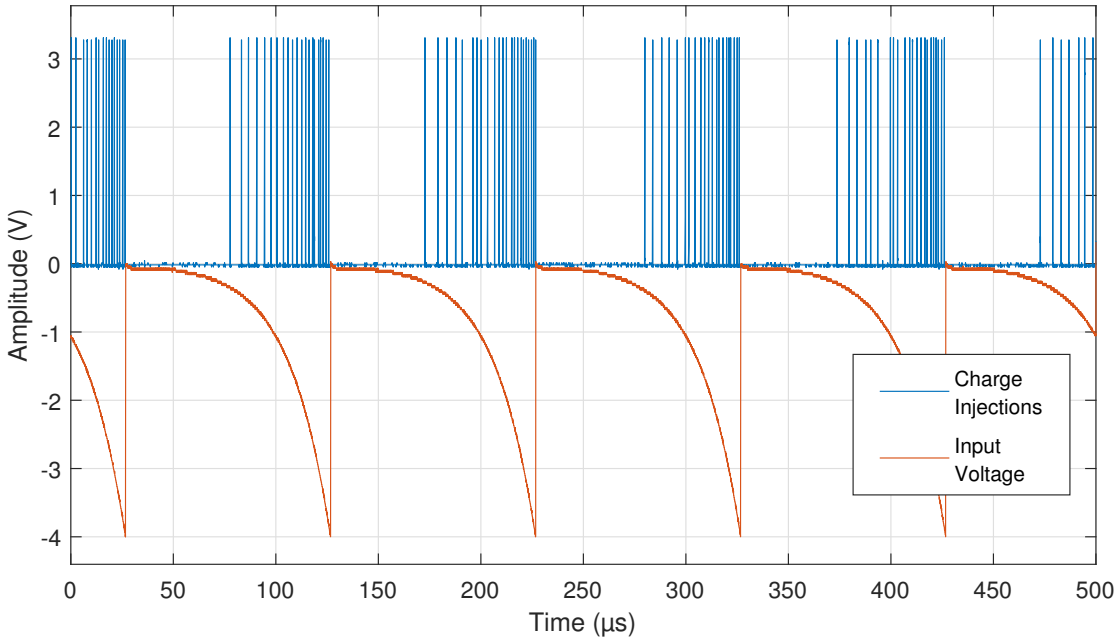

Figure 2.8: Response of UTOPIA 2 to exponential input

Sweeping a square input with an ON current corresponding to −5 µA from a frequency of 500 kHz to 10 MHz results in the output shown in Fig. 2.9. The input charge and measured charge agree to an input frequency of about 4.5 MHz. The chip produced outputs until an input frequency of 9.8 MHz, after which there was no output.

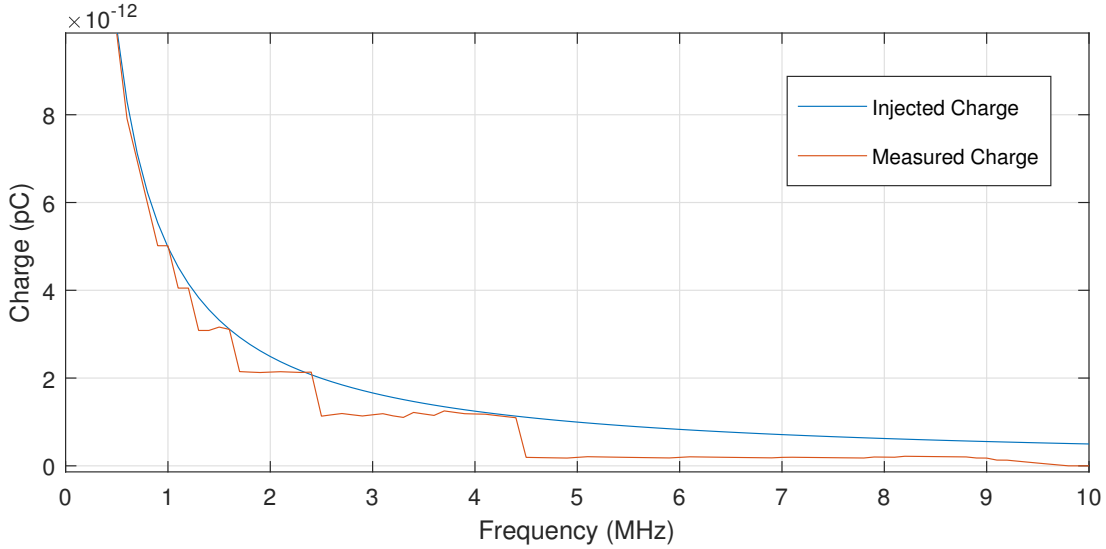

Figure 2.9: Response of UTOPIA 2 to square wave of −5 µA swept from 500 kHz to 10 MHz

The corresponding pulse width, 51 ns, is close to the result measured with pulsed input. For input beyond this frequency, the integrator output does not cross the comparator threshold to generate an output. So, in this scenario, when the feedback capacitor was constantly charged

and discharged using a square pulse, the maximum allowable frequency of the input to generate an output was lower compared to the case of injecting a single pulse.

From the laboratory measurements, it was concluded that UTOPIA 2 can successfully measure pulsed currents. Considering both pulsed input and square input current measurements shown in Figs. 2.7 and 2.9, it could be concluded that, for a maximum current of -5 µA, the chip measures the pulsed current to a frequency of around 4 MHz.

A first level assessment of interfacing UTOPIA 2 with an ionization chamber was performed by Dr. Voulgari by exposing the chamber to Co-60 and Cs-137 sources [21]. This test demonstrated further static current measurement by UTOPIA 2 with radiation sources. However, a detailed characterization with a pulsed radiation field was missing. The results obtained from different field tests are explained in the following sections.

2.4.3 UTOPIA 2 characterization with pulsed radiation

To assess the performance of the ASIC in a real application scenario, tests were done at the CERN Linear Electron Accelerator for Research (CLEAR) facility and the Institute of Radio Physics (IRA) at Lausanne University Hospital (CHUV).

Measurements at CLEAR aimed to test the whole measurement chain from the ionization chamber to the visualization software. The set-up used is shown in Fig. 2.10

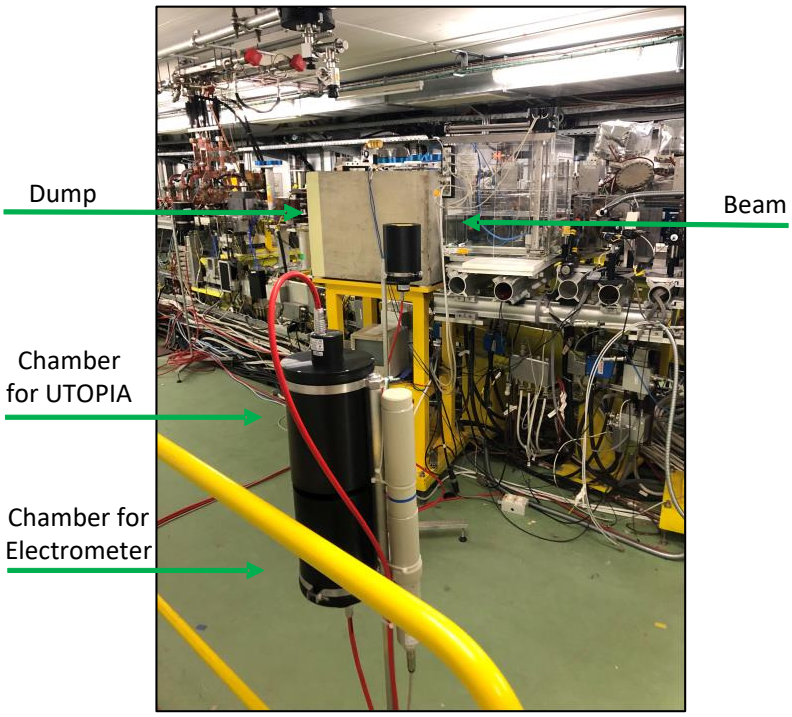

Figure 2.10: Experimental set-up at CLEAR showing the positions of the ionization chambers

The facility allows for a pulsed beam with adjustable parameters. Two air-filled PMI chambers were installed close to the beam dump where the maximum dose is expected. The output

of one chamber was connected to a reference electrometer and that of the other chamber to UTOPIA 2. Both the chambers were expected to receive similar dose rates. The outputs of the chambers were brought out of the experimental hall to be measured simultaneously by the two systems. The beam had a repetition frequency of 0.8 Hz. The charge in the beam was varied and measurements were done for three charges: 1 nC, 10 nC, and 15 nC.

A comparison of the charges measured by UTOPIA 2 and the reference electrometer is shown in Table 2.2.

Table 2.2: Charges measured by UTOPIA and reference electrometer at CLEAR

Beam Charge	Electrometer Charge (C)	UTOPIA2 Charge (C)	Error (%)
1 nC	1.18E-10	1.23E-10	4.50
10 nC	2.48E-10	2.33E-10	6.18
15 nC	3.43E-10	3.22E-10	5.96

The charges measured by UTOPIA 2 in the three iterations are plotted in Fig. 2.11

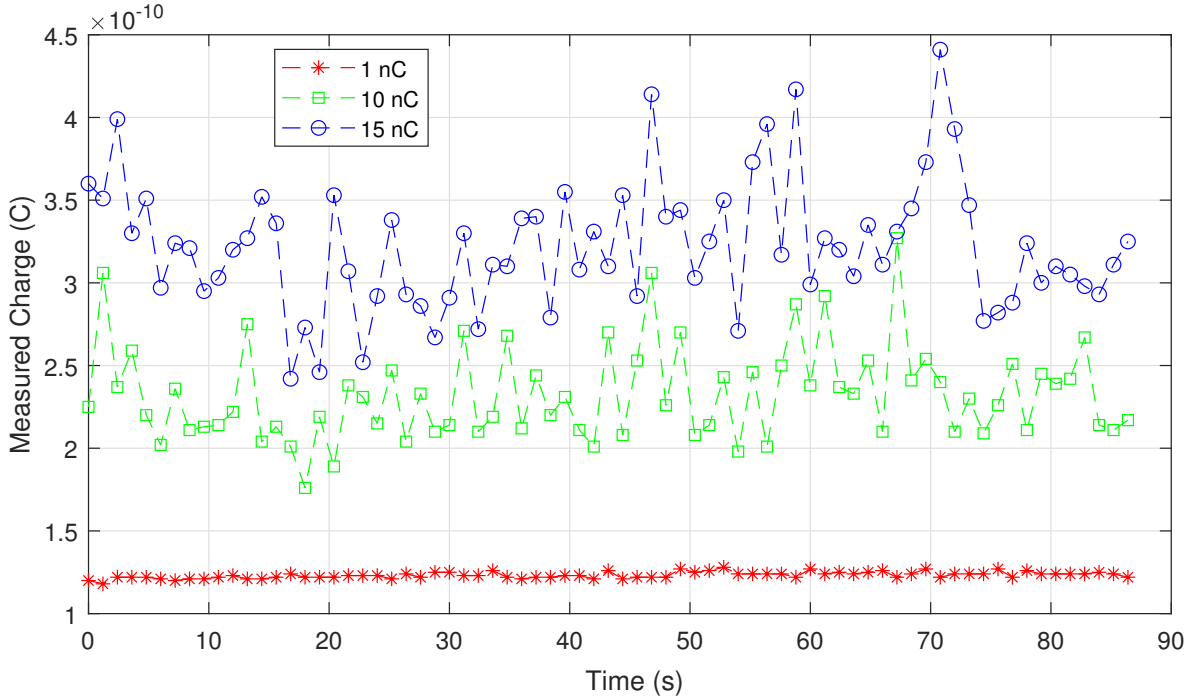

Figure 2.11: Charges measured by UTOPIA 2 with pulsed beam at CLEAR facility

The charges collected showed a good correlation with that measured with the electrometer. However, the chosen beam parameters did not allow for testing with higher charges. Also, the width of the beam pulse could not be adjusted, hence a series of pulses with cumulative charges was generated by the accelerator. As a result, the pulses were not distinguishable from the background. The tests, however, demonstrated that the ASIC could be interfaced with a PMI type of ionization chamber and, in the measured regime, the charge measurement capability was comparable to a reference system.

The radiation monitoring system specifications [13], however, demand a pulse processing capability with a pulse of up to 500 nC per pulse with a pulse width of a few milliseconds. Hence, higher dose rates were required. To measure in this desired regime, a second series of tests with pulsed radiation was conducted at IRA. It houses the Oriatron eRT6 accelerator [22] designed to generate high dose per pulse beams. The accelerator can generate repeatable doses with a standard deviation of less than 1%. The pulse width could be measured from 0.05 µs to 4 µs with a repetition frequency of 5 Hz to 200 Hz. The accelerator generates an electron beam at 6 MeV. The measurements employed the IG32 type ionization chamber. The measurement set-up used at IRA is shown in Fig. 2.12.

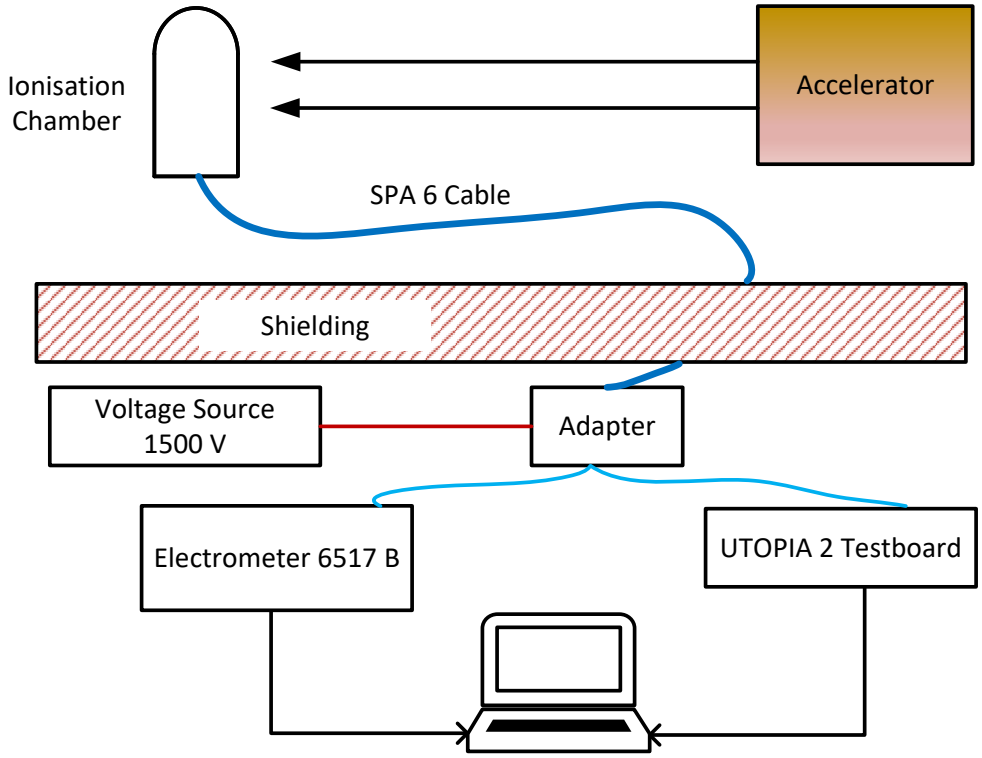

Figure 2.12: Measurement set-up at IRA

For the measurement, only the ionization chamber was placed in the beamline of the accelerator. The output of the chamber was carried by an SPA6 cable [14] through shielding to an adapter box. This cable was specifically designed within the section to combine the current and the high voltage paths into a single cable. The cable also provides sufficient immunity to physical effects such as triboelectric effects that can contribute to the leakage. The box also receives the high voltage from a voltage source and passes it to the ionization chamber through the same cable. The current signal from the SPA6 cable is then passed on to the measurement systems from the adapter box. The measurements were carried out sequentially; first recorded by the electrometer and then by UTOPIA 2. To generate higher charges, the tension on the current injection gun of the accelerator was varied. The various settings used are detailed in Table 2.3.

Table 2.3: Charges measured by the reference electrometer for different pulse settings at IRA

Tension (V)	Pulse Width (µs)	Mean Charge (nC)	Sigma (C)
100	0.5	1.28E-09	9.43E-12
100	1	3.23E-09	3.56E-11
100	4	4.99E-09	1.41E-10
105	4	1.45E-08	3.93E-10
110	4	3.61E-08	8.49E-10
120	4	9.80E-08	1.32E-09
150	4	2.75E-07	8.16E-10
170	4	3.22E-07	5.72E-09
200	4	3.26E-07	1.25E-09

For each tension and pulse width setting, three pulses were measured. The measurement by the reference electrometer shows great stability of the beam charges. For each set of measurements, UTOPIA 2 also captured the injected charges. The results obtained by comparing the charges measured by both systems are plotted in Fig. 2.13.

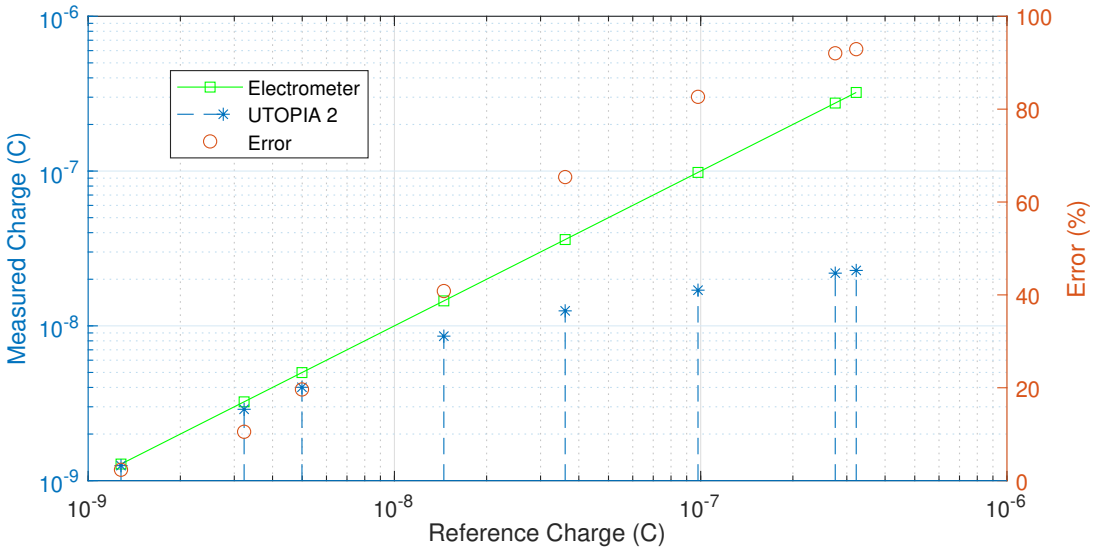

Figure 2.13: Comparison of charge measurement by UTOPIA 2 and reference electrometer for a pulsed beam

For lower charges, the measurement by UTOPIA 2 agreed with that measured by the electrometer. However, as the input charge was increased, the measurement error increased too. For charges of around 100 nC, the error in the UTOPIA 2 measurement reached around 80%. The measurements were repeated also with the CROME system, which demonstrated superior charge measurement in comparison to UTOPIA 2. This is attributed to the higher time constant of the charge discharging circuit presented by CROME to the ionization chamber. The feedback capacitor in CROME is 120 pF and the input path consists of a series switch which offers a definite resistance, slowing down the flow of charges. In UTOPIA 2, the output of the ionization chamber is directly connected to the charge integrator through a very low impedance path. Also, the feedback

capacitor is 1 pF. Hence, the chip started to saturate for charges above 15 nC. The time constant of the input port of the ASIC must be increased by increasing the feedback capacitor or input impedance to facilitate a better collection of charges.

2.5 Conclusion

The chapter presented various radiation monitoring systems developed by the RP group at CERN over the years. The principle of operation of the legacy systems – ARCON and RAMSES – is followed by that of the new generation radiation monitoring system – CROME. During the long 2019–2020 technical shutdown of CERN's accelerator complex and experiment, CROME successfully replaced ARCON. The replacement of RAMSES by CROME is planned for the end of the next long technical shutdown starting in 2025.

The development of the future radiation monitoring system is already underway with the design of specific ASICs for the front-end electronics of the ionization chamber current measurement. UTOPIA 2 is a state-of-the-art current measurement ASIC with 9 decades of operation. The characterization of the ASIC was presented in detail in the chapter. The linearity of the ASIC was well established from -1 fA to -5 µA with static currents. The capability of the ASIC to interface with different ionization chambers was established. The performance of the ASIC in pulsed radiation fields was experimentally determined. The measurement carried out at IRA revealed the need for a redesign of the ASIC with increased charge measurement capabilities to meet all of the requirements of the specification. The digital processing of the ASIC was handled by an FPGA. To comply with the objectives set by CERN to simplify the implementation and use of this type of ASIC for measuring ultra-low currents as a standalone unit that can be directly interfaced with a supervisory system, the digital section needs to be integrated into the ASIC.

This chapter explained how ultra-low current measurement systems were implemented at CERN for radiation monitoring. Current measurement in the sub-picoampere range finds applications in other research fields too. To gain a broader perspective for the design of the next version of the ASIC, a detailed literature review of the existing sub-picoampere current measurement systems was performed. The details of the study are presented in the next chapter.

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Chapter 3

State of the Art Low Current Measurement Methods

Measuring very low currents, particularly in the sub-picoampere range, has wide applications. Radiation monitoring, biomedical signal processing, and electrochemical sensing, however, are the three main frontrunners driving the research in this domain. A literature review of various current measurement systems, with a minimum measurable current in the picoampere range or lower, is summarized in Table 3.1.

Table 3.1: State of the art low current measurement systems

Year	Method	Min. Current	Max. Current	Supply	ASIC	Technology	Input	Ref.
1953	Charge Balancing	100 pA	10 µA	300 V	Discrete	Relays and Capacitor	Photomultiplier Tube	[16]
1968	Charge Balancing	300 pA	3 µA	15 V	Discrete	OPAMP, BJT	Photomultiplier Tube	[23]
1968	Charge Balancing	10 nA	1 mA	15 V	Discrete	DC Amplifier	NA	[24]
1970	Charge Balancing	500 fA	60 µA	15 V	Discrete	JFET Opamp	Photomultiplier Tube	[25]
1983	Charge Balancing	1 pA	10 µA	5 V	Discrete	Opamp and CMOS Gates	Ionization Chamber	[26]
1994	Dual Slope ADC	100 fA	40 µA	4.8 V	2 µm	CMOS Amplifier	Electroanalytical Instruments	[27]
1998	Charge Balancing and Reset Method	1 nA	600 nA	NA	1.2 µm	FC OTA	Parallel Plate Strip Ionization Chambers	[28]
2000	Dual Slope ADC	1 pA	1 nA	5 V	0.7 µm	OTA, Iref	Electrochemical Transducers	[29]

2004	Integrator, Amplifier, ADC	10 pA	10 µA	3.3 V	0.5 µm	FC OTA	Biosensor	[30]
2005	Charge Balancing	20 pA	2 µA	5 V	0.8 µm	OTA	Strip Ionization detectors	[31]
2006	Sigma Delta ADC	50 fA	100 nA	3.3 V	0.5 µm	FC OPAMP	Biosensor	[32]
2006	Current Conveyer	1 pA	200 nA	5 V	0.5 µm	Cascoded OTA	Electrochemical Sensing	[33]
2007	Sigma Delta ADC	100 fA	1 µA	3 V	0.5 µm	Single Stage Cascode Differential Amplifier	Electrochemical Analysis	[34]
2007	TIA	200 fA	2 µA	3.3 V	0.5 µm	Logarithmic Amplifier	Photodiode	[35]
2008	Reset Method	20 fA	100 nA	3.3 V	0.35 µm	FC Opamp	Simulation	[36]
2009	Direct Slope Method	1 pA	100 µA	3.3 V	0.5 µm	Cascoded Amplifier	Biosensor	[37]
2009	TIA	1 pA	25 nA	±1.5 V	0.35 µm	Miller Opamp	Nanodevices	[38]
2010	Current Mode ADC	15 pA	16 nA	1.5 V	1.5 µm	Current Mirror, Encoder	Biosensor	[39]
2011	Sigma Delta ADC	4 pA	21 nA	1.8 V	0.18 µm	FC Amplifier with Gain Boosting	Fluorescence Sensor	[40]
2012	Charge Balancing	1 pA	1.05 mA	2.5 V	0.25 µm	Differential Amplifier	Ionization Chamber	[41]
2013	Single Slope ADC, Reset Method	24 pA	350 nA	3.3 V	0.35 µm	Current Conveyer FC OTA	Potentiostat	[42]
2013	TIA	10 pA	350 nA	1.2 V	0.13 µm	Chopper Stabilized FC OTA	Biosensor	[43]
2013	Current Conveyer	8.6 pA	350 nA	1.2 V	0.13 µm	FC OTA	Biosensor	[43]
2013	Current Amplifier	1.5 fA	30 nA	±1.5 V	0.35 µm	External TIA	Nanoelectrodes	[44]
2015	Sigma Delta ADC	314 fA	250 µA	2.5 V	0.18 µm	Two Stage Miller Opamp	Biosensor	[45]
2016	Sigma Delta ADC	100 fA	16 µA	5 V	0.5 µm	FC OTA	Gas Sensor	[46]

2017	SAR ADC	470 fA	20 µA	3.3 V	0.35 µm	FC OTA	Bio Nanosensor	[47]
2017	Charge Balancing	80 pA	12 µA	3.3 V	0.35 µm	FC OTA	Ionization Chamber	[48]
2018	Sigma Delta ADC	100 fA	10 µA	1.8 V	0.18 µm	Cascode Compensated Amplifier	Biosensor	[49]
2019	Sigma Delta ADC	123 fA	1.1 µA	-	0.18 µm	FC OTA	Biosensor	[50]

The study of the different reported literature shows that the current measurement is achieved by either converting the current into a voltage and measuring the voltage or by direct digitization of the current. The different current measurement methods studied can be classified into the following.

1. Using transimpedance amplifier (TIA) [35], [43], [51]–[53]
    (a) Resistive TIA [54]
    (b) Capacitive TIA [55]
        i. Discrete time
        ii. Continuous time
            A. Resistive feedback
            B. Active feedback
2. Direct current measurement
    (a) CFC
        i. Charge balancing [16], [23]–[26]
            A. Current source based charge injection
            B. Switched capacitor based charge injection
        ii. Reset counting [42]
    (b) Current Conveyor [33], [43], [56], [57]
    (c) Current input delta sigma ADC [45], [46], [49], [50]

The various low current measurement methods are depicted in Fig. 3.1. Almost all methods use an amplifier as the first stage, which decouples the current to be measured and passes it on to rest of the measurement chain.

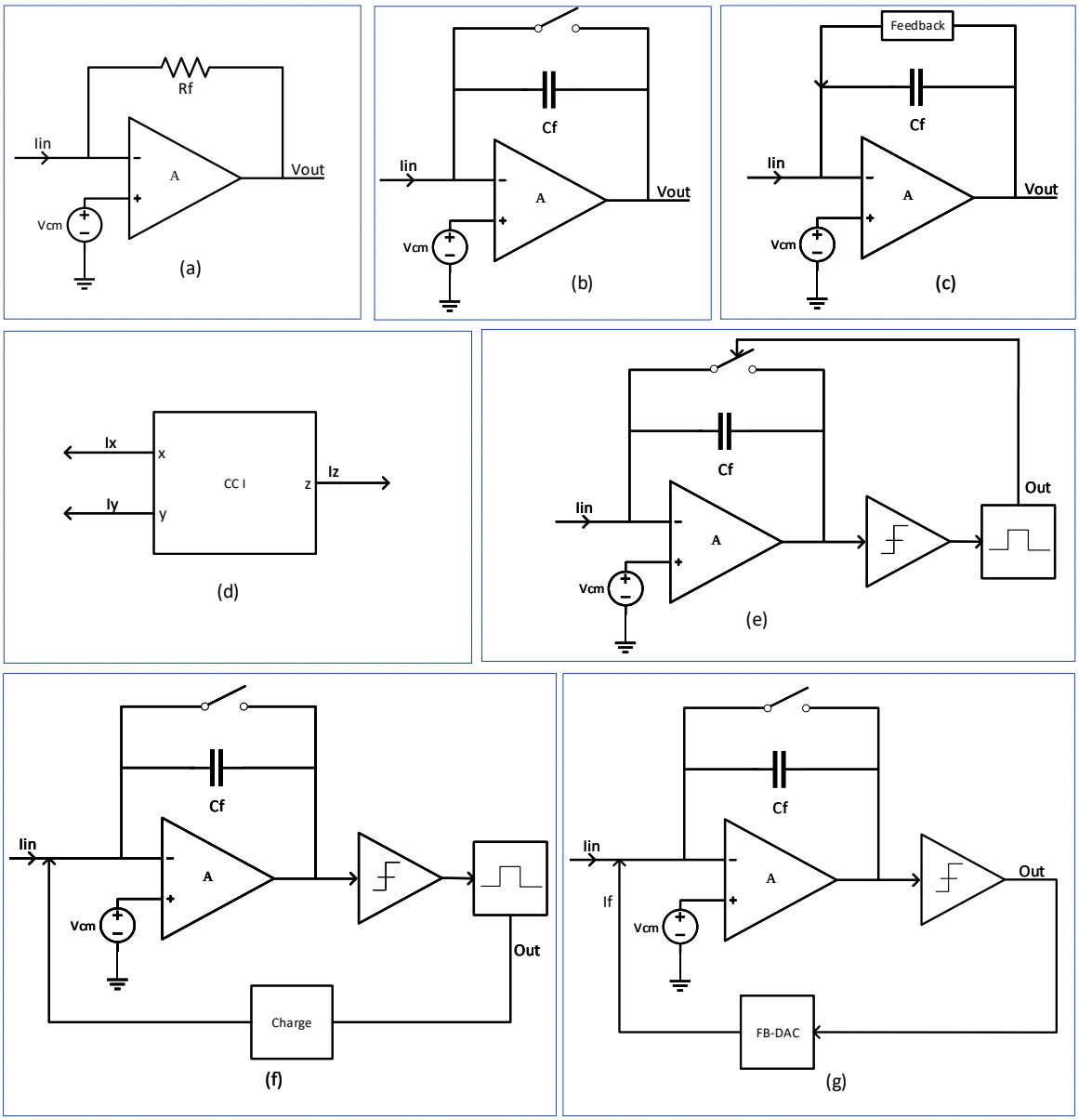

Figure 3.1: Low current measurement methods: (a) resistive TIA, (b) discrete time capacitive TIA, (c) continuous time capacitive TIA, (d) current conveyor, (e) reset counting CFC, (f) charge balancing CFC, and (g) current input delta sigma ADC

3.1 Transimpedance amplifiers

Transimpedance amplifiers convert the low input current into a voltage that can be easily measured using an ADC. Either a resistor or a capacitor can be used as the feedback element of an OPAMP to realize the transimpedance amplifier. A comparison of resistive and capacitive methods is presented in [58] and [59].

The presence of a large feedback resistor affects the noise performance of resistive TIAs. These huge resistors can usually be integrated in the form of pseudoresistors which are quite nonlinear.

They additionally suffer from the trade-off between bandwidth and transimpedance [58]. Capacitive TIAs have a better bandwidth and are hence the popular alternative. They are usually implemented in two stages, with an integrator followed by a differentiator [52]. This implementation exhibits much lower noise and better sensitivity compared with the resistive TIA. The limitation of the capacitive TIAs is the saturation of the capacitor in the presence of a constant DC input or leakage. This issue is addressed by using extra elements in the feedback path to the input. Based on the type of feedback, capacitive TIAs can either have a discrete time implementation or a continuous time approach. In the discrete time method, using a reset switch, the charge stored in the feedback capacitor is periodically reset, hence avoiding saturation. In the continuous time approach, a high-value resistance based feedback or active feedback is used, which will adapt the bias point at the input. Both approaches are commonly employed, with the continuous time method favored for applications requiring higher bandwidth.

3.2 Current conveyors

For measuring currents in electrochemical processes, current conveyors (CC) are commonly used. They are counterparts of OPAMPs in current mode circuits. The input current is decoupled and collected by a low impedance node and presented at the output on a high impedance node. They can be configured as current amplifiers, integrators, etc. They often perform the dual functions of applying a reference voltage to bias the electrode in a sensor and measuring the generated current. They typically amplify the low input current to be processed by further stages. A comparison between the resistive TIA, capacitive TIA, and the current conveyor presented in [54] shows that the latter has the highest noise among the three. The main reason is that the high bias current of the CC interfering with the sensor current makes the overall input noise high. Hence, they are not generally preferred in sub-picoampere current measurement systems.

3.3 Current to frequency conversion

Transimpedance amplifiers dominate the biomedical field, which requires low current measurement with large bandwidth. However, for radiation monitoring, where a large dynamic range requirement dominates over bandwidth, direct current measurement methods, especially using a current to frequency conversion (CFC) circuit, is the preferred choice.

The CFC architecture comprises an integrator followed by a comparator and a pulse generator. The input current is integrated in a feedback capacitor and, when the voltage at the output of the integrator reaches a certain threshold, the comparator output is asserted. This enables a pulse generation. In the reset counting CFC, this pulse resets the feedback capacitor and the whole operation is repeated. The number of resets in a fixed time is proportional to the input current. This reset counting method suffers from a dead time, when the capacitor is in reset. The precise levels at which integrator output is reset has to be determined using additional circuitry to make

this method work accurately. In a charge balancing CFC, instead of resetting the capacitor, a fixed charge of opposite polarity is injected into the input node, thus subtracting this charge from the capacitor. The number of charge injections in a defined time is proportional to the input current. The charge generation can be attained by either charging a reference capacitor to a voltage or by connecting a reference current source for fixed time duration to the input node. The stability of generated charge quantum is the main factor determining the accuracy of this topology. Both the reset counting and charge balancing methods are used for sub-picoampere current measurements.

3.4 Current input delta sigma ADC

Another method of measuring current directly is to use current mode sigma delta ADCs. The front end of the circuit is very similar to the capacitive TIA or CFC. The input current is integrated into a feedback capacitor along with a reference current and a comparator output flips when the output is above a threshold. The comparator output drives a counter. Also, this output selects a different source with opposite polarity in the input. The integrator slope flips direction and integrates in the opposite direction than the first time. When there is no input current, the comparator generates alternate ones and zeros. When there is a current of one polarity, the slope of integration changes, taking more time for the comparator to flip. Hence, the output of the counter changes too. Thus, the input current can be deducted from the counter output. Sigma Delta ADCs are becoming increasingly popular, especially when the current is generated by a biosensor. They are often characterized by a large dynamic range.

Irrespective of the current measurement method, the front end of most of the circuits is an OTA or OPAMP. The most widely used architecture is the folded cascode (FC) OTA. The numerous advantages of this architecture, such as the wide bandwidth and gain accompanied by a wide swing, makes it an ideal choice.

3.5 Radiation monitoring systems

The characteristics of various radiation monitoring systems and ASICs developed at CERN are listed out in Table 3.2. Apart from the system described in Chapter 2, the ASICs designed by the beam loss monitor (BLM) section at CERN are also included. For the BLM systems, as they are installed very close to the accelerators, the current measurement range is higher. They cater to the picoampere to milliampere range. Apart from the ARCON system, which was realized using a TIA, all of the other systems are based on the CFC principle. The best femtoampere measurement was demonstrated by UTOPIA 2 and the currently installed CROME system. They are based on charge balancing and reset counting CFC respectively.

Year	Project	Architecture	Min. Current	Max. Current	Supply	ASIC	Accuracy	Ref.
1988	ARCON	Capacitive TIA	100 fA	50 nA	24 V	Discrete	10%	[14]
2007	RAMSES	Integrator, ADC	10 fA	5 µA	24 V	Discrete	5%	[15]
2012	BLM ASIC	Charge Balancing	1 pA	1.05 mA	2.5 V	0.25 µm	5%	[41]
2012	BLM V1	Integrator, ADC	10 pA	200 mA	48 V	Discrete	10%	[60]
2012	BLM CFC	Charge Balancing	2.5 pA	1 mA	5 V	Discrete	25%	[60]
2015	UTOPIA 1	Charge Balancing	12 fA	5 µA	3.3 V	0.35 µm	2.5%	[21]
2016	UTOPIA 2	Charge Balancing	1 fA	5 µA	3.3 V	0.35 µm	1%	[21]
2016	CROME A	Reset Counting, ADC	1 fA	1 µA	28 V	Discrete	7.2%	[61]
2020	CROME Q	Reset Counting, ADC	0.5 fA	5 µA	28 V	Discrete	8%	In dev

Table 3.2: CERN Radiation monitoring systems

3.6 Conclusion

It can be seen from the detailed literature review presented in this chapter that CFC based charge balancing is one of the oldest and most widely employed methods for low current measurement. The measurement of the total ionizing radiation is efficiently carried out by these architectures. They have simpler architectures compared to Sigma Delta ADCs. The lower number of leakage current sources connected to the input node in a CFC architecture makes them an efficient choice when femtoampere sensitivity is desired. Hence, in this research, the CFC architecture was chosen to explore further. The architecture having an already proven performance record with legacy systems and with UTOPIA ASICs reinforced the choice. A detailed analysis of three current measurement topologies using the CFC architecture is carried out in Chapter 5.

The need for designing a new version of the ASIC was discussed in Chapter 2. Designing the next version of the ASIC met with an unexpected stumbling block in the form of the unavailability of the technology used for the UTOPIA 2 development. Hence, a new technology node had to be found. The literature review showed that the majority of the current measurement systems that could reach the femtoampere range were realized in a 350 nm node or higher. A few works in a 180 nm node could also achieve a sensitivity of hundreds of femtoamperes. The increase of the leakage current with technology scaling makes it challenging to achieve femtoampere sensitivity in finer nodes. Various technologies were evaluated for assessing the leakage current for redesigning the ASIC. The technology nodes studied are – GLOBALFOUNDRIES 22FDX, X-FAB XH03H, STMicroelectronics 28 nm FDSOI, IHP SG13G2, and TSMC 130 nm. The 350 nm transistors of X-FAB had very similar leakage currents to the AMS 350 nm transistors. The core transistors of the smaller nodes progressively demonstrated increasing leakage currents. Ready availability of the GF 22FDX and TSMC 130 nm design kits at the University of Wuppertal and CERN, respectively, directed more studies towards these technology nodes.

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Chapter 4

Attaining Femtoampere Sensitivity in 22 nm Technology

The static characterization of the UTOPIA ASICs yielded promising results and it was proven that UTOPIA 2 can be used for applications to measure currents from -1 fA to -5 µA. However, the results from the dynamic characterization in pulsed radiation fields necessitated a redesign of the ASIC. Both of the UTOPIA chips were designed in AMS 350 nm technology. The low leakage feature of the technology was particularly interesting and aided UTOPIA 2 in accurately measuring femtoampere currents. To redesign the ASIC, other technology options were considered, since the already proven AMS 350 nm technology was unfortunately no longer available for new designs. The 22 nm fully depleted silicon on insulator (FDSOI) technology from GlobalFoundries – GF22FDX [62] was chosen for evaluation for its leakage current performance and to assess if the technology could be used for applications targeting femtoampere measurements.

The work utilized the free silicon provided by GLOBALFOUNDRIES under the 22FDX university partnership with the University of Wuppertal. The aim of creating circuits to measure femtoampere currents in such an advanced node was to establish techniques for using lower technology nodes which would pave the way for the design of a new generation of radiation monitoring ASICs called ACCURATE – Atto to miCro CoURAnt meTEr.

4.1 GF22FDX evaluation

The fully depleted 22FDX is a very versatile technology widely used in a myriad of designs in varied application fields [63], [64]. The technology boasts ultra-low leakage characteristics which could be further enhanced by reverse body biasing. For each application scenario, different transistor variants are available. They differ in threshold voltage (Vt) range, power consumption, and leakage performance. Typical transistors which were considered for evaluating the leakage

currents are: 1. Super low-Vt pfet (slvtpfet), 2. normal-Vt pfet (pfet) 3. high-Vt pfet (hvtpfet), 4. low-leakage high-Vt pfet (llhvtpfet), and 5. ultra-low leakage IO transistor (egullpfet).

To make a detailed study of the leakage currents, Spectre simulations were carried out. The transistors were tied to a supply voltage of 0.8 V and were dimensioned to be 1 µm/1 µm. The technology offers devices in flip well or conventional well configuration. By varying the back-gate voltage, Vbg, the transistor could be biased as forward body biased to increase the speed, or reverse body biased to reduce the leakage. In the simulations, the back gate was tied to 1.6 V to have a low leakage state and was in the conventional well configuration. The results of the simulations are shown in Fig. 4.1.

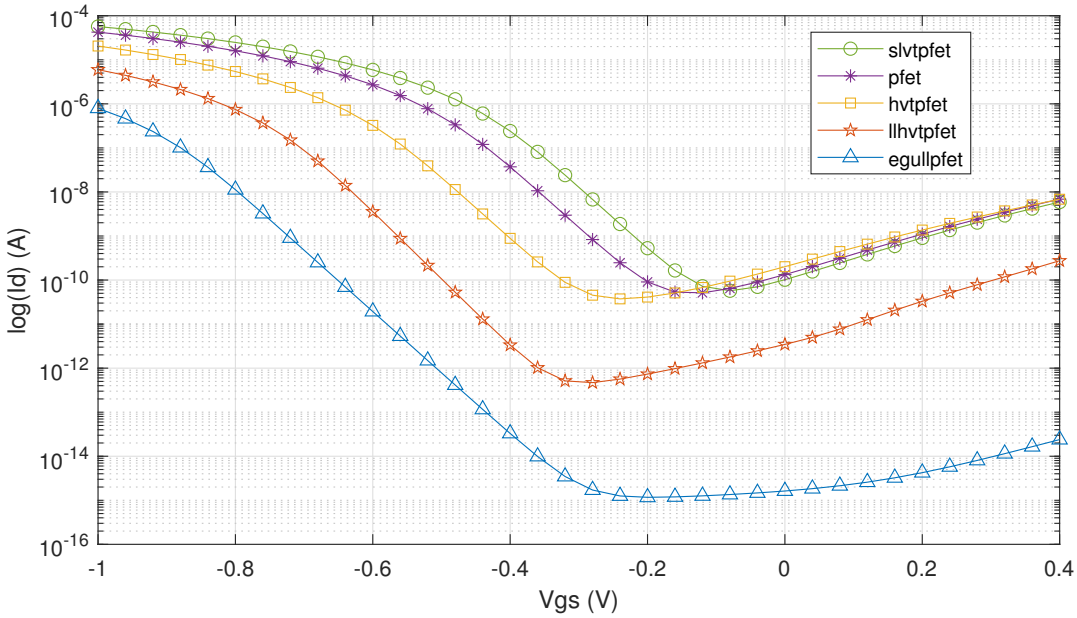


Figure 4.1: Drain current characteristic for different transistors of 22FDX process design kit © 2019 IEEE

From the simulations, the lowest off current among the core transistors was observed for the low-leakage high-Vt pfet (llhvtpfet). For the IO transistor (egullpfet), the drain leakage current was observed to be -1.2 fA. Changing the back-gate voltage had a considerable effect on the leakages for the core transistors. However, the effect of body bias on the egullpfet was very low, the leakage current changed to -1.3 fA for a Vbg of 0.8 V and to -2 fA for a Vbg of 0 V.

For the advanced technologies, such as the 22 nm FDSOI, among the different leakage currents that exist in a transistor, the gate leakage could also make a considerable contribution. This is an effect of scaling down the gate oxide thickness. Currents such as gate tunneling, which were ignored in higher technology nodes, become significant [65], [66]. Gate leakage simulations were performed with the drain to source voltage fixed to 0.1 V, with the back gate tied to 0 V. The transistor dimensions were the same as for drain current simulations. From the results that are plotted in Fig. 4.2, it could be concluded that the thick gate IO transistors have the lowest gate leakage among all the transistors at of the order of attoamperes. Among the core transistors, low-leakage high Vt pfet had the lowest leakage current. Usage of other core transistors was

thus found to be infeasible for low current measurement applications as their inherent leakages were of the order of picoamperes. Changing the back-gate voltage had no influence on the gate leakage currents.

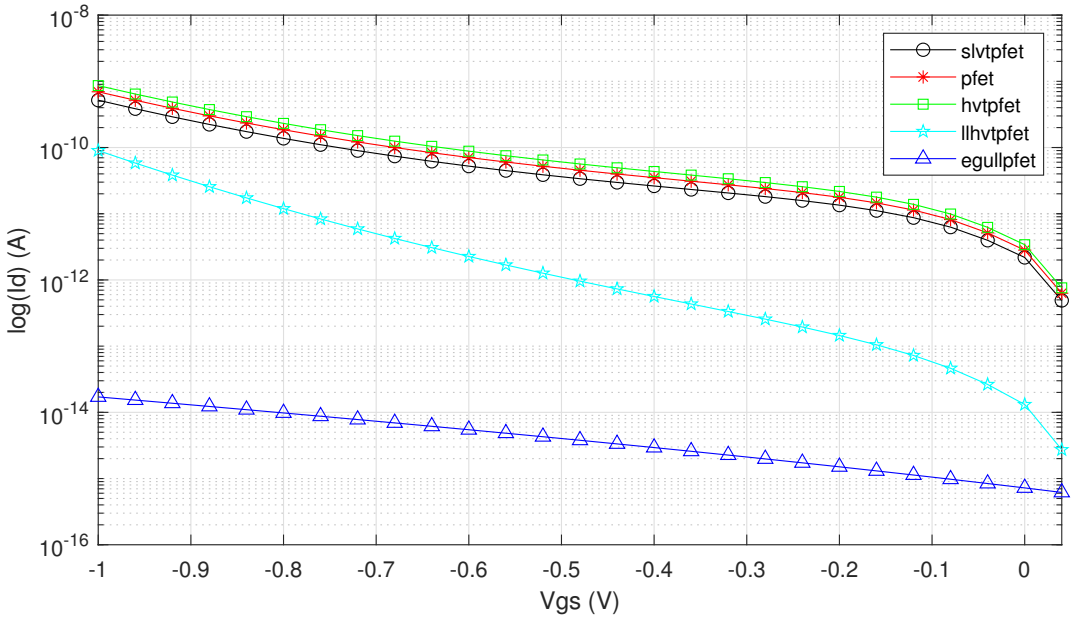


Figure 4.2: Gate current characteristic for different transistors of 22FDX process design kit

4.2 Architecture

To evaluate the leakage currents and assess the performance, the ASIC was designed with three channels. The third channel is shown in Fig. 4.3.

The circuit is the classical current to frequency converter with the OTA configured as an integrator with a reset switch. The various components that can contribute to the total leakage current of this channel are the subthreshold leakage of the reset switch, the input leakage of the OTA arising from the gate leakage of the input transistors, leakage of the ESD diode, and the antenna diode. Channel 1 of the ASIC has only the OTA to be configured in different circuit topologies and the second channel is identical to the third channel with the exception that

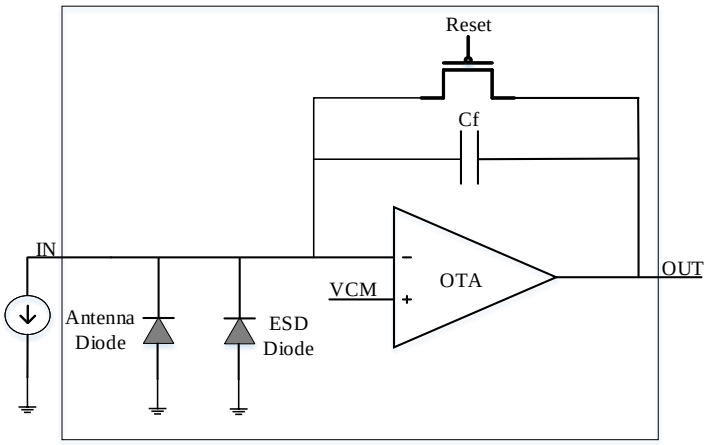


Figure 4.3: OTA integrator © 2019 IEEE

the ESD diode is not included. The feedback capacitance was chosen as 500 fF of the type medium oxide RF NCAP. The reset switch was realised using egullpfet with dimensions W/L = 160 nm/150 nm.

The architecture of the designed OTA is a folded cascode structure and the topology used is the same as that for UTOPIA 2 [21]. The input transistors determined the overall gain and the input leakage current of the chip. Hence, IO transistors with thick gate oxide were used as the input transistors. The schematic of the OTA is shown in Fig. 4.4. The bias voltages V1 and V2 were determined to be 0.35 V and 0.72 V respectively. A supply voltage of 1.2 V and a common mode voltage voltage of 0.6 V was used for the circuit.

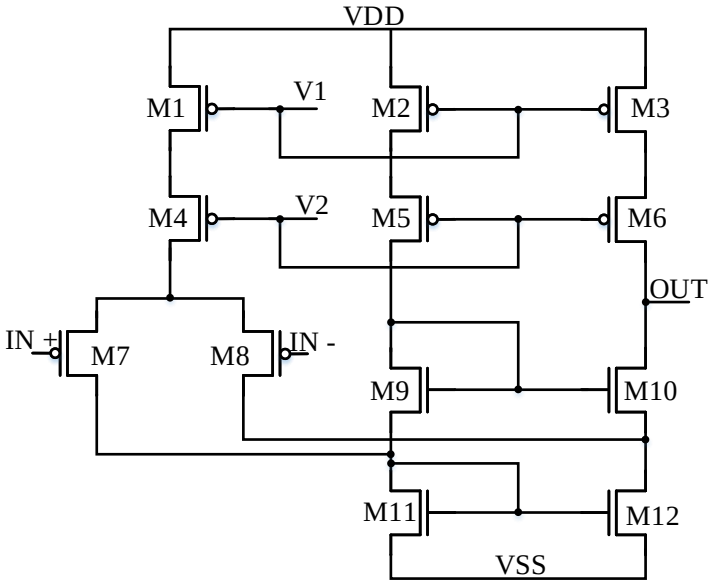


Figure 4.4: Folded Cascode OTA

Device	W (µm)	L (µm)
M1	160	1
M2	32	1
M3	32	1
M4	160	0.5
M5	32	0.5
M6	32	0.5
M7	192	0.2
M8	192	0.2
M9	32	0.5
M10	32	0.5
M11	64	1
M12	64	1

Table 4.1: Transistor dimensions

Transistors M7 and M8 were chosen to be of the type egullpfet, the thick gate IO transistor. Transistors M1 – M6 were realized using slvtpfet, super low-vt pmos. The NMOS transistors M9 – M12 were of the type slvtnfet, super low vt nmos. The transistors were dimensioned by using the gm/Id methodology as a guideline [67]. At the chosen operating conditions, the simulated gain was 78 dB and the gain bandwidth 222 MHz.

The layout of the test chip with the three channels is shown in Fig. 4.5. The dimensions of the test structure are 665 µm $\times$ 490 µm. Along with the supply voltage, the common-mode voltage and the bias voltages are also supplied by external circuitry. The input pads of channel 2 and 3 were placed with pads connected to common mode voltage on both sides to ensure similar leakage environment. To protect the gate oxides of the input transistors, antenna diodes were inserted.

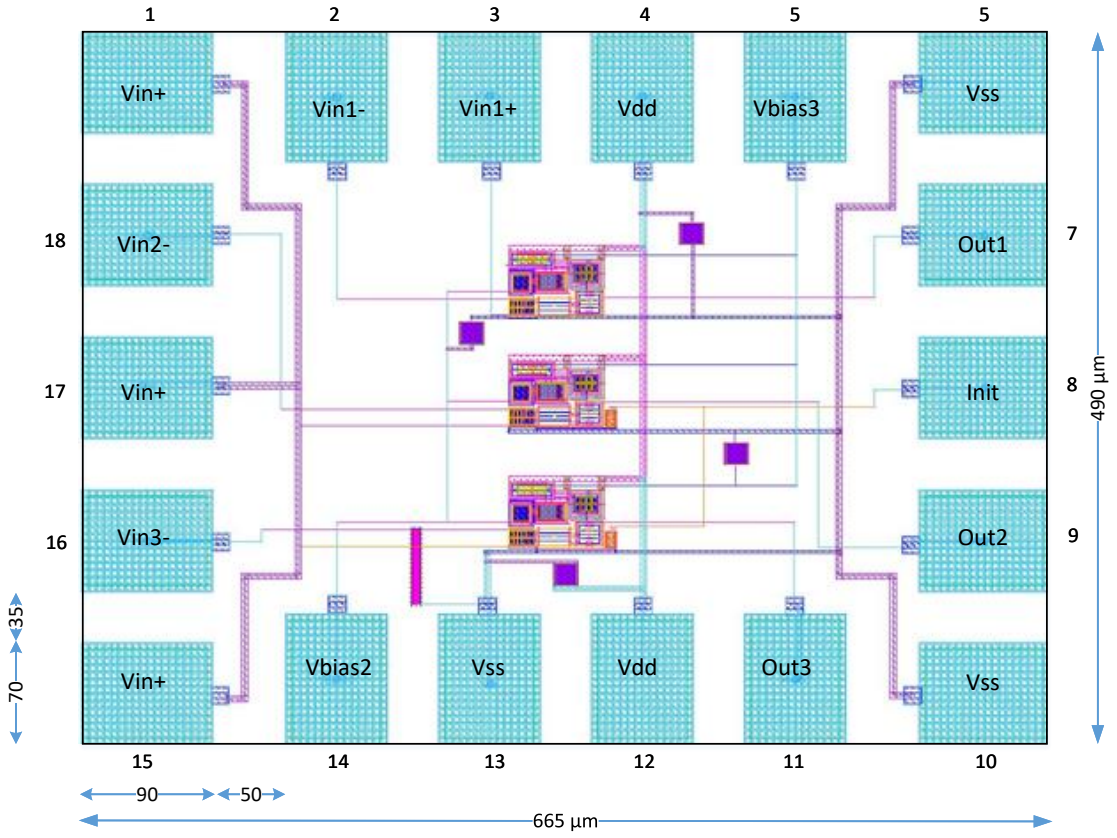


Figure 4.5: Layout of ACCURATE 0 © 2019 IEEE

4.3 Measured results

The test board used to characterize the chip is shown in Fig. 4.6. The chip was directly wire bonded onto the printed circuit board (PCB). A Keithley 6430 current source was used to generate precise currents for characterization. An Artix-7 based FPGA board was interfaced to the test board which programmed the digital to analog converters to generate the different bias voltages. The OTA output waveform was monitored using an oscilloscope, which in turn was connected to a MATLAB-based characterization platform through Ethernet. The entire board was shielded within a metallic box to avoid external interference.

The integrator output of channel 2 with the input current varying from -1 fA to -15 fA is shown in Fig. 4.7. An initial result pulse fixed the OTA output to the common voltage of 0.6 V. The output was integrated for 10 seconds to have a distinguishable slope for different currents while characterizing in the femtoampere range. It was observed that the ASIC was successful in distinguishing currents with a resolution of 1 fA. The integration slope is zero for a current of around -7 fA. This corresponds to the input bias current of the chip and is contributed by the drain leakage current of the reset switch, gate leakage of the input transistor, the leakage from

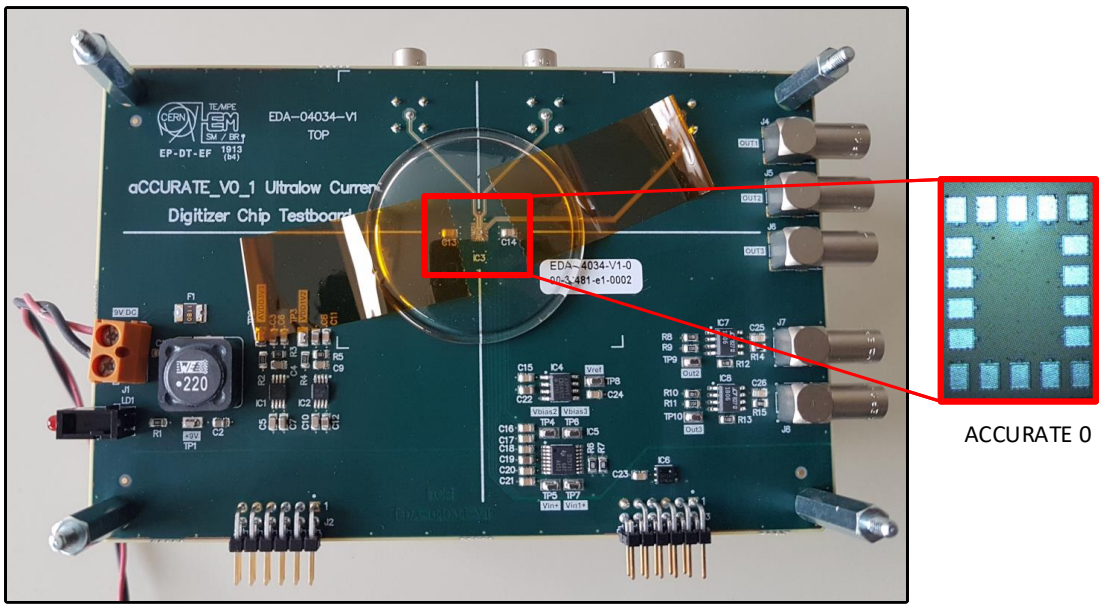


Figure 4.6: ACCURATE 0 test board

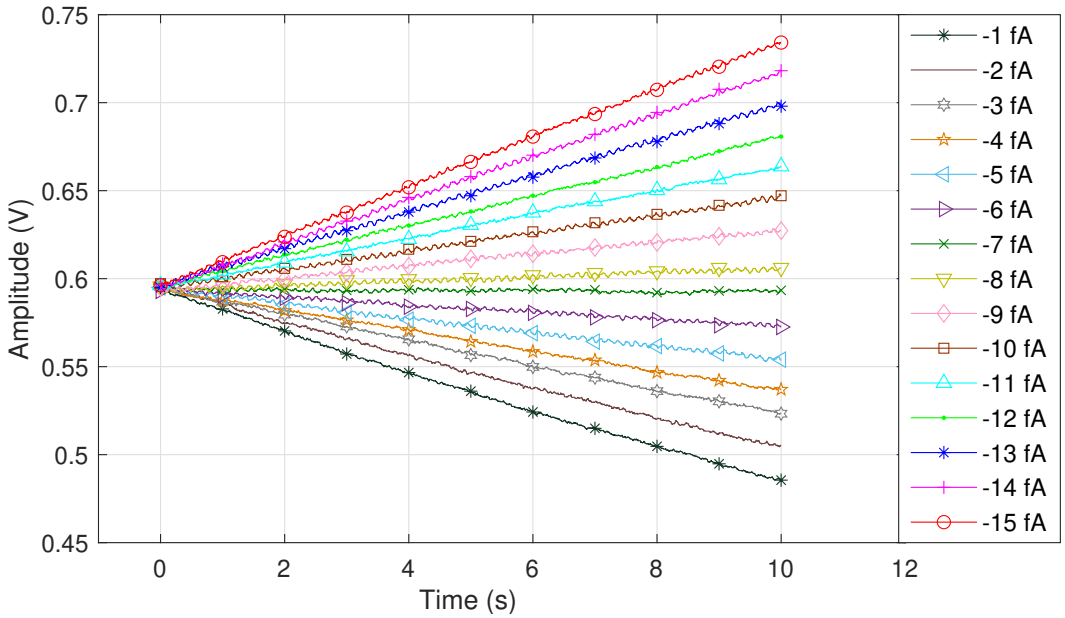


Figure 4.7: Channel 2 output with input current swept from −1 fA to −15 fA © 2019 IEEE

antenna diodes, leakage of the PCB track, and that of the input connectors. For currents above −7 fA, the OTA integrates in the positive direction.

Channel 3 was characterized to specifically measure the leakage contribution from the ESD diode. It was observed that the input bias current increased to around −240 fA. Thus, the ESD diode was found to be the main contributor to the leakage current for the CFC architecture in this technology.

Current estimate, I_{meas}, could be calculated from the OTA output.

$$I_{\text{meas}} = \frac{C_{\text{f}}(V_{\text{f}} - V_{\text{cm}})}{T\text{m}}. \tag{4.1}$$

Here, C_{f} is the feedback capacitance, V_{cm} is the common-mode voltage, which is the initial voltage at the output, V_{f} is the final voltage reached at the output in an integration time of T_{m}. Using 550 fF for C_{f}, for a measurement time of 10 s, the output was calculated and plotted as shown in Fig. 4.8. The linearity of the circuit can be seen from the plot in the measurement range of -1 fA to -15 fA. It can also be seen that the measurement accuracy increases with an increase in input current.

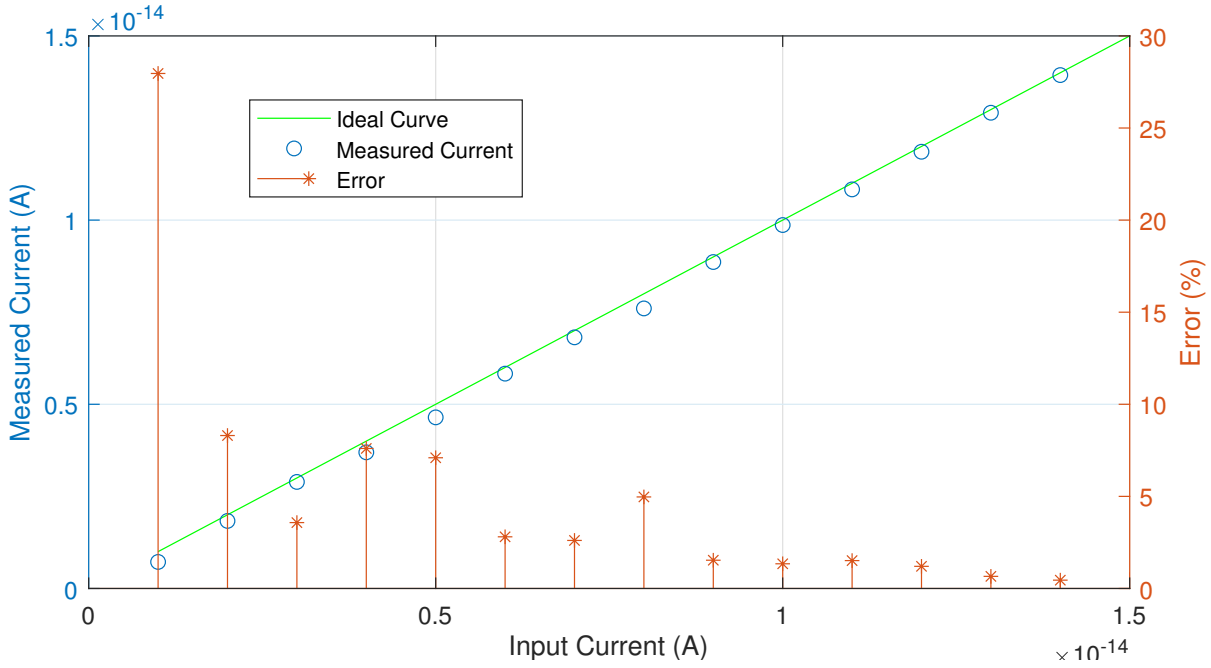


Figure 4.8: Linearity and error plot of channel 2 for currents from -1 fA to -15 fA © 2019 IEEE

The output of the channel 2 when the input current was swept from -1 pA to -1 nA can be seen in Fig. 4.9. It is seen that the output slope varies with the input current and with a much shorter integration time of 200 ns, the differentiation of the slope is evident. However, the chip cannot integrate for a long enough period to obtain a resolution in the femtoampere range since the integrator will saturate within the required time of 10 seconds for femtoampere sensitivity.

For the measurement, the reset signal generated externally by a pulse generator was held active for a few nanoseconds, corresponding to the minimum pulse width specification of the pulse source. For this duration, the OTA does not integrate and result in the initial nonlinear section in the output. Another interesting observation was the shift in the initial voltage from the set common-mode voltage. This shift arises from the transistor in the reset path. For the reset transistor, the drain to source voltage (Vds) increases as the input current increases since it is dimensioned targeting the lowest leakage possible. Since the transistor terminal connected

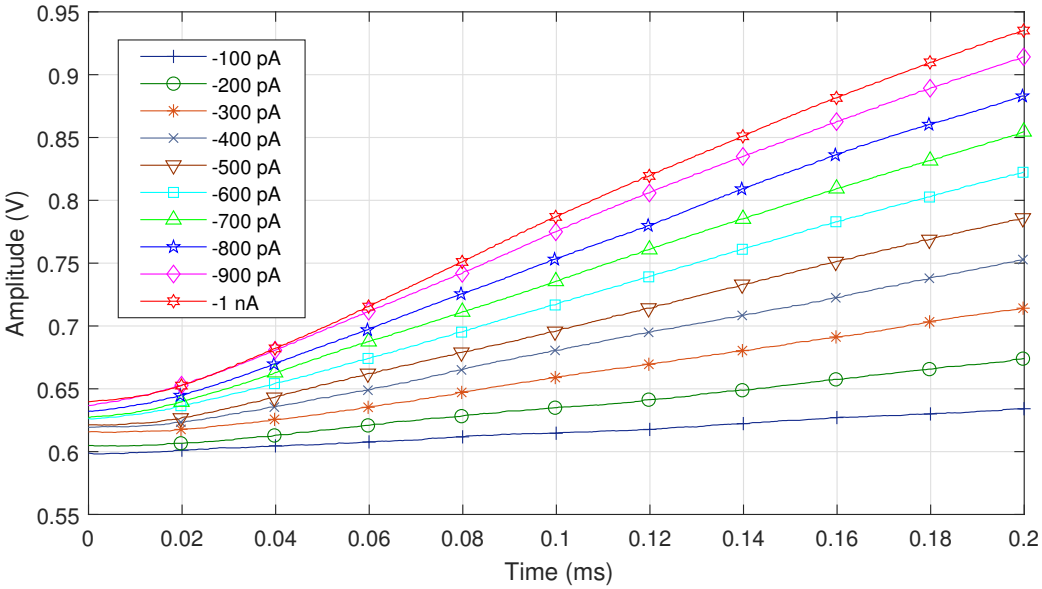


Figure 4.9: Channel 2 output for input current sweep of -1 pA to -1 nA © 2019 IEEE

to the input was biased at Vcm, the terminal connected to the OTA output increases to have higher Vds. This resulted in the initial output of the OTA deviating from Vcm. By changing the gate voltage applied to the reset transistor from the pulse generator, it could be seen that this deviation could be minimized. Further, in the simulations, it was found that the transistor could be dimensioned to have a good balance with the allowed leakage and permitted shift in initial voltage. In either case, it was, however, found that the slope of the integration remained constant for each input current.

4.4 Conclusion

The use of an advanced technology node for low current measurement applications was successfully demonstrated. With a careful choice of transistors and using a stable low valued capacitor, femtoampere sensitivity with an error margin of ± 0.5 fA was achieved for a very short duration of 10 seconds. It was found that the use of standard core transistors of the 22 nm technology is not feasible to precisely measure a femtoampere current since the leakage current in the picoampere would be difficult to compensate or calibrate. As in the study of UTOPIA 1 with the AMS 350 nm technology, the ESD diodes were again found to be the biggest contributor to the leakage current in a typical front end for low current measurement in the 22FDX technology. The technique of using thick gate IO transistors in the critical path was demonstrated and was further used in the design of the next version of ACCURATE chips.

Chapter 5

Technology Demonstrator ASIC in 130 nm Technology

The demonstration of femtoampere measurements in 22 nm technology established a methodology of using thick gate transistors in the critical path for low current measurements with advanced technology nodes. The leakage current of the typical front end including the ESD diodes was found to be around -240 fA, which would increase the complexity of the compensation methodology. The TSMC 130 nm technology being the mainstream technology node widely used at CERN was evaluated along similar lines for its leakage current performance. The technology extensively used in many high-energy physics applications has demonstrated the potential to be radiation hardened [68]–[70]. Although radiation hardness is not a specified requirement for the current version of the radiation monitors, future upgrades are projected in this direction. Hence, five different ASICs were designed in TSMC 130 nm to assess femtoampere measurement capability and to compare different current measurement topologies. These ASICs form the second generation of the ACCURATE series of ASICs and are hence named ACCURATE 1.

As outlined in Chapter 2, the various current measurement circuits developed in the radiation protection group at CERN have adopted different topologies. The literature review also showed that many architectures are used for the front ends of radiation monitors. Hence, a detailed analysis of three main current measurement topologies that were primarily used in the legacy systems was carried out. This chapter delves deep into the intricacies of those architectures. The summary of the analysis and the findings are published in [71].

5.1 Analysis of different current measurement architectures

All of the topologies are built around the current to frequency conversion principle. The input charges are collected by a capacitor and topologies aim to measure the slope of the integration. The slope measurement is attained in multiple ways.

5.1.1 Reset counting method

The latest generation of radiation monitoring system installed at CERN [61] is based on this method. The block diagram of the architecture is shown in Fig. 5.1

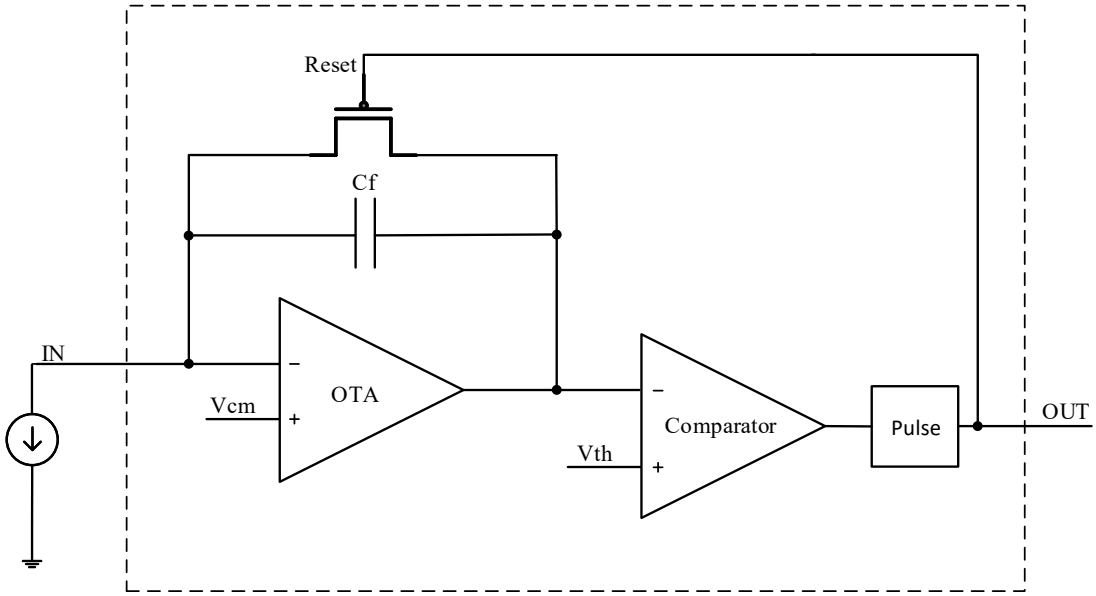


Figure 5.1: Reset counting method

The input current is integrated into the feedback capacitor Cf. The OTA output increases linearly from the common-mode voltage Vcm. When this output reaches the threshold voltage of the comparator Vth, the comparator output switches. This enables the pulse generator which generates a pulse. This pulse resets the switch across the feedback capacitor, bringing back the OTA output to the initial level. The pulse duration is designed to discharge fully the feedback capacitor. The various signals of the circuit are shown in Fig. 5.2.

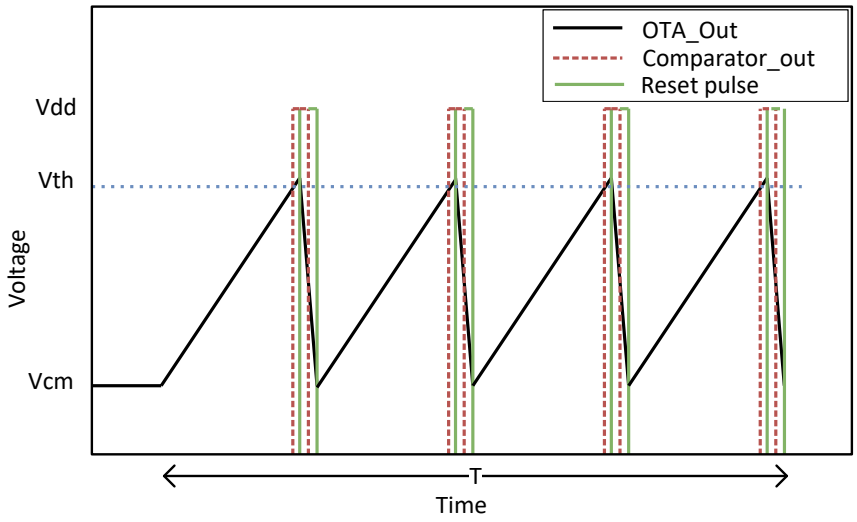


Figure 5.2: CFC output in the reset counting method

In an ideal circuit, the number of pulses generated in a fixed time is proportional to the input current. The current I_{in} can be calculated as

$$I_{\mathrm{in}} = \frac{NC_{\mathrm{f}}(V_{\mathrm{th}} - V_{\mathrm{cm}})}{T}, \tag{5.1}$$

where T is the time of integration, N the number of pulses generated in time T, and V_{cm} is the common-mode voltage of the OTA. For an input current swept from 1 pA to 50 pA on a feedback capacitor of 1 pF for a measurement time of 10 s, the output is as shown in Fig. 5.3. The common-mode voltage was taken as 1.6 V and the threshold voltage as 2.5 V.

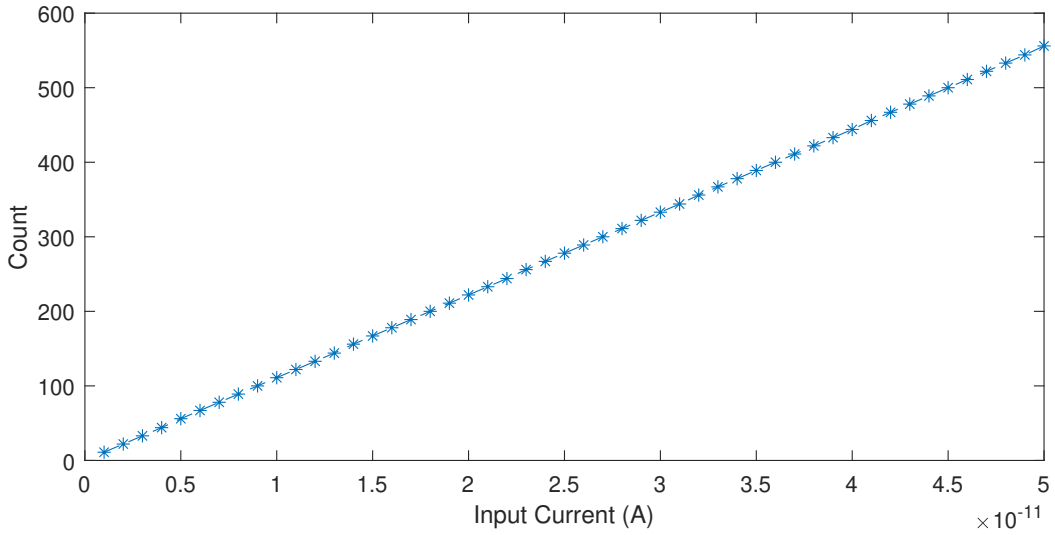


Figure 5.3: Ideal output of the reset counting CFC

However, many non-idealities can affect the current calculation. These are explained in the following sections.

5.1.1.1 Duration of the reset pulse

The reset pulse duration is dependent on the values of Cf and the on-resistance of the reset switch. For a definite reset time, the number of pulses received in T will be less than in the ideal case. The reset time T_{rst} can be included in the calculation of the current to minimize the error. Thus (5.1) can be modified to

$$I_{\mathrm{in}} = \frac{NC_{\mathrm{f}}(V_{\mathrm{th}} - V_{\mathrm{cm}})}{T - NT_{\mathrm{rst}}}. \tag{5.2}$$

The effect of the reset time with the following parameter values can be evaluated: I_{in} = 10 µA, C_{f} = 1 pF, V_{th} – V_{cm} = 1 V and T = 0.1 s. The plot in Fig. 5.4 shows the improvement in measurement error when the correction factor is applied for different currents.

It can be seen that applying the correction factor greatly improves the accuracy by nullifying the effect of the reset time. The error plotted arises from quantization since the count N is an

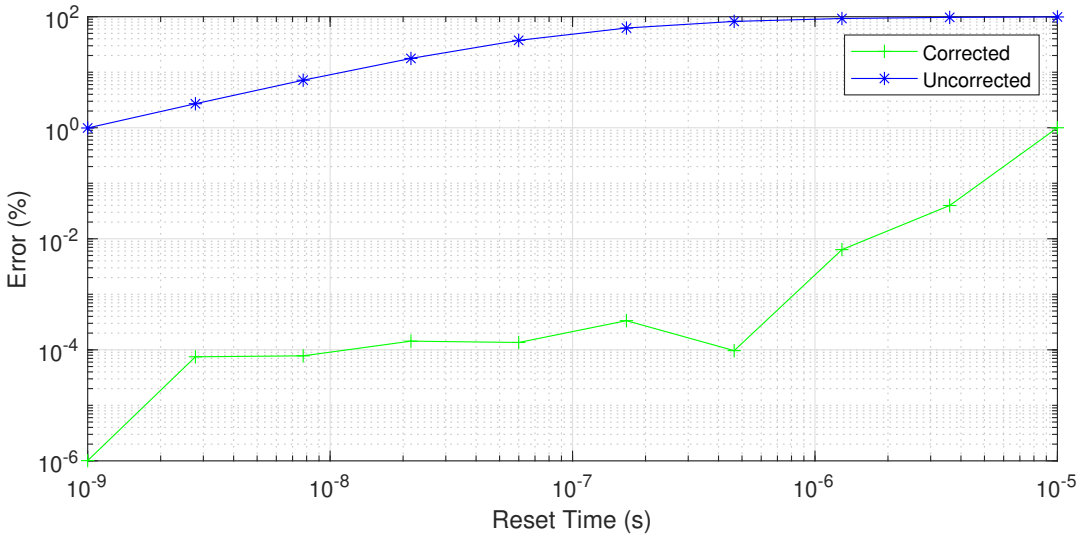


Figure 5.4: Effect of reset time on current calculation in the reset counting method

integer. The impact of the correction is valid only for $T \gg T_{\mathrm{rst}}$. The nominal value for the measurement time used in most radiation monitoring systems at CERN is 100 ms. The reset time can be calculated as

$$t = R_{\mathrm{on}}\, C_{\mathrm{f}}\, \ln\left(\frac{V_{\mathrm{init}}}{V_t}\right), \tag{5.3}$$

where R_{on} is the resistance of the transistor used as the reset switch when it is turned on, V_{init} is the initial voltage across the capacitor, and V_t is the final voltage. For a transistor with W/L = 4 µm / 350 nm, the on-resistance is found to be around 600 Ω. Thus, for a reset structure with two transistors in series, the total R_{on} is 1.2 kΩ. Using the value from the previous calculation, for a 1 pF capacitor, T_{rst} can be calculated as 6 ns. The condition is thus met, and the effect of the reset time can be compensated.

5.1.1.2 Comparator delay

The comparator in the data path also affects the number of pulses that will be generated. A finite comparator delay results in a lower number of pulses than in the ideal case. The effect is very similar to that of the reset time and hence can be compensated in the same way, provided the delay remains constant. The main difficulty here is that, as the input current changes, the slope of the signal that is fed to the comparator changes. This slope directly affects the rise and fall time of the output of the comparator. Thus, the delay varies slightly with the input current, making the compensation difficult.

5.1.1.3 Comparator threshold

A change in the comparator threshold manifests directly as the gain of conversion as it affects the amount of charge that is reset in each reset cycle. The threshold voltage change ΔV_{th} can be

included in the current calculation as

$$I_{\mathrm{in}} = \frac{NC_{\mathrm{f}}(V_{\mathrm{th}} - V_{\mathrm{cm}} + \Delta V_{\mathrm{th}})}{T}. \tag{5.4}$$

5.1.1.4 OTA offset

A finite OTA offset also affects the current calculation. The modified equation is

$$I_{\mathrm{in}} = \frac{NC_{\mathrm{f}}(V_{\mathrm{th}} - V_{\mathrm{cm}} - V_{\mathrm{os}})}{T}, \tag{5.5}$$

where V_{os} is the OTA offset. The initial voltage from which the integration starts is $V_{\mathrm{cm}} + V_{\mathrm{os}}$.

5.1.2 Direct slope measurement method

The simplest method for slope measurement is to measure the time difference between two defined levels on the integrator output. The circuit for this method is shown in Fig. 5.5.

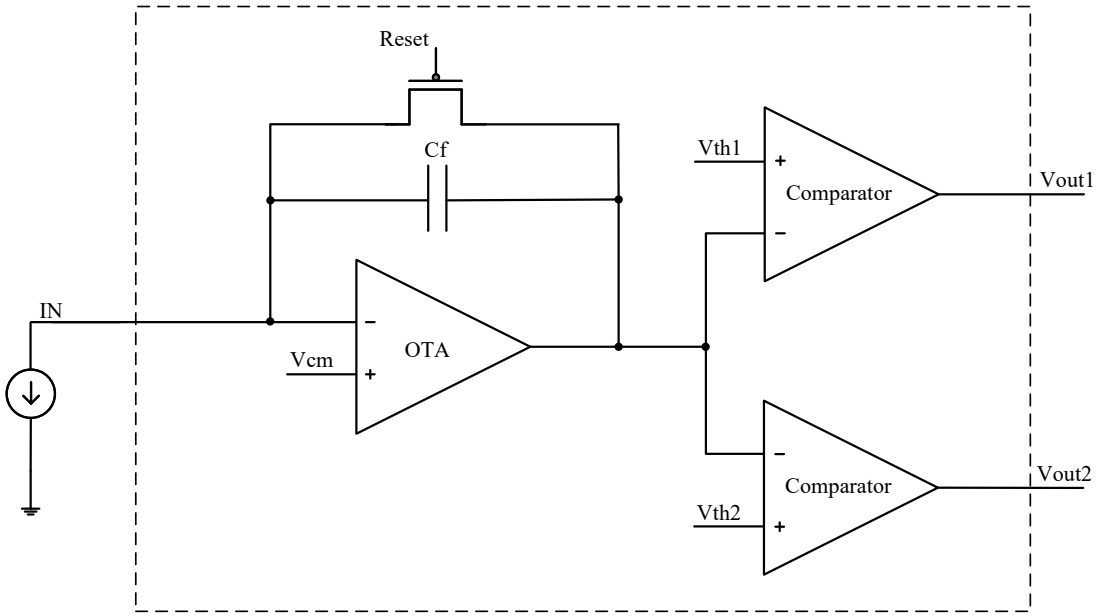


Figure 5.5: Direct slope measurement method

The output of the OTA is fed to two comparators with threshold voltages V_{th1} and V_{th2} with V_{th2} $>V_{\mathrm{th1}}$. The time of integration from the initial voltage until the first comparator is asserted is recorded as t_1. The time when the OTA output reaches V_{th2} is measured as t_2. The input current can be calculated as

$$I_{\mathrm{in}} = \frac{C_{\mathrm{f}}(V_{\mathrm{th2}} - V_{\mathrm{th1}})}{t_2 - t_1}. \tag{5.6}$$

The output of the comparators Vout1 and Vout2 can be used to start and latch a counter output to measure the time interval $t_2 - t_1$. As Vout2 is asserted the counter is reset and the reset switch of Cf is enabled to start the next measurement cycle.

The different factors affecting the accuracy of measurement are detailed further.

5.1.2.1 Noise in the OTA output

The method depends heavily on the accuracy of the time measurements t_1 and t_2. Noise in the output of the OTA can trigger the comparators multiple times, resulting in erroneous measurement. The comparator switching needs to be debounced to avoid the wrong triggering of the counter. The debouncing logic needs to be implemented in the readout section before feeding the comparator edges to the counter. The comparator threshold also should have hysteresis to accommodate any fluctuations arising from the noise in the circuit.

5.1.2.2 Comparator delay

The delay in the comparator affects t_1 and t_2. When the comparators are perfectly matched, the delay gets canceled out. However, as the threshold voltages are different, the delays are also different. When the input current increases, along with the variation in input slope, the delay of the comparator also varies. Hence, for higher currents, this method becomes erroneous.

5.1.2.3 Comparator threshold

As in the case of comparator delay, if the threshold changes with the same magnitude for both the comparators, the effect is nullified. The accuracy of the voltage generator creating the comparator threshold voltages also affects the switching threshold. Using more comparators, a different point on the slope of integration can be calculated and the non-ideal effects could be averaged to a great extent.

5.1.2.4 Resistor values

To provide the hysteresis, resistors are needed. The resistors modify the current calculation as

$$I_{\mathrm{in}} = \frac{C_{\mathrm{f}}(V_{\mathrm{th2}} - V_{\mathrm{th1}})R_1}{(t_2 - t_1)(R_1 + R_2)}, \tag{5.7}$$

where R_1 and R_2 are the feedback resistors to define the threshold points. R_1 is introduced between comparator output and its non-inverting terminal and R_2 between the external threshold voltage and the non-inverting terminal. The use of larger resistors can minimize the impact of non-ideal values. The resistor values can be calibrated to minimize errors.

The OTA offset does not affect the current measurement in this method as it gets canceled in the calculation.

5.1.3 Charge balancing method

This is the most widely used method in low current measurement systems [26]. The architecture is shown in Fig. 5.6. Instead of resetting the feedback capacitor as in the reset counting method,

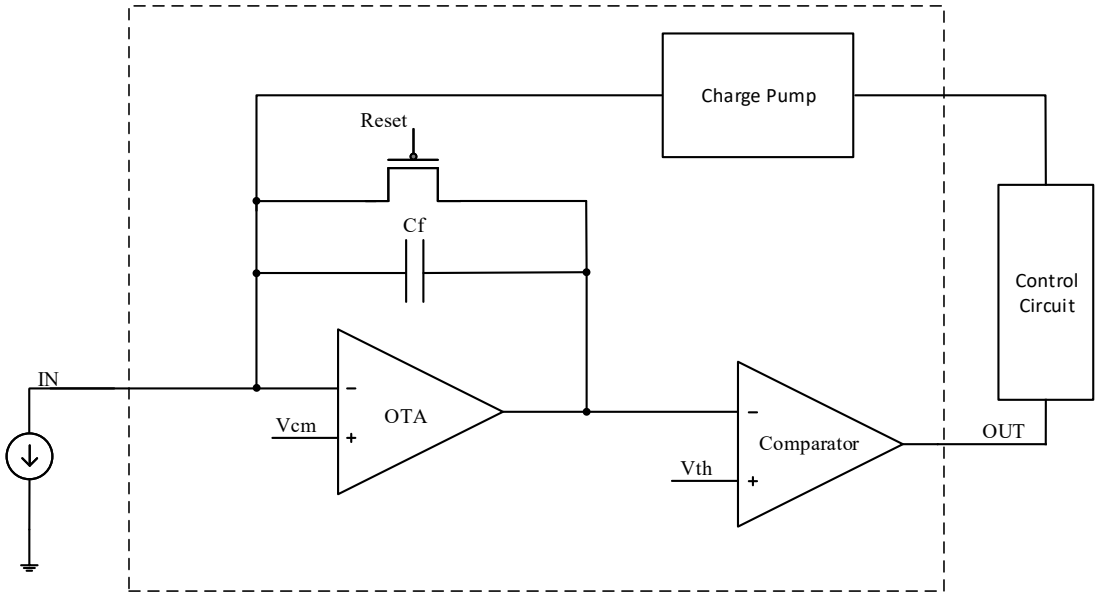


Figure 5.6: Charge balancing method

a fixed amount of charge is injected into the input node discharging Cf whenever the comparator output is high. The charge injection is managed by a control circuit and the charges are generated in a charge pump. After the charge injection, the charge pump restores a predefined amount of charge. The number of times the charge is injected N is proportional to the current to be measured.

$$I_{\mathrm{in}} = \frac{NQ_{\mathrm{ref}}}{T}, \tag{5.8}$$

where T is the time of measurement and Q_{ref} is the quanta of charge that is injected each time.

This method is not affected by comparator parameters such as the threshold and delay as long as they remain constant. The quantum of charge that is subtracted in each cycle is

$$C_{\mathrm{ref}} V_{\mathrm{ref}} = C_{\mathrm{f}}(V_{\mathrm{th}} - V_{\mathrm{f}}). \tag{5.9}$$

The feedback capacitor is discharged from the initial voltage of V_{th}, the threshold voltage of the comparator, to a final voltage V_{f}. Any change in V_{th} is absorbed in V_{f}, hence maintaining the same charge.

The main challenge in this methodology is the creation of an accurate reference charge. The various factors affecting the current calculation in this method are summarized below.

5.1.3.1 Capacitor values

The charge generation is attained by switched capacitors which are fed with a fixed voltage. The amount that is accumulated in these capacitors varies with their value. This value needs to be calibrated to correct the error in capacitor values.

5.1.3.2 Switched capacitor non-idealities

Charge injection and clock feedthrough are two effects that further affect the accuracy of the charge generated in the switched capacitors. These effects can be minimized with the sizing of the transistor switches and by supplying stable accurate clocks [21].

5.1.3.3 OTA offset and input bias voltage

The voltage present at the input terminal of the OTA also contributes to the errors accumulated in reference charge generation. In the discharge cycle, when the switched capacitor is connected to the input path, the amount of charge that is injected is dependent on the voltage at that node. If the input terminal is at a voltage that is different from the common-mode voltage, the charge that is transferred gets modified. The current calculation is affected as well.

$$I_{\text{in}} = \frac{NC_{\text{ref}}(V_{\text{ref}} - V_{\text{inp}})}{T}, \tag{5.10}$$

The voltage V_{inp} is the error voltage at the input with respect to the common-mode voltage and includes the OTA offset.

5.2 Leakage current evaluation

As evident from the literature survey presented in Chapter 3, the majority of low current measurement applications are reported in 350 nm or higher nodes. No published literature were available where a current measurement with femtoampere sensitivity and a dynamic range extending into the microampere range were obtained. Hence, it was essential to evaluate how the TSMC 130 nm technology would fare in achieving low leakage and the wide dynamic range in order to design a front end for the ionization chambers that meets all the requirements.

A simple transistor characterization was performed in Spectre for different transistor variants in this technology. The transistors of the AMS 350 nm technology were taken as the reference for comparison. The plot of drain-to-source current when the gate-to-source voltage was swept for the NMOS transistors of the TSMC 130 nm technology and the AMS 350 nm technology is shown in Fig. 5.7. The transistors were dimensioned to have a width and length of 1 µm. The source and bulk terminals were tied to the ground. The drain to source voltage applied was 0.1 V. This value was chosen as this was the maximum voltage that was observed across the drain to source terminals of the leakage critical switches in the architecture considered in the study. The off current extracted, corresponding to a zero gate-to-source voltage, was found to be 40 fA for the AMS 350 nm NMOS core transistor. For the TSMC 130 nm core transistor, it was found to be 178 pA, and for the corresponding thick gate IO transistor, the simulated leakage was 460 fA.

Similar simulations were performed for the PMOS transistors of both the technologies with the same dimensions and drain to source voltage. The plot is shown in Fig. 5.8. For the PMOS, the

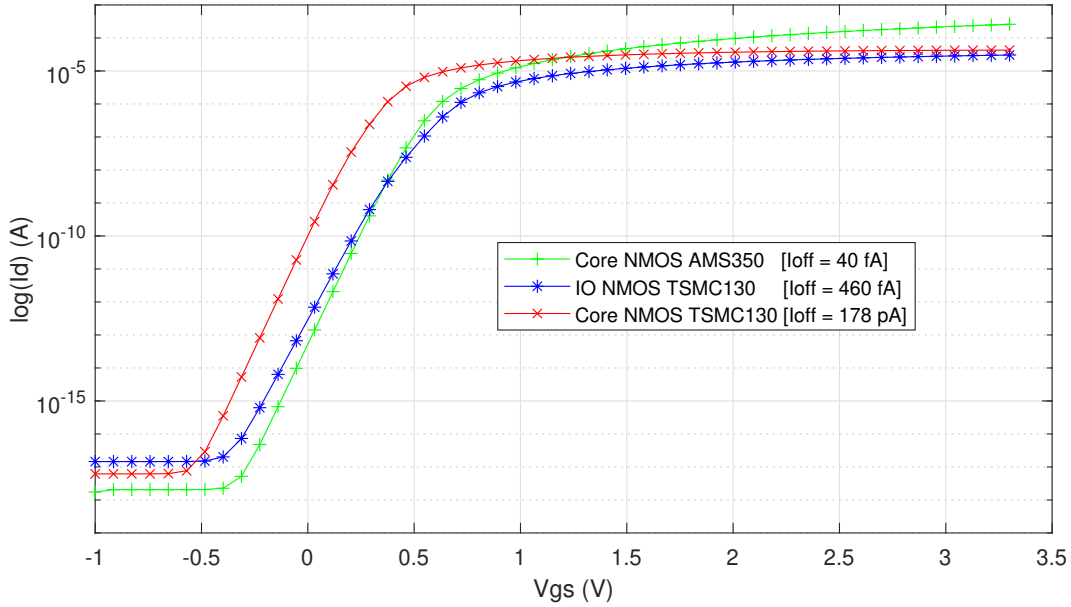


Figure 5.7: Drain current characteristics for TSMC 130 nm and AMS 350 nm NMOS transistors with W/L = 1 µm/1 µm and Vds = 0.1 V

observed off currents were 22 aA for the AMS 350 nm core transistor, 33 fA for the TSMC 130 nm IO transistor, and 74 pA for the core transistor.

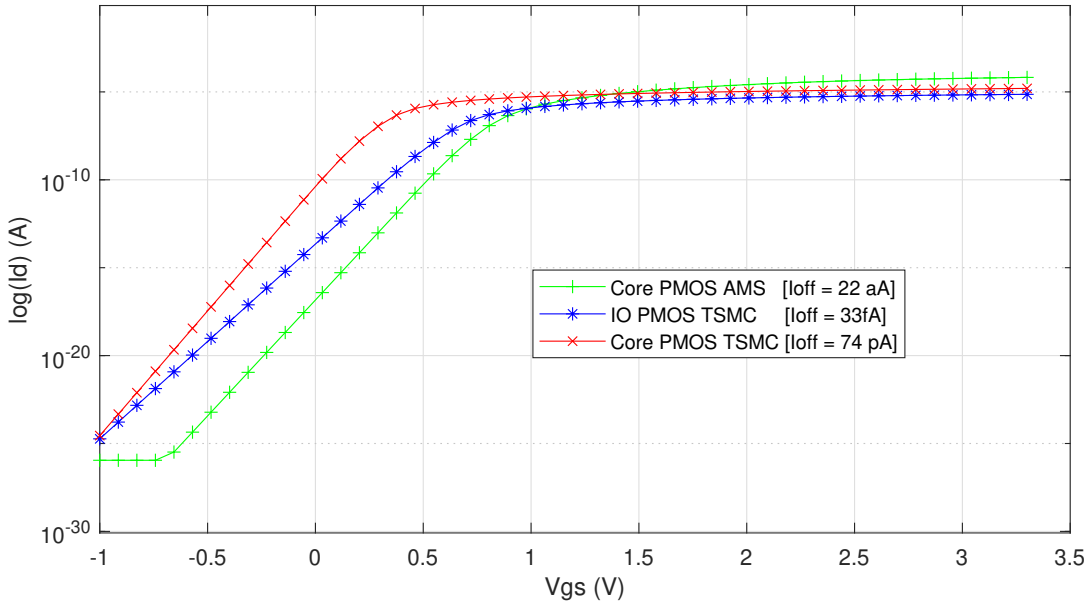


Figure 5.8: Drain current characteristics for TSMC 130 nm and AMS 350 nm PMOS transistors with W/L = 1 µm/1 µm and Vds = 0.1 V

From the simulations, it was evident that the leakages for the TSMC core transistors would be of the order of picoamperes. For measuring with femtoampere sensitivity, it would be very difficult

to compensate. Hence, for all the series switches that would influence the current calculation, usage of a core transistor was ruled out. When the technology feature size is reduced, they suffer also from the reduced thickness of the gate oxide and the various gate leakage currents could also become significant in ultra-low current measurements. It was not possible to estimate the gate leakage current of the TSMC 130 nm transistors as they were not included in the available transistor models. However, a thick gate IO transistor rated for 3.3 V was estimated to have very low leakage and was hence the best option for the input transistors of the current measurement circuit.

Unlike the study with the GD22FDX, where the low leakage transistors were used only in the input path and for the switches, it was decided to have the entire current measurement circuit designed using 3.3 V IO transistors. This simplifies the design and avoids the possibility of the high voltage appearing across any transistor beyond its specified maximum. Thus, various architectures for current measurement were implemented in five different ASICs using the thick gate transistors of TSMC 130 nm technology.

5.3 System design

The current measurement topologies were evaluated using different ASICs designed in the TSMC 130 nm technology. The architecture of channel 1 of different ASICs designed is detailed in Fig. 5.9.

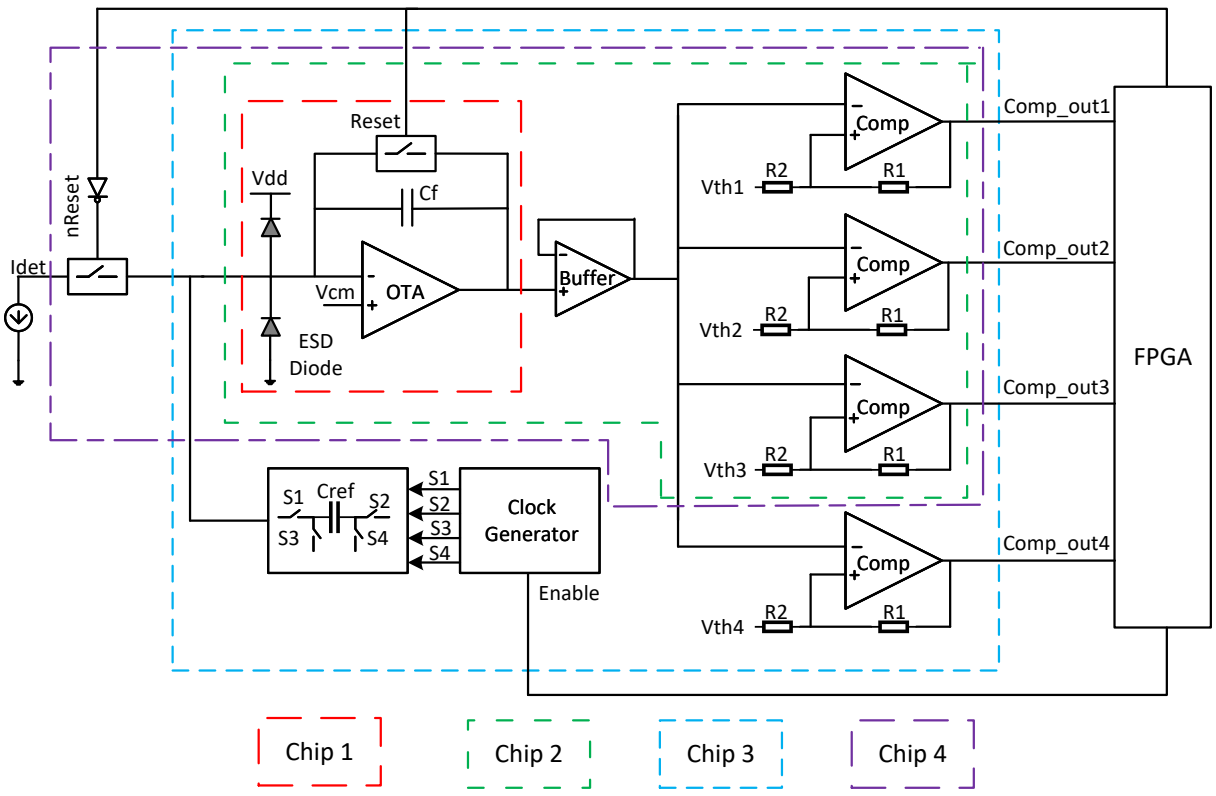


Figure 5.9: System architecture of ACCURATE 1

In Chip1, an OTA is configured as an integrator with a reset. The OTA used in the ASIC is similar to the one described in Chapter 4. The folded cascode OTA of the UTOPIA 2 ASIC [21], originally designed in AMS 350 nm technology, is adapted for the TSMC 130 nm technology. There are two channels in the chip of which the first is shown in the figure. The second channel is identical to the first one, without the ESD diodes. The chip aims to determine the achievable sensitivity of the current measurement in this configuration for the 130 nm technology. The chip also helps to estimate the leakage current associated with the ESD diodes. To determine the leakages, the input current is swept in the femtoampere range and the point where the slope of integration is close to zero is determined. The same when repeated with both channels helps to determine the leakage current contribution from the ESD diodes.

Chip 2 aims to evaluate the current calculation with the reset counting method and direct slope method. Apart from the integrator in Chip1, there are three comparators and a buffer that feeds the integrator output to the comparators. A classical two-stage OPAMP [72] is used for the comparator and buffer realization. The comparators have progressively increasing threshold voltages which could be externally tuned. To provide sufficient debouncing, hysteresis is introduced into the comparator threshold voltages with the feedback resistors R1 and R2. The upper and lower threshold points are hence calculated as

$$\mathrm{UTP} = V_{\mathrm{th}} + (V_{\mathrm{satp}} - V_{\mathrm{th}})\,\frac{R_2}{R_1 + R_2}, \tag{5.11}$$

$$\mathrm{LTP} = V_{\mathrm{th}} + (V_{\mathrm{satn}} - V_{\mathrm{th}})\,\frac{R_2}{R_1 + R_2}, \tag{5.12}$$

where V_{satp} and V_{satn} are the positive and negative saturation voltages of the comparator. It was experimentally found that a value of 20 KΩ for R_1 and 3 KΩ for R_2 provided sufficient immunity against noise-related triggering in the standard measurement conditions.

Three points on the integration slope could be found from the outputs of the three comparators – (Vth1:t1), (Vth2:t2), (Vth3:t3). Hence, three sets of values for the input current could be calculated from three different time intervals ($t_2 - t_1, t_3 - t_2$, and $t_3 - t_1$). An average of the three values gives a better result. The output of the third comparator also triggers a pulse which will reset the feedback capacitor. These reset pulses can be used to make the current calculation with the reset counting method. V_{th} in equation 5.1 can be replaced with V_{th3} to get the current estimate.

The charge balancing method was evaluated using Chip 3. Hence, in addition to comparators, a charge generation block is present. When the comparator 4 output is asserted, a pulse of fixed on and off time is generated by the FPGA. This pulse is delayed by a few nanoseconds on the clock generator block to create different control signals for the switched capacitor block. The capacitor C_{ref} is first charged to a voltage V_{ref} in the first phase of operation. In the second phase, the charged capacitor is connected to the input, thereby discharging the feedback capacitor Cf by an amount of charge

$$Q_{\mathrm{ref}} = C_{\mathrm{ref}} V_{\mathrm{ref}}. \tag{5.13}$$

The durations of the control signals S1 – S4 are managed so that sufficient time is available for the C_{ref} to charge to the reference voltage and the discharge is also complete. The chip also generates the comparator outputs for current calculation with the direct slope method as in Chip 2.

In the case of the reset counting method, the measurement circuit is blind for the duration for which the feedback capacitor is held in reset. Any charges that are generated by the ionization chamber during this time interval are lost. This dead time can result in loss of accuracy in collected charges, especially for pulsed input currents with short pulse duration. To mitigate this limitation, a popular solution applied for legacy systems at CERN is to introduce an input switch that is turned off when the reset switch is turned on. This effectively blocks any flow of charges from the ionization chamber into the measurement circuitry during the reset phase. The timing of the activation of the two switches is also accurately controlled from the FPGA such that, first, the input series switch is turned off and then the reset switch is turned on. The series switch has the potential to act as a charge buffer in case the off resistance of the switch is not sufficiently high. Chip 4 was designed with this series switch to study the effects of such a switch in the input path, especially for very low current measurements.

Chip 5 is very similar to Chip 2 and is hence not separately shown in the system architecture. The difference is that the comparators are designed without hysteresis. The noise that can lead to false switching of the comparator was dealt with only using the debouncing logic in the FPGA. This chip is aimed at evaluating the effectiveness of different debouncing strategies.

All the chips except Chip 3 have a second channel identical to the first channel aiming to measure the leakage currents. The chips are designed as analog blocks and all of the digital calculation and control signal generation is carried out by an FPGA. The comparator outputs are received by the FPGA and the various counts, such as the number of reset pulses and the time interval between different comparator outputs, are calculated. The generation of the reset pulse of the feedback capacitor, enabling of the pulse for the clock generation block, the timing of the pulse for the charge injection, and the control of the series switch are all handled by the FPGA. The clock frequency of the FPGA is 100 MHz. A granularity of 10 ns was required, mainly for the generation of precise pulse signals for charge injection. The data processed in the FPGA is sent out through a serial interface for further analysis.

5.4 Current measurement limits

The highest and the lowest currents that can be measured using different current measurement topologies are evaluated in this section.

5.4.1 Lower limit

Theoretically, there is no strict lower limit for the current that could be measured with any of the current measurement topologies discussed. However, limitations are imposed by the cumulative

leakage currents in the whole measurement system that could not be calibrated. The leakage contribution comes from a plethora of sources – from the source generating the current, the cables and connectors through which it is transported to the measurement system, the leakages from the transistors of the chosen technology node, variations in the ambient temperature in the measurement set-up, etc.

For all three methods, it is imperative to optimize the transistors of the reset switch since they sum up directly to the injected current. The charge balancing method has additional switches from the charge generation block, which adds further to the leakage. The series input switch that would be needed in the reset counting method also contributes to increased leakage. It was also well seen from [18] and [73] that ESD diodes play a huge role in leakage current contribution both in AMS 350 nm and GF22FDX technologies.

The key factor in any low current measurement system is the ability to determine the leakage and compensate for this leakage from the actual measurement. As the magnitude of leakage current increases, the difficulty of sieving out the desired current from the cumulated measured current increases. It boils down to how accurately the time difference in integration with and without leakage current is determined. This time difference could be calculated as

$$\Delta t = \frac{C_{\mathrm{f}} \cdot \Delta V \cdot I_{\mathrm{min}}}{I_{\mathrm{leak}}(I_{\mathrm{leak}} + I_{\mathrm{min}})}, \tag{5.14}$$

or

$$\Delta t \cong \frac{C_{\mathrm{f}} \cdot \Delta V \cdot I_{\mathrm{min}}}{I_{\mathrm{leak}}^2}. \tag{5.15}$$

C_{f} is the feedback capacitor, ΔV is the difference between the initial voltage at the integrator output and the threshold voltage to which it integrates, I_{leak} is the leakage current in the system and I_{min} is the minimum measurable current. While calculating the time difference for a system to measure a 1 aA current with 1 pA leakage, C_{f} of 1 pf, and ΔV of 0.1, the value is 100 ns. This value, although theoretically possible, is so small in magnitude that any variation in the leakage current from the temperature, voltage, and process variation can affect the compensation. Thus, an absolute lower current limit is difficult to estimate.

5.4.2 Upper limit

The various non-idealities mentioned in the previous section affect mainly the maximum current that can be measured by a topology. Many of those effects can be compensated by appropriate correction coefficients and by calibration. However, beyond a certain limit, the corrections fail to work. Apart from those listed factors, certain circuit-specific parameters also limit the current measurement in each of the methods. A circuit that is common to all the methods is the input integrator. The OTA that is used to realize the integrator has certain limitations.

The folded cascode OTA of current implementation has a bias current of around 140 µA. When the input current increases beyond the bias current, the OTA loses its linearity. The

common-mode voltage to which the output of the OTA has initialized changes when the current increases beyond the nominal bias current. The output stage of the OTA which sinks the input current will not be able to take in more current and loses its stable operation. Hence, to be able to measure current in the higher microampere range or milliampere range, the OTA must be redesigned with a higher bias current.

It was also observed from the studies with the GF22FDX chip in Chapter 4 that the sizing of the transistors of the reset switch affects the initial voltage at the integrator output. The reason was the shifting of the drain terminal of the reset switch to match the high input current by increasing the drain-to-source voltage of the transistor switch. It was found with Spectre simulations that a shift of around 300 mV is caused at the OTA output when the input current is changed from 1 µA to 10 µA while using the minimum-sized transistors. This shift increases with the input current. The effective voltage headroom reduces and hence it affects the current calculation as the OTA output reaches the saturation voltage. To decrease this shift in the output, the transistor must be dimensioned to have a higher drain current. This adversely affects the leakage current.

5.4.2.1 Reset counting method

The various non-idealities affecting the measurement in the reset counting method were elaborated in the previous section. Considering all the effects, the modified measured current is given by

$$I_{\mathrm{in}} = \frac{N\alpha\, C_{\mathrm{f}}(V_{\mathrm{th}} - V_{\mathrm{cm}} - V_{\mathrm{os}} - \Delta V_{\mathrm{th}})}{T - NT_{\mathrm{rst}} - \beta N T_{\mathrm{c}} - T_{\mathrm{d}}}, \tag{5.16}$$

In the equation, ΔV_{th} is the correction for the change in comparator threshold voltage, T_{c} and T_{d} are the delays from the comparator and the digital logic in the FPGA, respectively. Two other correction factors included are α and β. The value of the feedback capacitor is calibrated to obtain α. The comparator delay is dependent on the input current. Hence, it is a variable that must be corrected differently for different input currents. Hence, the correction factor for the comparator delay β is associated with the number of reset counts N, which is again proportional to the input current. This is the most difficult value to determine by calibration. It was found that β varies with different current bands and hence acts as the main limiting factor for having accurate measurement beyond a certain limit.

The total delay from the comparator and the logic section plays a pivotal role in determining the maximum current measurable in this method. For a 3.3 V system with a 1 pF capacitor, with a total delay of 50 ns, an input current of 15 µA pushes the integrator output to saturation. Thus, optimizing the total delay in the measurement path from the comparator input to the reset switch output can help in increasing the maximum current range.

5.4.2.2 Direct slope method

Among the three methods, this method has the lowest maximum current threshold. The reason is the challenge in measuring fine time intervals. In the above example system, when the

input current is 5 µA and the threshold voltage difference of the comparators is 0.1 V, the time interval to be measured accurately is 20 ns. This value decreases as the current increases. The measurement error proportionally increases. Also, since the method is prone to debounce, different debouncing logics are applied to eliminate the influence of noise. The strength of debouncing is determined by the values of the feedback resistors and the logic in the FPGA. As the current to be measured increases, the probability of treating the small time interval as an influence of noise by the debouncing logic increases. Thus, to have good immunity to noise, the maximum current that can be measured needs to be limited.

5.4.2.3 Charge balancing method

In the current implementation of this method, the limiting factor in the maximum current that can be measured comes from the switched capacitor section. A definite time is required for the capacitor to charge to the reference voltage and to discharge it completely to the input node. The time of charging and discharging determines the maximum current that can be measured.

$$I_{\text{max}} = \frac{V_{\text{ref}}}{5(R_{\text{on1}} + R_{\text{on2}})}. \tag{5.17}$$

Here, R_{on1} is the series on-resistance of the transistor switch through which the capacitor is charged to the reference voltage and R_{on2} is the corresponding resistance of the transistor which connects the capacitor to the input node. For a reference voltage of 1 V, the simulated maximum current in the implemented system is found to be 2.6 µA.

5.5 Measurement results

The test chip is characterized in a set-up very similar to the one used for characterizing UTOPIA 2 and ACCURATE 0. The ACCURATE 1 chip and its PCB are shown in Fig. 5.10.

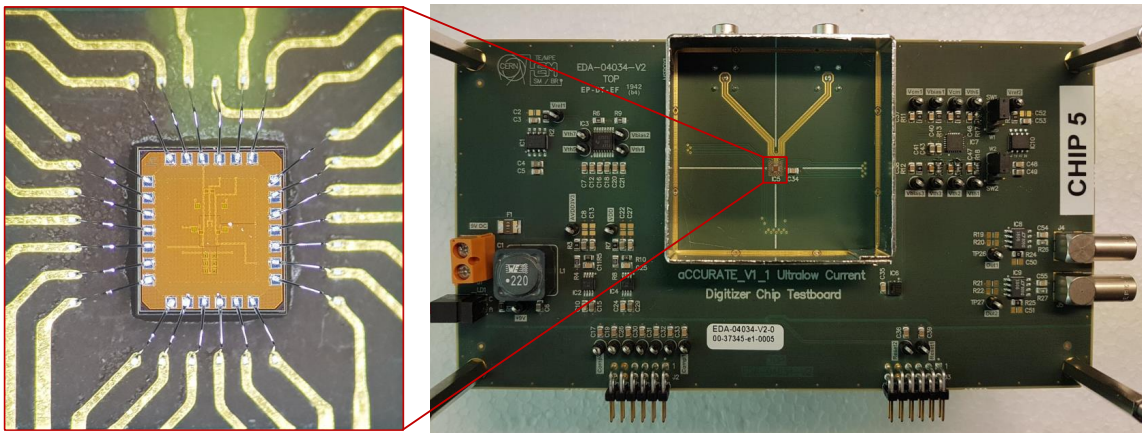


Figure 5.10: ACCURATE 1 ASIC and its test board

The test board shown in the figure generates the voltage for the ASIC and provides an interface to the FPGA board. It was found that the ASIC is ultra-sensitive to measurement conditions in the laboratory like temperature and humidity. It is housed in a metallic housing to protect against electromagnetic perturbations. The chip is also very sensitive to light. Since it is not packaged, the metallic enclosure provides immunity against light too. While characterizing a current in the femtoampere range, the measurements were carried out in a climatic chamber at a temperature of 25 °C.

5.5.1 Chip 1 results

The main objective of Chip 1 was to determine the feasibility of femtoampere measurements using the TSMC 130 nm technology. The output of channel 1 of this chip when the input current is swept from −7.5 fA to 7.5 fA is plotted in Fig. 5.11.

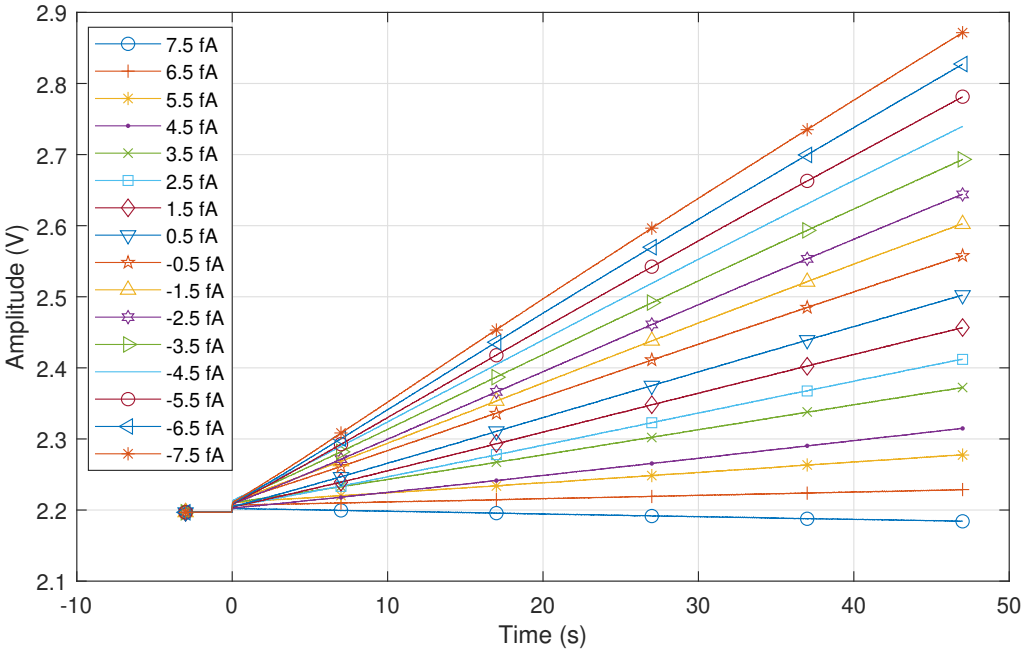


Figure 5.11: Femtoampere sensitivity demonstrated by the output of Chip 1 of ACCURATE 1

It was observed that the chip can generate distinguishable integration slopes when the current is increased in steps of one femtoampere. The integration slope is close to zero for an input current of around 7 fA. This represents the total input bias current. The observed value is the cumulative leakage from the ESD diodes, reset switches, gate leakage of the input transistors, the cables, connectors, and the PCB. Chip 1 also aimed at determining the specific leakage of the ESD diodes. Channel 2 of the chip had similar output, but the leakage observed was around −2 fA. So, the contribution from the ESD diodes in this technology is around −5 fA. The ESD structure used is the classical two diode topology.

The OTA output with two different common-mode voltages is shown in Fig. 5.12. It was observed that, at a common-mode voltage of 1.5 V, the OTA output exhibited a nonlinearity until an output voltage of 2.1 V. Fixing the common-mode voltage to 2.2 V thus helped in extracting the linear portion of the OTA output. It was found that the low noise amplifier's input capacitance, to which the OTA output was connected on the test board, was responsible for the observed behavior. The output stage was modified for the next version of the ASIC. For characterization of all the ACCURATE 1 chips, 2.2 V was used as the common-mode voltage.

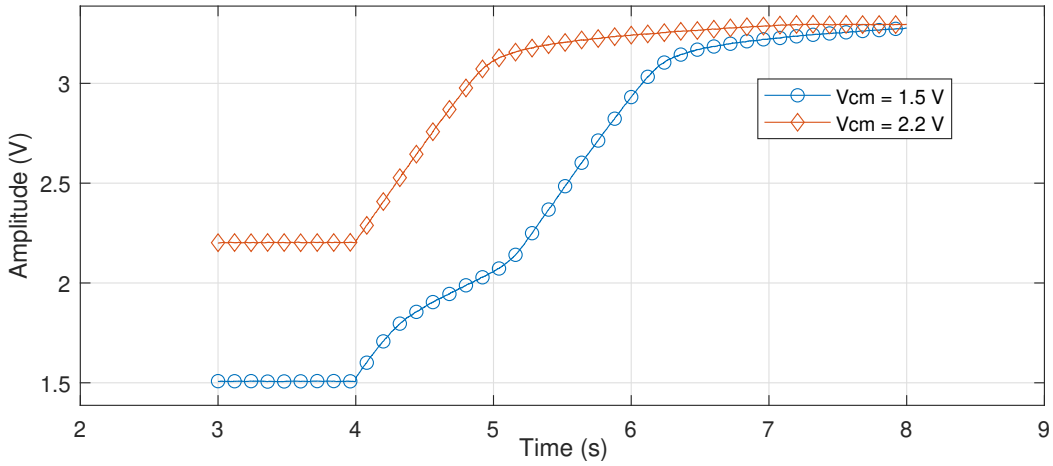


Figure 5.12: OTA output for an input current of −1 pA for two different common-mode voltages

5.5.2 Chip 2 results

The reset counting method and the direct slope method were evaluated using Chip 2. Both methods were found to have a comparable performance for measurements in the femtoampere range. The currents measured using these methods and the percentage errors in measurement

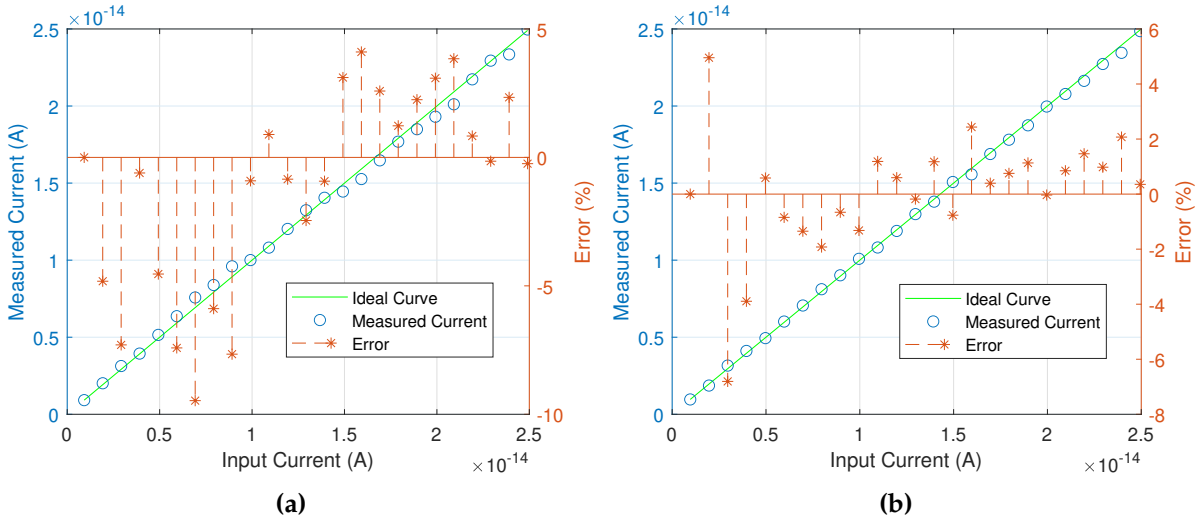


Figure 5.13: Femtoamperes characterization of (a) reset counting method, (b) direct slope method

when the input current was swept from −1 fA to −25 fA are shown in Fig. 5.13. Both the methods exhibit excellent linearity, even in this challenging measurement band. The plots shown are obtained after compensating for the observed leakage current.

The middle current band in the pico-to-nano ampere range was the most accurate since, in this range, the influence of both the leakage current and the non-idealities is negligible. The measured current and the error for an input current from −1 pA to −1 nA are shown in Fig. 5.14.

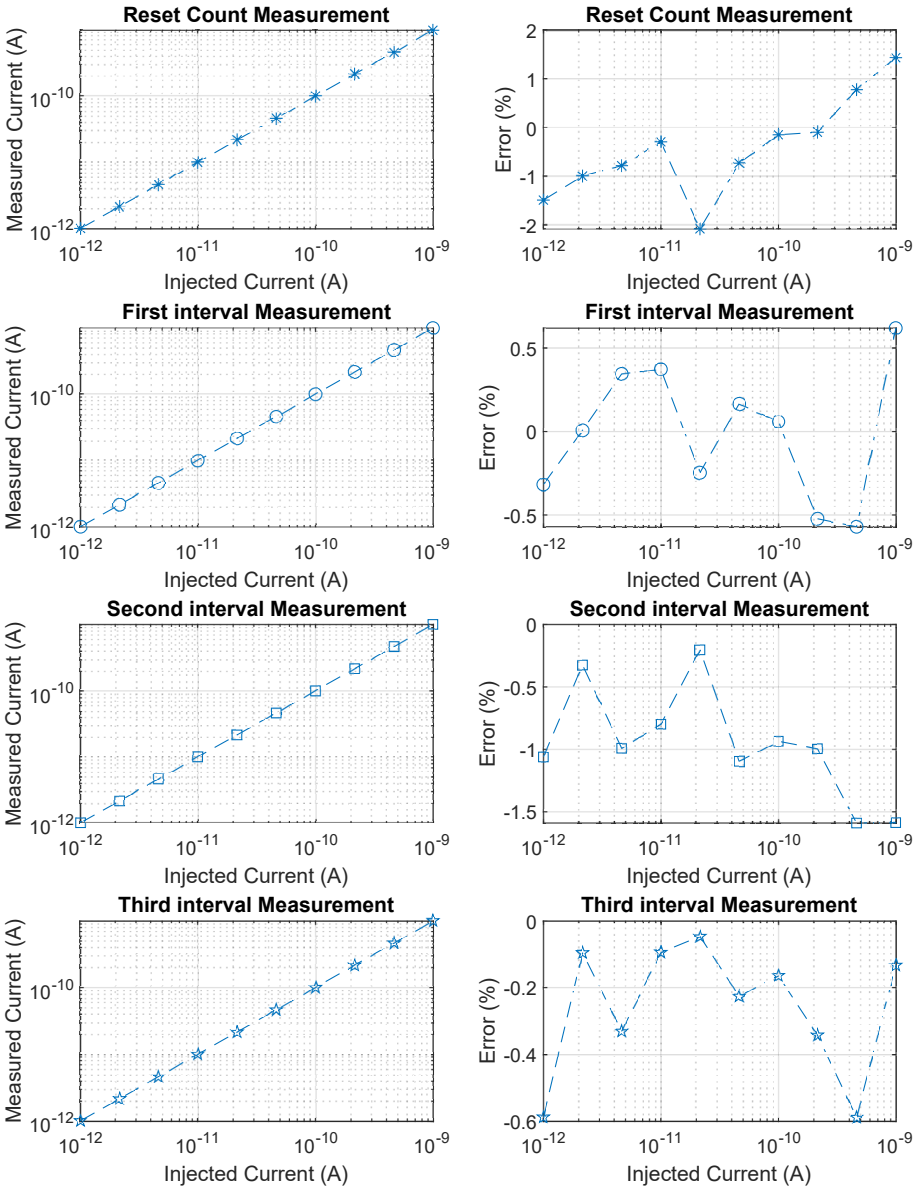


Figure 5.14: Output of Chip 2 with input swept from −1 pA to −1 nA

The first two subplots are the result of the reset counting method. The observed error is within ±2%. The subsequent plots show the result from the different interval counts. As previously mentioned with the three comparator outputs, three interval counts are measured. The measurement from all three counts shows excellent accuracy. The average observed accuracy

was $\pm 1\%$ of the input current. Hence, this method was found to be slightly better in accuracy compared to the reset counting method.

The upper limit of measurement of the direct slope method was found to be around -10 nA and for the reset counting method to be around -50 nA. Beyond these limits, the measurement error was beyond 10 %. These limits were dictated by two main factors – noise from the measurement set-up interfering with the measurement and the strong influence of non-idealities.

Keithley 6430 was used for the generation of accurate currents. It was, however, noticed that a 60 kHz signal was cross-coupled with the measured output while injecting currents from this current source. The influence of this signal was particularly bad for currents around the -10 nA range. In this range, the single measurement time for the input of -10 nA for a voltage difference of 0.3 V was 30 µs. This was close to the period of the interfering signal (16 µs). In the reset counting method, the voltage overshoot for resetting increased because of this interference. For the direct slope method also, the observed interval counts were very different for each of the three measurements and hence resulted in large errors. Thus, the two methods suffered from external noise. As the current range increased, the influence of the noise reduced, however, the overshoot of the comparator output was difficult to estimate with the correction factors and the method lost its linearity. Similarly, the delay associated with the comparator started to become dominant and the variations in this delay with the input current started to become noticeable, resulting in erroneous measurements in the direct slope method. The OTA output with the superimposed 60 kHz signal is shown in Fig. 5.15.

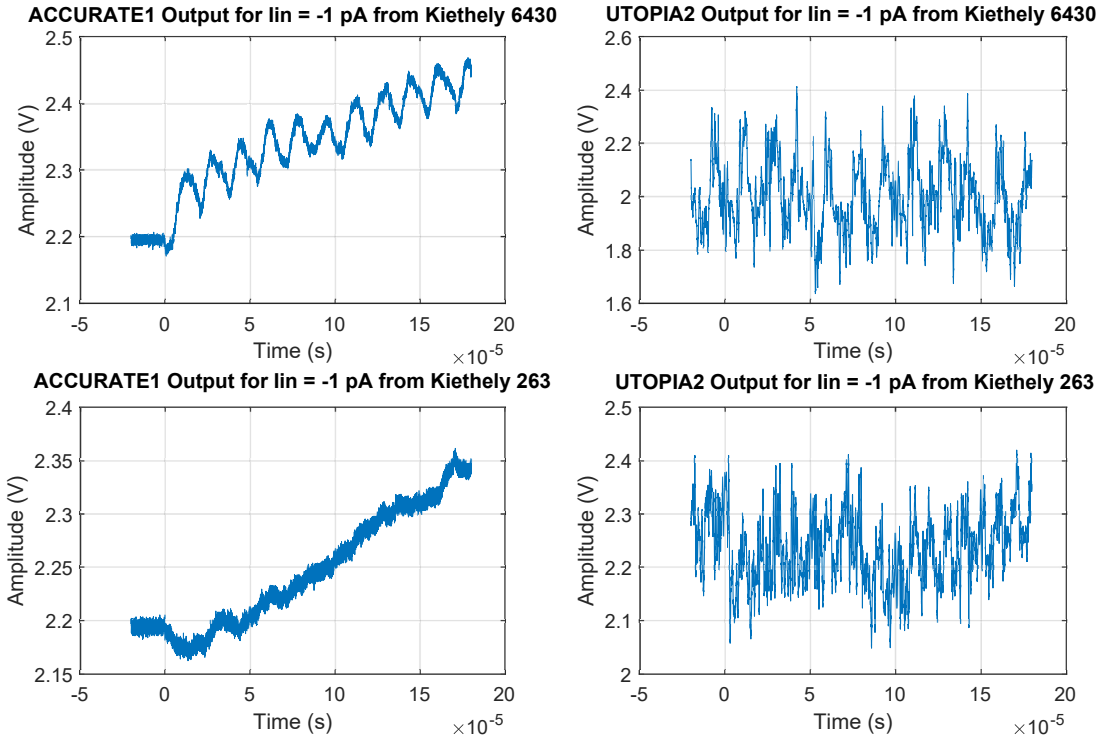


Figure 5.15: OTA output from ACCURATE 1 and UTOPIA2 influenced by external noise

The OTA output from ACCURATE 1 Chip 1 when -1 pA is injected from two different current sources and the same from UTOPIA 2 were measured. It was found that the measurements with the Keithley 6430 demonstrated the noise signal but the one with the Keithley 263 was devoid of it. This external signal was responsible for the erroneous behavior of the current measurement in the direct slope and reset counting method.

5.5.3 Chip 3 results

The aim of Chip 3 was to mainly evaluate the charge balancing method. The linearity and error plot for currents injected from -1 fA to -25 fA and from -1 fA to -1 µA is shown in Fig. 5.16.

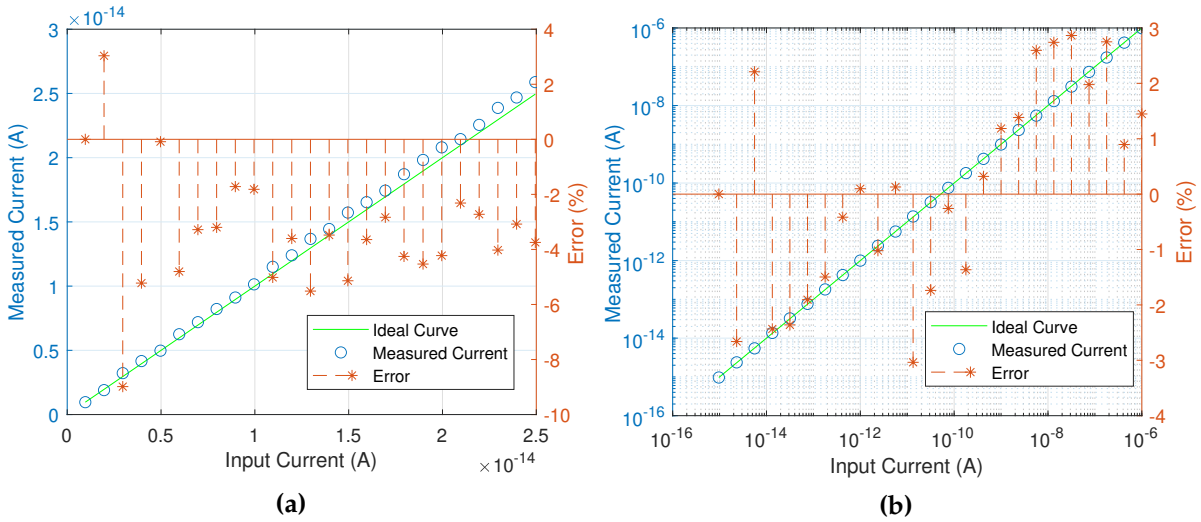
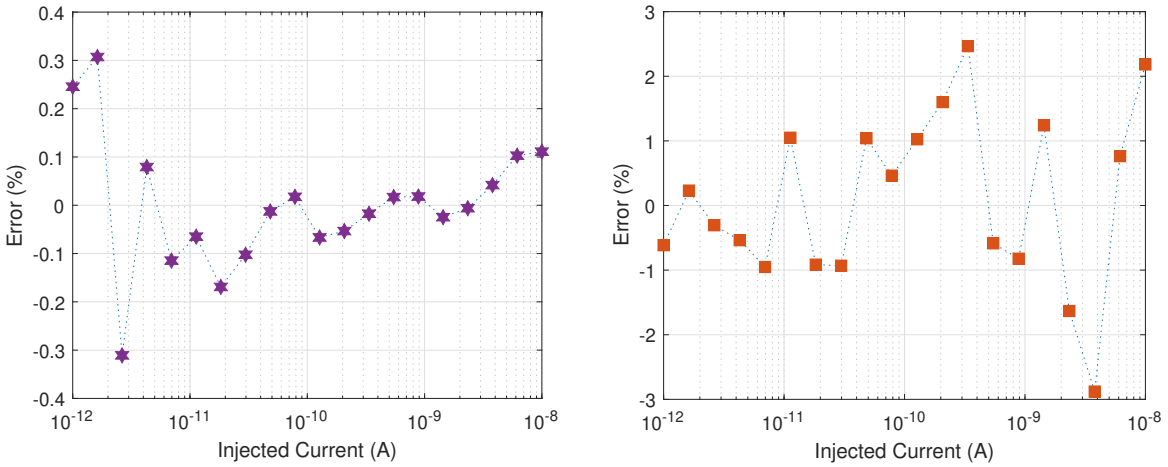


Figure 5.16: Output of ACCURATE 1 Chip 3 for injected currents from (a) -1 fA to -25 fA, (b) -1 fA to -1 uA

The femtoampere range output of the chip is very comparable to the performance exhibited by Chip 2. Hence, it was found that the errors reported by all the three evaluated current measurement methods are very similar. The chip demonstrates excellent linearity in the measurement range from -1 fA to -1 µA. The interference from the 60 kHz signal did not prevent the method from measuring high currents. The method was able to perform in the higher range because it is immune to delays such as the comparator delay. The chip could also measure the output using the direct slope method. The most accurate measurement band of both methods is shown in Fig. 5.17. This was observed for currents from -1 pA to -10 nA. The error reported by the charge balancing method was within $\pm 0.35\%$ and for the direct slope method, it was within $\pm 3\%$. The measurement shows that the charge balancing method is substantially accurate compared to the direct slope method. The measurement above -10 nA was marred by the 60 kHz noise signal.



(a) **(b)**

Figure 5.17: Output of ACCURATE 1 Chip 3 for injected currents from −1 pA to −10 nA with (a) charge balancing method, (b) direct slope method

5.5.4 Chip 4 results

The influence of the input switch while using the reset counting method was assessed by Chip 4. The output of the chip is shown in Fig. 5.18. The first two comparator outputs are shown in the two subplots. The third subplot is the OTA output.

The comparator outputs are normally high when the chip is in reset. When the integrator output reaches 2.3 V, the first comparator output goes low. The threshold for the second comparator is fixed at 2.4 V. The second comparator output is also configured to provide a reset in the measurement scenario shown. An interesting observation was that, while the chip is in reset, the input series switch accumulated some charge which gets released into the feedback capacitor upon release of the reset. The switch thus acts like a charge buffer, storing leakage charges during the reset phase. The very first measurement after the reset phase thus records this accumulated charge. This can impede the accuracy of the average measured current. It was also observed that the amount of charge that gets accumulated is proportional to the reset time of the first reset. During the normal reset time of nanoseconds, the accumulated charge is negligible and was not affecting the measurements. The issue could be compensated by discarding the first measurement sample after the first reset.

5.5.5 Chip 5 results

The comparator of Chip 5 had no hysteresis and the effect of noise was managed only by the debouncing logic in the FPGA. It was found that the digital debouncing did not provide sufficient immunity and the measurements were prone to larger errors. The frequent switching of the comparator was measured as high current and the measurement algorithm was not able to distinguish noise-related measurement from the input current above nanoamperes.

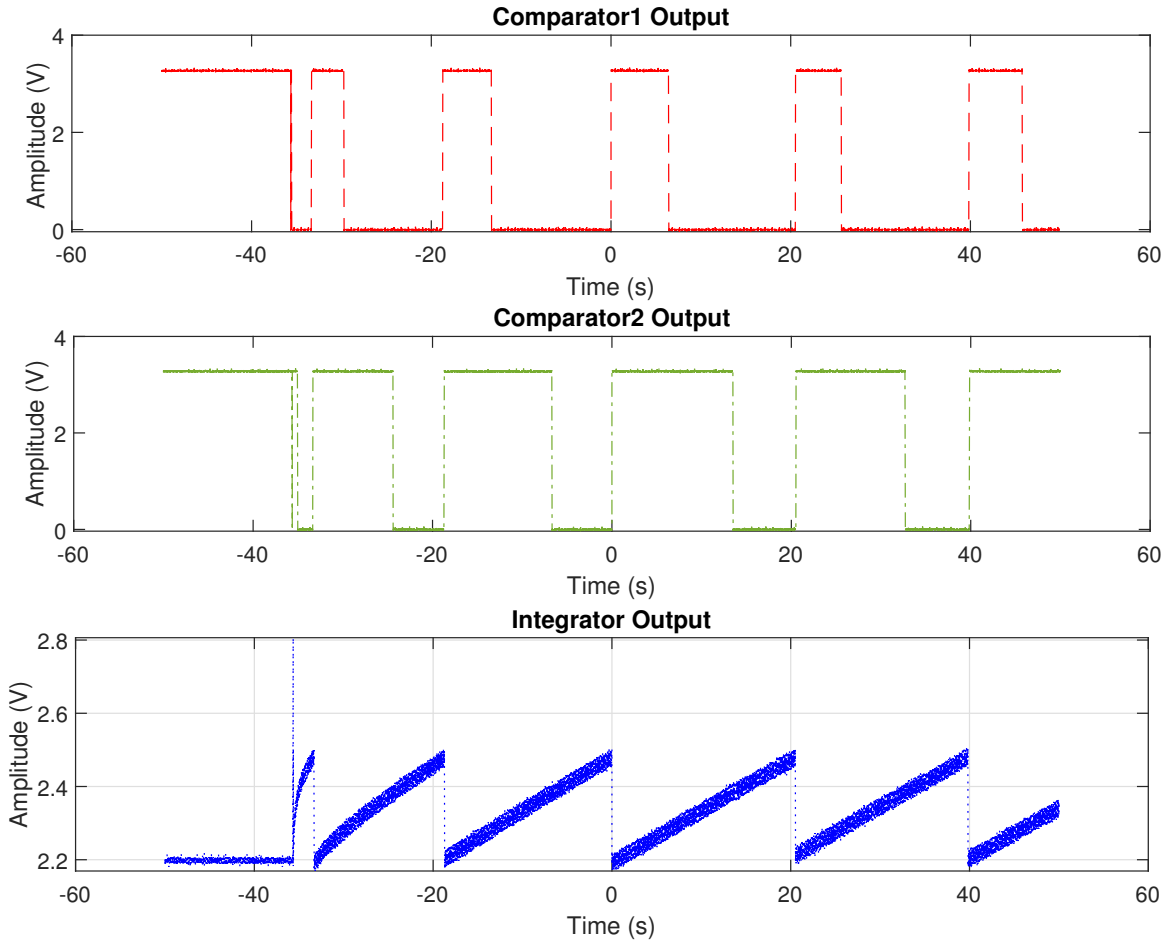


Figure 5.18: ACCURATE 1 Chip4 output showing the effect of input switch on current measurement

Hence, it was concluded that strong hysteresis with digital debouncing was required for stable measurements.

5.6 Leakage current measurements

The leakage currents observed by the different chips using the different methods were measured in different scenarios. A leakage current measurement output is shown in Fig. 5.19.

The result shown is from the characterization of Chip 4 with the input left open. The measurement current obtained at a sampling interval of 100 ms is plotted. The measurement ran for 400 seconds, corresponding to a sample count of 4000. The first 3 subplots are obtained from the measurement using the direct slope method. The fourth subplot is the result of the measurement by reset counting method. The average leakage observed by all four measurements is around -9 fA. In the direct slope method, the discharge of the initial charge stored in the switches is visible. The stored charge, which is estimated or be around -3 fA, is eventually

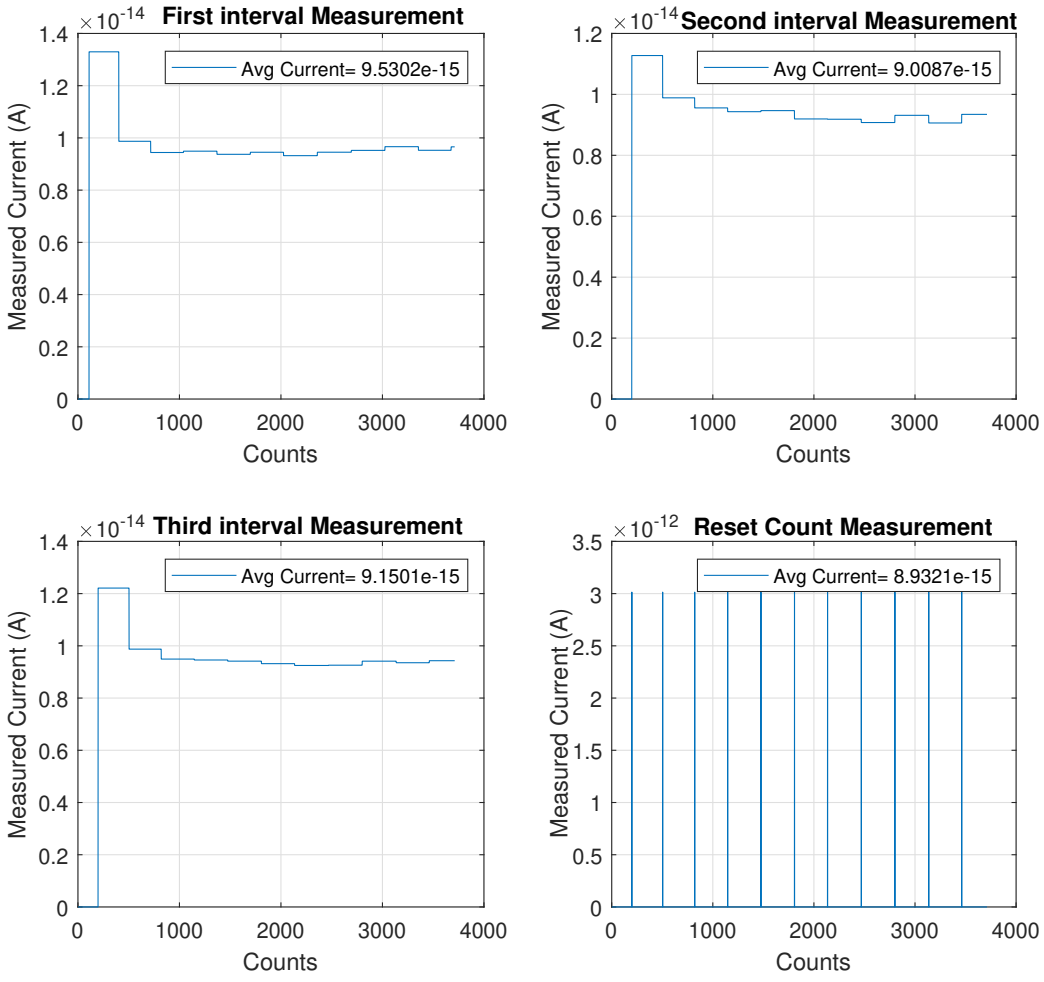


Figure 5.19: Leakage current measurements by Chip 4

discharged and the measurement stabilizes. The reset pulses obtained are almost equidistant after the first pulse, which also shows the settling behavior.

Another kind of leakage current measurement was performed by directly plotting the integrator slope. Input current both of positive and negative magnitude was injected by the current source. The input current for which the slope is zero is then calculated as the total input leakage current of the chip. This method also considers the uncertainty of the generated source and the leakage of the connectors. Graphs like that shown in Fig. 5.19 are extracted for all the chips. The final average leakage currents estimated for all the chips are listed in Table 5.1 below.

The nominal leakage current observed across all the chips is around -7 fA. From channel 2 of Chip 1, it is evident that the major contribution of this leakage comes from the ESD diodes, which is around -5 fA. For Chip 3, which has an additional switch connected to the input for charge injection, and Chip 4, which has the series input switch, an additional -3 fA is observed. The gate leakage of the input transistors is thus estimated to be -1 fA or less.

Table 5.1: Leakage current of different ACCURATE 1 ASICs

Chip	**Channel 1**	**Channel 2**
Chip 1: OTA	−7 fA	−2 fA
Chip 2: OTA + Comparators	−7 fA	−7 fA
Chip 3: Charge Injection	−10 fA	NA
Chip 4: Input Series Switch	−10 fA	−10 fA
Chip 5: OTA + Comparators	−7 fA	−7 fA

5.7 Conclusion

The foundation for building a femtoampere sensitive wide dynamic range current measurement system using TSMC 130 nm technology was firmly laid by the ACCURATE 1 ASICs. The philosophy of using the thick gate transistors of the low technology node, as already demonstrated in the previous chapter, was further cemented using the 130 nm technology.

Detailed analysis of the current measurement methods exposed the difficulties and advantages associated with different methods. It was experimentally proven that all of the three current measurement methods could be used for femtoampere measurements and can expect similar accuracy. Among the methods, the reported maximum error for currents in the femtoampere range was −9.4% and was seen in the reset counting method. For the charge balancing method, the maximum error observed was −7.2%, and for the direct slope method, it was almost the same and stood at 7%. The charge balancing method had a maximum dynamic range from −1 fA to −1 µA with an accuracy better than around $\pm 7\%$.

The measurement in the current range above nano-amperes was erroneous for the direct slope and reset counting method. The main factor responsible for this limitation was the comparator delay, which effectively also appears as a change in the threshold voltage. The change in the threshold voltage directly affects the current calculation in the direct slope method. In the reset counting method, the comparator output overshoots and the estimations of the overshoot with the correction factors were proven to be ineffective after a current of tens of nanoamperes. The amount of charge that is discharged in each reset cycle was not accurate when this overshoot was prominent. For the systems that employ the reset counting method, different correction strategies need to be adopted. For the CROME system [61], the limitation is overcome by using ADCs to determine the level to which the integrator output overshoots before being reset. Also, the voltage level attained after a reset pulse is applied is measured. From these two voltages, the exact amount of charge that is discharged in one cycle could be estimated. This will increase the accuracy considerably. Thus, effectively, the system becomes immune to the comparator threshold and the delays. The method also suffers from the dead time for the reset duration. The dead-time problem could be solved by introducing a series input switch. This switch will, however, introduce additional leakage and the first measurement after a reset had to be discarded to remove the charge injection from the switch.

A strategy to improve the measurement range for the direct slope method is to increase the feedback capacitance, which will eventually increase the granularity in the time measurement. Also, the common-mode voltage, when adjusted to a lower value compared to the current 2.2 V, will give sufficient headroom to make more accurate measurements. It was also found that the comparator output levels did not reach the saturation voltage for current above tens of nanoamperes. This affected the upper and lower threshold crossing calculations. This manifested directly as an error in measurement. By using level restoring buffers at the output of the comparator, the feedback generated by the resistors could be more accurate. Hence, the measurement range and accuracy could be improved.

The charge balancing method provided the most accurate results. The increase of the feedback capacitor, as suggested for the direct slope method, can improve the maximum range for the charge balancing too. The amount of improvement in the maximum measurable current when the feedback capacitor is increased from 1 pF to 5 pF is determined in the next chapter. Increasing the amount of charge injected in each cycle will also help to prevent the saturation of the integrator output and effectively increase the measurement range. This method, however, like the reset counting method, requires a sufficient number of measurement cycles to attain a good accuracy. The measurement time increased geometrically with a decrease in injected current. For ultra-low current measurement, such as in the femtoampere range, the direct slope method can output a fast result with comparable accuracy.

The findings from the characterization of the ACCURATE 1 chips paved the way for the design of the ACCURATE 2 chips. By demonstrating the capability of the technology for low current measurements, avenues for a single system solution encompassing both the analog measurement section and the digital processing section on a single chip are opened. The details of the new design and the performance observed are explained in the next chapter.

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Chapter 6

A Single Chip Solution for the Front-End of Ionization Chambers

ACCURATE 1 demonstrated the capability of the TSMC 130 nm technology for ultra-low current measurements with femtoampere sensitivity. By designing the current handling blocks with thick gate transistors, the influence of the leakage currents was minimized. The potential of using the faster thin gate core transistors to make a complete system was mentioned. The architecture comparison also helped in making an educated choice for the next version of the ASIC. Based on the studies on the five versions of ACCURATE 1 ASICs, the next version in the series – ACCURATE 2 ASICs was designed.

Two versions of ACCURATE 2 were designed – an analog-only version (ACCURATE 2A) and a mixed-signal version (ACCURATE 2M). The mixed-signal version was designed with the analog section implemented with 3.3 V transistors and the digital block with 1.2 V transistors. The complete chain from receiving the currents from the input ionization chambers to converting the current to digital counts to processing the counts and sending the data out through a serial interface to a visualization software is handled by the chip. Thus, it acts as an autonomous entity for any low current measurement systems. The ACCURATE 2 ASICs can measure currents with a wide dynamic range from -6 fA to -20 uA and have a sensitivity of 200 aA. This chapter explains the design details of ACCURATE 2A and ACCURATE 2M. The techniques adopted to attain the dynamic range and sensitivity are also presented.

6.1 System architecture

From the comparison of the three current measurement methods in ACCURATE 1, it was found that all the three methods, the reset counting method (RC), direct slope measurement method (DSM), and charge balancing method (CB), have similar performance while measuring currents in the femtoampere range. The reset counting method was more prone to the effect of non-idealities. The charge balancing method had better immunity to non-idealities among

the three. The direct slope method was able to provide the fastest results. Also, the absence of a feedback path helped in achieving more accurate results. Thus, based on the various observations, an architecture for the new version of the ASIC was designed. The block diagram of the mixed-signal version of the ASIC is shown in Fig. 6.1. The ASIC incorporates the direct slope measurement method and the charge balancing method. Since the reset counting method had more errors in the higher current regime, this method was eliminated.

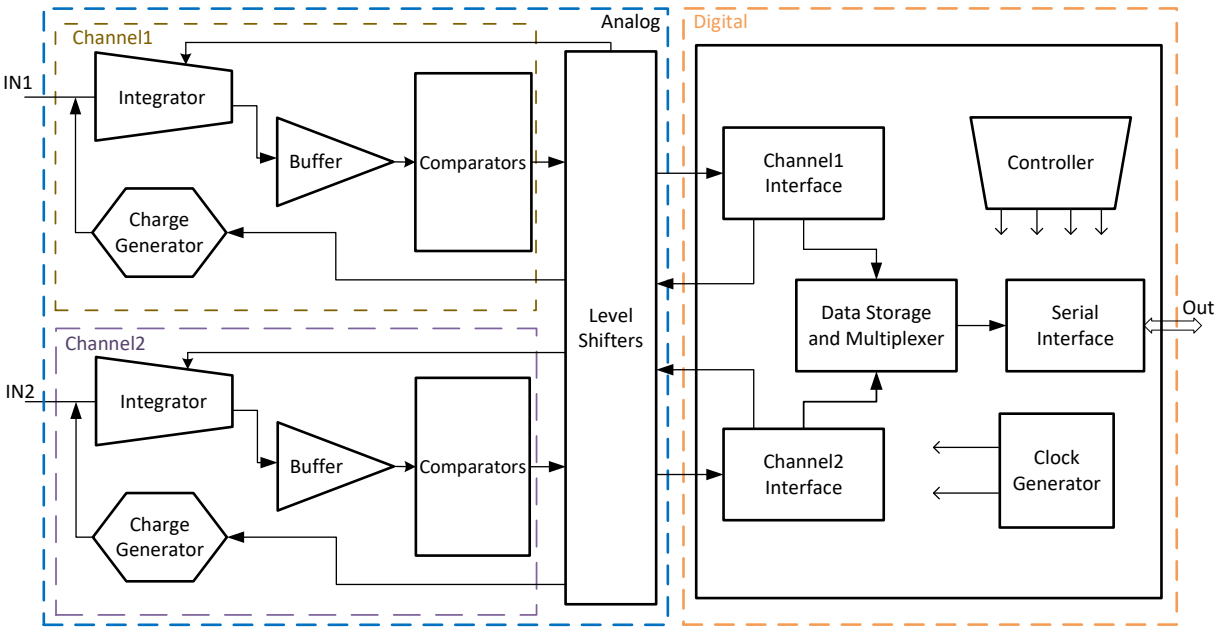


Figure 6.1: ACCURATE 2 system architecture

Both the channels of the ASIC measure current using the same principles. However, the channels are so designed that the primary channel acting as the main measurement channel can measure current until -20 µA while the secondary channel can measure only until -1 µA. The primary intention of the second channel is to measure the leakage currents and thus compensate the measurement of channel 1. The results from both channels are processed in the digital section, where different counts corresponding to the two measurement methods are derived. The calculated counts are stored in internal memory before transmitting through a serial interface. The data flow through the digital blocks is supervised by a controller. The 3.3 V analog domain and 1.2 V digital section are interfaced through level shifters. The various modules in the analog and digital blocks are detailed in further sections.

6.1.1 Analog section

The architecture of ACCURATE 2A is shown in Fig. 6.2. The analog-only version of the ACCURATE 2 chip is an improved version of the ACCURATE 1 Chip3. The OTA integrator has an increased feedback capacitance of 5 pF. This helped in increasing the range of both the DSM and CB methods. Increased Cf directly translates to an increase in the time interval to be precisely measured for the same input current. Hence, the sensitivity of the circuit increased and the current limit where the time to be measured became comparable to the system time period

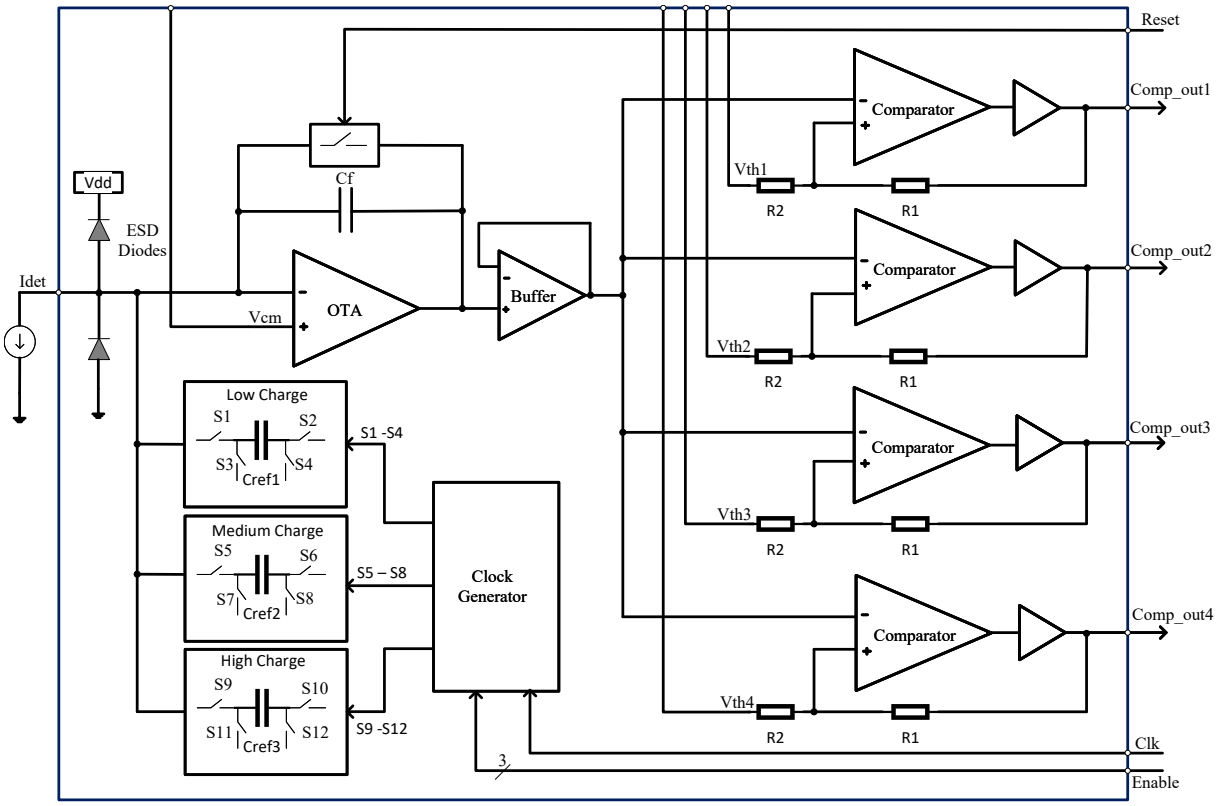


Figure 6.2: ACCURATE 2 system architecture – analog block

increased, facilitating an increased current measurement range with the DSM. In the case of the CB also, a higher Cf allowed for the collection of more charge before the comparator outputs saturated. Thus the upper current measurement range could be increased with CB too.

The comparator receiving the buffered integrator output has a modified structure to improve the accuracy in the DSM method. A level restoring buffer is inserted in the feedback path to have a more deterministic delay for the comparator. In the characterization of the comparators of ACCURATE 1, it was found that the delay of the comparator was dependent on the input current. As the input current dictated the slope of the input to the comparator, the output of the comparator had variable rise and fall times. Although the effect was minimal, it was particularly important in higher currents when the delay started to be of the order of magnitude of the time interval to be measured. The comparator delay was compensated by calibration, but when the delay was not constant, calibration was not effective beyond currents of the order of tens of nanoamperes. The introduction of the buffer helped in achieving deterministic delay. Hence, the calibration was easier and valid for higher current ranges.

The chip has four comparators for the two current measurement methods. The outputs from the first two comparators are used to calculate the current in the DSM method. The first current thus calculated is given by

$$I_{\mathrm{meas1}} = \frac{C_{\mathrm{f}}(V_{\mathrm{th2}} - V_{\mathrm{th1}})R_2}{\Delta t(R_1 + R_2)}, \tag{6.1}$$

where C_{f} is the feedback capacitance, V_{th2} and V_{th1} are the threshold voltages of the two comparators, Δt is the time difference between the two comparator outputs, and R_1 and R_2 are the resistors for hysteresis.

For the CB block, two additional channels are added to cater for higher input currents. The first channel generates a charge of 500 fC, the second one 1 pC, and the third one 4 pC. These charges are defined for a nominal reference voltage of 1 V, which could be changed in the switched capacitor block to tune the amount of charge generated. The second comparator is shared between the DSM and CB methods. The output of this comparator acts as an enabler for the low charge branch of the charge generation block. It also triggers the generation of a pulse of fixed width and period from the digital block. This pulse is used by the clock generation block to generate the control signals S1 to S4. Corresponding to each pulse generated a charge of 500 fC is subtracted from the feedback capacitor. The OTA output reaches a value given by

$$V2 = V1 - \frac{Q_{\mathrm{ref1}}}{C_{\mathrm{f}}}, \tag{6.2}$$

where $V1$ is the initial voltage at the start of integration at the OTA output and Q_{ref1} is the charge generated by the first change generation branch.

For currents above around -2 µA, the OTA output shoots above the third comparator threshold, triggering its output. This results in the generation of the enable of the medium charge branch. For even higher currents, similarly the fourth comparator's output is asserted and the high charge branch is enabled. The total charge injected is the sum of all the charges generated by the enabled branches.

Another factor that had to be carefully designed to achieve a wide dynamic range was the sizing of the transistor used in the reset switch. The switch is used only in the initialization phase to remove the residual charges from the feedback capacitor. The output voltage is also fixed in this phase. The structure used for the switch is shown in Fig. 6.3

The terminals T1 and T2 are connected to the input and the output nodes of the integrator. In the initialization phase, M1 and M2 are switched on, thus creating a path between the input and output nodes through a resistance 2Ron, the on resistances of the transistors. M3 remains off in this phase. Since the entire input current is flowing through the transistors M1 and M2, they should be dimensioned for this drain current. In the integration phase, M1 and M2 are turned off and M3 is switched on. The common

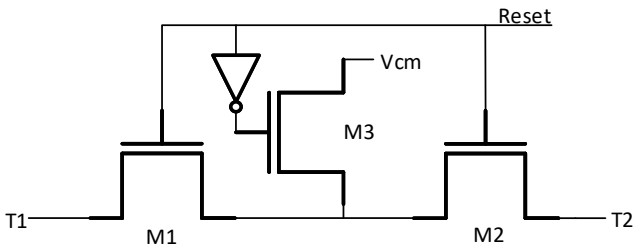


Figure 6.3: Reset switch configuration

node of M1 and M2 is tied to the common voltage Vcm through M3. The nominal bias voltage at the input and output of the integrator is Vcm. Thus, the drain-to-source voltages of M1 and M2 are very close to zero, thus reducing the leakage current generated by the transistors. In this phase, the dimensions of the transistors are important to generate as low a leakage as possible. Thus there is a trade-off with leakage current and maximum current that the transistors allow. They are dimensioned to be W/L = 4 µm/350 nm.

The comparator outputs are fed to the digital section to generate the counts for various current measurements. The signals have to be level shifted from the 3.3 V domain to 1.2 V before feeding to the digital logic. Buffers realized with 3.3 V transistors and supplied with a 1.2 V supply voltage achieve this conversion. The digital section also generates various enable signals and the clock signal for generating the control signals of the charge generation block. These 1.2 V signals are level shifted to 3.3 V by dedicated converters.

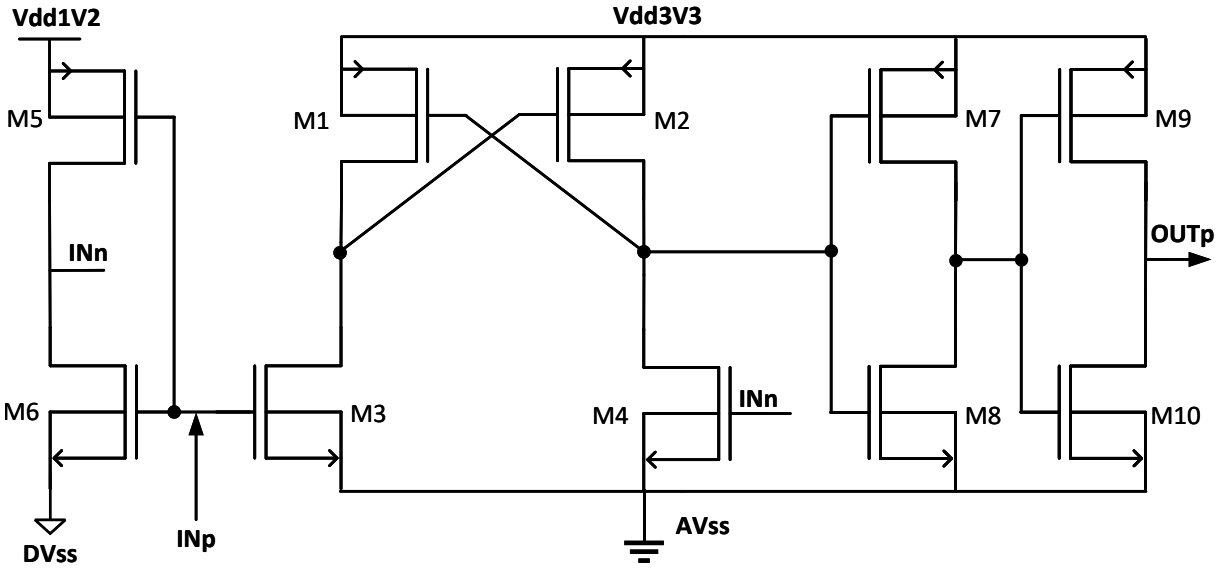


Figure 6.4: 1.2 V to 3.3 V level shifter

The circuit for the level shifter based on classical cross-coupled topology is shown in Fig. 6.4. The signal and its inverted versions are applied to transistors M3 and M4. When the input is high, transistors M3 and M2 turn on, making the output high. Transistors M1 and M4 turn on when the input is low, further propagating the level to the output through the output buffer. The signals from the 1.2 V are up-converted to the 3.3 V domain through these level shifters. DVss is the digital ground corresponding to the 1.2 V core transistors and AVss is the analog ground of the thick gate 3.3 V transistors. These grounds are connected externally on the test board. Although numerous improved architectures were available in the literature with improved performances, the level shifter in the discussion was found to be meeting the requirements and was simulated to have a fast translation with a delay of 500 ps.

The described architecture constitutes also the primary channel of the analog section of the ACCURATE 2M. There is only one channel in analog only chip while a similar secondary channel exists for the mixed signal chip. The second channel consists of only two comparators and only

one branch for the charge injection block. Since the currents to be measured are only less than the picoampere range, the higher charge branches were not required. The feedback capacitor for this channel is 1 pF to facilitate fast measurement of low currents. The lower integration time will result in a faster generation of interval counts for measuring the leakage. The charge generation block generates a nominal charge of 100 fC. In the case of ACCURATE 2A, the digital section is realized in an FPGA. While for the ACCURATE 2M, the digital logic is embedded within the chip.

6.1.2 Digital section

The main objective of the digital section is to measure the two main parameters for current calculation – the time interval between two comparator outputs and the number of charge injections. This measured data are arranged into packets and sent out through a UART interface. The block diagram of the digital section is shown in Fig. 6.5.

The default clock of the digital section is 100 MHz generated by an external oscillator. All the outputs from the analog section are synchronized to the local clock domain in the synchronizers, which are the entry point to the digital section. The asynchronous comparator outputs are thus fed through two flip-flops to eliminate metastability and to align with the clock edge. The outputs of the first two comparators are then fed to pulse generators which generate a single pulse when the comparator triggers an output. These two pulses are fed to an interval counter which eliminates any debounces in the comparator outputs and measures the time interval between two pulses which makes the interval count 1. The various logic implemented in the interval counter are listed below and the timing diagram with different scenarios are shown in Fig. 6.6.

1. The counter starts counting when there is a start pulse. Any subsequent start pulse before an end pulse is ignored. Thus all the debounces in the start pulse are ignored.
2. The value of the counter is latched when there is an end pulse succeeding a start pulse. The counter, however, does not reset but continues to count.
3. If there are more end pulses, the output is latched with the new value of the counter. Thus, the settling time of the end pulse is taken into account. The counter is not reset with any number of end pulses.
4. The output counter is reset with the first start pulse after a reset. The counting restarts whenever there is a start pulse that comes after an end pulse. The output counter is, however, not reset in this case but holds the value of the previous count i.e. the value updated with the previous end pulse. Thus output register always holds a value and the interval counter can hence work independently of the system operating cycle.
5. When start and end pulses arrive in the same clock cycle the count output is made 1. The counting then restarts. This is a typical scenario that can occur when there is a high input current and both the comparator outputs are generated within the time of 10 ns, the

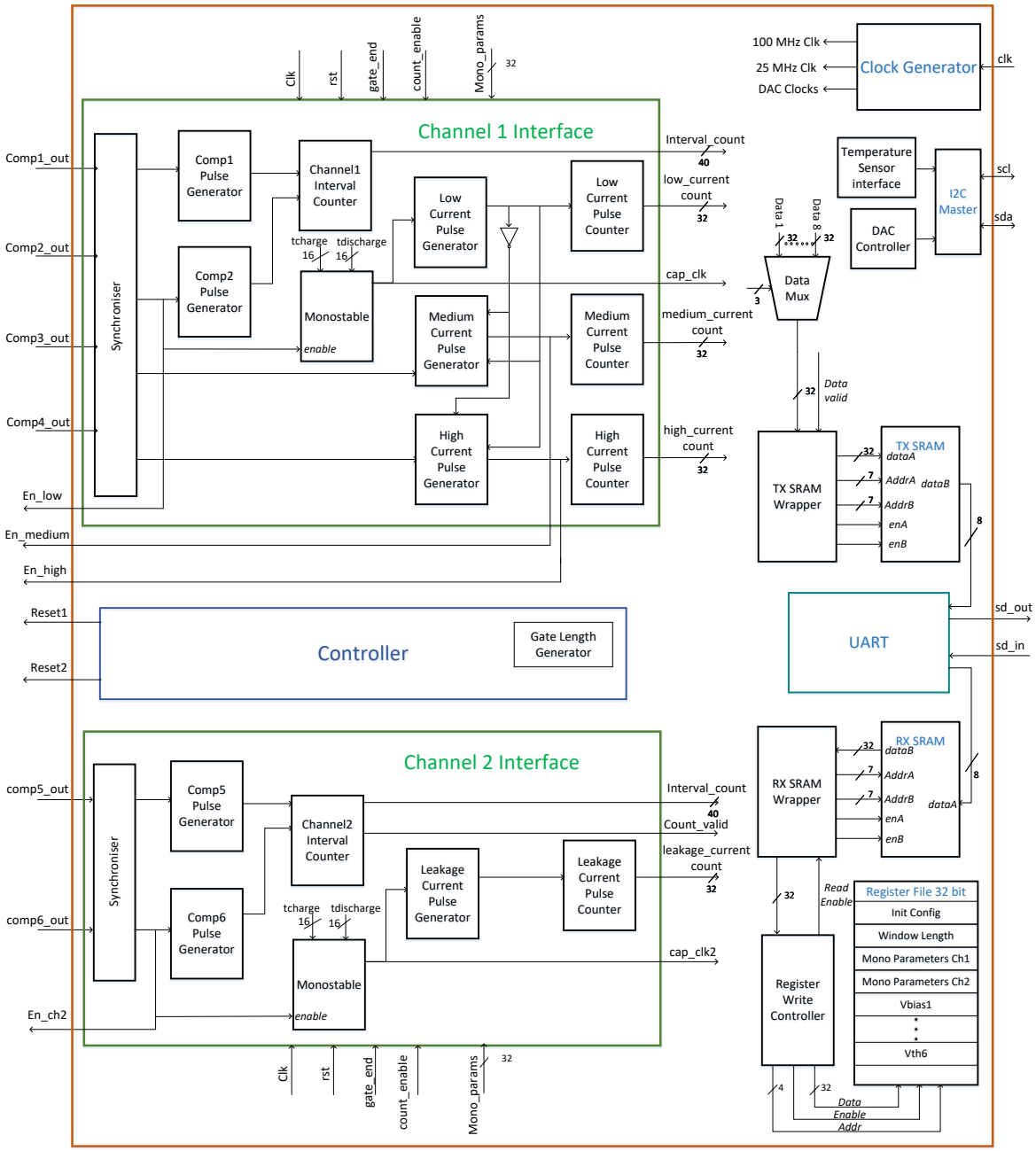


Figure 6.5: Digital section of ACCURATE 2M

system clock period. Thus this condition corresponds to the maximum current that can be measured by the DSM method.

6. In case the counter overflows, the counter holds the maximum value until there is a reset. When there is a new start pulse, which comes after an end pulse, the output counter remains at the maximum value until it gets updated at the next end pulse but the counting restarts in this scenario. This corresponds to the minimum current that can be measured

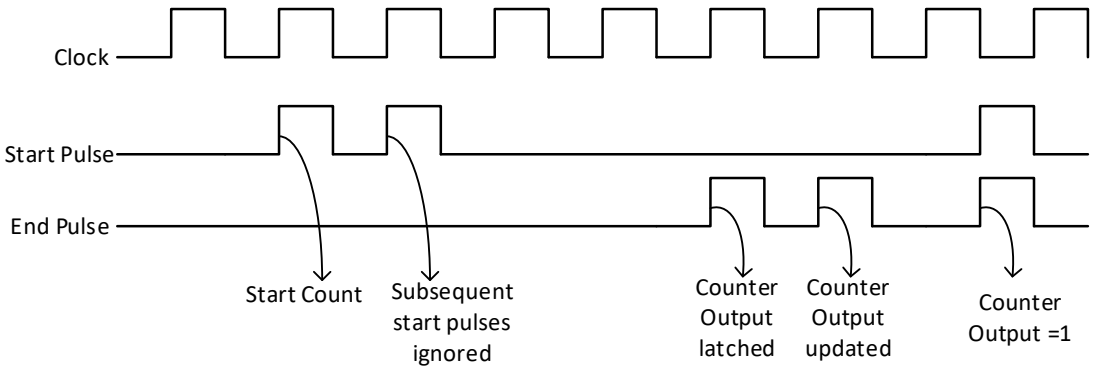


Figure 6.6: Behaviour of interval counter module

by the interval counter. For a comparator threshold difference of 0.1 V, the 40-bit interval counter can count up to a minimum current of around 45 aA.

The synchronized second comparator's output is sent to the analog section to generate the clocks for the low charge generation block. The output of the second comparator also triggers the generation of a pulse from the monostable module. The module receives on-time and off-time of the pulse as 16-bit values. Thus digital monostable allows easy tuning of the pulse widths from 10 ns to around 650 µs. As long as the comparator output remains high, the monostable generates an output. However, if the comparator output falls before the completion of a pulse, the output pulse is not terminated immediately but only after the current pulse time. New pulse parameters are only applied at the start of the pulse time.

The monostable pulses are converted to one clock cycle wide by the low current pulse generator module. These pulses are then fed to the low current pulse counter. The pulse counter module counts the number of input pulses in a specified time interval. The window length is communicated to the pulse counter in the form of pulses that appear every fixed duration. The module also receives an enable signal which should be high for the counter to start. The various functionalities of the pulse counter are:

1. Whenever there is an input pulse, the counter is increased but the output is loaded with a count only when there is a window indicator signal.

2. When the input pulse and the window indicator rise in the same clock cycle, the counting restarts with a value of 1 and the output counter is loaded with the count counted until that clock cycle.

3. In an input clock cycle when there is no input pulse or window indicator, the counters are unaltered.

4. In an input clock cycle when there is no input pulse but there is a window indicator, then the output is loaded with the current value of the counter and the counter is reset to 0, starting a new count cycle.

5. The counter output always holds a value. That is, once a valid count is reached, this value is held until it is updated by the next valid count. The absolute reset of the count value happens only when reset is asserted or enable is de-asserted.

6. When an overflow occurs, the output stays at the maximum value i.e. all bits 1 until there is a reset or disabling of enable signal. When the reset is asserted or enable is de-asserted, the output count is reset to 0. When there is a new window indicator, only the counter restarts (with either count value of 1 or 0 depending on whether an input pulse is present or not in the same clock cycle), the output count is loaded with the maximum value of the counter.

Thus, corresponding to the monostable output a low_current_count is generated. When the charge injection by the low charge branch is not sufficient to reset the charge stored in the feedback capacitor, the net voltage at the OTA output continues to increase until the third threshold is crossed. The output of the third comparator is asserted in this case. The digital section receives the comparator output in a similar path to the first two comparators – through a synchronizer and pulse generator to a medium current pulse counter. The medium current pulse generator acts as a gate that passes out the monostable output through it whenever there is an output from the third comparator. Thus, there is no separate monostable for the medium current path but it uses the one from the low current path. This is because the monostable output is always active when the second comparator output is high. Since the thresholds of the comparator are progressively higher whenever there is an output of the third comparator, the output of the second comparator should have already been high and the monostable should be already active. The medium current pulse counter generates the medium_current_count value. Similarly, when the fourth comparator is asserted, a high_current_count is generated. The medium and high current pulse generator also produces the enable signals for the corresponding charge generation blocks in the analog part.

The described module constitutes the channel 1 interface. Similarly, the channel 2 interface receives the outputs of the fifth and sixth comparators and generates the interval count as the time between these outputs and a pulse count corresponding to the sixth comparator output. A monostable module with independent parameters also exists.

The comparator thresholds are determined by two external DACs on the test board. These voltages are set through an on-chip I2C module. Upon receiving an enable signal for programming the DACs, eight values corresponding to different voltages are set in the register of each of the DACs. These values come from a register file. The I2C module also handles the reading of the temperature and humidity data from an onboard temperate sensor. The same I2C ports are used for both purposes and are hence done sequentially. The clocks for the I2C

module, state machines of the controller module for programming the DACs and other clocks are derived by a clock generation module from the external clock.

The whole operation of the digital module is orchestrated by a controller by generating various enable signals. The time window generator is also embedded within the controller. The system operating frequency is dependent on this time window. The state machine of the controller is shown in Fig. 6.7

In the reset phase, the controller remains in the idle state. In the normal operational mode, the state machine is enabled by default. Depending on the configuration register, the controller issues signals for programming the DACs and reading the temperature and humidity sensor. The corresponding modules for DACs and sensor issues hand shake signals to indicate completion of operation for the state machine to advance further. The sensor delay required for measurement of the parameters is included as a state in the controller for the first measurement cycle. Subsequent measurement time is contained within the time period of the operation of the system and does not require a specific extra delay.

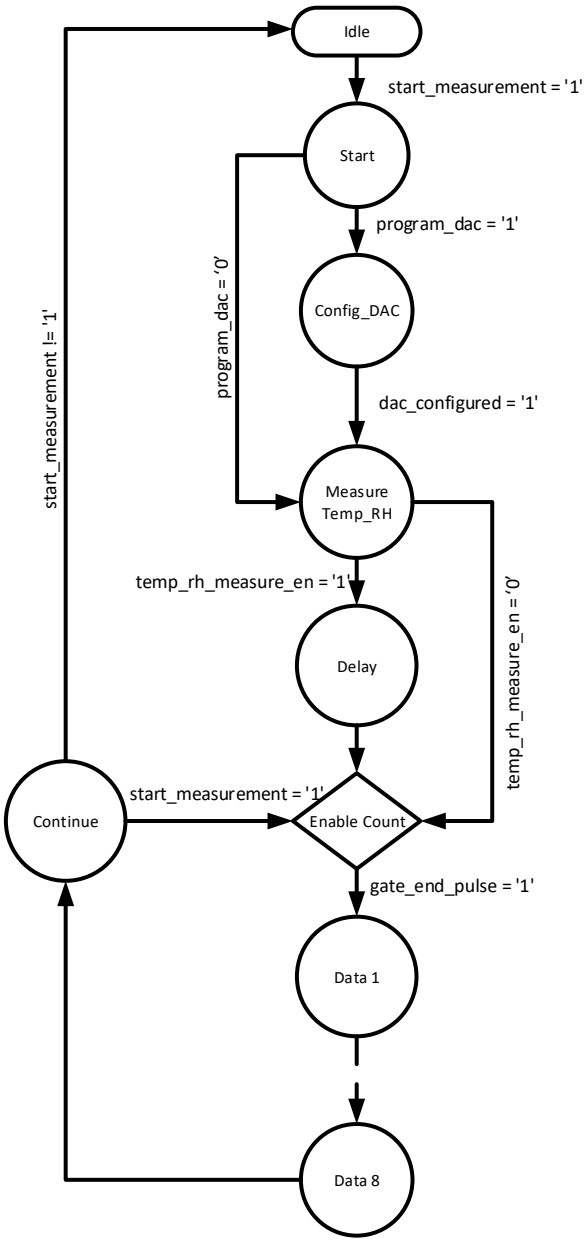


Figure 6.7: Controller state machine

After these operations, in the enable count state, the timing window generator counter is enabled. A window indicator pulse is generated each time the counter reaches the programmed time window. At this moment various pulse counters and interval counter registers are updated. A select signal corresponding to each of the words to be transmitted is asserted in each of the data states of the controller. The select signal for the multiplexer also acts as the data indices for storing the words in the memory. After sending the eight data words, depending on the enable signals, the whole operation is repeated. In the normal operation, the controller circles through the data transmit states continuously updating the data register at a fixed time

interval. When the DACs must be reprogrammed, the control signal has to be changed through the configuration register to restart the controller from the idle state.

All the generated counts are multiplexed and written to a transmit SRAM. Both the memories are 32 bits wide and 128 words deep. A wrapper module supervises the writing of the data to the SRAM and sends it out to the UART module. It thus acts as a tight interface between the controller module and the UART interface. Data to be transmitted are generated as packets of eight 32 bit wide words. The write enable signal for the SRAM is asserted at the start of the write cycle and is held high for eight clock cycles. The index generated by the controller is used by the SRAM interface module as the least significant bits (LSB) for the final address generation for the SRAM. The writing to the SRAM thus happens sequentially without interruption in batches of eight words. The most significant four bits are increment each time a block of data is written. The interface module also flips an empty signal as soon as the first block of data is written. The logic for empty generation also keeps track of data reads and maintains the empty signal high if at least a single data word is available in the memory.

The empty signal acts as an enabler for the UART module which starts the transmit state machine when this signal falls. The module then generates a read enable signal to the SRAM wrapper. The UART module sends out data as packets of eight bits and hence needs the input data in this format. The transmit SRAM wrapper generates a read enable signal once for every four read enables received from the UART interface module. The read address is also increased by one in this situation. The readout 32-bit data is split into four packets and sent to the UART interface. The transmit UART module then serially sends out this eight-bit data word at a predefined baud rate.

At the receive side of the UART, the serially received data in packets of eight bits are converted to 32-bit words by the receive SRAM wrapper and stored in the Rx memory. The interface module controls the data flow between the UART and the register write control module, which controls the writing to the register file. The 32 bit first data written to the Rx SRAM is treated as the address of the register in the register file. The register write control module writes the next received data to the register at the address specified in the first received data. There are 20 registers with varied functionalities. The first register holds various control signals which determine if the DACs should be programmed, if the temperature sensor should be read and the signals for calibration. The reset signals for the analog channels and enable signal for starting the controller state machine are contained in this register. The length of the time window is configured through another register. The pulse widths of two monostable modules of the two channels are defined in two different registers. All the other registers hold the value of voltages for programming various DAC channels.

6.2 Reset generation scheme

The digital section is a predominantly synchronous design with all the flip-flops with asynchronous reset input. Both the synchronous and asynchronous reset schemes come with specific pros and cons. The details of different kinds of resets are summarized in [74]. The best choice is to use a mix of both kinds of resets. Hence, the implemented reset logic is to assert the reset asynchronously and to remove the reset synchronously. Making the reset assertion asynchronous helps in achieving immediate reset of all flip-flops without any delay. The problem with the asynchronous reset is the risk of leaving different flip-flops in different states when the reset is de-asserted. Also, the timing with the data can result in certain flip-flops having a metastable state if the reset and data change occur too close together. By making the reset removal synchronous, this situation is avoided. The logic for the generation of the reset signals is shown in Fig. 6.8.

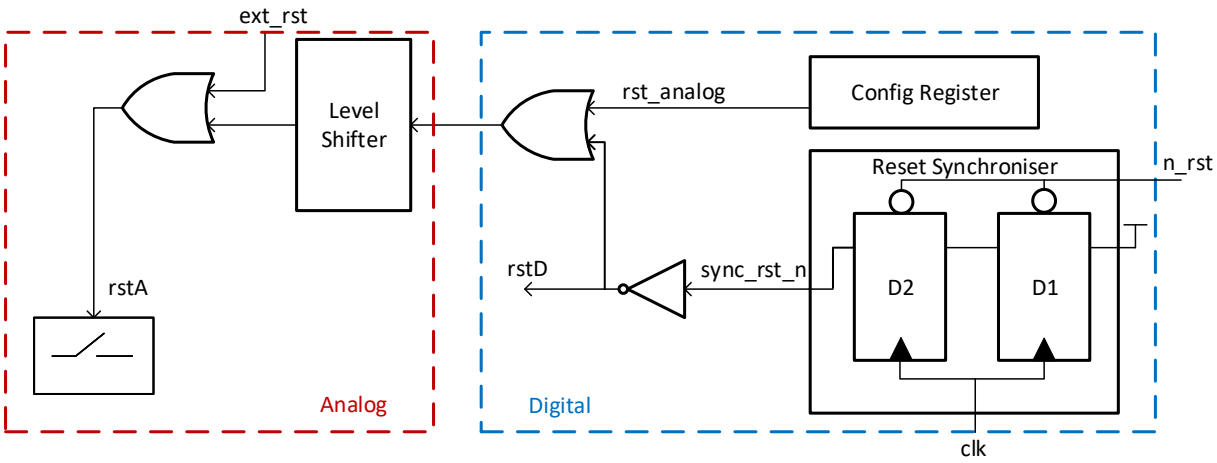


Figure 6.8: Reset generation logic

The system reset for the digital section rstD is derived from the external reset n_rst which is fed to the reset synchronizer. When n_rst is de-asserted, the reset removal happens in two clock cycles. For the analog side a reset bit is allocated in the configuration register for either of the channels. The analog reset bit is ORed with the digital system reset and passed on to the analog section. There is a separate dedicated reset pin for the analog section. This reset is combined with the reset from the digital section to derive the final analog reset rstA.

6.3 Design flow

The system design started with the architecture evaluation using VHDL AMS blocks. The measurement capabilities and proof of concept were established using the ideal components designed in VHDL AMS. Mixed-signal simulation of the equivalent analog block in VHDL AMS with the digital blocks in VHDL was the basis for tuning the data flow in the digital section. Cadence ASM simulator with generic connect modules was used in the simulation. The

results from the technology evaluation ASIC explained in [71] provided the base for the current measurement topology selection.

The most time consuming and challenging section in the design step was the simulation and verification of the digital sections. For the verification of the digital section, the various practices adopted were

1. RTL simulation of the digital block at various levels of hierarchy.
2. Mixed-signal simulation with the analog blocks initially with the models and later with the actual circuits.
3. Formal verification of various sub-blocks and major data paths in the top level.
4. Use of the Questa Autocheck tool to detect uninitialized signals and verifying the state machines.
5. Gate level simulation of the synthesized netlist.
6. Gate level timing simulation after place and route.
7. Conformal equivalence checking after synthesis and routing.
8. Testing of most of the blocks on an FPGA board.

The formal verification methodology was found to be particularly useful in finding bugs and evaluating all the corner cases missed out in simulation. The independent verification was carried out by a verification specialist. In the process, a verification document was created based on the design specification document. This document is structured into assumptions, cover properties, and assertions. The behavior of the module is described through different properties. A cover property is coverable if the formal tool is able to find an input stimuli sequence that satisfies the property. They can be used to sanity check the verification code or for design exploration. Assumptions are properties that constrain the signal value combination for which the formal assertions are valid. Thus, assertions are proven for all scenarios that have not been removed by input assumptions. Assertions are proven by the model checker if they are true at any clock cycle and for any input signal value combination which is not removed by an assumption.

Formal verification was performed using Questa PropCheck by Siemens. The formal tool tries to find counter examples that demonstrate a case where the property is not satisfied. The example scenario thus found by the formal tool was then used to recreate the situation in simulation to confirm that the bug found is in fact a design bug and not arising from the verification code. The verification process was thus a continuous interaction with the verification engineer. The number of mismatches found in different modules which lead to an update in the design specification, design, verification document, and the verification code are listed in Table 6.1. The interval counter was the first module that was considered for verification. The format to describe the specification and the various scenarios with counter-like overflow conditions were established

with this module. Hence, maximum faults were found. The methods established with the verification of this module were adopted in further modules to make the process systematic.

Table 6.1: Functional verification results summary

Block	Specification	Design	Verification requirement	Verification code	Total mismatch
Interval Counter	6	8	8	5	16
Pulse Counter	-	1	-	-	1
Pulse Generator	1	-	2	2	2
Synchronizer	1	-	-	1	1
Monostable	1	2	1	1	3
Channel2 Interface	1	1	2	2	2
TxSRAM Wrapper	1	1	3	3	3
Top Module	-	2	-	-	2
Total	**11**	**15**	**16**	**14**	**30**

All the other blocks were only simulated and further tested with an FPGA. Testing of the common cases for the input and output paths was, however, also done with the formal tool.

The RTL code was synthesized using the Genus tool targeting the TSMC 130 nm library. The logic was mapped using 4052 logic cells. The synthesized netlist was placed and routed using the Innovus tool. The power grid was tuned to optimize the IR drop reported by the power analysis tool, Voltus. The power distribution estimated using Voltus is shown in Fig. 6.9.

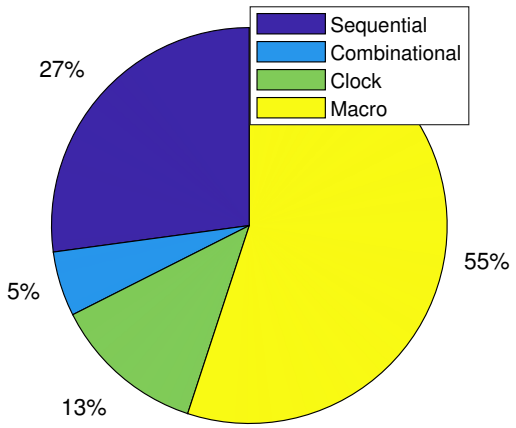


Figure 6.9: Power distribution in the digital section of ACCURATE 2M with estimated total power consumption of 34 mW

It could be seen that the majority of the power consumption is attributed to the SRAM macros. The total static power consumption for the design was estimated to be around 34 mW. The

contribution from each SRAM is around 9 mW. The width of the power lines was adjusted to support the required current, as reported by the tool.

Layer hoping was implemented on signal routes from different ports to overcome antenna rule violations. After running the design rule checks (drc) and layout versus schematic (lvs) checks, the parasitic associated with the whole chip was extracted. A complete simulation of the parasitic extracted design was performed in Virtuoso and the analog outputs were observed. The simulation for 10 µs took 24 hours to complete. Digital outputs would appear only after 100 ms and was hence not feasible to observe. The design thus verified was signed off for fabrication.

6.4 Mixed signal layout

The aim for this series of ACCURATE ASICs is to achieve femtoampere sensitivity or better. ACCURATE 1 had determined the expected leakage currents in the analog section of the chosen architecture. All sources of leakage in the front end were studied and optimized. As the design scales to include the digital section also in the same chip, additional challenges arise. The main source of noise in the mixed signal system is the coupling from the substrate [75]–[79]. The substrate noise can affect the sensitive analog nodes and hinder their operation. In the current design, any noise that would couple to the OTA input or output nodes would affect the accuracy of the system. Standard design practices do exist to mitigate this issue [80]. The details of the techniques adopted to minimize the noise from the digital section are detailed further.

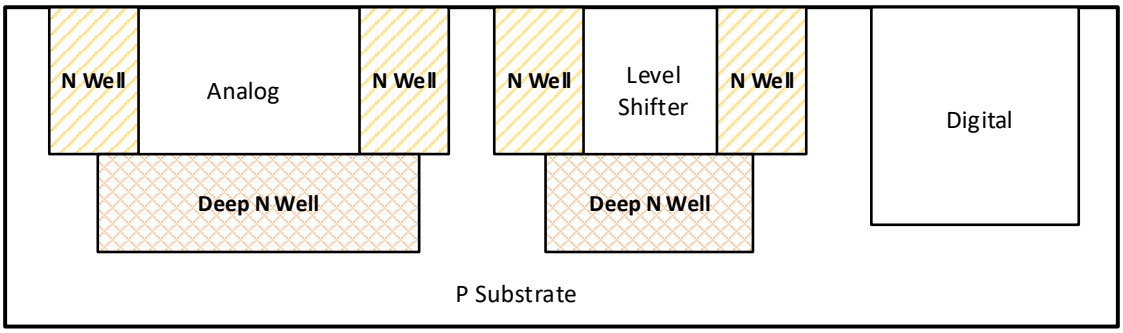


Figure 6.10: Design separation using Deep N-Well

The classic solution for protecting the analog section is by using a Deep N-Well structure [81]–[83]. The use of Deep N-Well in the current design is illustrated in Fig. 6.10. The entire analog section is surrounded by an N-Well which sits on a Deep N-Well. This separates the P substrate of the NMOS transistors from the common substrate in the chip which is shared with the digital section. The PMOS transistors that were already in their separate N-Wells, are now connected through the Deep N-Well. For the PMOS transistors requiring a separate potential for the N-Well, a cut has to be made in the Deep N-Well structure. The level shifters were also

placed on an island of separate N-Well. Additionally, each section was surrounded by a guard ring which was tied to the corresponding supply voltage. Further, each of the sensitive PMOS and NMOS blocks were surrounded with their own guard rings tied either to supply or ground respectively. The input stage of the OTA realized using PMOS transistors were also separated using dedicated guard rings.

Floor planning and pin planning are also crucial in the design of the mixed signal ASIC. The representation of the final layout with details of the pin structure is shown in Fig. 6.11. The chip occupies an area of 1920 µm $\times$ 1832 µm. The digital section occupies the majority of the active area. The SRAMs consume most of it. The power and ground ring around the chip is cut into two sections using power cut cells. The left side of the cut cells is dedicated to the 3.3 V analog domain while the right side is for 1.2 V digital pins. Two pairs of supply and ground pins are provided for each analog and digital domain. The various practices described in [84], [85] are considered while designing the layout to minimize EMC. The supply and ground pads are placed close to minimize the length of the power loop. Providing a sufficient number of pads are also vital for EMC. The power and ground lines are made as wide as possible, providing a low resistance path throughout the chip. A big array of on-chip decoupling capacitors are provided for all the supply voltages and bias voltages.

The sensitive input pads providing the current to channels 1 and 2 are surrounded by pads with a common voltage. The input pads In1 and In2 thus have a similar environment around them. The length of the signal paths from the pads to the gates of the input transistors of the OTA is matched.

6.5 Measurement set-up and results

The ACCURATE 2A was designed as pin compatible with ACCURATE 1. Hence, the same test board could be used for the characterization of the analog-only chip. The micrograph of the die is shown in Fig. 6.12.

The UART data was readout in MATLAB as seven 32 bit words for the analog chip and eight words for the mixed-signal chip. For synchronization, the UART data packet includes an identifier word. This word is used as the index to identify the different data words in a single packet. The current calculation is carried out based on various counts received. The current measured from DSM method is

$$I_{\mathrm{DS}} = \frac{\gamma C_{\mathrm{f}}}{T_{\mathrm{int}} t_p}, \tag{6.3}$$

where γ is the proportionality factor taking into consideration the effects of variation of the feedback capacitance and the effective threshold voltage difference between the first two thresholds, C_{f} is the nominal value of the feedback capacitance(= 5 pF), and t_p is the system time period (= 10 ns). T_{int} is the number of clock periods between two comparator outputs. With a sweep of input currents, the best fit value is chosen for γ to minimize errors.

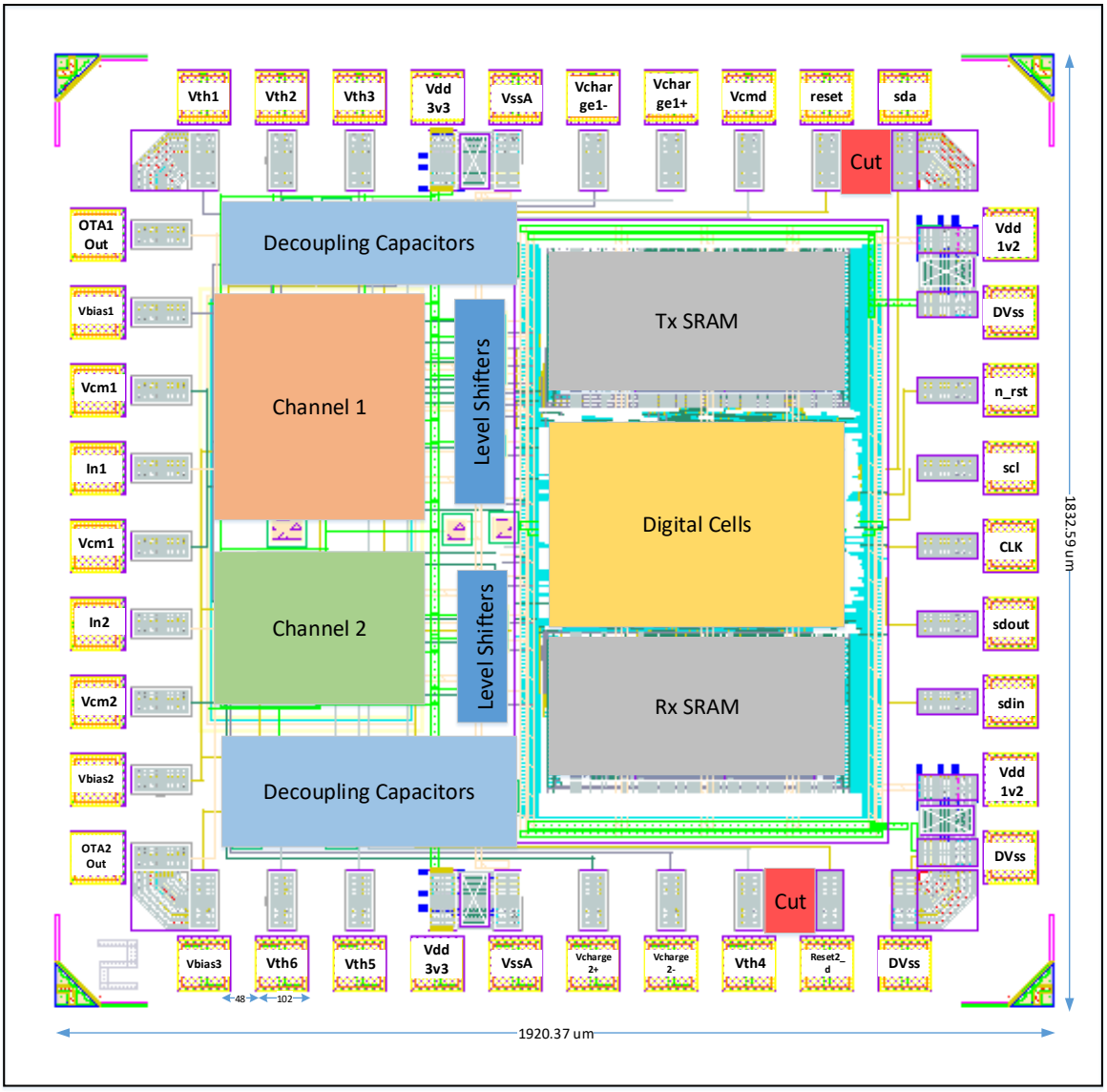


Figure 6.11: ACCURATE 2 layout

Three other counts received are N_{low}, N_{medium}, and N_{high} which correspond to the number of low charge, medium charge, and high charge injections in a fixed time period, T_{window}. The current thus calculated based on the CB method is

$$I_{\text{CB}} = \frac{aN_{\text{low}} + bN_{\text{medium}} + cN_{\text{high}}}{T_{\text{window}}}, \tag{6.4}$$

where a,b, and c are the calibration factors that represent the effective charge generated by each branch of the charge generation block. All these factors are determined by the calibration of the chips by sweeping the current. Different current ranges are chosen such that the charge injection blocks are progressively activated to calibrate each channel. An example of the spread of data counts received for different current values is shown in Fig. 6.13.

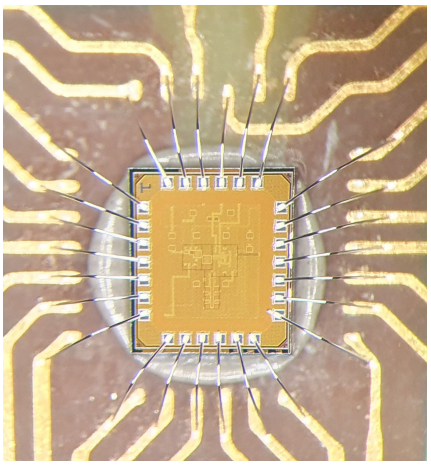


Figure 6.12: Micrograph of ACCURATE 2A

For the first current (-500 nA), only the low charge injection block is enabled and the number of counts generated in a time window of 40 µs for 5000 different data packets are plotted in the first subplot. As the current increases the value of N_{low} increases and for a current of -2.6 µA there are both the low current counts and medium current counts. In the case of -7.2 µA the N_{low} approaches saturation value of 250 and all the three counts N_{low}, N_{medium}, and N_{high} coexist. For the highest measured current of -20 µA, the low and medium current counts saturate. For currents above -20 µA, all the currents saturate and any further change in the input is not detected by the ASIC.

The details of the board used for characterizing the mixed signal ASIC are shown in Fig. 6.14. The board is partitioned with separate analog and digital islands. Apart from the chip, the board also houses a microcontroller – SAM D21 from Microchip Technology. The inclusion of this microcontroller is to provide an interface to the supervision software in the next version of the board. The current version of the board can be configured such that the ASIC can function alone without the microcontroller. The different functionalities currently handled by the microcontroller are listed below.

1. Providing an alternate way for programming the DACs and reading the temperature and humidity data.
2. Provide a second UART channel for communicating with a test software.
3. Controlling the resets of the ASIC.

There are also different level shifters on the board. The clock is generated by a MEMS oscillator. The generated 3.3 V clock is fed to a buffer supplied with 1.2 V to convert the clock to the 1.2 V domain. Bidirectional level shifters are used for the I2C signals. The UART signals are converted using direction controlled level shifter. In the default operation, the UART ports of the ASIC are fed to a UART to USB converter to be interfaced to the test PC. The board, however, also allows the UART data to be directed to the microcontroller which then sends it out through a USB bridge.

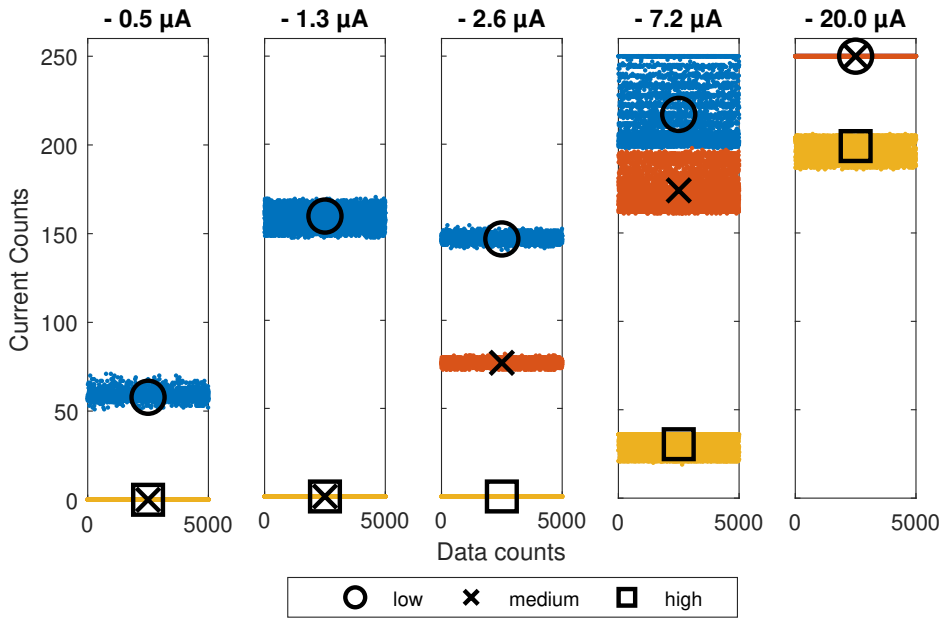


Figure 6.13: Spread of charge injection pulse counts for different currents

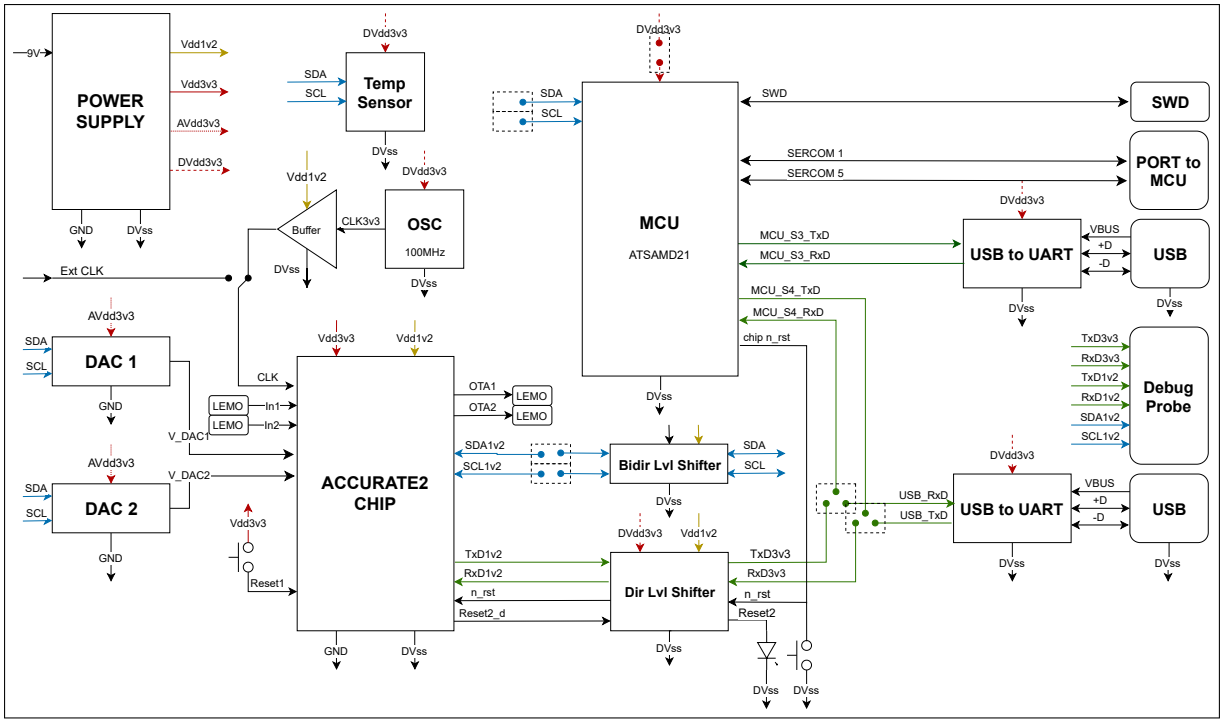
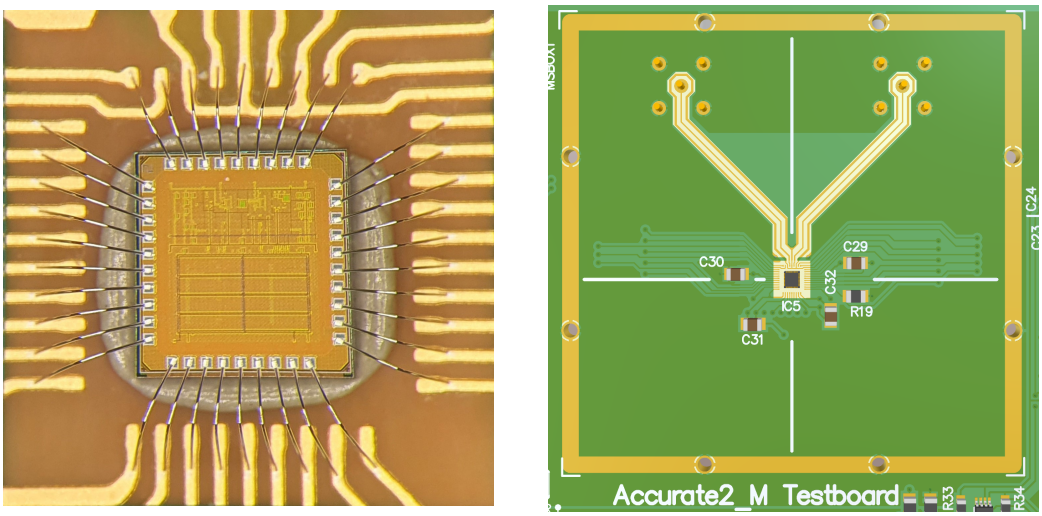


Figure 6.14: Details of test board of ACCURATE 2M

The ACCURATE 2M chip and the bonding section on the test board are shown in Fig. 6.15. The input current path is routed on the top level and the solder mask is removed in the area. The paths for both the channels are matched and are enclosed within a signal track running the common-mode voltage. The metal layers from the inner layers are removed below the sensitive track to avoid any coupling through the PCB stack. The entire chip is surrounded by a ground

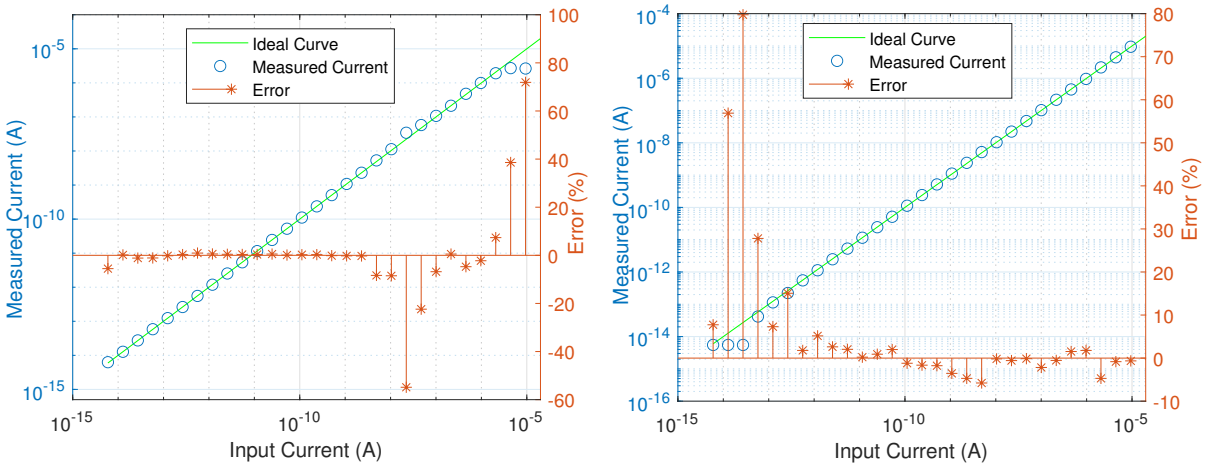


(a) (b)

Figure 6.15: ACCURATE 2M of (a) micrograph, (b) bonding section on test board

track on which a metallic box is soldered to minimize EMC issues. The digital signals from the chip are routed on the bottom layer and the oscillator is also placed on the bottom layer.

To minimize the influence of external interference and to eliminate the dependency on temperature, the board was characterized inside a climatic chamber at a temperature of 25°C. A Keithley 6430 current source, which was kept inside the chamber, generated precise currents. In ACCURATE 2A the time window of measurement was 100 ms. The response of the ASIC when injected with different currents from −6 fA to −20 µA is shown in Fig. 6.16. The absolute values of the currents are used in the plot.



(a) (b)

Figure 6.16: Current measured by ACCURATE 2A when injected with current from −6 fA to −20 µA (a) direct slope method, (b) charge balancing method

The received data from the ASIC were averaged to create an effective time window of 100 seconds to measure the ultra-low currents. For the chosen time window the CB method did not

accumulate enough counts to have an accurate representation of the input current for currents less than 1 pA. Hence, the measurement error was quite high. However, in the higher range, the measurement was precise.

In the case of the DSM method, currents from femtoamperes to nanoamperes were precisely measured with an accuracy even better than the CB method. The method could measure current up to around 1 µA, beyond which the method saturates. The time window to be precisely determined reduces, which makes the measurement more erroneous beyond the nanoampere range with this method. Based on the raw counts received, a decision algorithm in MATLAB chooses the best values from both the current measurement methods. The combined output hence generated is plotted in Fig. 6.17. It can be observed that, in the specified environment, the maximum error in the measurement of currents from -6 fA to -20 µA by ACCURATE 2A is $\pm 6\%$.

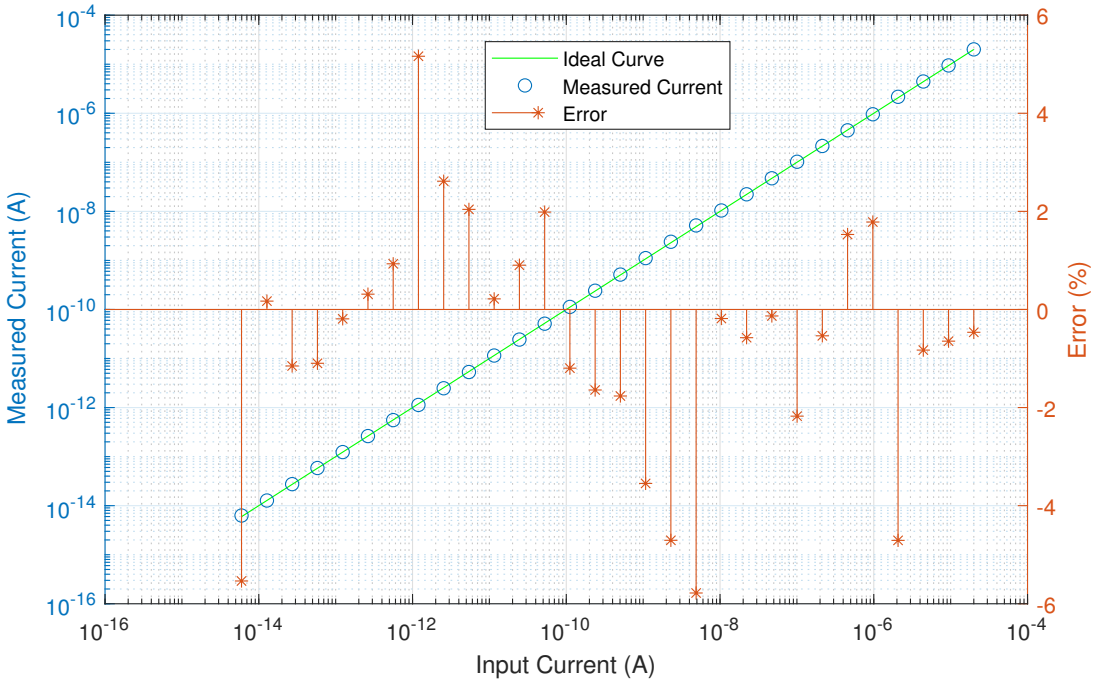


Figure 6.17: System linearity of ACCURATE 2A

The lower measurement range was determined from the total input bias or leakage current. The net input bias current was observed to be around 6 fA. Hence, for any current less than this, the OTA output integrates in the negative direction. Since the target application is for acting as the front end of ionization chambers whose output current is always negative, the system was designed to measure only negative currents. As a result, when the effective input current is positive, the system does not output any measurement.

For the mixed signal chip, the maximum time window length could only be set to 40 µs instead of the default value of 100 ms. This has to be corrected in the next version. As a result, the lower usable limit of the CB method was shifted to around 10 nA. The shorter time window resulted

in a lower number of counts to be collected in a window. Also, with the decrease in the time window, more data packets were generated and the memories were filled before reading out all the data. For higher current, sufficient numbers of counts were obtained in each current time window and the measurement was accurate. The DSM method, which was independent of the time window, could be used for determining the current in the lower range. Thus, by combining the results of the two methods, the limitation of the time window could be overcome and the ACCURATE 2M chip could also measure currents from around −7 fA to −20 µA with similar accuracy as ACCURATE 2A.

The bias current of the ASICs was determined by observing the integrator output directly with an oscilloscope. For the value of bias current of opposite polarity, the integrator slope becomes zero. In the tested chips, the net input bias current was observed to be around 6 fA to 7 fA. To determine the minimum current resolution that could be accurately measured, the input current was varied from −5 fA to −10 fA in steps of 200 aA. The output obtained is plotted in Fig. 6.18.

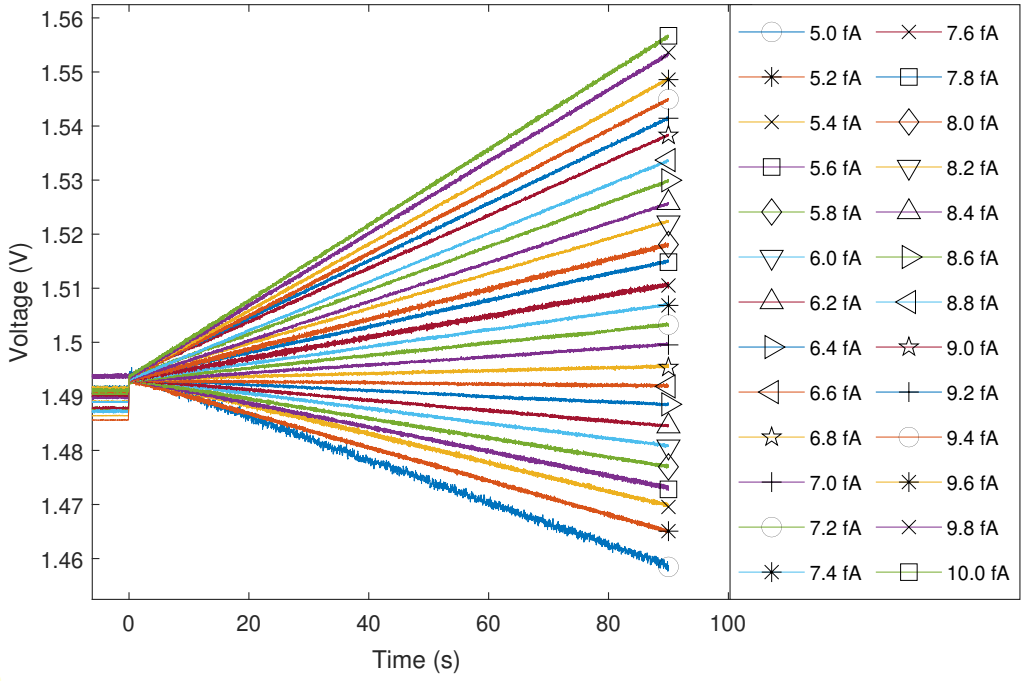


Figure 6.18: Integrator output with input current swept from −5 fA to −10 fA in steps of 200 aA

The observed output was obtained after averaging 25 times for each current bin to remove the effects of noise. The OTA was reset using a pulse with an on-time of 10 seconds and an off-time of 90 seconds. The microcontroller was used for generating the reset and timing the measurement. The plotted data when used in MATLAB for current calculation also yielded accurate results with errors less than 1%. The demonstrated 200 aA is the best resolution achievable with the existing set-up. The current source is rated for providing attoampere sensitivity [86] and have demonstrated attoampere measurement capability[87]. The time to achieve this resolution is however attributed also to the high-speed ADC of the Lecroy HDO6104-MS oscilloscope.

ACCURATE 2M being the more error prone among the two versions, was used for determining the best current resolution using the full measurement chain. Current from −10 fA to −13 fA was injected and measured by the ASIC, as shown in Fig. 6.19. The current measured in the first iteration was used as the net bias current to compensate the whole data set. Thus, it was demonstrated that the current measurement with 200 aA sensitivity is accurate to ±1%. The injected current is sensed by the same source current source and the error is calculated in comparison to this sensed current. The current measured is using the DSM method. The first two comparators had threshold voltages of 1.6 V and 1.7 V respectively. The measurement was hence observed after 300 seconds. This thus represents the actual time required for the measurement by the ASIC alone.

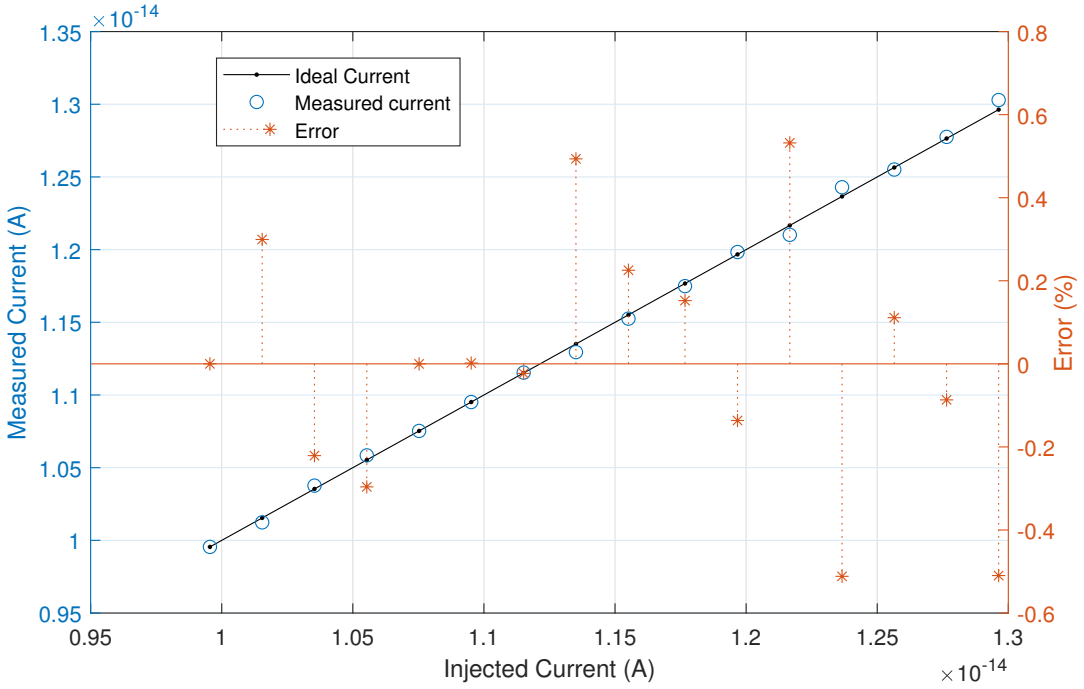


Figure 6.19: ACCURATE 2 output with input current swept from −10 fA to −13 fA in steps of 200 aA

6.6 Conclusion

The design details of the ACCURATE 2 series of ASICs were presented in this chapter. The design presents an extension of the architectures already analyzed in Chapter 5 with the design of ACCURATE 1 ASICs. By employing two current measurement methodologies in parallel, the range of measurement was improved without compromising the time of measurement. It was demonstrated that the ASICs can achieve a remarkable dynamic range with a minimum resolvable current of 200 aA.

ACCURATE 2A, the analog only version has the feedback capacitance increased to 5 pF from 1 pF used in ACCURATE 1. Additionally, two charge generation blocks were included for generating 1 pC and 4 pC charges which helped in increasing the maximum measurable current

to -20 µA from -1 µA attained by ACCURATE 1. The increase of the feedback capacitance helped to increase the dynamic range too since more charges could be collected. The improvement in the sensitivity is also attributed to the increased capacitance since the interval count, which is used for current measurement in the direct slope method, increased five times and hence could be distinguished with better precision. The chip reported a power consumption of around 3 mW and occupies an area of 1.95 mm^2.

The mixed signal version, ACCURATE 2M, with the additional secondary channel and digital section also achieves similar performances for sensitivity and dynamic range. Various considerations that were taken in the mixed signal layout to minimize the cross-talk between the analog and digital domains were detailed. The area occupied is 3.52 mm^2 and the total power consumption increased to 17.4 mW. The digital section reported 10.8 mW consumption contributed primarily by the SRAMs. The different aspects considered while designing the test board for such a mixed signal chip for ultra-low current measurement were also explained in the chapter. The behaviour of the ACCURATE 2 ASICs when interfaced to different ionization chambers and with different temperatures is explained in the next chapter.

Chapter 7

Characterization of ACCURATE 2

ACCURATE 2 ASICs were extensively tested for linearity for a measurement range from femto to microamperes. The results presented in Chapter 6 were based on testing the ASIC with Keithley current sources 6430 and 263. The presented measurements were carried out in ideal conditions. This chapter explains in depth various measurements performed with the ASIC in different application scenarios.

7.1 Measurements with radioactive sources

ACCURATE 2 chips were extensively tested with different kinds of ionization chambers exposed to different dose rates. Tests were performed with all the three main types of ionization chambers used at CERN for radiation protection– Centronic IG5-A20, IG32-A3.1, and PTW PMI T32006.

The measurements were performed at the Calibration laboratory at CERN [88]–[90]. This facility is primarily intended for calibrating the radiation protection monitors at CERN and the qualification of different instruments to be used in radiation areas. The installation in the laboratory is shown in Fig. 7.1.

Figure 7.1: Calibration laboratory set-up

The radioactive sources are securely stored with shielding at a level a few meters below the metal floor of the hall shown in the picture. The irradiator shown is for the gamma source [91]. The source, when it needs to be exposed, is transported to the right position by compressed air through pneumatic tubes and is held by a suction pump [92]. The ionization chamber is placed on a movable table whose distance from the source can be adjusted remotely to vary the received radiation dose. Cesium 137 sources at different activity levels

were used for the characterization. The source is exposed through a collimator, which provides a circular beam. The selection of the source, time of exposure, and position of the table for the desired dose rate are all controlled through a software interface.

Three sets of tests were performed at this facility. The objective of the first measurement campaign was to ascertain the operation of the ASIC when interfaced to an ionization chamber and to evaluate the dose measurement in comparison to the existing radiation monitoring system used at CERN – CROME. The second set of tests extended the objectives by interfacing the ASIC with two more kinds of ionization chambers. Additionally, the effective dose measured by the ASIC was compared to that measured by a reference electrometer at different radiation levels using different Cesium 137 sources. To evaluate the performance at even higher dose rates, a third set of measurements with a Cobalt 60 source was also performed. The measurement set-up used is shown in Fig. 7.2.

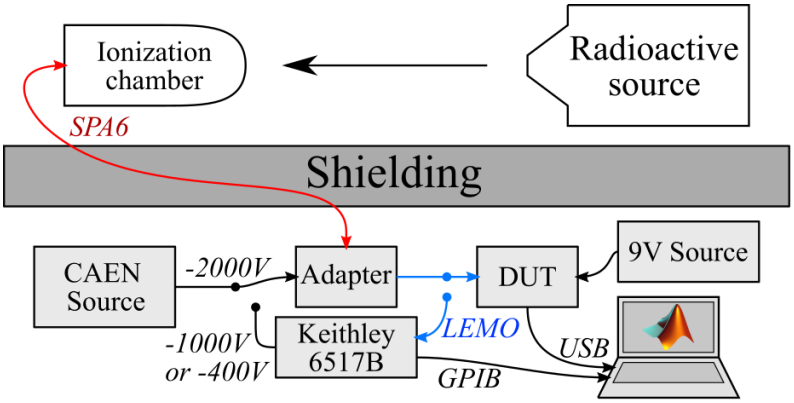


Figure 7.2: Measurement set-up at calibration laboratory

The output from the ionization chamber is brought out with an SPA6 cable outside the irradiation hall. The cable is also designed to carry the high voltage required for biasing the chamber. The signal and high voltage paths of the cable are separated in an adapter box. The signal is then fed to the ASIC or an electrometer. The Keithley 6517B was used as the reference meter and also for the generation of the high voltage. An additional voltage source (CAEN NDT1471) was used for polarisation above −1000 V. The tests were done sequentially with the output first measured by the electrometer followed by the ASIC. The electrometer was operated through a GPIB interface and the output of the ASIC was read through a USB interface in the MATLAB program.

7.1.1 Comparison with CROME

In the first measurement, two IG5 ionization chambers were placed side by side on the measurement table with the output of the first chamber connected to CROME and the output from the second one to ACCURATE 2A. The chamber was supplied with −1000 V by the 6517B. Cs-137 sources with activity levels of 300 MBq, 3 GBq, and 30 GBq were used to generate dose rates from 5 µSv/h to 80 µSv/h. The results obtained are plotted in Fig. 7.3. Currents measured using both the DSM and CB methods were recorded. A conversion factor of 1.45 µA/(Sv/h) was

used to convert the current measured by ACCURATE 2A to a radiological dose rate. It could be seen that the dose rate measured by the ASIC matches well with that measured by CROME. The small mismatch could be assumed to be coming from the non-homogeneity of the field with the chambers not receiving the same dose rate.

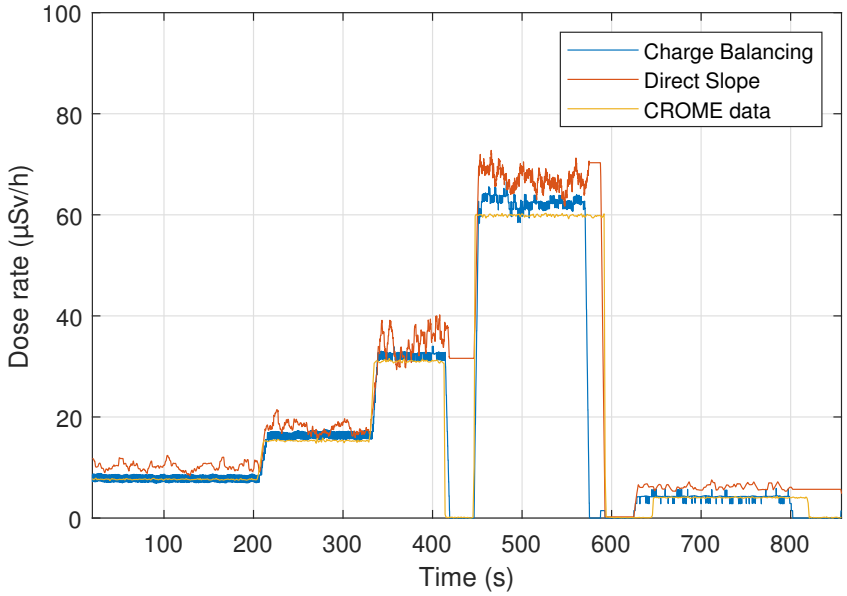


Figure 7.3: ACCURATE 2A measurement in comparison with CROME

The measured data shows that the charge balancing provided a more stable output compared to the DSM. There are two reasons for this behavior. It was observed with an oscilloscope that the output from the ionization chamber is very noisy and the coupled noise at the OTA output was around 100 mV. Even with the hysteresis and digital debouncing, the comparator outputs fluctuated. This results in measurements that are slightly offset from each other. The solution would be to increase the hysteresis. The CB method, which is more immune to comparator parameters, produced a better output. Another factor is that the output of the interval counter which gives the time difference of comparator outputs is read at the end of a measurement window (100 ms for ACCURATE 2A). With this approach, if the interval measured was shorter, only the last measured value is read out. By implementing an averaging module that averages all the measurements in the measurement window, the output stability would increase a lot, especially for higher currents.

7.1.2 Comparison with electrometer

The second set of measurements compared the currents measured by the electrometer with that measured with the ACCURATE 2 ASICs for different dose rates. Various sources used to generate different dose rates are listed in Table 7.1. The different currents measured using the direct slope method of ACCURATE 2M when an IG5 chamber was exposed to the specified dose rates are recorded as shown in Fig. 7.4. Each exposure step was timed to be 60 seconds.

Dose rate	Source
5 µSv/h	300 MBq Cs-137
28 µSv/h	3 GBq Cs-137
155 µSv/h	30 GBq Cs-137
866 µSv/h	300 GBq Cs-137
4.8 mSv/h	300 GBq Cs-137
29.9 mSv/h	3 TBq Cs-137
150 mSv/h	3 TBq Cs-137
260 mSv/h	3 TBq Cs-137

Table 7.1: Sources used to generate different dose rates

The spread in the data points is attributed to the noise in the set-up. The initial background dose rate measurement gave a current of around −100 fA.

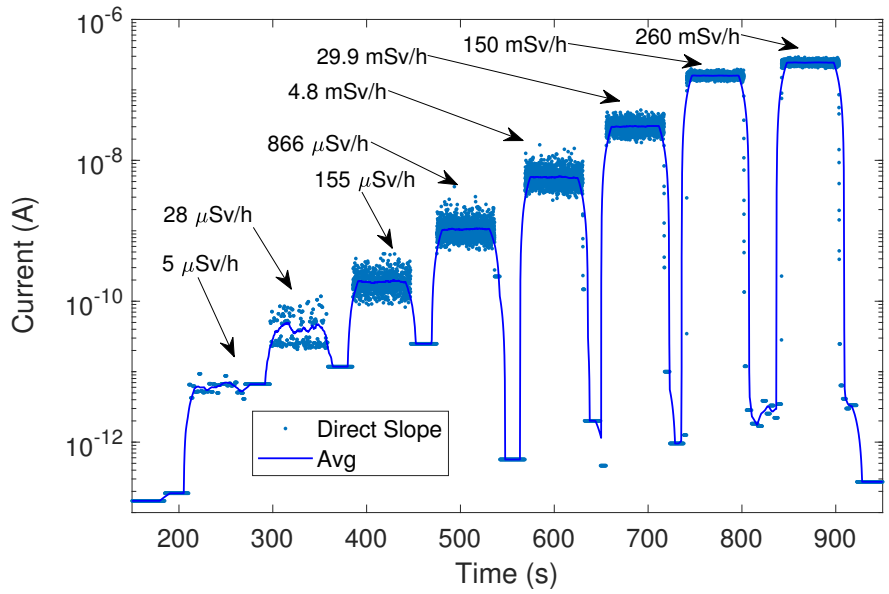


Figure 7.4: Current measured by ACCURATE 2M with IG5 chamber for different dose rates

7.1.2.1 Interfacing with the PTW PMI T32006 chamber

The ASIC was interfaced with the air filled PMI chamber. The chamber was exposed to the same set of dose rates as listed in the previous section. The currents measured by the electrometer for different dose rates are plotted in Fig. 7.5.

The chamber was previously calibrated and the conversion factor determined was 22.9 nA/(Sv/h). The error in the measurement with the electrometer is high only for the first and the last dose rates. For the first dose, the equivalent current was around −140 fA. The measurement time window of 60 s was not sufficient to determine the current in this range accurately. Also, the background current measured by the chamber was around −15 fA. The low sensitivity of the this chamber resulted in lower background current compared to that measured

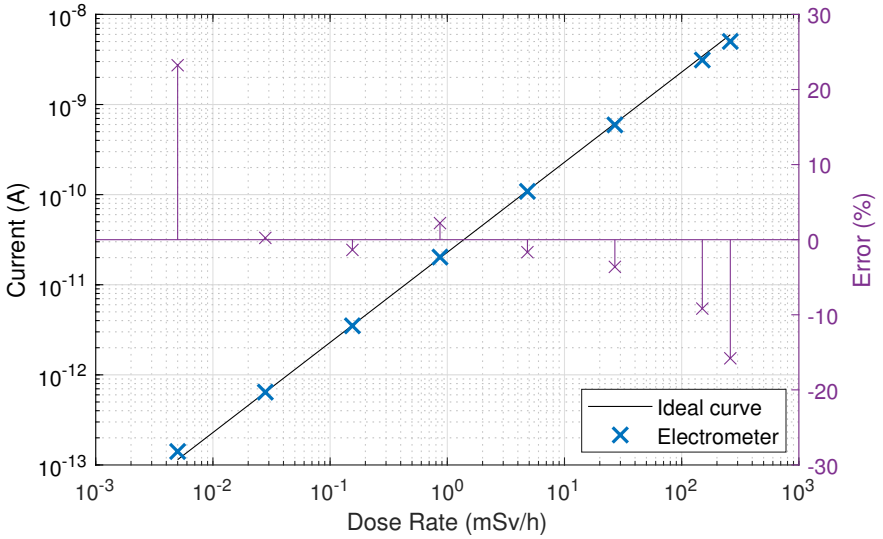


Figure 7.5: Current measured by electrometer for different dose rates

by IG5. The first measurement point was not very different from the background and hence was more susceptible to the background noise. For the last dose rate, this dose was achieved by placing the chamber very close to the collimator. In this condition, it could be assumed that the entire active volume in the chamber is not fully ionized and hence the charge generation is lower, resulting in a current different from the calibrated value.

The measurement with the electrometer was followed by the two ACCURATE 2 chips - ACCURATE 2A and ACCURATE 2M. The current measured by the chips and the error in measurement taking the electrometer reading as reference is shown in Fig. 7.6. It was demonstrated that both chips could measure the current with great accuracy. The error in the first measurement, as explained previously, is due to smaller measurement time and background noise.

7.1.2.2 Interfacing with IG32 chamber

ACCURATE 2A was also tested with IG32 chambers. It was found to be generating a lot more noise compared to the other chambers. Also, the background current generated when there was no source fluctuated a lot. Since the chamber was not calibrated, a calibration factor was derived from the average value of the conversion factor for different dose rates with the electrometer. The factor thus calculated, 103 nA/(Sv/h), was used to derive the effective dose rates measured by the ASIC. The current measured by the electrometer and the ASIC for different input dose rates with the mentioned conversion factor is plotted in Fig. 7.7.

In the test range, it was found that the measurement is linear. The first data point being an outlier is explained by the higher noise generated by the chamber.

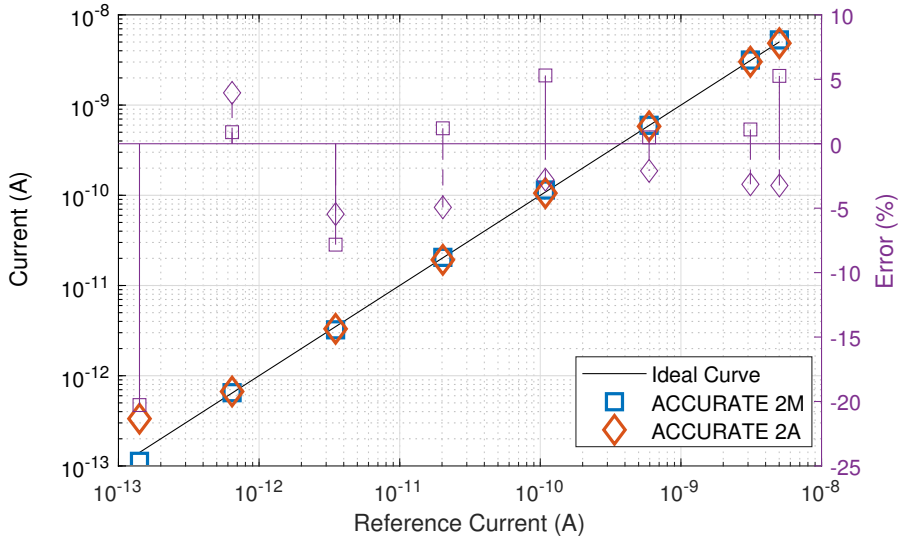


Figure 7.6: Current measured by ACCURATE 2 ASICs with PMI chamber compared with that measured by electrometer for different input dose rates

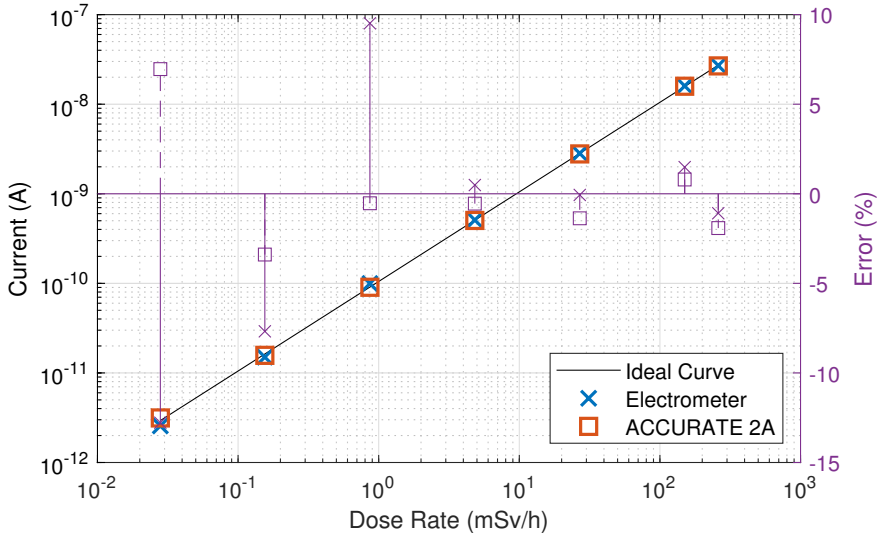


Figure 7.7: Current measurement with IG32 chamber

7.1.2.3 Interfacing with the IG5 chamber

The measurement with the IG5 chamber was accomplished with two different set-ups. To generate higher dose rates, Cobalt 60 sources were used in addition to the Cs-137 sources. The current measured by ACCURATE 2A compared with that measured with the electrometer is shown in Fig. 7.8.

Thus, using different ionization chambers, a current measurement from around -100 fA to -5.5 µA was demonstrated. The ASICs could measure currents in this broad range with acceptable accuracy. The error is influenced largely by the set-up itself. The sources used in the measurement are stored in a container as shown in the Fig. 7.9(b). Every time the source

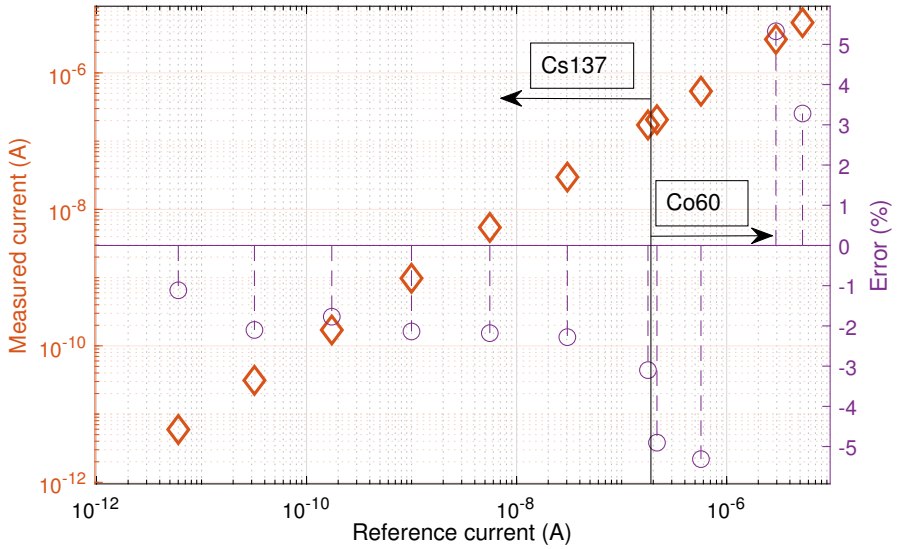
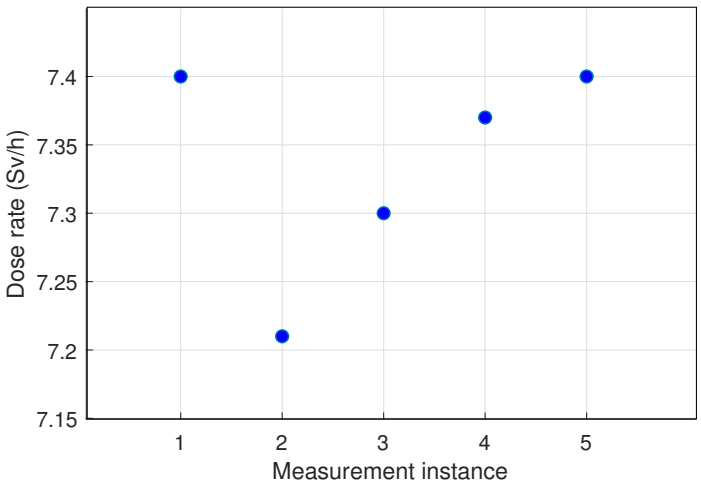


Figure 7.8: Current measurement with IG5 chamber

is bought back to the exposure zone by the pressurized system, the alignment of the source in the container can vary. This can lead to small differences in the net dose rate. The variation in the dose rate measured by a reference meter at the same exposure conditions for five different instances is plotted in Fig. 7.9(a). The measurement shows a variability of around 2.5%. This contributes to the error in the measurement as the measurements are done sequentially by lowering and pushing the source between each iteration.



(a)

(b)

Figure 7.9: (a) Dose rates measured at the same exposure settings, (b) container of the radiation source

Thus the measurements with the radiation sources demonstrated the capability of the ACCURATE 2 chips to interface with different kinds of ionization chambers. The ASICs were able to precisely measure the dose rates from around 5 µSv/h to 7.4 Sv/h. The demonstrated limits arise from the measurement set-up used. The maximum current reached with the radiation

sources was around −5 µA. Stronger sources are required to extend the current range in the continuous measurement regime.

The characterization with radiation sources demonstrated the static current measurement capabilities of the ASICs in real application scenarios. The radiation monitors are installed in the vicinity of the particle accelerators where the radiation profile is pulsed rather than continuous. Hence, the behavior in such environments had to be assessed. The next section explains the experiments carried out in the presence of pulsed radiation.

7.2 Characterization of ACCURATE 2 with pulsed radiation

The Proton Synchrotron - Antiproton collector Irradiation Facility (PSAIF) [93] at CERN was used to determine the measurement efficiency of ACCURATE 2 with a pulsed input current. The facility sits on top of the target of the antiproton factory (AD). A typical mixed radiation field produced near the particle accelerators is generated when the protons from the proton synchrotron (PS) hits the target. The facility consists of a hole of around 8 m depth, reaching close to the beam line of the AD. The access to the pit is provided through a tube, which is shown in Fig. 7.10.

Figure 7.10: PSAIF pit

An IG5 A20 ionization chamber was inserted and held at different positions with the help of ropes. The high voltage input and output signal interface to the chamber was made with the red SPA6 cable. The chamber height determined the strength of the received radiation pulse. The facility allows parasitic operation when the AD beam is active. In the normal operation, the beam is composed of around $1.5 * 10^{13}$ protons per pulse. The pulse width is around 500 ns with a repetition of around 100 s.

The measurement electronics was installed in an adjacent room, as shown in Fig. 7.11. The ionization chamber was biased with -1000 V provided by the Keithley 6517B electrometer. The electrometer was also used as the reference to measure the charges produced for each position of the chamber. The output of the chamber was connected sequentially to the electrometer, UTOPIA 2, and ACCURATE 2A. The charges measured by the three systems were recorded using MATLAB. A neutron counter recorded the ambient dose rate in the room.

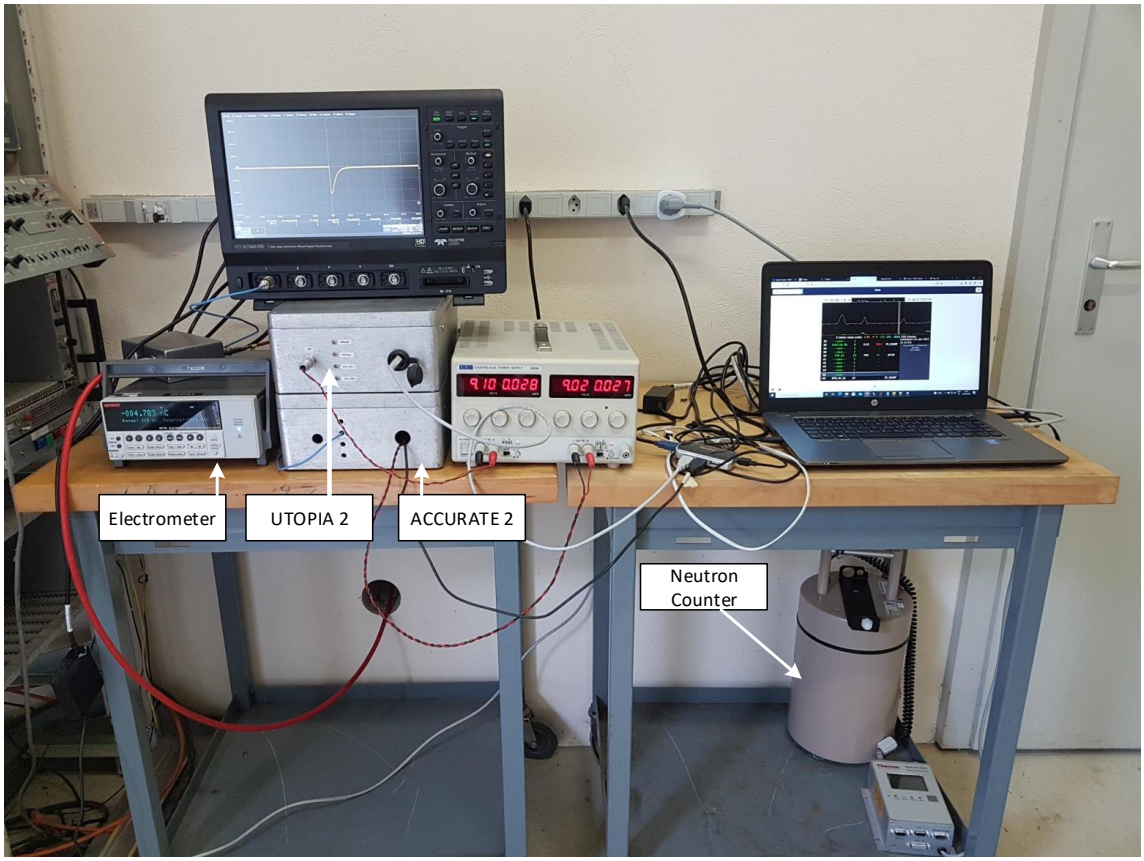


Figure 7.11: Measurement set-up at PSAIF

The output of the chamber was also measured using an oscilloscope. The current from the chamber measured with the 1 MΩ input resistance of the oscilloscope is shown in Fig. 7.12. The discharge of the charges collected by the chamber exhibits exponential behavior with 90% of the charges discharged within 10 ms in this configuration. It was found that almost 100% of

the discharge was completed within 100 ms for the charges recorded. The quantity of charge collected by the electrometer was validated by estimating the area under the discharge curve recorded by the oscilloscope.

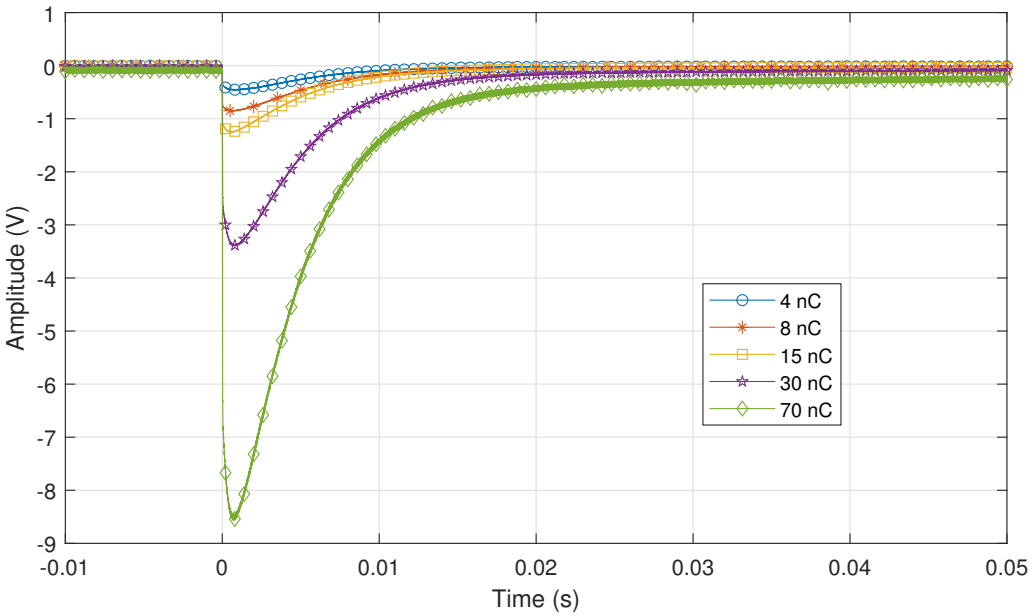


Figure 7.12: Ionization chamber output recorded by the oscilloscope with 1 MΩ input resistance

A set of eight data points were recorded corresponding to charges from 1 nC to 110 nC. For each of the data points, five pulses were recorded per instrument. The recorded charges were normalized with the actual number of protons in each charge pulse as measured by a dedicated monitor at the level of the accelerator. An average of the pulses received for each data point was calculated for each instrument. The charges measured by ACCURATE 2A and UTOPIA 2 and the corresponding error in comparison to the charges measured by the reference electrometer are plotted in Fig. 7.13.

It can be seen that both ASICs can precisely measure charges until around 15 nC. The error in measurement increased with the input charge. For an input charge of 110 nC, the errors in the measurement for ACCURATE 2 and UTOPIA 2 were around 40% and 55%, respectively. Thus, it was demonstrated that the charge measurement capability of the ASIC could be improved. The two main factors that contributed to the improvement are the increase in the feedback capacitance from 1 pF to 5 pf and the addition of the high charge branch for charge balancing.

The reasons for the charge losses in the system were investigated. The speed of the system was found to be the main limiting factor. The output of the OTA integrator of ACCURATE 2A when an input pulse of 55 nC is injected is shown in Fig. 7.14.

The low impedance path between the detector output to the OTA input allows the instantaneous transfer of created charges from the chamber to the feedback capacitor (Cf) in the presence of an input radiation pulse. It was found that, even with 1 nC input charge, the OTA output saturates,

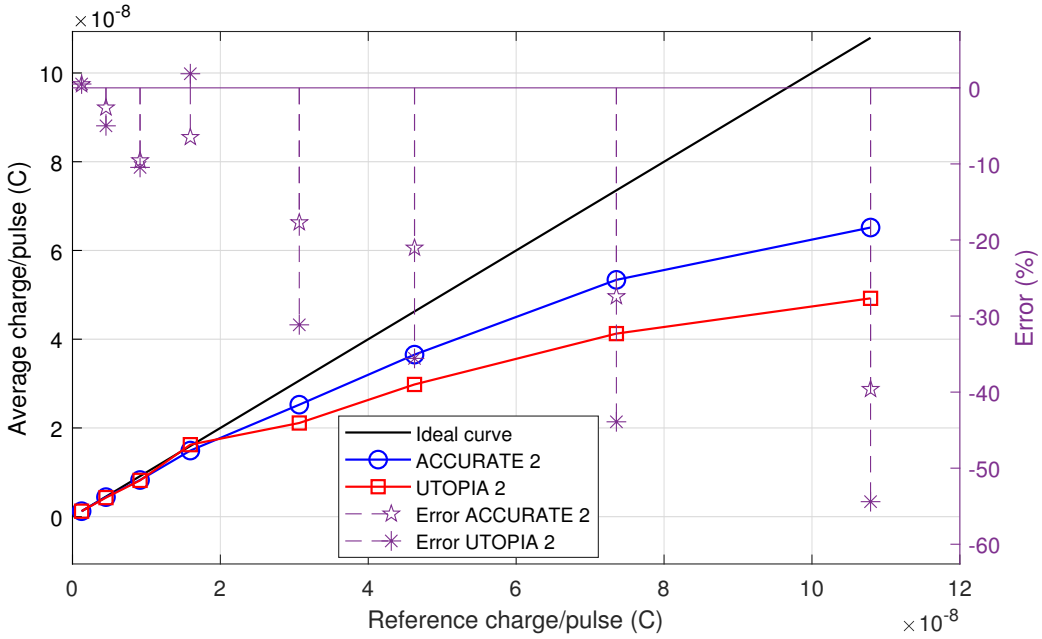


Figure 7.13: Charges measured by ACCURATE 2A and UTOPIA 2 with pulsed radiation

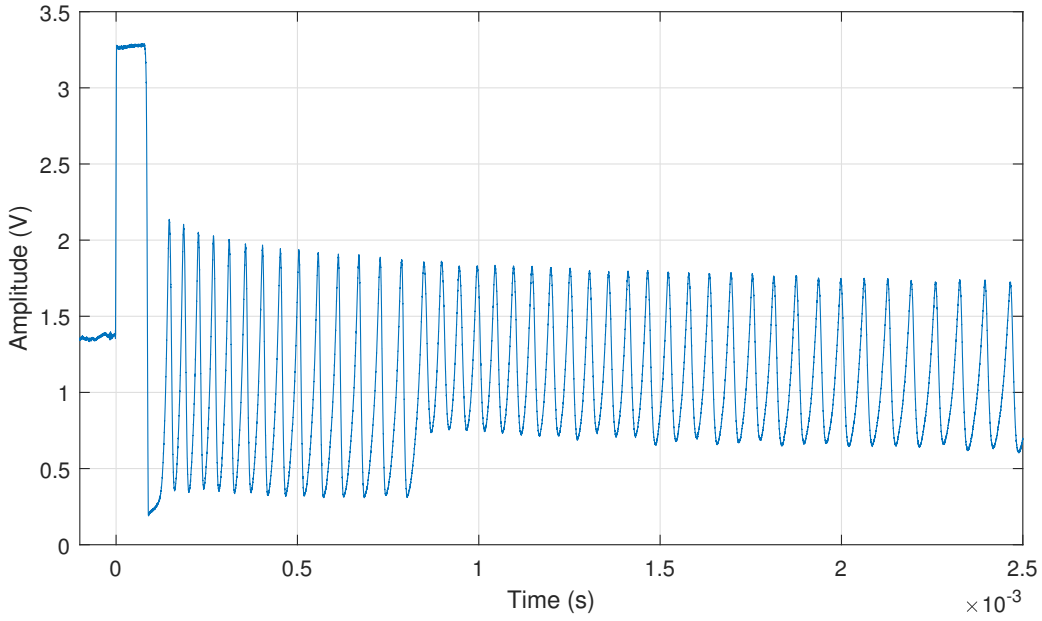


Figure 7.14: OTA output of ACCURATE 2A with an input pulse of 55 nC

reaching 3.3 V within a few microseconds. For an input charge of 8 nC the OTA output ramps from common mode voltage of 1.5 V to supply voltage of 3.3 V in around 2 µs, suggesting that the input current at the instant was around 3.75 µA. However, the output remains at 3.3 V for around 85 µs. This indicates that the current output from the chamber ramped to a higher value than that could be measured by the ASIC. All three comparators are triggered simultaneously, activating the low, medium, and high charge generation blocks. The amount of charge that flows

to Cf is so high that the total charge subtracted by the charge generation block is not sufficient to discharge Cf. The maximum charge that can be balanced by the ASIC in around 200 ns is 5.5 pC. This quantum is significantly lower than that created by the chamber. Thus, the OTA remains in saturation for a duration proportional to the input charges. During this duration, the charges that flow from the chamber are lost through the output stage of the OTA. A huge flux of particles is created the moment the proton beam hits the target. The number of secondary particles created decreases with time, thus lowering the output of the ionization chamber. As the charge generated by the chamber decreases, the charge generated by the charge generation of the ASIC becomes comparable to the input charge and the OTA returns from saturation. The discharge continues for hundreds of milliseconds depending on the input charge. Thus, the percentage of the charge generated by the chamber that is collected by the ASIC decreases significantly with an increase in input charge.

To increase the charge collection efficiency, the simplest method is to insert a resistor in the input path of the ASIC. The time constant of the charge transfer from the chamber to the feedback capacitor increases, thus preventing the OTA from saturation. A sudden huge influx of charge is controlled, thus allowing the charge generation block to precisely balance the received charge. The effectiveness of the method was experimentally determined by introducing a 50 MΩ resistor between the chamber output and the ASIC input. The experiment was repeated for different input charges and the charges were collected by the electrometer and ACCURATE 2A. The error in charge collection is plotted in Fig. 7.15.

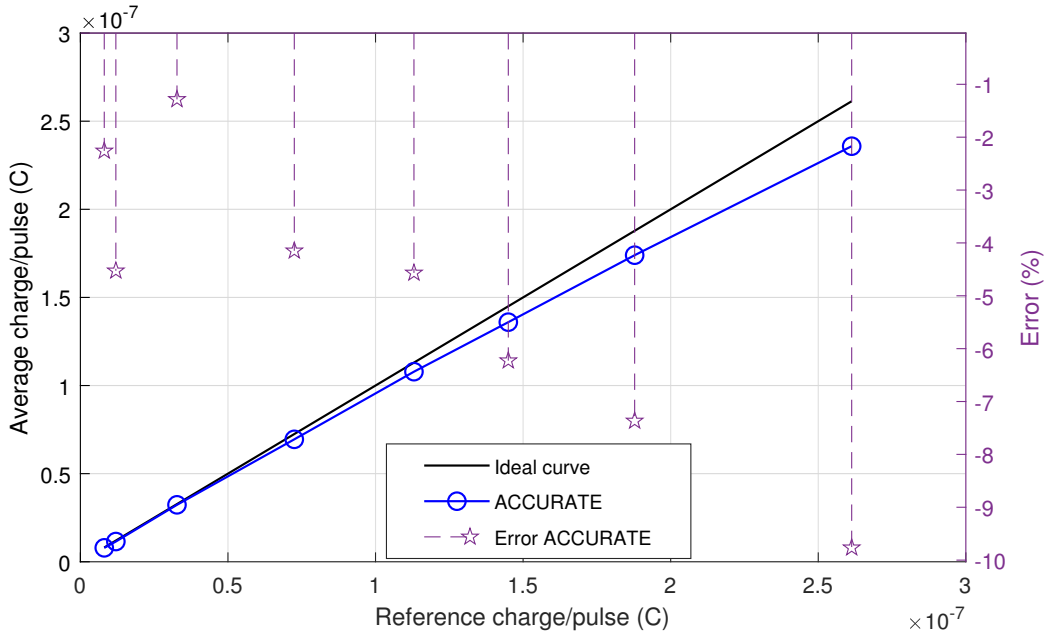


Figure 7.15: Charges measured by ACCURATE 2A with 50 MΩ input resistor

The charge collection efficiently increased significantly. For charges around 110 nC, the error decreased from 40% to 5%. Measurements were continued until around 260 nC and the error was still less than 10%, which is the determined accuracy of the ionization chamber, even with a

continuous radiation dose. For even this high charge, only the low charge block was triggered and the OTA could precisely measure the generated charges. This method, although it helped in understanding the limitation, cannot be employed for all the systems as the noise generated by the resistor is significantly high, impairing the low current measurements. The introduction of the resistor also generates additional leakage current from the voltage difference arising across it due to the common-mode voltage of the OTA. Hence, a very high value is required to limit the leakage. This value remains constant at a given temperature and can hence be compensated. The plot shown in Fig. 7.15 is obtained after subtracting this extra leakage current. Increasing the feedback capacitance further can also improve the charge collection capability. The OTA design also has to be adapted for higher bias currents. Another solution is to connect multiple ASICs in parallel so that the total charge is split among them. The sum of the charges collected by different ASICs should more accurately represent the total input charge. This arrangement would need additional switches which operate in a complementary fashion so that the charge balancing from one ASIC does not interfere with that of the others. These solutions will be explored in the next version of the ASIC to increase the charge collection limit.

7.3 Influence of humidity on current measurement

ACCURATE 2M was characterized also to study the influence of humidity on the low current measurement. The ASIC bonded on the test board was placed in a climatic chamber where the temperature was controlled but with varying humidity levels. An input current of -10 fA was injected. The ASIC measured the temperature and the humidity using the onboard sensor during the measurement time. The obtained result is shown in Fig. 7.16. As the humidity was not controlled, at lower temperatures the level of humidity rose exponentially. It was interesting to find that the current measurement followed exactly the path of humidity change and rose with its levels. The leakage current increased from around 7 fA to 70 pA at the peak humidity level observed.

A strong influence with humidity was observed since the ASIC is not packaged or hermetically sealed and is vulnerable to external fluctuations.

7.4 Influence of temperature on current measurement

The influence of humidity could be minimized by properly sealing the die, however, the temperature effects are harder to evade. For the sub-picoampere regime, the main consequence of fluctuating temperature is the change in the leakage current. The effect of temperature can be compensated by two methods. An identical second channel that mimics the variation in leakage current in the primary channel with temperature can be used to compensate for the variations. Another method involves characterizing the leakage current with temperature for each system and using the temperature data measured by a sensor to correct the current measurement. The second method is used in the CROME system [94]. A detailed characterization is required

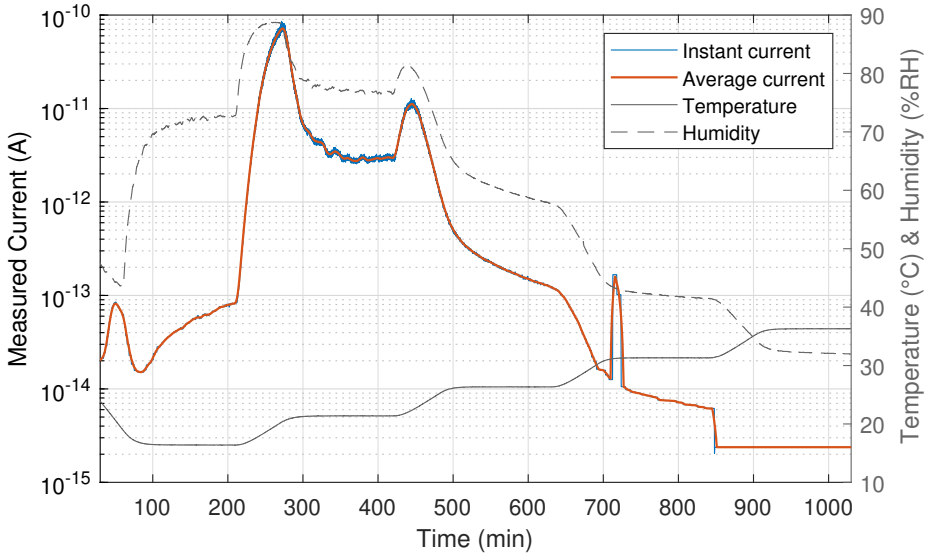


Figure 7.16: Leakage current variation with humidity

to evaluate the dependency of the leakage current on temperature. The results obtained are presented in the next sub-section.

For higher currents, the various non-idealities associated with the measurement method become more pronounced and can impact the measurement accuracy. The influence of temperature on the two different current measurement methods is also studied and presented in further subsections.

7.4.1 Leakage current measurement at different temperatures

The net input leakage current of the ACCURATE 2 ASICs was found to be positive with a value around 7 fA at 25°C. Since the ASIC is designed to measure only negative currents, any input current until this net leakage value cannot be directly measured by the ASIC. The total leakage current could be estimated by two methods – (a) by observing the slope of the OTA by sweeping different currents and determining the current corresponding to zero slope and (b) by finding the difference between the measured current and input current by injecting a current close to the expected leakage. The current calculation by measuring the slope is very time consuming. Hence, the second approach was adopted for characterizing the temperature dependence.

The measurements were performed with a climatic chamber where humidity was regulated and maintained at a level less than 5% RH. The temperature was varied in steps of 5°C from 15°C to 40°C. A current of −20 fA was injected to make sure that the net leakage is negative and could be measured with the ASIC. The result obtained with the DSM method of ACCURATE 2A is shown in Fig. 7.17.

The net leakage was observed to change from −5 fA at 15°C to around −20 fA at 20°C. As expected, the net leakage current increased with an increase in temperature. The current

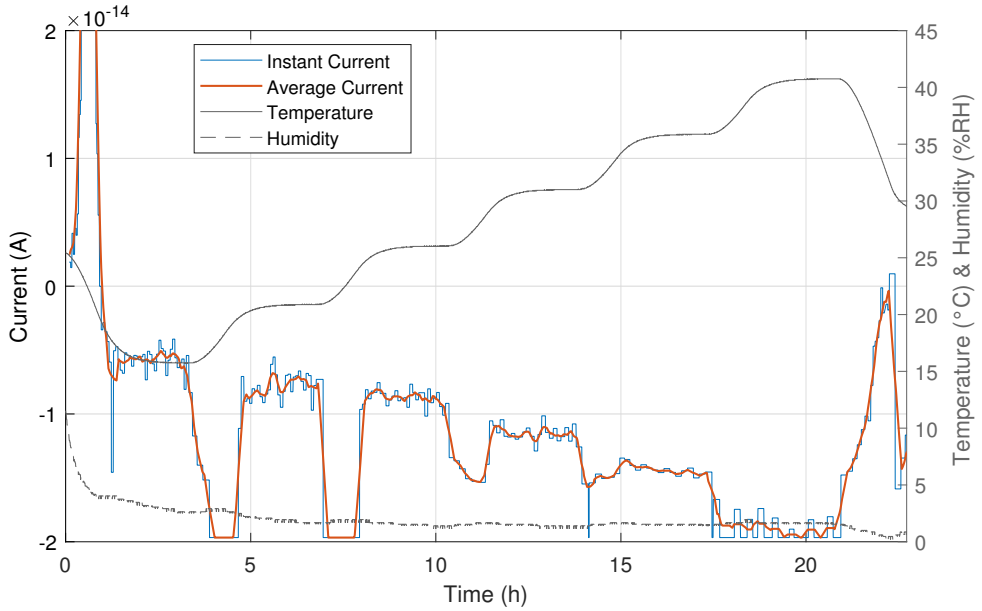


Figure 7.17: Leakage current variation of ACCURATE 2A with temperature

measured by the CB method had similar values. The current was injected by placing the preamplifier of the Keithley 6430 current source inside the chamber. The variation in the current while the temperature is ramping arises from the current source. This behavior was confirmed by measuring the output of the current source directly with a Keithley 6517B electrometer by placing only the preamplifier inside the climatic chamber. The measured current in this set-up is plotted in Fig. 7.18. The current source was found to be regulating the current with temperature resulting in a net increase of only 2 fA in the measured temperature range.

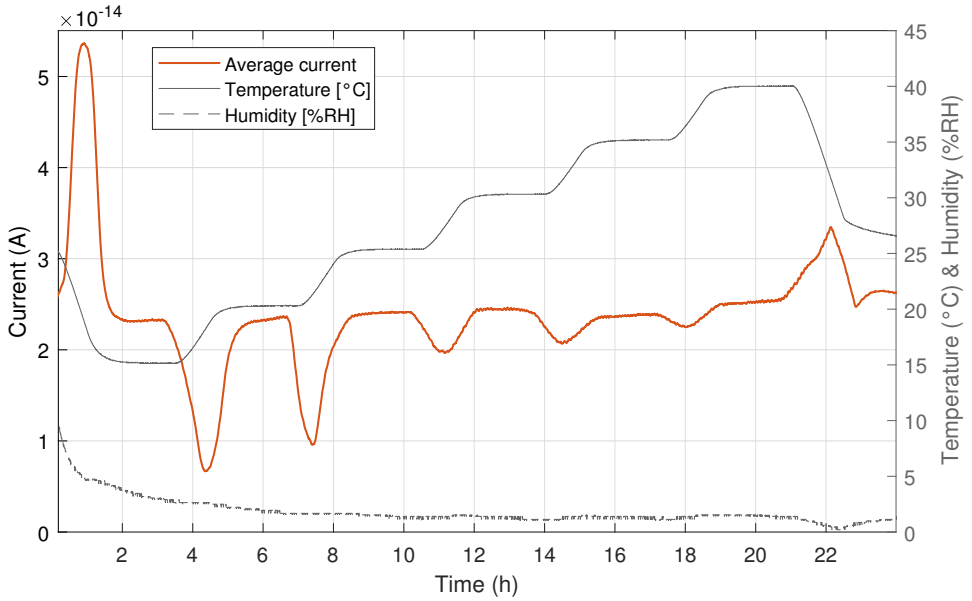


Figure 7.18: Output variation of Keithley 6430 current source with temperature

For ACCURATE 2M, an extended temperature cycling from −10°C to 50°C was performed to cover the radiation monitoring system specification. A current of −50 fA was injected. The measurements were conducted sequentially by injecting first to channel 1 and then to channel 2. The currents measured in this scenario are plotted in Fig. 7.19. The ratio between the currents measured by both the channels is also shown in the graph. It can be observed that the ratio also does not remain constant and varies between 1.3 to 1 in the measured temperature range. Thus, a direct compensation of the leakage current measurement with the channel is not possible and the temperature information is additionally needed to compensate the measurement of channel 1.

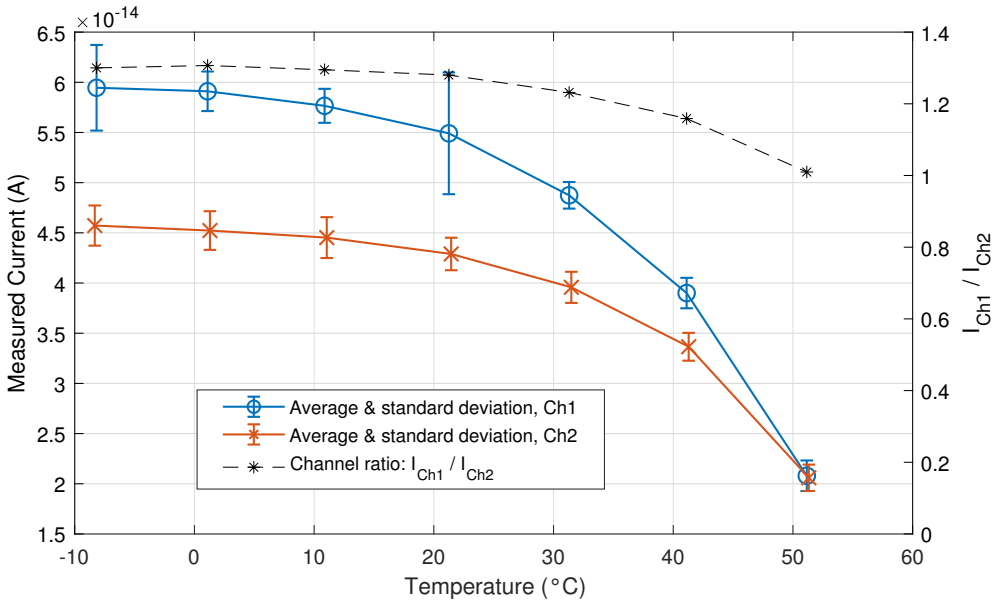


Figure 7.19: Current measured by two channels of ACCURATE 2M for temperatures from −10°C to 50°C with an input current of −50 fA

It can be seen that the currents follow an exponential relationship with temperature. Since the leakage current is caused primarily by the ESD diodes, the observed output reflects the behavior of diode leakage. The ASIC uses a simple ESD structure with two diodes connected back to back between the supply and ground. The leakage currents of the ESD diodes were simulated and the result obtained is shown in Fig. 7.20. The currents plotted are obtained after subtracting ±3.3 pA, which was the current observed at −20°C from the diodes. The diodes A and B had complementary leakages and in the ideal case, as depicted in the simulation, shows that the net leakage from the ESD pad is zero. However, in reality, there is a mismatch between the leakage current of both the diodes, which appears as the input leakage current for the ASIC. From the Fig. 7.19 it can be seen that the net leakage varies between two different pads.

The current measured by the two channels after subtracting the injected current is shown in Fig. 7.21. The net leakage with varying temperature T can be expressed using the equations

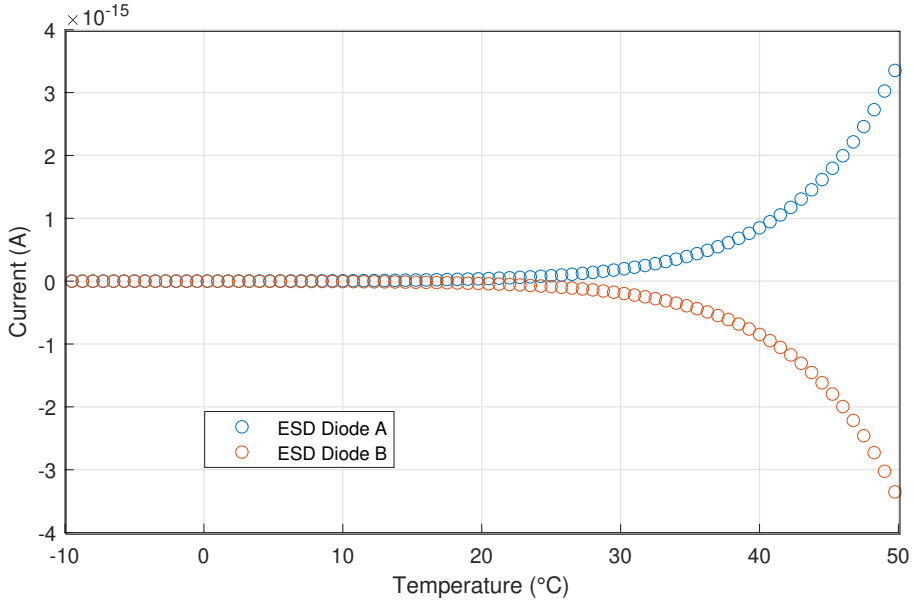


Figure 7.20: Simulated leakage currents of ESD diodes

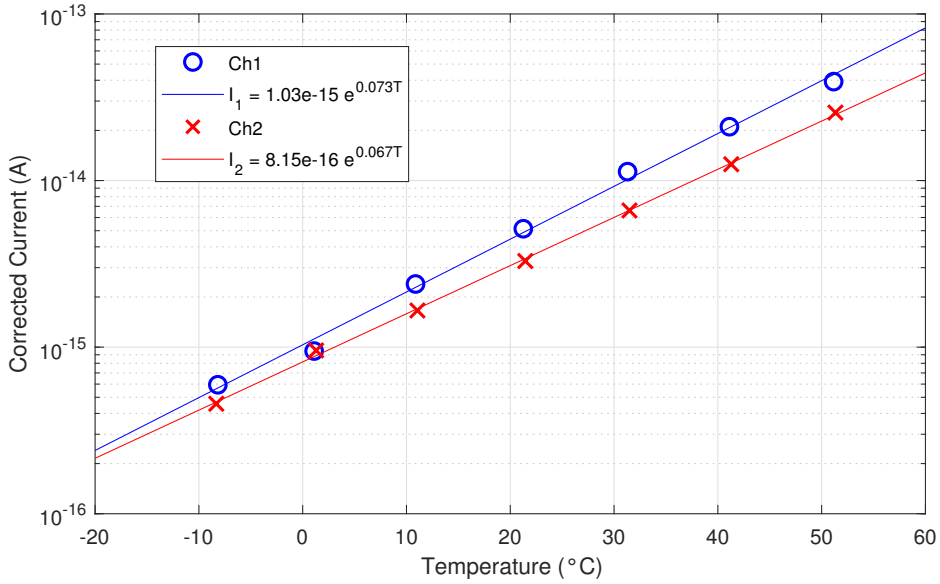


Figure 7.21: Variation of net leakage measured by two channels of ACCURATE 2M with temperature

$$I_{\text{ch1}} = 1.03e^{0.073T}\ fA, \tag{7.1}$$

$$I_{\text{ch2}} = 0.815e^{0.067T}\ fA. \tag{7.2}$$

As it was concluded that the net leakage varies with process variations and temperature, simple leakage compensation by subtracting the current measured by the secondary channel is not feasible. A combination of the two methods mentioned, where the leakage profile for each ASIC is determined by a temperature cycling followed by compensation with the current measured

by the secondary channel, has to be adopted. This thus remains the main challenge in achieving femtoampere sensitivity across different temperatures.

7.4.2 Temperature dependency for the DSM method

The current calculation with the direct slope measurement method is influenced by the variation in the feedback resistor values, comparator offset voltage, effective switching thresholds, and various delays. To determine experimentally the cumulative effect of all the variations on the current measurement, an input current of -100 nA was injected and the temperature was changed from $-20°$C to 55°C. The fluctuation in the interval count was less than 5%. The corresponding current measurement and the errors in comparison with the injected current are shown in Fig. 7.22. The average current in a window of 10000 samples is shown along with the spread of the values in each window. Although the variation within a window is wide, the magnitude of the variation is fairly constant across the temperature.

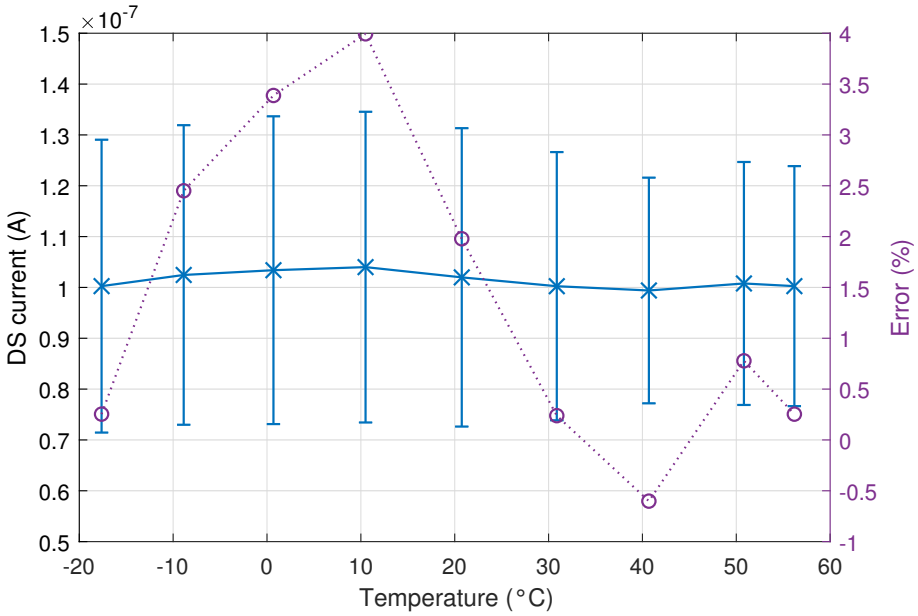


Figure 7.22: Variation of current measurement accuracy of DS method with temperature

7.4.3 Stability analysis of the charge quantum

The accuracy of the current measurement with the charge balancing method depends on the stability of the charge quantum that is subtracted in each charge injection cycle. The reference voltage to which the charge generating capacitor is connected and the capacitor itself determines the values of the total charge. The charges generated by the switches during the transition also makes a very small contribution to the net charge. The equivalent charge is determined by calibration by sweeping different currents. If the calibrated charge remains constant, then the accuracy of the measurement is conserved.

To determine the variation in the charge, a fixed current was injected and the number of charge injections in each measurement window of 100 ms is recorded by the chip. Hence, the charge quantum can be calculated. The average values of the charge quantum thus calculated among every 10000 samples for different temperatures are plotted in Fig. 7.23. The standard deviations in each sample window are also shown.

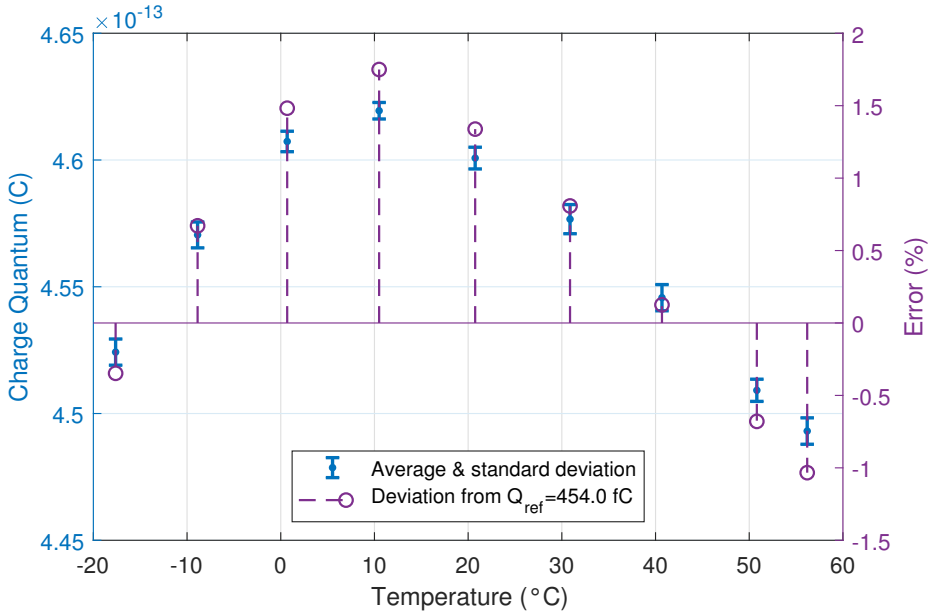


Figure 7.23: Variation in charge quantum with temperature

The calculated average charges are compared against the calibrated charge and the errors observed are less than $\pm 2\%$. The procedure was repeated for different currents and the variation was found to be the same. Thus, it was determined that, even though the absolute value of the charge quantum varies with temperature, the variation is within an acceptable range.

7.5 Conclusion

This chapter detailed the characterization of the ACCURATE 2 ASICs under different conditions. The performance of the ASICs with radiation sources established that they could be interfaced with different types of ionization chambers used at CERN. Using the three different chambers and using Cs 137 and Co 60 sources, it was demonstrated that the ACCURATE 2 ASICs can measure dose rates from 5 µSv/h to 7.4 Sv/h.

To complement the static characterization with radiation sources, dynamic characterization with pulsed radiation was also performed. It was found that ACCURATE 2 can measure charge with increased accuracy compared to its predecessor UTOPIA 2. The improvement of 16% achieved could be mainly attributed to the architectural modifications of larger feedback capacitor and higher charge generation blocks. However, the measurement capabilities have to be increased further for the next version of the ASIC. The use of an input resistor to increase the collection

efficiency was demonstrated. The maximum error observed for charge collection up to 260 nC was less than 10% in this modified configuration. Alternate solutions by increasing the feedback capacitance and bias current of the OTA and interfacing multiple ASICs were also suggested. The test with pulsed radiation was performed with ACCURATE 2A only as the 40 µs gate length limitation of ACCURATE 2M limits the charge collection capabilities. This has to be fixed in the next version of the ASIC.

The leakage current variation of the ASICs with humidity and temperature was also determined. The importance of hermetic sealing to limit the influence of humidity was ascertained. It was found that the leakage current varies exponentially with temperature as it is dominated by the ESD diodes. The stability of the charge quantum and DSM method with temperature variation was also demonstrated. The maximum error in the charge quantum was less than $\pm 2\%$ and the variation in the DSM current measurement was less than 5%.

Chapter 8

Conclusion and outlook

The thesis presents the design of an ultra-wide dynamic range current digitizer ASIC with better than the state-of-the-art sensitivity. The designed ASIC is intended to be used as the front end of ionization chambers for radiation monitoring at CERN. The summary of the accelerator complex at CERN generating various kinds of radiation and the need for radiation monitoring in such an environment presented in the first chapter established the basis for the design of such an ASIC. The various legacy radiation monitors presented in the second chapter reveals the complexity of the systems and the difficulty in maintaining and upgrading such systems based on discrete components. An in-house developed ASIC solution simplifies the process and hence justifies the replacement of these systems with a single chip solution for future radiation monitors.

UTOPIA 2, the predecessor of the ACCURATE family of ASICs, was characterized with continuous and pulsed input currents. The dynamic characterization of the ASIC revealed the need for an upgrade of the analog front end. Integrating the analog and digital blocks into a single ASIC to remove the dependency on an external FPGA was another motivation for the upgrade. Various technologies were considered for designing the next version of UTOPIA. Also, a detailed literature review was performed to determine possible architectural upgrades.

The design of the ACCURATE family of ASICs started with a test structure in the GF22FDX technology. The ASIC developed, called ACCURATE 0, established methods to achieve femtoampere sensitivity in advanced technology nodes. The ASIC could measure currents from -1 fA to -1 nA. The leakage current of the front end was evaluated to be around -240 fA.

The second series of ACCURATE ASICs, named ACCURATE 1, was designed in the TSMC 130 nm technology. Five variants of ACCURATE 1 compared different low current measurement architectures and ascertained the applicability of the 130 nm technology node for femtoampere sensitive current measurements. Reset counting and charge balancing based current to frequency conversion and direct slope measurement methods were the topologies evaluated. It was found that all three methods had comparable performance in the femtoampere measurement region. The direct slope method was the fastest among the three. The charge balancing method had the best dynamic range. The charge balancing version had an average leakage current of

−10 fA. The ASIC demonstrated good linearity from −1 fA to −1 µA with the maximum error in measurement less than 7%.

Based on the insights from ACCURATE 1, the next version was designed. ACCURATE 2 has two variants – an analog-only version and a mixed-signal version. The analog front end combines the direct slope measurement method and the charge balancing method to achieve an ultra-wide dynamic range spanning from −6 fA to −20 µA. The performance of the ASIC in comparison with ultra-low current measurement ASICs reported in the literature is summarized in Table 8.1. It could be seen that the demonstrated minimum current resolution of 200 aA is the best achieved so far. Various techniques that helped in achieving this performance were elaborated in the thesis. The demonstration of achieving sub-femtoampere sensitivity in the technology node of 130 nm opens avenues for using advanced technology nodes for such applications.

Table 8.1: Comparison with the state of the art

Year	**Minimum Current Resolution**	**Maximum Measurable Current**	**Methodology**	**Technology Node**	**Ref.**
2013	550 aA	30 nA	Current Amplifier	350 nm	[44]
2015	314 fA	250 µA	Sigma Delta ADC	180 nm	[45]
2016	100 fA	16 µA	Sigma Delta ADC	500 nm	[46]
2017	1 fA	5 µA	Charge Balancing CFC	350 nm	[21]
2017	470 fA	20 µA	SAR ADC	350 nm	[47]
2018	80 pA	12 µA	Charge Balancing CFC	350 nm	[48]
2021	1 fA	1 µA	Charge Balancing CFC	130 nm	[71]
2021	200 aA	20 µA	Charge Balancing CFC + Direct Slope	130 nm	This Work

ACCURATE 2M, which combines the analog and digital sections, also achieves the same performance. Careful floor planning by isolating substrate the sensitive analog nodes with Deep N-Well structures and guard rings helped in limiting the substrate noise from the digital section affecting the current measurement. The details of the mixed signal design and various factors considered in the design of the test board used for characterizing the ACCURATE 2 ASICs were also explained. It was found that leakage current in the same technology nodes varies from fab to fab. The ACCURATE 1 series of ASICs fabricated in 12-inch wafer fab reported a leakage of around −10 fA while the ACCURATE 2 ASICs had a leakage of around +6 fA at 25°C.

The variation of the leakage currents with temperature and humidity was experimentally determined. It was found that, in the presence of a high humidity of more than 40% RH, the leakage current profile strongly followed the humidity variation. The ASIC was bonded directly on the PCB and hence was not hermetically sealed and was hence profoundly influenced by humidity variations. Using a climatic chamber with controlled humidity, the temperature was varied from −20°C to 55°C and various parameters were measured. The leakage current profile was found to follow a typical exponential diode current profile. Thus, the leakage current remained fairly constant for sub-zero temperatures and increased significantly as the

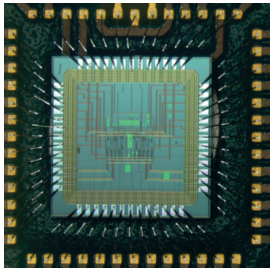
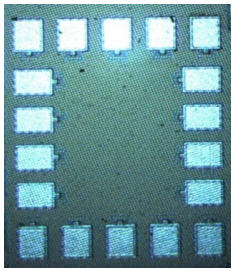
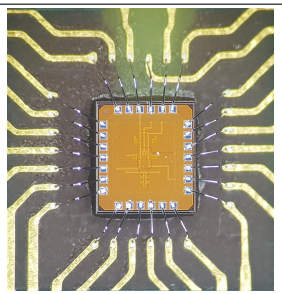
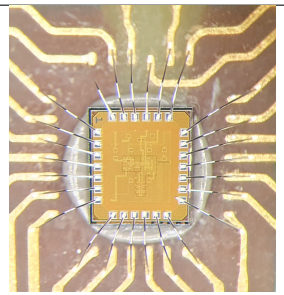
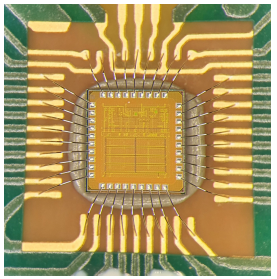
temperature reached room temperature. The balance of the leakage currents between the two channels of the ASIC was determined. It was found that the ratio of the leakage also changed with temperature. Hence, a direct compensation of the leakage current of the primary channel with that of the secondary channel was not feasible. To effectively compensate for variations in leakage current, each ASIC has to be characterized to determine the correction factors and then, based on the current measured by the secondary channel, the correction can be applied.

The accuracy of the charge balancing method, which is one of the methods used for current measurement in ACCURATE 2, depends on the stability of the charge quantum that gets subtracted in each operation cycle. Hence, the variation of this factor with temperature was studied. It was found that the charge remains fairly constant with variations of less than 3%. The variation of the leakage of various switches in the charge generation block results in this fluctuation. The accuracy of the direct slope measurement method with temperature was also studied and the variation was contained within 5%.

Apart from demonstrating the linearity with current sources, the ACCURATE 2 ASICs were extensively characterized in different application scenarios. Measurements with radioactive sources were performed at the calibration laboratory at CERN. Using the Cesium 137 and Cobalt 60 sources, dose rates from around 5 µSv/h to 7.4 Sv/h were generated. The dose rates were converted to currents by three different ionization chambers – IG5 A20, IG32, and PMI T32006. The currents generated by the chambers were measured using ACCURATE 2 and a reference meter. ACCURATE 2 chips were successfully interfaced with these chambers and the measured current matched well with that measured by the reference. Dynamic characterization of the ASIC was performed at the PSAIF at CERN. The facility allows exposure to pulsed radiation of 500 ns pulse width with a repetition rate close to 2 minutes. The strength of the radiation could be adjusted by varying the position of an ionization chamber within the facility. Charges measured by ACCURATE 2 and UTOPIA 2 were recorded for different dose rates and compared to that measured by a reference electrometer. It was demonstrated that ACCURATE 2 was able to collect a significantly higher amount of charge compared to UTOPIA 2, especially at charges per pulse higher than 100 nC. However, it was observed that there is room for improvement. The direction to follow to increase the charge collection efficiency further was also discussed.

The summary of all the ASICs designed in this research and the comparison with their predecessor -UTOPIA 2 is shown in the table.8.2.

Table 8.2: Comparison of different ASICs designed in this research with UTOPIA 2

ASICs	**UTOPIA 2**	**ACCURATE 0**	**ACCURATE 1**	**ACCURATE 2A**	**ACCURATE 2M**
Micrograph					
Year	2016	2018	2019	2021	2021
Technology node	AMS 350 nm	GF 22 nm	TSMC 130 nm	TSMC 130 nm	TSMC 130 nm
Minimum current	-1 fA	-1 fA	-1 fA	-6 fA	-7 fA
Minimum current resolution	1 fA	1 fA	1 fA	200 aA	200 aA
Maximum current	-5 µA	-1 nA	-1 µA	-20 µA	-20 µA
Feedback capacitance	1 pF	0.5 pF	1 pF	5 pF	5 pF
Area	7.56 mm^2	0.33 mm^2	1.95 mm^2	1.95 mm^2	3.52 mm^2
Power supply	3.3 V	1.2 V	3.3 V	3.3 V	3.3 V ,1.2 V
Leakage current	-50 fA	-240 fA	-10 fA	+6 fA	+7 fA
Number of channels	2	3	1	1	2
Percentage of charge collected for 100 nC pulse	45%	-	-	61% , 95% with 50 MΩ input resistor	-
Primary objective	Current digitiser	Technology Evaluation	Architectural comparisons, Technology evaluation	Current digitiser	Mixed signal current digitiser

The various activities planned and the path towards ACCURATE 3 are explained further.

1. Integration with CROME

   A project in the pipeline is the development of CROME+ where the next version of the radiation monitoring system will be developed by combining ACCURATE 2 and CROME. The IVC, which handles the current to frequency conversion on CROME, will be replaced with ACCURATE 2. The high voltage generation section and interface to supervision on CROME will be used to develop a full radiation monitoring system. An experimental project where the output of multiple ACCURATE 2 ASICs will be combined in the FPGA on CROME to develop a radiation monitoring module to be installed near the accelerator complex is in progress.

2. Modification to include the measurement of positive currents

   ACCURATE 3 will include a measurement path for positive input current for both the primary and the secondary channels. The architectural modification is minor and involves adding additional comparators with threshold voltage connected to the inverting terminal. Since the leakage current measurement is performed with the direct slope method, the charge generation block does not need to be reconfigured.

3. Internal DACs and bandgap reference voltage blocks

   The different reference voltages for the ASIC are now generated externally by DACs on the test board. The fixed voltages, such as the bias voltages for the OTA and the comparator, have to be generated using bandgap reference circuits. The tunable voltages, such as the threshold voltages, have to be generated using internal DAC modules. These modules need to be designed to make the ASIC more standalone.

4. Digital section with scan chain

   The ASIC developed has to be evolved from a prototype to a more standalone system. Various aspects concerning design for testability by inserting a scan chain and test pads have to be incorporated.

5. Packaging

   The ASIC has to be hermetically sealed to minimize the impact of humidity. The effect of different kinds of packaging on the leakage current performance has to be studied. Studies have been initiated and steps to launch a flip-chip packing and bonding of the chip to minimize the pad length are under investigation.

6. Study with different PCB material

   The test board used for characterizing the ASICs were designed with FR4 material. Ceramic composites, such as Rogers, are reported to have lower leakage compared to FR4 and are hence reported to be used in designing femtoampere sensitive circuits [95], [96]. The

extent of improvement achievable with the current architecture and environment has to be experimentally determined.

7. Reliability studies and EMC analysis

   Evolving the ASIC to be a qualified product to be installed for operation means it has to undergo different analyses such as EMC and reliability. The safety-critical radiation monitors installed at CERN need to be compliant to Safety Integrity Level 2 (SIL2). A similar analysis as carried out for CROME [97] has to be done for ACCURATE to determine the SIL. Various factors have been considered while designing the ASIC to minimize the EMC issues. However, detailed analysis and testing have to be done further to assess the EMI and EMC aspects of the ASIC.

8. Radiation hardening

   The studies for upgrading the LHC with a new tunnel of around 100 KM aiming to increase the energy from currently achieved 13 TeV to 100 TeV are progressing [98]. The new Future Circular Collider (FCC) brings with it new promises and challenges. The current requirement for radiation monitoring electronics does not mandate radiation hardness. The main reason is that the radiation protection radiation monitors are either installed in low radiation areas or are connected with cables to ionization chambers which are in high radiation areas. The installation of long cables to bring the signals of the ionization chambers to radiation safe areas might not be feasible with the future collider project. Hence, discussions are ongoing to assess the feasibility of upgrading the system to make the ASIC radiation hard. This was also a deciding factor in making the ACCURATE design with the TSMC 130 nm technology, which is already proven to be effective for radiation hard designs. The different steps to upgrade the ASIC have to be analyzed.

The research for designing ACCURATE 3 will continue through the steps listed above. The ASIC will act as the strong pillar supporting the future radiation monitoring at CERN, thus safeguarding the personnel by ensuring a safe and secure working environment for the countless innovations and discoveries to be made at this wonderful scientific laboratory.

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