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# Development of the front end amplifier circuit for the ATLAS ITk silicon strip detector

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Abstract: We present the development of the front end amplifier circuit for the ABCStar readout ASIC designed for the upgraded ATLAS Inner Tracker (ITk) detector. The amplifier is intended to work with silicon strip sensors of moderate length between 1.9 cm and 5.5 cm dependent on position in the detector. The final circuit is implemented in a commercial 130 nm CMOS process tolerant up to the total ionizing doses (TID) predicted for the lifetime of the detector, that is maximum of 66 Mrad (660 kGy) (Si) for the endcap region. The final architecture and the performance of the circuit is presented in the context of a long development program which started soon after the construction of the present ATLAS Semi-Conductor Tracker (SCT) detector.

Keywords: Front-end electronics for detector readout; Particle tracking detectors (Solid-state detectors); Si microstrip and pad detectors

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## Contents



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## 1 Introduction

The work on the development of the front end electronics for the ATLAS Semi-Conductor Tracker (SCT) detector upgrade was launched after the construction of the present detector. The fast front end amplifier implemented in the IBM 250 nm process [1] has been successfully applied in the ABCN-25 front end chip [2]. Although it was clear from the beginning that this technology is not ideal from the point of view of power consumption and feature size, the latter allowing a rather low 42 μm channel pitch, the ABCN-25 chip allowed for a long and intense module development program [3].

A logical continuation of the work in quarter micron technology was the exploitation of the 130 nm CMOS process which became available at CERN in 2007. It offered a factor of two increase in transconductance parameter (increase of $K_a$ from 330 to 720 μS for NMOS) and a significant increase in transit frequency (increase of $f_t$ from 35 to 94 GHz) allowing for better noise and power optimization as well as improved Power Supply Rejection Ratio (PSRR), the latter imposed by higher bandwidth of the input stage.

In order to maintain a high open loop gain of the input stage in the presence of the degradation of intrinsic transistor gain and to cope with the lower supply voltage (changed from 2.5 V to 1.2 V) keeping at the same time a high dynamic range in the shaper, a new architecture of the building block amplifiers had to be developed. The design and the performance of the front end amplifier used later in the ABC130 chip ([4, 5] and [6]) has been described in detail in [7].

Although the noise performance and power consumption of the front end channel had been satisfactory at the moment of the design, the final change in the specification for the sensors intended for the ATLAS upgrade (change from $p^+$ on n to $n^+$ on p) as well as unexpected degradation of the noise performance after irradiation forced major modification of the front end architecture.

The input stage of the ABC130 front end (see [7]) employs an active feedback built with PMOS transistor biased in the saturation region with relatively low, 300 nA, current. For the positive signals, as arises from $p^+$ on n sensors, the parallel noise contributed by the feedback transistor depends only on its transconductance, stabilised with the bias current. For the negative signal, as arises from $n^+$ on p sensor, the input current modulates the transconductance of the feedback transistor causing degradation of the noise as well as the gain of that stage. The comparison of the noise performance of the ABC130 prototype front end channel for positive and negative input signals is presented in figure 1. As it will be shown later in this paper, the active feedback architecture has been changed in the ABCStar front end to resistive feedback, which has an additional implication on the architecture of the following stages, but it has solved the problem of the response to the negative signals.

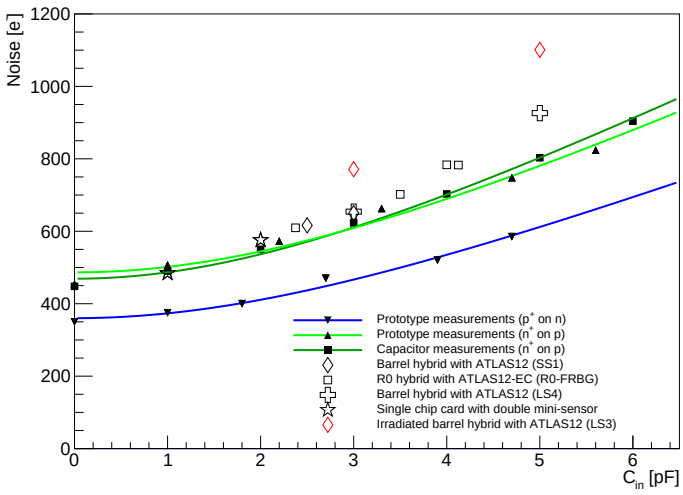


**Figure 1.** Equivalent Noise Charge of the ABC130 front end prototype for positive and negative input signals as a function of the input capacitance.

The evolution of the equivalent noise charge (ENC) as a function of total ionizing dose (TID) of the unloaded ABC130 channel for various irradiation conditions and rates is shown in figure 2. For the low dose rate and low temperature, up to a 50% degradation of the equivalent noise charge was measured.

Similar degradation was seen in irradiated modules built with the ABC130 chip (see red diamonds in figure 1), i.e. for the front end input loaded with the capacitance. This has indicated that the increase of the noise can be attributed to the series noise contributed by the input transistor. A similar, but less significant degradation (up to 20%), was observed on a very similar front end ([8]) implemented in the same technology but with faster shaper (peaking time around 10 ns). The latter observation implies that the noise degradation can be attributed to the increase of the flicker noise in the regular NMOS transistor used at the ABC130 preamplifier input. Indeed, later work presented



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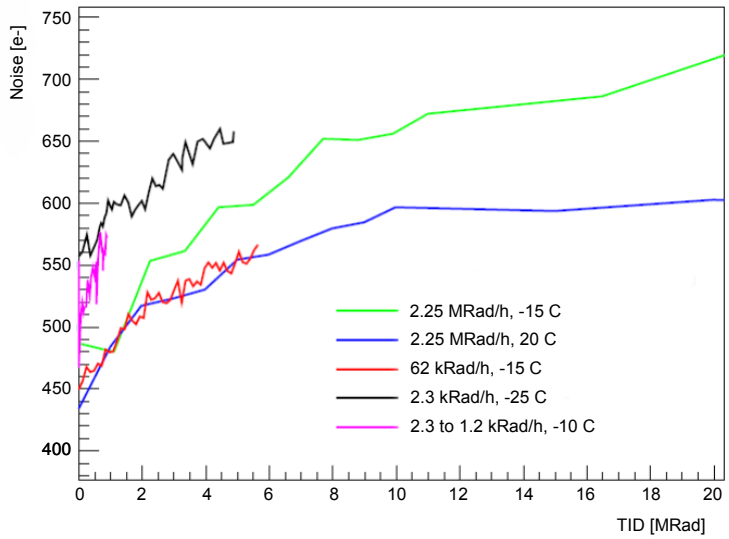


**Figure 2.** Equivalent Noise Charge evolution as a function of TID for various temperature and dose rate for the ABC130 front end not loaded with the input capacitance.

in [9] confirmed the sensitivity of the regular layout NMOS transistors to ionizing radiation. The reported degradation of the flicker noise coefficients was specially pronounced in the weak and moderate inversion region i.e. the typical operating point of the transistors in low noise, low power amplifiers designed for silicon strip sensors. The hypothesis that the increase of the flicker noise is related rather to the edge effect associated with the shallow trench isolation (STI) of the regular layout transistor and not to the gate oxide has been confirmed later in [10], where it has been shown that the noise spectra of the irradiated NMOS transistor designed with enclosed layout geometry are the same as before irradiation. Therefore, all NMOS transistors in the ABCStar front end input stage are designed in the edge-less configuration.

## 2 Testing the ABCStar

### 2.1 Testing setups

Initial functionality tests and characterisation of the ABCStar prototype ASIC were performed on single chip boards (SCBs) which allow both capacitive loading of single channels using discrete surface mount components and also the connection of small 100 channel strip sensor prototypes. Readout of the chips on these SCBs was performed via a commercial FPGA development board with a custom FMC-based readout board, the FMC-1701. The FMC-1701 performs high speed data buffering for chip differential inputs and outputs and includes commercial ADCs and DACs to measure chip voltages and provide calibration voltages for the internal ABCStar ADC. FMC-1701 also provides temperature monitoring of the ASIC via an NTC on the single chip board and monitoring of voltage and current of the digital and analogue power rails. Connection between FMC-1701 and SCB is performed using 0.05 inch pitch ribbon cables. An example of an SCB and the FMC-1701 are shown in figure 3.



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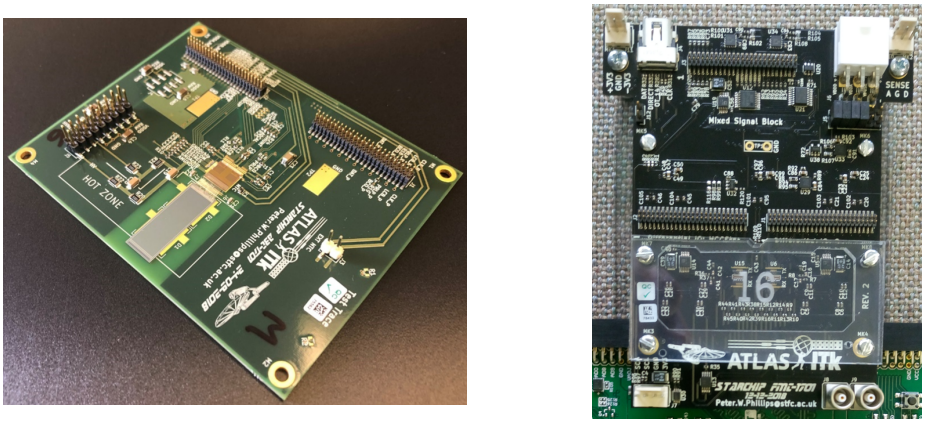


**(a)** Single chip board

**(b)** FMC-1701

**Figure 3.** A single chip board housing a single ABCStar connected to a 2.5 cm long prototype strip sensor and the custom FMC-1701 board used to test single chips.

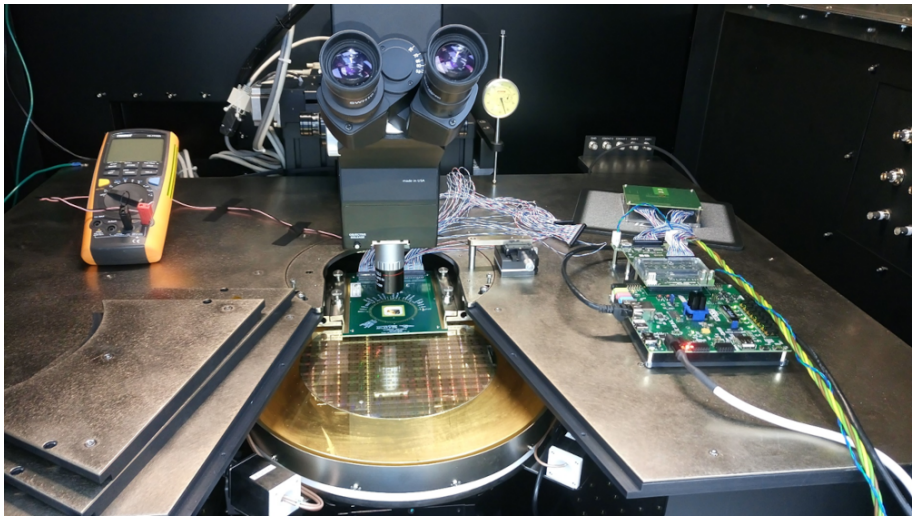

**Figure 4.** The wafer probing setup used in the further characterisation and testing of the ABCStar ASIC.

Once the chip was demonstrated to work, wafer probing was carried out using the same readout system as used for SCB testing as can be seen in figure 4. Furthermore, inner barrel (short-strip), outer barrel (long-strip) and inner end-cap (R0) modules were built using the prototype ABCStar ASIC. These were tested using a second custom FMC-based board, the FMC-0514-DP, an evolution of FMC-1701 designed for multi-module testing via mini-DisplayPort connectors and cables instead of 0.05" ribbons. These modules and readout board can be seen in figure 5. Short-strip modules have a strip length of 24 mm corresponding to a load of approximately 2.5 pF, long-strip modules have 48 mm strips (5 pF) and R0 modules have a range of strip lengths from 19–32 mm (2–3 pF).

Having characterised the chip before irradiation, SCBs were irradiated using a 3kV tungsten x-ray tube. Dose and dose rate were calibrated using a 1mm silicon diode. A beamspot was chosen to provide a mean dose rate of 0.7 Mrad/hr over the full ABCStar ASIC with 15% uniformity as shown in figure 6. The chip was powered and clocked during irradiation and the irradiation was



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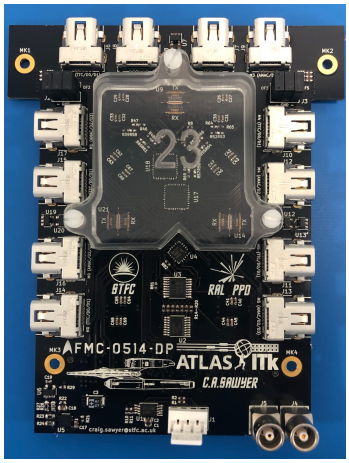
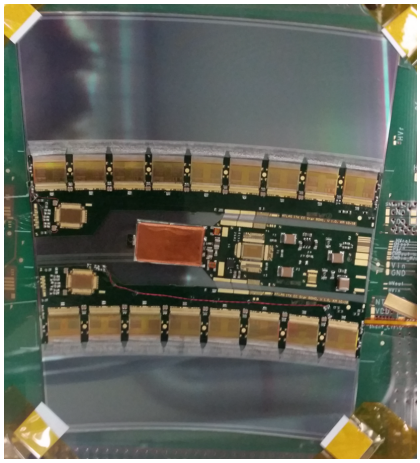
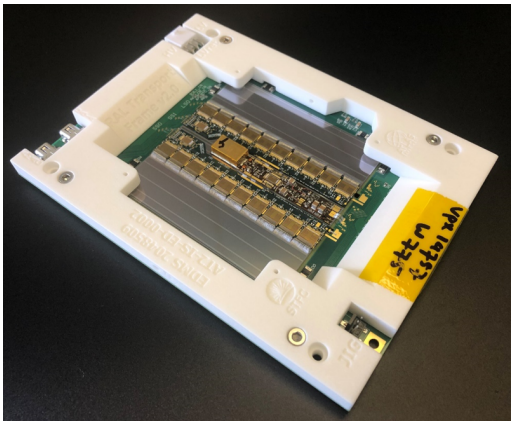


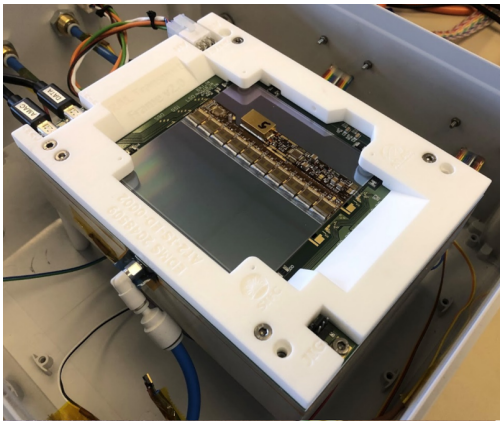

**(a)** FMC-0514-DP



**(b)** Prototype R0 module



**(c)** Prototype short-strip module



**(d)** Prototype long-strip module

**Figure 5.** The prototype modules and readout board used to complete the characterisation of the ABCStar prototype ASIC.

paused every 30 minutes for the chip performance to be characterised as a function of total ionising dose (TID). This was continued up to a total delivered dose of 80 Mrad.

### 2.2 Testing methodology

Figure 7 shows a block diagram of the ABCStar calibration scheme. The characterisation of the ABCStar has primarily been carried out using the internal charge injection circuitry. The calibration circuit is based on a 9-bit DAC supplying a DC current to the resistor which is short circuited by an NMOS switch controlled by the strobe signal. The calibration charge is injected to the front end amplifier input through on-chip, per channel calibration capacitors (Cc in the diagram). The default timing (strobe delay) between charge injection and readout is varied using the in-built 6-bit delay line which is applied to the generation of the charge injection pulse. The DC amplitude of the calibration DAC can by measured through the internal test multiplexer (monitoring ADC). Therefore the absolute value of the calibration charge depends directly on the accuracy of the metal-oxide-metal (MIM) capacitor value. The maximum tolerance of the MIM capacitor during



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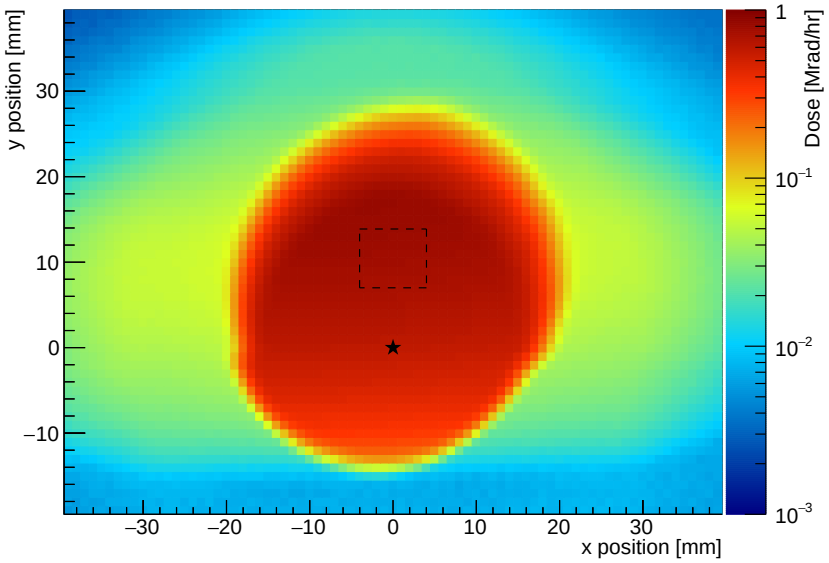


**Figure 6.** Measured beamspot from the tungsten x-ray tube at a distance of 20 cm. The measurement was performed using a 1 mm silicon diode previously calibrated at CERN. Also shown is the position of the alignment laser (star marker) and the position at which the chip is placed (dashed box).

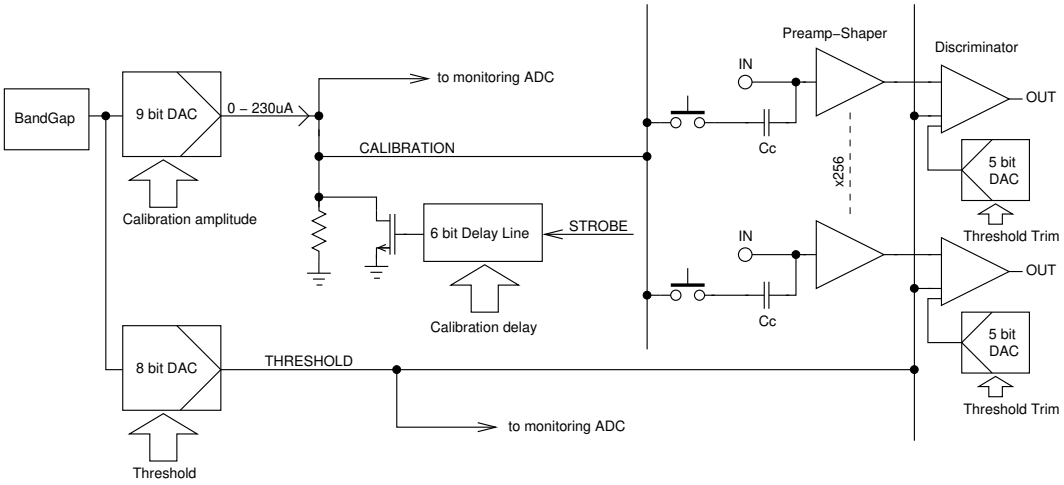


**Figure 7.** Block diagram of the ABCStar calibration scheme. The DACs used for setting calibration amplitude, threshold and channel-by-channel threshold trim are shown along with the delay line on the calibration pulse signal (strobe).

the production is guaranteed by the foundry to be below 10% (3 sigma distribution). In practice (engineering runs of ABC130 and one engineering run of the ABCStar chip) this tolerance was within 5% which has been verified through process control monitor (PCM) data provided by the foundry. The matching of the MIM capacitors of the sizes used in the ABCStar across the channels is around 0.8% (3 sigma distribution). To investigate the strobe delay, approximately 4 fC of charge is injected with the threshold set to 2 fC equivalent via the 8-bit threshold DAC.



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Initially noise and gain have been investigated as a function of strobe delay with the default timing being set based on the delay for which maximum gain is measured. This is found to be 57% of the way across the window in which the charge is seen, as measured from the rising edge. In later measurements, strobe delay is set based on the 57% point of the window rather than directly finding the setting which gives maximum gain.

Gain and noise are extracted from threshold scan measurements at three different charges, 0.5, 1.0 and 1.5 fC. Each threshold scan is fitted with a complimentary error function (S-curve) from which the median and width can be extracted. The gain is extracted from the dependence of the median (vt50) on the injected charge whilst the noise is extracted from the width of the fitted S-curves. All threshold scans are performed in DAC counts which are then calibrated to mV using results from simulations which can be cross checked using the on-chip ADC or the external ADC on the FMC-1701. An extension of this measurement is that of a full response curve which uses ten different injected charges from 0 to 6 fC. An example of such a response curve is shown in figure 8.

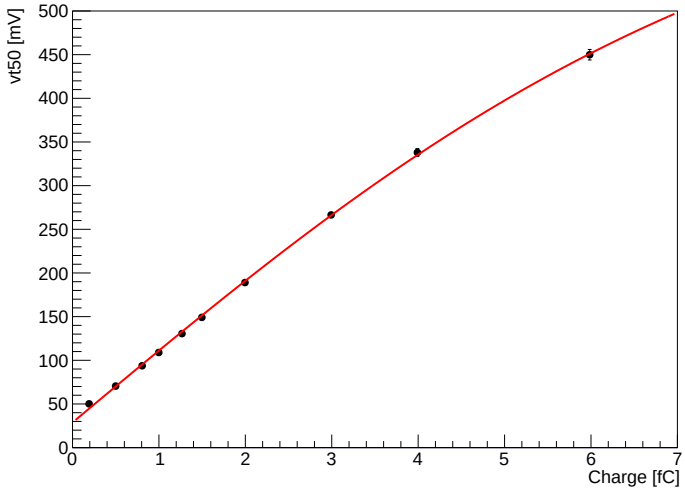


**Figure 8.** vt50 versus injected charge for an ABCStar ASIC. The average vt50 across 128 channels of a single chip is shown whilst the error bars show the RMS of the channel-by-channel variation. Non-linearity at higher values is caused by the change in the operating point of the devices used in the DAC output current source. The data is fitted with an empirical fit function, $A + B/(1 + e^{-x/C})$.

Response variations across the chip are reduced (trimmed) via channel-by-channel configuration of the offset applied to the chip pedestal using a 5-bit threshold trim DAC per channel. This is derived by scanning the trim DAC settings with no injected charge. Trim DAC settings for each channel are selected such that the channel-by-channel response (without injected charge) is as close to uniform as possible.

Finally, the timing variation of the front-end as a function of injected charge (time-walk) is measured by scanning the strobe delay for different injection charges for a fixed threshold. Calibration between strobe delay DAC units and nanoseconds is performed by taking the width of the timing window from a strobe delay scan and scaling this to a 25 ns readout window. For these measurements, the expected end-of-life threshold of 0.5 fC is chosen, driven by the expected noise



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performance of the final system. The time-walk is measured from 0.75 fC as this is the lowest expected charge injection, given the expected charge collection of sensors at end-of-life [16] and assuming the worst case charge sharing of 50% across neighbouring channels.

## 3 The ABCStar front end channel

The predicted detector occupancy at the upgraded LHC has defined the granularity of the sensor i.e. the length of the detector strip and the number of channels implemented on the front end readout chip. The ABCStar ASIC comprises 256 readout channels and to cope with this requirement the single channel has been laid out with relatively narrow, 22 µm, pitch.The input stage of the ABCStar front end channel is optimized for the relatively short silicon strips ranging from 1.8 to 5.5 cm length (various geometry for end cap and barrel regions) equivalent to between 2 and 7 pF total load capacitance including parasitic capacitance related to the assembly. Radiation damage, which is the primary source of signal degradation, is generally higher for the innermost layers requiring more segmented and smaller sensors at lower radii. Consequently the affordable noise levels for the outer sensors with larger parasitic capacitance can be higher than for the inner layers. This facilitates the noise and power optimization of the input stage which can be biased at the fixed input transistor current allowing for slightly higher noise for longer strip sensors. For example, the maximum ENC for long barrel strips (4.8 cm long equivalent to 6 pF load) is specified as 1050 $e^-$ ENC, whilst the acceptable levels for the short barrel strips (2.4 cm strips equivalent to 3.5 pF load) should be below 750 $e^-$ ENC.

Limiting the current and power delivered to the front end circuit is important for two reasons. First is in order to optimise the cooling system which is mandatory to keep the whole detector at negative temperatures to minimize radiation damage. Second, is the minimisation of the cross-sections of the supply cables. Both components directly influence the total material installed inside the tracker. The constraints set by the design of the detector module and stave specified the maximum current consumed by the analogue part of the chip to be below 70 mA. This gives around 260 µA current budget per channel taking also into account power spent in the common analogue blocks like bias generator, voltage regulator, threshold and calibration circuitry etc.

The schematic diagram of one channel of ABCStar front end is shown in figure 9. Each channel consists of a preamplifier and a booster amplifier, AC coupled to the differential shaper, and a threshold interface connected to the discriminator providing binary information about the particle hit.

### 3.1 The preamplifier

The input stage of the preamplifier is built with a telescopic regulated cascode amplifier with the NMOS input transistor $T_1$ of dimensions 316 µm over 300 nm and total gate capacitance of about 600 fF. The dimension of the input transistor has been optimized for the 6 pF input capacitance equivalent to the load of the 5 cm strip sensor. The input transistor is operating in the moderate inversion region with nominal bias current of 130 µA. The regulated cascode (transistors $T_1$, $T_2$ and $T_3$ in deep NWELL) is loaded with the cascode current source built with the transistors $T_5$ and $T_7$. The extra current source made with the transistors $T_6$ and $T_8$ is driving the transconductance of the input transistor, $T_1$, improving the bandwidth of the input stage. The simulated gain bandwidth



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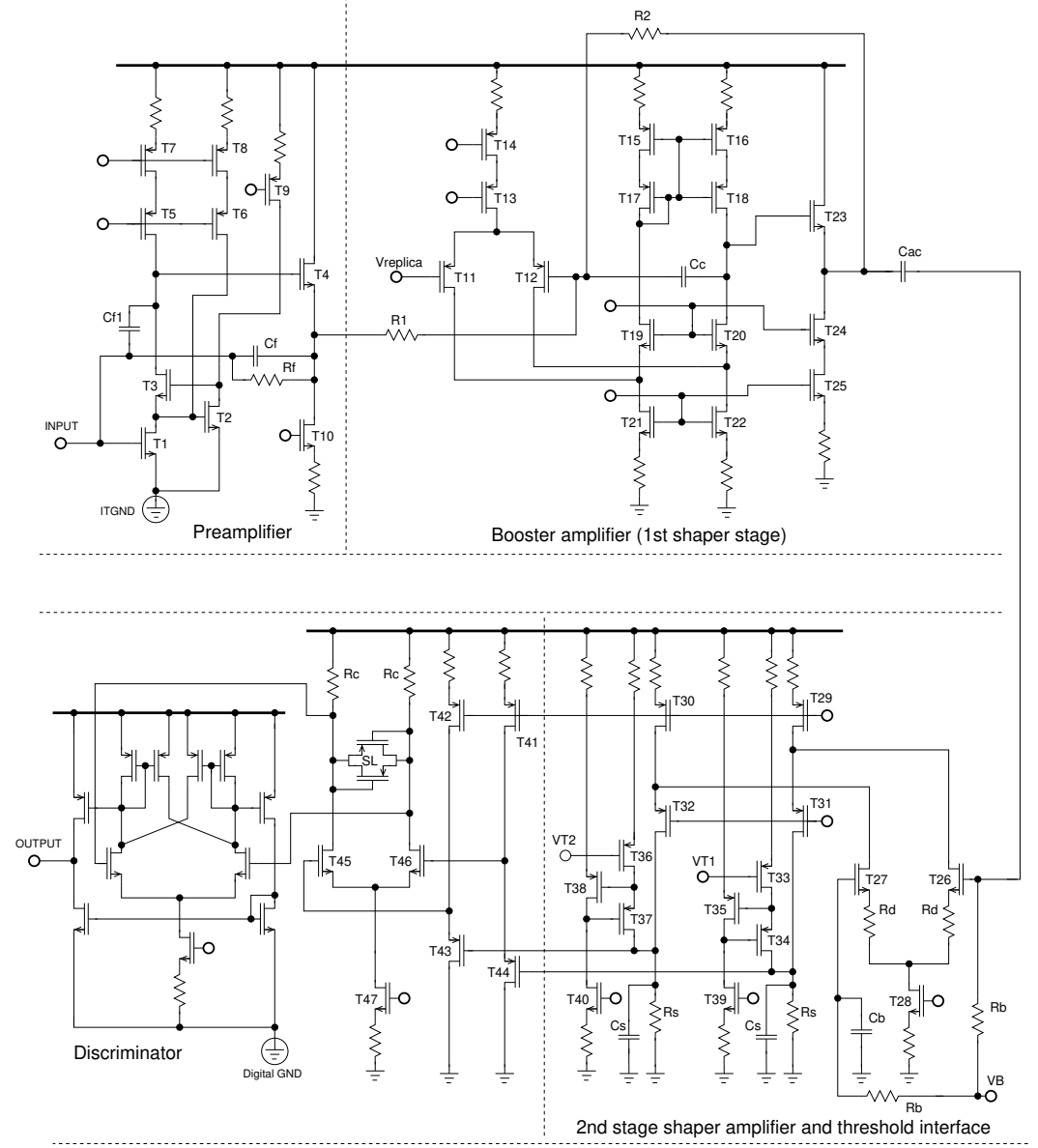


**Figure 9.** Schematic diagram of the ABCStar front end channel. The front end channel is AC coupled to the strip sensor implant.

product (GBP) of the preamplifier post extracted view is around 1.5 GHz. The cascode amplifier is buffered with the source follower built with $T_4$ placed in deep NWELL, which allows for direct source-body connection and prevents the gain loss due to the body effect. The preamplifier works in a transimpedance configuration with resistive and capacitive feedback ($R_f = 105\,\text{k}\Omega$, $C_f = 60\,\text{fF}$). The use of a simple resistor instead of the active feedback used in previous prototypes has solved the problem of the modulation of the feedback impedance by the signal but it has some drawbacks from the point of view of the stabilization of the DC operating point over the PVT (process, voltage and temperature) variation.



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The relatively high variability of the DC voltage at the cascode output (drain of $T_5$) defined by the gate source voltages ($v_{gs}$) of the input and buffer transistors was a primary motivation for the modification of the configuration of the preamplifier load and architecture of the next stage. Because of the new sensor dimensions and relaxed specifications for the open loop gain it was possible to replace the regulated cascode architecture used in the active load of the ABC130 input stage with a low voltage cascode. This has increased the margins for the DC operating point of the input cascode and allowed for stronger resistive degeneration (voltage drop of 130 mV for nominal bias current) and consequently for the minimization of noise contributed by the active load [11]. The open loop gain of the preamplifier for nominal bias condition is about 75 dB (80 dB in ABC130) which, with the GBP of 1.5 GHz, is sufficiently high to keep cross talk signals at a reasonable level (3.3% maximum for the 5 cm sensor). The cascode Miller compensation done by the means of capacitor $C_{f1}$ (68 fF) provides 90° phase margin for the worst case PVT and input load condition. To improve the stability and the robustness of the front end working in multi-channel configuration the sources of the input transistors are connected together (ITGND ground) and referenced externally to the hybrid ground using a separate set of the pads. This avoids the parasitic feedback on possible common bond inductance connecting sensitive reference node of the input cascode which is biased in class A with the circuits behind having much higher current supply swing.

The regulation amplifier, built with transistors $T_2$ and $T_9$, is biased with 8 µA, which provides sufficient margins to neglect its noise contribution (see the detailed noise analysis in [7]).

Another positive effect of the new, resistive, feedback configuration can be observed on the distribution of the front end signal gain. The RMS of the ABCStar gain is better by a factor of two when compare to the ABC130 gain distribution which was affected slightly by the variation of the low, 300 nA, feedback currents distributed across the whole chip area. The comparison of the distributions of the gains for a single ABC130 and ABCStar chips normalized to 1 fC response is shown in figure 10.

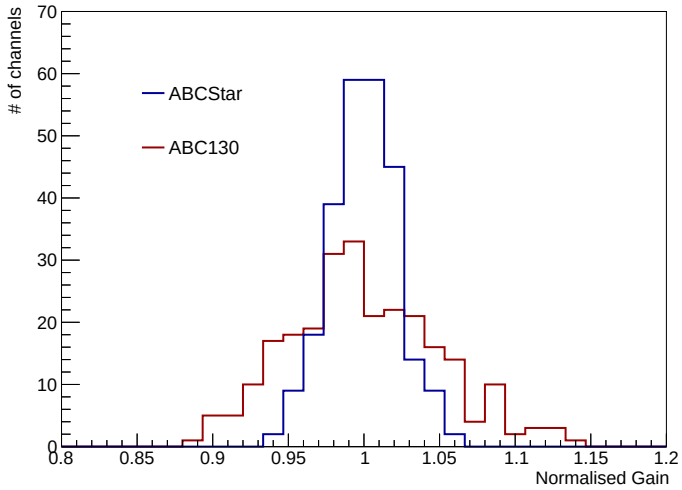


**Figure 10.** The distribution of signal gain in ABC130 and ABCStar front end chips normalized to 1 fC response for a single chip of each type. An rms of 4.9% is measured for ABC130 whilst that for ABCStar is 2.2%.



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As was already mentioned, all NMOS transistors are laid out with enclosed geometry configurations which solves previous problems with the increase of noise after irradiation. The noise evolution of the ABCStar front end is shown in figure 11.

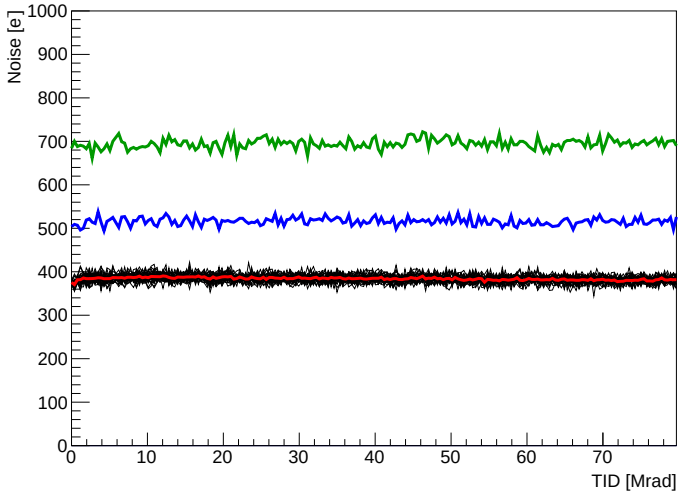


**Figure 11.** The evolution of the noise as a function of TID radiation for ABCStar ASIC. The blue and green channels are respectively connected to 2.5 pF and 4.7 pF external capacitors. The red trace shows the average of 30 unloaded channels which are each individually shown in black.

### 3.2 The booster amplifier

Although the presented front end circuits are designed for tracking detectors where only binary information is needed, some linearity and dynamic range is indispensable in order to evaluate the noise and gain and to calibrate the discriminator threshold for which the system will operate.

On the other hand the analogue gain measured at the discriminator input should be maximized in order to have a good separation between signal and threshold variation as well as to keep the kick back noise and digital interference coming from the digital part of the discriminator at a negligible level. In order to achieve a gain in the range of 80 to 100 mV/fC, which is a reasonable compromise between all requirements, an additional gain stage is needed.

The booster amplifier is designed as a differential input folded cascode amplifier with a source follower buffer built with a zero Vt NMOS transistor ($T_{23}$). The PMOS input transistors ($T_{11}$ and $T_{12}$) and the NMOS cascode transistors ($T_{19}$ and $T_{20}$) are biased nominally with 9 µA each. The overall current consumed by this stage for the nominal bias condition is around 45 µA. The open loop gain is of the order of 48 dB which is sufficiently high to provide good stability in the closed loop configuration defined by the ratio of $R_2$ and $R_1$ resistors (150 kΩ and 15 kΩ respectively). The simulated gain bandwidth product (extracted view) is slightly below 300 MHz which for the closed loop gain of 10 V/V effectively limits the bandwidth down to about 30 MHz and provides the integration of the signal. The peaking time at the booster output is around 13 ns and the signal gain is of about 35 mV/fC.

All current sources are degenerated with the resistors providing voltage drops of the order of 80 mV which improves the matching and reduces its noise contribution to the circuit. The inverting input of the booster amplifier is DC connected to the preamplifier and the $R_1$ resistor loads its output. The 15 kΩ value of this resistor is a trade off between its noise contribution, which is kept below 3% for a 5 cm strip sensor, and the power spent in the preamplifier buffer avoiding the loading effect which could degrade the preamplifier phase margin. The non-inverting input of the booster amplifier is referenced by the voltage generated by the replica of the preamplifier input transistor. Because of the high, 10 V/V, closed loop gain of the booster stage, the offsets propagated from the preamplifier output are amplified significantly. The simulated distribution of the DC offsets at the booster output in one ABCStar chip is in the range of 25 mV rms. This was one of the motivations to use the AC coupling between booster and the shaper stage.

### 3.3 The shaper and threshold interface

Regardless of its simplicity, the binary readout architecture cannot cope with the coupled noise or interference coming from the digital activity of the chip which can affect all channels synchronously. Therefore it is important to keep their amplitude below the level defined by the noise performance of the input stage which should be dominant in a properly behaving front end chain. The interference could be propagated through the power supply lines or global bias and threshold distribution networks. From this point of view a fully differential architecture of the front end channel could be beneficial, however the penalty in the consumed power makes this option unrealizable.

The PSRR for the input stage and booster which are single ended stages, as for any feedback amplifier, can be maintained at an adequate level providing high open loop gain and bandwidth higher than the cutoff frequency of the shaper [12].

A very good PSRR at low and middle frequency range is provided by the AC coupling of the booster and the shaper stage. In order to keep good PSRR over the entire frequency range, the shaper stage is designed in a differential configuration. It is built with a differential folded cascode with NMOS input transistors $T_{26}$ and $T_{27}$, loaded with the resistors $R_S$ which with the capacitors $C_S$ provide the final integration of the signal. The drawback of this solution is that, regardless of the stabilisation by means of the degenerated resistors $R_d$, the gain of the stage is still bias dependent. This is in fact not an issue since all biases are generated and stabilised with the band gap circuit. The advantages of the used architecture is very low power consumption, only 32 µA in the overall stage, and a simple interface for the discriminator threshold providing reasonable linearity. The impact of this stage on the gain of the full channel will be discussed in the following section.

A high impedance, regulated, current source built with the PMOS transistors $T_{33}$ to $T_{35}$ and $T_{36}$ to $T_{38}$ produces the DC shift at the amplifier output which effectively acts as a differential threshold for the discriminator. The VT2 input is controlled by an 8-bit DAC producing a common threshold for 256 channels, while the VT1 input is used to apply a 5-bit correction generated by on-channel trimming DACs with adjustable range. This solution improves the initial matching of the discriminator offsets from around 10 mV rms to better than 2 mV rms.

Figure 12 demonstrates the effect of the trimDAC setting measured on a long-strip module. Channels are first configured to have a trimDAC setting of 15 (mid-range) and the 50% occupancy threshold (vt50) is measured when 1 fC of charge is injected into each channel. Subsequently the channels are trimmed such that the vt50 response of each channel is equalised across the chip.



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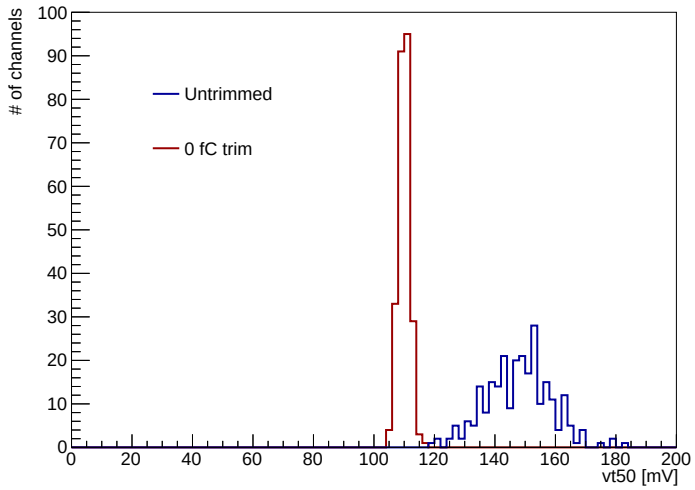


**Figure 12.** vt50 distribution with 1 fC injected charge over a single ABCStar before (trim DAC set to mid-range) and after trimming. The trim is performed at 0 fC input charge. The chip is loaded with 5 cm strips on a long-strip module. The RMS is measured to be 10.73 mV before trimming and 1.86 mV after.

The vt50 measurement with 1 fC of injected charge is then repeated. The distribution of the vt50 response is much narrower once the chip has been trimmed and an rms of 1.86 mV can be achieved (compared to 10.73 mV before trimming). To the already mentioned current consumed by the shaper stage, one should add the consumption of the 5-bit trimming DAC which is around 16 µA.

The final gain of the complete channel for the nominal bias set is around 85 mV/fC and the peaking time of the signal response is around 22 ns. The Full Width at Half Maximum (FWHM) is around 34 ns which is somewhere in between of the FWHM of the 2$^{nd}$ and 3$^{rd}$ order CR-RC filter of the same, 22 ns, peaking time. This is due to the fact that the preamplifier, which is a first amplification stage, is designed for the maximum bandwidth and its contribution to the integration of the signal is minimized.

### 3.4 Discriminator

As it was already mentioned the peaking time of the full chain response is around 22 ns which is comparable with the BCO (Bunch Cross Over) clock period. For that reason the ABCStar channel can employ a simple leading edge discriminator architecture providing both simplicity and low power consumption. The first stage of the discriminator is a simple differential pair (transistors $T_{45}$ and $T_{46}$) loaded with the resistors and swing limiter based on PMOS devices in diode configuration preventing the saturation of this stage. The differential pair is buffered with the PMOS source followers to cancel kick back effect which could otherwise propagate through common threshold line VT2. The differential pair together with the source follower buffers is supplied with the analogue power rail consuming 22 µA current.

The second stage of the discriminator is a classical differential to single ended CMOS converter with the hysteresis supplied from the digital power rail and consuming 9 µA of current. The bias for this stage is generated from a self biased current reference connected to the digital power domain.



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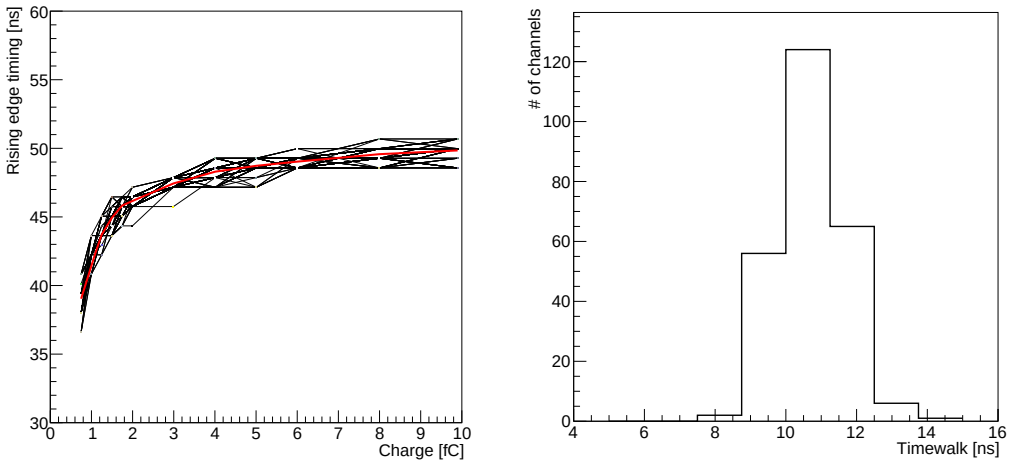


**(a)** Channel-by-channel time-walk measurement

**(b)** Histogram of Min-Max time-walk

**Figure 13.** Time-walk measurement for a chip on a long strip module for a threshold of 0.5 fC. The left hand side shows the rising edge timing as a function of injected charge for one chip, with the mean timing shown in red. The right hand side shows the distribution of the time-walk between 0.75 and 10 fC for the same chip.

The architecture of the discriminator and applied separation of analogue and digital power domains results in high rejection of the disturbances from the digital power supply to the differential input of the discriminator (gates of $T_{45}$ and $T_{46}$). The simulated rejection ratio for the extracted layout view is above 70 dB.

The simulated time-walk of the full channel response to 0.75 and 10 fC signals for the discriminator set to the 0.5 fC threshold is below 14 ns for worst case of load and PVT variation what provides correct association of the signal to the given BCO clock. Figure 13 shows the measurement of the time-walk for the typical ABCStar chip. The variation of the time-walks of the individual channels are related to the matching of the discriminators working with very low overdrive (0.25 fC). As can be seen, the variation of the time-walk is well within the 16 ns requirement.

## 4 Temperature and bias dependence and TID effects

The stability of the parameters of the front end ASIC over the PVT variation and radiation dose for very large scale systems, such as the ATLAS ITk detector, are of primary importance. All chip internal biases, current and voltage references for cascode amplifiers and threshold and trim DACs, are derived from the internal bandgap reference circuit providing good stability over the temperature as well as low drift, of about 1%, during the irradiation, as shown in figure 14. This provides good stabilisation of the discriminator threshold and operating points of all amplifiers especially the high open loop gain cascode stages employed in the preamplifier and booster.

Good stability of the bias current is also very important for the performance of the third amplification stage, i.e. the fully differential amplifier, and threshold interface which works in open loop gain configuration with light resistive degeneration. The gain of this stage depends directly



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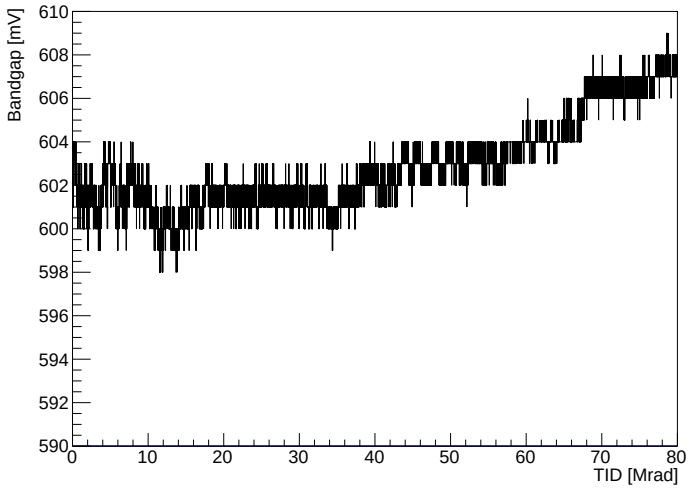


**Figure 14.** The evolution of the bandgap as a function of TID radiation for ABCStar ASIC.

on the transconductance of the transistors $T_{26}$ and $T_{27}$ loaded with the resistors $R_S$ and degenerated with the resistors $R_d$. For the nominal bias of 6 µA the transconductance of the devices $T_{26}$ and $T_{27}$ is of the order of 180 µS which for the 64 kΩ load could provide an open loop gain of around 12 [V/V] degenerated further with an 8 kΩ $R_d$ resistor to 4.5 [V/V]. Finally the ± 20% bias current variation causes up to ± 10% change of the gain. This behaviour is not ideal but one must stress that this is a price to be paid for the fully differential architecture, optimal from the PSRR standpoint, and very low power consumed by this stage.

Figure 15 shows the gain of the full channel for various setting of the voltage references for the cascode amplifiers, BVREF. One can see that for higher than nominal current biases, where the $T_{26}$ and $T_{27}$ transistors are biased in the moderate inversion region, the dependence of the gain on the bias is less pronounced. One can also notice that 20% variation in the voltage reference values does not affect the gain of the channel which confirms good design margins for the operating points of all cascode amplifiers. The dependence of the gain on the bias current is the same before and after irradiation.

Figure 16 shows the dependence of the input noise on the bias current setting, BIREF, for an unirradiated and irradiated ABCStar chip. The reduction of the ENC for higher biases follows the formula for the thermal noise contribution from the input transistor (see [7]) which is inversely proportional to the square root of the device transconductance. The improvement is less significant for larger bias currents because of the square root function as well as the nonlinear dependence of the transconductance to the current of the input transistor biased in a moderate inversion region. As it was previously shown in figure 11 the input noise does not change with irradiation.

Figure 17 shows the dependence of the gain and input noise on temperature. Over a 60 degree range from -40 to +20 C a 14% increase in the gain (and corresponding decrease in the input noise) was measured as the temperature was decreased. The variation of the gain with the temperature is once more related to the differential stage and the temperature dependence of the transconductance of the devices $T_{26}$ and $T_{27}$ (coefficient of the order of -0.3%/C, see [13]). The improvement of



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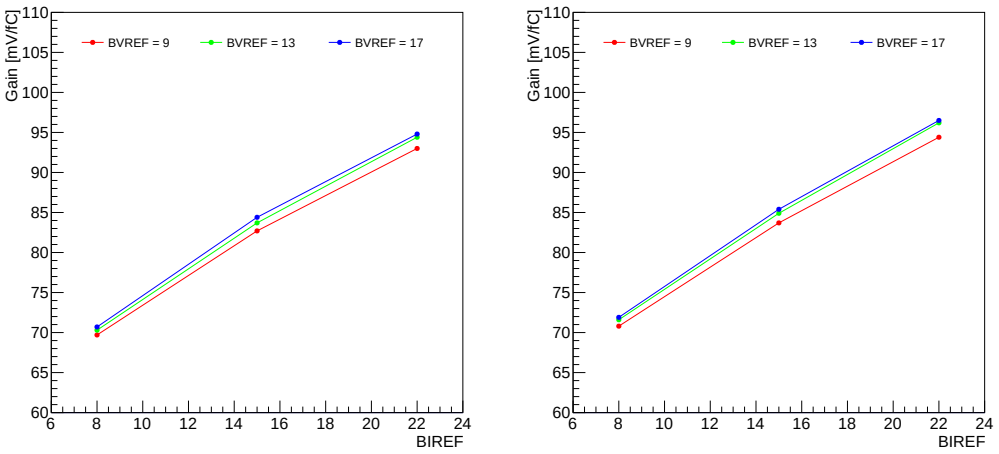
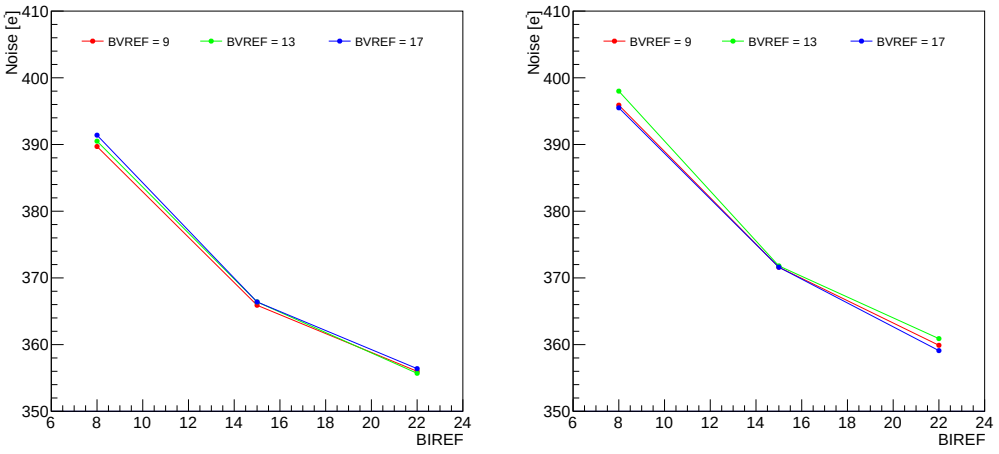



**(a)** Unirradiated chip **(b)** Irradiated chip

**Figure 15.** The evolution of gain as a function of the front-end bias DAC setting, BIREF for an unirradiated and an irradiated (to 80 Mrad) ABCStar. BIREF set to 15 provides nominal current bias, BIREF set to 22 and 8 is equivalent to ±20% of nominal current bias. BVREF set to 13 provides nominal voltage bias for cascode amplifiers, BVREF set to 17 and 9 is equivalent to ±20% of nominal voltage bias.




**(a)** Unirradiated chip **(b)** Irradiated chip

**Figure 16.** The evolution of noise as a function of the front-end current bias DAC setting, BIREF for an unirradiated and an irradiated (to 80 Mrad) ABCStar. BIREF set to 15 provides nominal current bias, BIREF set to 22 and 8 is equivalent to ±20% of nominal current bias. BVREF set to 13 provides nominal voltage bias for cascode amplifiers, BVREF set to 17 and 9 is equivalent to ±20% of nominal voltage bias.

the ENC for lower temperatures is twofold. First the transconductance of the input transistor is increased towards lower temperatures, as it was mention previously, which directly impacts the series noise contribution similar to the case of an increase of bias current. Secondly, the input noise is improved proportionally to the square root of the k·T product of the Boltzmann constant and the



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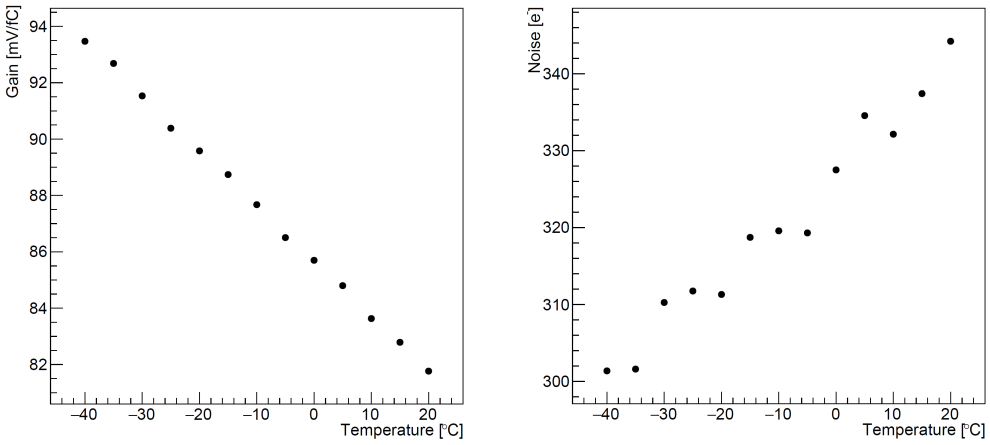


**(a)** Gain

**(b)** Input noise

**Figure 17.** The evolution of the gain and input noise as a function of temperature for ABCStar. The temperature listed here is the set point of the climate chamber. The temperature of the SCB in close proximity to the ASIC was measured to be 2 degrees higher than the chamber set point.

temperature which influence both the series (input transistor) and parallel (feedback resistor) noise contributions (see [7]).

Figure 18 shows the evolution of the channel gain with TID irradiation up to a maximum dose of 80 MRad. The relatively low, 5%, degradation around 10 MRad correlates with the so called TID peak of the leakage current for the regular layout NMOS devices (see [14]). Again the effect can be attributed to the differential stage and the transistors $T_{26}$ and $T_{27}$ which are 10 finger devices. The transistors are biased with low, 6 µA current, fixed by the current source and the leakage, which is related to the side effect in Shallow Trench Isolation, decrease effective current in the channel causing the degradation of the transconductance and consequently the gain of this stage. Although this degradation is at an acceptable level, in case of further change of the ABCStar masks before final production the layout of $T_{26}$ and $T_{27}$ transistors will also be changed to the enclosed geometry configuration.

All the above bias and temperature effects as well as possible gain degradation due to TID radiation can always be calibrated in-situ using the internal calibration circuit biased with the on chip bandgap circuit which does not show any temperature or bias dependence and which is stable during irradiation. The bandgap circuit is the modified (different error amplifier) version of the design described in [15]. It is based on the current summing principle and in contrary to the classical structure, instead of diodes, uses DTMOST (dynamic threshold MOS) devices. This provide good tolerance to the TID radiation (drift below 1%, see figure 14) and in practice immunity to the NIEL damage (no lightly doped PN junction in critical devices). The operating threshold as well as trim values for the per channel Trim DACs should be obtained for the given set of the bias DACs and operating temperature (chips working on modules with or without cooling, single chips on the PCB, chips probed on the wafer probe station etc.).



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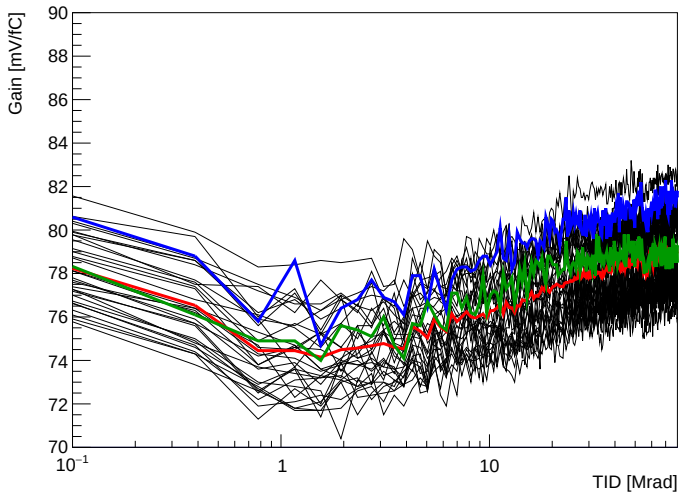


**Figure 18.** The evolution of the gain as a function of TID radiation for ABCStar ASIC. The blue and green channels are respectively connected to 2.5 pF and 4.7 pF external capacitors. The red trace shows the average of 30 unloaded channels which are each individually shown in black.

## 5 Perspectives for operating ABCStar front end chip in the ATLAS experiment

Using the provision on the SCBs to load single ABCStar front-ends with discrete capacitive loads, the noise as a function of load can be measured. This is performed for a 1 fC input charge. This is shown in figure 19 for both an unirradiated and irradiated ASIC. Compared to the previous ABC130 chipset the noise is lower across the capacitance range measured. Of particular note, compared to ABC130, the increase in noise with capacitance is shallower and, most importantly, the curve is almost entirely unchanged when the chips are irradiated to 80 Mrad.

Figure 20 compares the dependence of noise on capacitance for single ABCStar ASICs on SCBs with capacitive loads compared to the noise on modules where the front-ends are connected to real silicon strips. The capacitance values for the modules are derived from probe station measurements of the inter-strip and strip-backplane capacitance of real sensors. Only nearest neighbour inter-strip capacitance is included. Across the full capacitance range a 10% noise increase is observed comparing module measurements to single chip measurements.

Using a fit to the module level noise results shown in figure 20 (black dotted line) combined with measurements of sensor charge collection [16], calculations of expected shot noise, and radiation levels taken from simulations, a signal-to-noise ratio can be calculated for all locations in the detector. The detector requirements of at least 99% efficiency and less than 0.1% noise occupancy equate to a signal-to-noise requirement of at least 10 throughout the life of the detector. Given the results shown above, the signal-to-noise ratio at end-of-life is calculated to be no lower than 12.2 across the whole detector and so, the ABCStar successfully satisfies the required end-of-life performance.



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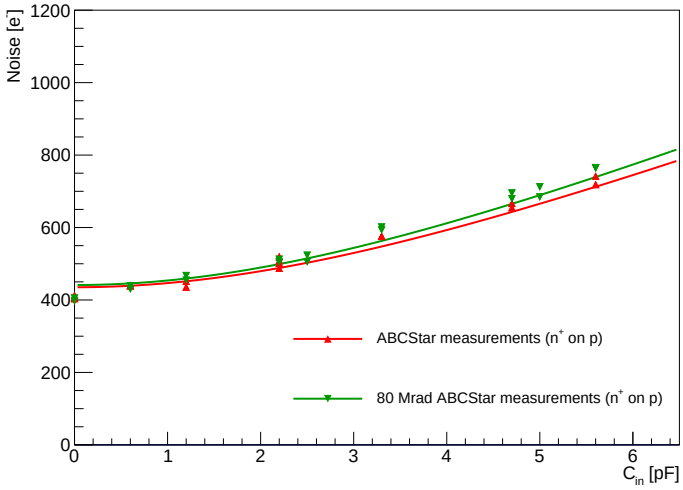


**Figure 19.** The ENC as a function of input capacitance for the irradiated (to 80 Mrad) and non-irradiated ABCStar front end chip. Note that the measurements done before and after irradiation are done using separate chips. Two channels are measured per chip.

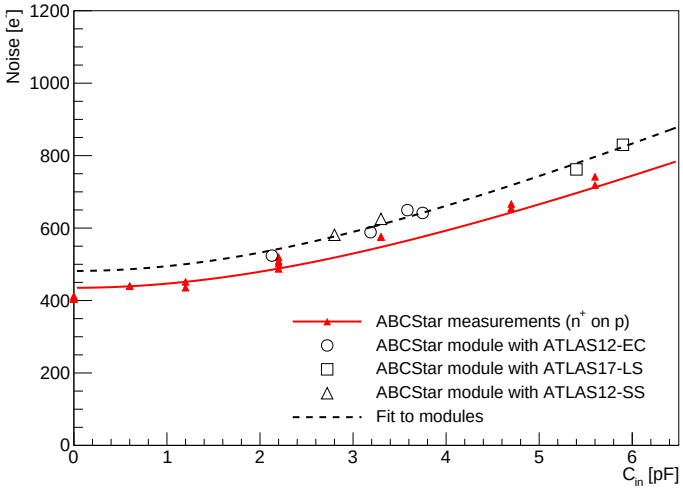


**Figure 20.** The ENC as a function of input capacitance comparing single chip measurements (red) to measurements made on prototype modules. The capacitance values for the module points are taken from sensor probing measurements and include capacitance to both back plane and nearest neighbour. Next-to-nearest neighbours have not been included in the calculation.

## 6 Summary

We present the final version of the front end amplifier optimised for ATLAS ITk strip sensors and implemented in a radiation tolerant CMOS 130 nm process. The ABCStar front end chip meets all requirements of the ATLAS ITk detector staying within allowable current consumption budget. For the nominal bias settings the current consumed by the single channel is around 260 µA. The current consumed in the whole analogue part of the ABCStar chip (256 channels and common



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analogue blocks) is below 68 mA. The noise measured for 3.5 pF and 6 pF input capacitance is below 650 $e^-$ and 800 $e^-$ ENC respectively which is below the specified levels. The time-walk of the discriminator set to a 0.5 fC threshold for the 0.75 and 10 fC signal response is well below the required 16 ns which ensures the correct association of the event to the given BCO clock. The noise degradation after ionizing radiation stays at a negligible level, which guarantees correct operation of the chip at the end of the detector lifetime and is consistent with an expected signal-to-noise ratio at end-of-life of more than 12:1 across all regions of the detector.

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