

# Quantum-Inspired Fourier Transforms Based on Circuits

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Fourier transform (FT) is ubiquitous in modern society due to their broad applications in many branches of science and engineering. Improving the speed of FT is a common interest in the fields of signal processing. The quantum FT is generally believed to be superior to classical algorithms, but it requires a special quantum environment to perform, which has not yet been widely used. Inspired by quantum FT, here a new FT scheme is demonstrated based on circuits. In the circuit scheme, a new type of classical correlation, which its mathematical form corresponds to those of quantum entanglement, has been constructed. The calculation speed using the designed circuit scheme is equivalent to those based on the quantum FT algorithms, which is faster than those based on the classical fast FT algorithms. Furthermore, some basic gates have been designed and experimentally fabricated using classical circuit networks, which can emulate the functions of quantum gates. Fast calculation efficiencies for the FT based on the designed classical circuit networks have been demonstrated. Extensive applications of the FT scheme in the signal processing are anticipated.

environment, where information is encoded using quantum states. Because quantum states are quite fragile and easily affected by external disturbance, the bottleneck issues such as decoherence and scalability are particularly difficult to address.<sup>[9,20]</sup> Although there have been significant progresses in the research of quantum information process in recent years,<sup>[21–31]</sup> applying QFT to solve practical problems still keeps great challenges.

Recent investigations have shown that a formal analogy between classical and quantum information processes can be constructed.<sup>[32–53]</sup> Based on such a correspondence, the QFT has been emulated in some classical systems.<sup>[54–56]</sup> For example, an electric circuit scheme for performing the QFT has been discussed in a recent work, by using the simulation of quantum walks.<sup>[56]</sup> However, the proposed scheme is not scalable. Namely, it needs  $2^n$  number of circuit components to

realize  $n$  qubits. This means that the scheme failed to provide a classical analogy of QFT circuit in sources. The question is whether it is possible to design classical circuits to implement better analogy of QFT circuit.

Inspired by the QFT circuit scheme, in this work we propose an analog scheme of classical circuit for the QFT. In our scheme, the classical circuit network, which includes the information processing elements that corresponds to the quantum gate sets, is designed. The information is encoded using correlated electrical signals, which establishes a mathematical correspondence between the novel classical correlation and quantum entanglement. This makes the classical circuit network have processing functions similar to that of quantum computation. As a results, the number of the basic computing components employed in our circuit, including only the copy, addition, subtraction and multiplication operations, is consistent with the number of the quantum gate in quantum circuit. Based on our theoretical consideration, we present an experimental verification on the analogy of the two, three and five qubit processors.

## 1. Introduction

Fourier transform (FT) becomes a standard tool in contemporary sciences since the ‘fast Fourier transform (FFT)’ algorithm was developed in 1965.<sup>[1]</sup> It has been used in many fields such as physics, number calculation, signal processing, probability statistics, cryptography, acoustics, and optics.<sup>[2,3]</sup> The FFT plays an important role in these fields. On the other hand, with the progress of research in quantum information, the quantum FT algorithm has been proposed.<sup>[4–9]</sup> The quantum FT (QFT) is believed to outperform the classical FFT in signal processing, which has attracted much attention in recent decades.<sup>[10–19]</sup> However, the QFT is typically believed to be performed in a quantum computing

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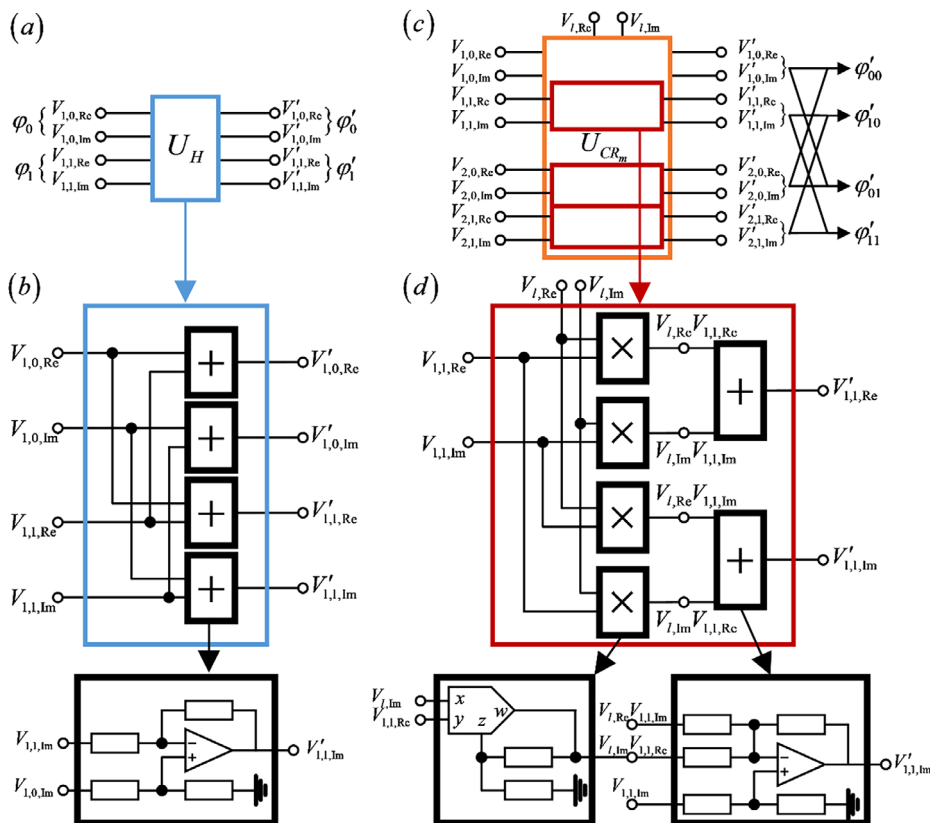
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## 2. Theoretical Scheme of Quantum-Inspired Fast Fourier Transforms Based on Circuits

The  $n$ -qubit QFT is a basis transformation in an  $N = 2^n$ -state space that transforms the state  $|K\rangle$  to  $|J\rangle$  ( $K$  and  $J$  are integers ranging from 0 to  $N - 1$ ) according to

$$|K\rangle \xrightarrow{\text{QFT}} \frac{1}{\sqrt{N}} \sum_{J=0}^{N-1} e^{i2\pi KJ/N} |J\rangle, \quad (1)$$



**Figure 1.** a) The diagram of the 1-cebit gate  $U_H$ . In 1-cebit system, the amplitude  $\phi_0$  depends on voltage signals  $V_{1,0,Re}$  and  $V_{1,0,Im}$ , while the amplitude  $\phi_1$  depends on voltage signals  $V_{1,1,Re}$  and  $V_{1,1,Im}$ . b) The circuit design of the 1-cebit gate  $U_H$ . It consists of 4 adder modules. These modules share a similar design, but their specific configurations differ. One typical module includes 1 operational amplifier (represented by triangle) and 4 resistors (represented by a rectangle). c) The diagram of the 2-cebit gate  $U_{CR_m}$ . In 2-cebit system, the amplitude  $\phi_{00}$  depends on the voltage signals  $V_{1,0,Re}$ ,  $V_{1,0,Im}$ ,  $V_{2,0,Re}$  and  $V_{2,0,Im}$ , and so do the other amplitudes. d) The circuit design of the CR module. It consists of 4 multiplier modules (marked by “ $\times$ ”) and 2 adder modules (marked by “+”). Different multiplier modules share identical designs, containing 1 analog multiplier (represented by pentagon) and 2 resistor (represented by a rectangle), while adder modules differ in their circuit designs, containing 1 analog adder (represented by triangle) and varying numbers resistor (represented by a rectangle).

$$\sum_{K=1}^N x_K |K\rangle \xrightarrow{\text{QFT}} \sum_{J=1}^N X_J |J\rangle = \sum_{J=1}^N \frac{1}{\sqrt{N}} \sum_{K=1}^N x_K e^{i2\pi KJ/N} |K\rangle, \quad (2)$$

where the  $N$  data points  $x_1, x_2, \dots, x_{N-1}$  and  $x_N$  are encoded into the  $N$  amplitudes of the  $N$  basis states, and the output amplitudes  $X_1, X_2, \dots, X_{N-1}$  and  $X_N$  are the results of the discrete FT of the  $N$  input amplitudes.

The quantum circuit model of the QFT utilizes the 1-qubit Hadamard gate

$$\hat{U}_H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (3)$$

and the 2-qubit controlled phase gates

$$\hat{U}_{CR_m} = \begin{bmatrix} 1 & & & \\ & 1 & & \\ & & 1 & \\ & & & e^{2\pi i/2^m} \end{bmatrix}, \quad (4)$$

where  $m$  is a variable parameter. To simulate the QFT using an electric circuit, two essential actions must be performed. One is defining the analog of a qubit with the state of the electric circuits, and the other is certifying the electric operations on those states that can realize the function of the above quantum gates. To simulate the qubit, we define “cebit” in our circuit design. Each cebit contains 4 voltage signals, and we can get  $2^n$  classical states to correspond to quantum states using the  $4n$  voltage signals of the  $n$  cebits. To simulate the quantum gates, we realize the corresponding circuit gates.

We first take the correspondence to the 1-qubit gate  $\hat{U}_H$  as an example. The  $\hat{U}_H$  gate acts on the quantum state  $|\phi\rangle = \phi_0|0\rangle + \phi_1|1\rangle = \begin{bmatrix} \phi_0 \\ \phi_1 \end{bmatrix}$  as

$$\begin{bmatrix} \phi'_0 \\ \phi'_1 \end{bmatrix} = \hat{U}_H \begin{bmatrix} \phi_0 \\ \phi_1 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} \phi_0 + \phi_1 \\ \phi_0 - \phi_1 \end{bmatrix}, \quad (5)$$

where  $\phi_0$  and  $\phi_1$  represent the amplitude of the quantum state  $|\phi\rangle$ , and they are transformed into  $\phi'_0$  and  $\phi'_1$ . To implement the corresponding 1-qubit operation in the classical circuit, we construct the circuit network  $U_H$  as shown in Figure 1a. The 4 in-

put voltage signals denoted by  $\overline{V}_1 = (V_{1,0,Re}, V_{1,0,Im}, V_{1,1,Re}, V_{1,1,Im})^T$ , where “T” represents the matrix transpose, are used as the analog of a qubit as a whole and known as a cebit. Each component of  $\overline{V}_1$  is a time-dependent voltage function. To implement the function of the Hadamard gate correspondingly, the circuit network  $U_H$  is required to transform the input voltage signals into the output voltage signals ( $V' = (V'_{1,0,Re}, V'_{1,0,Im}, V'_{1,1,Re}, V'_{1,1,Im})^T$ ), as shown by

$$\begin{bmatrix} V'_{1,0,Re} \\ V'_{1,0,Im} \\ V'_{1,1,Re} \\ V'_{1,1,Im} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} V_{1,0,Re} + V_{1,1,Re} \\ V_{1,0,Im} + V_{1,1,Im} \\ V_{1,0,Re} - V_{1,1,Re} \\ V_{1,0,Im} - V_{1,1,Im} \end{bmatrix}. \quad (6)$$

Subsequently we demonstrate that the transformation of the voltage signals can be described by the classical state  $|\varphi\rangle$  corresponding to the quantum state  $|\phi\rangle$ . To illustrate the relation between the classical states and the quantum states clearer, we employ the notation “|” to denote the classical states given by cebit. In particular, the classical state of the voltage signals is expressed by

$$|\varphi\rangle = \varphi_0 |0\rangle + \varphi_1 |1\rangle = \begin{bmatrix} \varphi_0 \\ \varphi_1 \end{bmatrix}, \quad (7)$$

where

$$\varphi_0 = \frac{1}{T} \int_0^T dt \sum_{w=1}^W e^{-i\omega t} (V_{1,0,Re} + iV_{1,0,Im}), \quad (8)$$

$$\varphi_1 = \frac{1}{T} \int_0^T dt \sum_{w=1}^W e^{-i\omega t} (V_{1,1,Re} + iV_{1,1,Im}). \quad (9)$$

$\varphi_0$  and  $\varphi_1$  represents the complex amplitudes of the classical state  $|\varphi\rangle$  corresponding to the complex amplitudes of the quantum state  $|\phi\rangle$ . As complex values, they are obtained from the complex voltage signal function  $V_{1,0,Re} + iV_{1,0,Im}$  and  $V_{1,1,Re} + iV_{1,1,Im}$  respectively.  $T = 2\pi/\omega$  is the period of the voltage signals, where the frequency  $\omega$  depends on the experimental setting. And the summation upper limit  $W$  for the index  $w$  is determined by the input voltage  $V_{1,0,Re}, V_{1,0,Im}, V_{1,1,Re}$  and  $V_{1,1,Im}$ . We denote the highest frequency component in the spectrum of  $V$  as  $W\omega$ . Since  $\omega$  is known,  $W$  can be derived accordingly. Under the definition above, the gate  $U_H$  transforms the input classical state  $|\varphi\rangle$  into the output state  $|\varphi'\rangle = \varphi'_0 |0\rangle + \varphi'_1 |1\rangle$ , where

$$\begin{aligned} \varphi'_0 &= \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} (V'_{1,0,Re} + iV'_{1,0,Im}) \\ &= \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \frac{V_{1,0,Re} + V_{1,1,Re} + iV_{1,0,Im} + iV_{1,1,Im}}{\sqrt{2}} \\ &= \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \frac{V_{1,0,Re} + iV_{1,0,Im}}{\sqrt{2}} \end{aligned}$$

$$\begin{aligned} &+ \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \frac{V_{1,1,Re} + iV_{1,1,Im}}{\sqrt{2}} \\ &= \frac{\varphi_0 + \varphi_1}{\sqrt{2}}, \end{aligned} \quad (10)$$

and

$$\varphi'_1 = \frac{\varphi_0 - \varphi_1}{\sqrt{2}}. \quad (11)$$

So we have

$$|\varphi'\rangle = \varphi'_0 |0\rangle + \varphi'_1 |1\rangle = \begin{bmatrix} \varphi'_0 \\ \varphi'_1 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} \varphi_0 + \varphi_1 \\ \varphi_0 - \varphi_1 \end{bmatrix}, \quad (12)$$

which corresponds to the result shown in Equation (5).

Next, we briefly describe the design of the circuit network  $U_H$  used to implement the transformation shown in Equation (6). As is shown in Figure 1b,  $U_H$  consists of 4 analog adder/subtractor modules, which are referred to as “adder/subtractor circuit”. Since subtraction is mathematically equivalent to adding a negative value, we simply call it “adder module”, and mark the module by the black boxes with plus sign “+”. Each module has 2 input and 1 output, performing weighted addition operations on the input voltage signals and outputs the result. These adder modules share a similar design, but their specific configurations are different. Here, we illustrate the structure of one certain modules. This depicted module contains 1 operational amplifier (represented by triangle) and 4 resistors (represented by rectangle). The design details of the module and its calculation results are provided in the subhead “The detailed circuit design of 1-cebit gate (adder module)” of Experimental Section.

Now we consider the correspondence 2-qubit gate  $\hat{U}_{CR_m}$ . The  $\hat{U}_{CR_m}$  acts on the quantum state  $|\phi\rangle = \phi_{00}|00\rangle + \phi_{01}|01\rangle + \phi_{10}|10\rangle + \phi_{11}|11\rangle$  as

$$\begin{bmatrix} \phi'_{00} \\ \phi'_{01} \\ \phi'_{10} \\ \phi'_{11} \end{bmatrix} = \hat{U}_{CR_m} \begin{bmatrix} \phi_{00} \\ \phi_{01} \\ \phi_{10} \\ \phi_{11} \end{bmatrix} = \begin{bmatrix} \phi_{00} \\ \phi_{01} \\ \phi_{10} \\ e^{2\pi i/2^m} \phi_{11} \end{bmatrix}, \quad (13)$$

where  $\phi_{00}, \phi_{01}, \phi_{10}$  and  $\phi_{11}$  represent the amplitude of the quantum state. To implement the corresponding 2-qubit operation using the classical circuit, we construct the circuit network  $U_{CR_m}$  as shown in Figure 1c. The 8 voltage signals for two cebits are denoted as  $\overline{V}_k = (V_{k,0,Re}, V_{k,0,Im}, V_{k,1,Re}, V_{k,1,Im})^T$  ( $k = 1, 2$ ). In addition, this classical gate contains 2 fixed inputs  $V_{1,Re}$  and  $V_{1,Im}$ , which multiply with these component voltage signals. The circuit network  $U_{CR_m}$  transforms these voltage signals into  $\overline{V}'_k = (V'_{k,0,Re}, V'_{k,0,Im}, V'_{k,1,Re}, V'_{k,1,Im})^T$ , and we have

$$\begin{cases} \begin{bmatrix} V'_{1,0,Re} \\ V'_{1,0,Im} \\ V'_{1,1,Re} \\ V'_{1,1,Im} \end{bmatrix} = \begin{bmatrix} V_{1,0,Re} \\ V_{1,0,Im} \\ V_{l,Re} V_{1,1,Re} - V_{l,Im} V_{1,1,Im} \\ V_{l,Re} V_{1,1,Im} + V_{l,Im} V_{1,1,Re} \end{bmatrix}, \\ \begin{bmatrix} V'_{2,0,Re} \\ V'_{2,0,Im} \\ V'_{2,1,Re} \\ V'_{2,1,Im} \end{bmatrix} = \begin{bmatrix} V_{2,0,Re} + V_{l,Re} V_{2,0,Re} - V_{l,Im} V_{2,0,Im} \\ V_{2,0,Im} + V_{l,Re} V_{2,0,Im} + V_{l,Im} V_{2,0,Re} \\ V_{2,1,Re} + \cos(2\pi/2^m) F_{Re} - \sin(2\pi/2^m) F_{Im} \\ V_{2,1,Im} + \sin(2\pi/2^m) F_{Re} + \cos(2\pi/2^m) F_{Im} \end{bmatrix}. \end{cases} \quad (14)$$

$(F_{Re} = V_{l,Re} V_{2,1,Re} - V_{l,Im} V_{2,1,Im}, F_{Im} = V_{l,Re} V_{2,1,Im} + V_{l,Im} V_{2,1,Re})$

The classical state  $|\varphi\rangle$  can be expressed by the voltage signals using the above definitions

$$|\varphi\rangle = \varphi_{00} |00\rangle + \varphi_{01} |01\rangle + \varphi_{10} |10\rangle + \varphi_{11} |11\rangle = \begin{bmatrix} \varphi_{00} \\ \varphi_{01} \\ \varphi_{10} \\ \varphi_{11} \end{bmatrix}, \quad (15)$$

where

$$\varphi_{s_1, s_2} = \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} F_{1, s_1} * F_{2, s_2}. \quad (16)$$

Here  $\varphi_{s_1, s_2}$  represents the amplitude of the classical state, and the subscript  $s_1$  and  $s_2$  take the value 0 or 1, the functions represent

$$F_{1, s} = V_{1, s, Re} + iV_{1, s, Im}, F_{2, s} = V_{2, s, Re} + iV_{2, s, Im}, \quad (17)$$

and the symbol “\*” is the convolution operation, for the periodic functions  $f_1$  and  $f_2$  with period  $T$ , we have

$$f_1 * f_2 = \frac{1}{T} \int_0^T d\tau f_1(\tau) f_2(t - \tau). \quad (18)$$

In general convolution operations, the integration limits range from  $-\infty$  to  $+\infty$ , however, for periodic sine and cosine function, the integration limits are confined to the interval  $[0, T]$ . Both Equations (16) and (18) have  $T$  as the upper integration limits, which is the period of the voltage signals.

As an example, if we take  $s_1 = s_2 = 0$ , then

$$\begin{aligned} F_{1,0} * F_{2,0} &= \frac{1}{T} \int_0^T d\tau [(V_{1,0,Re}(\tau) + iV_{1,0,Im}(\tau)) \\ &\times (V_{2,0,Re}(t - \tau) + iV_{2,0,Im}(t - \tau))]. \end{aligned} \quad (19)$$

So the amplitude  $\varphi_{00}$  depends on the complex voltage signals  $V_{1,0,Re} + iV_{1,0,Im}$  and  $V_{2,0,Re} + iV_{2,0,Im}$ , as the other amplitudes do.

Under the representation scheme in the above, the gate  $U_{CR_m}$  transforms the input classical state  $|\varphi\rangle$  into the output state

$$|\varphi'\rangle = \begin{bmatrix} \varphi'_{00} \\ \varphi'_{01} \\ \varphi'_{10} \\ \varphi'_{11} \end{bmatrix} = \begin{bmatrix} \varphi_{00} \\ \varphi_{01} \\ \varphi_{10} \\ e^{2\pi i/2^m} \varphi_{11} \end{bmatrix} \quad (20)$$

It corresponds to the result in Equation (13), which describes the action of the 2-qubit quantum gate  $\hat{U}_{CR_m}$  on the quantum state. The proof details are provided in the subhead “The detailed circuit design and the output calculation of CR module” of Experimental Section.

Next, we describe the design of the circuit network  $U_{CR_m}$  used to implement the transformation in Equation (14). As shown in Figure 1c,  $U_{CR_m}$  consists of 3 modules (red boxes), which we refer to as “CR modules”. The first CR module receives input voltage signals  $V_{1,1,Re}$  and  $V_{1,1,Im}$ , the second incorporates  $V_{2,0,Re}$  and  $V_{2,0,Im}$  among its inputs, while the third operates with  $V_{2,1,Re}$  and  $V_{2,1,Im}$ . The remaining 2 input signals  $V_{1,0,Re}$  and  $V_{1,0,Im}$  remain fixed. In addition,  $V_{l,Re}$  and  $V_{l,Im}$  are externally applied single-frequency cosine and sine signals, respectively. Their frequency is set to match the highest spectral component within the combined spectra of all the voltage signals.

Figure 1d illustrates a certain CR module whose outputs  $V'_{1,1,Re}$  and  $V'_{1,1,Im}$  are defined by Equation (14). To achieve  $V'_{1,1,Re}$ , we multiply  $V_{l,Re}$  and  $V_{1,1,Re}$  through the multiplier module (marked by “×”) to obtain  $V_{l,Re} V_{1,1,Re}$ , and multiply  $V_{l,Im}$  and  $V_{1,1,Im}$  to obtain  $V_{l,Im} V_{1,1,Im}$ . These two resultant signals are then subtracted through the adder module (marked by “−”), producing the final output  $V_{l,Re} V_{1,1,Re} - V_{l,Im} V_{1,1,Im}$ . The left component voltage signals follow the analogous procedure, but the adder modules in these cases incorporate additional input signals.

One CR module consists of 4 multiplier modules and 2 adder modules, and we illustrate one certain multiplier module and one certain adder module. Generally, each multiplier module contains 1 analog multiplier (represented by pentagon) and 2 resistor (represented by rectangle), while each adder modules contains 1 analog adder (represented by triangle) and varying numbers resistor (represented by rectangle), with the resistor count dependent on the number of input signals to the analog adder. The design details of the module and its calculation results are provided in the subhead “The detailed circuit design and the output calculation of CR module” of Experimental Section.

It is well known that generating quantum entanglements is the key function of the 2-qubit quantum gate, therefore our 2-cebit circuit gate needs to have analogous effects. Now we analyze the classical correlation in our circuit design from two aspects. Mathematically, it manifests in the operational equivalence between the classical gates described in Equation (20) and the quantum gates in Equation (13). Physically, since entanglement typically originates from interactions that can be mathematically characterized through multiplication operation, the multiplication introduced in our circuit generates similar interaction-like effects. In the following section, we will provide experimental evidence.

After the discussion of the circuit correspondence of the quantum gates in low-qubit systems, we now consider scaling the system up to  $n$  cebit, which can be thought of as an analog of an  $n$ -qubit system. When the number of cebit increases to  $n$ , the implementation of the two types of circuit gates is required to be generalized properly based on the above designs. Since the gates

depend on the definition of the classical states obtained by the voltage signals, we first address how the definition evolves when scaling from a 2-cebit to an  $n$ -cebit system.

In the  $n$ -cebit circuit, the input voltage signals for each cebit are denoted as  $\vec{V}_k = (V_{k,0,Re}, V_{k,0,Im}, V_{k,1,Re}, V_{k,1,Im})^T$  ( $k = 1, 2, \dots, n$ ). The classical state is obtained from the complex voltage signals as

$$|\varphi\rangle = \sum_{s_1, s_2, \dots, s_n} \varphi_{s_1 s_2 \dots s_n} |s_1 s_2 \dots s_n\rangle, \quad (21)$$

$$\varphi_{s_1 s_2 \dots s_n} = \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \prod_{k=1}^n * (V_{k,s_k,Re} + iV_{k,s_k,Im}), \quad (22)$$

where the subscripts  $s_k$  take the value 0 or 1, so  $\varphi$  has  $2^n$  subscripts. We denote the successive convolution operation by the symbol “ $\prod *$ ”, which is defined as

$$\prod_{k=1}^n * (f_k) = f_1 * f_2 * \dots * f_n. \quad (23)$$

Following the discussion on the evolution of the definition of the classical states, we now address the modifications to the  $U_H$  gate and the  $U_{CR_m}$  gate when scaling to the  $n$ -cebit system. The design of  $U_H$  gate remains consistent in the  $n$ -cebit system. To implement  $U_H$  gate on the  $k_0$ -th cebit, we feed the input voltage signals of the  $k_0$ -th cebit into the  $U_H$  gate, while we keep the voltage signals of all other cebits unchanged. The  $U_H$  gate transforms the classical state into

$$\begin{bmatrix} \varphi'_{s_{k_0}=0} \\ \varphi'_{s_{k_0}=1} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} \varphi_{s_{k_0}=0} + \varphi_{s_{k_0}=1} \\ \varphi_{s_{k_0}=0} - \varphi_{s_{k_0}=1} \end{bmatrix}. \quad (24)$$

This expression corresponds to the result of extending Equation (12) to the  $n$ -cebit system. Detailed calculations are provided in the subhead “The Detailed Circuit Design of 1-Cebit Gate (Adder Module)” of Experimental Section This expression also corresponds to the action result of the 1-qubit Hadamard gate  $\hat{U}_H$  in the  $n$ -qubit system

$$\begin{bmatrix} \varphi'_{s_{k_0}=0} \\ \varphi'_{s_{k_0}=1} \end{bmatrix} = \hat{U}_H \begin{bmatrix} \varphi_{s_{k_0}=0} \\ \varphi_{s_{k_0}=1} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} \varphi_{s_{k_0}=0} + \varphi_{s_{k_0}=1} \\ \varphi_{s_{k_0}=0} - \varphi_{s_{k_0}=1} \end{bmatrix}, \quad (25)$$

where  $\varphi_{s_{k_0}=0}$  should be understood as selecting the components when the subscript  $s_{k_0} = 0$  from the entire set of  $\varphi_{s_1 s_2 \dots s_n}$ , and then forming a column vector composed of these selected components. And so are  $\varphi_{s_{k_0}=1}$ ,  $\varphi_{s_{k_0}=0}$  and  $\varphi_{s_{k_0}=1}$ .

During the extension of the  $U_{CR_m}$  gate to the  $n$ -cebit system, we uncover an intriguing property, that the circuit system can efficiently implement the classical correlations among multiple cebits. We first talk about the multi-qubit entanglement in quantum system. As is shown in Figure 2a, the multi-qubit entangled operation  $\hat{U}_{CR}$  in QFT is constructed by cascading multiple  $\hat{U}_{CR_m}$  gate

$$\hat{U}_{CR} = \hat{U}_{k_1 \rightarrow k_1+1} \hat{U}_{k_1 \rightarrow k_1+2} \dots \hat{U}_{k_1 \rightarrow n}. \quad (26)$$

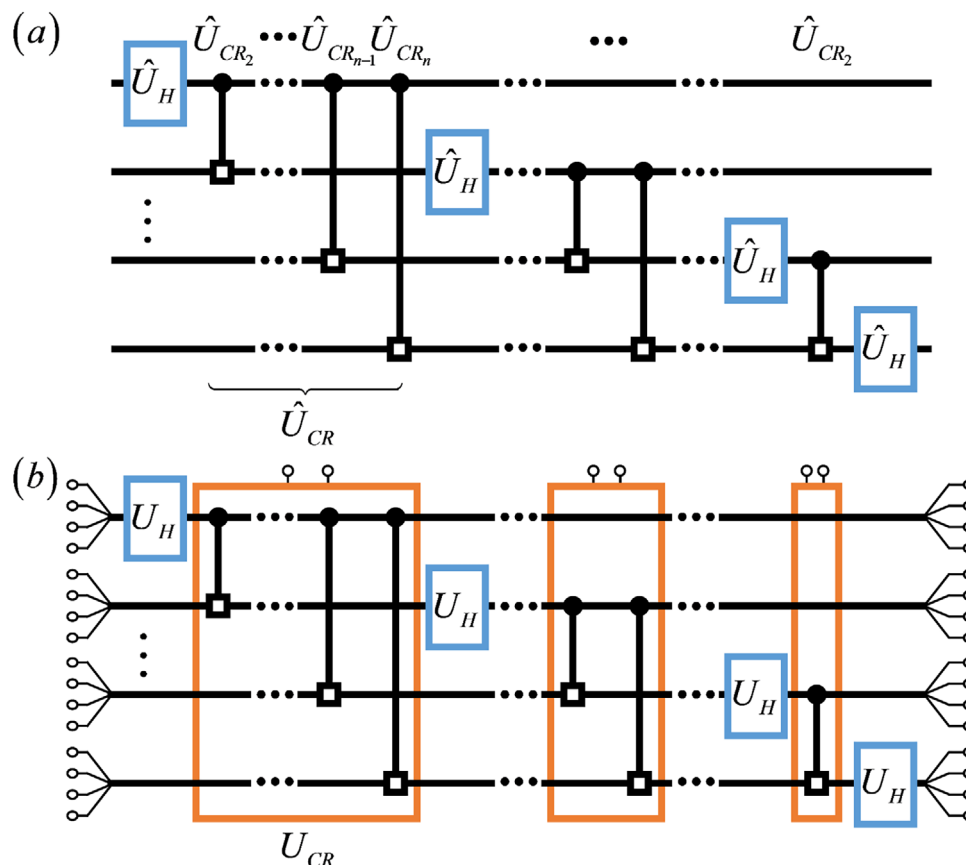
Here  $\hat{U}_{k \rightarrow k+l}$  ( $l = 1, 2, \dots, n - k$ ) represents a controlled-phase  $\hat{U}_{CR_m}$  gate with the  $k$ -th qubit being the control qubit and the  $(k + l)$ -th qubit being the target qubit, and the parameter  $m$  equals to  $l + 1$ . The qubits in  $\hat{U}_{CR_m}$  gate are divided into three part  $k_0, k_1$  and  $k_2$  as followed. In this multi-qubit entanglement scheme, these  $\hat{U}_{CR_m}$  gates share the same control qubit called  $k_1$ . And the  $(k_1 + 1)$ -th to the  $n$ -th qubit are collectively denoted as  $k_2$ , since these qubit are the target qubit for one controlled-phase gate in  $\hat{U}_{CR}$ . The remain qubits are labeled as  $k_0$ , spanning from 1 to  $k_1 - 1$ . In quantum system, these gates rely on distinct entanglement correlations between different qubits, and is hard to be implemented with a single quantum operation. However, in classical circuit, such classical correlations among multi-cebit can be realized straightforwardly. This is achieved using a single  $U_{CR}$  gate as is shown in Figure 2b, and it transforms these voltage signals into

$$\begin{bmatrix} V'_{k_0,0,Re} \\ V'_{k_0,0,Im} \\ V'_{k_0,1,Re} \\ V'_{k_0,1,Im} \\ V'_{k_1,0,Re} \\ V'_{k_1,0,Im} \\ V'_{k_1,1,Re} \\ V'_{k_1,1,Im} \\ V'_{k_2,0,Re} \\ V'_{k_2,0,Im} \\ V'_{k_2,1,Re} \\ V'_{k_2,1,Im} \end{bmatrix} = \begin{bmatrix} V_{k_0,0,Re} + V_{l,Re} V_{k_0,0,Re} - V_{l,Im} V_{k_0,0,Im} \\ V_{k_0,0,Im} + V_{l,Re} V_{k_0,0,Im} + V_{l,Im} V_{k_0,0,Re} \\ V_{k_0,1,Re} + V_{l,Re} V_{k_0,1,Re} - V_{l,Im} V_{k_0,1,Im} \\ V_{k_0,1,Im} + V_{l,Re} V_{k_0,1,Im} + V_{l,Im} V_{k_0,1,Re} \\ V_{k_1,0,Re} \\ V_{k_1,0,Im} \\ V_{l,Re} V_{k_1,1,Re} - V_{l,Im} V_{k_1,1,Im} \\ V_{l,Re} V_{k_1,1,Im} + V_{l,Im} V_{k_1,1,Re} \\ V_{k_2,0,Re} + V_{l,Re} V_{k_2,0,Re} - V_{l,Im} V_{k_2,0,Im} \\ V_{k_2,0,Im} + V_{l,Re} V_{k_2,0,Im} + V_{l,Im} V_{k_2,0,Re} \\ V_{k_2,1,Re} + \cos(2\pi/2^m) F_{Re} - \sin(2\pi/2^m) F_{Im} \\ V_{k_2,1,Im} + \sin(2\pi/2^m) F_{Re} + \cos(2\pi/2^m) F_{Im} \end{bmatrix}, \quad (27)$$

$(F_{Re} = V_{l,Re} V_{k_2,1,Re} - V_{l,Im} V_{k_2,1,Im}, F_{Im} = V_{l,Re} V_{k_2,1,Im} + V_{l,Im} V_{k_2,1,Re})$

Similar to the qubits in Equation (26), the cebits are also divided into three parts labeled as  $k_0, k_1$  and  $k_2$ , where  $k_0$  spans from 1 to  $k_1 - 1$  and  $k_2$  ranges from  $k_1 + 1$  to  $n$ . Here  $V_{l,Re}$  and  $V_{l,Im}$  are externally applied single-frequency cosine and sine signals, respectively. Their frequency is set to match the highest spectral component within the combined spectra of all the voltage signals. By comparing Equation (27) with Equation (14), it can be observed that the fundamental construction schemes of the  $U_{CR}$  gate and the  $U_{CR_m}$  gate are similar, and both are composed of CR modules. In the  $U_{CR}$  gate, each  $k_0$ -th cebit contains 2 CR modules, each  $k_1$ -th contains 1 CR module, and each  $k_2$ -th cebit contains 2 CR modules. Using the definition of the classical states in Equation (22), the result of the  $U_{CR}$  gate corresponds to the  $\hat{U}_{CR}$  gate. The detailed computing process is provided in Method (B).

Using the circuit gates mentioned above, the circuit simulation of the QFT can be realized. As is shown in Figure 2a, the  $n$ -qubit QFT can be implemented using the quantum  $\hat{U}_H$  and  $\hat{U}_{CR_m}$  gates, and the omitted quantum swap gate. By replacing the quantum gates in the quantum circuit with our corresponding circuit designs, the classical circuit simulation is achieved, as is shown in Figure 2b. For visual simplicity, the 4 input signals for each cebit are merged into a single line. In circuit simulation, we omit the swap gates too.



**Figure 2.** a) Quantum circuit for the  $n$ -qubit QFT. b) Classical circuit simulating the  $n$ -qubit QFT.

Now, we briefly describe the QFT simulation in the classical circuit using the classical basic state as an example. Since the definition of the classical states obtained by the voltage signals has been established, we no longer describe the voltage signals, but instead focus solely on the evolution of the classical state. The input classical basic state is expressed as

$$|K\rangle = \left| \overline{K_1 K_2 \dots K_n} \right\rangle = |K_1\rangle \otimes |K_2\rangle \otimes \dots \otimes |K_n\rangle, \quad (28)$$

where the decimal representation  $K$  is rewritten as the binary representation  $\overline{K_1 K_2 \dots K_n}$ .

At first, the  $U_H$  gate acts on the input state as

$$\begin{cases} \frac{|0\rangle + |1\rangle}{\sqrt{2}} \otimes \left| \overline{K_2 \dots K_n} \right\rangle, & K_1 = 0, \\ \frac{|0\rangle - |1\rangle}{\sqrt{2}} \otimes \left| \overline{K_2 \dots K_n} \right\rangle, & K_1 = 1. \end{cases} \quad (29)$$

We rewrite it as

$$\frac{|0\rangle + e^{i2\pi \overline{0.K_1}} |1\rangle}{\sqrt{2}} \otimes \left| \overline{K_2 \dots K_n} \right\rangle. \quad (30)$$

Here we employ the binary fractional notation

$$\overline{0.a_1 a_2 \dots a_n} = \sum_{j=1}^n 2^{-j} a_j. \quad (31)$$

For example,  $\overline{0.K_1} = K_1/2$ .

Next, the  $U_{CR}$  gate acts on the classical state as

$$\frac{|0\rangle + e^{i2\pi \overline{0.K_1 K_2 \dots K_n}} |1\rangle}{\sqrt{2}} \otimes \left| \overline{K_2 \dots K_n} \right\rangle = |K'_1\rangle \otimes \left| \overline{K_2 \dots K_n} \right\rangle \quad (32)$$

The component  $|1\rangle$  of the classical state  $|K_1\rangle$  has a  $2\pi/2^{K_1}$  phase shift controlled by the  $k$ -th cebit, transforming  $|K_1\rangle$  into  $|K'_1\rangle$ . Subsequent gates similarly transform  $|K_2\rangle$  into  $|K'_2\rangle$ , transform  $|K_3\rangle$  into  $|K'_3\rangle$ , and so on, but these gates no longer change the state  $|K'_1\rangle$ . And we have

$$|K'_k\rangle = \frac{|0\rangle + e^{i2\pi \overline{0.K_k K_{k+1} \dots K_n}} |1\rangle}{\sqrt{2}}. \quad (33)$$

After the SWAP gate, the final circuit output is

$$\text{SWAP} \left( \left| \overline{K'_1 K'_2 \dots K'_n} \right\rangle \right) = \left| \overline{K'_n K'_{n-1} \dots K'_1} \right\rangle. \quad (34)$$

Now we consider the amplitude of one basic state  $\overline{|J_1 J_2 \dots J_n\rangle}$ . Each  $J_j$  term induces a phase shift  $\Delta\theta_j = J_j 2\pi \overline{0 \cdot K_{n-j+1} \dots K_n}$ , so the phase shift of  $\overline{|J_1 J_2 \dots J_n\rangle}$  is

$$\begin{aligned} \sum_{j=1}^n \Delta\theta_j &= 2\pi \sum_{j=1}^n \overline{J_j \cdot 0 \cdot K_{n-j+1} \dots K_n} \\ &\equiv 2\pi \sum_{j=1}^n \overline{J_j \cdot 0 \cdot K_{n-j+1} \dots K_n} + 2A\pi \\ &= 2\pi \sum_{j=1}^n \overline{J_j K_1 K_2 \dots K_{n-j} \cdot K_{n-j+1} \dots K_n} \\ &= 2\pi 2^n \sum_{j=1}^n J_j 2^{-j} \sum_{k=1}^n 2^{n-j} 2^{-k} K_k \\ &= 2\pi 2^n \overline{0 \cdot J_1 \dots J_n \cdot 0 \cdot K_1 \dots K_n} \\ &= 2\pi KJ/N. \end{aligned} \quad (35)$$

Here

$$A = \sum_{j=1}^n \overline{J_j K_1 K_2 \dots K_{n-j}} \quad (36)$$

is an integer. The symbol “ $\equiv$ ” in Equation (35) means that the two sides of the symbol differ by an integer multiple of  $2\pi$ , thus they induce identical phase shifts. Also the phase shift in Equation (35) is equivalent to the phase shift in Equation (1). Based on the linear properties of the circuit system, the correspondence to Equation (2) arises naturally, and we successfully realize the QFT simulation in the classical circuit.

We emphasize that the speed-up in QFT arises from quantum entanglement, which enables a single quantum gate to process all information contained in a quantum state in parallel, thereby drastically reducing computing resource demands. Analogously, our circuit design achieves a similar parallel speed-up by introducing a novel definition of the classical states based on correlated voltage signals, emulating classical correlations. This allows a single analog circuit component to efficiently process all information in parallel. For example, in the 2-cebit circuit simulation of QFT, the input classical state

$$|0\rangle \otimes \frac{|0\rangle + |1\rangle}{\sqrt{2}} \quad (37)$$

is transformed into the output state

$$\frac{2|00\rangle + (1-i)|01\rangle + (1+i)|11\rangle}{2\sqrt{2}} \quad (38)$$

which can be further rotated into a classical state  $\frac{|00\rangle+|11\rangle}{\sqrt{2}}$  corresponding to a quantum Bell state  $\frac{|00\rangle+|11\rangle}{\sqrt{2}}$  via two 1-cebit gates acts on the 1-st and the 2-nd cebit respectively

$$\frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \otimes \frac{1}{\sqrt{2}} \begin{bmatrix} 1-i & -1+i \\ 1+i & 1-i \end{bmatrix}. \quad (39)$$

Therefore, it is able to exhibit similar properties analogous to the quantum Bell state. The experimental demonstrations are given in the following section. This result shows the presence of the entanglement-like correlation in the circuit system, and reveals the intrinsic source of the speed-up effect in our circuit simulation scheme.

At the end of this section, we discuss the computational complexity of our circuit design. In quantum system, computational complexity is considered proportional to the number of quantum gates. Similarly in classical system, computational complexity should depend on the number of basic computing components in the circuit. However, we emphasize that multiple circuit components can be integrated into a single component, and such an integrated component clearly cannot be regarded as a basic computing component. Therefore, to start it, we need to define the basic computing component in our circuit design.

The definition of the basic computing component is based on the mathematical operations it performs. In our circuit design, we only use 3 kinds of basic computing components. The first is the wire, performing copy operation that maps one function  $f$  into two identical functions  $f$ . The second is the analog adder, performing addition (subtraction) operation that maps two functions  $f_1$  and  $f_2$  into one function  $f_1 \pm f_2$ . The last is the analog multiplier, performing a multiplication operation that maps two functions  $f_1$  and  $f_2$  into one function  $f_1 \times f_2$ . Thus, the computational complexity in our circuit design is determined by the number of the basic computing components employed.

Our  $n$ -cebit circuit design consists of  $n$   $U_H$  gate and  $n-1$   $U_{CR}$  gate. Each  $U_H$  gate contains 4 analog adders, while each  $U_{CR}$  gate contains  $O(n)$  analog multipliers and  $O(n)$  analog adders. Consequently, an  $n$ -cebit simulation circuit requires a total of  $O(n^2)$  fundamental analog circuit components. This matches the  $O(n^2)$  quantum gates needed for the  $n$ -qubit QFT quantum circuit, and outperforms the  $O(n2^n) = O(N \log N)$  elementary operations of FFT.

After comparing the algorithm complexity among the circuit scheme, QFT and FFT, we additionally consider the processing time required per individual circuit component to compare these FT scheme in terms of process time. In our design, a circuit component operates on the voltage signals composed of sine and cosine voltage signals of different frequencies. The period of the voltage signals is denoted as  $T = 2\pi/\omega$  as is in the above text, where the frequency  $\omega$  is a fixed parameter set before the circuit is built. Although the output signal of the circuit component contains more frequency signals, its period remains  $T$ . According to Equation (22), we only need to extract a signal segment of duration  $T$  from each voltage signal to perform computation. The voltage signal outside the interval from time 0 to time  $T$  is redundant and should not be counted in the processing time. Consequently, the total complexity of this circuit design can be calculated as the processing time  $T$  required by the circuit components multiplied by the algorithm complexity  $O(n^2)$ , and its order remains at the order of  $O(n^2)$ . That is, the computation time of this circuit design scales proportionally with the hardware complexity of the circuit.

In next section, we present several circuit simulation experiments of simulating QFT to validate the correctness of our circuit design. We also experimentally verify the existence of the correspondence between the classical correlation within the designed circuit and the quantum entanglement in the quantum system.

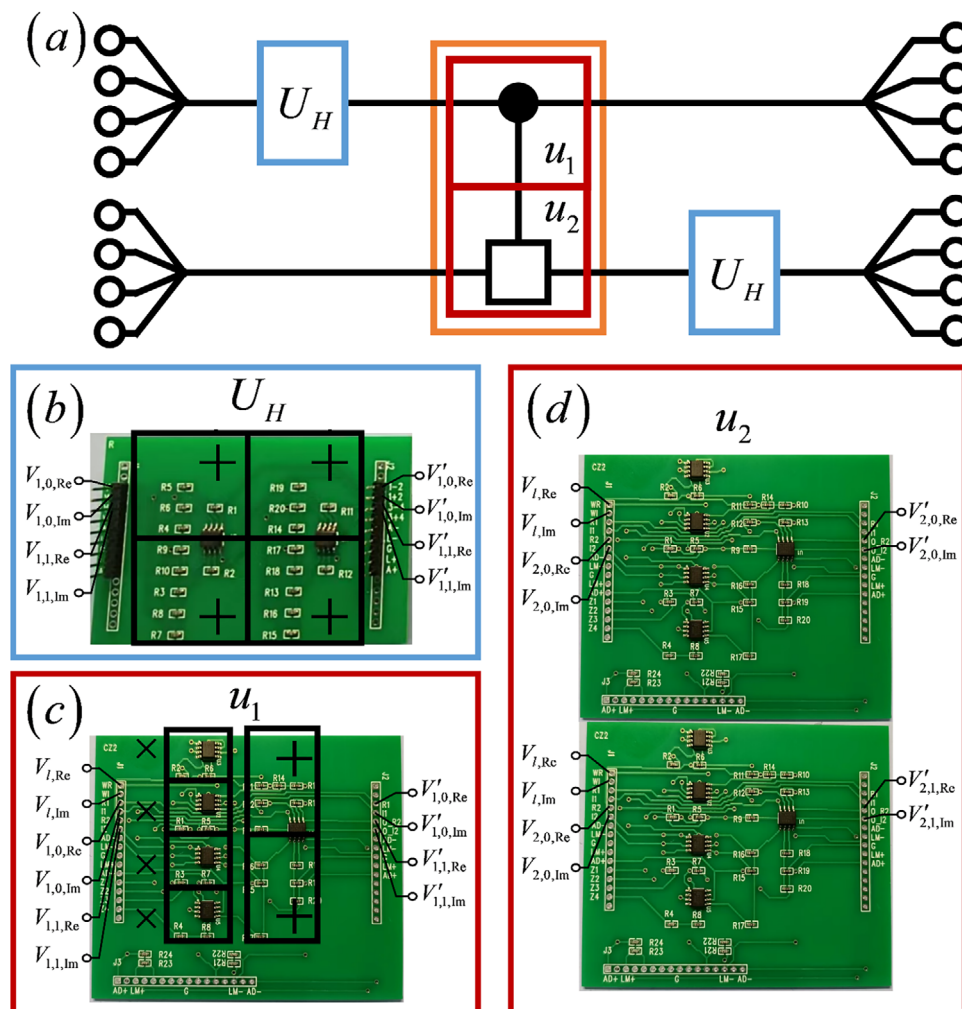


Figure 3. a) The schematic diagram of the 2-qubit simulation circuit. b) The PCB layouts for the  $U_H$  gate. c,d) The PCB layouts for the  $U_{CR_2}$  gate.

### 3. Experimental Demonstration of the Circuit Simulation for QFT

We begin with the circuit simulation of the 2-qubit QFT. The schematic diagram of the 2-qubit simulation circuit is shown in Figure 3a, consisting of 2  $U_H$  gates and 1  $U_{CR_2}$  gate. The  $U_{CR_2}$  gate includes 2 submodules  $u_1$  and  $u_2$  (marked by the red boxes). The  $u_1$  submodule acts on the control qubit and contains 1 CR module, while the  $u_2$  submodule acts on the target qubit and contains 2 CR modules. The corresponding PCB layouts for these circuit gates are provided in Figure 3b–d. On the PCB boards, we mark the adder modules by “+” and the multiplier modules by “×”, consistent with the designs in Figure 1b,d. In these modules, the operational amplifiers used are model LM358, with each LM358 chip integrating 2 operational amplifiers. The analog multipliers employed are model AD633. The initial voltage signals in the experiment are generated using an FY2300 signal generator.

We validate our circuit design using the following 5 input states in the 2-qubit system. These input states correspond to the initial voltage signal configurations listed below (voltage unit is  $V$ , and  $\omega$  is set to 1kHz).

$$|00\rangle : \begin{cases} V_{1,0,Re} = V_{2,0,Re} = \cos(\omega t), \\ V_{1,0,Im} = V_{2,0,Im} = \sin(\omega t), \\ V_{1,1,Re} = V_{1,1,Im} = V_{2,1,Re} = V_{2,1,Im} = 0, \end{cases} \quad (40)$$

$$|01\rangle : \begin{cases} V_{1,0,Re} = V_{2,1,Re} = \cos(\omega t), \\ V_{1,0,Im} = V_{2,1,Im} = \sin(\omega t), \\ V_{1,1,Re} = V_{1,1,Im} = V_{2,0,Re} = V_{2,0,Im} = 0, \end{cases} \quad (41)$$

$$|10\rangle : \begin{cases} V_{1,0,Re} = V_{1,0,Im} = V_{2,1,Re} = V_{2,1,Im} = 0, \\ V_{1,1,Re} = V_{2,0,Re} = \cos(\omega t), \\ V_{1,1,Im} = V_{2,0,Im} = \sin(\omega t), \end{cases} \quad (42)$$

$$|11\rangle : \begin{cases} V_{1,0,Re} = V_{1,0,Im} = V_{2,0,Re} = V_{2,0,Im} = 0, \\ V_{1,1,Re} = V_{2,1,Re} = \cos(\omega t), \\ V_{1,1,Im} = V_{2,1,Im} = \sin(\omega t), \end{cases} \quad (43)$$

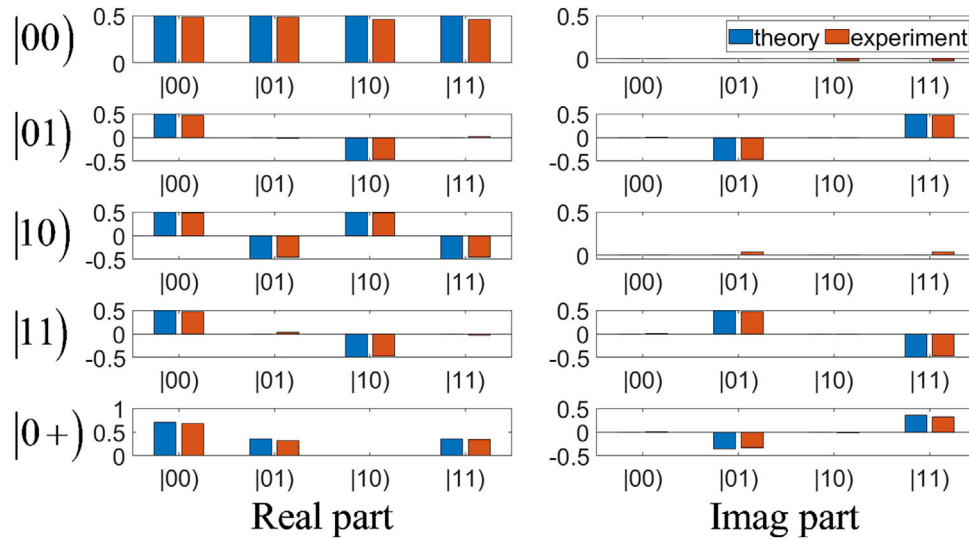


Figure 4. The theoretical and experimental results of the circuit simulation of the 2-qubit QFT.

$$|0+\rangle : \begin{cases} V_{1,0,Re} = \cos(\omega t), \\ V_{1,0,Im} = \sin(\omega t), \\ V_{1,1,Re} = V_{1,1,Im} = 0, \\ V_{2,0,Re} = V_{2,1,Re} = \cos(\omega t) / \sqrt{2}, \\ V_{2,0,Im} = V_{2,1,Im} = \sin(\omega t) / \sqrt{2}, \end{cases} \quad (44)$$

where we define

$$|+\rangle = \frac{|0\rangle + |1\rangle}{\sqrt{2}}, |-\rangle = \frac{|0\rangle - |1\rangle}{\sqrt{2}}, |L\rangle = \frac{|0\rangle + i|1\rangle}{\sqrt{2}}, |R\rangle = \frac{|0\rangle - i|1\rangle}{\sqrt{2}}. \quad (45)$$

The theoretical and experimental results are provided in Figure 4. From top to bottom, the panels correspond to the input states  $|00\rangle$ ,  $|10\rangle$ ,  $|01\rangle$ ,  $|11\rangle$  and  $|0+\rangle$ . The left column displays the real parts of the results, while the right column displays the imaginary parts. The horizontal axis represents the states, while the vertical axis represents the amplitudes. The blue bar plots represent the theoretical results of QFT

$$|00\rangle \xrightarrow{\text{QFT}} \frac{|00\rangle + |01\rangle + |10\rangle + |11\rangle}{2}, \quad (46)$$

$$|01\rangle \xrightarrow{\text{QFT}} \frac{|00\rangle - i|01\rangle - |10\rangle + i|11\rangle}{2}, \quad (47)$$

$$|10\rangle \xrightarrow{\text{QFT}} \frac{|00\rangle - |01\rangle + |10\rangle - |11\rangle}{2}, \quad (48)$$

$$|11\rangle \xrightarrow{\text{QFT}} \frac{|00\rangle + i|01\rangle - |10\rangle - i|11\rangle}{2}, \quad (49)$$

$$|0+\rangle \xrightarrow{\text{QFT}} \frac{2|00\rangle + (1-i)|01\rangle + (1+i)|11\rangle}{2\sqrt{2}}, \quad (50)$$

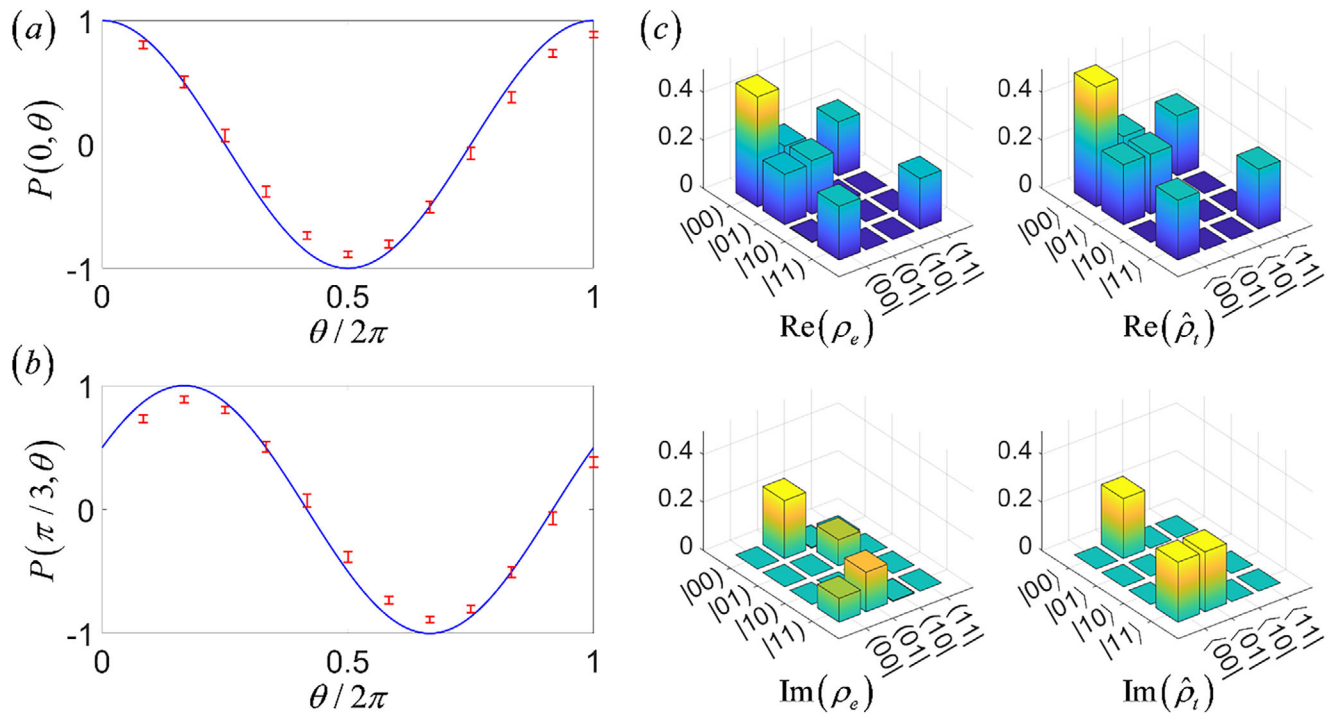
while the orange bar plots represent the experimental results, consistent with the theoretical results. Among these classical states, the mathematical form of Equation (50) corresponds to the quantum entangled state  $\frac{2|00\rangle + (1-i)|01\rangle + (1+i)|11\rangle}{2\sqrt{2}}$ . That is, our constructed classical correlation in circuits is a concept different from the quantum correlations that are generally believed to exist only in quantum systems, but their mathematical forms are the same. In fact, not only do they have the same mathematical form, but they can also exhibit similar physical properties.

It is well known that there are typically two approaches to characterize the quantum correlations of entangled states, one using violation of the Bell inequality and the other using entanglement entropy. Similarly, the correlation properties of our constructed classical correlated states in circuits can also be tested by two corresponding ways. We first discuss the circuit version of the violation of the Bell inequality. Its adaptation requires projective measurements on the state corresponding to the Bell-like state along three directions  $\theta_1, \theta_2$ , and  $\theta_3$ , and substitute the measurements into the classical version of the Bell-like inequality

$$|P(\theta_1, \theta_2) - P(\theta_1, \theta_3)| \leq 1 - P(\theta_2, \theta_3) \quad (51)$$

where  $P(\theta_1, \theta_2)$  represents the correlated measurement outcome when the first qubit is measured along  $\theta_1$  and the second qubit along  $\theta_2$ . In traditional classical systems, this inequality cannot be violated.

In our circuit experiment, we first rotate the output state of the input state  $|0+\rangle$  into a classical state corresponding to the quantum Bell-like state via two 1-qubit gate described in Equation (39), and subsequently perform Bell-like inequality measurements on the classical state corresponding to the quantum Bell state. Figure 5a,b show the variation of  $P(\theta', \theta)$  with  $\theta$  under different parameter  $\theta'$ . For parameters  $\theta_1 = 0$ ,  $\theta_2 = \pi/3$  and  $\theta_3 = 2\pi/3$ , we obtain  $P(\theta_1, \theta_2) = 0.51$ ,  $P(\theta_1, \theta_3) = -0.39$  and  $P(\theta_2, \theta_3) = 0.51$ . Consequently, the inequality in Equation (51) is violated. This means that although our constructed classical correlation in circuits is the concept different from the quantum correlations,



**Figure 5.** a,b) The variation of the correlated measurement outcomes  $P(\theta', \theta)$  with  $\theta$  under different parameter  $\theta'$ . The blue line represents the theoretical results, while the red error bars represent the experimental results. c) The classical density matrix of the output classical state when the input classical state is  $|0+\rangle$  and the corresponding quantum density matrix. From left to right, the subfigures represent the real part of the classical density matrix of the experimental results, the real part of the quantum density matrix of the theoretical results, the imaginary part of the classical density matrix of the experimental results and the imaginary part of the quantum density matrix of the theoretical results.

it has a correlation relationship corresponding to the quantum correlations.

Now, we analyze the circuit version of the entanglement entropy. Its classical version requires the density matrix, which can be obtained through state tomography. The mathematical framework of state tomography remains unchanged, where projective measurements on the output state are performed on 4 states  $|0\rangle$ ,  $|1\rangle$ ,  $|+\rangle$  and  $|L\rangle$  for each qubit and the density matrix of the output state can then be reconstructed from these projective measurements results. However, these projective measurement operations require adaptation for classical implementation. In our circuit design, the correspondence to projective measurements can be divided into two steps, the correspondence to projection and to the measurement. The 1-qubit gate rotations implement the projection step, for example, the  $U_H$  gate projects  $|0\rangle$  to  $|+\rangle$  and  $|1\rangle$  to  $|-\rangle$ . And the operation that defines the classical states by the voltage signals corresponds to the measurement step, for example, the amplitude  $\varphi'_{00} = 1/2$  in Equation (46) indicates that the measured amplitude of the output voltage signal projected to  $|00\rangle$  state is  $1/2$ . Figure 5c presents the experimentally reconstructed classical density matrix  $\rho_e$  and the corresponding theoretical quantum density matrix  $\hat{\rho}_t$ . From left to right, the subfigures represent the real part of the classical density matrix of the experimental results, the real part of the quantum density matrix of the theoretical results, the imaginary part of the classical density matrix of the experimental results and the imaginary part of the quantum density matrix of the theoretical results.

Using the classical density matrix  $\rho_e$  of the output state, we compute the reduced classical density matrix  $\rho_{e,1}$  and calculate the classical correlation corresponding to the quantum entanglement entropy

$$S(\rho_e) = -\text{Tr}(\rho_{e,1} \ln \rho_{e,1}) = 0.75 = S(\hat{\rho}_t) \Rightarrow 0. \quad (52)$$

These results also support the correspondence between the classical correlation among classical states of the electric circuits and the quantum entanglement in the quantum system.

Based on the correspondence between classical correlation and quantum entanglement, our circuit design can be extended to scenarios with more qubits. We demonstrate the scalability of our circuit design through the two examples, the circuit simulation of 3-qubit QFT and the theoretical simulation of 5-qubit QFT. Figure 6 shows the schematic diagram of the 3-qubit simulation circuit, which consists of 3  $U_H$  gates and 2  $U_{CR}$  gates. The first  $U_{CR}$  gate consists of 3 submodules called  $u_1, u_2$  and  $u_3$ , the second  $U_{CR}$  gate consists of  $u_4, u_5$  and  $u_6$ . The submodules  $u_1$  and  $u_5$  act on the control qubit, containing 1 CR module. The submodules  $u_2, u_3$  and  $u_6$  act on the target qubit, containing 2 CR modules. And the submodule  $u_4$  acts on the other qubit, containing 2 CR modules. The PCB layouts for these CR modules share a similar design with the PCB layouts shown in Figure 3c,d, but their specific configurations differ, as is shown in Method (B).

Theoretically, our 3-qubit circuit is able to simulate the 3-qubit QFT for arbitrary input states. For testing purposes, we arbitrarily selected a 3-qubit state

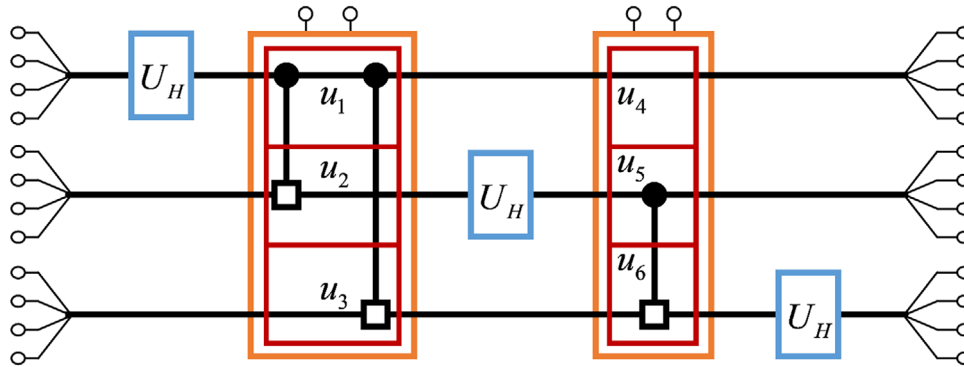


Figure 6. The schematic diagram of the 3-qubit simulation circuit.

$$|\varphi\rangle = \begin{bmatrix} 0.38 + 0.38i \\ 0.61 + 0.59i \end{bmatrix} \otimes \begin{bmatrix} 0.53 + 0.31i \\ 0.66 + 0.43i \end{bmatrix} \otimes \begin{bmatrix} 0.24 + 0.65i \\ 0.61 + 0.38i \end{bmatrix}$$

$$= \begin{bmatrix} -0.19 + 0.13i \\ -0.01 + 0.23i \\ -0.25 + 0.16i \\ -0.10 + 0.29i \\ -0.29 + 0.21i \\ -0.11 + 0.36i \\ -0.39 + 0.25i \\ -0.16 + 0.45i \end{bmatrix} \quad (53)$$

$$\begin{bmatrix} V_{2,0,Re} \\ V_{2,0,Im} \\ V_{2,1,Re} \\ V_{2,1,Im} \end{bmatrix} = \begin{bmatrix} 0.53 \cos(\omega t) - 0.31 \sin(\omega t) \\ 0.31 \cos(\omega t) + 0.53 \sin(\omega t) \\ 0.66 \cos(\omega t) - 0.43 \sin(\omega t) \\ 0.43 \cos(\omega t) + 0.66 \sin(\omega t) \end{bmatrix}, \quad (55)$$

$$\begin{bmatrix} V_{3,0,Re} \\ V_{3,0,Im} \\ V_{3,1,Re} \\ V_{3,1,Im} \end{bmatrix} = \begin{bmatrix} 0.24 \cos(\omega t) - 0.65 \sin(\omega t) \\ 0.65 \cos(\omega t) + 0.24 \sin(\omega t) \\ 0.61 \cos(\omega t) - 0.38 \sin(\omega t) \\ 0.38 \cos(\omega t) + 0.61 \sin(\omega t) \end{bmatrix}. \quad (56)$$

It corresponds to following initial voltage configuration (voltage unit is V, and  $\omega$  is set to 1kHz)

$$\begin{bmatrix} V_{1,0,Re} \\ V_{1,0,Im} \\ V_{1,1,Re} \\ V_{1,1,Im} \end{bmatrix} = \begin{bmatrix} 0.38 \cos(\omega t) - 0.38 \sin(\omega t) \\ 0.38 \cos(\omega t) + 0.38 \sin(\omega t) \\ 0.61 \cos(\omega t) - 0.59 \sin(\omega t) \\ 0.59 \cos(\omega t) + 0.61 \sin(\omega t) \end{bmatrix}, \quad (54)$$

The theoretical and experimental results are provided in Figure 7. The top subfigure displays the real parts of the results, while the bottom subfigure displays the imaginary parts of the results. The horizontal axis represents the states, with the vertical axis representing the amplitudes. The blue bar plots represent the theoretical results of QFT, and the orange bar plots represent the experimental results, consistent with the theoretical results.

Similarly, Figure 8 displays the schematic diagram of the 5-qubit simulation circuit. As discussed above, each circuit gate

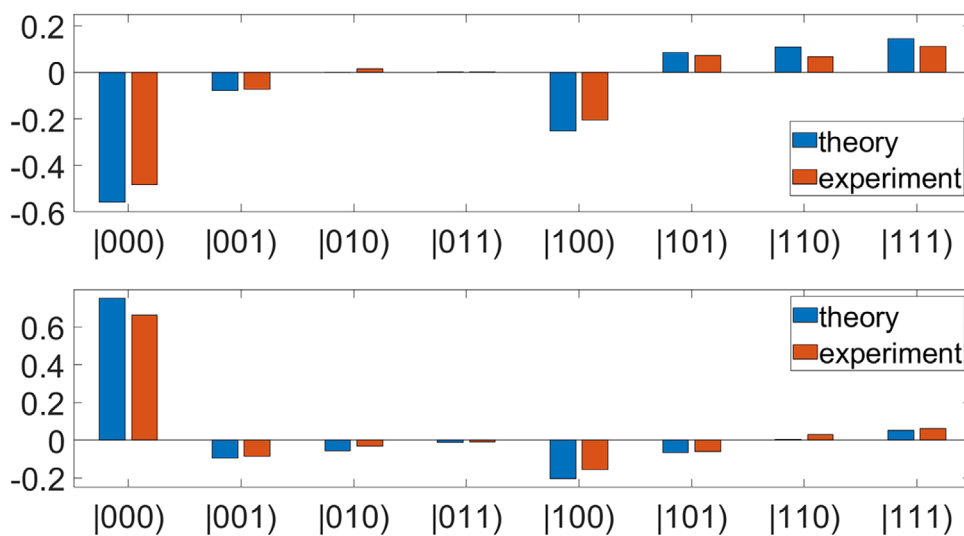


Figure 7. The theoretical and experimental results of the circuit simulation of the 3-qubit QFT.

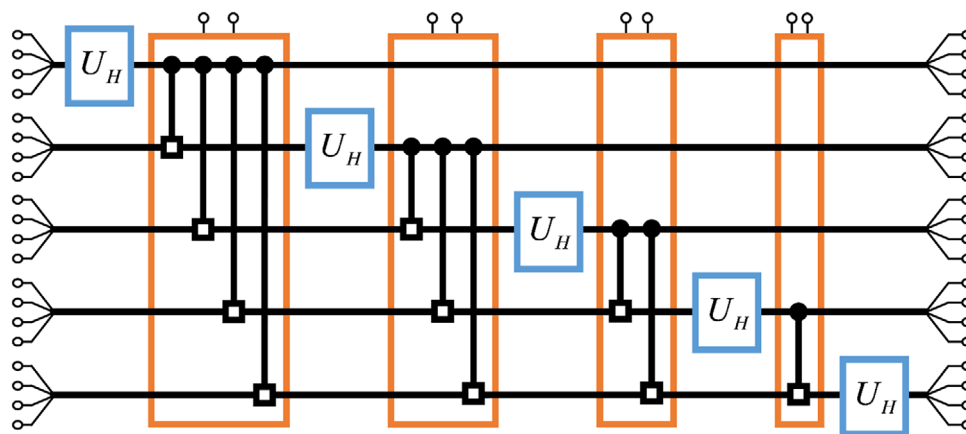


Figure 8. The schematic diagram of the 5-qubit simulation circuit.

(blue and orange boxes) contains polynomial number of basic computing components. In this theoretical simulation, we arbitrarily select a 5-qubit state

$$|\varphi\rangle = \begin{bmatrix} 0.37 + 0.20i \\ 0.63 + 0.65i \end{bmatrix} \otimes \begin{bmatrix} 0.21 + 0.58i \\ 0.65 + 0.44i \end{bmatrix} \otimes \begin{bmatrix} 0.56 + 0.60i \\ 0.35 + 0.46i \end{bmatrix} \otimes \begin{bmatrix} 0.59 + 0.03i \\ 0.46 + 0.66i \end{bmatrix} \otimes \begin{bmatrix} 0.37 + 0.26i \\ 0.67 + 0.59i \end{bmatrix}. \quad (57)$$

The theoretical results and the simulation results are provided in Figure 9, with the accuracy of the circuit components configured to 1%. The top subfigure displays the real parts of the results, while the bottom subfigure displays the imaginary parts of the results. The horizontal axis represents the index of the states, with the vertical axis representing the amplitudes. The blue bar plots represent the theoretical results of QFT, and the orange bar plots represent the simulation results, consistent with the theoretical results.

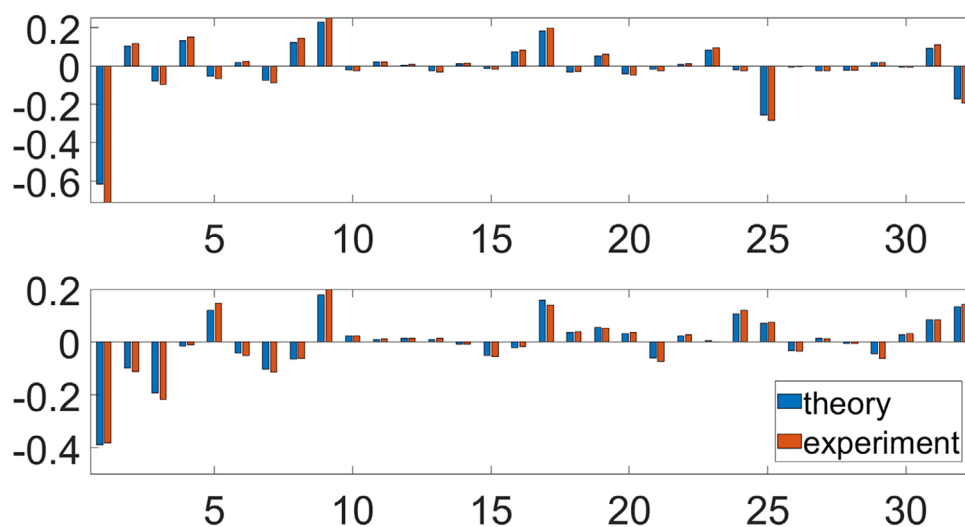


Figure 9. The theoretical results and the simulation results of the circuit simulation of the 5-qubit QFT.

#### 4. Discussion and Conclusion

We have realized the circuit simulation of QFT, where the number of the basic computing components required in our circuit design matches that of quantum gates in the quantum circuit. The correctness of the 2-qubit, 3-qubit and 5-qubit circuit simulation schemes has been validated. We summarize the principles underlying the speedup achieved by our simulation scheme as follows.

First, based on previous researches on classical correlation, we employ the correlated circuit wave systems as the experimental platform, which provides the foundation for demonstrating classical correlation in the systems. Second, we have successfully developed a novel definition of the classical states by the voltage signals, which mathematically corresponds to quantum entanglement, establishing the theoretical basis for our experiments. Within this scheme, a single computing component, processes all information in the waveform across one circuit channels, as one operation, enabling parallel computation over the

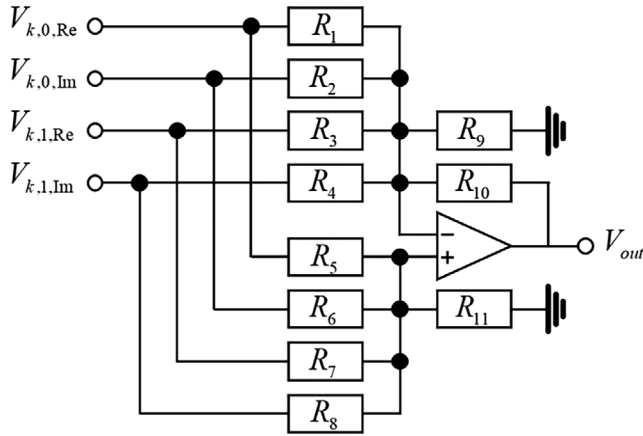


Figure 10. The circuit design of the arbitrarily 1-cebit gate.

entire dataset and thereby generating speedup. Notably, this parallel speedup relies on the existence of the novel classical correlations, thus traditional classical computing systems lacking such correlations cannot achieve this speedup. In traditional classical algorithms, significant time is consumed by operations such as permutation and selection within the input data itself. In contrast, the scheme presented in this work eliminates the need for any internal manipulation of the input data, requiring only global operations in the entire dataset.

Leveraging the mature, stable, and scalable nature of circuit platforms, our quantum-inspired computing scheme based on circuit holds the potential to circumvent the challenges faced by quantum platforms and open a new way toward advanced information processing with high quality and efficiency. Furthermore, our work highlights the significant potential of analog computing in parallel speedup, which can be further optimized to realize practical speedup effects.

## 5. Experimental Section

*The Detailed Circuit Design of 1-Cebit Gate (Adder Module):* The 1-cebit gate is an important basic gate in circuit design, and here the detailed design of the arbitrarily 1-cebit gate is illustrated. It consists of 4 adder modules shown in Figure 10. Each adder module contains 4 inputs, 1 operational amplifier, at most 11 resistors, and 1 output. The add module is referred to as “add circuit”, performing weighted addition (and subtraction) operations on the input voltage signals.

According to Kirchhoff's law,

$$0 = \frac{V_- - V_{k,0,Re}}{R_1} + \frac{V_- - V_{k,0,Im}}{R_2} + \frac{V_- - V_{k,1,Re}}{R_3} + \frac{V_- - V_{k,1,Im}}{R_4} + \frac{V_-}{R_9} + \frac{V_- - V_{out}}{R_{10}} + I_{-,in} \quad (58)$$

$$0 = \frac{V_+ - V_{k,0,Re}}{R_5} + \frac{V_+ - V_{k,0,Im}}{R_6} + \frac{V_+ - V_{k,1,Re}}{R_7} + \frac{V_+ - V_{k,1,Im}}{R_8} + \frac{V_+}{R_{11}} + I_{+,in} \quad (59)$$

is observed. Subsequently, by combining the properties of operational amplifier that

$$V_- = V_+, I_{-,in} = I_{+,in} = 0, \quad (60)$$

is obtained

$$V_{out} = \left( \frac{k}{R_5} - \frac{1}{R_1} \right) V_{k,0,Re} + \left( \frac{k}{R_6} - \frac{1}{R_2} \right) V_{k,0,Im} + \left( \frac{k}{R_7} - \frac{1}{R_3} \right) V_{k,1,Re} + \left( \frac{k}{R_8} - \frac{1}{R_4} \right) V_{k,1,Im}, \quad (61)$$

where

$$k = R_{10} \frac{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_9} + \frac{1}{R_{10}}}{\frac{1}{R_5} + \frac{1}{R_6} + \frac{1}{R_7} + \frac{1}{R_8} + \frac{1}{R_{11}}} \quad (62)$$

By adjusting the resistance values,  $V_{out}$  can be configured as an arbitrary linear superposition of the inputs, thereby realizing any 1-cebit gate. For example, in a 4-input 4-output circuit, the resistance values are adjusted for output  $V'_{1,0,Re}$  to (the resistance unit is  $k\Omega$ )

$$R_5 = R_7 = 5\sqrt{2}, R_9 = \frac{10}{2\sqrt{2}-1}, R_{10} = 10. \quad (63)$$

Resistors not explicitly mentioned are disconnected from the circuit, and

$$V'_{1,0,Re} = \frac{V_{1,0,Re} + V_{1,1,Re}}{\sqrt{2}} \quad (64)$$

is observed. Similar configurations are applied to the remaining 3 outputs

$$V'_{1,0,Im} : R_6 = R_8 = 5\sqrt{2}, R_9 = \frac{10}{2\sqrt{2}-1}, R_{10} = 10, \quad (65)$$

$$V'_{1,1,Re} : R_3 = R_5 = 5\sqrt{2}, R_{10} = R_{11} = 10, \quad (66)$$

$$V'_{1,1,Im} : R_4 = R_6 = 5\sqrt{2}, R_{10} = R_{11} = 10. \quad (67)$$

Resistors not explicitly mentioned are disconnected from the circuit, and the  $U_H$  gate is obtained

$$\begin{bmatrix} V'_{1,0,Re} \\ V'_{1,0,Im} \\ V'_{1,1,Re} \\ V'_{1,1,Im} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} V_{1,0,Re} + V_{1,1,Re} \\ V_{1,0,Im} + V_{1,1,Im} \\ V_{1,0,Re} - V_{1,1,Re} \\ V_{1,0,Im} - V_{1,1,Im} \end{bmatrix} \quad (68)$$

In the experiment circuit, specific resistance values can be achieved through rounding and series-parallel combinations of resistors.

Furthermore, this adder module can be extended to contain any number of input signals, with the output equaling the weighted sum of all inputs. Since the underlying principle remains consistent, further elaboration is omitted here.

In the last, the detailed calculation for the 1-cebit gate  $U_H$ , and the arbitrary 1-cebit gate  $U_R$ , in  $n$ -cebit system are discussed. The  $U_H$  gate on the  $k_0$ -thcebit transforms the voltage signals into

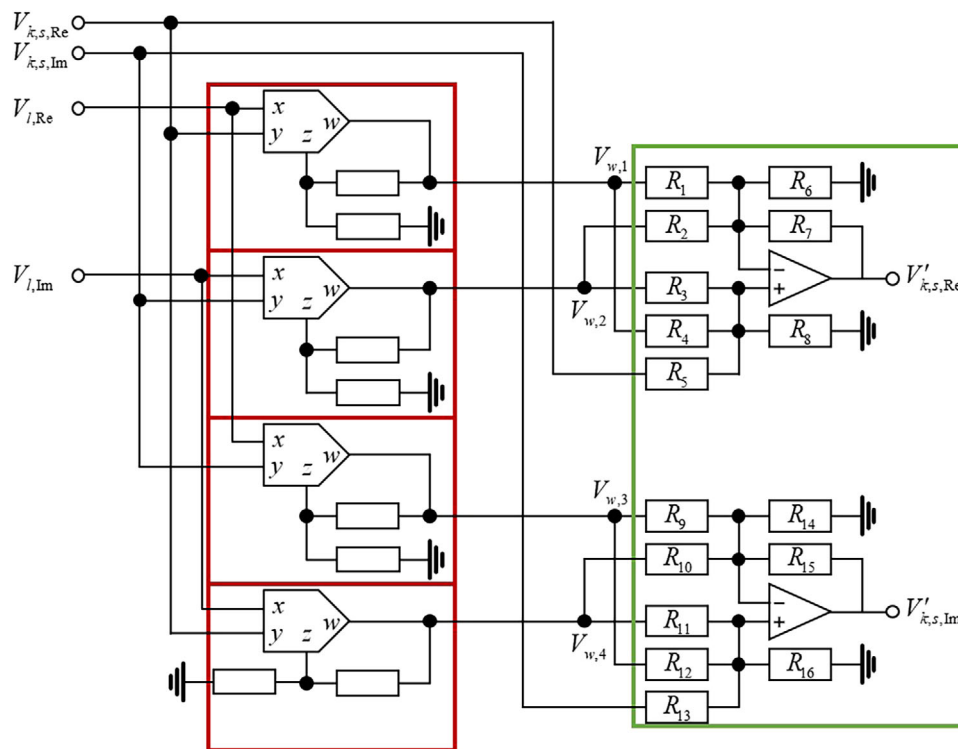


Figure 11. The circuit design of one certain CR module. It consists of analog multipliers (red box) and adder modules (green box).

$$\begin{cases} \begin{bmatrix} V'_{k,0,Re} \\ V'_{k,0,Im} \\ V'_{k,1,Re} \\ V'_{k,1,Im} \end{bmatrix} = \begin{bmatrix} a_1 V_{k,0,Re} - b_1 V_{k,0,Im} + a_2 V_{k,1,Re} - b_2 V_{k,1,Im} \\ b_1 V_{k,0,Re} + a_1 V_{k,0,Im} + b_2 V_{k,1,Re} + a_2 V_{k,1,Im} \\ a_3 V_{k,0,Re} - b_3 V_{k,0,Im} + a_4 V_{k,1,Re} - b_4 V_{k,1,Im} \\ b_3 V_{k,0,Re} + a_3 V_{k,0,Im} + b_4 V_{k,1,Re} + a_4 V_{k,1,Im} \end{bmatrix}, & k = k_0, \\ \begin{bmatrix} V'_{k,0,Re} \\ V'_{k,0,Im} \\ V'_{k,1,Re} \\ V'_{k,1,Im} \end{bmatrix} = \begin{bmatrix} V_{k,0,Re} \\ V_{k,0,Im} \\ V_{k,1,Re} \\ V_{k,1,Im} \end{bmatrix}, & k \neq k_0. \end{cases} \quad (69)$$

where  $a_1$  to  $a_4$  and  $b_1$  to  $b_4$  are adjustable circuit parameter. This expression is the result of extending Equation (6) to the  $n$ -qubit system. Using the  $n$ -qubit definition of the classical states in Equation (22), is observe

$$\begin{aligned} \varphi'_{s_{k_0}=0} &= \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \left( \prod_{l \neq k}^n * (V'_{k,s_k,Re} + iV'_{k,s_k,Im}) \right) \\ &\quad * (V'_{k_0,0,Re} + iV'_{k_0,0,Im}) \\ &= \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \left( \prod_{l \neq k}^n * (V_{k,s_k,Re} + iV_{k,s_k,Im}) \right) \\ &\quad * \left( (a_1 + ib_1) V_{k_0,0,Re} + i(a_1 + ib_1) V_{k_0,0,Im} \right) \\ &\quad + \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \left( \prod_{l \neq k}^n * (V_{k,s_k,Re} + iV_{k,s_k,Im}) \right) \\ &\quad * \left( (a_2 + ib_2) V_{k_0,1,Re} + i(a_2 + ib_2) V_{k_0,1,Im} \right) \\ &= (a_1 + ib_1) \varphi_{s_{k_0}=0} + (a_2 + ib_2) \varphi_{s_{k_0}=1}, \end{aligned} \quad (70)$$

$$\varphi'_{s_{k_0}=1} = (a_3 + ib_3) \varphi_{s_{k_0}=0} + (a_4 + ib_4) \varphi_{s_{k_0}=1}, \quad (71)$$

is observed, namely

$$\begin{bmatrix} \varphi'_{s_{k_0}=0} \\ \varphi'_{s_{k_0}=1} \end{bmatrix} = \begin{bmatrix} (a_1 + ib_1) \varphi_{s_{k_0}=0} + (a_2 + ib_2) \varphi_{s_{k_0}=1} \\ (a_3 + ib_3) \varphi_{s_{k_0}=0} + (a_4 + ib_4) \varphi_{s_{k_0}=1} \end{bmatrix}, \quad (72)$$

where  $\varphi_{s_{k_0}=0}$  should be understood as selecting the components where the subscript  $s_{k_0} = 0$  from the entire set of  $\varphi_{s_1 s_2 \dots s_n}$ , and then forming a column vector composed of these selected components. And so are  $\varphi_{s_{k_0}=1}$ .

The computing details of the 4-input 1-input adder module are discussed. It can be simply extended to scenarios with additional inputs and outputs.

*The Detailed Circuit Design and the Output Calculation of CR Module:* The controlled phase gate  $U_{CR_m}$  (and  $U_{CR}$ ) are another kind of important basic gate in the design of circuit. This kind of gate consists of CR modules, and here the detailed design of the CR modules is illustrated. Figure 11 shows one simple CR module, that contains 4 inputs, 4 analog multiplier, 2 operational amplifier, 24 resistors (8 in red box and 16 in green box) and 2 output.

Here  $s = 0$  or  $1$ , and the red box marks the fixed structure of the analog multiplier, with the output

$$\begin{bmatrix} V_{w,1} \\ V_{w,2} \\ V_{w,3} \\ V_{w,4} \end{bmatrix} = \begin{bmatrix} V_{l,Re} V_{k,s,Re} \\ V_{l,Im} V_{k,s,Im} \\ V_{l,Re} V_{k,s,Im} \\ V_{l,Im} V_{k,s,Re} \end{bmatrix}. \quad (73)$$

The red box marks the adder modules, with the output

$$V'_{k,s,Re} = V_{k,s,Re} + C_1 V_{w,1} + C_2 V_{w,2} \quad (74)$$

where  $C_1$  and  $C_2$  depend on the resistance values. If the resistance values are adjusted to

$$R_2 = R_4 = R_5 = R_7 = R_{11} = R_{12} = R_{13} = R_{15} = 10, R_{14} = 5, \quad (75)$$

and resistors not explicitly mentioned are disconnected from the circuit, then

$$\begin{aligned} \begin{bmatrix} V'_{k,s,Re} \\ V'_{k,s,Im} \end{bmatrix} &= \begin{bmatrix} V_{k,s,Re} + V_{w,1} - V_{w,2} \\ V_{k,s,Re} + V_{w,3} + V_{w,4} \end{bmatrix} \\ &= \begin{bmatrix} V_{k,s,Re} + V_{l,Re} V_{k,s,Re} - V_{l,Im} V_{k,s,Im} \\ V_{k,s,Re} + V_{l,Re} V_{k,s,Im} + V_{l,Im} V_{k,s,Re} \end{bmatrix}. \end{aligned} \quad (76)$$

is observed. Take  $k = 1$  and  $s = 1$ , and  $V'_{1,1,Re}$  in the main text in Equation (14) is achieved. By adjusting the resistance values and the circuit connection, the voltage signals transformation in Equations (14) and (27) can be achieved. More generally, it can be achieved

$$\begin{cases} V'_{k,s,Re} = C_1 V_{k,s,Re} + C_2 V_{l,Re} V_{k,s,Re} + C_3 V_{l,Re} V_{k,s,Im} \\ \quad + C_4 V_{l,Im} V_{k,s,Re} + C_5 V_{l,Im} V_{k,s,Im}, \\ V'_{k,s,Im} = C_6 V_{k,s,Im} + C_7 V_{l,Re} V_{k,s,Re} + C_8 V_{l,Re} V_{k,s,Im} \\ \quad + C_9 V_{l,Im} V_{k,s,Re} + C_{10} V_{l,Im} V_{k,s,Im}, \end{cases} \quad (77)$$

where the coefficients  $C$  depend on the resistance values in the adder module.

In the last, it is demonstrated that the output classical states of the  $U_{CR}$  gate correspond to the results of quantum  $\hat{U}_{CR}$  gate. In the  $k$ -th cebit, suppose that  $V_{k,s,Re}$  and  $V_{k,s,Im}$  consists of sine waves and cosine waves with  $W$  different frequencies

$$\begin{bmatrix} V_{k,s,Re} \\ V_{k,s,Im} \end{bmatrix} = \sum_{w=1}^W \begin{bmatrix} A_{k,s,Re,w} \cos(\omega t) - B_{k,s,Im,w} \sin(\omega t) \\ A_{k,s,Re,w} \sin(\omega t) + B_{k,s,Im,w} \cos(\omega t) \end{bmatrix}, \quad (78)$$

or equivalently expressed as

$$V_{k,s,Re} + iV_{k,s,Im} = \sum_{w=1}^W (A_{k,s,Re,w} + iB_{k,s,Im,w}) e^{i\omega t}. \quad (79)$$

And the fixed inputs in the multiplier module are set as

$$V_{l,Re} = \cos(W\omega t), V_{l,Im} = \sin(W\omega t). \quad (80)$$

The output voltage signals of the  $k_1$ -th cebit are

$$\begin{aligned} \begin{bmatrix} V'_{k_1,0,Re} \\ V'_{k_1,0,Im} \\ V'_{k_1,1,Re} \\ V'_{k_1,1,Im} \end{bmatrix} &= \begin{bmatrix} V_{k_1,0,Re} \\ V_{k_1,0,Im} \\ V_{l,Re} V_{k_1,1,Re} - V_{l,Im} V_{k_1,1,Im} \\ V_{l,Re} V_{k_1,1,Im} + V_{l,Im} V_{k_1,1,Re} \end{bmatrix} \\ &= \sum_{w=1}^W \begin{bmatrix} A_{k_1,0,Re,w} \cos(\omega t) - B_{k_1,0,Im,w} \sin(\omega t) \\ A_{k_1,0,Re,w} \sin(\omega t) + B_{k_1,0,Im,w} \cos(\omega t) \\ A_{k_1,1,Re,w} \cos((W+w)\omega t) - B_{k_1,1,Im,w} \sin((W+w)\omega t) \\ A_{k_1,1,Re,w} \sin((W+w)\omega t) + B_{k_1,1,Im,w} \cos((W+w)\omega t) \end{bmatrix} \end{aligned} \quad (81)$$

or equivalently expressed as

$$V'_{k_1,s,Re} + iV'_{k_1,s,Im} = \sum_{w=1}^{2W} (A'_{k_1,s,Re,w} + iB'_{k_1,s,Im,w}) e^{i\omega t}, \quad (82)$$

where

$$\begin{cases} A'_{k_1,0,Re,w} = A_{k_1,0,Re,w}, & B'_{k_1,0,Im,w} = B_{k_1,0,Im,w}, & (0 < w \leq W) \\ A'_{k_1,0,Re,w} = 0, & B'_{k_1,0,Im,w} = 0, & (W < w \leq 2W) \\ A'_{k_1,1,Re,w} = 0, & B'_{k_1,1,Im,w} = 0, & (0 < w \leq W) \\ A'_{k_1,1,Re,w} = A_{k_1,1,Re,w-W}, & B'_{k_1,1,Im,w} = B_{k_1,1,Im,w-W}. & (W < w \leq 2W) \end{cases} \quad (83)$$

Since the output signals share the same mathematical structure as the input signals, it can be directly utilized as the input signals for the subsequent circuit gate.

The output voltage signals of the  $k_0$ -th cebit and the  $k_2$ -thcebit are

$$\begin{bmatrix} V'_{k_0,0,Re} \\ V'_{k_0,0,Im} \\ V'_{k_0,1,Re} \\ V'_{k_0,1,Im} \end{bmatrix} = \begin{bmatrix} V_{k_0,0,Re} + V_{l,Re} V_{k_0,0,Re} - V_{l,Im} V_{k_0,0,Im} \\ V_{k_0,0,Im} + V_{l,Re} V_{k_0,0,Im} + V_{l,Im} V_{k_0,0,Re} \\ V_{k_0,1,Re} + V_{l,Re} V_{k_0,1,Re} - V_{l,Im} V_{k_0,1,Im} \\ V_{k_0,1,Im} + V_{l,Re} V_{k_0,1,Im} + V_{l,Im} V_{k_0,1,Re} \end{bmatrix}, \quad (84)$$

$$\begin{bmatrix} V'_{k_2,0,Re} \\ V'_{k_2,0,Im} \\ V'_{k_2,1,Re} \\ V'_{k_2,1,Im} \end{bmatrix} = \begin{bmatrix} V_{k_2,0,Re} + V_{l,Re} V_{k_2,0,Re} - V_{l,Im} V_{k_2,0,Im} \\ V_{k_2,0,Im} + V_{l,Re} V_{k_2,0,Im} + V_{l,Im} V_{k_2,0,Re} \\ V_{k_2,1,Re} + \cos(2\pi/2^m) F_{Re} - \sin(2\pi/2^m) F_{Im} \\ V_{k_2,1,Im} + \sin(2\pi/2^m) F_{Re} + \cos(2\pi/2^m) F_{Im} \end{bmatrix}. \quad (85)$$

$(F_{Re} = V_{l,Re} V_{k_2,1,Re} - V_{l,Im} V_{k_2,1,Im}, F_{Im} = V_{l,Re} V_{k_2,1,Im} + V_{l,Im} V_{k_2,1,Re})$

or equivalently expressed as

$$\begin{cases} A'_{k_0,0,Re,w} = A_{k_0,0,Re,w}, & B'_{k_0,0,Im,w} = B_{k_0,0,Im,w}, & (0 < w \leq W) \\ A'_{k_0,0,Re,w} = A_{k_0,0,Re,w}, & B'_{k_0,0,Im,w} = B_{k_0,0,Im,w}, & (W < w \leq 2W) \\ A'_{k_0,1,Re,w} = A_{k_0,1,Re,w-W}, & B'_{k_0,1,Im,w} = B_{k_0,1,Im,w-W}, & (0 < w \leq W) \\ A'_{k_0,1,Re,w} = A_{k_0,1,Re,w-W}, & B'_{k_0,1,Im,w} = B_{k_0,1,Im,w-W}, & (W < w \leq 2W) \end{cases} \quad (86)$$

where

$$\begin{cases} A'_{k_0,0,Re,w} = A_{k_0,0,Re,w}, & B'_{k_0,0,Im,w} = B_{k_0,0,Im,w}, & (0 < w \leq W) \\ A'_{k_0,0,Re,w} = A_{k_0,0,Re,w}, & B'_{k_0,0,Im,w} = B_{k_0,0,Im,w}, & (W < w \leq 2W) \\ A'_{k_0,1,Re,w} = A_{k_0,1,Re,w-W}, & B'_{k_0,1,Im,w} = B_{k_0,1,Im,w-W}, & (0 < w \leq W) \\ A'_{k_0,1,Re,w} = A_{k_0,1,Re,w-W}, & B'_{k_0,1,Im,w} = B_{k_0,1,Im,w-W}, & (W < w \leq 2W) \end{cases} \quad (87)$$

and

$$\begin{cases} A'_{k_2,0,Re,w} = A_{k_2,0,Re,w}, & B'_{k_2,0,Im,w} = B_{k_2,0,Im,w}, & (0 < w \leq W) \\ A'_{k_2,0,Re,w} = A_{k_2,0,Re,w}, & B'_{k_2,0,Im,w} = B_{k_2,0,Im,w}, & (W < w \leq 2W) \\ A'_{k_2,1,Re,w} = A_{k_2,1,Re,w-W}, & B'_{k_2,1,Im,w} = B_{k_2,1,Im,w-W}, & (0 < w \leq W) \\ A'_{k_2,1,Re,w} = e^{i2\pi/2^m} A_{k_2,1,Re,w-W}, & B'_{k_2,1,Im,w} = e^{i2\pi/2^m} B_{k_2,1,Im,w-W}, & (W < w \leq 2W) \end{cases} \quad (88)$$

Since the output signals share the same mathematical structure as the input signals, it can be directly utilized as the input signals for the subsequent circuit gate. Using the  $n$ -cebit definition of the classical states in

Equation (22),

$$\begin{aligned} \varphi'_{s_1 s_2 \dots s_n} &= \frac{1}{T} \int_0^T dt \sum_{j=1}^W e^{-ij\omega t} \prod_{k=1}^n * \left( V'_{k,s_k,Re} + iV'_{k,s_k,Im} \right) \\ &= \frac{1}{T} \int_0^T dt \sum_{j=1}^{2W} e^{-ij\omega t} \prod_{k=1}^n * \left( \sum_{\omega=1}^{2W} \left( A'_{k,s_k,Re,\omega} + iB'_{k,s_k,Im,\omega} \right) e^{i\omega t} \right) \quad (89) \\ &= \frac{1}{T} \int_0^T dt \sum_{j=1}^{2W} e^{-ij\omega t} \prod_{k=1}^n * \left( \sum_{\omega=1}^{2W} \left( A'_{k,s_k,Re,\omega} + iB'_{k,s_k,Im,\omega} \right) e^{i\omega t} \right) \\ &\quad + \frac{1}{T} \int_0^T dt \sum_{j=1}^{2W} e^{-ij\omega t} \prod_{k=1}^n * \left( \sum_{\omega=W+1}^{2W} \left( A'_{k,s_k,Re,\omega} + iB'_{k,s_k,Im,\omega} \right) e^{i\omega t} \right). \end{aligned}$$

is observed. Note that the convolution operation has the following property

$$\begin{aligned} C_{w_1} e^{iw_1\omega t} * C_{w_2} e^{iw_2\omega t} &= C_{w_1} C_{w_2} \frac{1}{T} \int_0^T dt e^{iw_1\omega t} e^{iw_2\omega(t-\tau)} \\ &= \delta_{w_1, w_2} C_{w_1} C_{w_2} e^{iw_1\omega t}. \quad (90) \end{aligned}$$

When  $s_{k_1} = 0$ ,

$$\begin{cases} A'_{k_1,0,Re,\omega} + iB'_{k_1,0,Im,\omega} = 0, & (W < \omega \leq 2W) \\ A'_{k_0,s_{k_0},Re,\omega} + iB'_{k_0,s_{k_0},Im,\omega} = A_{k_0,s_{k_0},Re,\omega} + iB_{k_0,s_{k_0},Im,\omega}, & (0 < \omega \leq W) \\ A'_{k_1,0,Re,\omega} + iB'_{k_1,0,Im,\omega} = A_{k_1,0,Re,\omega} + iB_{k_1,0,Im,\omega}, & (0 < \omega \leq W) \\ A'_{k_2,s_{k_2},Re,\omega} + iB'_{k_2,s_{k_2},Im,\omega} = A_{k_2,s_{k_2},Re,\omega} + iB_{k_2,s_{k_2},Im,\omega}, & (0 < \omega \leq W) \end{cases} \quad (91)$$

is observed, such that for any values of  $s_{k_0}$  and  $s_{k_2}$ ,

$$\begin{aligned} \varphi'_{s_{k_0}, s_{k_1}=0, s_{k_2}} &= \frac{1}{T} \int_0^T dt \sum_{j=1}^{2W} e^{-ij\omega t} \prod_{k=1}^n \\ &\quad * \left( \sum_{\omega=1}^W \left( A'_{k,s_k,Re,\omega} + iB'_{k,s_k,Im,\omega} \right) e^{i\omega t} \right) \\ &= \varphi_{s_{k_1}=0, s_{k_2}} \quad (92) \end{aligned}$$

is observed. When  $s_{k_1} = 1$ ,

$$\begin{cases} A'_{k_1,0,Re,\omega} + iB'_{k_1,0,Im,\omega} = 0, & (0 < \omega \leq W) \\ A'_{k_0,0,Re,\omega} + iB'_{k_0,0,Im,\omega} = A_{k_0,0,Re,\omega-W} + iB_{k_0,0,Im,\omega-W}, & (W < \omega \leq 2W) \\ A'_{k_1,0,Re,\omega} + iB'_{k_1,0,Im,\omega} = A_{k_1,0,Re,\omega-W} + iB_{k_1,0,Im,\omega-W}, & (W < \omega \leq 2W) \\ A'_{k_2,0,Re,\omega} + iB'_{k_2,0,Im,\omega} = e^{i2\pi/2^m} \left( A_{k_2,0,Re,\omega-W} + iB_{k_2,0,Im,\omega-W} \right), & (W < \omega \leq 2W) \end{cases} \quad (93)$$

is observed, where  $m = k_2 - k_1 + 1$ , and

$$\begin{aligned} \varphi'_{\dots s_{k_1}=1, s_{k_1+1}, s_{k_1+2}, \dots, s_n} &= \frac{1}{T} \int_0^T dt \sum_{j=1}^{2M} e^{-ij\omega t} \prod_{k=1}^n * \left( \sum_{\omega=W+1}^{2W} \left( A'_{k,s_k,Re,\omega} + iB'_{k,s_k,Im,\omega} \right) e^{i\omega t} \right) \\ &= \prod_{s_{k_2}=1} e^{i2\pi/2^m} \varphi_{\dots s_{k_1}=1, s_{k_1+1}, s_{k_1+2}, \dots, s_n} \quad (94) \end{aligned}$$

is observed. In other words, under the condition  $s_{k_1} = 1$ , each term of  $s_{k_2} = 1$  in the subscript of the classical state function  $\varphi$  introduces a phase shift of  $2\pi/2^m$  ( $m = k_2 - k_1 + 1$ ) in  $\varphi'$ . While in the  $\hat{U}_{CR}$  gate, each term of  $s_{k_2} = 1$  in the subscript of the quantum state  $\phi$  corresponds to an  $\hat{U}_{CR,m}$  gate, which also introduces a  $2\pi/2^m$  phase shift in  $\phi'$ . Therefore, both the classical  $U_{CR}$  gate and the quantum  $\hat{U}_{CR,m}$  gate introduce identical phase shifts by the same subscript terms in their respective state functions, resulting in equivalent operational outcomes. This confirms that the circuit  $U_{CR}$  gate corresponds to the quantum  $\hat{U}_{CR,m}$  gate.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

## Keywords

circuit gates, classical circuit networks, Fourier transform, quantum algorithm, signal processing

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