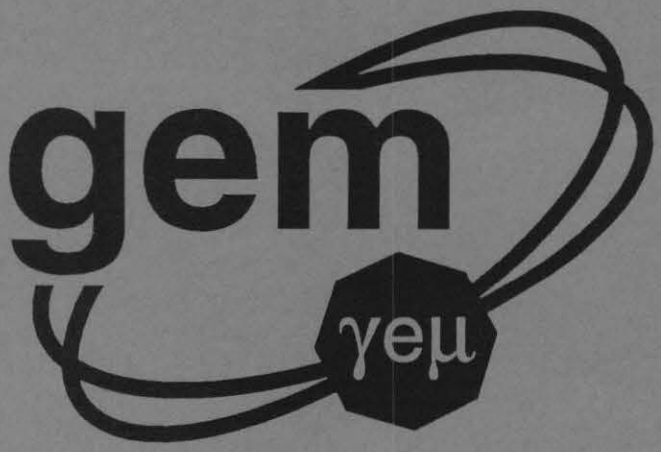
GEM TN-93-446



CSC Front Readout Meeting at Princeton

Daniel R. Marlow
Princeton University

July 18-19, 1993

Abstract;

Agenda, attendees, and presentations of the CSC Front Readout Meeting held at Princeton on July 18-19, 1993.

Revised Agenda

Sunday, July 18, 1993

11:00	Overview of the System Requirements and Architecture as set forth in the TDR.	Marlow
	Discussion of possible revisions.	
12:30	Lunch	
1:30	CSC Readout Work at Princeton. Status & Plans	Wixted
2:30	Lab tour and demonstration	
3:30	Anode Readout Work at Boston	Varner
	--- Prototype test electronics	
	--- Production readout and HV	
4:30	ROPCB work at U of H status and plans (discussion)	Pinsky
5:30	Free time (discussions etc.)	
6:30	Barbecue at the Marlows	

Monday, July 19, 1993

9:00	FPGA-based readout controller	Chinatti
9:30	Signal processing strategies	Prebys
10:30	Break	
11:00	Definition of PCB for Fermilab Tests	
12:00	Lunch	
1:30	Discussion of FY94 R&D Plan	
2:30	Draft of written meeting summary.	
3:00	Adjourn	

(People should allow 2 hours between their Princeton departure and their scheduled flight time. We can adjust time of adjournment accordingly).

18-19 July 93 Muon Readout Meeting at Princeton

Eric Prebys (609) 258-4910 prebys@puhep1.princeton.edu

Bruce R Broomer (303) 492-4363 FAX (303) 492-5119
BROOMER%KAOS@VAXF.COLORADO.EDU

Uriel Nauenberg (303) 492-7715 FAX (303) 492-5119
NAUENBER@COLOPHYS URIEL@RMCHEP.COLORADO.EDU

Lan, KEJIAN (713) 743-3554 FAX (713) 743-3589
LAN@UH.EDU.

Robert Wixted (609) 258-1509 Wixted@puphep.princeton.edu

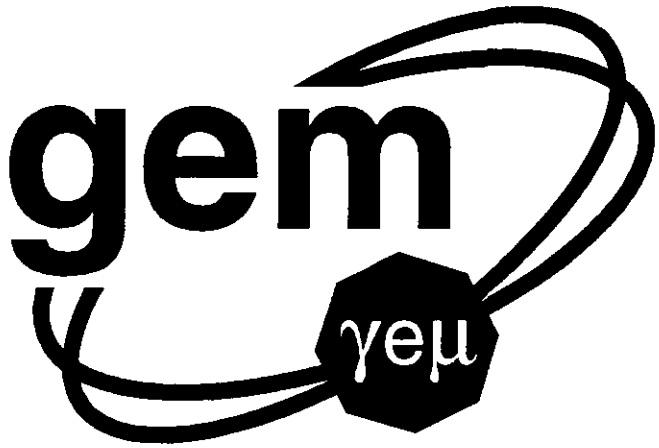
Steve Chinatti (609) 258-1509 chinatti@pucc.x.Princeton.EDU
chinatti@pupcad1.Princeton.EDU

GARY VARNER (617) 353-4114 -6057 varner@buphy.bu.edu
varner@budoe.bu.edu

Phil Baringer (913) 864-3953 BARINGER@UKANVAX (BITNET)
BARINGER@KUHUB.CC.UKANS.EDU

Dan Marlow 609 258 4383 ~~683 56~~ MARLOW@PUPHEP.PRINCETON.EDU

LARRY PINSKY (713) 743 3552 PINSKY@UHPHYS.UH.EDU



Overview of CSC Readout

CSC Readout Meeting at Princeton

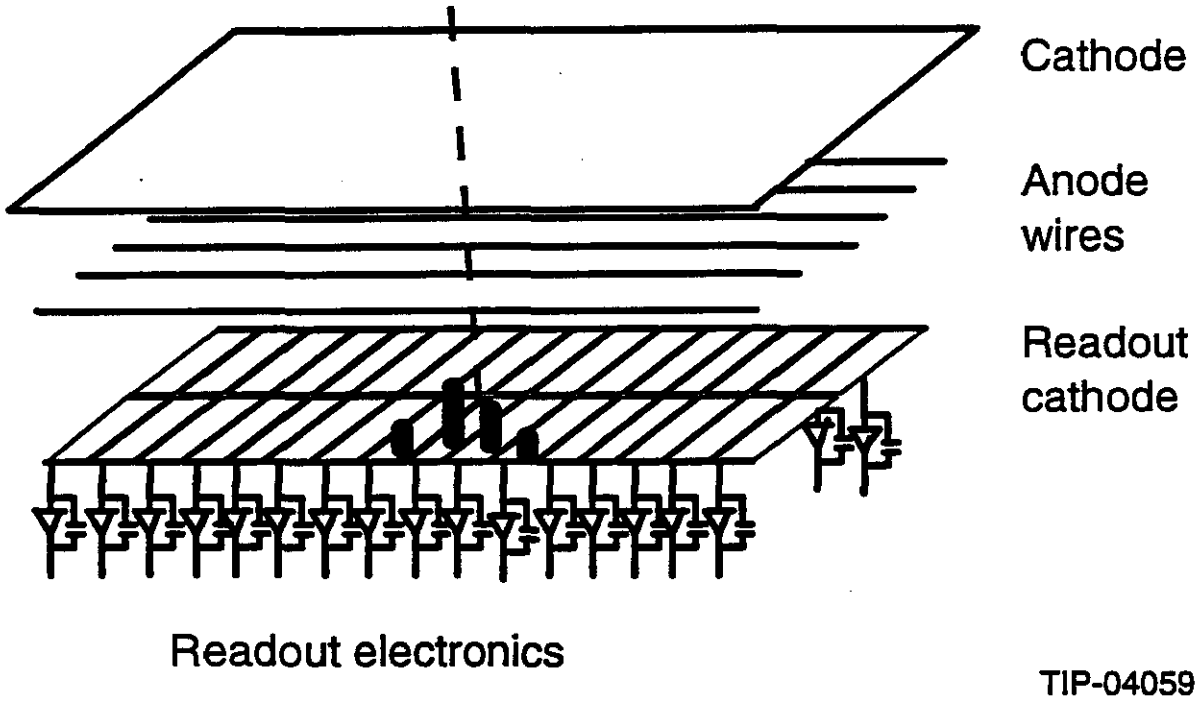
Presentation by:

Daniel R. Marlow
Princeton University

July 18, 1993

Principle of Charge Interpolation Readout

Start with a conventional MWPC, but form the cathode planes with a pattern of etched strips, running perpendicular to the wires.

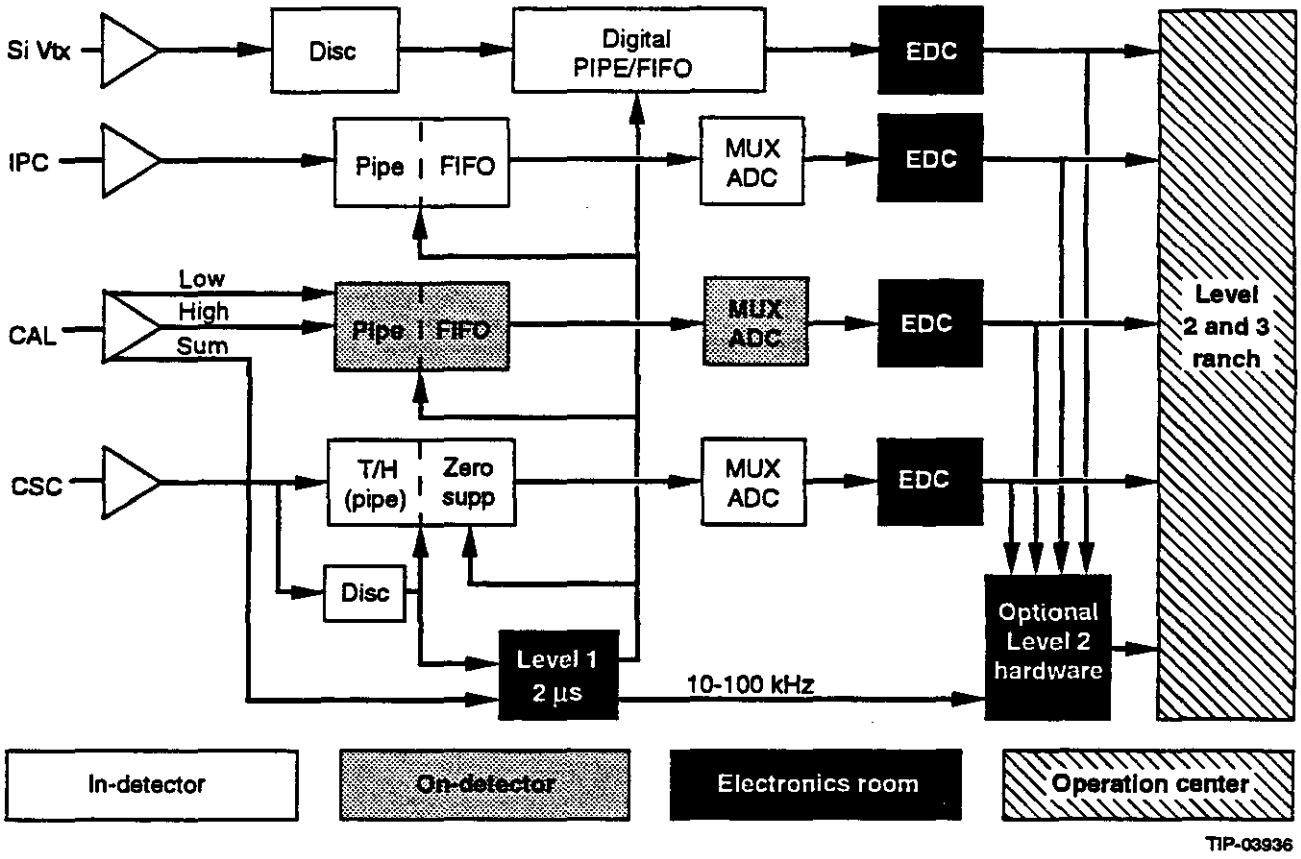


If each strip is instrumented with a charge-sensitive preamplifier, the position of incidence can be determined from the center of gravity of the induced charge. The position accuracy is then set by the accuracy with which the charge on each strip can be measured—*e.g.*,

$$\frac{\Delta x}{w} \simeq \sqrt{2}\,\frac{\Delta Q}{Q} \sim 1\%$$

where w is the strip width.

Electronic Architecture



Readout Rates

GEM Trigger/DAQ Design Goals				
Level	Rate In	Rate Out	Latency	Comments
1	60 MHz	10 kHz	2 μs	Pipelined
2	100 kHz	100 Hz	100 μs—100 ms	Asynchronous
3	3 kHz	100 Hz	—	CPU Ranch

GEM CSC Readout-Specific Design Goals

- Equivalent noise charge ($\sim$ 2000 e^-) rms (for τ = 300 ns)
- Dynamic Range
  - 50 μm measurement for strip width $w = 5$ mm

$$\frac{\sigma_s}{w} \simeq \sqrt{2}\frac{\sigma_q}{Q} \Longrightarrow \frac{Q}{\sigma_q} \simeq \sqrt{2}\frac{w}{\sigma_s} = 140$$

$$\Longrightarrow 7.1 \text{ bits}$$

  - Landau tail $\varepsilon \simeq 95\%$
    $\Longrightarrow$ $40 - 230\ e^-$ $\Longrightarrow$ 2.5 bits
  - $\times 2$ Design margin $\Longrightarrow$ 1.0 bits
  - Total $\Longrightarrow$ 10.6 bits
- < 10 μs *effective* conversion time
- Time resolution $\sim$ BX (for rejection of neutron hits)
- Low cost ($<$ \$10./ channel)
- Radiation hard? $F_n \simeq 10^{13}$ cm^{-2} 100 SSC-yr

Electrical Specifications for the CSC Readout	
Parameter	Value
Equivalent Input Noise	$< 2000\ e^-$ rms
Pulse Peaking Time	300 ns
Overall System Gain	0.4 fC/Count
Dynamic Range	10 bits
Accuracy	0.5%
Cross Talk	< -50 db
Readout Rate	100 kHz
Readout Latency	$< 100\ \mu$s
Temperature Range	20 ± 5 °C
Power Per Channel	< 100 mW
Rad. Hardness: Ionizing	(10 kRad)
Rad. Hardness: Neutrons	10^{13} cm^{-2}

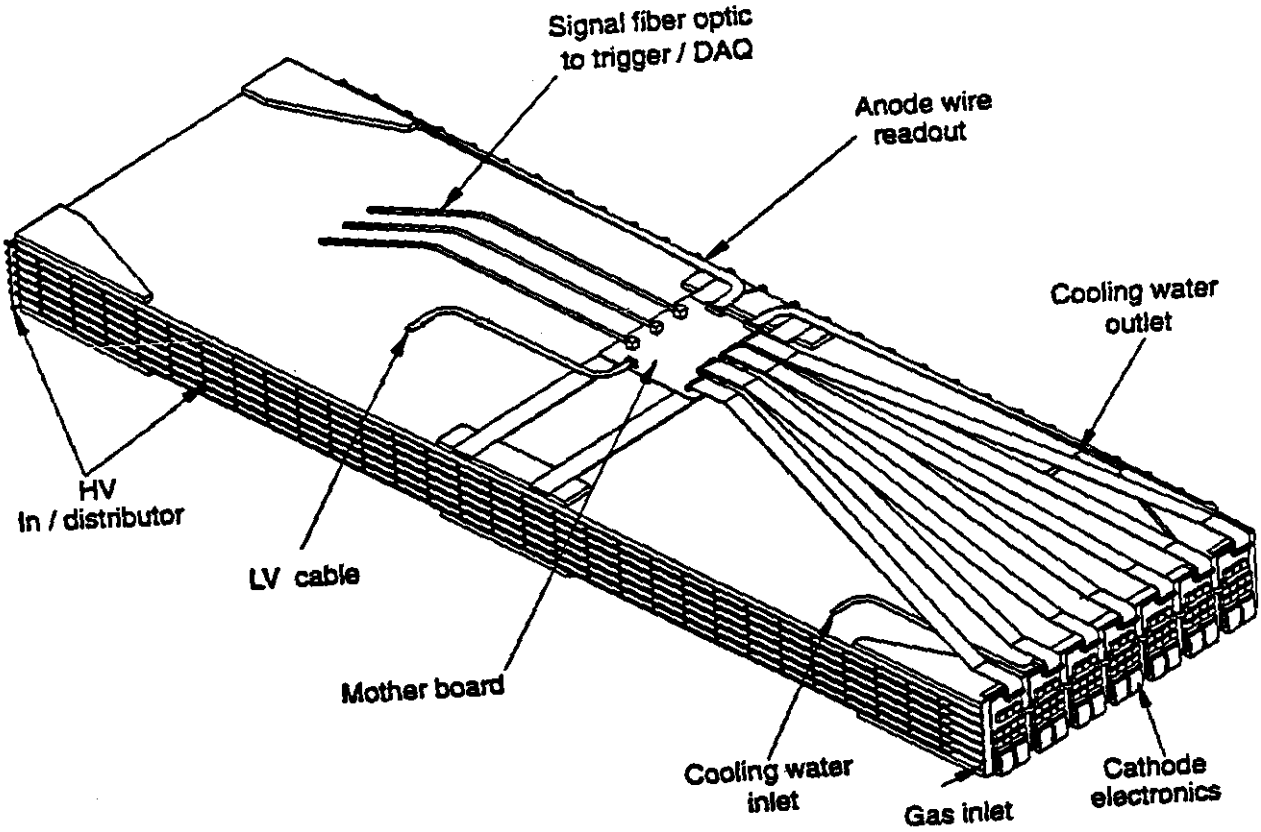


FIG. 4-48. Perspective view of complete CSC barrel chamber.

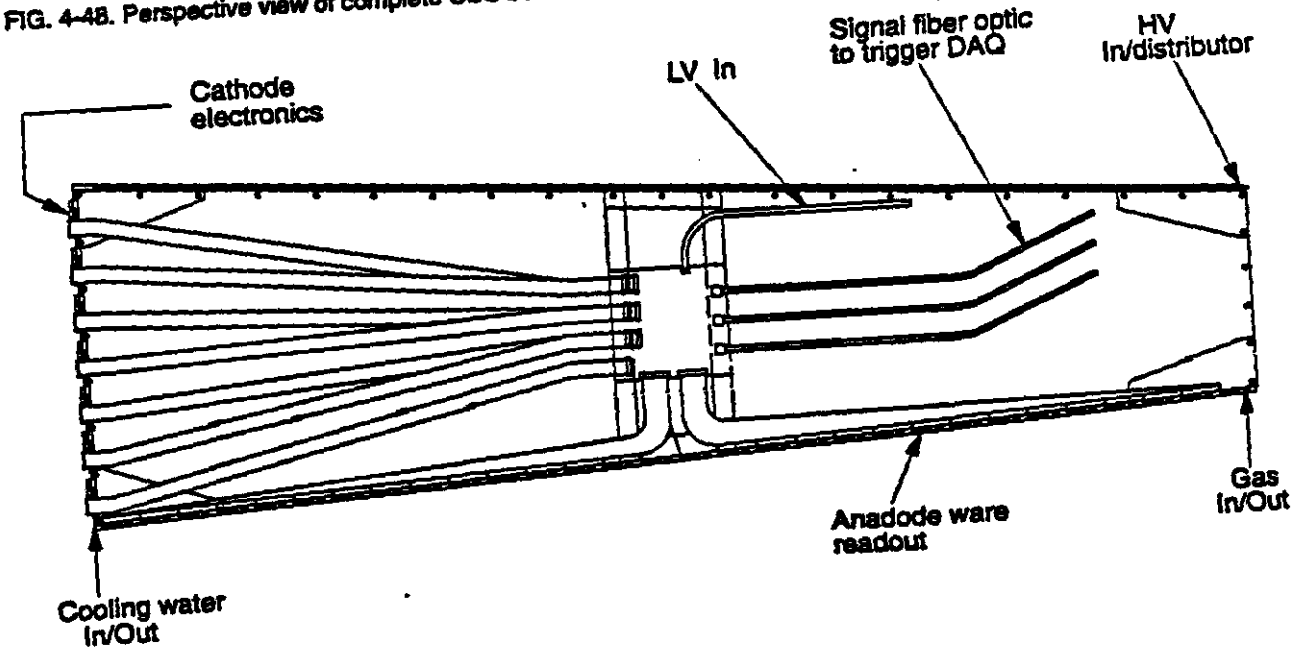


FIG. 4-49. Plan view of endcap chambers.

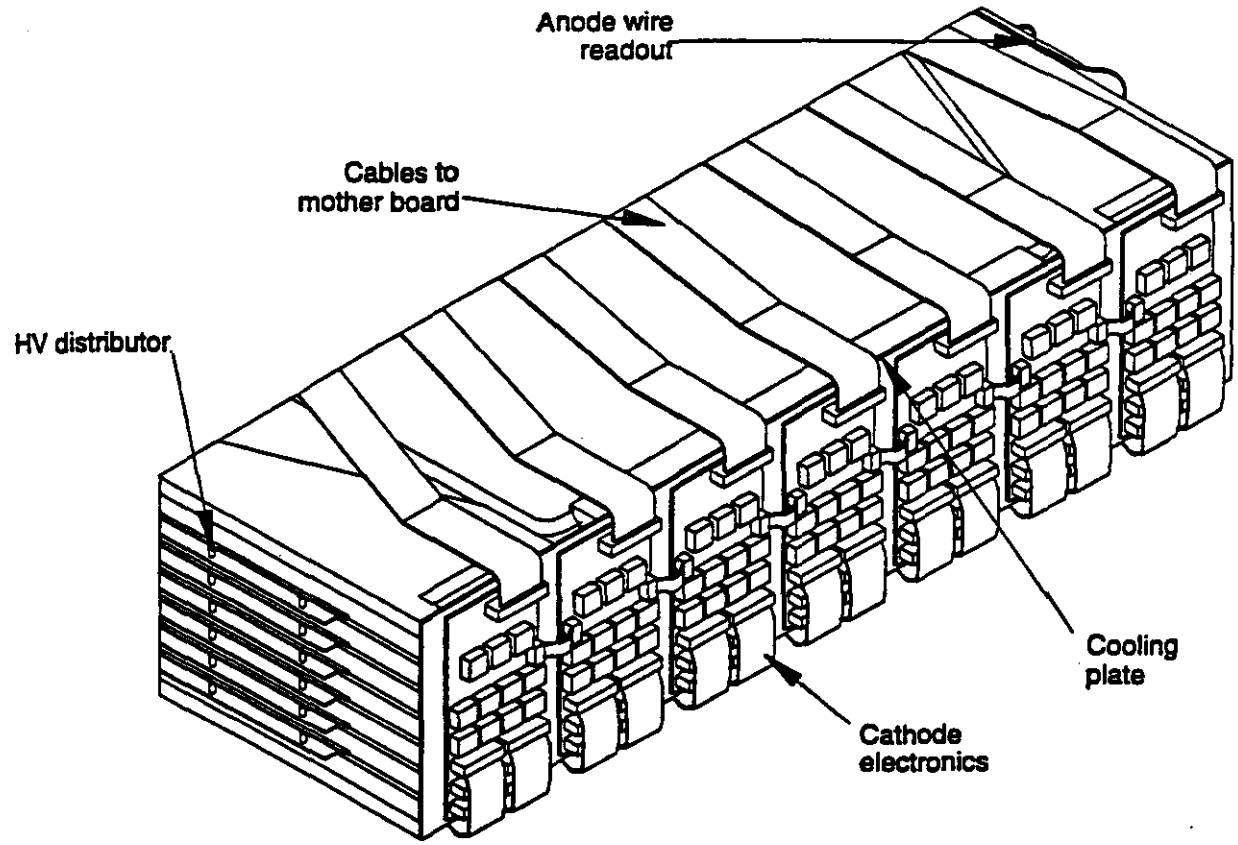


FIG. 4-50. Strip electronics and cooling concepts for the CSC.

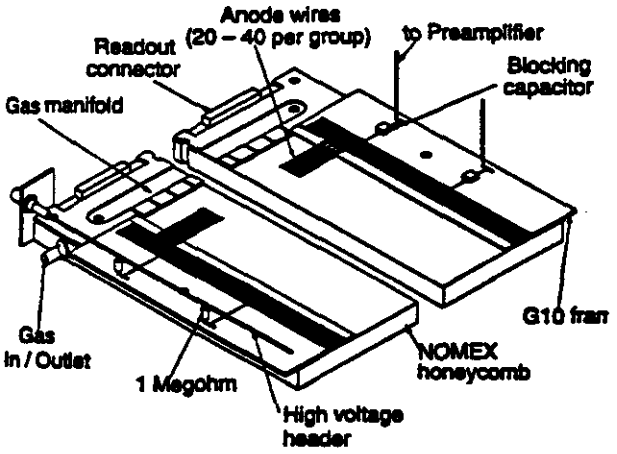


FIG. 4-51. Service layout for CSC showing gas connection, HV distribution and anode signal output.

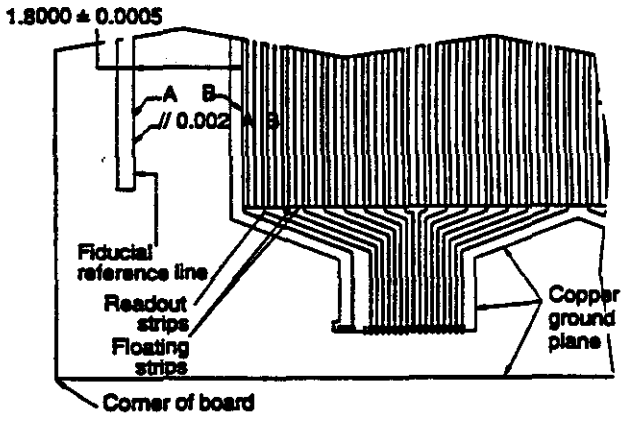


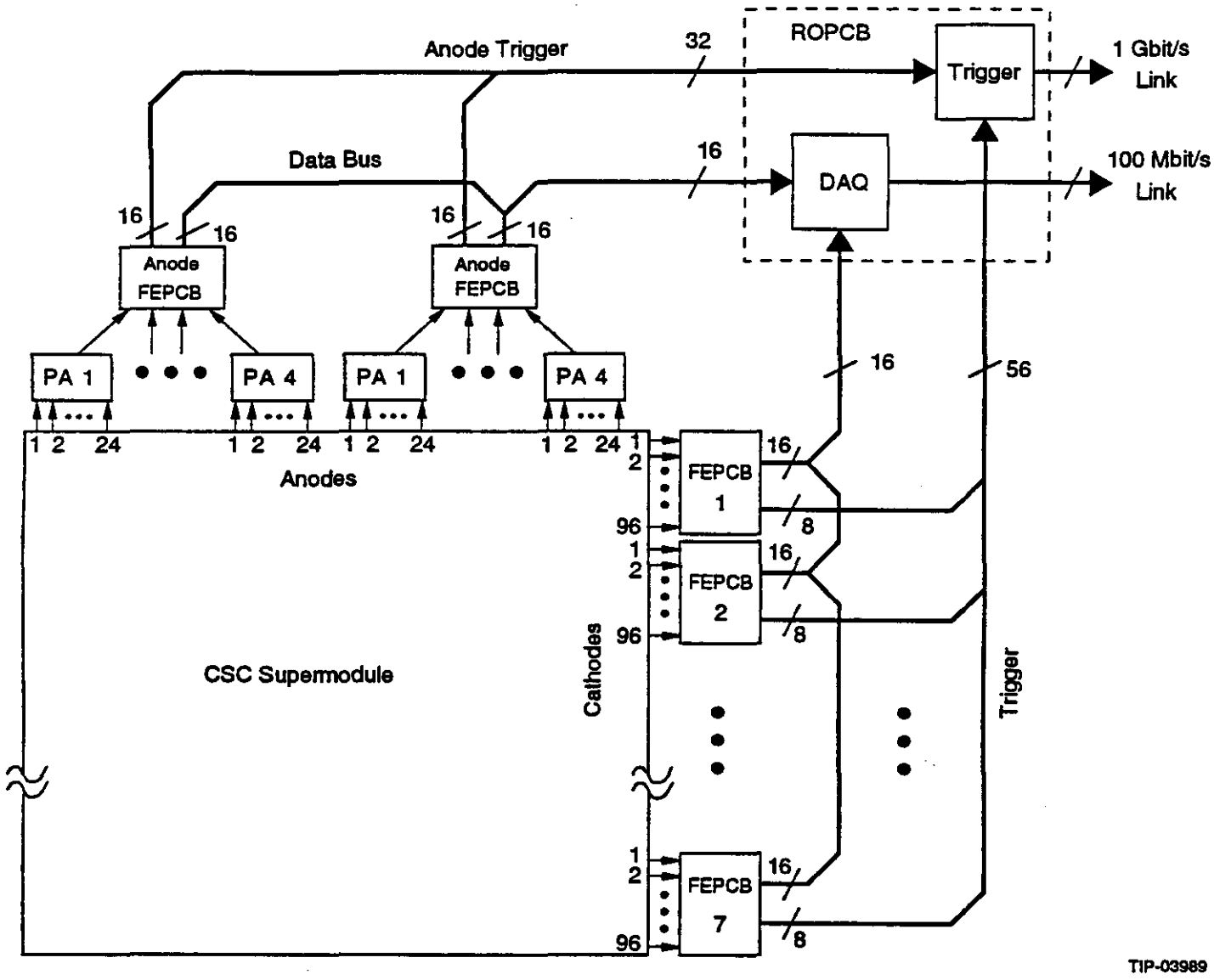
FIG. 4-52. Corner of a CSC cathode showing relationship of strips, readout connections and fiducial lines.

4.3.3 Support Structure

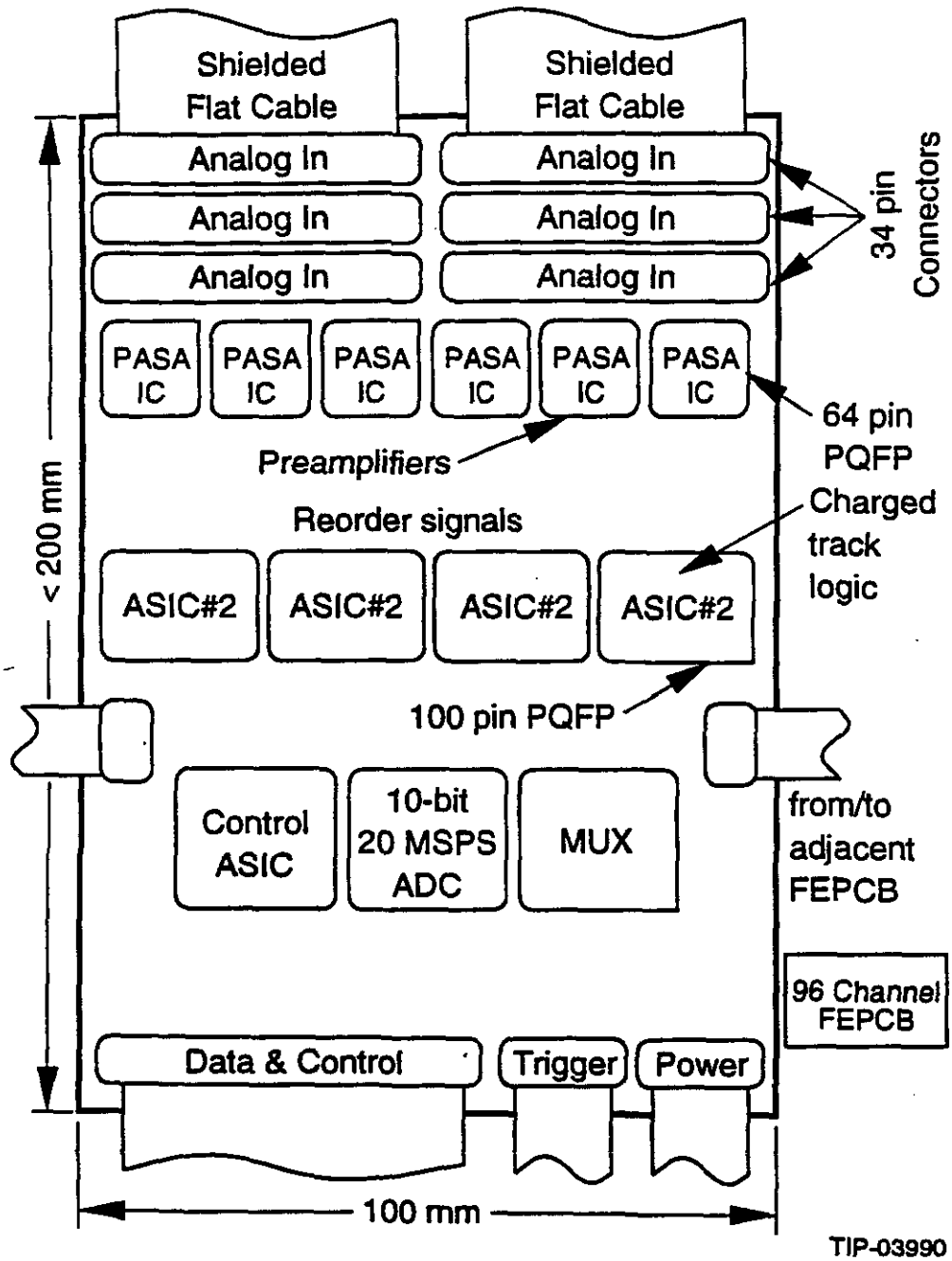
Overview

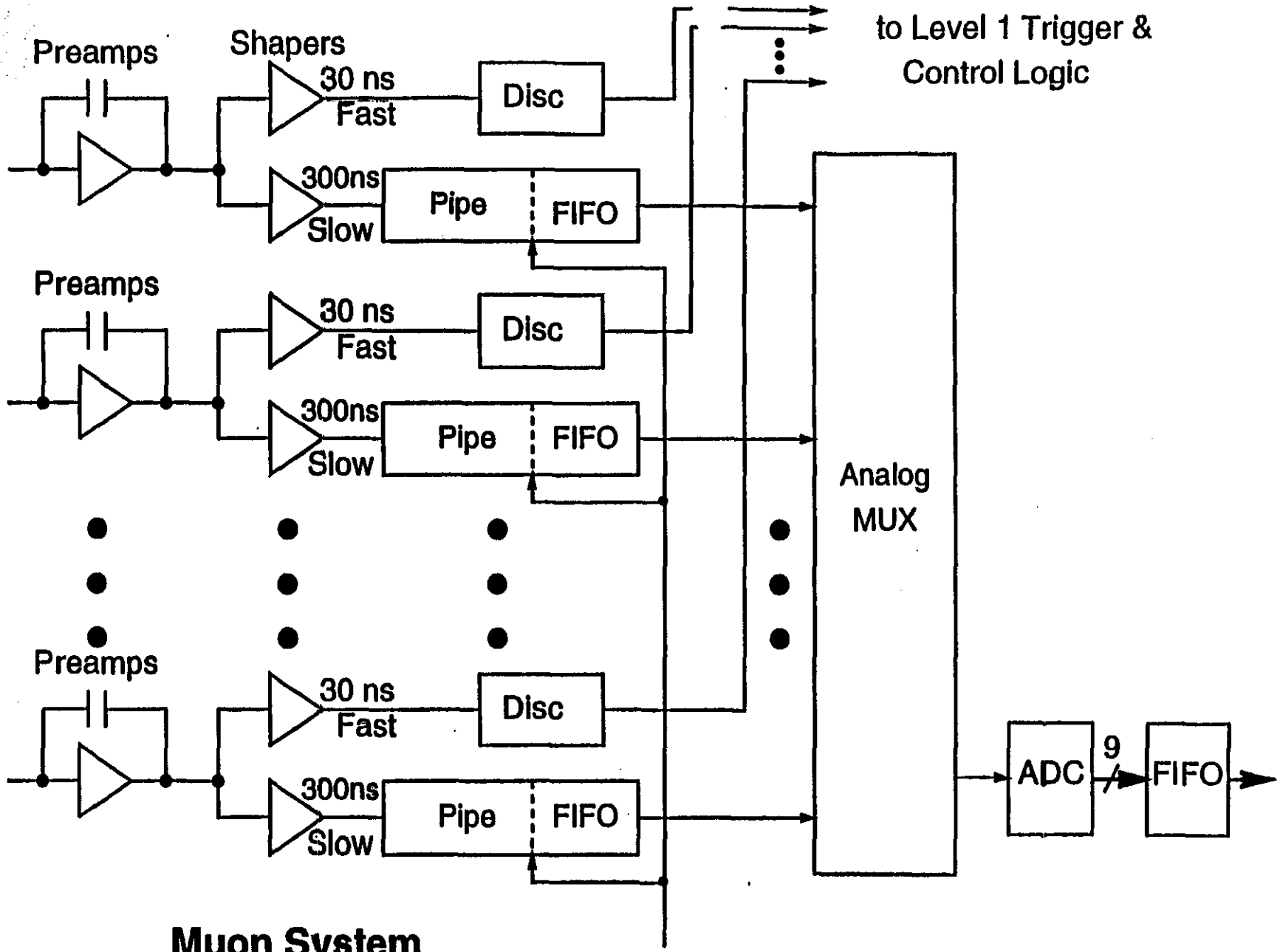
The design of the chamber support structures is driven by the chamber construction and layout and by the need for the chamber weights to be carried at or near structure support nodes. The design has minimized the number of different chamber sizes to minimize chamber production costs. A structural stability of better than 25 μm is needed between the respective superlayers of chambers within a muon projective tower. The muon chamber layouts have been designed to maximize the θ and ϕ coverage in

System Architecture



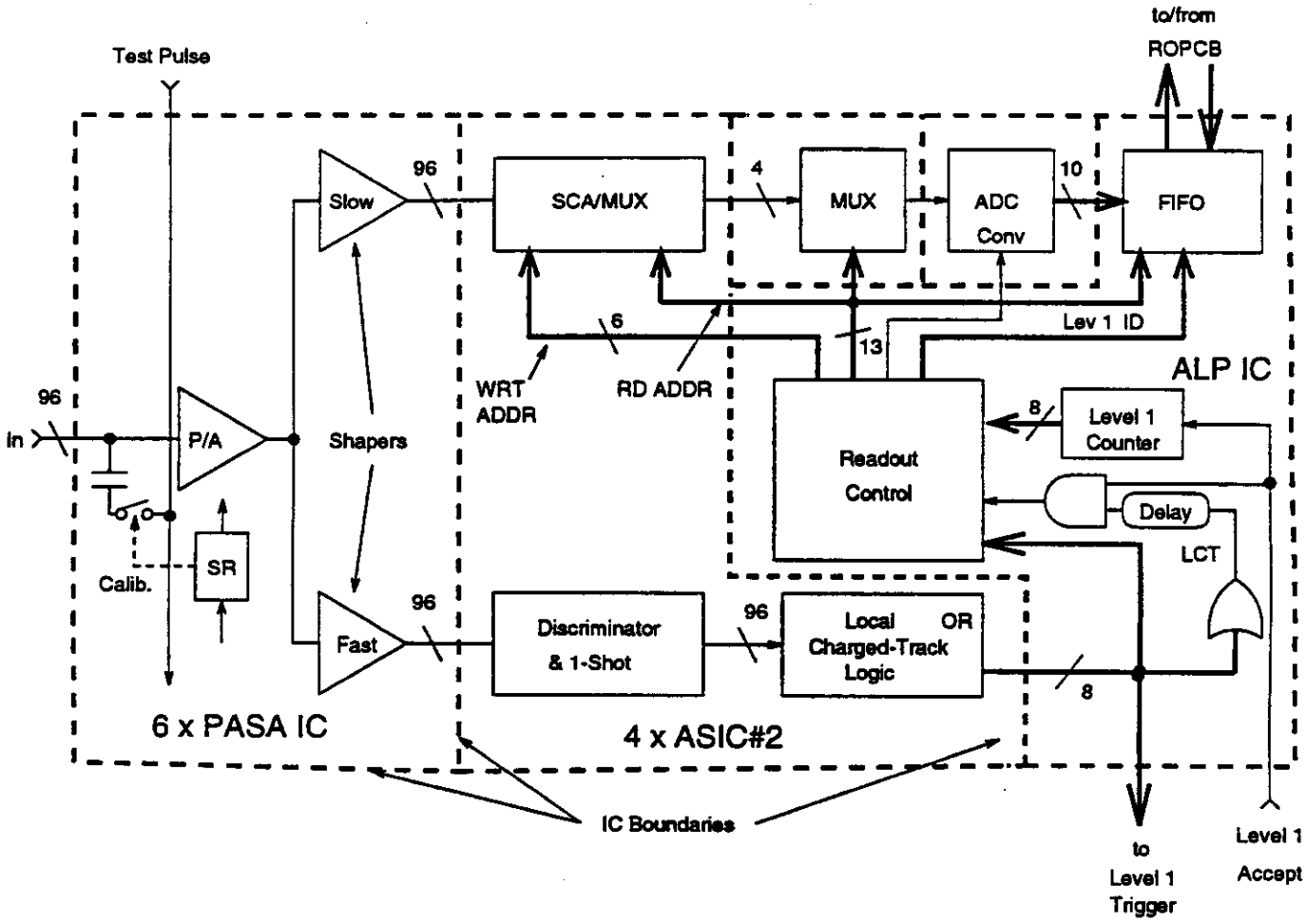
Front End Printed Circuit Board (FEPCB)



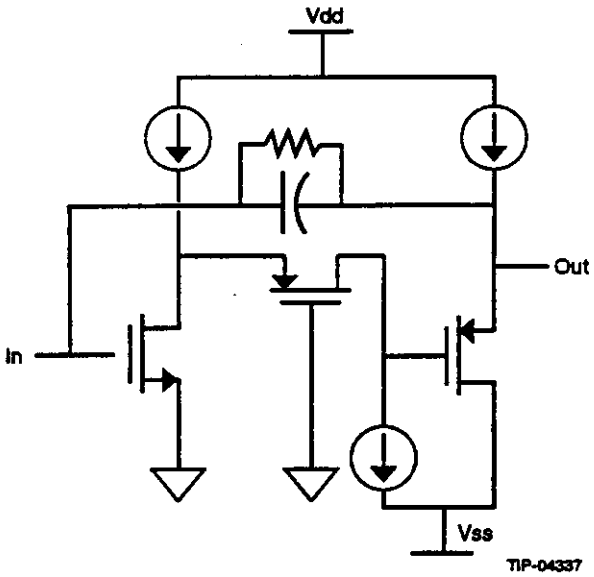


Muon System
Cathode Strip Chamber
SCA-Based Readout

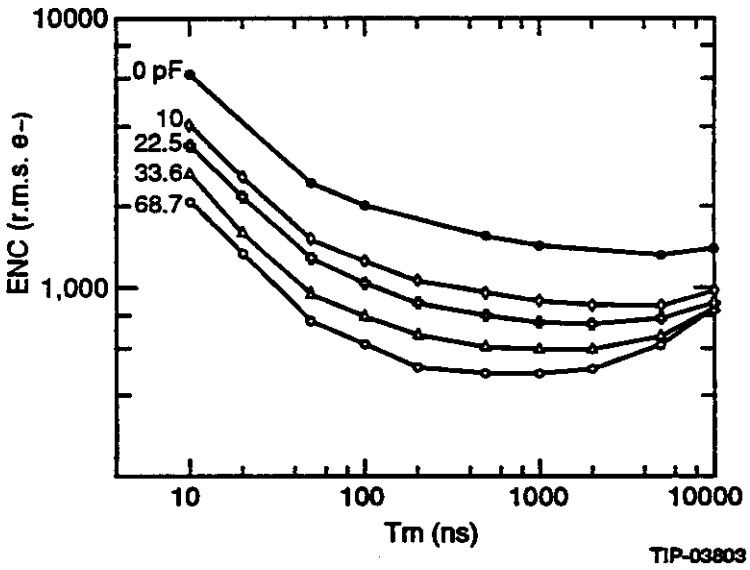
FEPCB Electrical Architecture
(SCA Version)



CMOS Preamplifier



Circuit Diagram

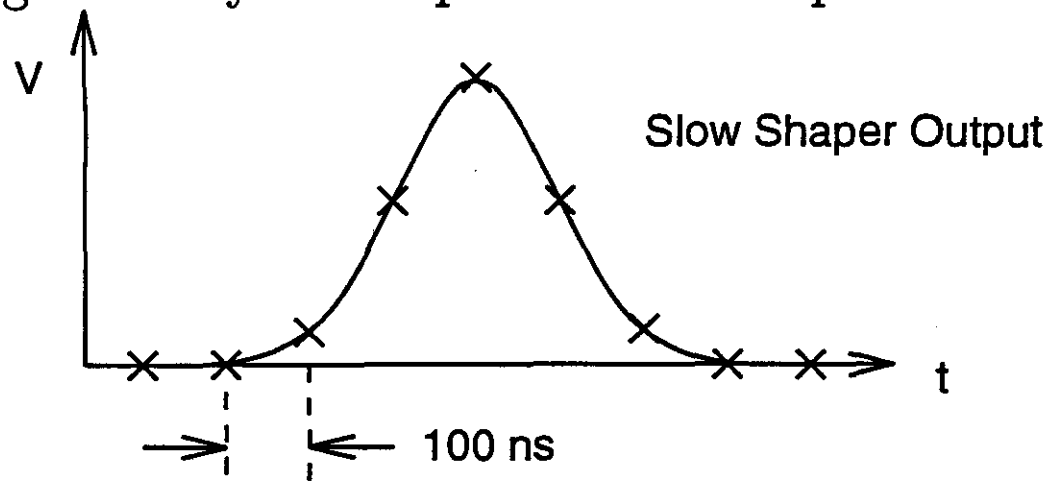


Noise versus Shaping Time—Preamp Only

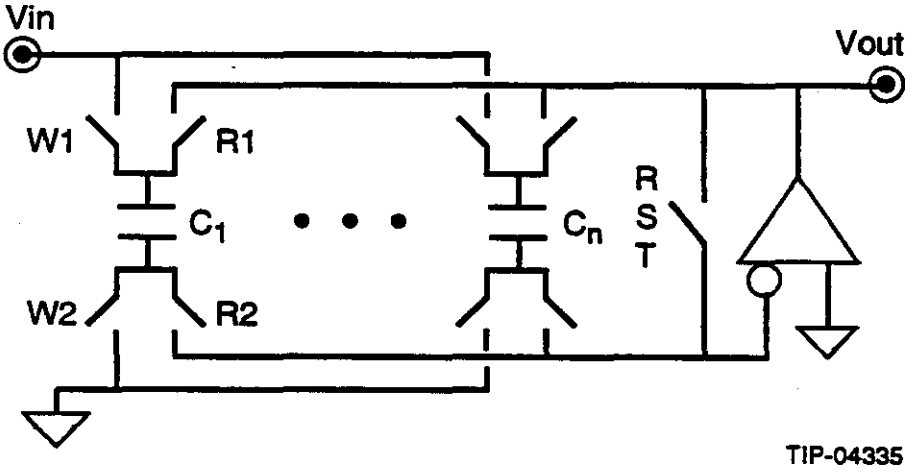
With a 700 ns shaper, the noise is 1800 e^-+12 e^-/pF.

Switched Capacitor Analog Memory

One approach is to sample the pulse every $\sim$ 100 ns using an array of sample-and-hold capacitors.



Such an array can be operated as a *logical* analog shift register to provide the required 2 μs Level 1 delay.



Digital logic controls the switches. Note that the charge doesn't move, but rather the status of each memory location changes with time.

Neutron Rates

- Inherently uncertain
- Product of three factors

$$R = \varepsilon_n F_n A \equiv r_n A$$

where in the endcap

$$\varepsilon_n \sim 10^{-3} = \text{detection efficiency}$$
$$F_n \sim 10^5 \text{ cm}^{-2} s^{-1} = \text{fluence}$$
$$A = 93 \times 0.5 \text{ cm}^2 = \text{strip area}$$

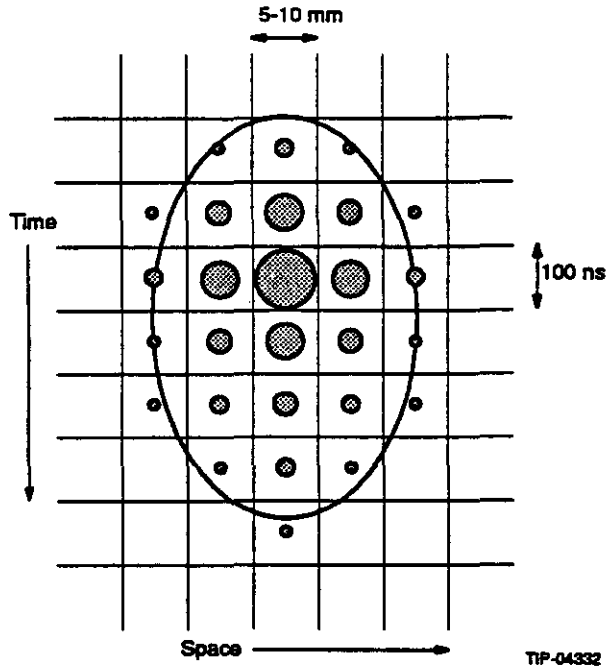
Note: The numbers above are inferred from the GEM TDR Table 4-6, which includes n's and γ's for $L = 10^{34}$ cm^{-2}s^{-1}. From the table one can extract only the detected fluence r_n, which is

$$10 < r_n < 100 \text{ cm}^{-2}\text{s}^{-1}$$

Assuming that each hit lights four strips the corresponding rates per strip are

$$6 < R < 20 \text{ kHz}$$

Analog Pipeline (SCA) Option



Assume

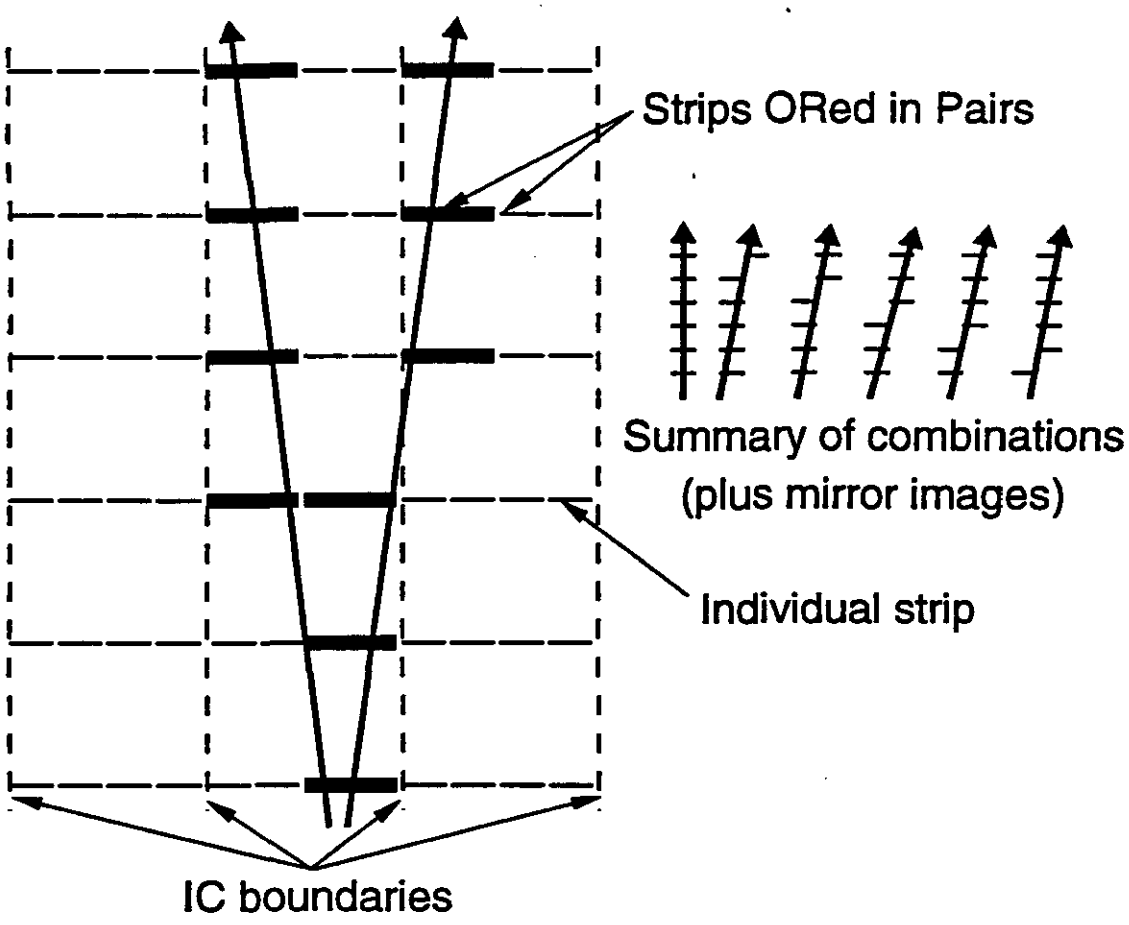
$$t_p = \text{pulse peaking time} = 300 \text{ ns}$$
$$\Delta t = \text{sample clock period} = 100 \text{ ns}$$

If accidental pulses falling within the indicated region in the space-time grid shown above are considered to spoil the signal pulse, the maximum unspoiled rate is given by

$$R_{\max} = \frac{p_{\max}}{21\Delta t} = \frac{0.1}{21 \times 10^{-7}} = 48 \text{ kHz}$$

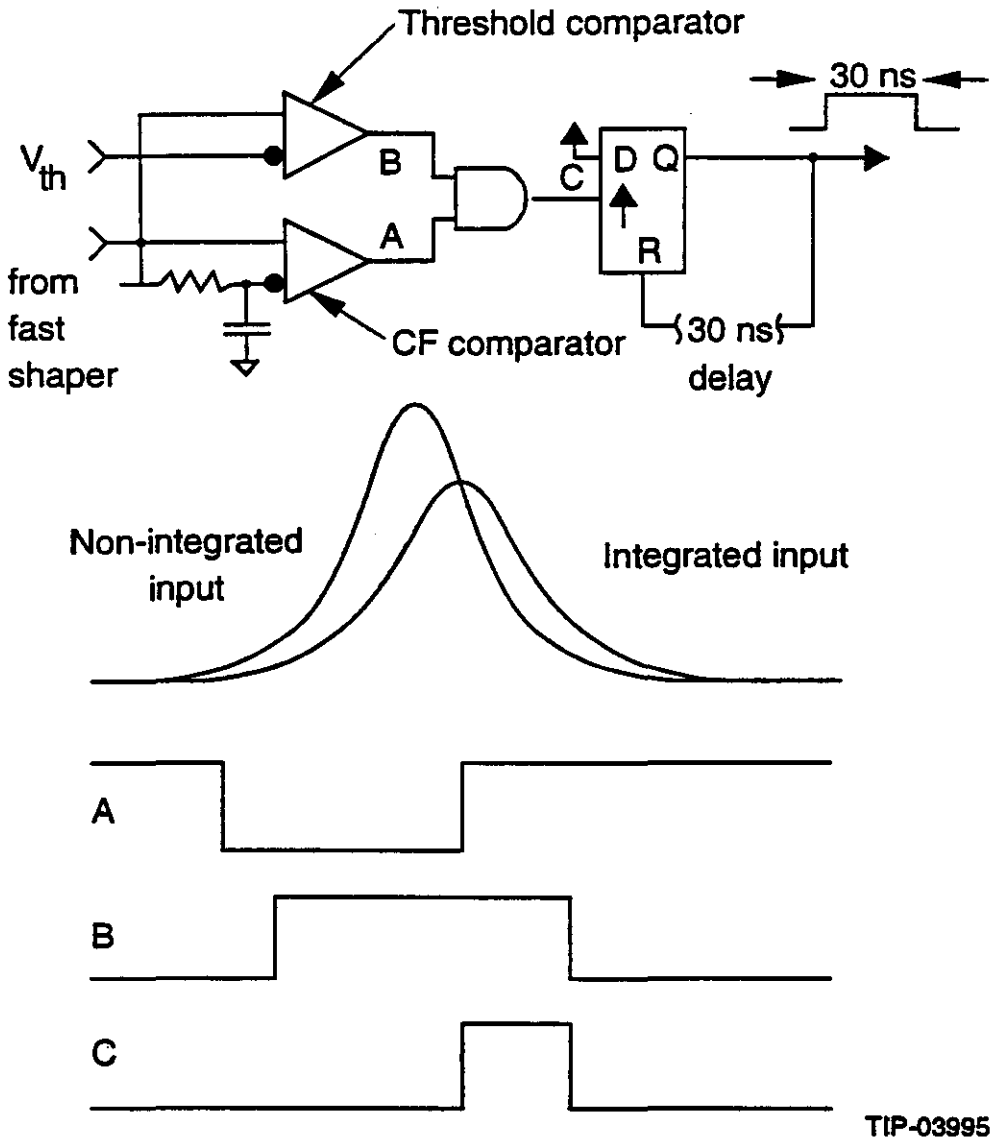
(corresponding to $r = 320 \text{ cm}^{-2}\text{s}^{-1}$)

Local Charged Track (LCT) Logic



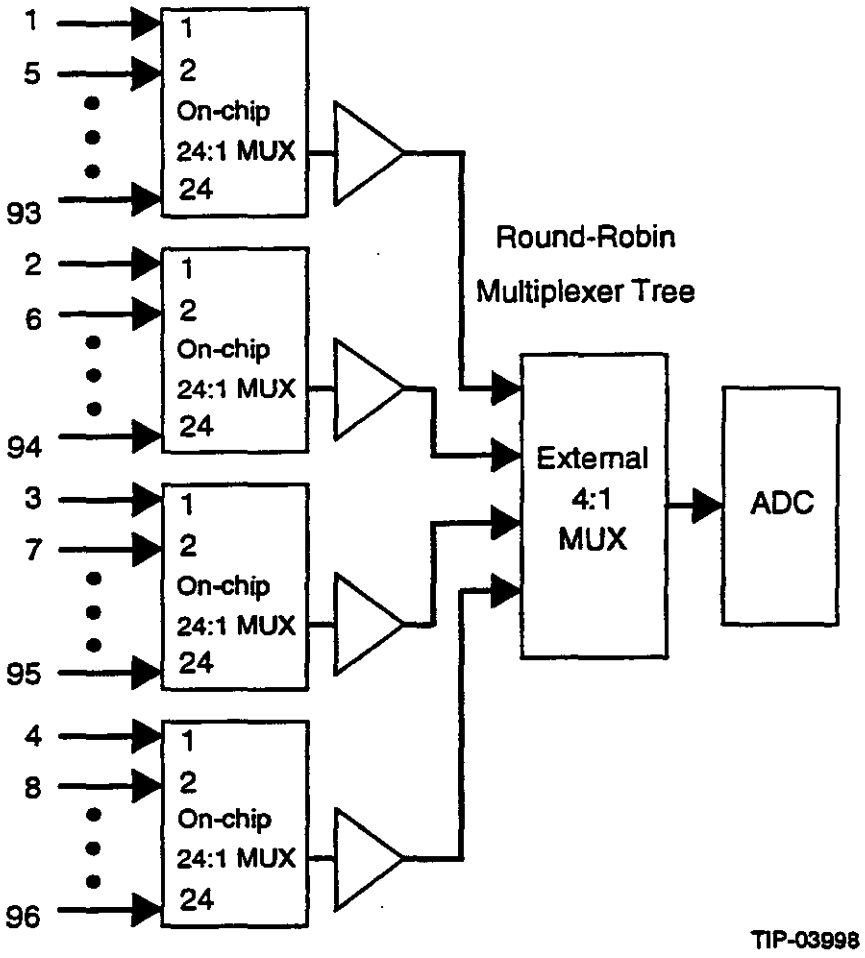
Note: This diagram shows just one of the possibilities. Other patterns are also possible. All will impose an "m-of-6" requirement to suppress noise, while maintaining efficiency.

Constant Fraction Discriminator



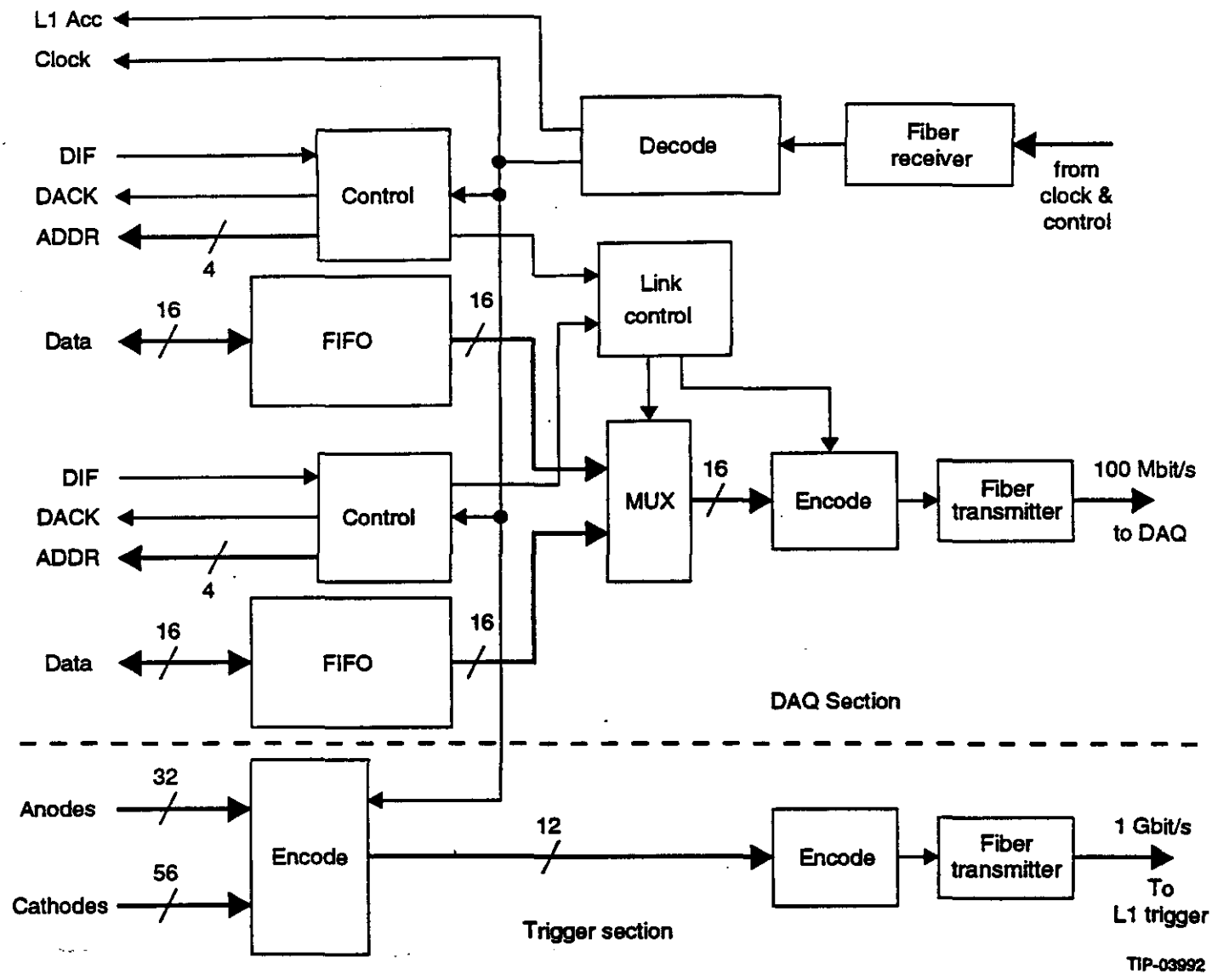
Note: This diagram shows just one of the possibilities. Other patterns are also possible. All will impose an "m-of-6" requirement to suppress noise, while maintaining efficiency.

ADC and Multiplexer

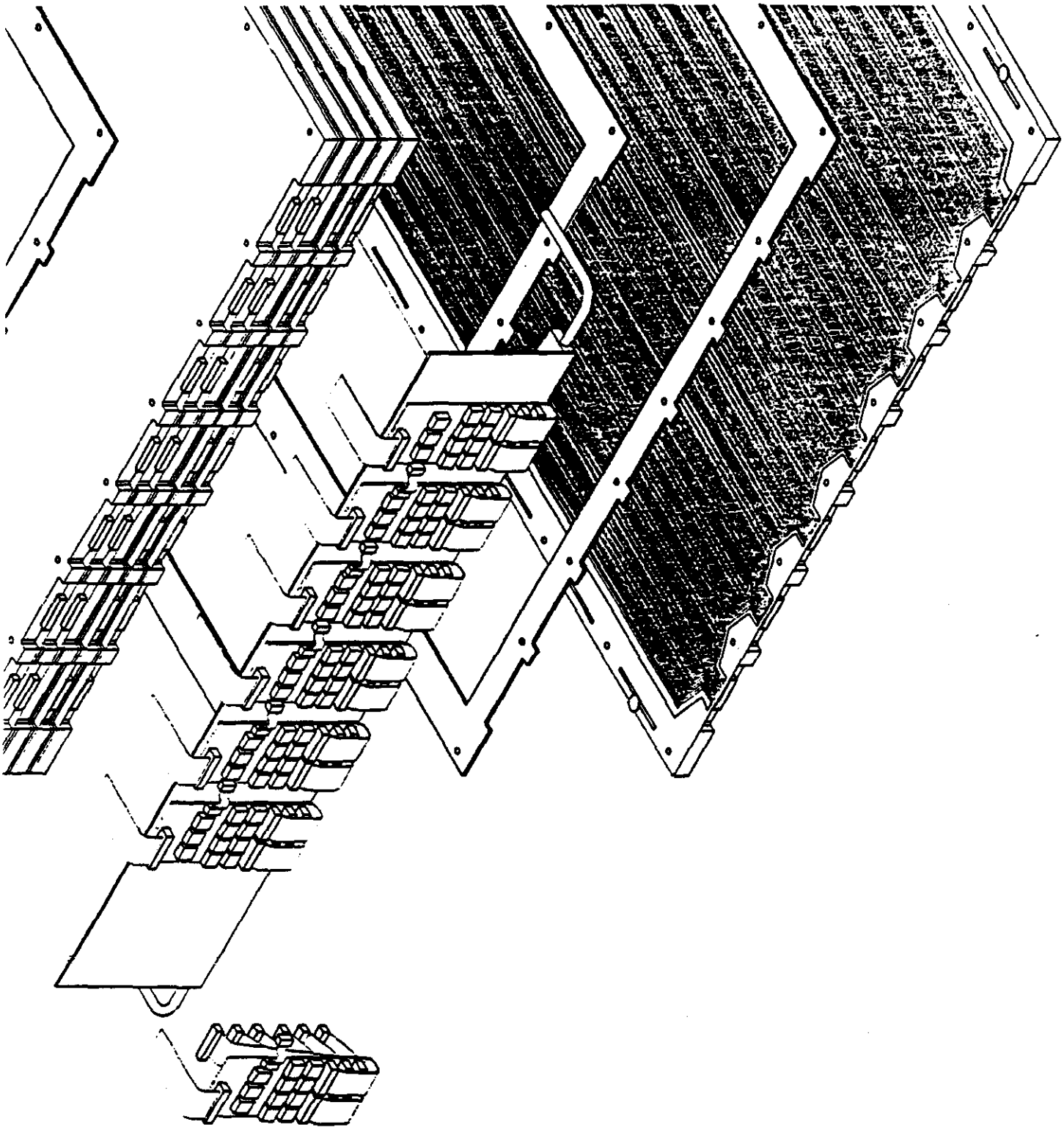


The LCT logic reduces the readout rate to a level where a single 10 MSPS ADC can handle an entire 96-channel FEPCB. Some care must be taken in the way that the multiplexer tree is arranged.

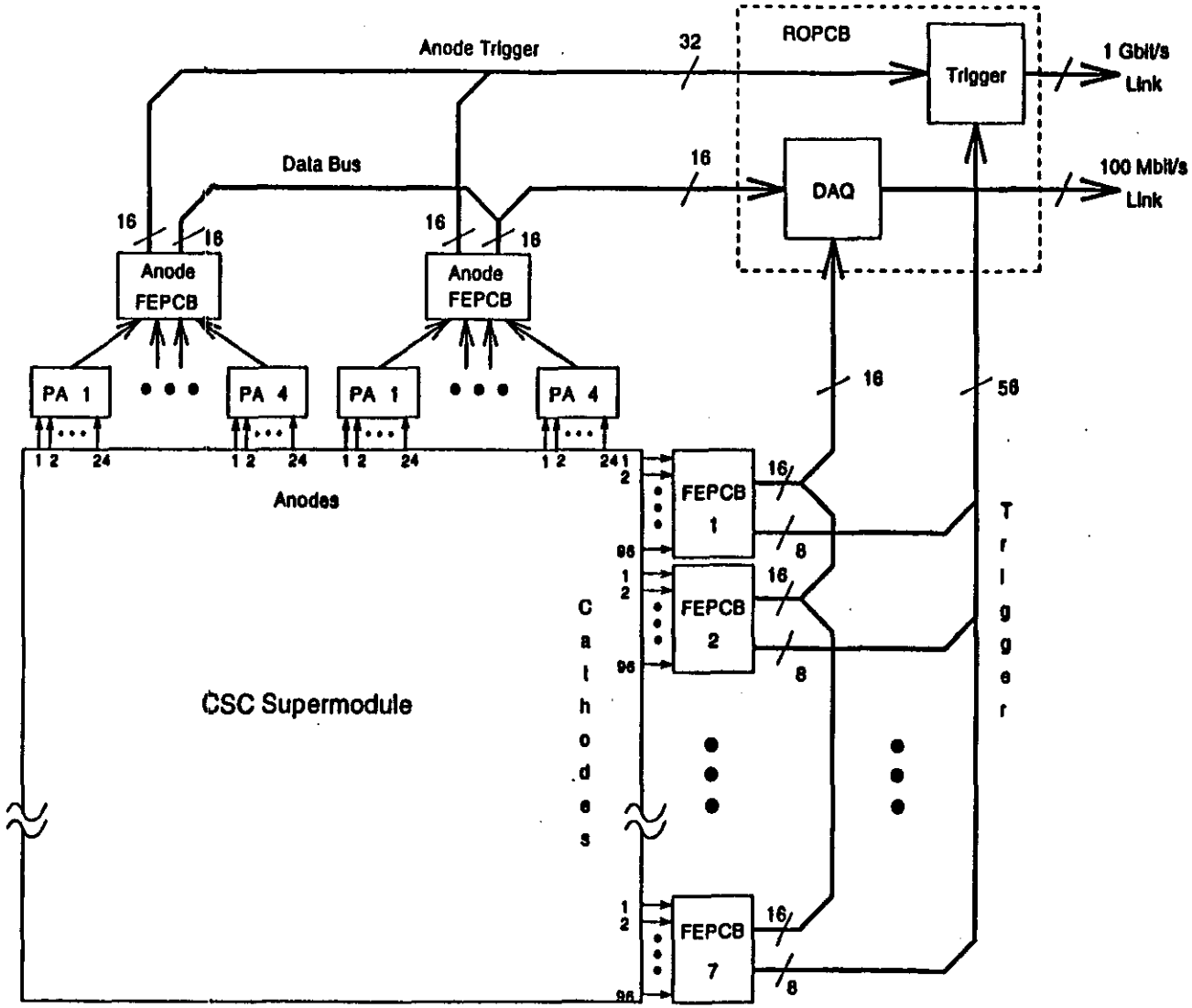
Readout Printed Circuit Board (ROPCB)



This board serves as the interface between the FEPCB's and the DAQ. It also formats, buffers, and retransmits, Level 1 trigger data.

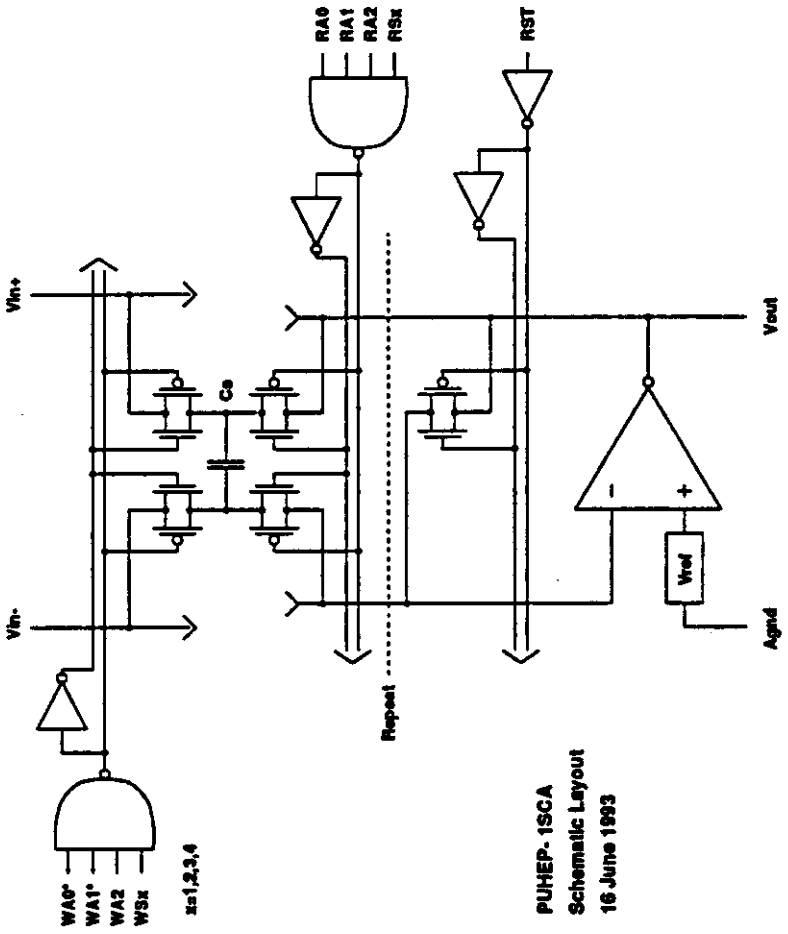


CSC Supermodule Readout Schematic Block Diagram

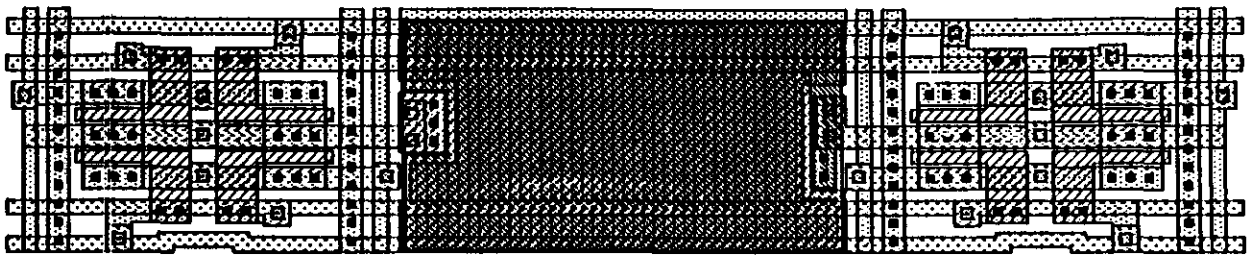


Electrical Specifications for the CSC Readout

Parameter	Value
ENC (100 pF, 300 ns)	$< 2000\ e^-$ rms
Slow Pulse Peaking Time	300 ns
Fast Pulse Peaking Time	30 ns
Overall System Gain	0.4 fC/Count
Dynamic Range	10 bits
Accuracy	0.5%
Cross Talk	< -50 db
Sample Rate	10 MHz
Readout Rate	100 kHz
Readout Latency	$< 100\ \mu$s
Temperature Range	20 ± 5 °C
Power Per Channel	< 100 mW
Rad. Hardness: Ionizing	< 1 krad
Rad. Hardness: Neutrons	10^{14}cm^{-2}


RA0
RA1
RA2
RSx
RST
Vin+
Vin-
Cs
Vout
Vref
Agnd
Repeat
WA0*
WA1*
WA2
WSx
x=1,2,3,4
PUHEP- 1SCA
Schematic Layout
16 June 1993

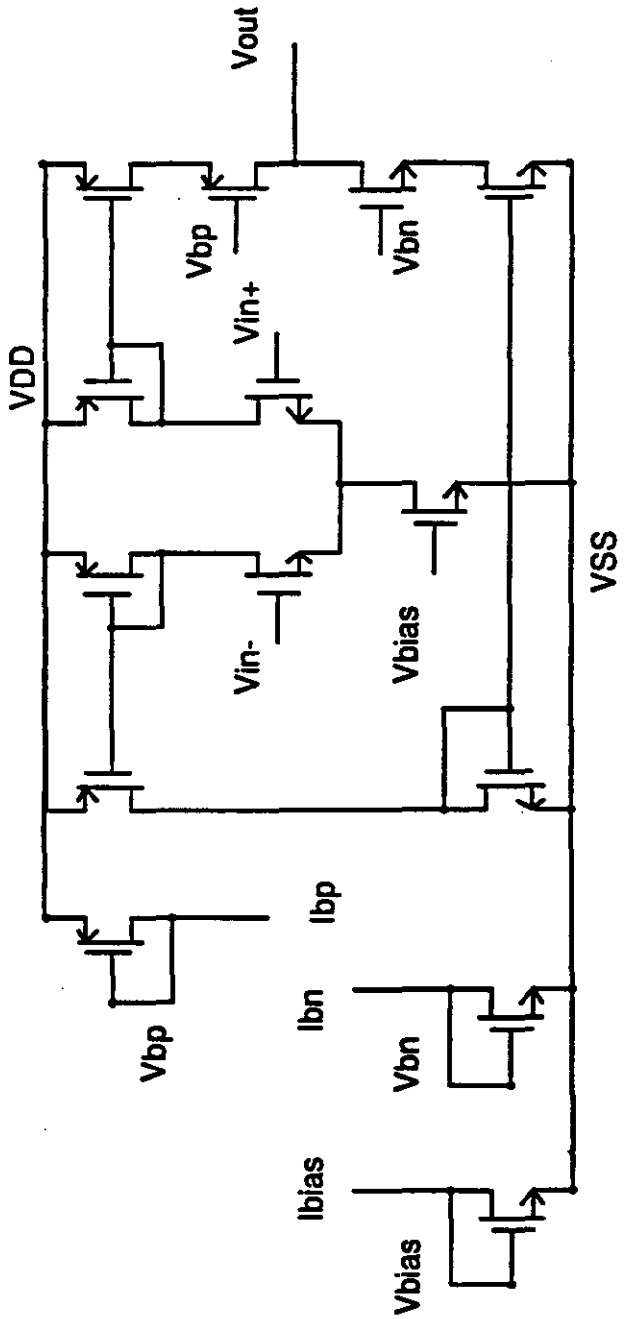
Switched Capacitor Array Memory Cell



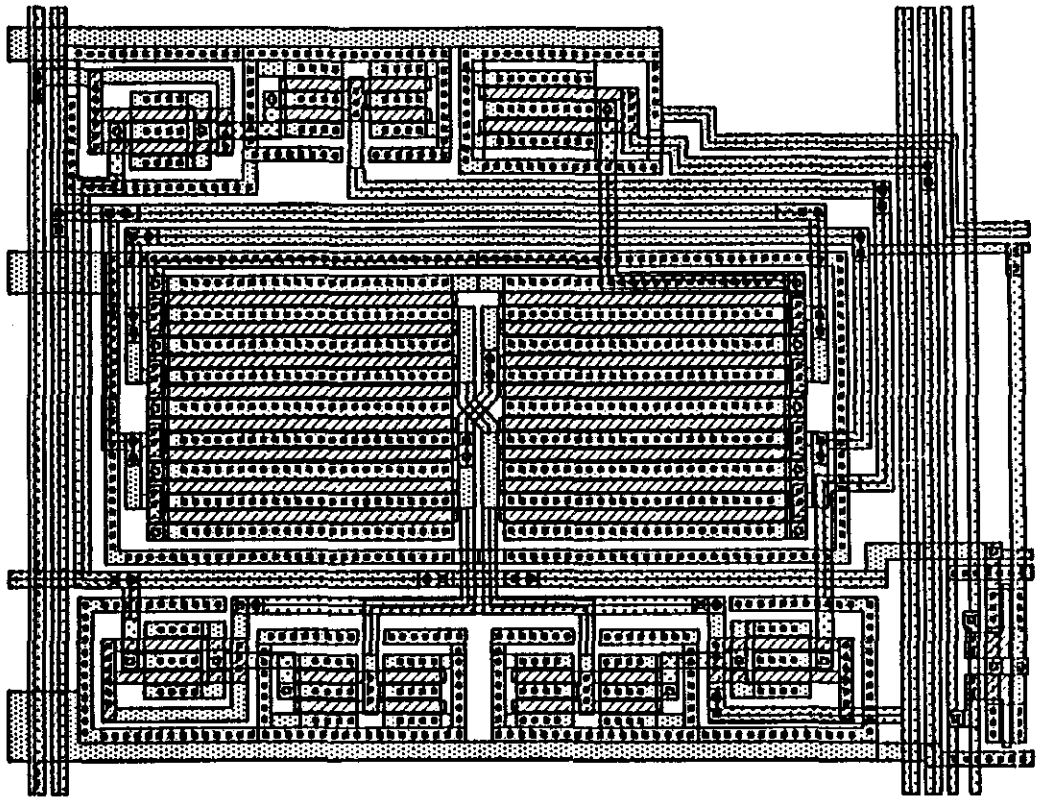
memh, 1000X

204 by 40 microns

SCA AMPLIFIER AND BIAS SCHEMATIC

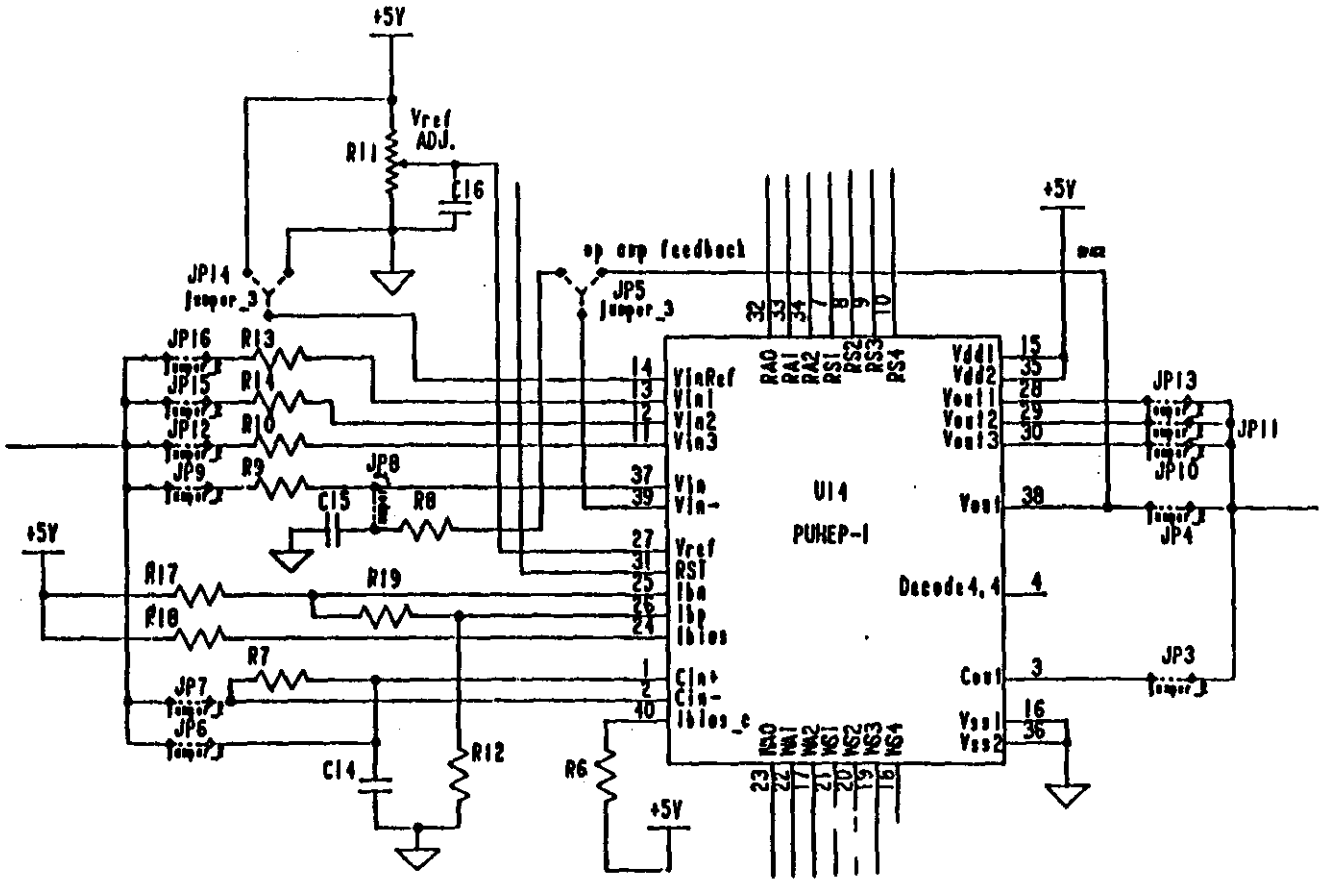


Switched Capacitor Array Amplifier



amprest, 500X

275 by 204 microns


+5V
Vref ADJ.
R11
C16
JP14 Jumper_3
op amp feedback
JP5 Jumper_3
JP16
JP15
JP12
JP9
R13
R14
R10
R9
JP8
C15
R8
+5V
R17
R19
R18
R7
JP7
JP6
C14
R12
R6
+5V
U14
PUHEP-1
VinRef
Vin1
Vin2
Vin3
Vin
Vin-
Vref
RST
Iba
Ibp
Ibias
Cin+
Cin-
Ibias_c
RA0
RA1
RA2
RS1
RS2
RS3
RS4
Vdd1
Vdd2
Vout1
Vout2
Vout3
Vout
Decode4,4
Cout
Vss1
Vss2
+5V
JP13
JP11
JP10
JP4
JP3

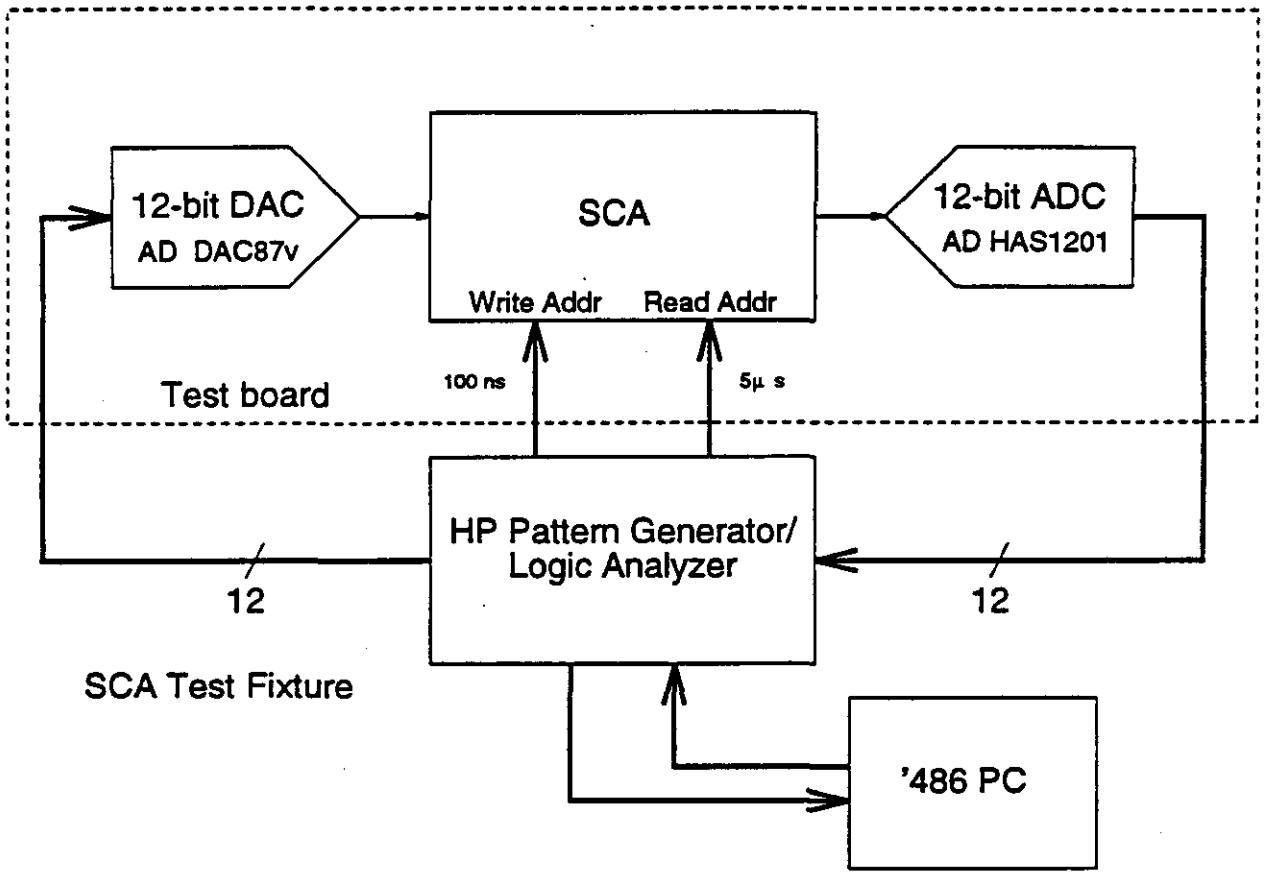
PUHEP-1 Pinouts

1	Cin+ (c)	(c) Ibias	40
2	Cin- (c)	(b) Vin-	39
3	Cout* (c)	(b) Vout	38
4	Decode (4,4) (d)	(b) Vin+	37
5	n/c	VSS2	36
6	n/c	VDD2	35
7	RS1	RA2	34
8	RS2	RA1	33
9	RS3	RA0	32
10	RS4	RST	31
11	Vin3	Vout3	30
12	Vin2	Vout2	29
13	Vin1	Vout1	28
14	VinRef	Vref	27
15	VDD1	Ibp	26
16	VSS1	Ibn	25
17	WA2	Ibias	24
18	WS4	WA0*	23
19	WS3	WA1*	22
20	WS2	WS1	21

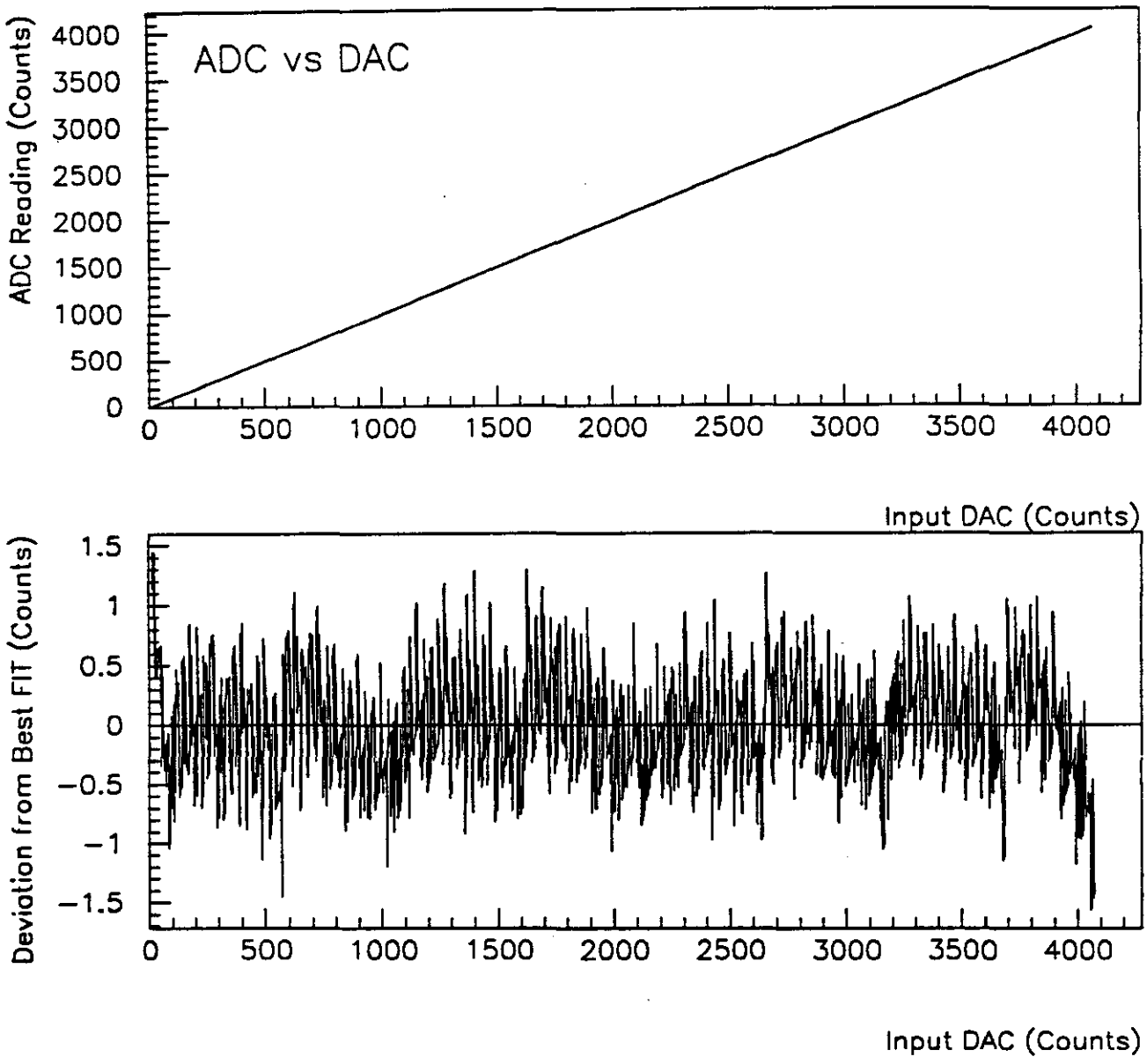
Notes

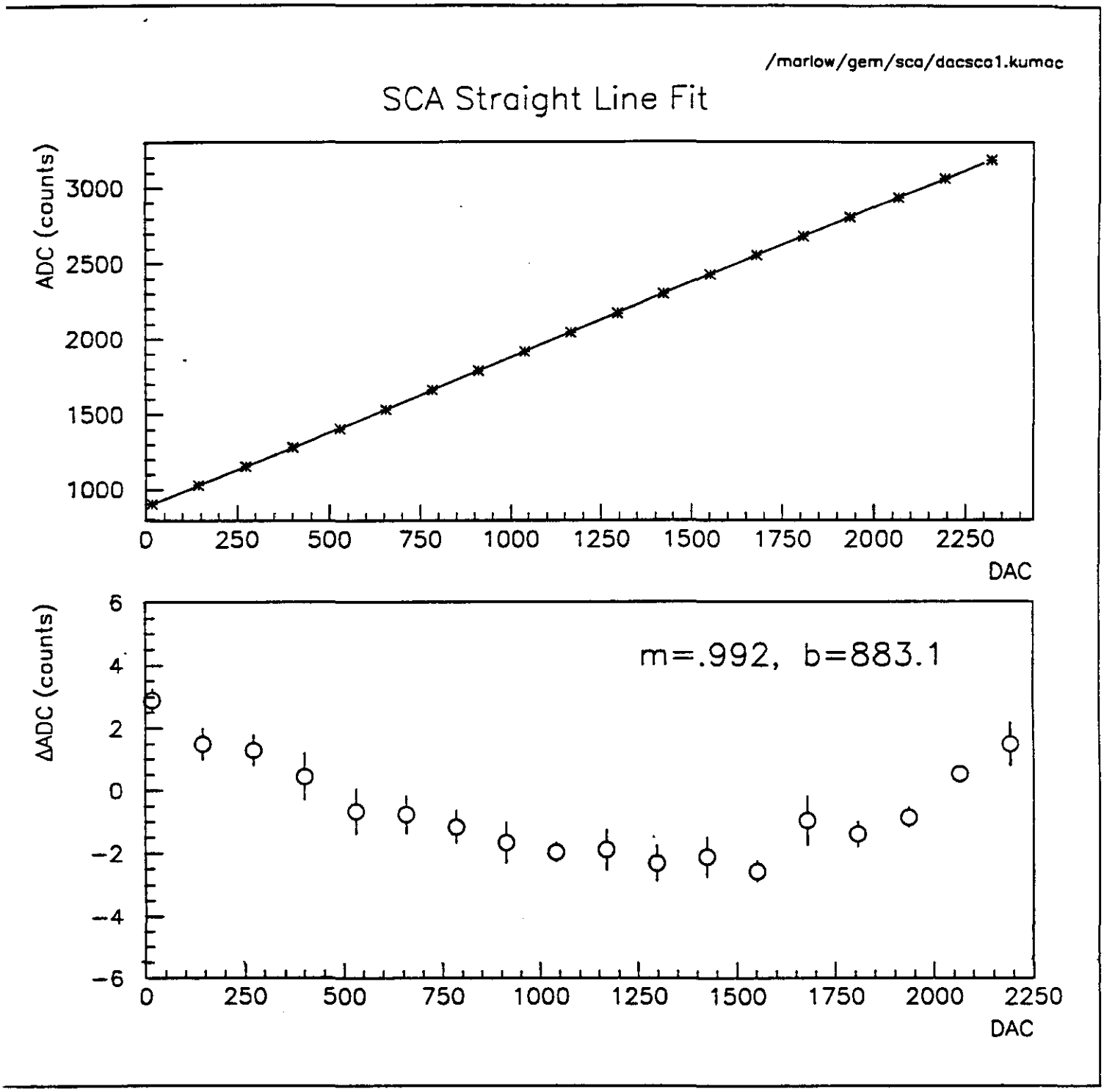
(b) SCA amplifier subcircuit
(c) Comparator subcircuit
(d) Internal address check

Test Setup

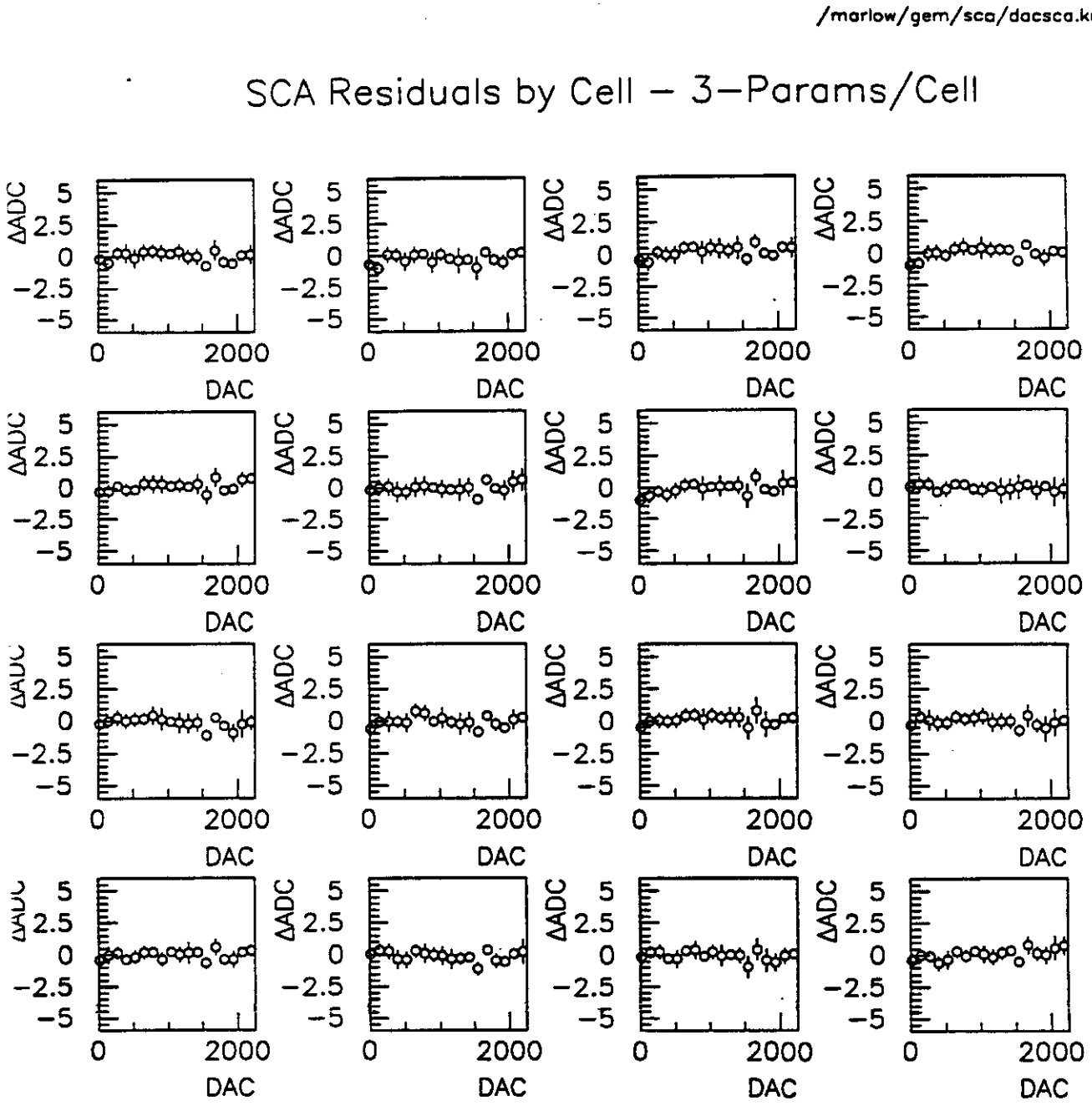


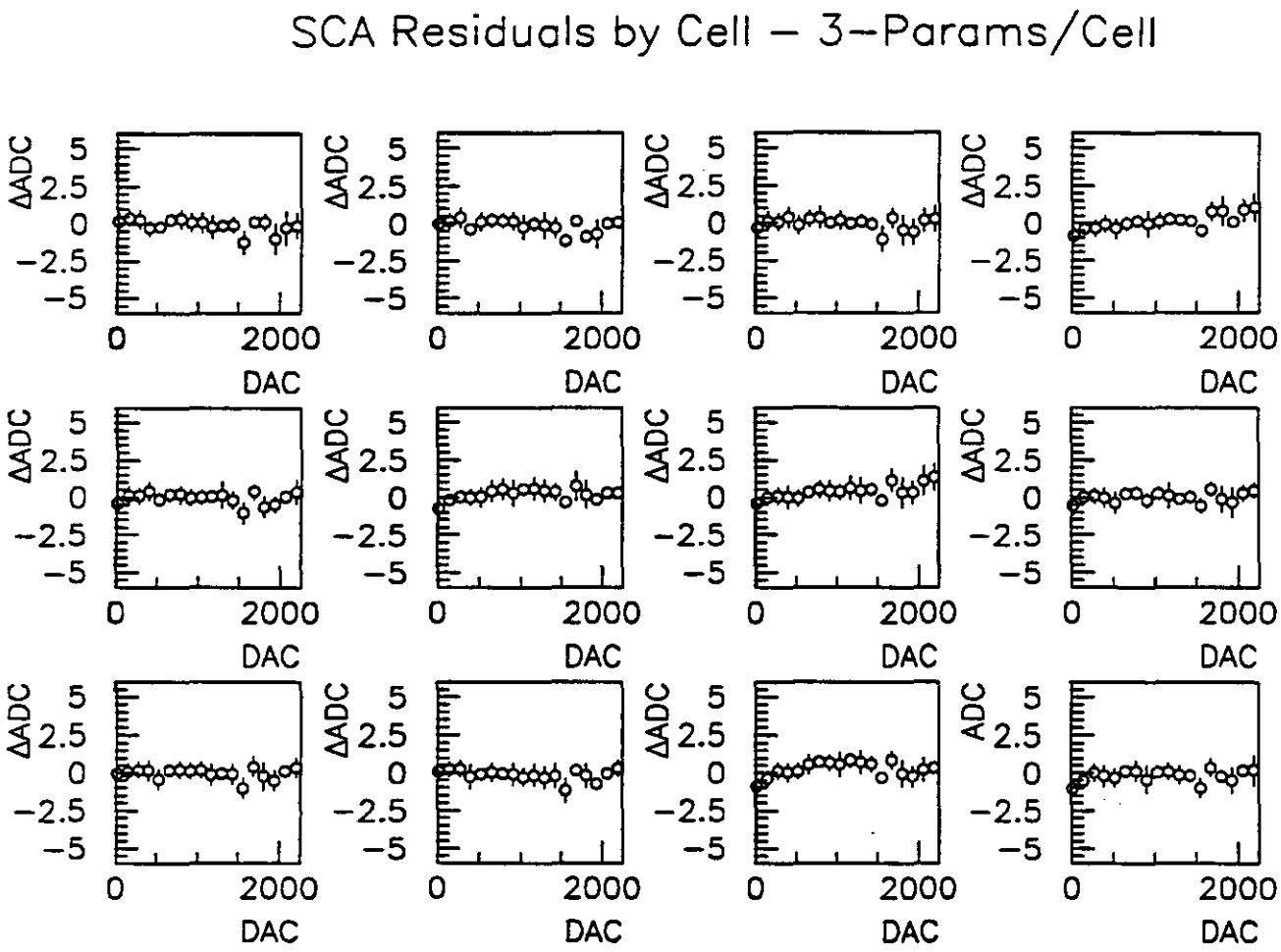
- Current tests use pattern generator to sequentially address the capacitors in the array. Readout follows same sequence and is not (yet) simulataneous with write.
- DAC settling time is 3 μs, so only "quasi-dynamic" tests are possible.

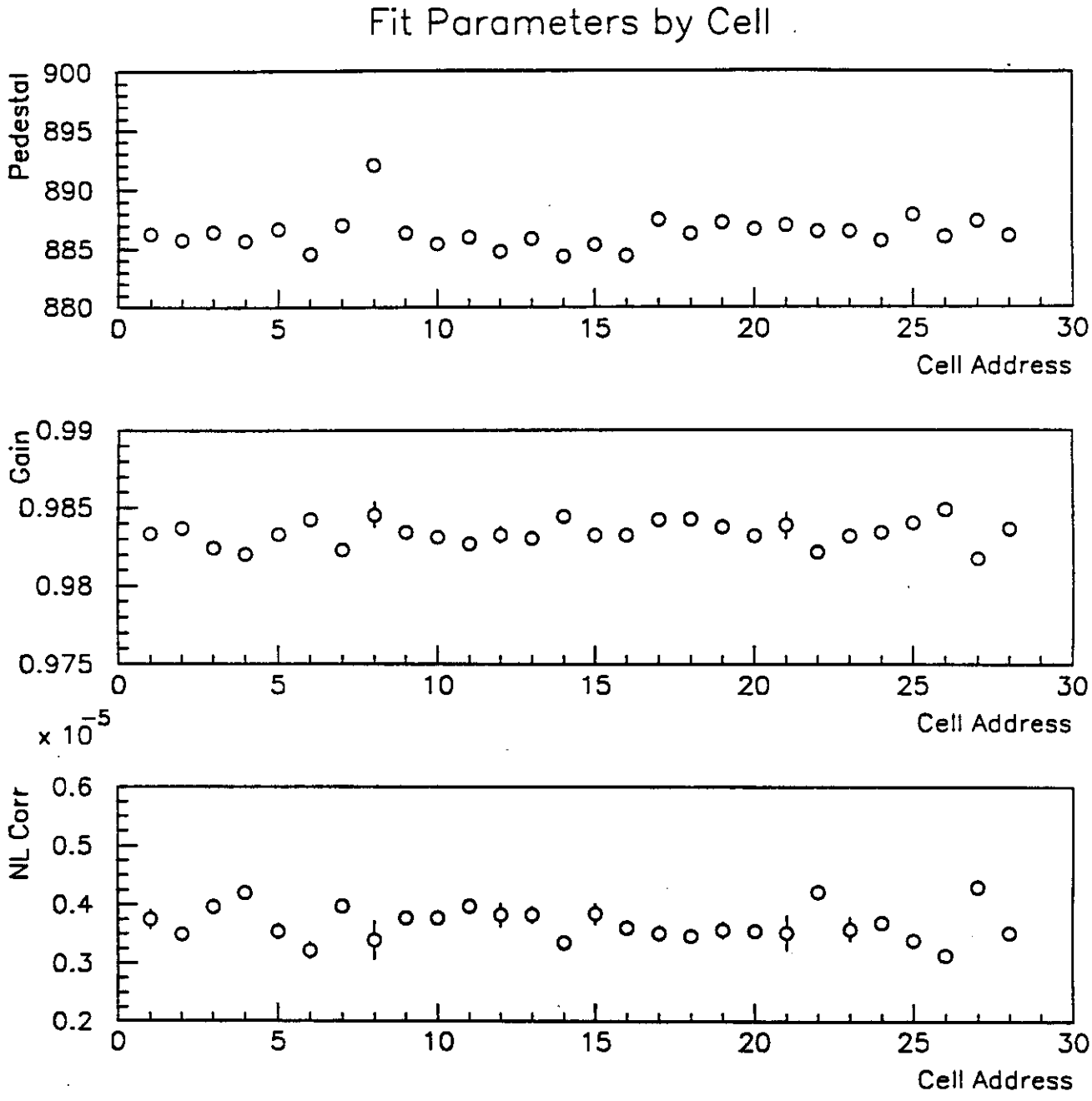

ADC vs DAC
ADC Reading (Counts)
4000
3500
3000
2500
2000
1500
1000
500
0
0
500
1000
1500
2000
2500
3000
3500
4000
Input DAC (Counts)
Deviation from Best FIT (Counts)
1.5
1
0.5
0
−0.5
−1
−1.5
0
500
1000
1500
2000
2500
3000
3500
4000
Input DAC (Counts)


/marlow/gem/sca/dacsca1.kumac
SCA Straight Line Fit
ADC (counts)
3000
2500
2000
1500
1000
0
250
500
750
1000
1250
1500
1750
2000
2250
DAC
ΔADC (counts)
6
4
2
0
−2
−4
−6
m=.992, b=883.1
0
250
500
750
1000
1250
1500
1750
2000
2250
DAC

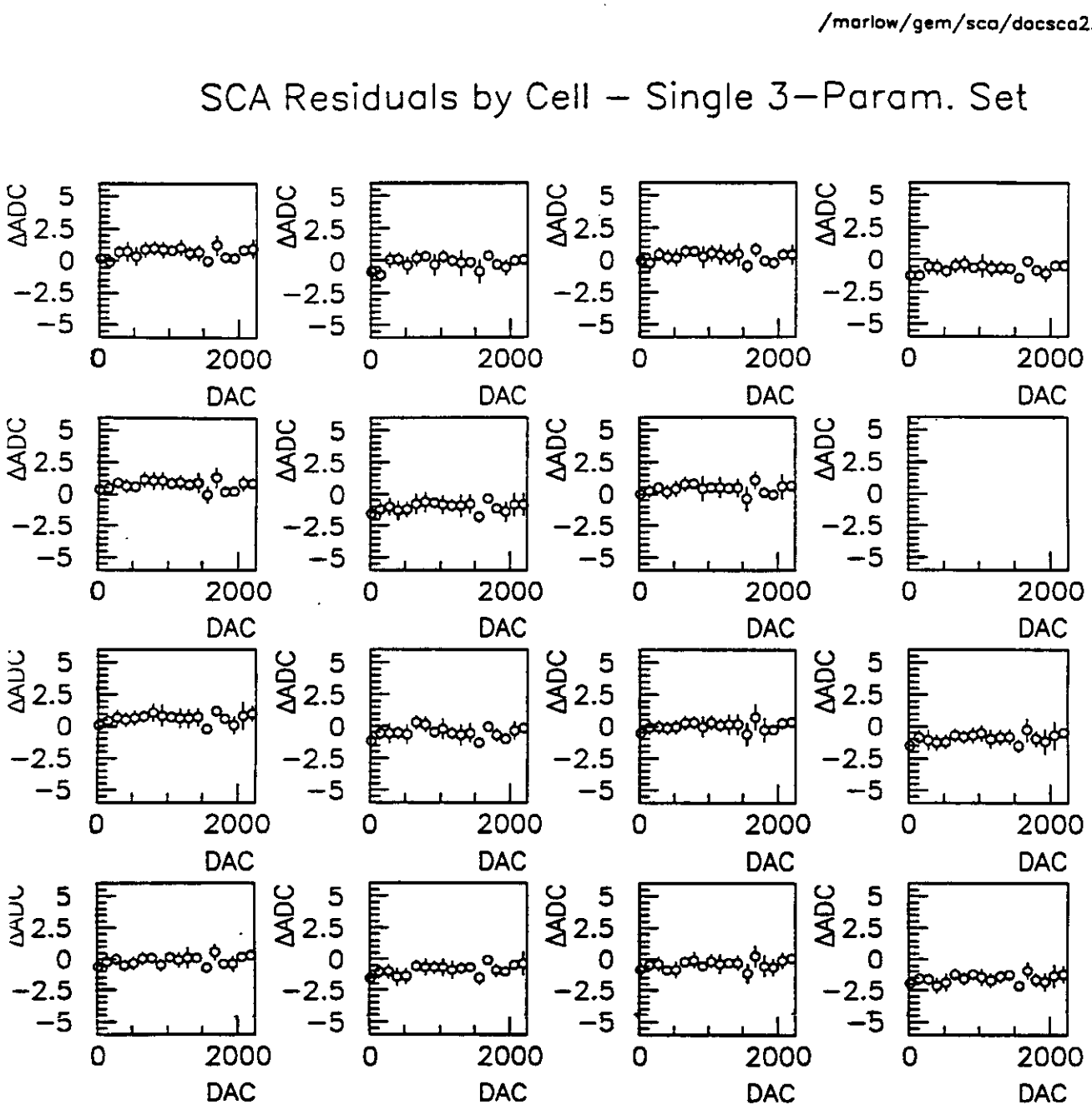
/marlow/gem/sca/dacsca.kumac



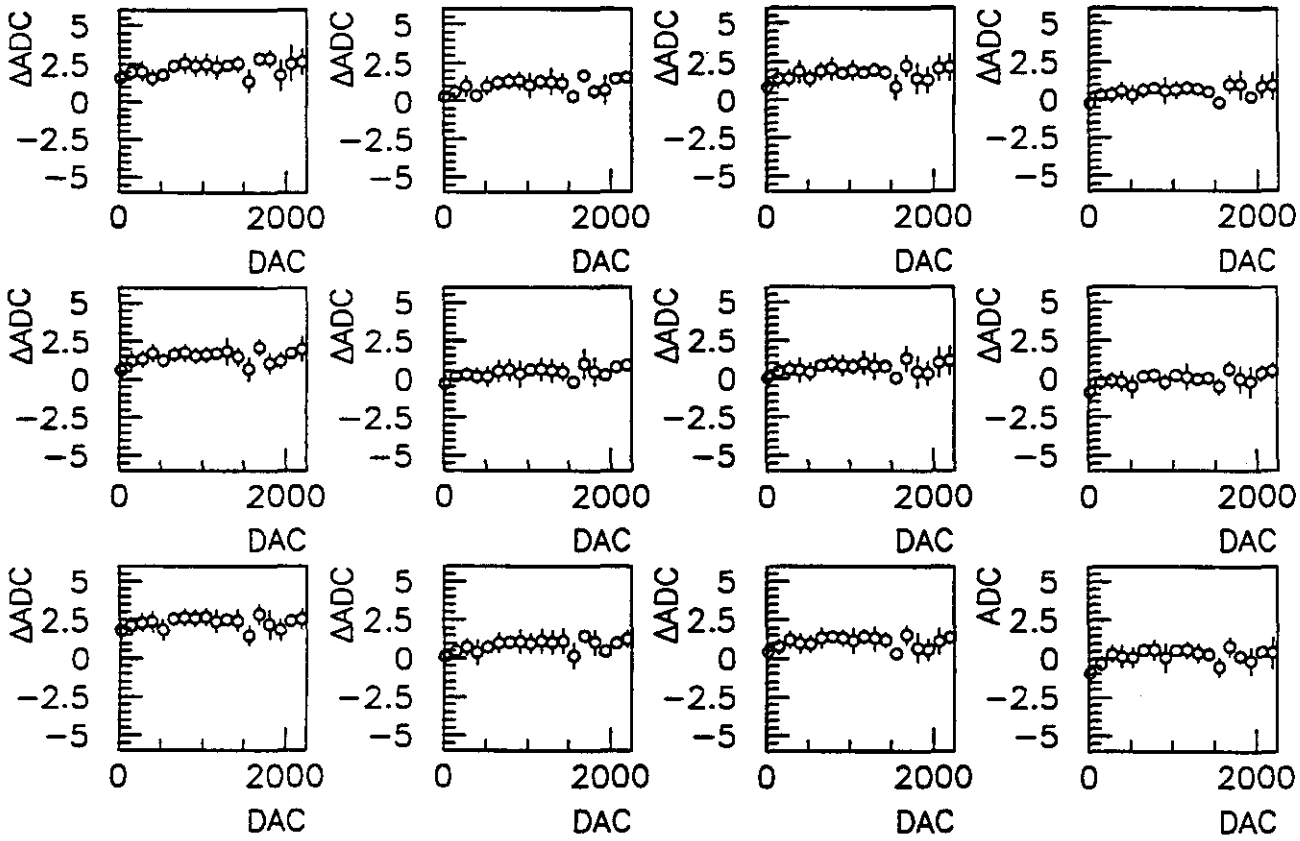

SCA Residuals by Cell – 3–Params/Cell
ΔADC
ADC
5
2.5
0
−2.5
−5
0
2000
DAC


Fit Parameters by Cell
Pedestal
900
895
890
885
880
0
5
10
15
20
25
30
Cell Address
Gain
0.99
0.985
0.98
0.975
0
5
10
15
20
25
30
Cell Address
x 10^-5
NL Corr
0.6
0.5
0.4
0.3
0.2
0
5
10
15
20
25
30
Cell Address

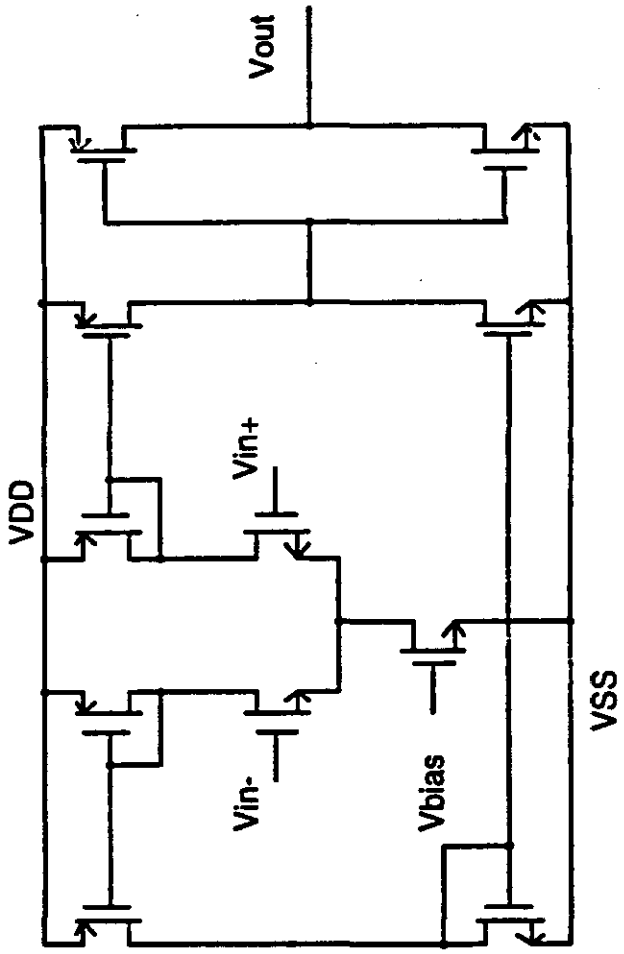
/marlow/gem/sca/docsca2.kumac



SCA Residuals by Cell – Single 3–Param. Set

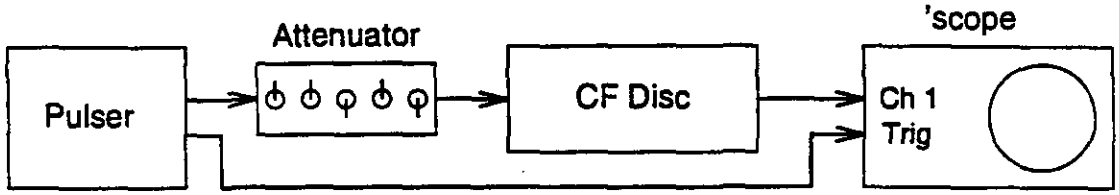


COMPARATOR SCHEMATIC

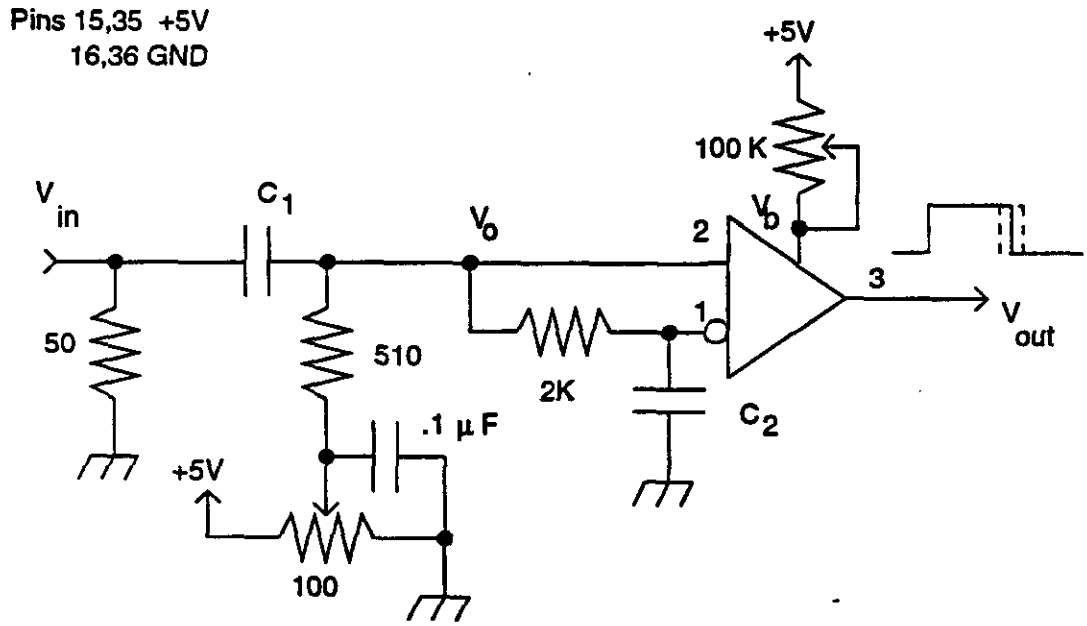


Constant Fraction Discriminator Test Setup

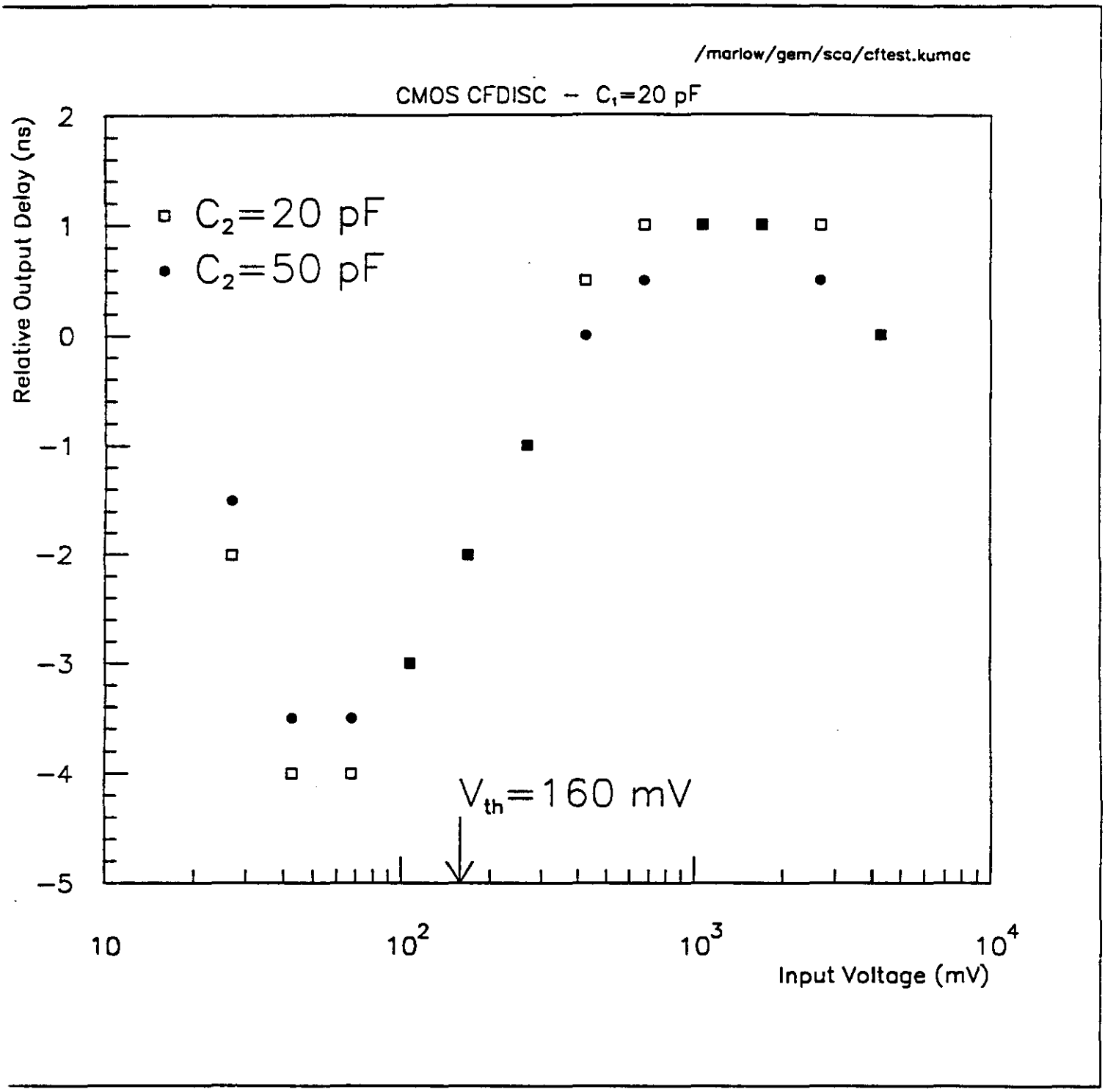
- Test setup is very simple.

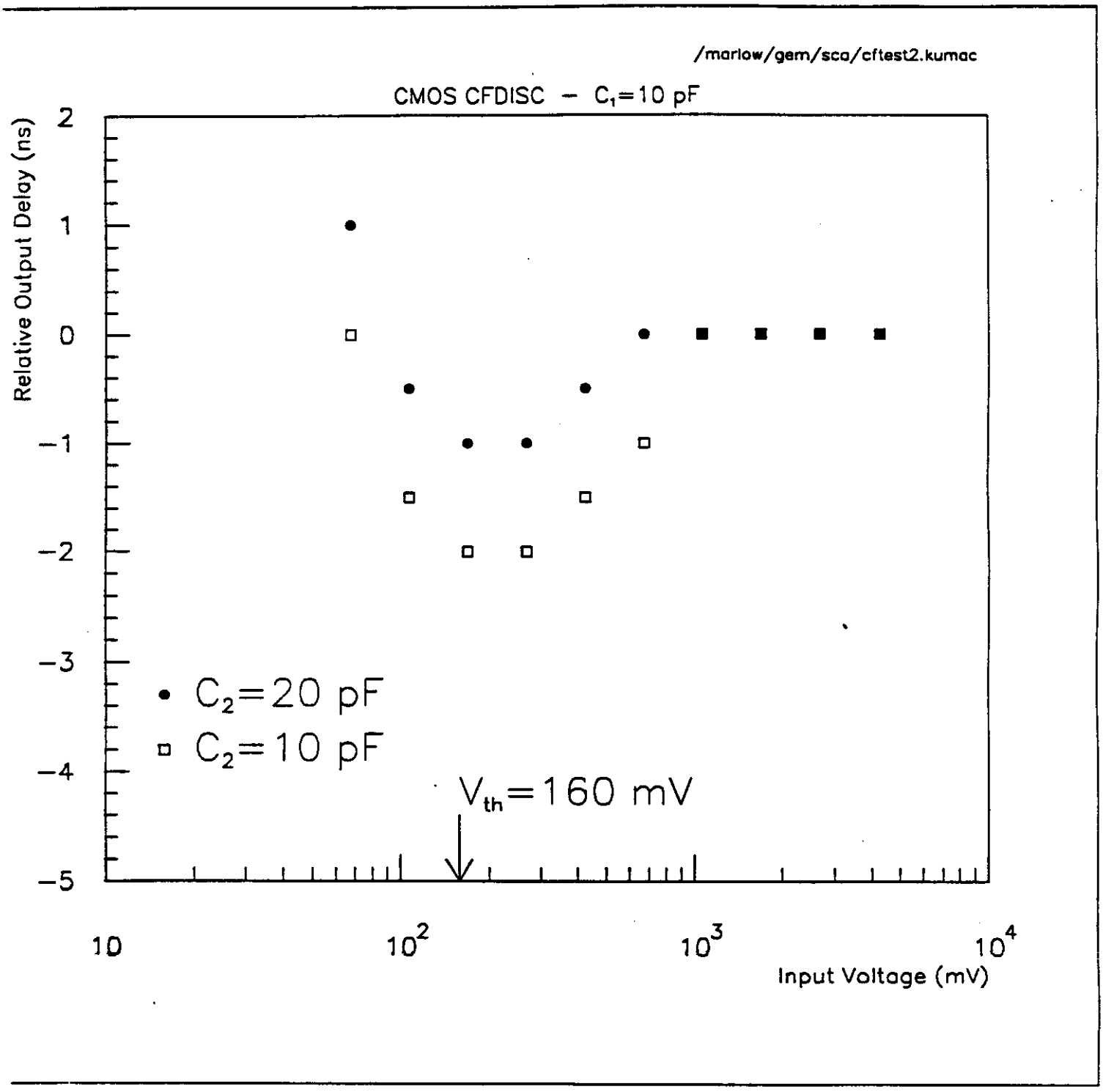


- Use simple RC differentiator to simulate pulse. (More realistic circuit needs to be developed.)



- Measure delay of *trailing* edge with respect to trigger as a function of V_{in}.


/marlow/gem/sca/cftest.kumac
CMOS CFDISC – C1=20 pF
C2=20 pF
C2=50 pF
Vth=160 mV
Relative Output Delay (ns)
Input Voltage (mV)
2
1
0
−1
−2
−3
−4
−5
10
10^2
10^3
10^4


/marlow/gem/sca/cftest2.kumac
CMOS CFDISC – C1=10 pF
Relative Output Delay (ns)
2
1
0
−1
−2
−3
−4
−5
• C2=20 pF
□ C2=10 pF
Vth=160 mV
10
10^2
10^3
10^4
Input Voltage (mV)

FUTURE PLANS

1 Continued testing of other PUHEP-1 devices

2 Integration of PUHEP-1 with the prototype address list processor

3 Further clocknoise testing with the address list processor

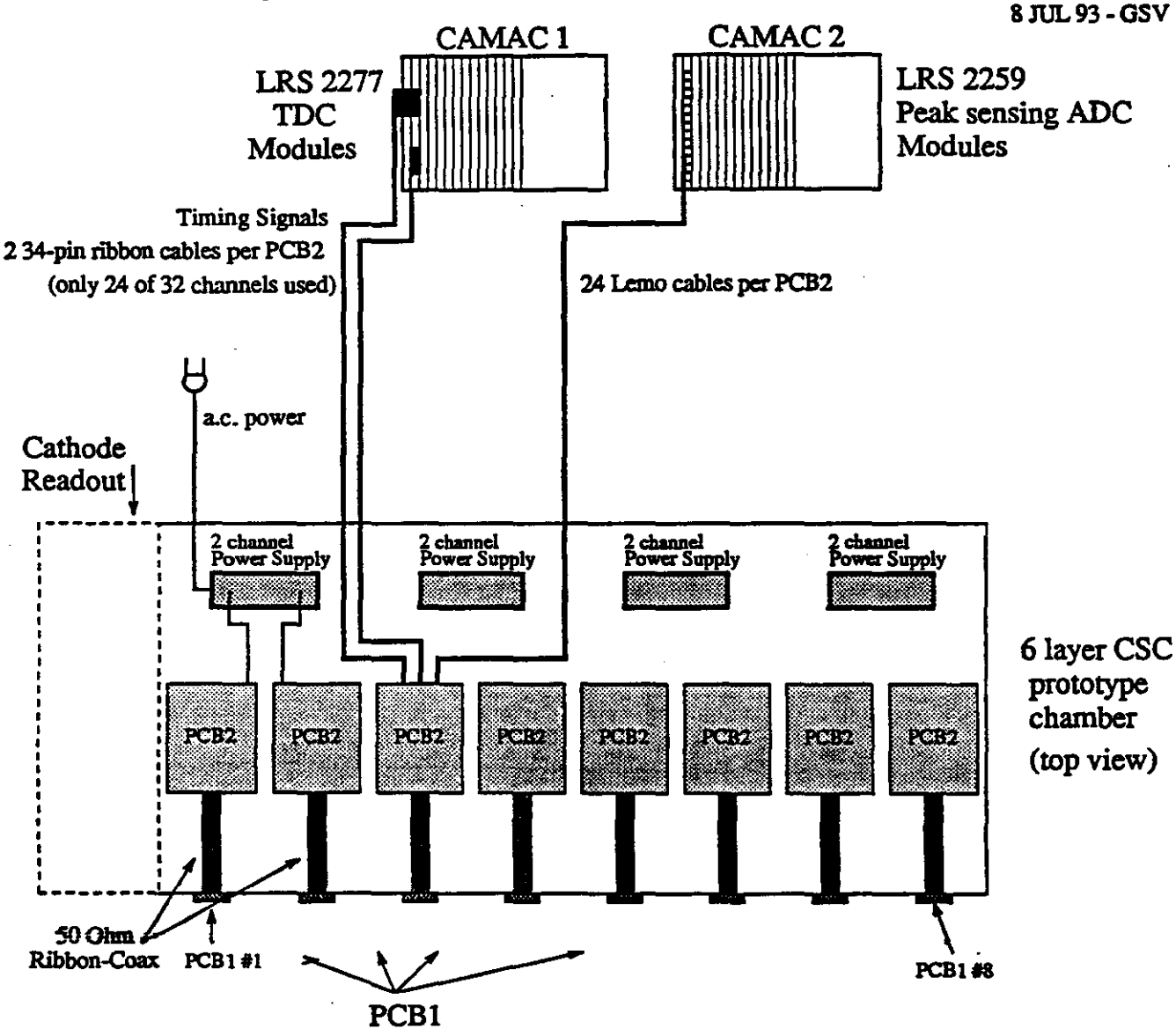
4 Expanded layout (8channels by 28 cells) possible enhancements include modifications to the substrate contacts more clockline shielding and an output mux subcircuit (still tiny chip size)

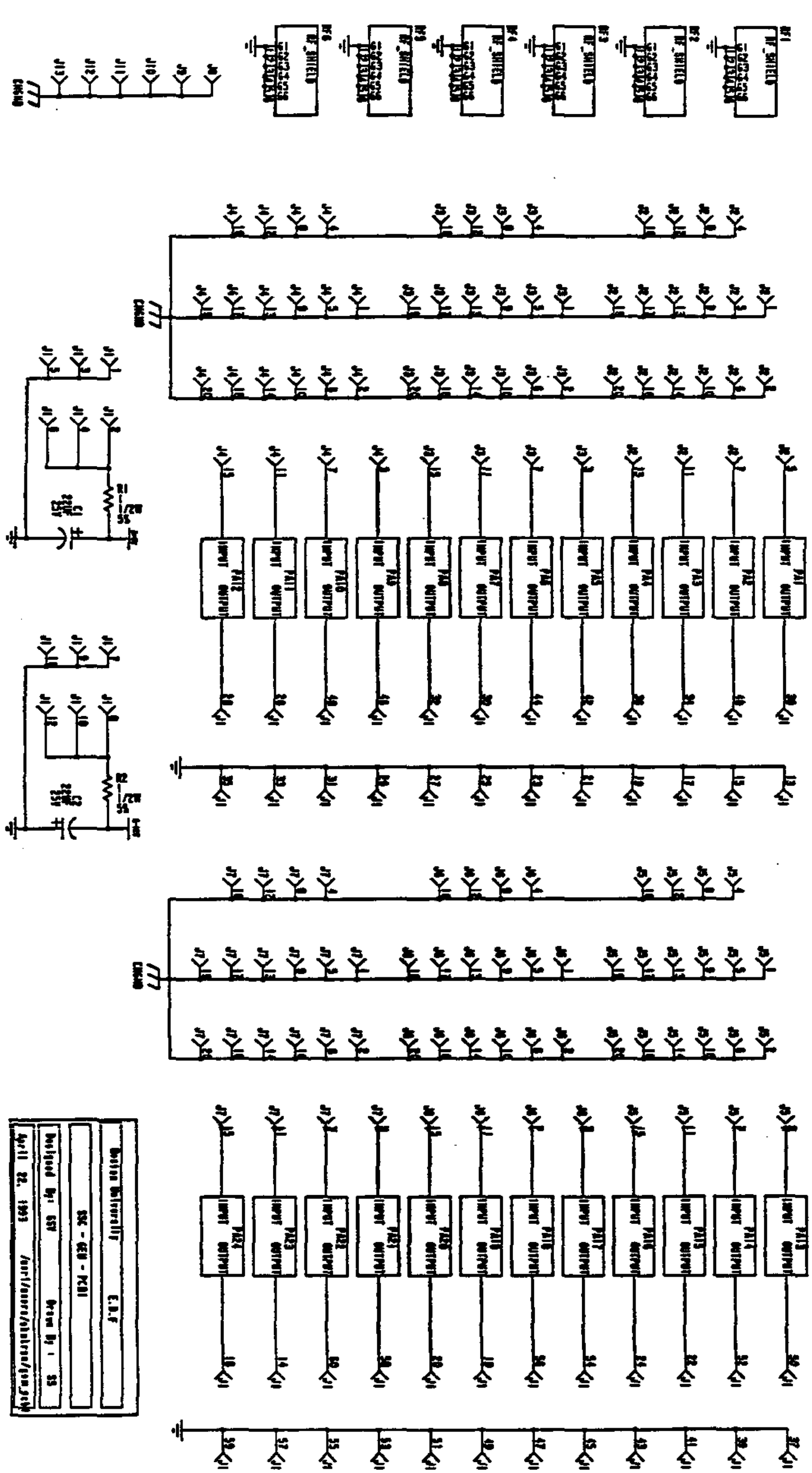
5 LCT trigger generator chip to include multiple discriminators and one or more versions of the track logic subcircuits

6 Full cusotm layout of the address list processor

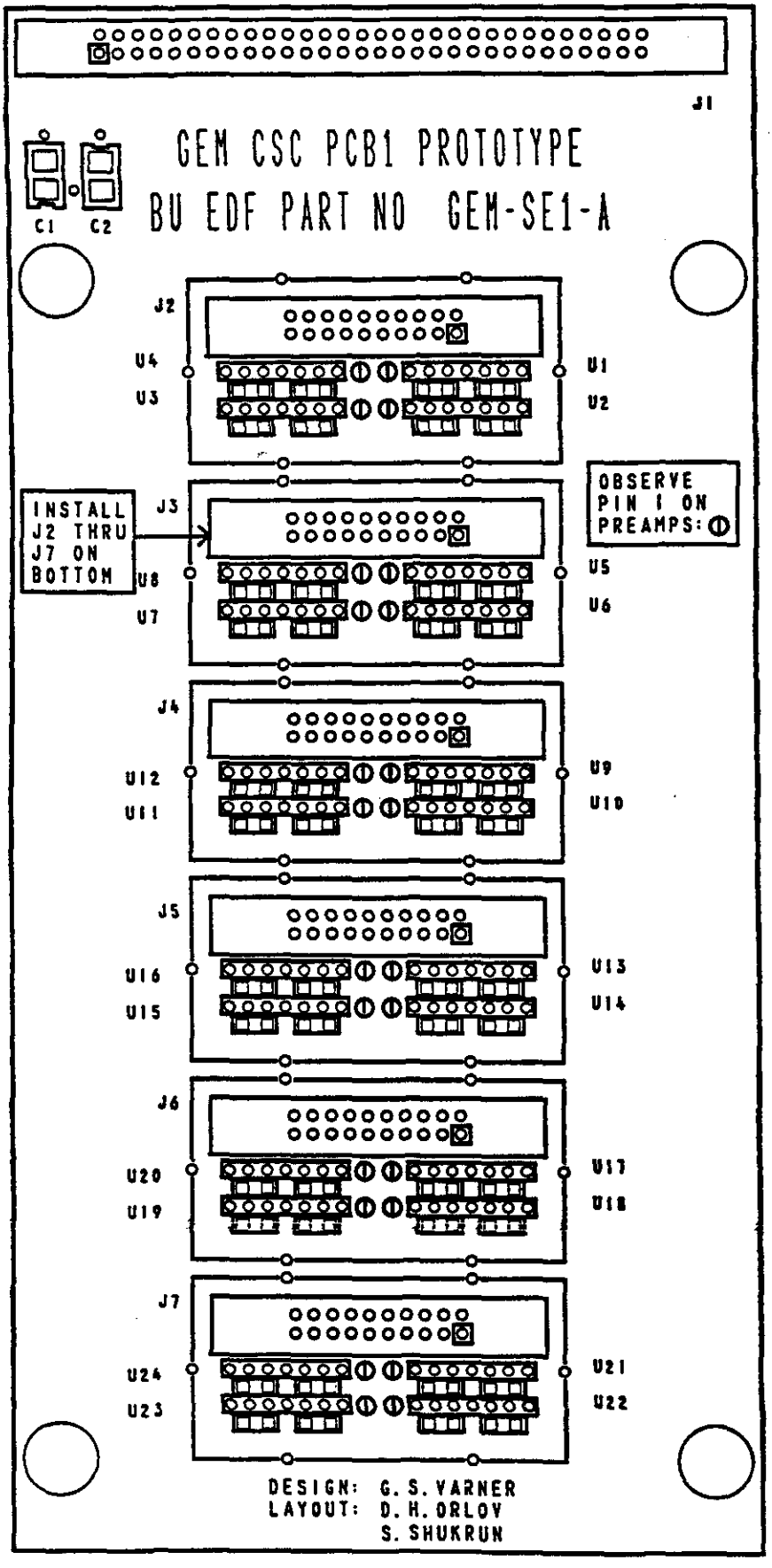
Wiring Schematic - CSC Anode Readout Electronics

8 JUL 93 - GSV

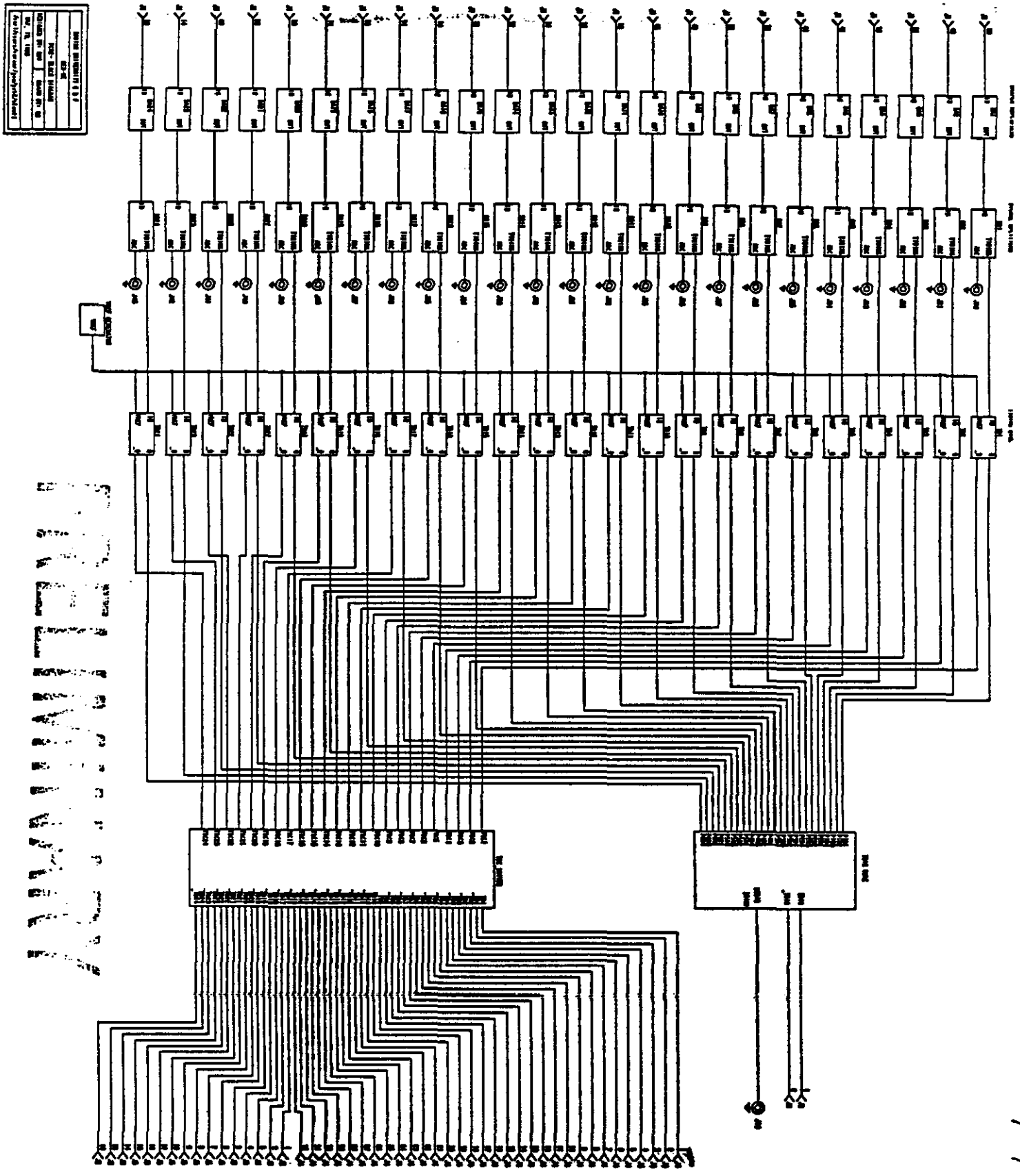



Boston University
E.D.F
Designed By: GSP
Drawn By : SS
April 22, 1993

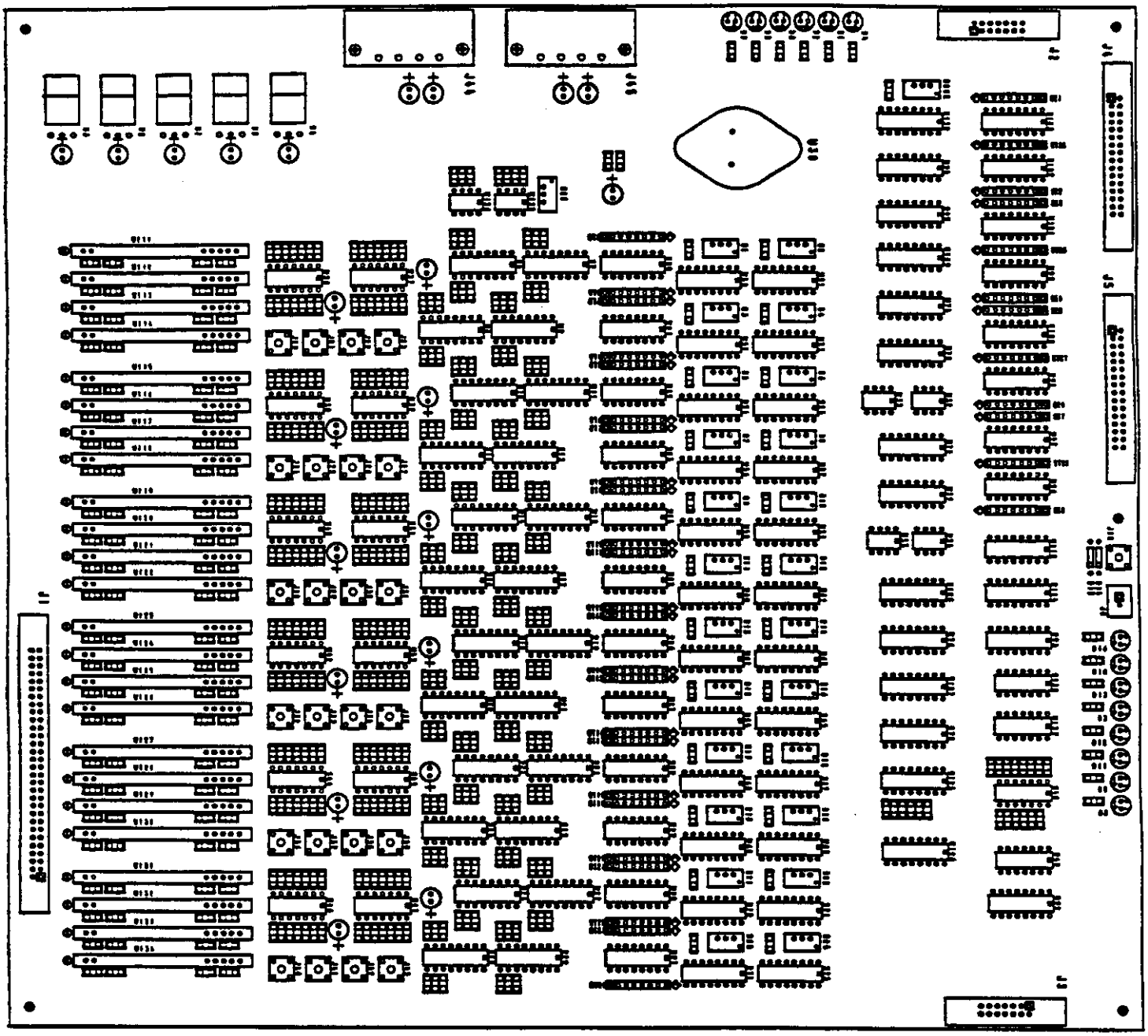
GEM-SE1-A



SILKSCREEN



11 am 7/15/93 P.O.



GEMSE2-A

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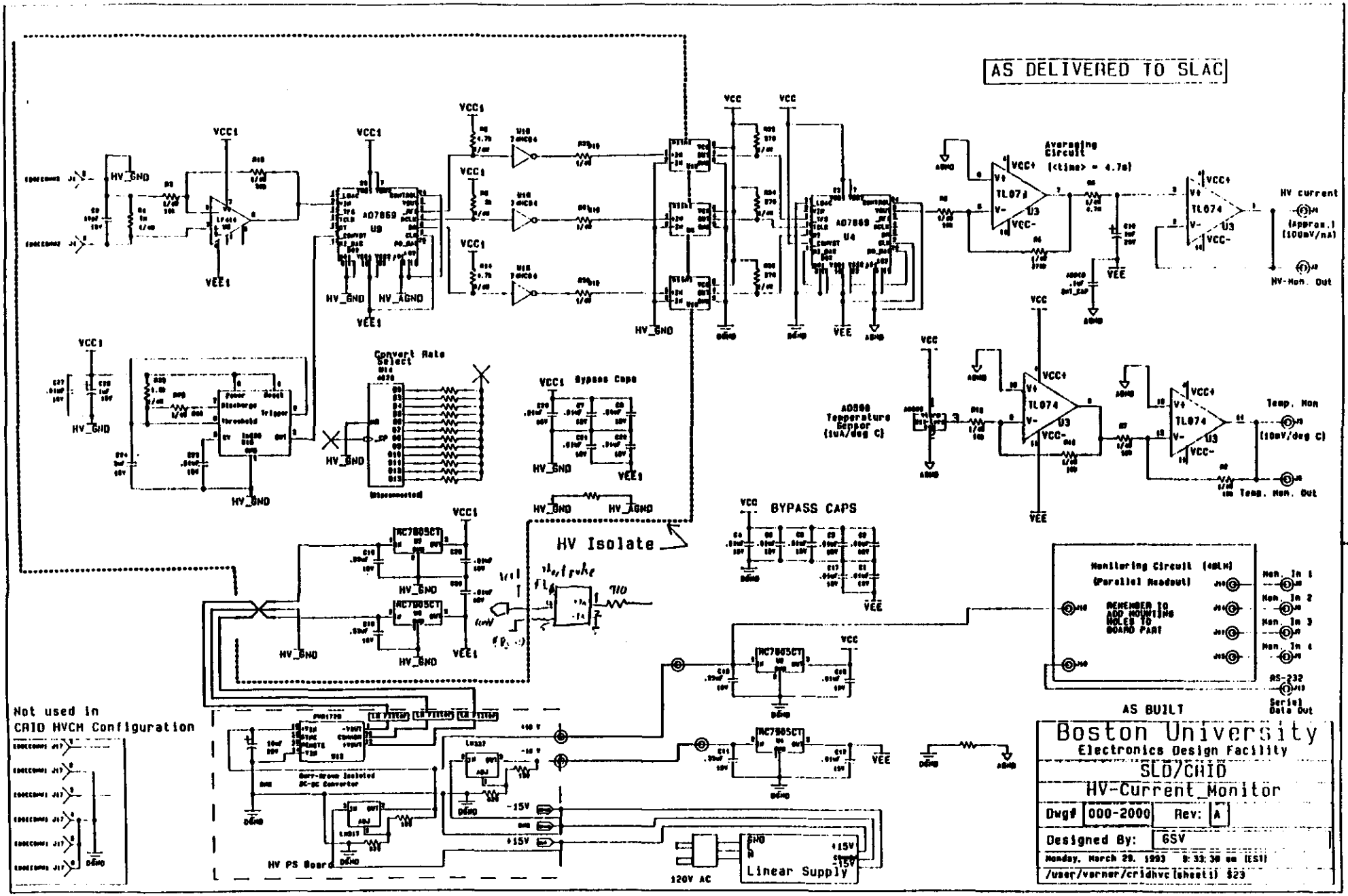
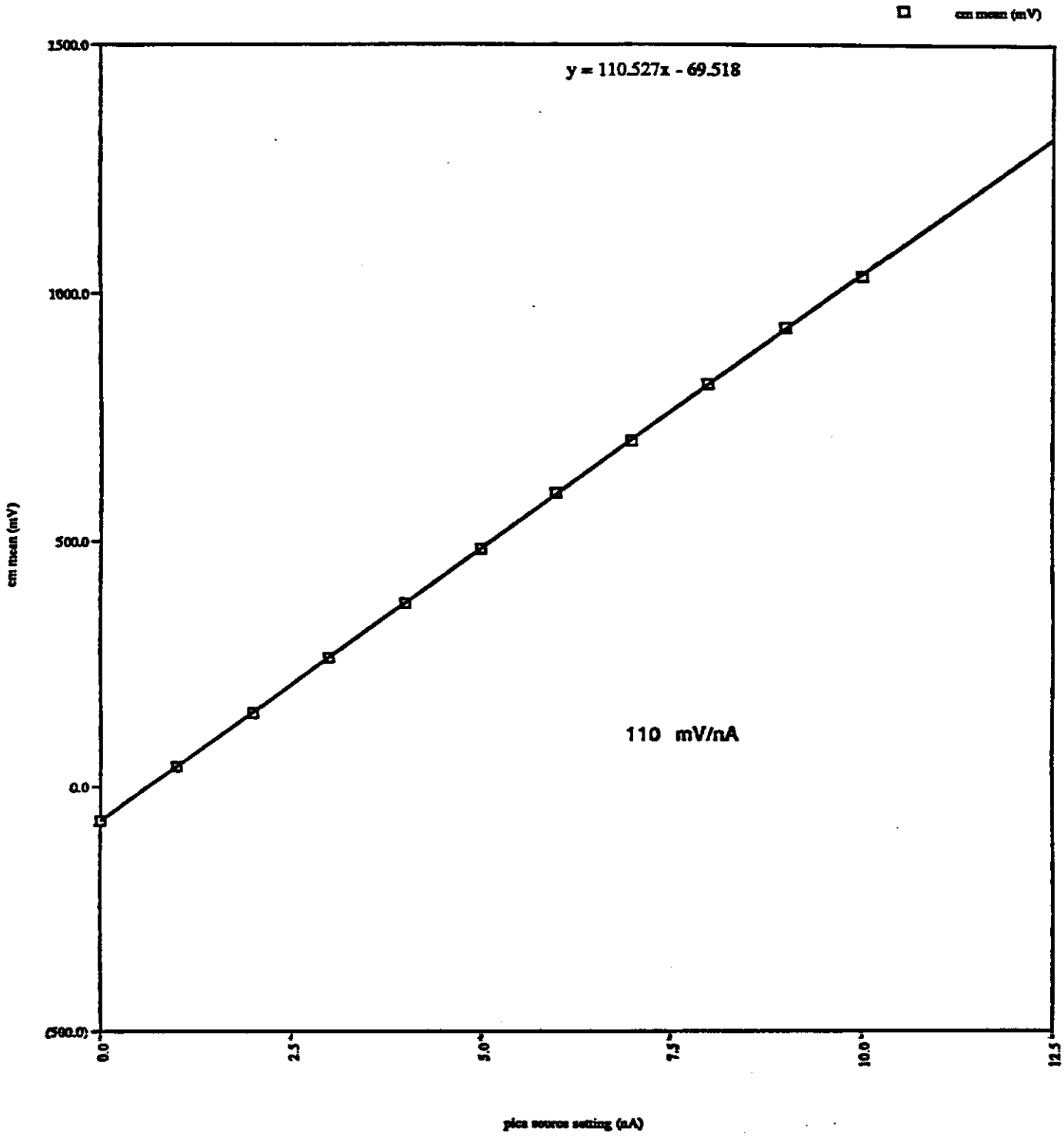
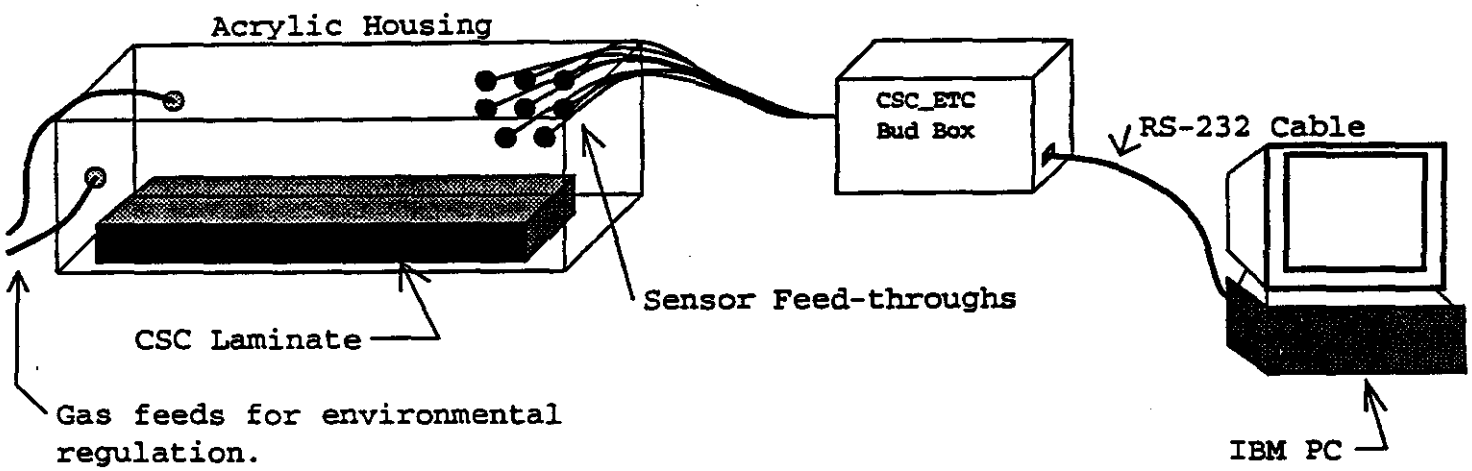

AS DELIVERED TO SLAC
HV_GND
VCC1
VEE1
AD7869
Averaging Circuit
HV current
(approx.)
(100mV/nA)
HV-Non. Out
Convert Rate Select
Disconnected
VCC1 Bypass Caps
AD590 Temperature Sensor (1uA/deg C)
Temp. Non
(10mV/deg C)
Temp. Non. Out
HV_AGND
HV Isolate
BYPASS CAPS
Monitoring Circuit (cBLH)
(Parallel Readout)
REMEMBER TO ADD MOUNTING HOLES TO BOARD PART
Non_In 1
Non_In 2
Non_In 3
Non_In 4
RS-232
Serial Data Out
AS BUILT
Not used in CRID HVCH Configuration
HV PS Board
Linear Supply
120V AC
Boston University
Electronics Design Facility
SLD/CRID
HV-Current_Monitor
Dwg# 000-2000
Rev: A
Designed By: GSV
Monday, March 29, 1993 9:33:30 am (EST)
/user/varner/cridhvc[sheet1] $23

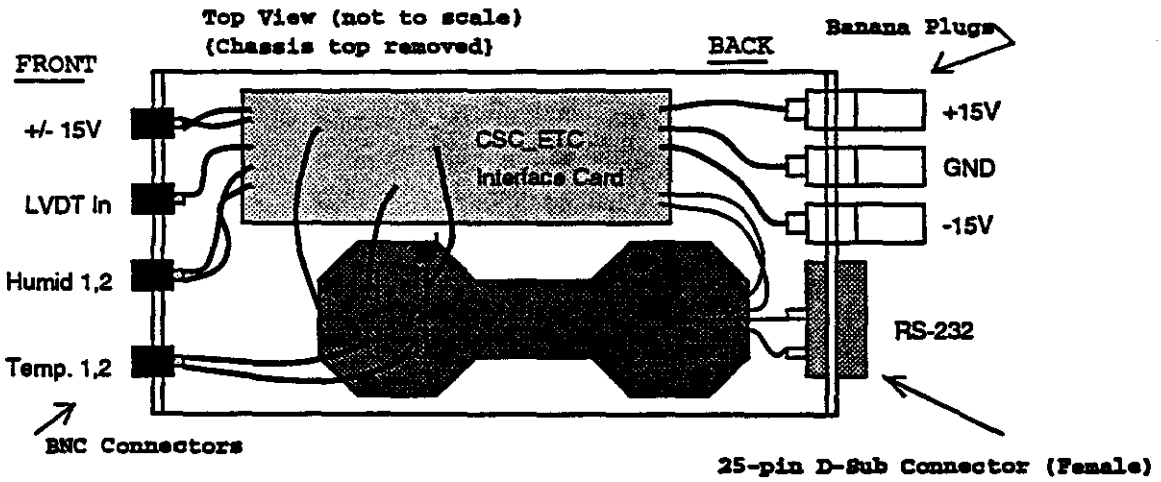
cm5 data wrksht txt

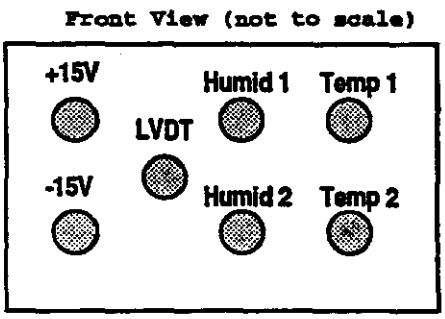


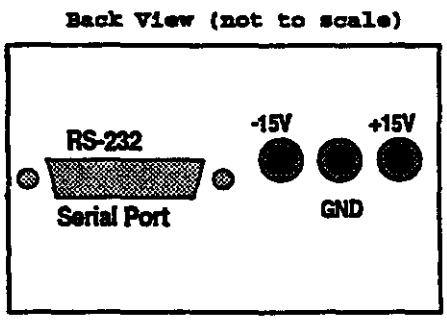
CSC Environmental Test Chamber

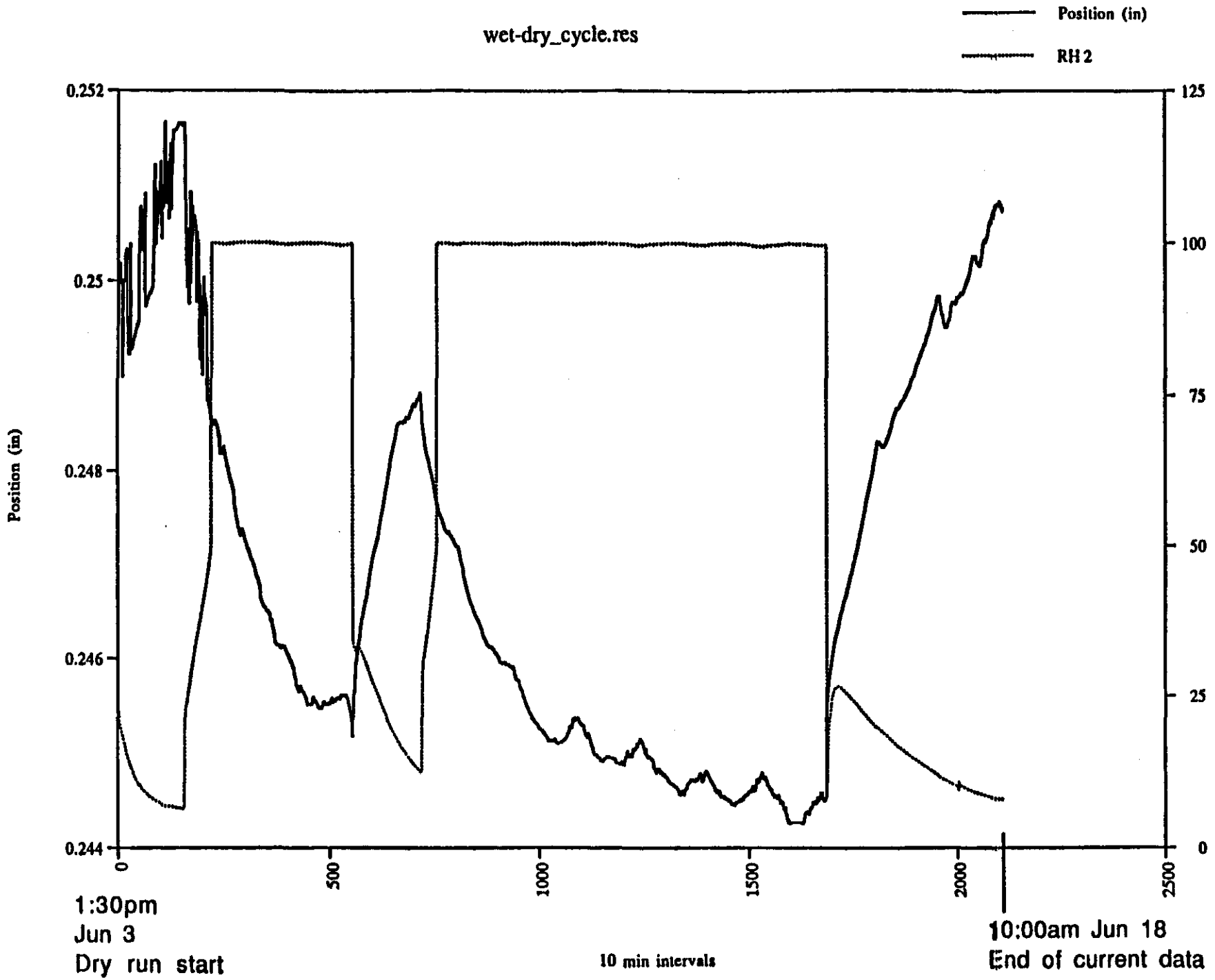


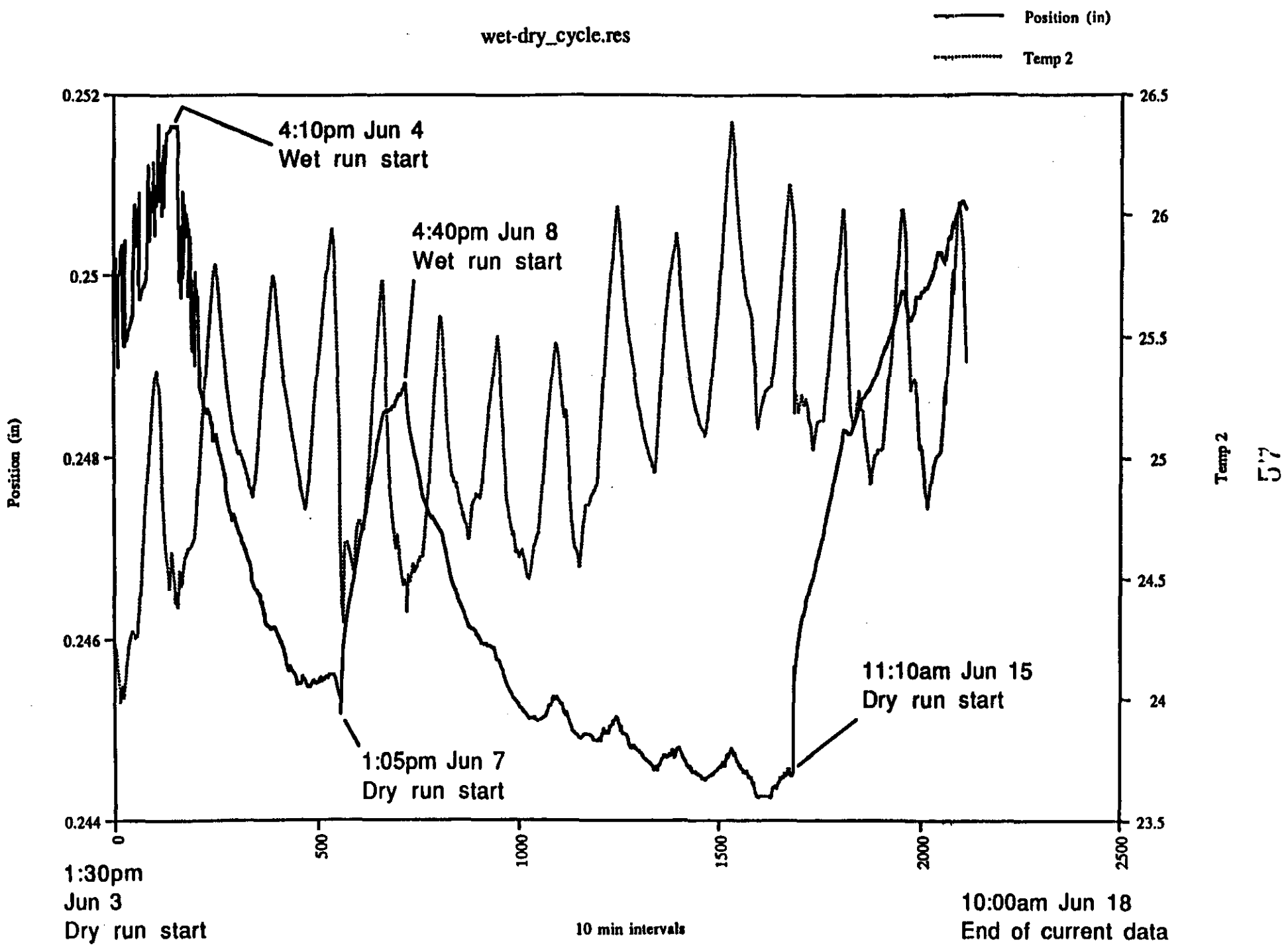
CSC Environmental Test Chamber Readout Box

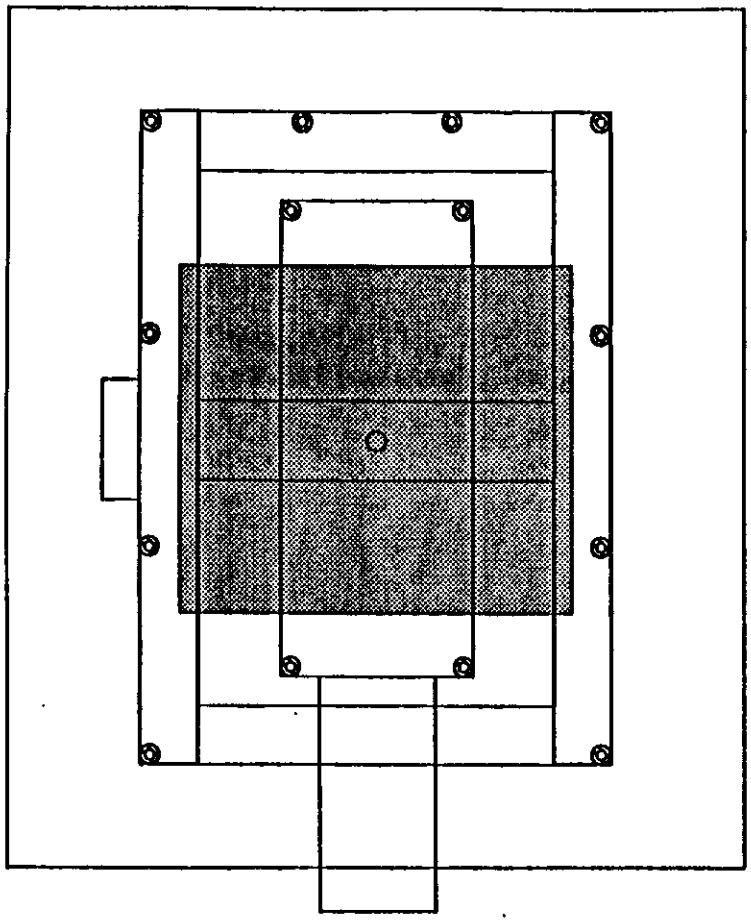


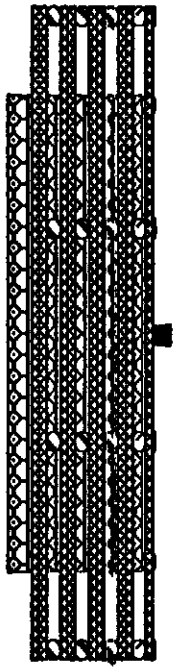


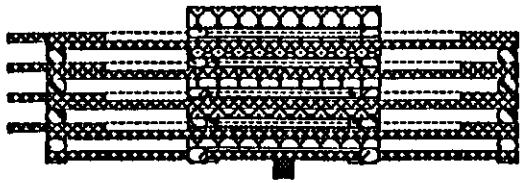



wet-dry_cycle.res
Position (in)
RH 2
0.252
0.25
0.248
0.246
0.244
125
100
75
50
25
0
0
500
1000
1500
2000
2500
Position (in)
RH 2
10 min intervals
1:30pm
Jun 3
Dry run start
10:00am Jun 18
End of current data


wet-dry_cycle.res
Position (in)
Temp 2
0.252
0.25
0.248
0.246
0.244
26.5
26
25.5
25
24.5
24
23.5
4:10pm Jun 4
Wet run start
4:40pm Jun 8
Wet run start
1:05pm Jun 7
Dry run start
11:10am Jun 15
Dry run start
0
500
1000
1500
2000
2500
1:30pm
Jun 3
Dry run start
10 min intervals
10:00am Jun 18
End of current data

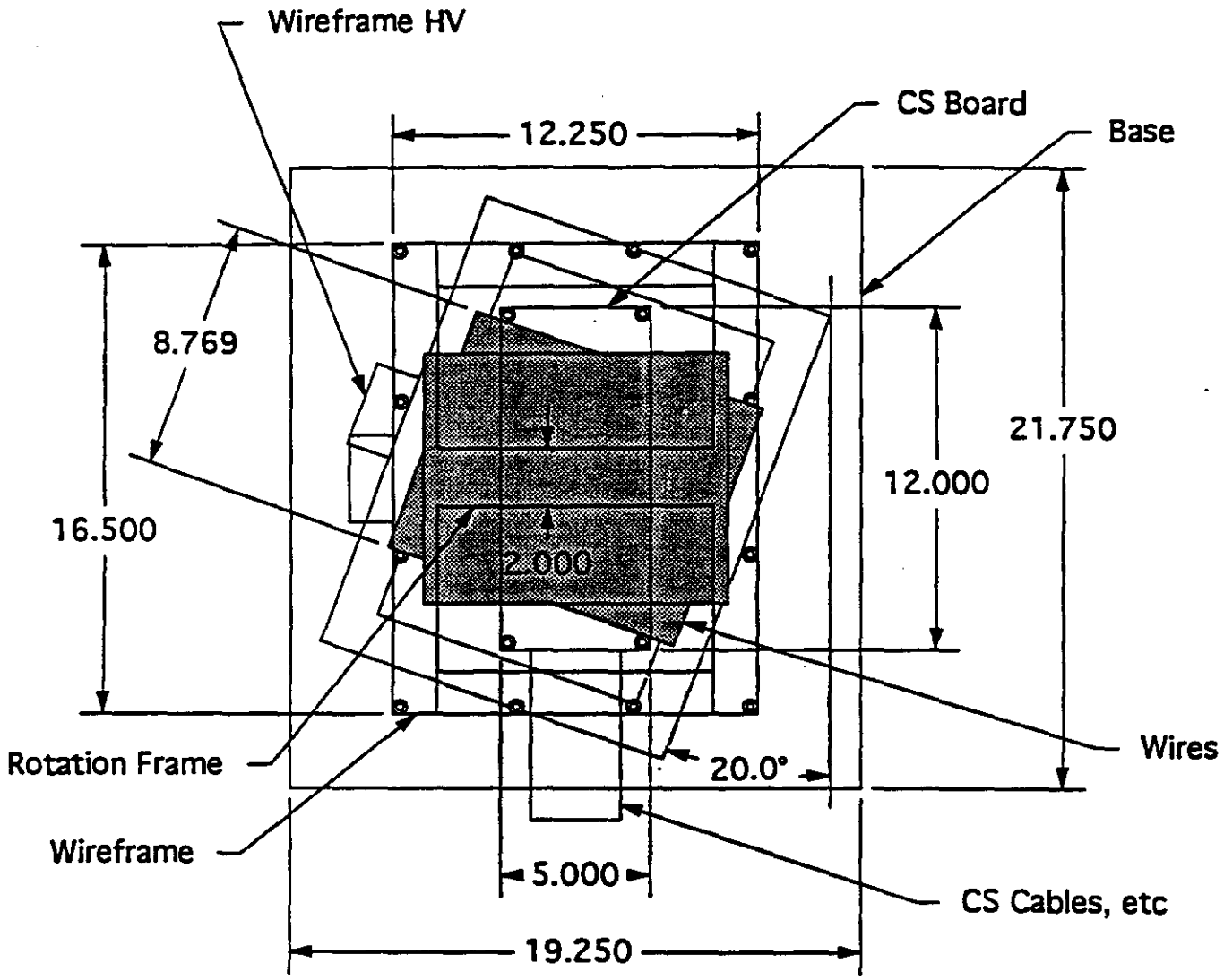






NOTES:	BOSTON UNIVERSITY PHYSICS DEPARTMENT
	Movable Wire Chamber

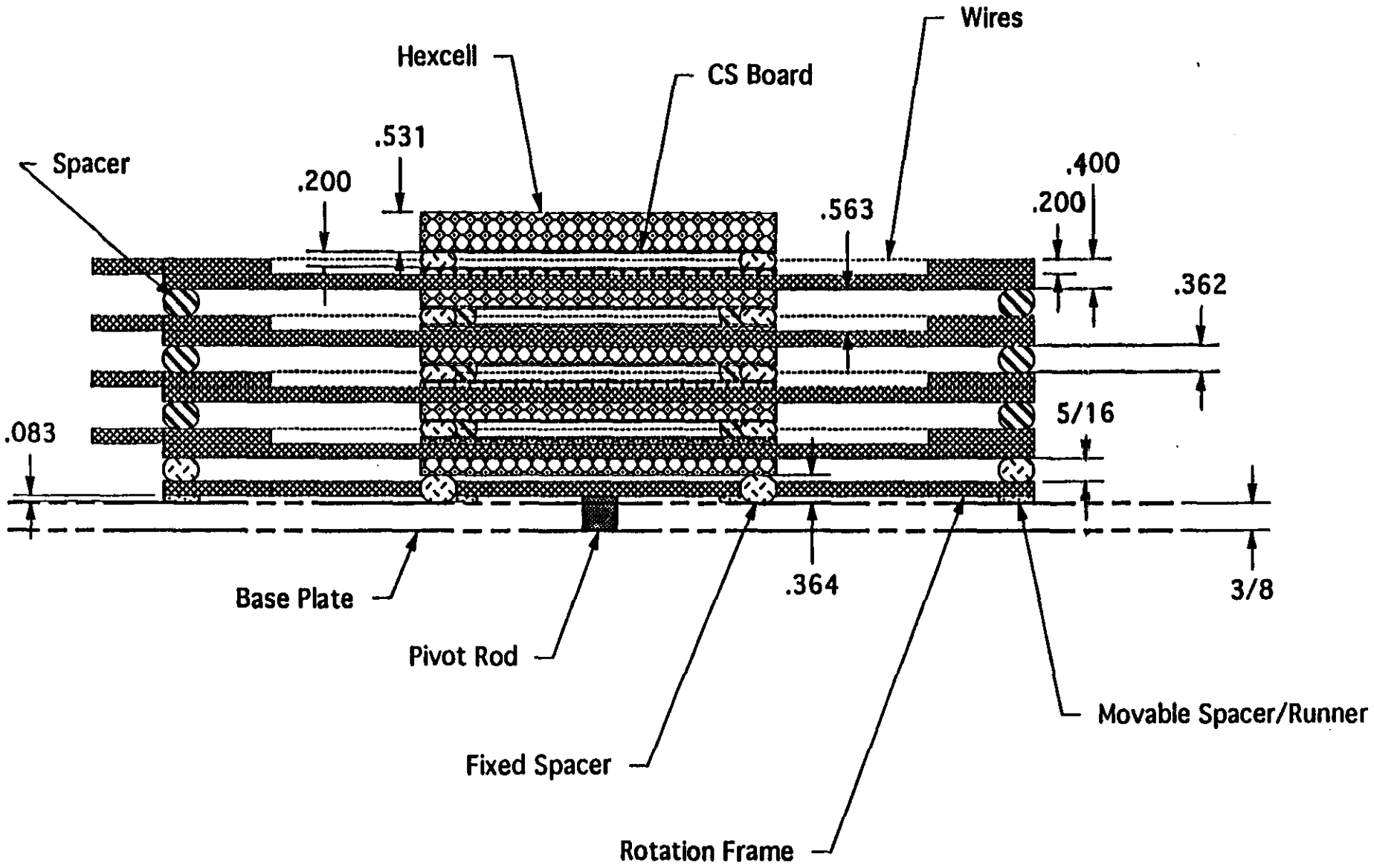
MWC: TOP view



Notes:
- 87 wires per wireframe
- 3/8" thick jig plate for base
- 30 μm wire
- 4 wireframes
- 5 hexcell sandwiches
- 1/2" thick plexiglass enclosure
- pivot point at geometric center

All units in inches

MWC: Positioning of Wireframes and Hexcell Sandwiches
FRONT view



Timing Discriminator - Prototype

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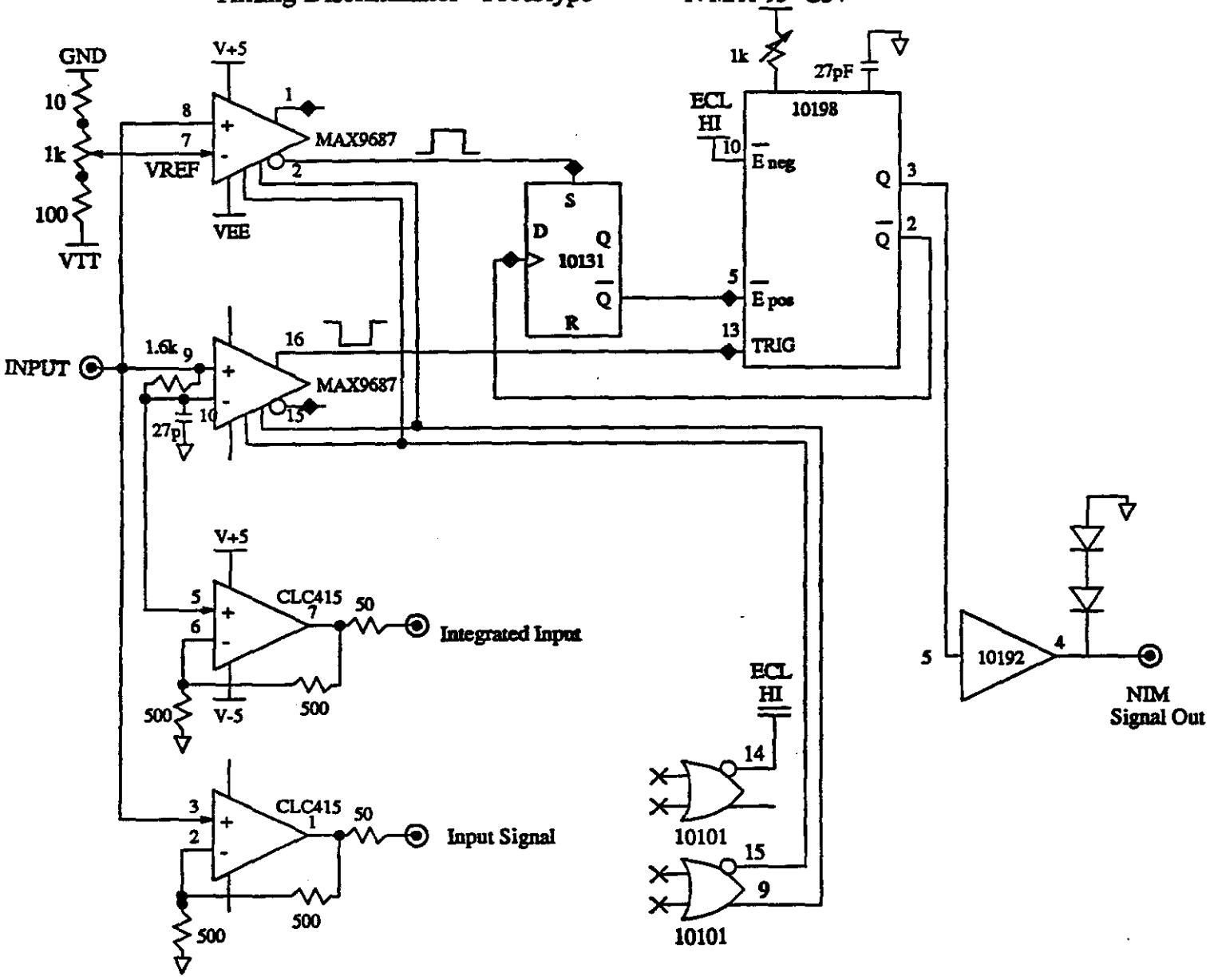
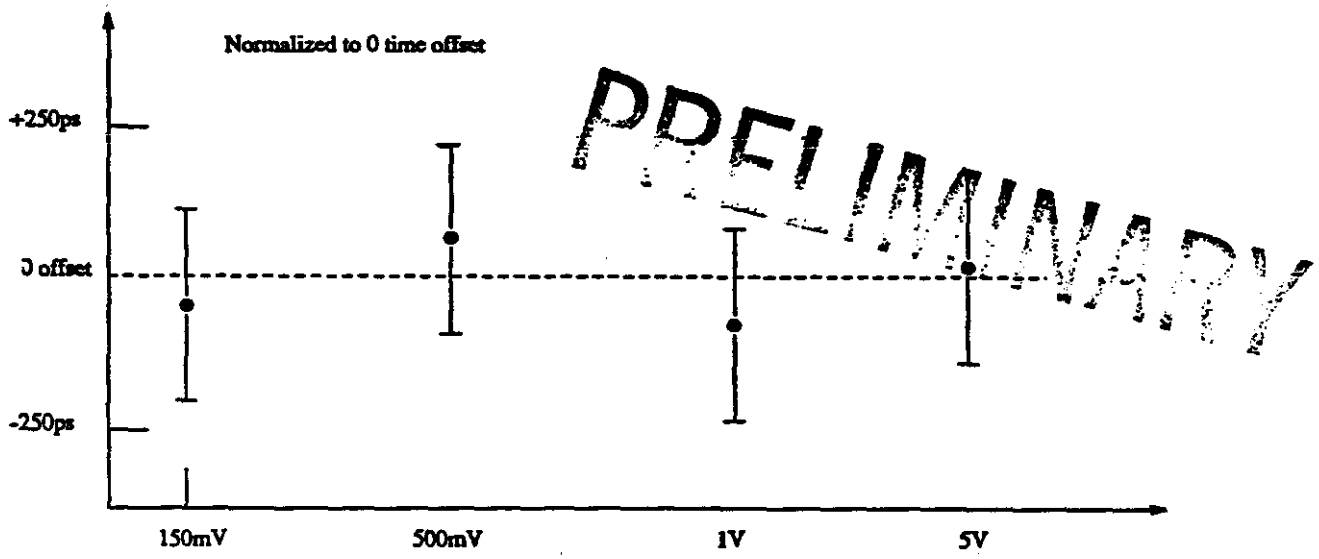




CONCLUSIONS

Current Anode Electronics

Future Anode Electronics

- **A LOT more to be studied, A sampling:**
- Cost Efficient Multi-hit Resolution
- Optimal Timing Scheme
- Signal Fan-in Density issues

Ongoing Studies - next 6 months

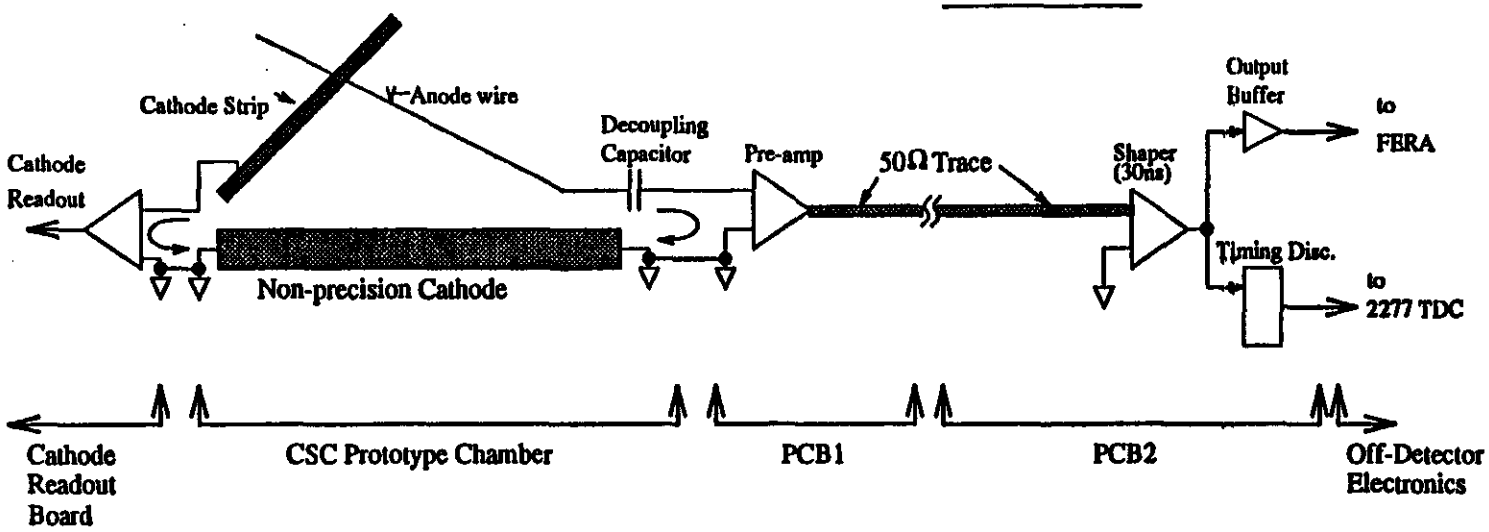
- Cheap and efficient HV control and monitoring
- Chamber deformation studies
- Moveable wire chamber studies
- Timing Studies
- Trigger Studies
- Pulse correlation studies

Future Studies

- ???

Electrical Signal Pathway

7 MAY 93 - GSV



LSP
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GEM MUON ELECTRONICS
READ OUT PRINTED CIRCUIT BOARD
(CSC MODULE MOTHERBOARD)

HOUSTON RESPONSIBILITY:

ROPCB

CATHODE FEPCB CONTROL ASIC ?

(IF NOT, WE NEED TO WORK CLOSELY WITH WHOEVER DOES!)

SO...

THIS DISCUSSION CENTERS ON THE

ROPCB FOR NOW...

ROPCB TASKS:

1. TRIGGER PASS-THROUGH
2. DATA INTERFACE (2-WAY)
3. POWER DISTRIBUTION ?

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ROPCB - DATA ACQ. RESPONSIBILITIES

I. UPLOAD REQUIREMENTS

JE SUGGEST THIS CONVENTION

→ DATA SENT TO FEPCB's

A.) KNOWN INFORMATION NEEDED

1. LEVEL 1 ACCEPT
   → HOW IS THE TIME STAMP PRESERVED ? (COINCIDENCE ?) (EVENT TAG ?)
   ABS. DELAY? →
   HOW IS A PARTICULAR LEVEL 1 ABSOLUTELY CORRELATED WITH A PARTICULAR LCT ?

2. 10 MHz BUS CLOCK (SCA CLOCK TOO?)

3. TEST PULSE ?
4. RESETS (COUNTERS)

B.) WHAT ELSE ?

1. INFO ON DATA LINES
   ← WOULD THIS EVER OCCUR DURING AN ACTIVE (ENABLED L1) PERIOD ?
2. CONTROL SWITCHING

FAULT TOLERANT DESIGNS → HV? POWER ? BACKUP ? SELECTIVE DISABLE

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ROPCB - DAQ

II. DOWN LOADING TO DAQ

A. BANDWIDTH — 100 MBIT/SEC
↑ LIMITED BY
1. F.O. LINK
2. DAQ OVERLOAD @ L2

"NOMINAL" EVENTS (1 TRK WITH VALID LCT PER CSC MODULE/L1)
... ARE NOT A PROBLEM.

BUT.

96 CHANNELS/FEPCB IS AN "INEFFICIENT" #

10 BIT ADC (MAYBE 11 ?)

7 BIT ADDRESS

(17)

IF WE PACK THE ADC DATA WITHOUT ADDRESS INFORMATION - THE ZERO SUPRESSION (SPARSIFICATION) ALGORYTHM MUST BE REPRODUCIBLE!

↑ KNOWN IN ADVANCE FROM LCT MASK!

DESIGNED IN ? ——→

7/18/93

ROPCB - DAQ

A. BANDWIDTH (CONTINUED!)

7 CATHODE FEPCB (96 CH)
2 ANODE FEPCD (96 CH)
9 → 2 BIT OR 1 WORD SEPERATORS
↓
9 WORDS
↳ REQUIRES UNIQUE WORDS POSSIBLE!

ASSUME 17 + 2 = 19 PER ADC

WITH SCAs THERE ARE (36-48)X5 READ-OUTS

TYPICAL PER MODULE

17 x 48 x 5 = 4080 BITS

~ 255 16-BIT WORDS

→ 25.5 μ SEC @ 10 MHz

+ (ANODE DATA ?)

2-3 HITS IN A MODULE MAX
↳ IS THAT OK?

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ROPCB - DAQ

1

B. ANODE REQUIREMENTS

TIME STAMP AVAILABLE LOCALLY ?

↳ ?

ARE THESE ALL ADC OUTPUTS ONLY ?

HOW MUCH PER LCT ?

WHERE IS THE BUNCH CROSSING I.D. MADE?

ROPCB - TRIGGER RESPONSIBILITIES

WHAT FLEXIBLITY IS REQUIRED IN THE LCT ENCODING?

WHAT TIME BUDGET EXISTS FOR THIS?

HOW IS THE TIME STAMP — BEAM CROSSING I.D. DONE.

DO ANY "ANALOG" SIGNALS NEED TO BE PASSED ON?

↑ TIMING PULSES ?

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ROPCB — POWER

- DO WE WANT SOME CONTROL?
  SELECTIVE ON/OFF

- DO WE WANT MONITORING CAPABILITIES?
  VOLTAGES
  CURRENTS
  TEMPERATURES

ROPCB — GENERAL PHILOSOPHIES

- SHOULD WE CONSIDER A MICROPROCESSOR(S)?
  - ↳ FAULT TOLERANCE
    - ↳ REPROGRAMABILITY

- REMOTE REPROGRAMMING OF FPGA'S?

- <u>GROUNDS</u>
  ANODE — HV
  CATHODE
  LV
  EXPT ? (FRAME)

LSP
7/18/93

ZERO SUPRESSION - SPARSIFICATION

HARD WIRED - BASED ON LCT ?
↑ PATTERN

UPLOADABLE ?

DATA DRIVEN - LCT + ADC

NEEDS A LOT OF CAREFUL WORK

VARIABLE TIME BINS
↑ LOCATION DEPENDENT
ADC DEPENDENT
↓
SUPRESS ALL PEDESTALS ?

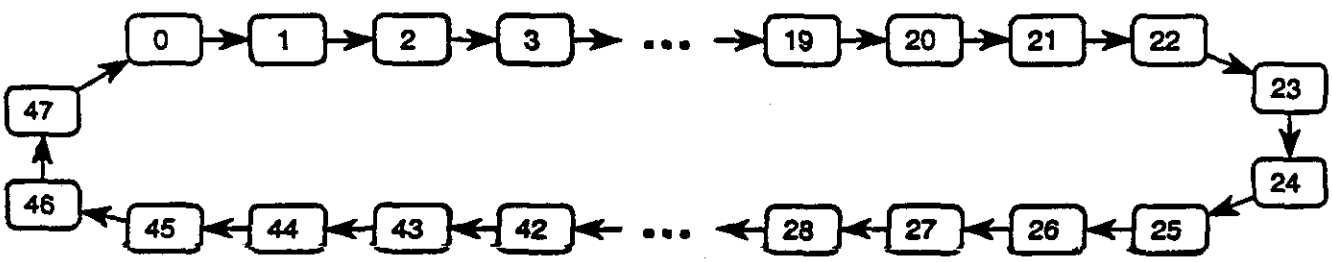
List Processor 2

48 addresses in the SCA:
one list element per address

Each address can be one of the following:

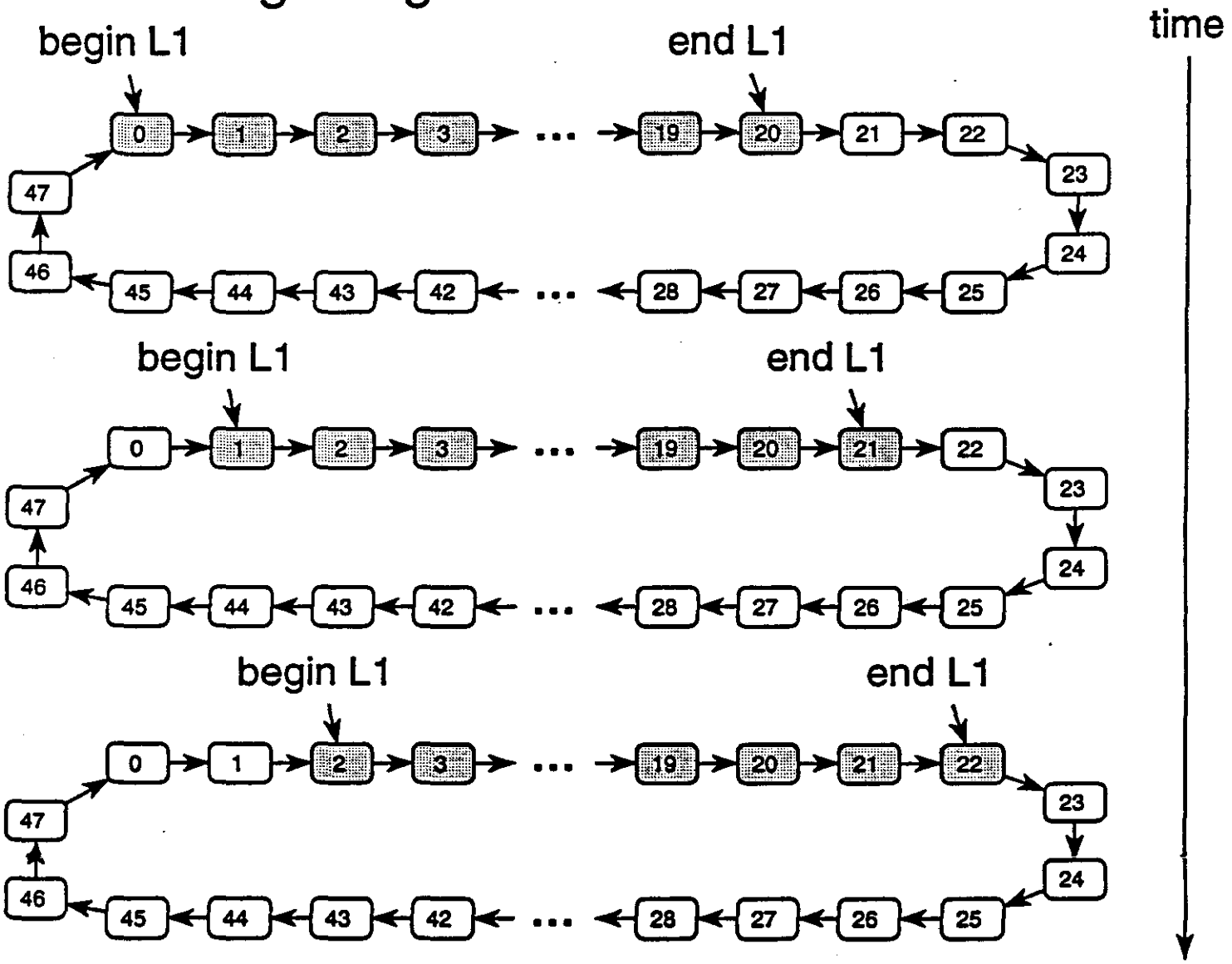
- free (no sample)
- pending L1 accept
- pending A/D conversion

Keep a circularly linked list of the addresses:



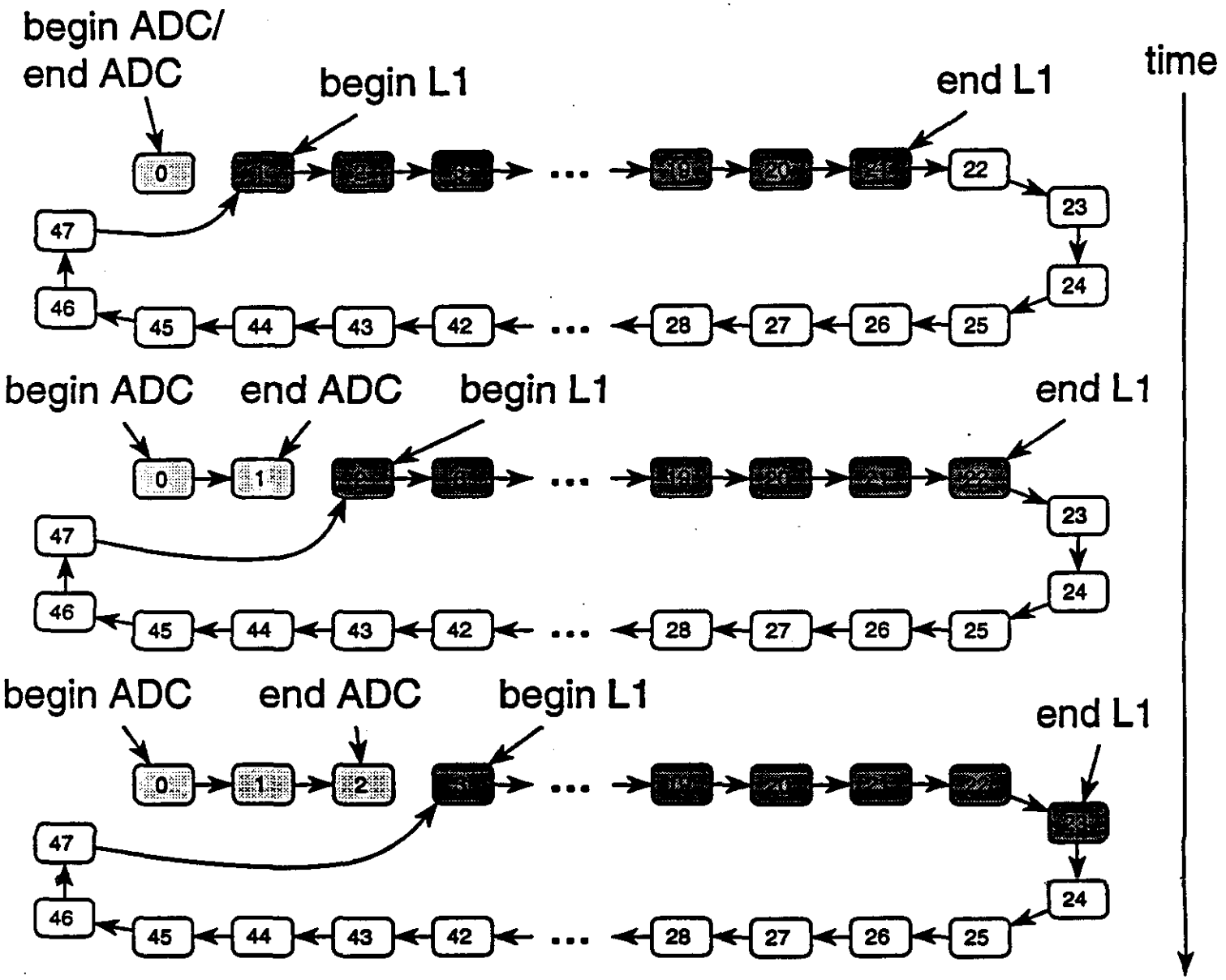
List Processor 3

Pending L1 accept (subset of free list): fixed length list, keep 2 pointers, for the beginning and the end of the list.



List Processor 4

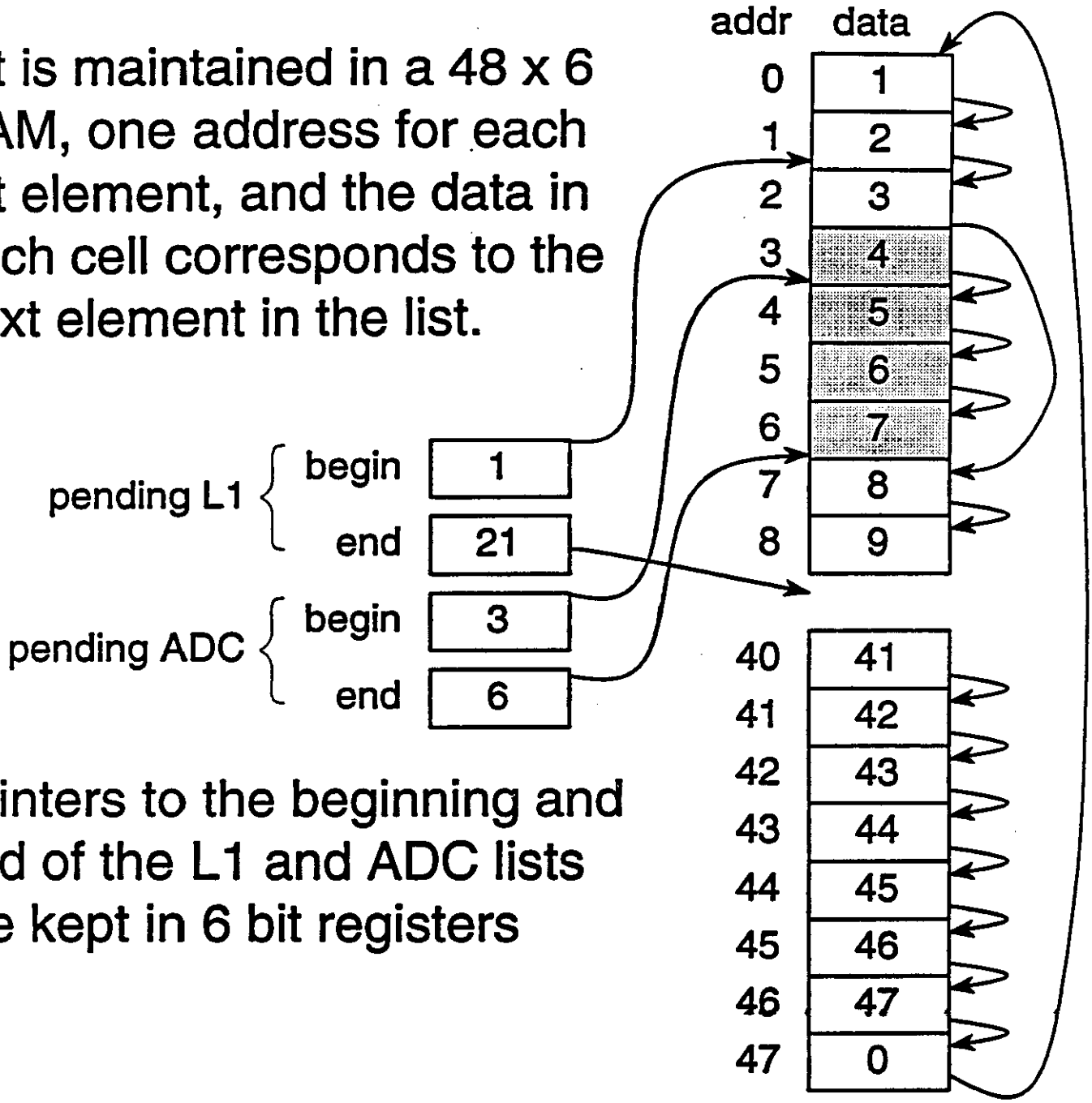
Pending ADC list:
move 5 elements to this list if L1 accept occurs



elements are moved back to free list once
A/D conversion has been completed.

List Processor 5

list is maintained in a 48 x 6 RAM, one address for each list element, and the data in each cell corresponds to the next element in the list.



pointers to the beginning and end of the L1 and ADC lists are kept in 6 bit registers

List Processor 6

- Inputs:
  - L1 accept signal
  - ADC complete signal
  - reset and initialization signals

- Outputs:
  - write address, write enable
  - read address, read enable, read reset
  - L1 accept ignored
  - start ADC signal

- Internal State
  - 4 pointers (beginning and end of L1 list and ADC list)
  - size of ADC list
  - # of samples remaining from L1 accept

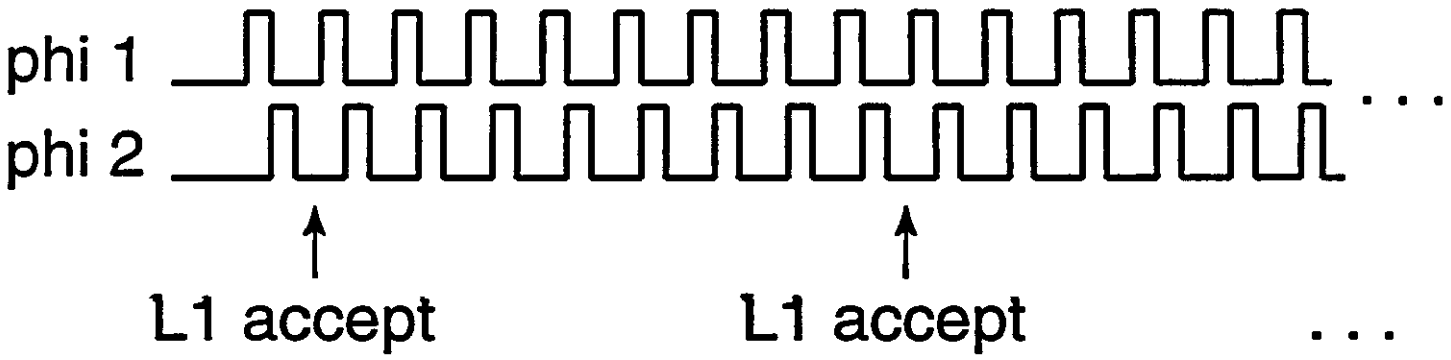
- Debugging
  - state maintained for each list element, can serially read out state and next address to check for errors

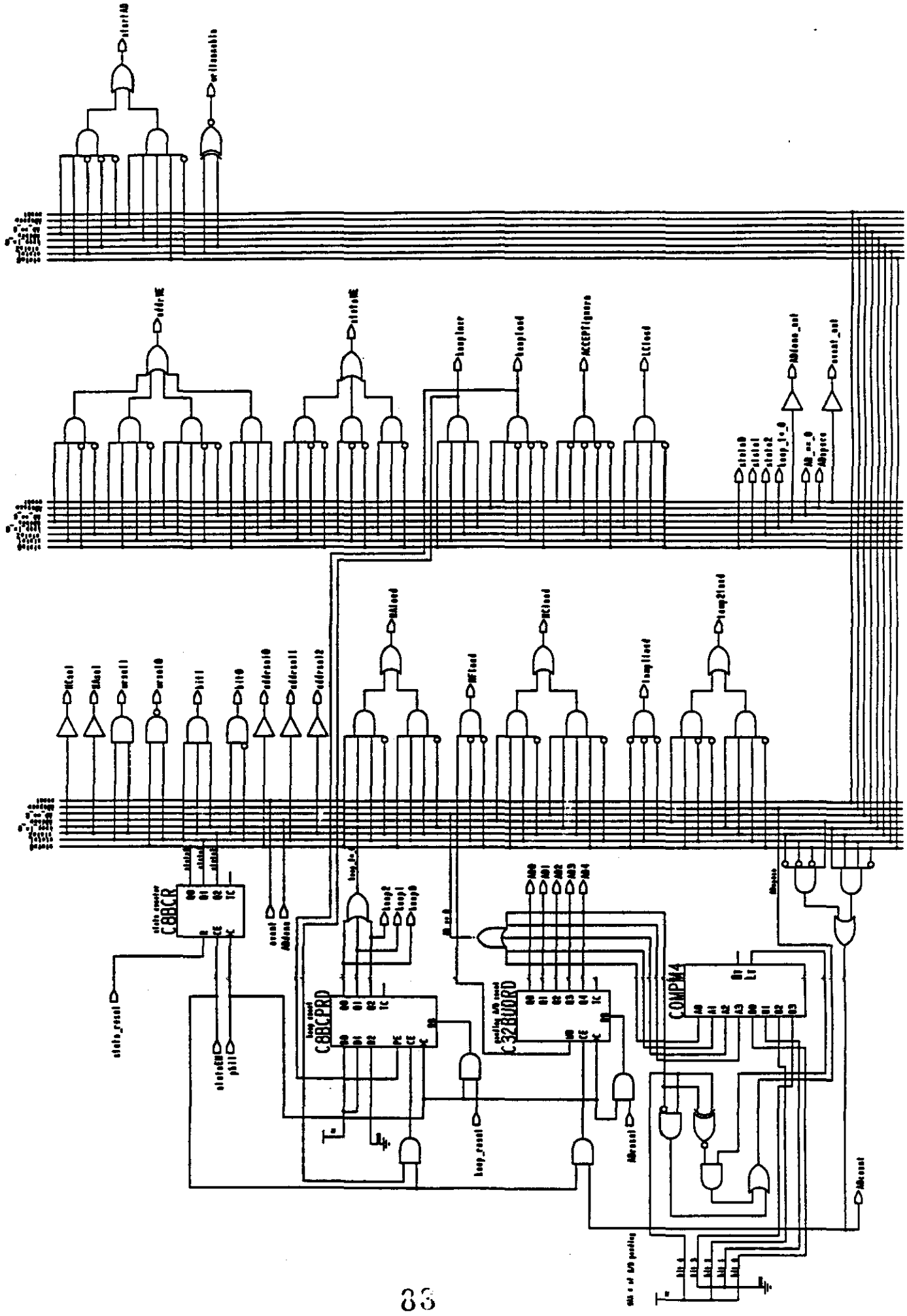
List Processor 7

- Control / Datapath based architecture

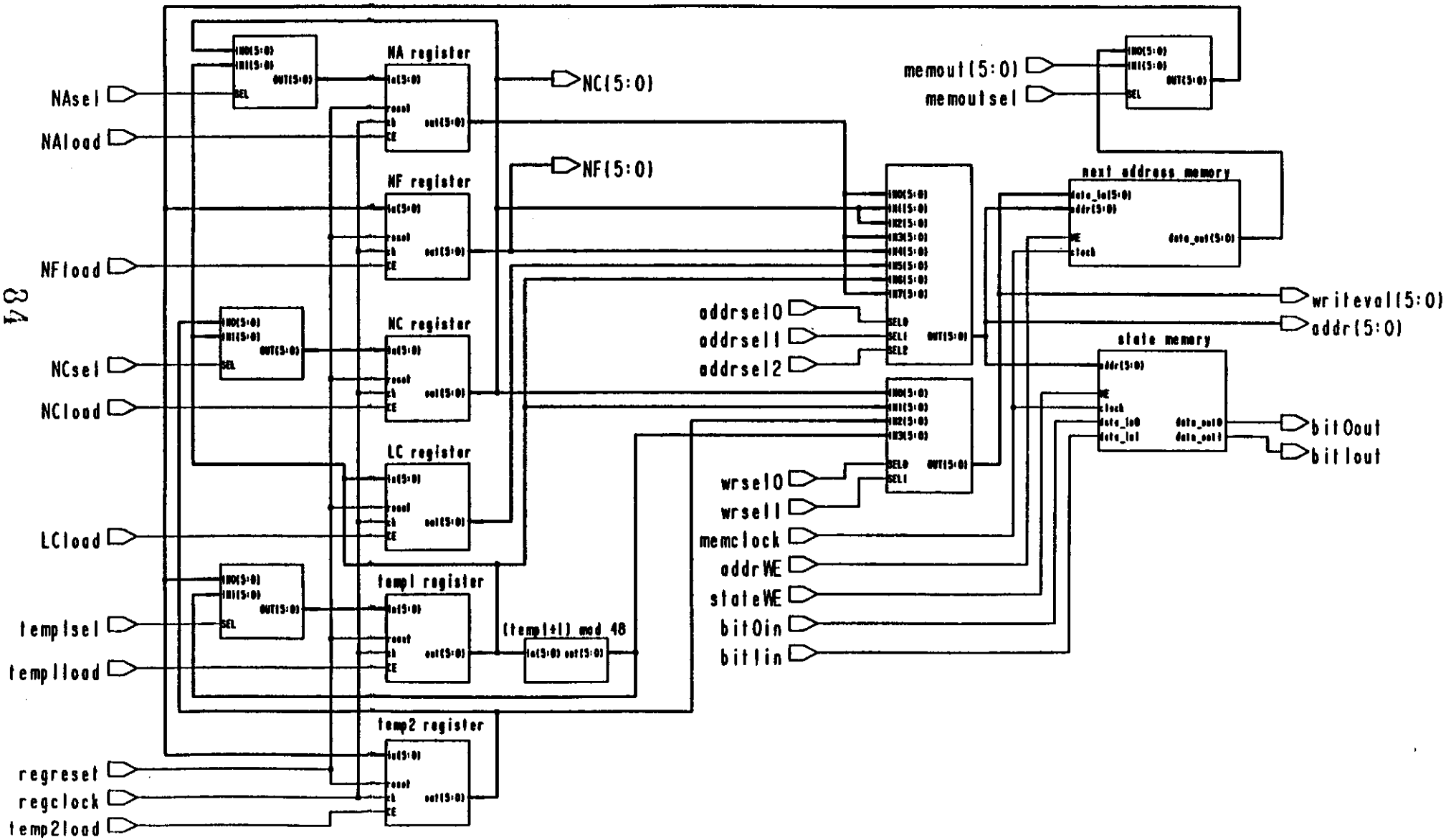
- 8 "micro-cycles" needed for each sample to maintain all internal pointers and update both lists- limitation imposed by need for 8 memory accesses (either read or write) per sample.

- 2-phase clock used:
  phi1 - load registers
  phi2 - write memory

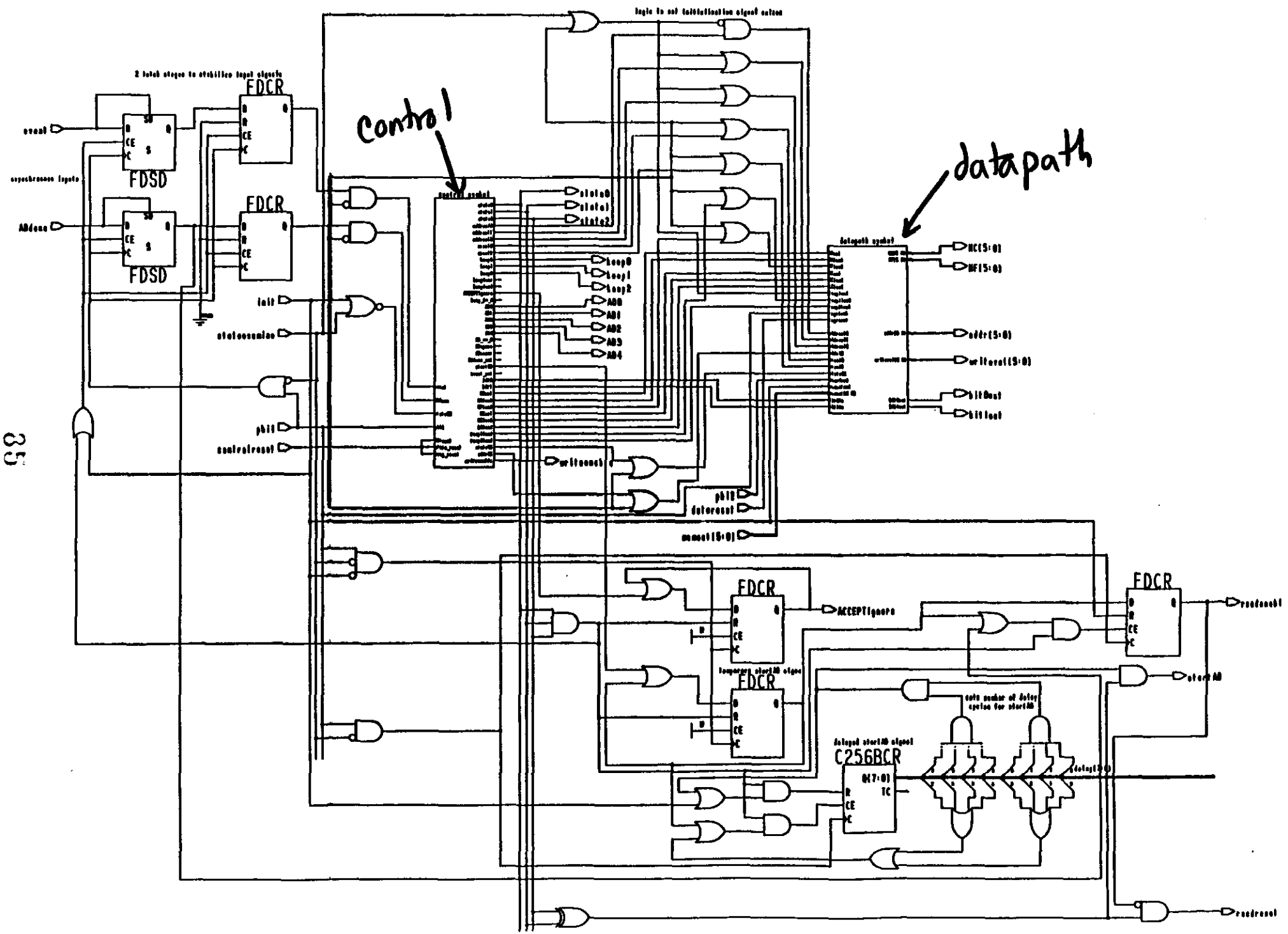



CONTROL
C8BCR
C8BCPRD
C32BUDRD
COMP4

DATAPATH


NA register
NF register
NC register
LC register
temp1 register
temp2 register
(temp1+1) mod 48
next address memory
state memory
NAsel
NAload
NFload
NCsel
NCload
LCload
temp1sel
temp1load
regreset
regclock
temp2load
NC(5:0)
NF(5:0)
memout(5:0)
memoutsel
addrsel0
addrsel1
addrsel2
wrsel0
wrsel1
memclock
addrWE
stateWE
bit0in
bit1in
writeval(5:0)
addr(5:0)
bit0out
bit1out

CONTROL + DATAPATH combined



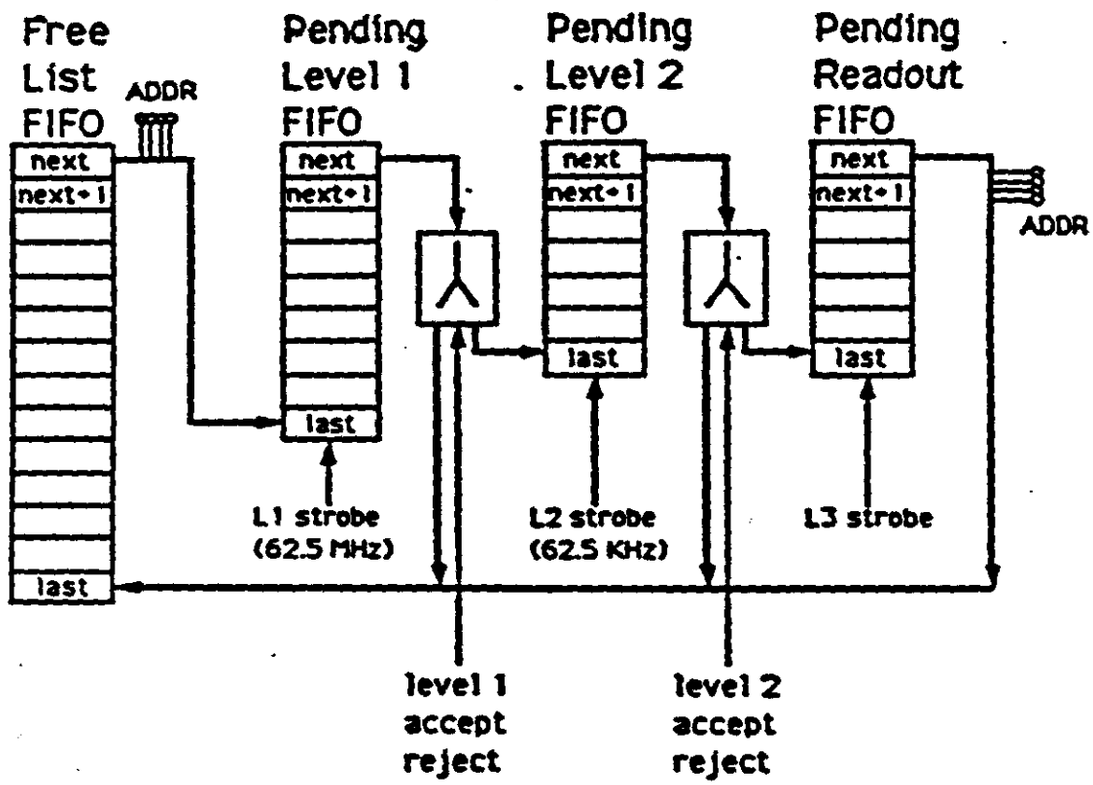
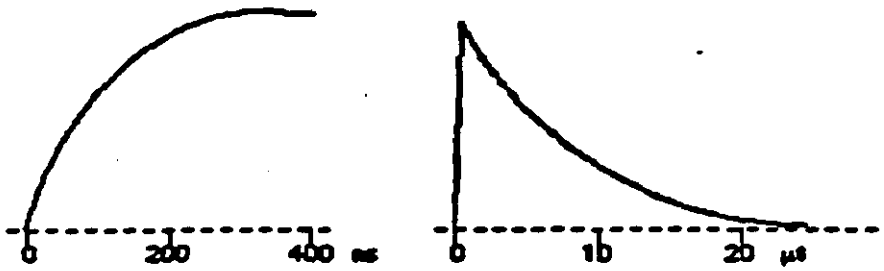


Figure 34: Block diagram of the address list processor, showing the four FIFO memories for the address pointer lists for: empty cells, pending Level 1, pending level 2, and pending read-out.

Pulse Shaping

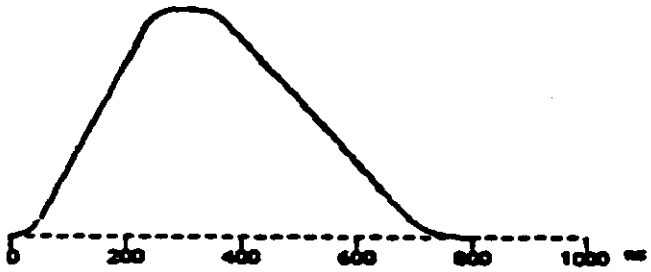
"No" Shaping:

$$h(t) \propto \left(1 - e^{-t/t_r}\right) e^{-t/t_d} \quad ;t_r = 60ns \quad ;t_d = 10\mu s$$



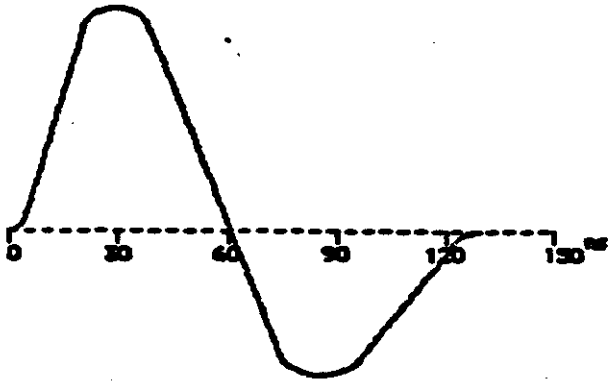
Slow Shaping:

$$h(t) \propto t^4 e^{-t/t_s} \quad ;t_s = 75ns \quad ;t_p = 4t_s = 300ns$$



Fast Shaping:

$$h(t) \propto \left(4 - \frac{t}{t_s}\right)\left(\frac{t}{t_s}\right)^3 e^{-t/t_s} \quad ;t_s = 15ns \quad ;t_p = 2t_s = 30ns$$



Noise Simulation

$$\text{"Parallel Noise"} \propto \int_{-\infty}^{\infty} |h(t)|^2 dt$$

With a noise power spectrum given by:

$$|H(\omega)|^2 = \left| \int_{-\infty}^{\infty} h(t) e^{i\omega t} dt \right|^2$$

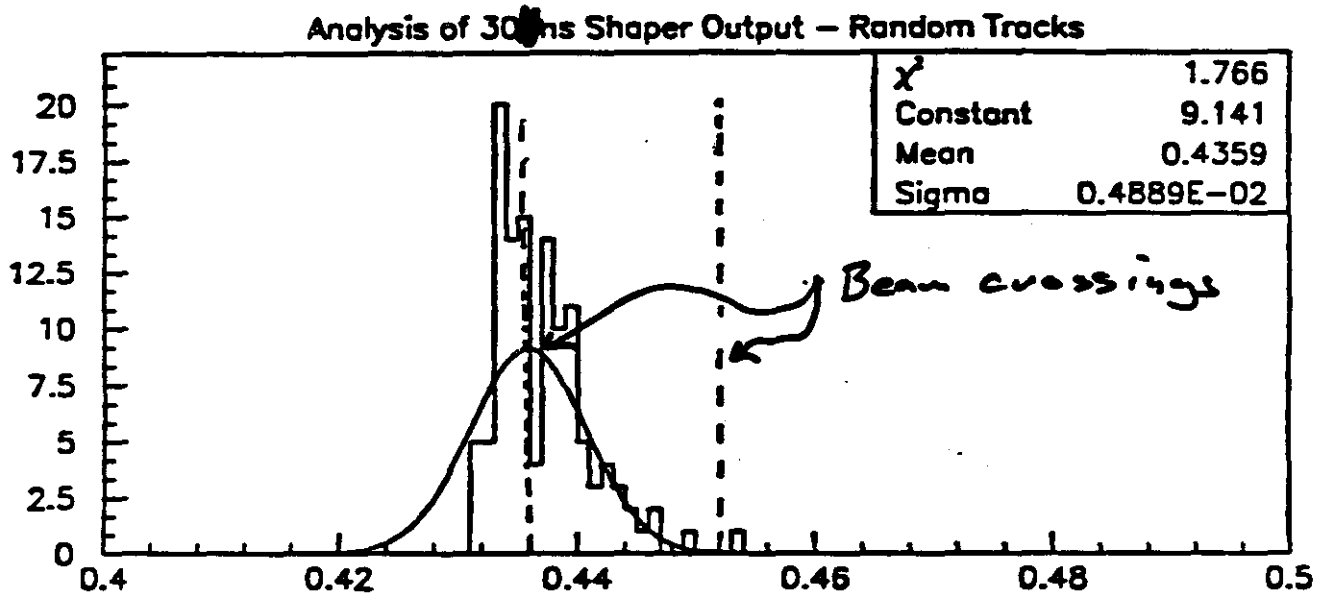
$$\text{"Series Noise"} \propto \int_{-\infty}^{\infty} |h'(t)|^2 dt$$

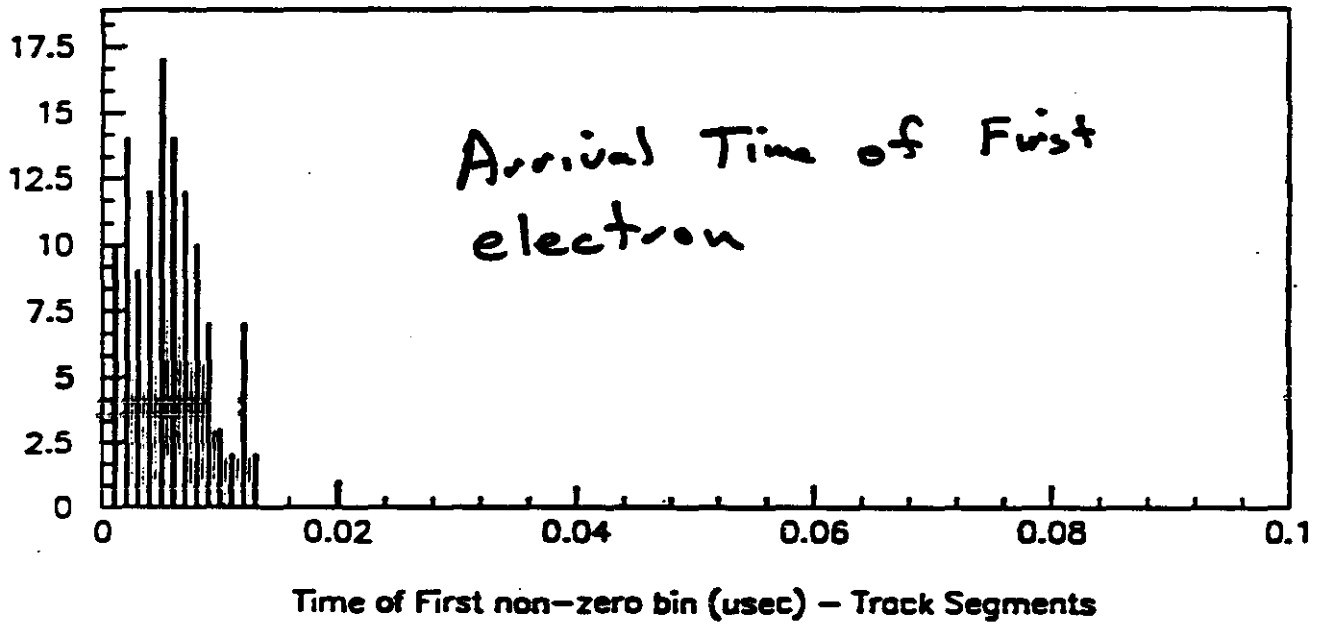
With a noise power spectrum given by:

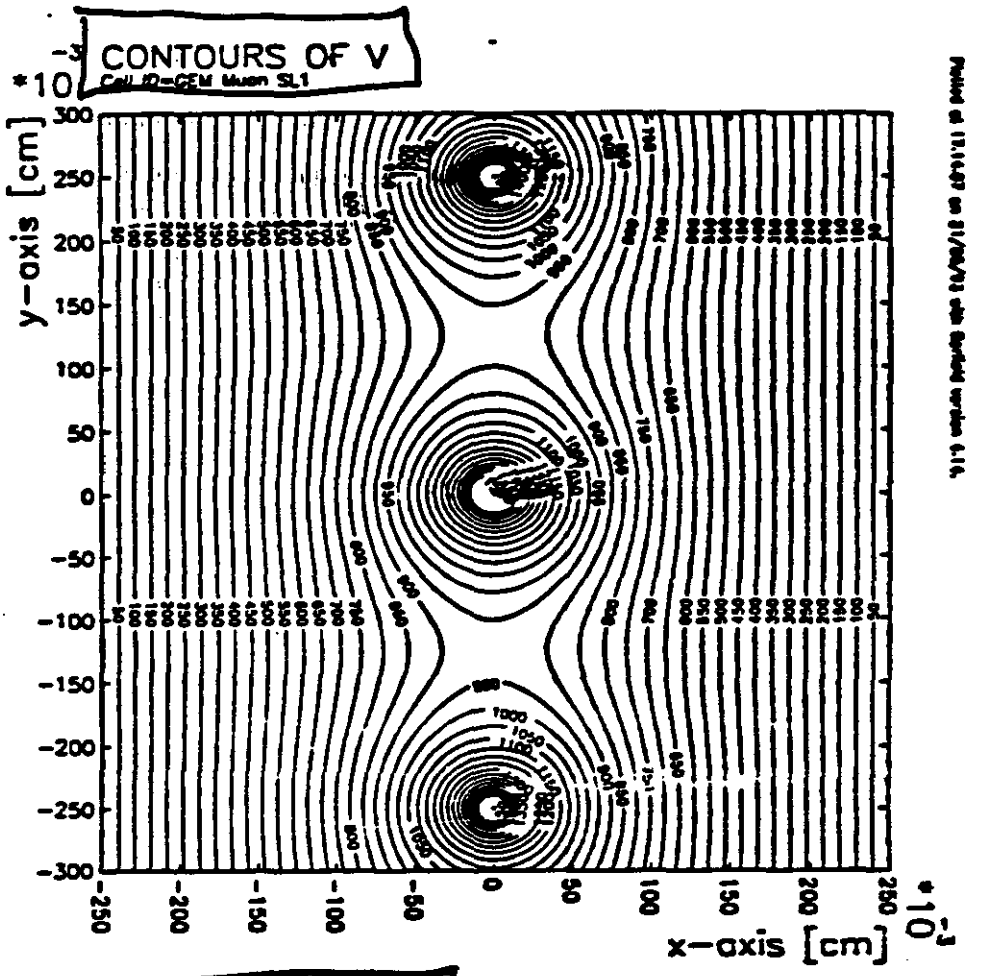
$$|H'(\omega)|^2 = \left| \int_{-\infty}^{\infty} h'(t) e^{i\omega t} dt \right|^2$$

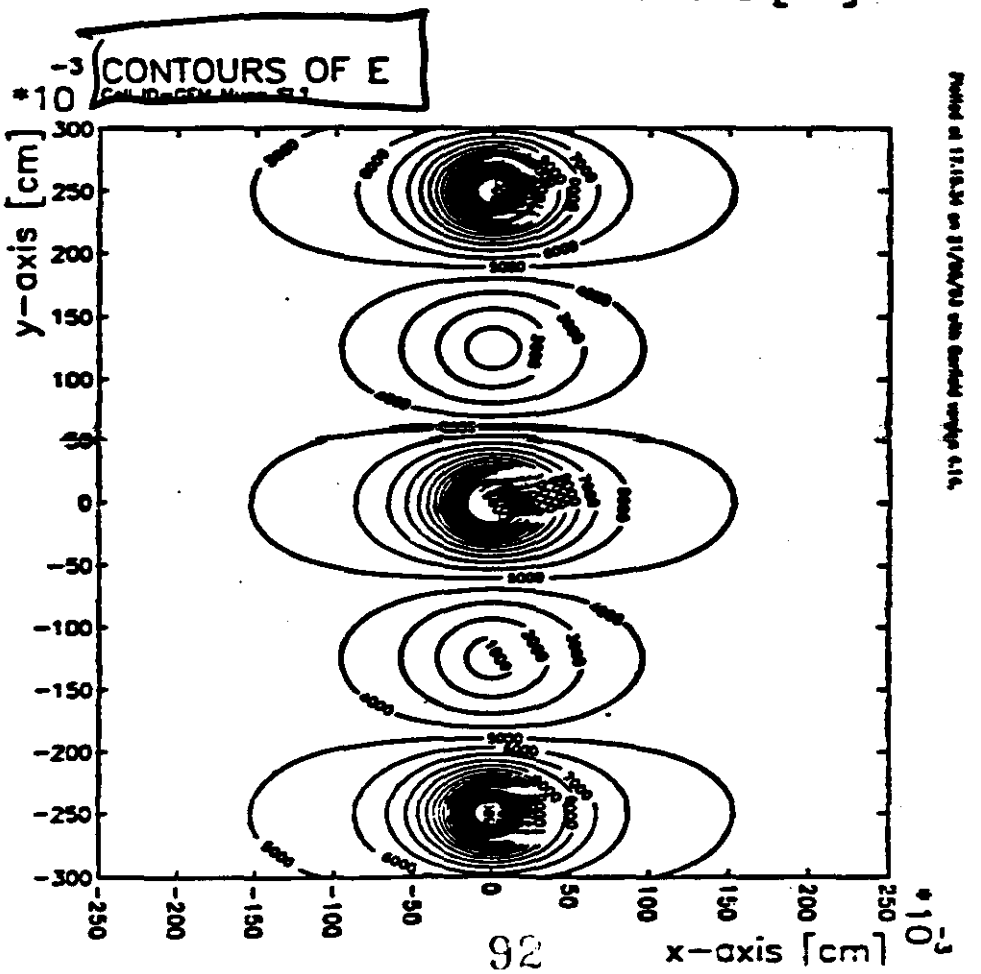
→noise spectra may be simulated by generating a large number of sine waves with random phases according according to the appropriate power spectrum.

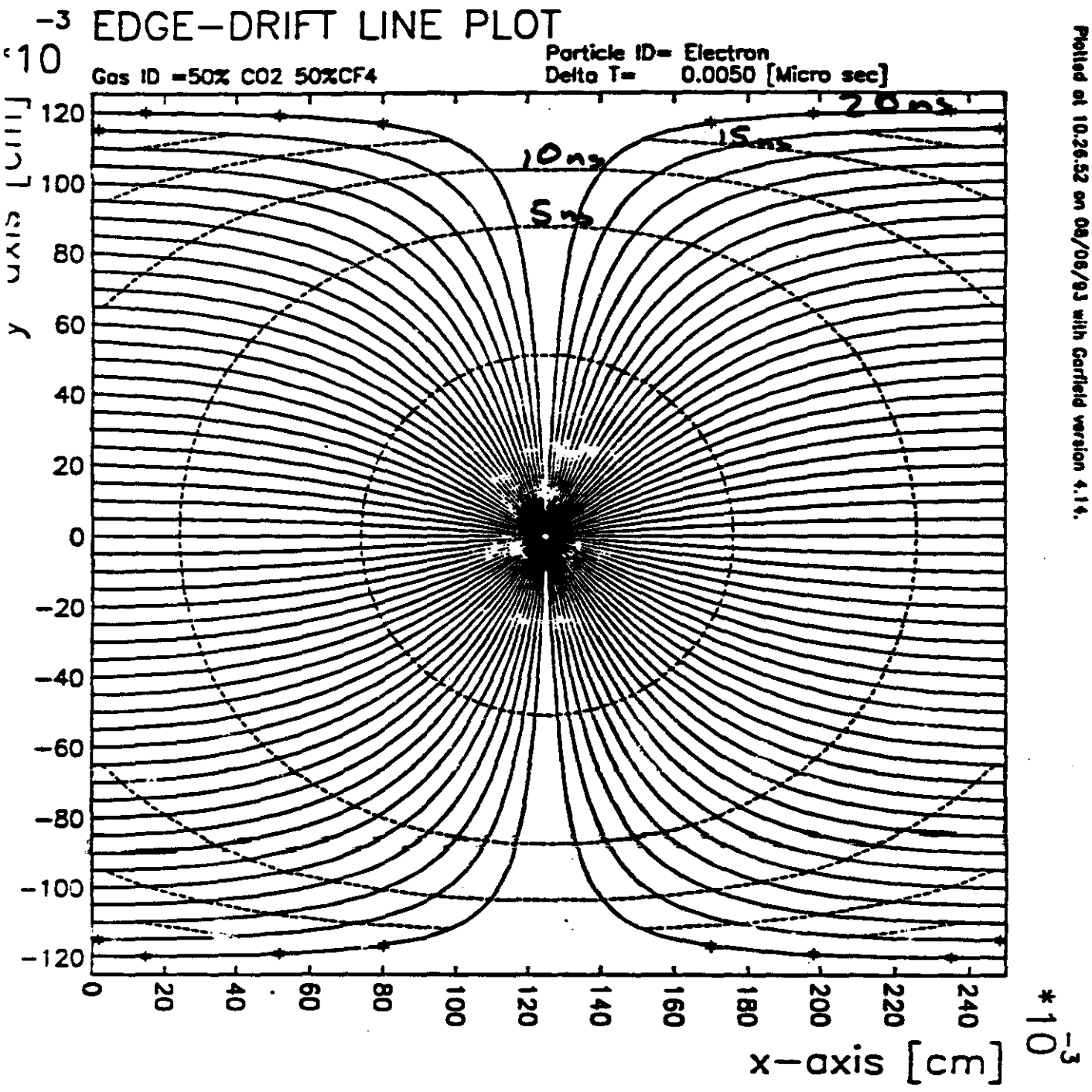
30[redacted] ns Shaping
T&S Time discriminator
Random tracks






CONTOURS OF V
Cell ID=CEM Muon SL1
y-axis [cm]
x-axis [cm]
*10^-3

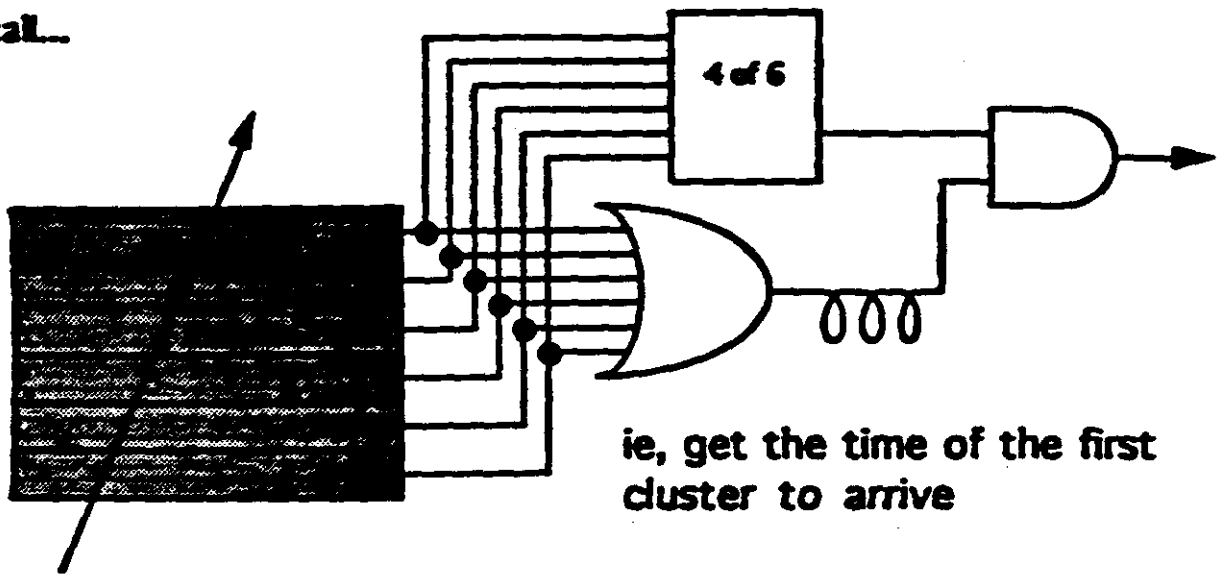

CONTOURS OF E
y-axis [cm]
x-axis [cm]
*10^-3



Plotted at 10.26.52 on 08/06/93 with Garfield version 4.14.

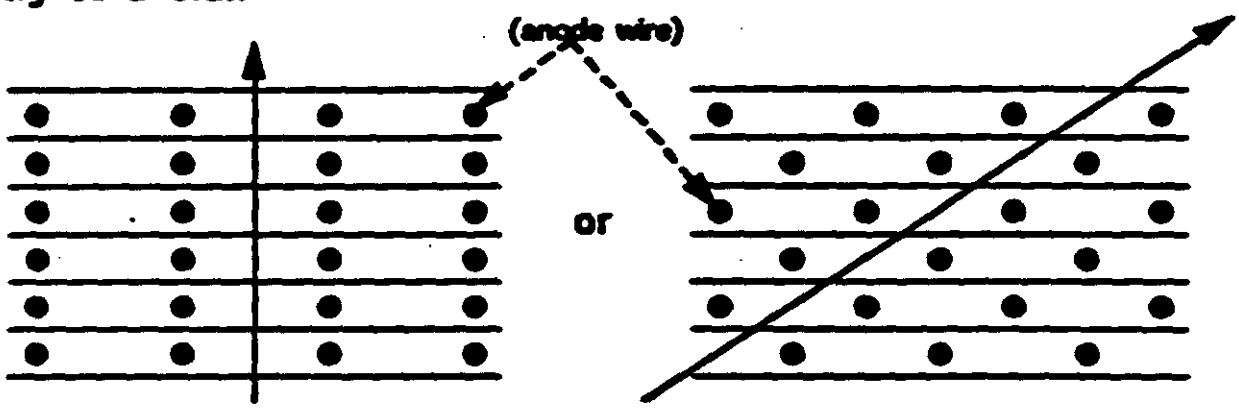
CSC Timing

Recall...

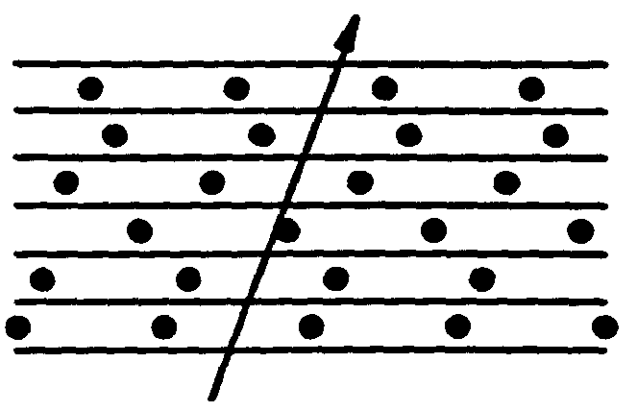


ie, get the time of the first cluster to arrive

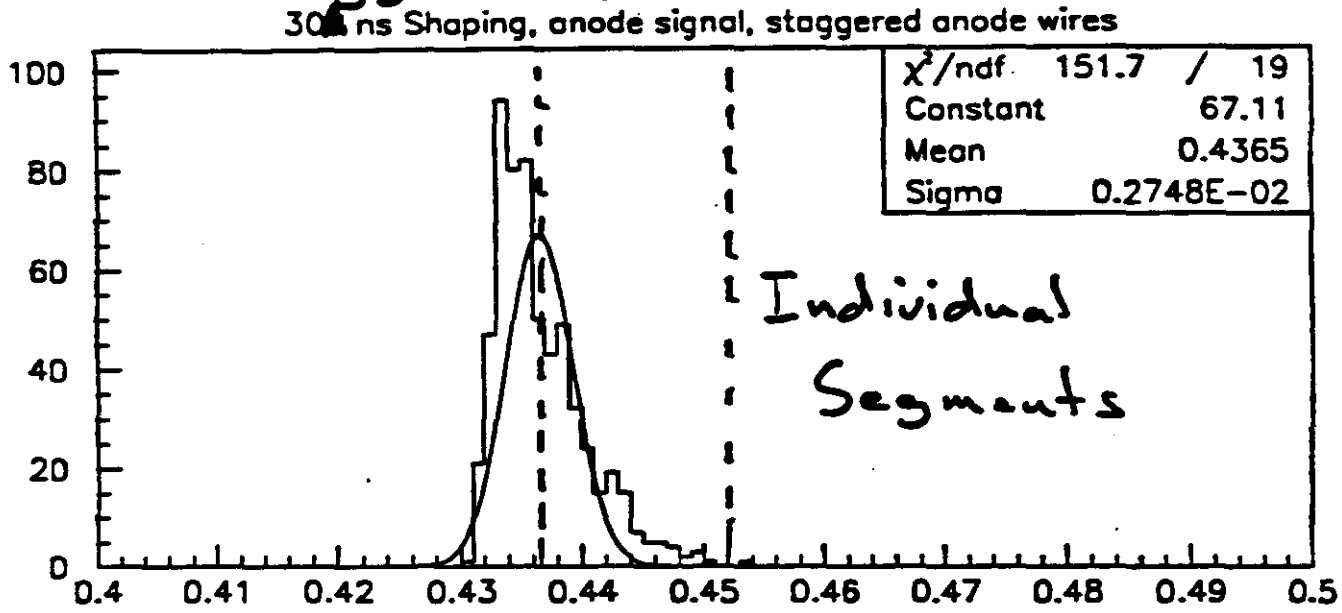
so try to avoid..

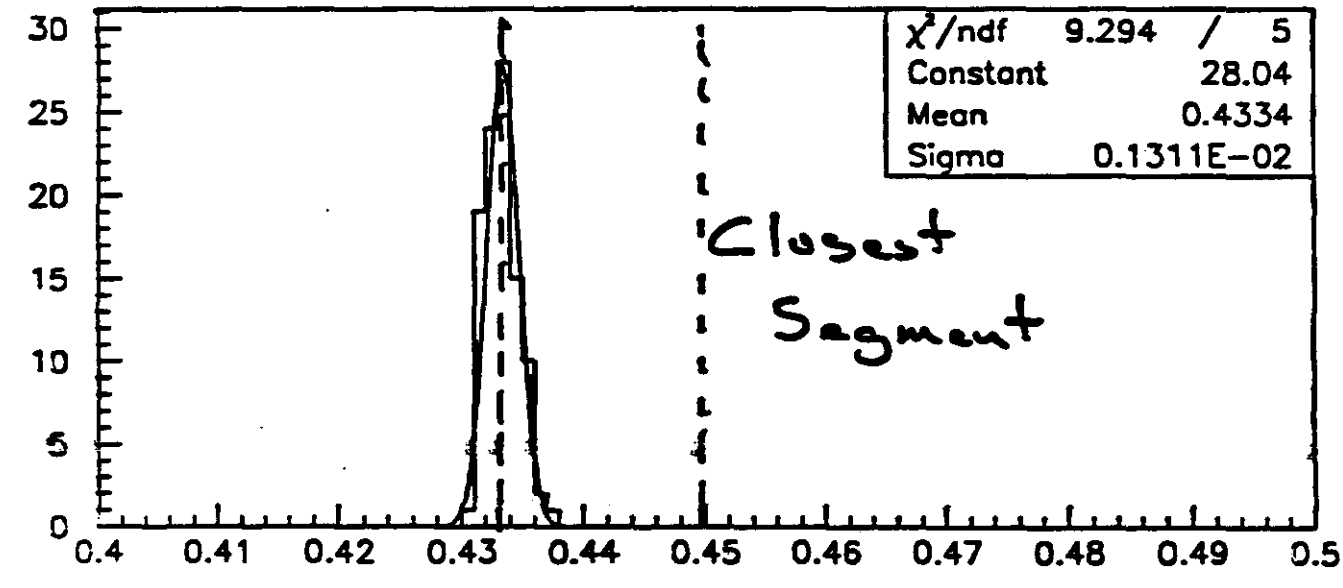


can try maximum staggering

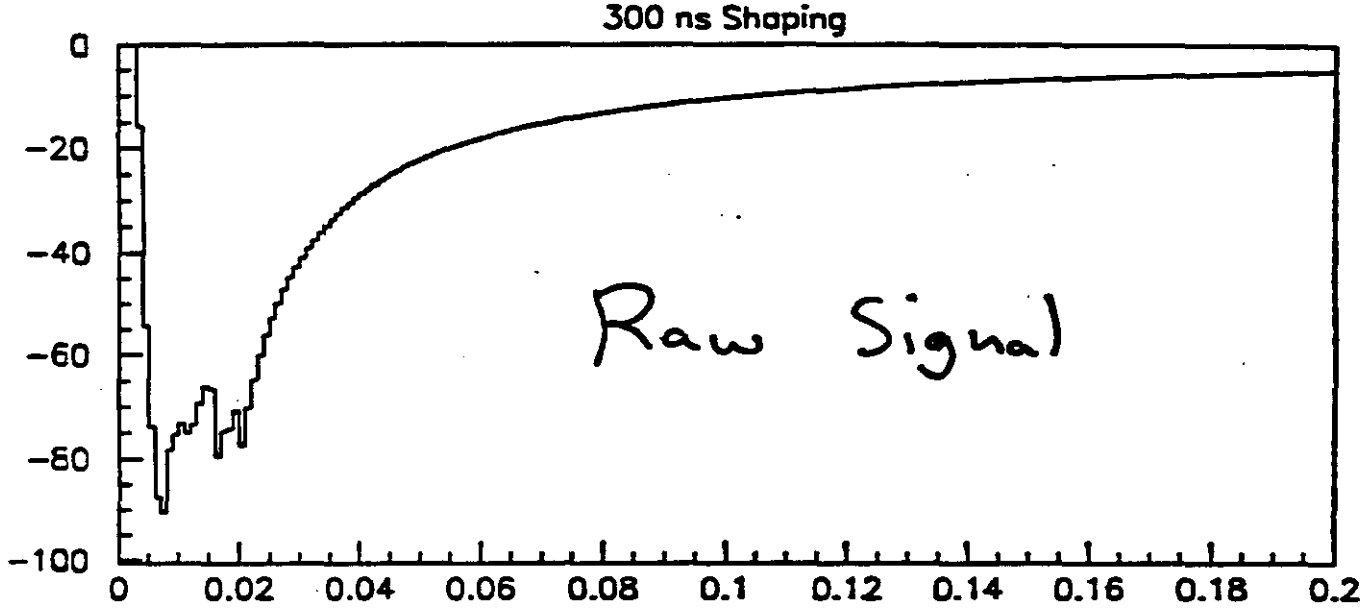


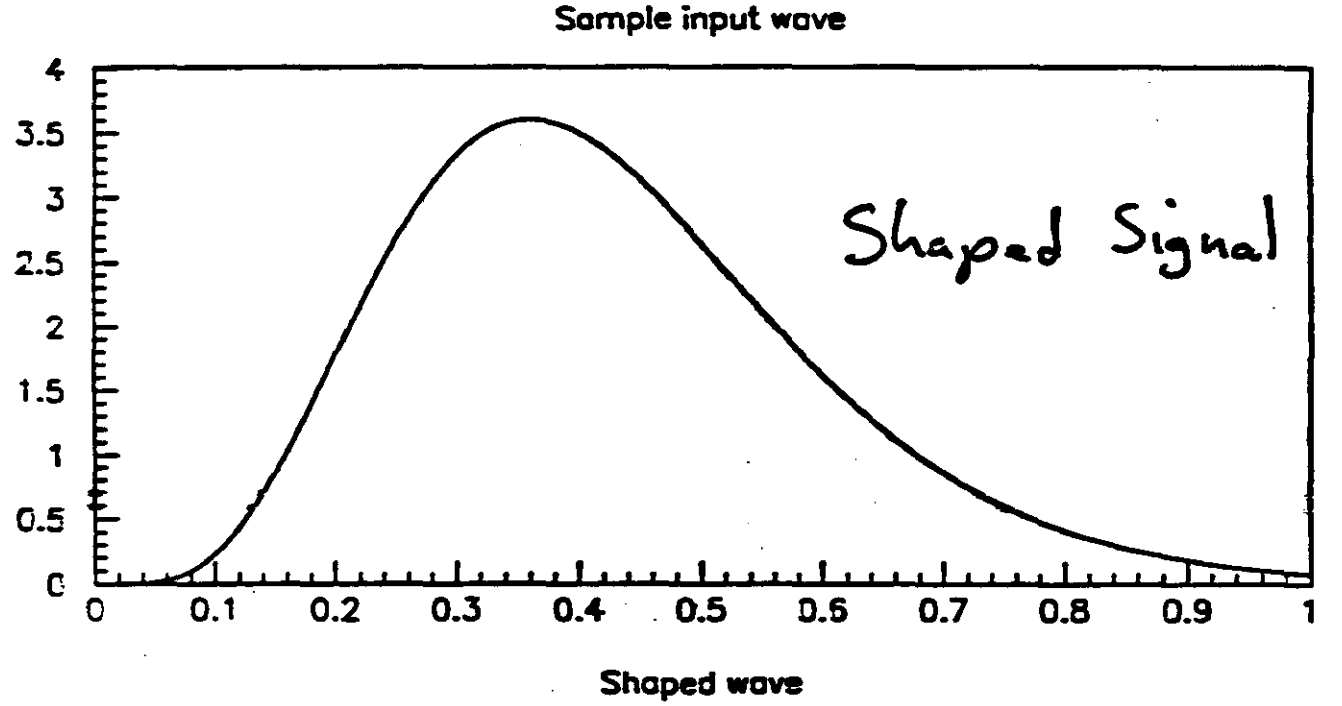
30 ns Shaping
Random [redacted] Tracks
Staggered Anode wires





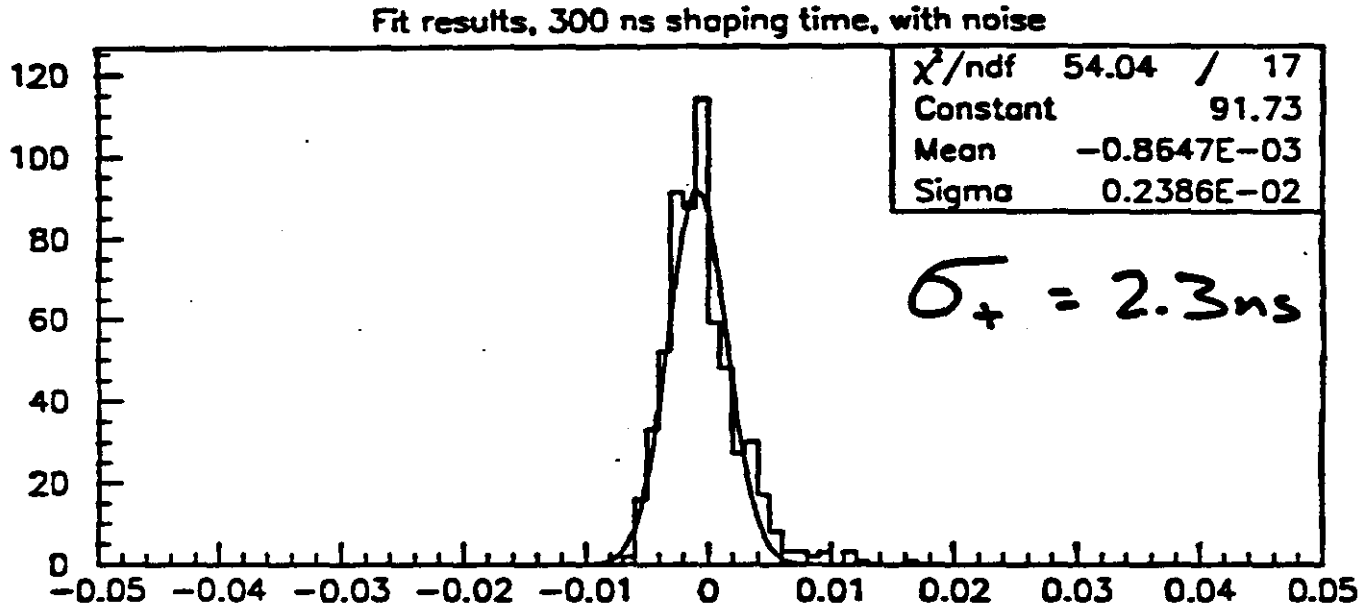
300 ns Shaping



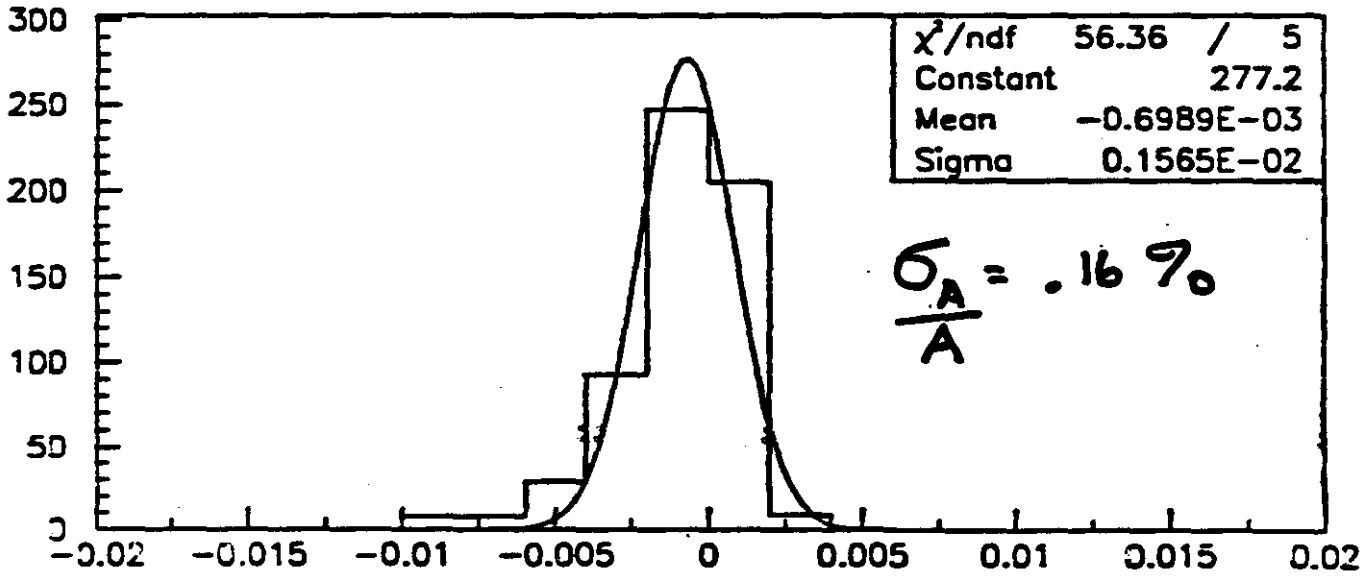


Note different time scale!

300 ns Shaper
4 200ns samples

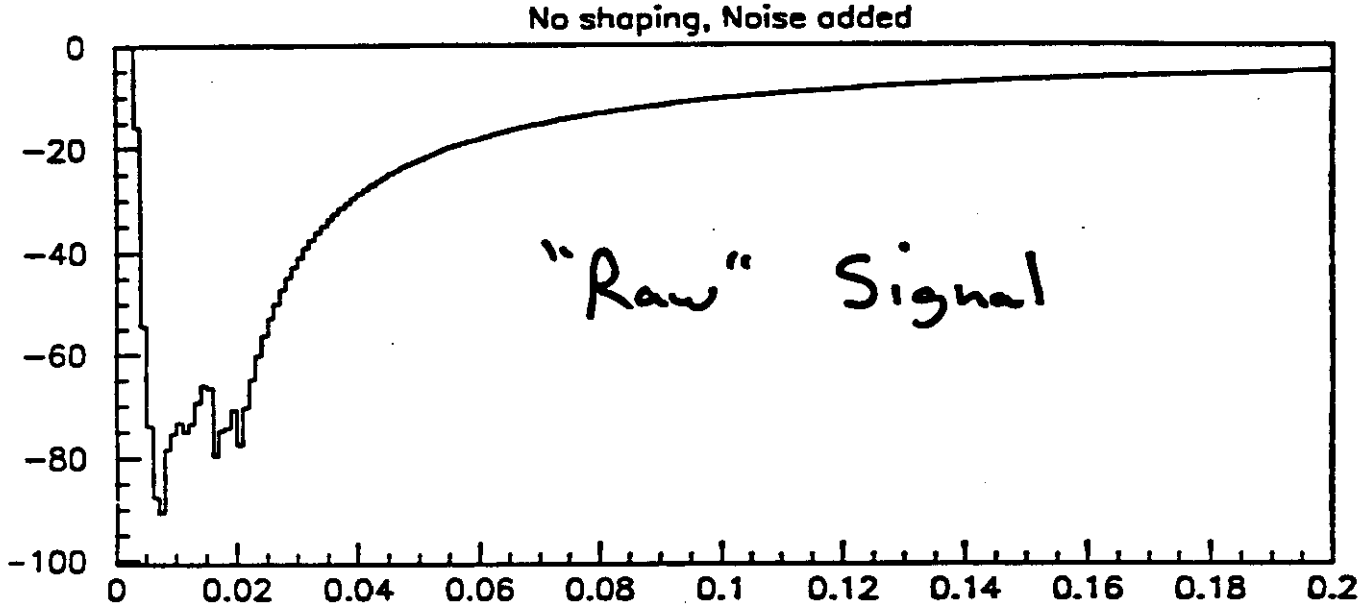


Corrected time

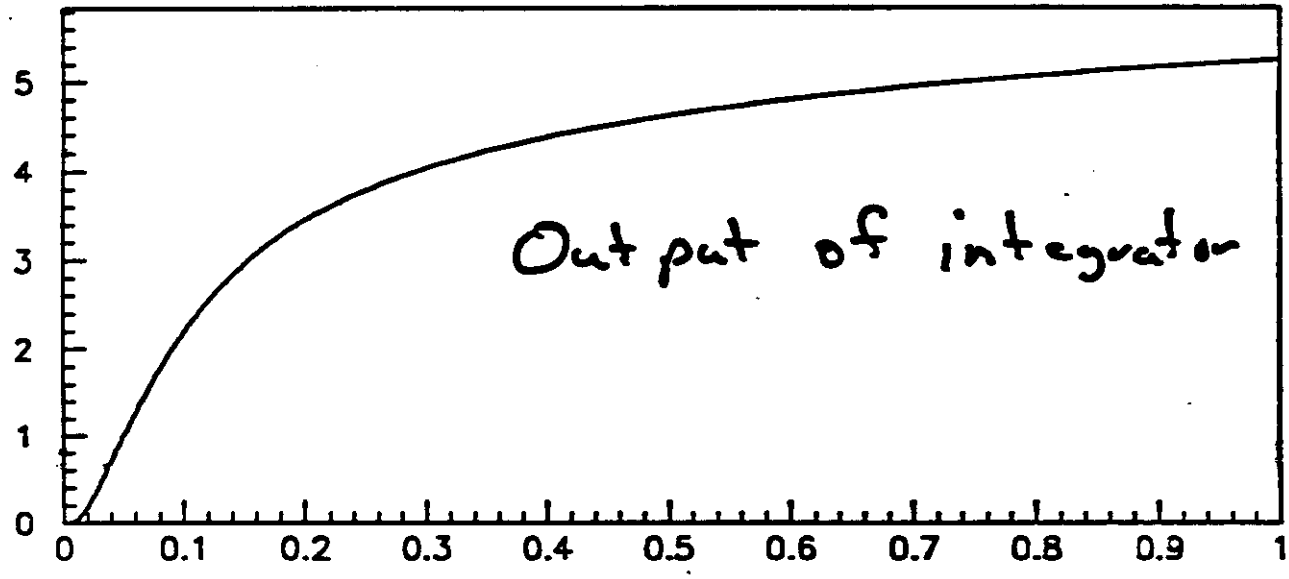


Ampfit/amp−1, corrected

"No" Shaping



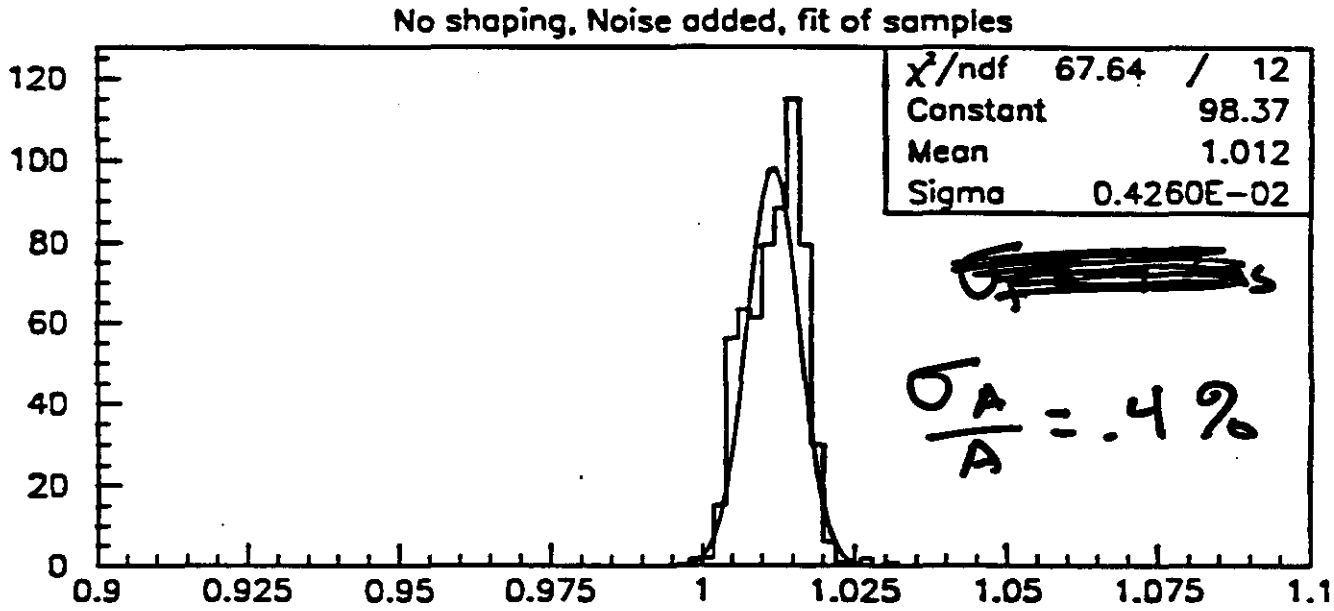
Sample input wave

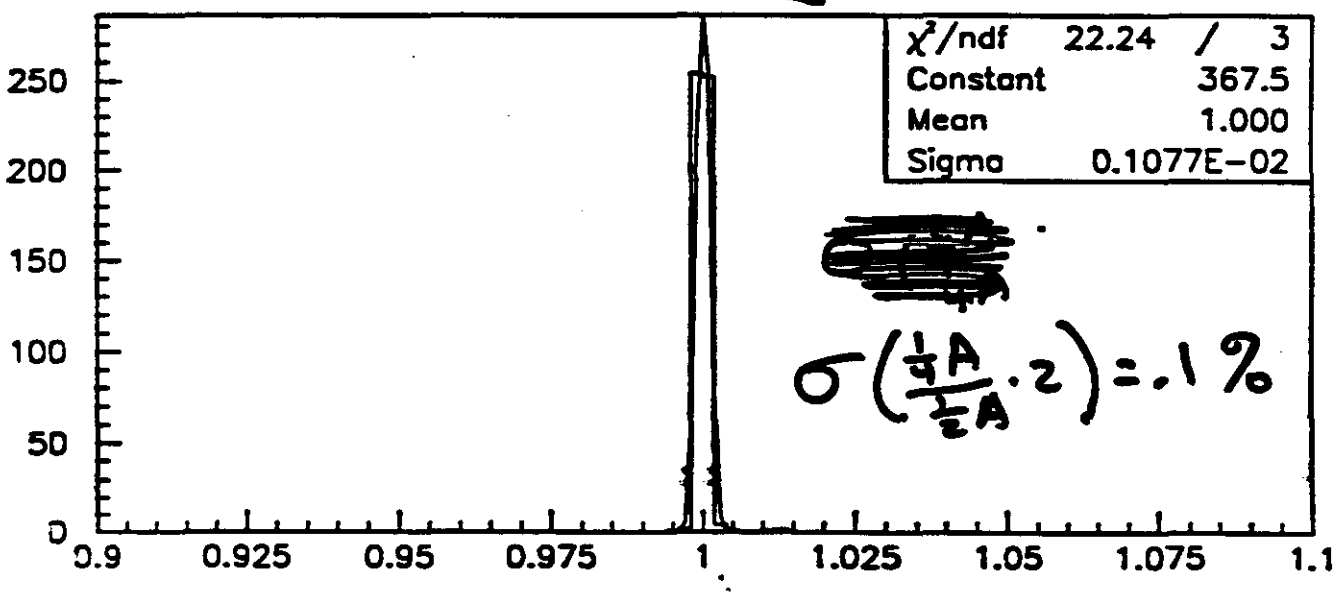


Shaped wave

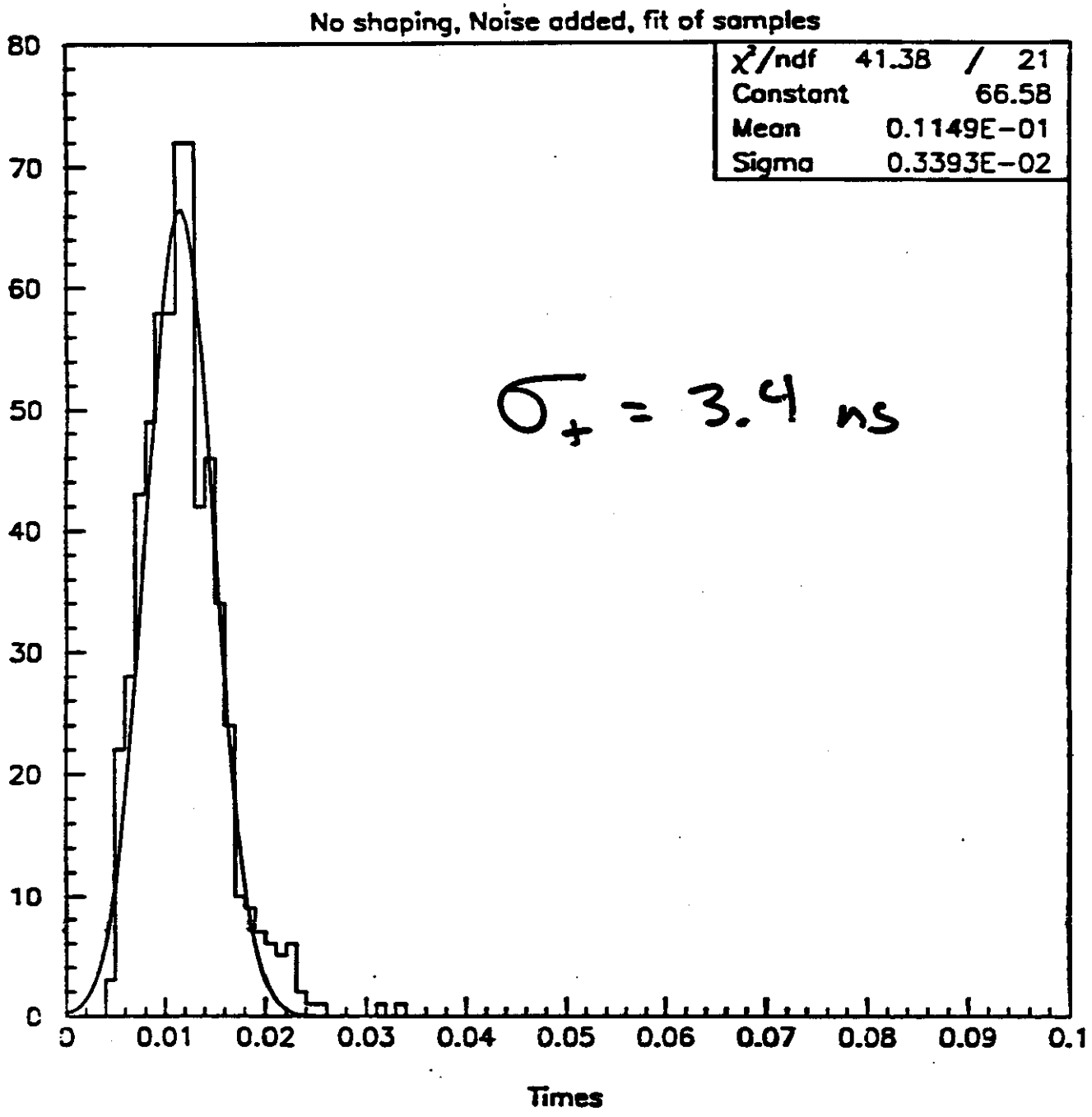
Results of 5-sample fit

Unshaped signal





Unshaped Signal Fit of 5 samples



$\sigma_t = 3.4$ ns

Conclusions

♦ Anode signals should be adequate to correctly tag the beam crossing providing care is taken to avoid tracks passing between the anode wires in all sublayers.

♦ Preliminary evidence indicates that unshaped signals will be satisfactory to determine pulse-height and timing of the cathode strip signals.

♦ More study is needed - particularly comparison of the model to actual signals from a prototype.

Meeting Summary & Conclusions

On July 18 & 19, 1993 the CSC front end readout group met at Princeton to discuss the status and plans of that work.

Present: Baringer,Broomer,Chinatti,Lan,Marlow,Pinsky,Prebys,Varner,Wixted

The following summarizes the major conclusions from that meeting.

1) The specification on operating temperature should be changed from 20 +/- 5 C to 25 +/- 5 C.

2) The CSC ROPCB design should incorporate various monitoring functions such as HV, HV current, LVPS, temperature, etc.

3) The main thrust of the R&D effort for FY94 should be aimed at producing a set of pre-production prototype electronics for the 1995 FNAL tests.

4) Each of the institutions working on the CSC readout electronics should submit a 2-3 page R&D summary for FY94. These summaries should be sent by e-mail to Dan Marlow by Aug 16, 1993.

5) The groups present expressed an interest in the following items:

   a Boston University: Work on current generation prototype analog electronics and work on support of various chamber R&D efforts (near term). Work in conjunction with BNL, PNPI, and Princeton on design of production (and pre-production prototype) anode electronics.

   b University of Colorado: Study of FEPCB design issues including thermal management, IC packaging, EMI effects, electrical interface between the IC's, selection and evaluation of an ADC/MUX set.

   c University of Houston: Work on design of ROPCB. This includes developing a specification of the operation of the control ASIC of the FEPCB.

   d Princeton University: Continued development of an SCA, an integrated Turko and Smith discriminator, and the LCT (virtual strip) logic. Completion of FPGA-based control logic.

6) A tentative plan to have another meeting in late Sept. or early Oct, possibly at BNL was made.