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Letter

Improving wafer-scale Josephson junction resistance variation in superconducting quantum coherent circuits

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Abstract

Quantum bits, or qubits, are an example of coherent circuits envisioned for next-generation computers and detectors. A robust superconducting qubit with a coherent lifetime of $O(100\ \mu s)$ is the transmon: a Josephson junction functioning as a non-linear inductor shunted with a capacitor to form an anharmonic oscillator. In a complex device with many such transmons, precise control over each qubit frequency is often required, and thus variations of the junction area and tunnel barrier thickness must be sufficiently minimized to achieve optimal performance while avoiding spectral overlap between neighboring circuits. Simply transplanting our recipe optimized for single, stand-alone devices to wafer-scale (producing 64, 1x1 cm dies from a 150 mm wafer) initially resulted in global drifts in room-temperature tunneling resistance of $\pm$ 30%. Inferring a critical current I_c variation from this resistance distribution, we present an optimized process developed from a systematic 38 wafer study that results in $< 3.5\%$ relative standard deviation (RSD) in critical current ($\equiv \sigma_{I_c}/\langle I_c \rangle$) for 3000 Josephson junctions (both single-junctions and asymmetric SQUIDs) across an area of 49 cm^2. Looking within a 1x1 cm moving window across the substrate gives an estimate of the variation characteristic of a given qubit chip. Our best process, utilizing ultrasonically assisted development, uniform ashing, and dynamic oxidation has shown $\sigma_{I_c}/\langle I_c \rangle = 1.8\%$ within 1x1 cm, on average, with a few 1x1 cm areas having $\sigma_{I_c}/\langle I_c \rangle < 1.0\%$ (equivalent to $\sigma_f/\langle f \rangle < 0.5\%$). Such stability would drastically improve the yield of multi-junction chips with strict critical current requirements.

Supplementary material for this article is available online

Keywords: Josephson junctions, uniformity, reproducibility, qubit

(Some figures may appear in colour only in the online journal)

1. Introduction

Josephson junctions, fabricated by isolating two superconductors with a thin insulating barrier, are the core circuit element for superconducting solid state quantum coherent devices. When shunted with a capacitor, the non-linear inductance from the junction forms an anharmonic oscillator making energy levels individually addressable [1]. Precise control over junction properties is crucial for state-of-the-art devices such as: quantum processors utilizing the cross-resonance gate [2], single microwave photon detectors based on ensembles of identical qubits [3], and travelling wave amplifiers where variations in nominally identical junctions lead to unwanted impedance variations [4]. Therefore, in this work we specifically focus on the reproducibility of shadow-evaporated submicron Al/AlO_x/Al Josephson junctions common to nearly all current qubits [5].

The critical current, I_c, of a Josephson junction, inversely proportional to its inductance, is tuned by either varying the critical current density, J_c, or the junction area. The former involves modifying the tunnel barrier thickness via the oxidation time or pressure when using a thermally grown barrier. Our wafer-scale fabrication process produces 64, 1 cm^2 dies from a 150 mm wafer—the maximum size accommodated by our evaporator. The junctions are located within the central $\approx$ 49 cm^2 of the die array and thus high uniformity is desired over this length scale. Previous works describe two types of Josephson tunnel junctions: large junctions, I_c $O(\mu A)$, typically realized with a Nb/AlO_x/Nb trilayer process suitable for superconducting digital electronics or microwave amplifiers; small junctions, I_c O(nA), typically realized with Al/AlO_x/Al suitable for qubits. Regarding the former, 2–4% intrachip variations have been reported [6] and $\approx$ 15% variation is observed across a wafer [7, 8]; a notable exception is [9] where 8.2% and 2.9% variation in resistance is reported for 300 nm and 800 nm diameter junctions, respectively, across a 200 mm wafer. Junctions with sizes ranging from 0.015 to 3.27 μm^2 mentioned in [10] had variations of 2.3% on 39 mm^2 chips. For qubits, it is advantageous to reduce the physical size of the junction to minimize the inclusion of noisy two level defects [11]. Authors fabricating deep sub-micron junctions typically report fluctuations of $\approx$ 5% within chips smaller than 50 mm^2 [12], 3.5% within a few mm^2 [13], and fluctuations of 2-3% for 0.04 μm^2 junctions patterned with hard masks across 50 mm wafers [14].

In this work, we strive to further improve this absolute level of resistance variation, and to realize it over a larger substrate in order to increase the yield of functional multi-qubit chips which have tight tolerances on qubit frequency. Furthermore, we investigated designs where a SQUID replaces a single junction and the magnetic flux-tunability of the circuit inductance is limited by introducing asymmetry in the SQUID junction areas ($\geq$ 5:1) to reduce the susceptibility to flux noise [1, 15]. As such, we produced small junctions over a range of areas spanning 0.003 6 to 0.013 μm^2. It is important to note that in such SQUIDs, the smaller junction only affects the tuning range so we focus on tight control over the critical current of the larger junction.

2. Methods and observations

For this study, both 100 and 150 mm wafers were used. Junctions were fabricated using the bridge-free 'Manhattan Style' [16, 17] on > 8000 Ω cm intrinsic (100) Si using e-beam lithography, see figure 1. Bridgeless junctions have an advantage over bridged designs, such as Dolan style [18], that the junction area is independent of resist thickness. Layouts were generated in python with GDSpy [19], proximity effect corrected with Beamer from GenISys, and exposed with 100 keV electrons in a Raith Electron Beam Pattern Generator (EBPG) 5150. The EBPG is housed in an enclosure made by MCRT within a class 100 cleanroom. The enclosure re-filters the air to at least class 10 and stabilizes temperatures to $\pm$ 0.05 $^\circ$C over month-scale time frames. A Spicer Consulting SC24 provides active 3-axis magnetic field cancellation from DC-13 kHz, measured at a single point next to the e-beam column. The environmental stability of the setup, combined with the Raith EBPG 5150 self-calibration protocol, provides highly reproducible lithography. Once exposed, samples are developed and subsequently coated with e-beam evaporated Al in a Plassys MEB550s with a base pressure of 3×10^{-8} mbar. After liftoff, junctions were individually probed to measure their room temperature resistance from which I_c can be inferred using the Ambegaokar-Baratoff formula [20]. These values can be converted into a qubit frequency using an estimate of the shunt capacitance. Initially, wafers were probed by hand but later, a Micromanipulator P200L semi-automatic probe station was used for the last 11 wafers to gather statistics on a larger number of junctions. Plots highlighting improvements made during this study can be found in figure 2.

2.1. Resist/exposure

The resist bi-layer was spun with a Laurell Technologies WS-650-23B spin coater. MicroChem MMA-EL13 (copolymer in ethyl lactate) was used as the high sensitivity bottom undercut layer for all wafers. Zeon Corp. ZEP 520A-7, MicroChem 950k PMMA A4, and AllResist GmbH AR-P 6 200.9 (CSAR) were all tested as the high resolution upper layer. It was found that the small ($\approx$ 20 mm diameter) vent hole in the top of the spin coater had to be covered to create a uniform spin of the MMA, which was unnecessary for the CSAR and ZEP likely because of the differences in viscosity of anisole and ethyl lactate. We initially had difficulties spinning defect free CSAR on MMA, behavior which was not observed with ZEP. This issue was solved after the resist was degassed by opening the lid and letting it sit for 2 hours allowing the pressure and humidity in the bottle to equilibrate with ambient conditions. CSAR was ultimately selected as the resist of choice over PMMA because of the flexibility it offered having (mostly) orthogonal development chemistry to MMA and over ZEP because of its lower cost. For our developers, described below, MMA and CSAR had an optimal dose of 180 and 1100 $\mu C\ cm^{-2}$ respectively. We note that partial clearing of CSAR in MMA developer was observed for doses above 1100 $\mu C\ cm^{-2}$ when immersed for extended times.

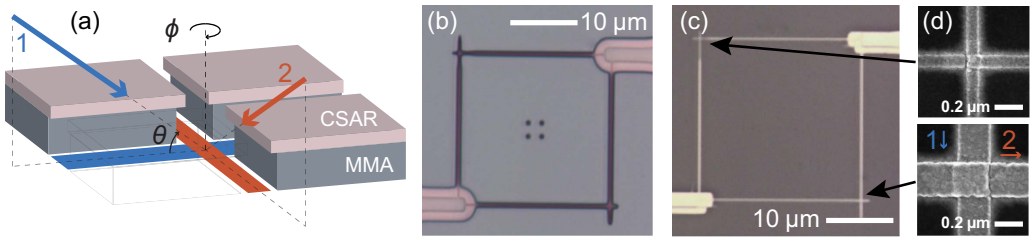

Figure 1. Device geometry for the asymmetric SQUID used in this study. (a) Sketch of the resist stack for 'Manhattan Style' junctions. Developed features are designed to be deeper than their width to allow metal to reach the substrate when evaporated parallel to a given channel, but block metal in orthogonal channels. Thermal oxidation of layer 1 occurs before rotating the substrate and depositing layer 2. A third layer, rotated by $\phi = 180^{\circ}$ relative to layer 2 (not shown) is required to form the second SQUID junction. A high sensitivity resist (MMA) results in a undercut of the high resolution top layer (CSAR) to improve liftoff quality. (b) Micrograph of the developed resist stack. (c) Micrograph of the final SQUID structure. (d) Scanning electron microscope images of the two Josephson junctions forming the 8:1 asymmetric SQUID on wafer 37.

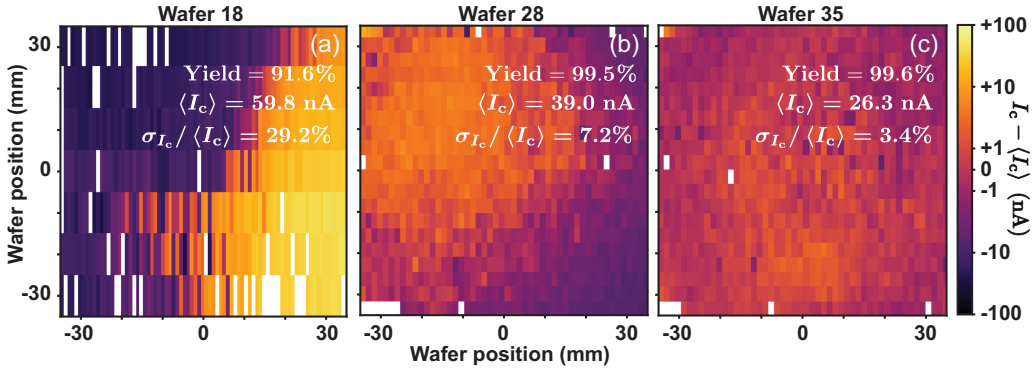

Figure 2. Select wafer-scale resistance variation data for 6:1 asymmetric SQUIDs. Shown here are improvements in uniformity over the course of this study with inferred I_c plotted as the difference from the mean of each wafer with a common z-axis. White cells indicate a junction that was open or shorted. (a) The first wafer-scale statistics acquired (wafer 18). (b) First wafer probed with the automated probe station and after implementation of dynamic oxidation and attenuated ultrasonic MMA development (wafer 28). (c) Current uniformity after implementing improved ashing, slower evaporation rate, and larger junctions with lower J_c. Yield is calculated excluding failures due to patterning junctions in the resist edgebead.

Proximity effect correction (PEC) in Beamer was first optimized by observing the uniformity (or lack) of residual undercut as the MMA provides a sensitive indicator of long range substrate backscattering compensation. The software's 3D-Edge mode of 3D PEC was chosen due to its ability to simultaneously proximity effect correct both resist layers which require different doses and a default point spread function (PSF): 500 nm PMMA on Si at 100 keV (Z-Position: 0.325) was used initially. Before the addition of short range corrections to this PSF, we had low yield of sub 100 nm features with CSAR which we did not observe with ZEP. The short range corrections that were added to improve yield were: an effective short range blur FWHM of 50 nm, a short range separation value of 5 μm, and a mid-range activation threshold of 2%. A 200 pA beam and 200 μm aperture (calculated spot size = 2 nm) was used with a 1 nm beam step size to ensure that designed area variations on the order of a few nm were reproduced. Backscatter dosing from the probe pads (which are not written on device wafers) were written 130 μm away (~ 4x the backscattering parameter for 100 keV electrons on Si) to ensure test wafers created junctions equivalent to device wafers.

SEM observations of as-evaporated junctions showed worse line edge roughness (LER) on the second evaporation compared to the first (see figure 1). Our theory is that Al deposited on the sidewall of the CSAR in the first evaporation introduces additional LER for subsequent evaporations. A tri-layer resist (MMA/CSAR/MMA) was briefly considered in an attempt to reduce this effect utilizing the top layer of MMA to shield the CSAR during off-axis evaporations. We did observe an improvement in LER, but since it did not reduce global I_c variations, it was abandoned due to its added complexity and the additional forward beam scattering from the top MMA would result in increased developed linewidths [21], limiting achievable SQUID asymmetry ratios.

2.2. Development

Cold development with manual agitation (or ultrasonication for wafer 36) was used for CSAR and ZEP. A Thermo Scientific PC200 immersion circulator filled with 50:50 H_2O: Propylene Glycol was used to chill N-amyl acetate (NAA) baths to $0 \pm 0.02\ ^{\circ}$C. NAA from Zeon corp. (ZED-N50) was used initially and AllResist GmbH AR 600-546 was used after wafer 26. No difference was noted between these nominally identical developers. The MMA was developed at room temperature and puddle development was briefly considered, but led to many CSAR constrictions so was abandoned in favor

Table 1. Summary of wafers made after delivery of automated probe station.

Parameter \ Wafer		28	29	30	31	32	33	34	35	36	37	38
oxidation		dyn	stat	dyn	dyn	dyn	dyn	dyn 2P, 2t	dyn 2P, 2t	dyn 2P, 2t	dyn 2P, 2t	dyn 2P, 2t
ashing		4x	4x	16x	16x	none	4x	4x	16x	16x	16x	16x
evaporation rate (nm/s)		3.0	3.0	3.0	3.0	3.0	0.3	0.3	0.3	0.3	0.3	0.3
fresh NAA		y	n	n	y	y	y	y	y	y	y	y
agitation during MMA dev		y	n	n	y	y	y	y	y	y	y	y
CSAR dev ultrasonication		n	n	n	n	n	n	n	n	y	n	n
single junction design size		A	A	A	A	A	A	1.06A	1.06A	1.06A	1.4A	1.4A
single JJ $\overline{I_c}$ (nA)		65.6	94.7	63.1	64.2	30.8	55.3	34.1	26.1	26.3	32.6	33.2
6:1 SQ junction design size		A	A	A	A	A	A	1.7A	2.2A	2.2A	2.9A	2.9A
6:1 SQ $\overline{I_c}$ (nA)		39.0	47.0	35.0	37.6	20.5	29.0	27.7	26.3	27.0	34.5	34.7
$\sigma_{I_c}/\langle I_c\rangle$ (%)	single JJ	6.5	9.1	3.5	5.2	10.8	3.6	4.4	3.1	3.7	3.8	3.1
	6:1 SQ	7.2	9.6	9.2	6.7	7.8	7.5	4.9	3.4	5.0	4.1	4.9
	8:1 SQ	7.5	8.4	8.0	6.9	8.2	7.4	4.9	3.5	5.1	4.3	4.7
$\overline{\sigma_{I_c}/\langle I_c\rangle_{1x1cm}}$ (%)	single JJ	1.8	2.8	2.3	3.5	6.7	1.7	2.5	1.8	2.0	1.9	2.1
	6:1 SQ	2.2	5.6	5.2	5.3	5.3	5.1	2.8	2.3	2.5	1.9	2.0
	8:1 SQ	2.3	5.1	5.0	4.9	5.1	5.1	2.8	2.3	2.4	2.1	1.9

Summary of modified process variables and uniformity results for the 11 wafers measured using automatic probing. The aluminum crucible was refilled after wafer 34. 2P, 2t refers to double oxidation pressure and time compared to unspecified cases. Agitation during MMA development is a gentle manual agitation of the wafer in the ultrasonic bath. Junction design size specifies nominal relative junction areas, useful when comparing average I_c between wafers. Wafer-to-wafer repeatability can be evaluated by comparing wafers 35/36 and 37/38.

of immersion development on PTFE wafer holders. Initially IPA:MIBK was used to develop the MMA but we observed many open junctions due to small resist bridges constricting the CSAR near the junction, especially for < 0.01 μm^2 junctions. Our hypothesis was that swollen, gel-like MMA removed by the developer [22] was the cause of these constrictions. Studies with PMMA (which has much higher molecular weight than MMA), showed that the co-solvent IPA:H_2O was a superior developer, resulting in reduced swelling and the addition of sonication was shown to increase the rate at which developed resist is removed [23–26]. Although the switch of developer alone did not drastically improve small junction yield, the addition of sonication did. Care had to be taken to attenuate the ultrasonication power to prevent collapse of the CSAR overhang which was accomplished by using the lowest bath power and, crucially, lining the bath with a polyurethane/vinyl sound absorbing foam, leaving the central 1x1 cm open to allow some power transmission.

After development, oxygen plasma ashing of the newly opened channels is performed. We used a Plasma Etch PE-50 with a 50 kHz pure oxygen plasma (80 s, $\approx$ 500 mbar, $\approx$ 60 W). It was found that large, non-radially symmetric I_c gradients were reduced and made more radially symmetric by splitting a single ashing step into four, 20 s steps with 90° substrate rotations between steps. In an attempt to further improve the ashing uniformity, the sample was rotated four times in each corner of the chamber, for a total of 16 x 5 s ashes. This resulted in the best wafer-scale statistics at the time: $\sigma_{I_c}/\langle I_c\rangle = 3.5\%$ for single junctions across 49 cm^2. Eliminating ashing resulted in worse $\sigma_{I_c}/\langle I_c\rangle$ but also a 2x reduction in J_c, strong evidence that residual organics have an effect on tunnel barrier properties [13, 27, 28].

After implementing 16x ashing, the dominant source of non-uniformity was found to be junction area variations which showed approximately radial dependence. First, the effect was reduced simply by increasing the junction area (and decreasing J_c to keep I_c constant). To test if this was introduced during development in NAA, manual agitation was replaced by ultrasonication for wafer 36 due contrast improvements seen in [29] and assumed higher uniformity. However, this showed no improvement and a ~ 1 cm^2 patch of abnormally low J_c on the wafer caused an overall $\sigma_{I_c}/\langle I_c\rangle$ degradation. Pinpointing the cause of, and a solution to, the area fluctuations is the path towards better wafer-scale uniformity for this process. To this end, a hard mask process would be helpful as it should be more robust during evaporation and diagnostic post-development SEM imaging.

2.3. Evaporation and oxidation

Motivated by the hypothesis that high energy electrons and UV radiation released during the evaporation could warp or distort the resist non-uniformly and produce the observed area fluctuations, a deposition rate of 3 nm/s was used for the majority of this study. However after other process optimizations, better uniformity was observed using a rate of 0.3 nm/s. Lower deposition rates provide more time for a growing film and substrate to thermalize, forming smaller grains [30]. Since the tunnel barrier thickness is not uniform grain to grain or at grain boundaries [31–33], we hypothesize that more grains per junction results in better averaging of the effective barrier thickness, improving site to site uniformity. To investigate this, cross section TEM analysis of junctions fabricated with the two deposition rates is ongoing [34]. Dynamic and static oxidations were also A/B tested. In a static oxidation, the chamber is filled with oxygen (in our case 95%/5% Ar/O) to a set pressure and then evacuated after a set time. In a dynamic oxidation, gas is continuously introduced and pumped out with rates

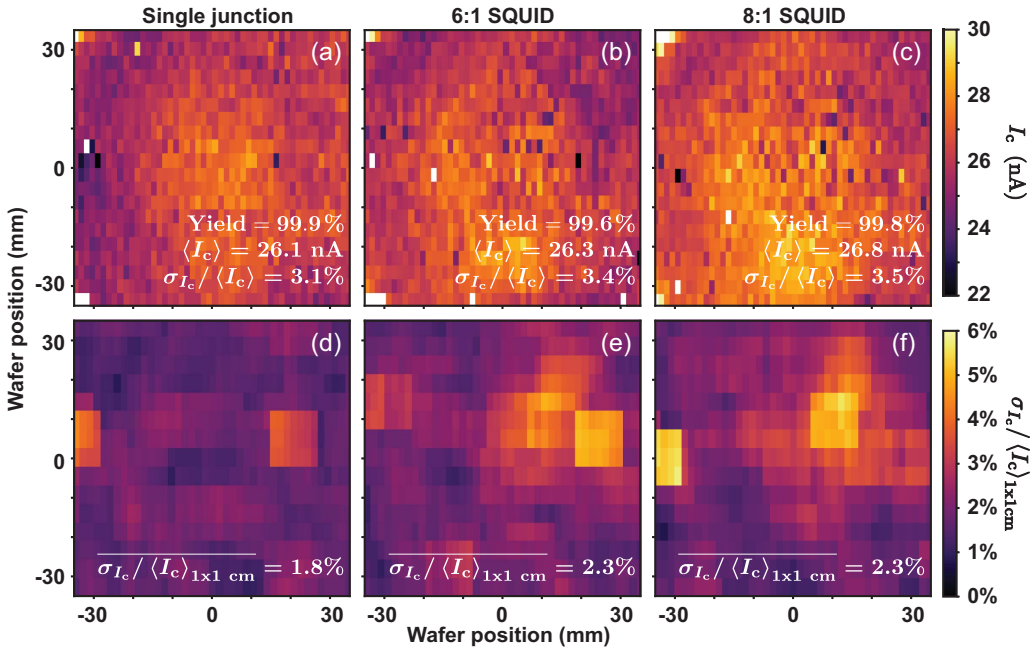

Figure 3. Wafer map of Josephson junction critical currents observed for wafer 35. (a), (b), (c) I_c values with white cells indicating a junction that was open or shorted. (d), (e), (f) $\sigma_{I_c}/\langle I_c\rangle$ for the 27 junctions of a single design within a 1x1 cm moving window. (a), (d) Fixed frequency single junction. (b), (e) 6:1 asymmetric SQUID. (c), (f) 8:1 asymmetric SQUID.

balanced such that the pressures are the same as the static oxidation case. Interestingly, we found dynamic oxidation produced a lower J_c and since it provided better uniformity, it was used for the remainder of the study.

3. Results

Wafers (which each had 1000 fixed frequency junctions, 1000 6:1 SQUIDs, and 1000 8:1 SQUIDs patterned in alternating rows of 50) made after delivery of the automated probe station are summarized in table 1. The full recipe yielding the highest uniformity can be found in the supplementary material (available online at stacks.iop.org/SUST/33/06LT02/mmedia) and the junction properties from wafer 35 are plotted in figure 3.

3.1. Qubit coherence and frequency predictability

Many measurements are still needed to rigorously correlate the observed improvements in junction uniformity with ultimate device performance. Nonetheless we describe here example measurements of two co-fabricated 8-qubit quantum processors. The 8 fixed-frequency transmon qubits on each chip had a mean target frequency of 5.6 GHz with detunings between neighbors optimized for the cross-resonance gate [2]. Fabricating 64 chips on a 150 mm Si wafer and binning the 64 junctions of each size across the wafer, we find an average $\sigma_{I_c}/\langle I_c\rangle = 6.9\%$, a 3.8x improvement over an 8-qubit ring wafer made using a process similar to wafer 29 (where MIBK was used instead of H_2O for MMA development). With this narrower distribution of critical currents, we found 3/64 chips had optimal qubit frequencies, consistent with numerical estimates of chip yield given the measured $\sigma_{I_c}/\langle I_c\rangle$. We hypothesize that the remaining ~ 2x discrepancy in $\sigma_{I_c}/\langle I_c\rangle$ between test wafers 35, 37 and 38 and the latest device wafer may be explained by the additional round of lithography that device wafers require after junction deposition (including resist baking and ion-milling) to define the low-loss junction-capacitor interconnects [36] or the different substrate surface between test and device wafers (RIE etched vs polished Si). The chips were wirebonded in two designs of Cu boxes and tested in separate dilution refrigerators. Coherence measurements and frequency predictability are summarized in table 2. Given the long lifetimes measured on sample #1, we conclude that the fabrication modifications made to improve uniformity do not come at the expense of qubit coherence. See

Table 2. Average qubit properties from a device wafer fabricated with the high-uniformity junction recipe of wafers 35, 37, and 38.

Sample #1:	average of 8 qubits
f_{01} (probing est.) (GHz)	5.803
f_{01} (difference at 8 mK)	$-2.62\% \pm 0.50\%$
T_1 (μs)	104
T_2^* (μs)	60
T_{2Echo} (μs)	107
Sample #2:	**average of 8 qubits**
f_{01} (probing est.) (GHz)	5.651
f_{01} (difference at 14 mK)	$0.38\% \pm 0.40\%$
T_1 (μs)	45
T_2^* (μs)	31
T_{2Echo} (μs)	49

Frequency estimates from room temperature junction resistance and simulated capacitance show good agreement with actual qubit frequencies, especially when considering detunings between neighbors. Coherences are quoted as the average value of the 8 qubits per chip. Data on individual qubits can be found in the supplementary material.

the supplementary material for discussion of the observed offsets between probing estimates and cryogenic measurements, the suppressed coherence of sample #2, and data on individual qubits.

4. Conclusions

Motivated by the challenging task of maintaining high Josephson junction uniformity when scaling quantum coherent circuit fabrication beyond a few qubits, we undertook a systematic study to identify and rectify sources of I_c variation. We have developed a process which has shown a $\sigma_{I_c}/\langle I_c\rangle$ as low as 3.1% over 49 cm^2 for single junctions. Looking within a chip sized 1 cm^2 window to remove global drift, an average $\sigma_{I_c}/\langle I_c\rangle = 1.8\%$ was measured with some areas $< 1.0\%$. To accomplish this, a reliable resist stack was found by changing proximity effect correction parameters and studying different development strategies, of which ultrasonication played a key role in producing high yield structures. Large gradients introduced by non-uniform ashing were mitigated by adding substrate rotations into that process, which may not be necessary with a more uniform asher. Slower evaporation rates and dynamic oxidations were then shown to further improve uniformity. Current levels of uniformity should be improved by minimizing the observed junction area fluctuations, whose origin is not currently understood. However, since $\sigma_{I_c}/\langle I_c\rangle$ within chip sized areas is small, detunings between qubits on a single chip can be accurately set and the non-zero global I_c drift can be used to target absolute frequencies; a useful capability as tolerances become tighter for quantum processors and microwave photon detectors growing in complexity, size, and qubit number.

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