Implementation of White Rabbit Time Synchronization System in State Acquisition System of High-energy Physics Experimental Device

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Abstract. The state acquisition system of high energy physics experimental device has very high requirements for the clock synchronization accuracy of each node. The White Rabbit (WR) distributed synchronous timing technology can realize multi node sub nanosecond clock distribution within several kilometers, and meet the requirements of clock synchronization accuracy of the system. This paper presents an implementation of WR timing system with ZYNQ 7045 as the core in the state acquisition system. This paper introduces the hardware design and implementation scheme of collector node, the implementation scheme of WR node, and the statistical data of WR-PTP time synchronization experiment results. The test results show that this method can realize the time synchronization between the nodes of the state collector, and the accuracy is better than 1 nanosecond. It can provide high-precision time synchronization function for the multi node signal acquisition system of high-energy physics experiment.

1. Introduction

Modern high-energy particle physics experimental devices are numerous and distributed in a wide space [1-2]. In order to ensure the normal operation of each device and the reliability of experimental data, its working state must be collected and fed back. The realization of multi node and high-precision condition monitoring has very high accuracy and stability requirements for the clock of each node of the condition monitoring system.

WR-PTP protocol is a sub nanosecond time synchronization technology based on optical fiber ethernet [3], which can realize time synchronization between tens of thousands of nodes in a wide range (< 10km) [4], and is widely used in distributed network measurement and control, 5G base station network time synchronization[5]. In order to meet the requirements of high-precision time synchronization between each node of the state acquisition system of high-energy physics experimental device, WR-PTP protocol is selected to realize sub nanosecond time synchronization of each node.

2. Materials and Methods

2.1.collector electronics design scheme

2.1.1. Overall system architecture
The overall design of the system is shown in Figure 1. Relying on WR time synchronization technology, a high-precision global time service network is established to realize sub nanosecond time synchronization of each monitor node. In terms of specific modules, the architecture is based on white rabbit (WR) protocol, including WR clock reference source, WR switching network, WR node, front-end electronics fee, DAQ system, etc. Among them, WR clock reference source is composed of a GPS timing machine and a WR top-level interactive machine; WR switching network is composed of multiple WR switches; WR node consists of monitor front-end electronics.

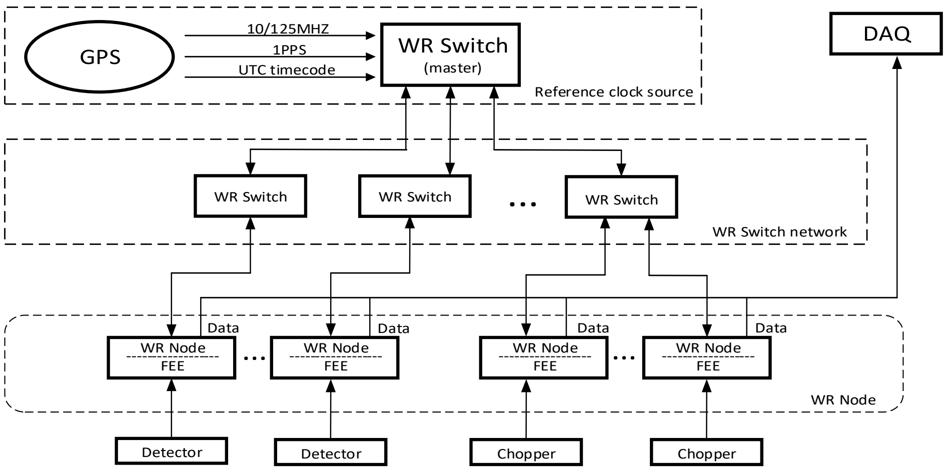


Figure 1. Electronic layout scheme of state acquisition system

2.1.2 Hardware design and implementation of signal collector based on ZYNQ + FPGA
On the premise of meeting the operation requirements of WR time synchronization system and the signal acquisition quality requirements of spectrometer supporting equipment, the hardware of signal collector based on ZYNQ + FPGA is designed and developed, and its principle diagram is shown in Figure 2. The acquisition of status signal is realized based on low-cost FPGA chip 10m08sae144c8g, and WR-PTP time synchronization technology and data processing are realized based on zynq7000 chip xc7z045ffg900. After the FPGA chip completes the data acquisition, it sends the data to the ZYNQ chip through serial communication. The two combine with each other to realize high-precision spectrometer equipment status signal acquisition and data transmission. In addition, the level selection function is added at the signal receiving end to provide 5V or 24V signal level selection to meet the application requirements of different equipment.

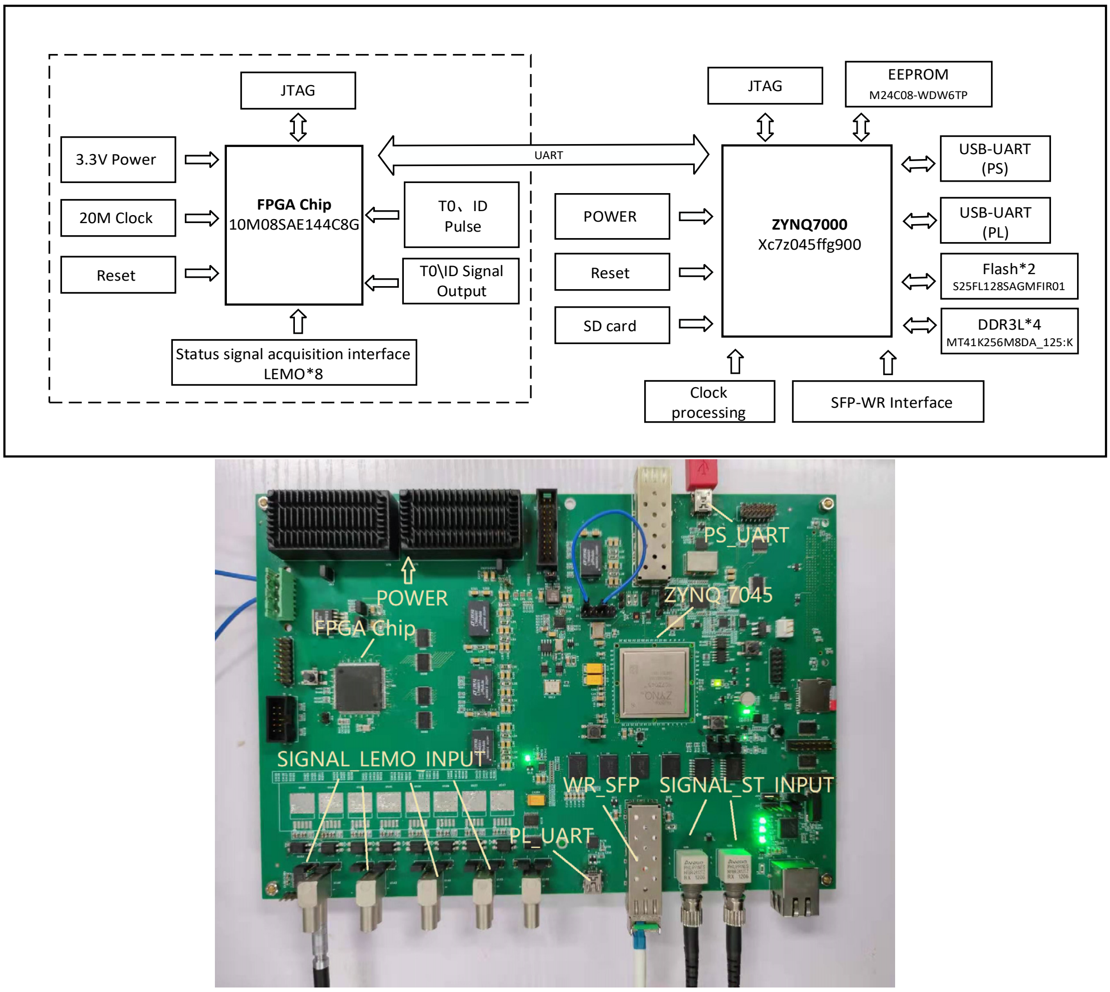


Figure 2. Circuit design scheme and hardware diagram of signal collector

2.2.Principle of WR time synchronization technology and Realization of WR-PTP node
White rabbit protocol is a high-precision distributed timing protocol based on optical fiber Ethernet [6]. As shown in Figure 3 (a), it is a chain time synchronization model of white rabbit protocol. Firstly, the White Rabbit protocol needs to build the clock loop between the master and slave nodes through the optical fiber transmission link, and then complete the high-precision time synchronization of the master and slave nodes based on PTPv2 protocol and clock data fusion technology. During synchronization, master is the time service node and slave is the time service node. The master terminal and slave terminal are connected through optical fiber. The synchronization includes time synchronization and clock phase synchronization.

2.2.1 Time synchronization
Time synchronization is based on PTPv2 synchronization principle, which was introduced by IEEE in 2008 [7]. In the process of synchronization, the time difference between the master and slave is corrected mainly by measuring the round-trip delay [6]. The synchronization process is shown in Figure 3 (b).

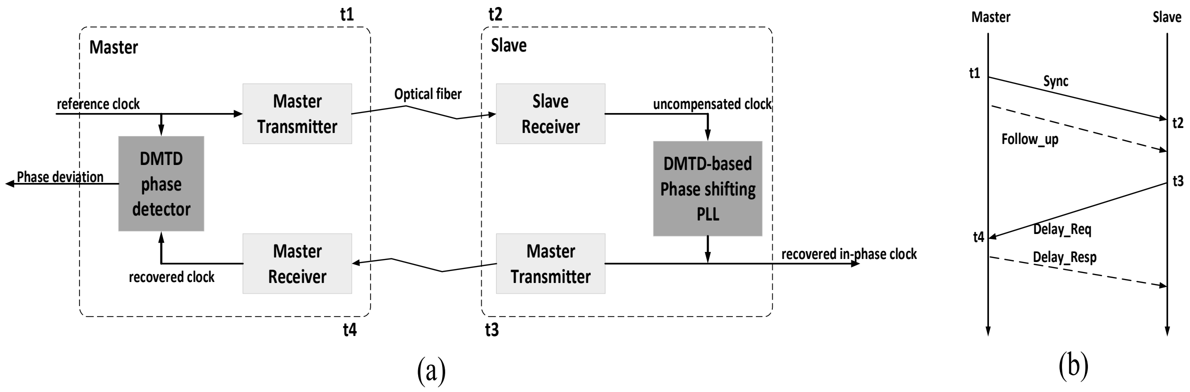


Figure 3.White Rabbit protocol chain time synchronization model and PTP synchronization mechanism

The specific process of PTPv2 synchronization message exchange is as follows: (1) the master node sends a sync message to the slave node, records the sending time as t1, and passes this t1 timestamp through follow_up message is sent to the slave node; (2) The slave node receives the sync message and records the receiving time as t2. The slave node receives follow_up message, obtain t1 timestamp; (3) Slave node sends delay_Req message and record the local sending time t3; (4) Master node receives delay_Req message, record the receiving time t4 and send it through delay_Resp message is sent to slave node; (5) Slave node receives delay_Resp message, obtain the t4 timestamp. So far, the slave node obtains the t1, t2, t3 and t4 timestamp, calculates the time difference between the master and slave using the timestamp,and adjusts the local time.

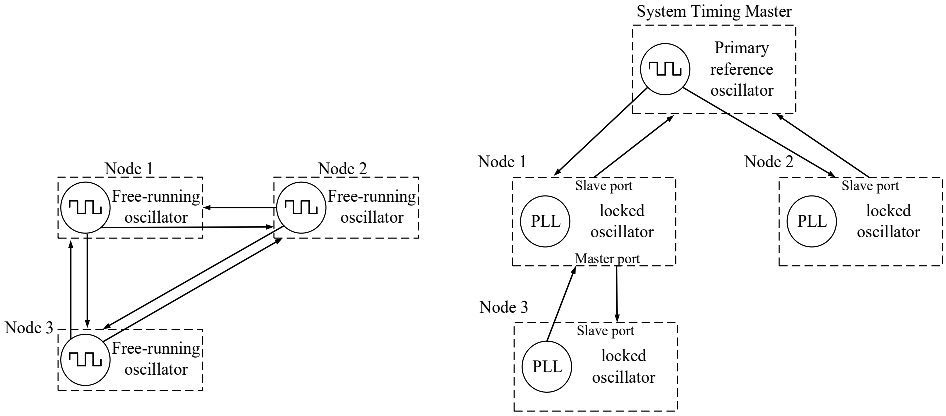
According to the PTP protocol, the link delay of the master and slave can be calculated: $\text{delay}_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$; The time difference between master and slave is $\text{offset}_{ms} = t_2 - t_1 - delay_{ms} = \frac{t_2 - t_1 + t_3 - t_4}{2}$.

2.2.2 clock phase synchronization

On the basis of full compatibility with PTPv2 protocol, White Rabbit protocol adopts synchronous Ethernet, Dual mixer time difference technology(DMTD) and WR synchronous link model to complete clock phase synchronization and improve the synchronization accuracy to sub nanosecond level [8].

(1)Synchronous Ethernet

WR technology adopts synchronous Ethernet to realize the same clock frequency of each node. As shown in Figure 4, in standard Ethernet,the clocks of each node operate independently. In synchronous Ethernet, all nodes form a clock network topology. Sub nodes or sub switches use clock and data recovery (CDR) technology to recover the clock from the data link, and eliminate the jitter caused by the clock recovery circuit from the PLL inside the node. The recovered clock is not only the system clock of the slave node, but also the reference clock of the next node. In this way, the clock frequency of all nodes of the whole network is consistent with that of the root node [9].



(a) Standard Ethernet (b) Synchronous Ethernet

Figure 4. Comparison between standard Ethernet and synchronous Ethernet

(2)Dual mixer time difference technology(DMTD)

In order to further improve the time synchronization accuracy, the white Rabbit protocol uses the phase detector to accurately measure the phase difference between the data recovery clock and the local clock and correct the time stamp, so as to further improve the time synchronization accuracy of PTPv2 technology and bring it into the sub nanosecond level.

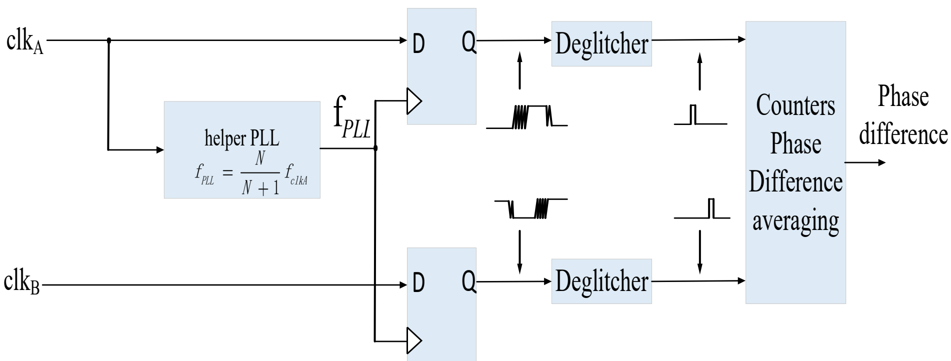


Figure 5. Principle of DMTD phase detection

The operation principle of DMTD is shown in Figure 5. ClkA and clkB represent the local clock and the recovery clock in the data stream respectively. They have the same frequency but different phase. An auxiliary clock signal is generated by an external phase-locked loop, and a small difference ($f_{PLL} = \frac{N}{N+1} f_{clkA}$)exists between the frequency of the signal and the frequency of the measured signals (clk_A and clk_B). Therefore, after sampling, D flip-flop will output a very low-frequency signal [6]. By measuring the phase difference of the output signal of D flip-flop, the phase difference of the measured signal can be calculated. The phase detector, filter control circuit and voltage controlled oscillator at the node constitute a phase-locked loop circuit to realize the phase locking and phase adjustment of the slave node clock.

(3)WR synchronous link model

The synchronization link of WR master-slave node is shown in Figure 6. The total delay of the round-trip link can be regarded as composed of three parts [11]: (1) Hardware delay of transceiver circuit of master-slave node(Δ_{TXM} , Δ_{TXS} , Δ_{RXM} , Δ_{RXS}); (2) Bit sliding delay caused by word alignment operation in serial parallel conversion circuit(ε_M , ε_S); (3) Optical fiber link transmission delay(δ_{MS} , δ_{SM}).

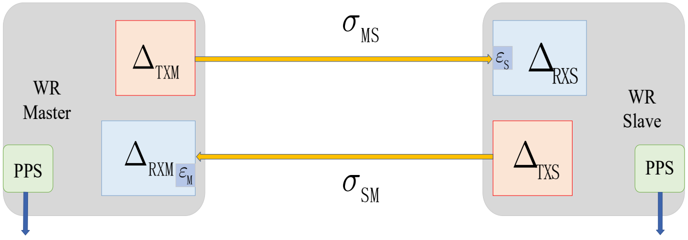


Figure 6. WR synchronous link model

The refractive index of optical fiber to different wavelength light is different, which leads to the difference of transmission delay of optical fiber link(δ_{MS} and δ_{SM}).WR defines the fiber asymmetry coefficient α describe their relationship as $\alpha = \frac{\delta_{MS}}{\delta_{SM}} - 1$. so as to achieve automatic calibration.

2.2.3 WR PTP node implementation

This paper is based on WRPC-v4.2 (White Rabbit PTP core) kernel[8] realizes WR time synchronization function on ZYNQ 7045 chip, and customizes peripheral hardware system, FPGA system and embedded system according to actual needs. As shown in Figure 7, it is the implementation block diagram of WR-PTP node, and its specific composition is as follows:

The peripheral hardware system mainly includes SFP optical transceiver, USB-UART and other interface circuits, clock processing circuit, power supply system and external memory (flash, EEPROM, DDR3L). The FPGA system is designed in VHDL language,mainly including latticemicro32 soft core processor (LM32), Minic network interface controller, MAC layer implementation (WR Endpoint), Wishbone bus, 1 PPS generator, UART interface, IRIG-B time encoder, etc. The design of embedded software system is based on LM32 soft core, mainly including WR-PTP protocol software, soft PLL, network protocol.

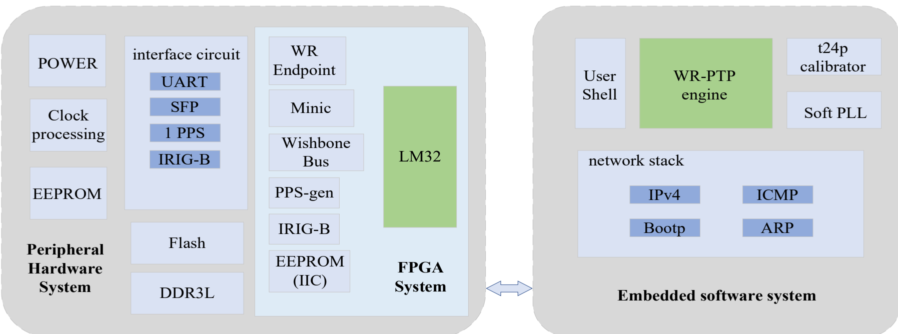


Figure 7. Implementation block diagram of WR-PTP node

3. Results & Discussion

3.1. WR-PTP time synchronization test of equipment

The test environment uses a WR switch and a signal collector node, and uses a 1909m long single-mode optical fiber to form a master-slave WR network structure. The two devices use their internal clock to regularly output a second pulse(PPS), and the WR-PTP time synchronization accuracy is given by measuring their deviation value. By connecting the PPS output of WR switch and the PPS signal of signal collector node to the oscilloscope at the same time, the synchronization results of two second pulses can be observed. The test results are shown in Figure 8 below. The Yellow waveform in the figure is the PPS signal of signal collector node, and the green waveform is the PPS signal generated by WR switch.

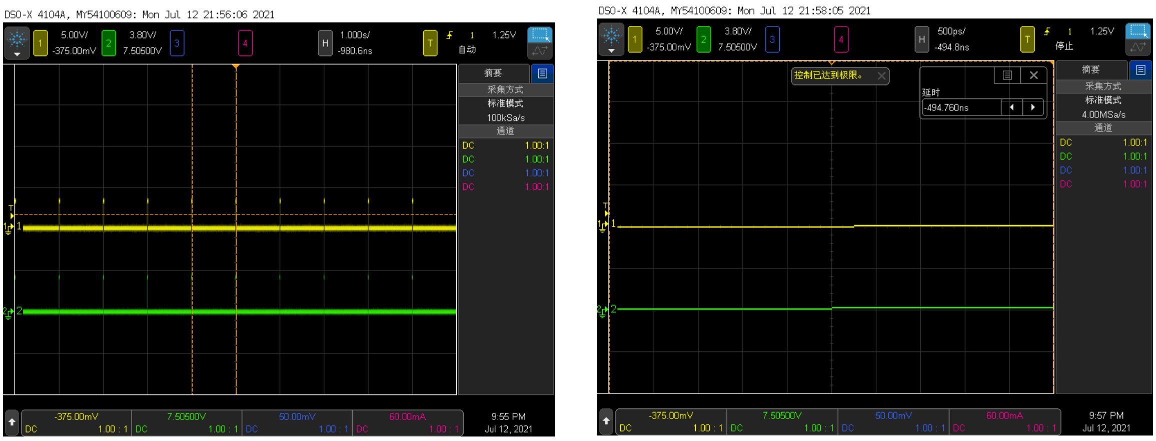


Figure 8. synchronization results of two PPS signals

In the test process, the delay of two PPS signals is continuously measured for 2000 times, and then the measured data are statistically processed. After Gaussian fitting, the probability density distribution of delayed data is shown in Figure 9 below, which conforms to the normal distribution. The measurement results show that the average delay of the two PPS signals is 250ps and the Sigma value is 23.12ps. The PPS signals of WR master-slave nodes can achieve sub nanosecond synchronization.

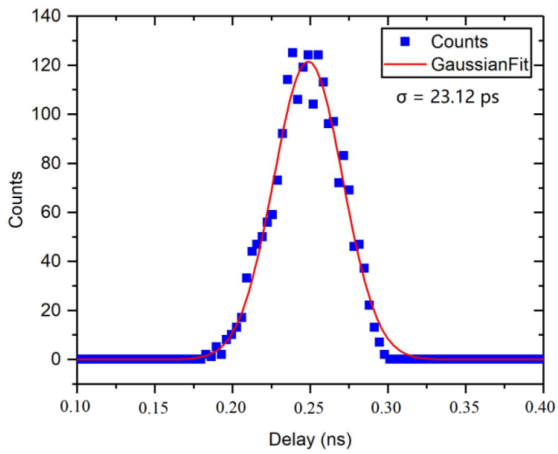


Figure 9. statistics of WR synchronization accuracy test results

4. Conclusions

In this paper, WR time synchronization technology is used to realize high-precision time synchronization between the state acquisition nodes of the state acquisition system of high-energy physics experimental device. WR is a new improved time synchronization method based on PTP protocol and synchronous Ethernet.It improves the synchronization accuracy to sub nanosecond level through DMTD and WR synchronization link model, and is suitable for multi node and wide range. The test results show that the WR time synchronization network realized in this paper can realize the time synchronization accuracy between the nodes of the state collector, which is better than 1ns. It solves the time service requirements of long-distance multi node and high-precision of the state acquisition system of the high-energy physics experimental device, and makes the system run accurately, reliable and easy to maintain, It can be used as the key supporting technology of the state acquisition system of high-energy physics experimental device.

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