

# Fast Sampling and Read-Out for Ground-Based Imaging Cherenkov Telescopes

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**Abstract.** The SCT telescope has been proposed as a medium-sized telescope for the Cherenkov Telescope Array. One of the major upgrades is the design of the new Front End Electronics Module (FEEM). New FEEMs aim to read-out and digitize the SiPM pre-amplified signals down to the single photoelectron (phe). This phe signal is assumed equivalent to a signal with 2 mV peak amplitude and 500 MHz maximum bandwidth. FEEM should have a linear response up to 2 V for a required dynamic range of 1000 phe. FEEM noise equivalent of 0.5 phe - 1 mV of RMS noise - is an acceptable value. Due to the severe mechanical constraints, and to have a very compact electronics and low noise performance, FEEM consists of two stacked-up submodules, one dedicated to the power supplies and the other to house the FPGA, which reads out and sends digitized data to the main backplane. An FEEM is capable of digitizing 64 analog channels with a sampling frequency of 1 GSamples/s.

## 1. Introduction

One of the most effective techniques to detect gamma rays at very high energies is the imaging of Cherenkov light from atmospheric showers. This field is soon to be revolutionized by the advent of the Cherenkov Telescope Array (CTA), which is meant to improve the sensitivity by about an order of magnitude, to extend the energy range, from a few tens of GeV to above 100 TeV, with enhanced angular and energy resolutions over existing imaging atmospheric Cherenkov telescope (IACT) systems [1] [2].

The large number of telescopes required to reach the performance aimed at for CTA calls for innovative ways to reduce their cost. One of the proposed solutions is using dual-mirror optics along with a compact camera design enabled by modern photosensors like multi-anode or silicon photomultipliers. This helps to bring down the costs by reducing the area that needs to be instrumented with photosensors to achieve the desired field of view.

One of the most important features is the analog to digital sampling of the signal coming from the photosensors. For this aim, an application-specific integrated circuit (ASIC), named TARGET, has been developed and housed in the board presented here.

TARGET is the acronym of TeV Array Readout Electronics with GSamples/s sampling and Event Trigger. This is an ASIC designed to read out fast analog signals with a sampling frequency typically 1 GSample/s.

The TARGET use is envisaged in the cameras of various CTA telescopes, e.g. the Gamma-ray Cherenkov Telescope (GCT) [3], a proposed 2-Mirror Small-Sized Telescope, and the Schwarzschild-Couder Telescope (SCT) [4], a proposed Medium-Sized Telescope, both officially used for the Cherenkov Telescope Array (CTA) [5].

The new version of the board, called FEEM is capable of reading 64 photodetector pixels and connected to a backplane via Gbit Ethernet, to manage data retrieved from the target chips.



The working principle and main features of TARGET, as well as a description of FEEM will be given in detail.

## 2. TARGET ASIC

TARGET is an ASIC designed to read out fast analog signals with a sampling frequency of typically 1 GSample/s, which is especially suited for imaging Cherenkov radiation from atmospheric showers. In its latest version, TARGET-C [6], it is devoted to the sampling, storing and digitization phases by means of a Wilkinson Analog to Digital converter (ADC). Thanks to a large number of channels (16 channels), low cost per channel, a deep buffer for trigger latency and window-selected read-out, TARGET-C is ideally suited for developing readout systems with thousands of channels.

The triggering task is performed by a specific ASIC (T5TEA), which implements the analog sum of the input signals in four independent groups of four adjacent channels, comparing the sums to a user-defined threshold and providing four differential outputs.

Concerning TARGET-C, the main blocks are analog sampling and storage buffers, and Wilkinson ADC for digitizing the signals as shown in Figure 1.

The sampling and storage of signals are done using switched capacitor arrays where the signal is connected sequentially to the capacitors via analog switches. The sampling array consists of two blocks with 32 cells (capacitors) operated in ping-pong mode: while data sampling is performed by one block, the other block is buffered to the storage array. In contrast, the storage array consists of a larger number of cells (16384 per channel) to guarantee a large buffer depth ( $\sim 16\mu\text{s}$ ). Wilkinson ADCs are used for digitizing the analog signals in the storage array on demand. The Wilkinson ramp generator passes an adjustable ramp to all channels and simultaneously a 12-bit counter starts counting until the ramp signal crosses the analog voltage. The measured counts then correspond to the value of the applied signal. The digitization is initiated by a request from the FPGA based on external or internal (i.e. from T5TEA) signals.

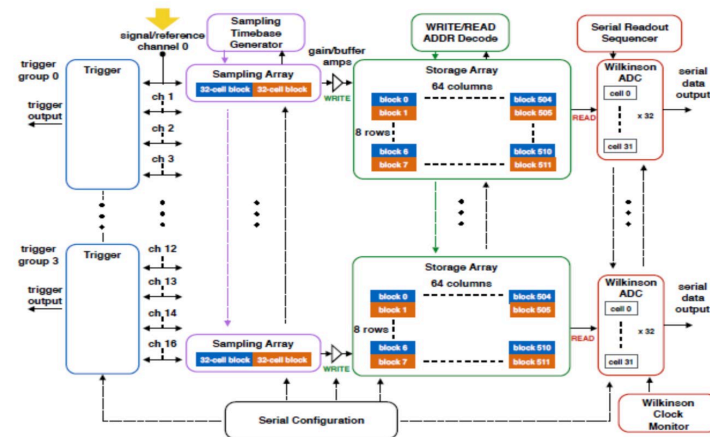


Figure 1: main functional block of TARGET-C: 16 channels capable of sampling 16 analog channel in parallel and storing them into a storage array 16384 cells width to guarantee a large buffer depth of about  $16\mu\text{s}$ .

The main features of TARGET-C and T5TEA are reported in table 1.

TABLE 1

| Characteristics                  | TARGET-C + T5TEA |
|----------------------------------|------------------|
| Number of Channels               | 16               |
| Sampling frequency (Gsample/s)   | 0.5 - 1          |
| Size of storage array            | 16384            |
| Digitization clock speed (MHz)   | 500              |
| Samples digitized simultaneously | 32x16            |
| Trigger (sum of 4 channels)      | T5TEA            |
| <b>Performance</b>               |                  |
| Dynamic Range (V)                | $\geq 1.9$       |
| Integrated non-linearity (mV)    | $\leq 70$        |
| Minimum trigger threshold (mV)   | $\leq 8$         |
| Trigger noise (mV)               | $\leq 1$         |

### 3. FRONT END ELECTRONICS MODULE: ARCHITECTURE AND STRATEGY

New FEEM module has been developed based on an existing prototype designed originally for the GCT camera [7]. In this version, FEEM is compliant with both GCT and SCT camera requirements, and so it can feature flexibility and low cost per channel; that is one of the most important features for the CTA observatory.

Mainly, FEEM is divided into two submodules, called Primary (PRIM) and Auxiliary (AUX). Each one houses two TARGET-C and two T5TEA, for a total of 64 channels that can be read simultaneously (32 channels per submodule). The submodules are stacked up together and connected via three connectors, as shown in Figure 2.

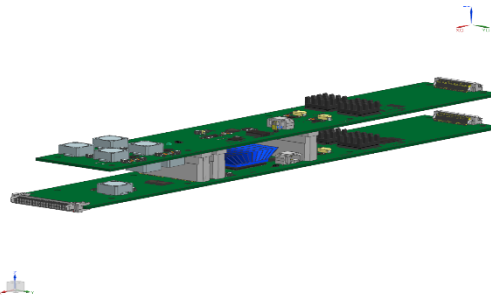


Figure 2: PRIMARY and AUXILIARY submodules connected together to realize a FEEM.

The underlying strategy to use two submodules is to have a well-separated area for analog and digital/power circuitries, avoiding of picking up noise due to the long path of each analog channel. Lastly, the dimensions of a single submodule are smaller than 274 mm length and 46 mm width, so allowing a compact camera for installation in the telescope (each camera for GCT or SCT is composed of about two thousands of channels to be read-out). Hence, a combined module of two submodules is necessary to comply with all requirements. Once the submodules are stacked up, they are encapsulated in a metallic cage that is used as a structure to protect the submodules and to which to attach the photosensor matrix.

### 4. PRIMARY Submodule

PRIM submodule houses two T5TEA and two TARGET-C chips, so that up to 32 analog channels can be digitized and stored in parallel.

A Xilinx Artix-7 FPGA (XC7A100T-FGG484) is embedded, which is responsible for setting-up TARGET-C and T5TEA chips, these require a complex setting operation to be ready to trigger

(T5TEA), sample and store (TARGET-C) data coming from the analog connector. Furthermore, the FPGA retrieves the digitized data and formats and sends them – via Gbit Ethernet, through the backplane connector, that is used to insert single FEEM in the main backplane that gathers all the data coming from all FEEMs.

Also, FPGA sets-up a custom ASIC for the pre-amplification task. These custom ASICs are mounted in an external board closer to the photosensors. FPGA interfaces with the ASIC via an SPI port.

Since the photosensors used are silicon-photomultipliers that have to be cooled and temperature stabilized around 25 degrees, a Peltier cell was developed, which is housed on the Auxiliary submodule. The main blocks of the Peltier cell are a microcontroller and an ADC that are controlled by the FPGA.

## 5. AUXILIARY Submodule

AUX submodule houses two T5TEA and two TARGET-C chips, so that up to 32 analog channels can be digitized and stored in parallel. On the bottom side, three connectors are placed to stack up AUX submodule with PRIM one. On the top right side are all the circuits devoted to the power supplies; this area is well-isolated from all the area (on the left) that is concerned by the analogue paths.

## 6. Conclusion

A new FEEM has been designed and is compliant with both GCT and SCT cameras for the Cherenkov Telescope Array. The first prototypes have been tested in the laboratory.

The first prototypes to be installed in the SCT camera will be delivered at the end of May 2020 and will be tested to deliver the full production before July 2020.

First FEEMs in the SCT camera (about 20 modules) are foreseen to be installed in September of 2020 in an SCT telescope.

## 7. Acknowledgments

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