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Development of methodology and implementation of SoC-based compact single-board validation system for the ATLAS Phase-II level-0 muon trigger system

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ABSTRACT: Firmware testing on actual hardware is an optimal way to validate large-scale FPGA-based trigger/DAQ systems. For the Phase-II level-0 muon trigger system at the ATLAS experiment, a methodology using prototype ATCA-based Sector Logic (SL) boards was developed, featuring self-complete DAQ, high-statistics test patterns, and various nature of input test data. The design exploits Zynq SoC on the board for control, injection of BRAM-based test patterns data and flexible DAQ to probe the process. This success is thanks to the flexibility of the SL board design around the SoC device. This methodology facilitates precise firmware validation and systematic debugging.

KEYWORDS: Data acquisition concepts; Simulation methods and programs; Trigger concepts and systems (hardware and software); Performance of High Energy Physics Detectors

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1 Introduction

In high-energy particle physics experiments, the Trigger and DAQ (TDAQ) system plays a crucial role in maximizing the overall performance of the experiment. With advancements in integrated circuit technology, TDAQ systems have become increasingly sophisticated and complex in recent years. To ensure accurate implementation and achieve optimal TDAQ performance, the development of a detailed and comprehensive hardware-based validation system is essential. In response to these challenges, we have designed and implemented an MPSoC¹-based validation system for the **Thin Gap Chamber (TGC)** system in the ATLAS experiment [1, 2] at the HL-LHC [3]. These new concepts for the validation system fully leverage the flexibility the SoC provides. Features such as timing control, pseudo data injection, register control, and readout can be naturally integrated around the MPSoC, enabling a standalone single-board validation system with full functionality. This approach significantly simplifies the setup compared to traditional systems. For instance, a conventional test system for full functionality validation typically requires additional components, such as a separate control master (e.g., a Single Board Computer for the VME master) and an external readout system. Furthermore, the availability of large-scale test pattern injection for various purposes is a unique feature of this new idea. In conventional systems, only extremely simple data patterns could be used as input for testing with actual hardware systems. In contrast, by implementing a system to generate test patterns from various datasets — such as Monte Carlo simulation data, collision data, and toy data emulating infinite-momentum straight tracks — we have made it possible to evaluate trigger responses against more realistic track patterns.

The operation of the ATLAS detector at HL-LHC will begin in 2030 for precision measurements of the Standard Model and to search for new physics with high statistics. The peak luminosity will be tripled, with the first stage (Level-0, L0) trigger rate expanded to 1 MHz and the trigger latency extended to 10 μ s [4]. To handle the increased collision rate and L0 trigger rate, the readout and trigger electronics of the TGC will be upgraded [5].

The TGC trigger electronics in HL-LHC will mainly consist of two front-end boards and one back-end board, as shown in figure 1(a). The charge signal generated in the TGC chamber is amplified, shaped, and discriminated on the **Amplifier-Shaper-Discriminator (ASD)** boards, which are mounted on the TGC detectors. The **Patch-Panel ASIC** and **Sender FPGA (PS)** board collects these signals, assigns rising edges to a corresponding bunch crossing, and sends a 256-bit hit-bitmap to the **Endcap Sector Logic (Endcap SL)** every 25 ns. The Endcap SL plays three roles: triggering, readout, and control. For triggering, it reconstructs muon tracks and estimates their transverse momentum (p_T) through layer coincidences of TGC hits. For readout, it retrieves hit data and the results of the trigger

¹In this study, a type of SoC with multiple processors (MPSoC) is adopted.

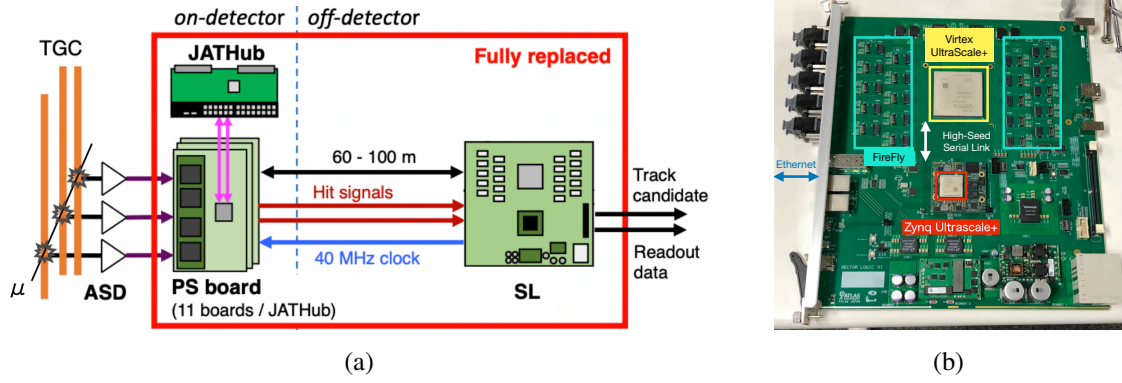


Figure 1. Overview of the TGC Phase-II electronics system. 1(a) shows the schematics of the TGC electronics. 1(b) shows the picture of the Endcap SL board.

calculation and conducts local event building for triggered events, and transmits this information via an optical link to the central readout system. For control, it distributes timing signals to the front-end board, and conducts electronics configuration and monitoring.

The SL is an ATCA blade equipped with high-bandwidth optical I/O (Samtec FireFly), a Virtex UltraScale+ FPGA (XC7VU13P-1FLGA2577E), and a Zynq UltraScale+ MPSoC (XC7ZU5EV-2SFVC784I), as illustrated in figure 1(b). The FPGA plays a central role. It consists of four silicon chips and is equipped with high-performance multi-gigabit SERDES transceivers (GTY) distributed across 32 quad banks for efficient data transfer. The MPSoC interfaces with the TDAQ systems via Ethernet and serves as the control master for the Virtex UltraScale+ FPGA and the PS boards. It also includes high-performance multi-gigabit SERDES transceivers (GTH) for communication with the Virtex UltraScale+ FPGA.

2 L0 endcap muon trigger and its validation system

Trigger algorithm. The TGC chambers consist of seven layers, which are grouped into three super-layers (stations): M1 (three layers), M2 (two layers), and M3 (two layers), located at $z = 13, 14, 14.5$ m, respectively (figure 2(a)). Muons originating from the interaction point (IP) are deflected in the toroidal magnetic field, and their momentum is estimated using point-angle measurements. These measurements rely on the observables $(\Delta\phi, \Delta\theta)$, defined as the difference between the reconstructed trajectories and the straight-line tracks connecting space points on the pivot station (M3) and the interaction point, as illustrated in figure 2(a). Look-up tables (LUTs) then map the $(\Delta\phi, \Delta\theta)$ observables to an estimate of the transverse momentum.

Integrated validation framework. To ensure that the trigger logic is accurately implemented in the FPGA, we have designed and implemented an integrated trigger validation system (figure 2(b)). This system consists of three main tools: 1. test vector generator, 2. single-board test system, and 3. bitwise simulator.

The test vector generator is a software tool designed to generate pseudo-test input bitstreams. These test vectors are based on Monte Carlo simulation data of realistic muon trajectories or toy data that emulates infinite straight-line tracks. A relational database is embedded to store cabling

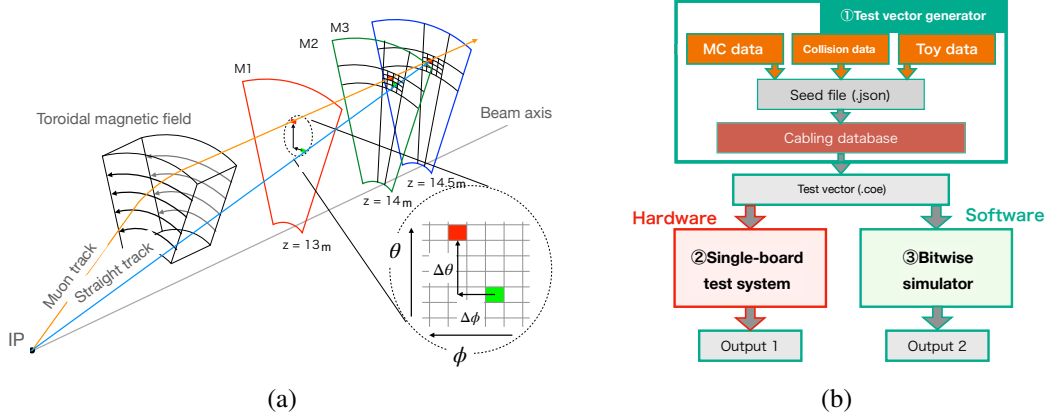


Figure 2. Overview of the trigger algorithm and validation system. 2(a) is a conceptual illustration of the muon trigger algorithm. 2(b) shows the overall design of the trigger validation system.

information from the front-end boards to the back-end SL, enabling the tool to map individual TGC hits from the original datasets to bit assertions in the pseudo input data. Thanks to this tool, seamless integration between software layers and hardware testing is achieved. This allows for the evaluation of trigger responses to arbitrary track patterns, regardless of the origin of the test vectors.

The single-board test system is an MPSoC-based validation platform that runs the trigger logic using test vectors as input on actual hardware. The input and output data are packaged into event data and recorded by a local readout system implemented within the MPSoC device.

The bitwise simulator is a software tool that fully emulates the trigger logic with bitwise precision. The input and output data formats are designed to match exactly those of the hardware. By processing identical input data through the hardware and the simulator and comparing the consistency of their outputs, comprehensive, efficient, and detailed validation of the trigger system is achieved.

Implementation of single-board test system. Figure 3 shows the schematic of the single-board test system. In addition to the main trigger logic, the system includes a timing controller to manage the test pulse trigger and Level-0 Accept (L0A) signal, as well as test vector injectors that provide pseudo data synchronized with the test pulse trigger. The readout path has been modified to enable a single-board readout system via the MPSoC, which runs Linux and is directly connected to the programmable logic. In this setup, the MPSoC also acts as the master for control. Tests are conducted through the following steps.

1. The MPSoC writes the test vector into the BRAM equipped with the test vector injector.
2. The timing controller generates the test pulse trigger as a single clock tick pulse synchronized with the 40 MHz clock.
3. The test vector injector feeds test vectors, consisting of 7,936 bits, into the trigger logic.
4. The trigger output is stored in the buffer (L0 buffer). The timing controller generates the L0A signal, a single clock tick pulse, with a defined delay relative to the test pulse trigger, emulating the fixed latency of the L0 logic. Upon receiving the L0A, the corresponding data — including the output from the test vector injection — is transferred to the MPSoC and stored in the BRAM on the programmable logic. The software running on the MPSoC's processing system can then access the stored data in the BRAM for readout.

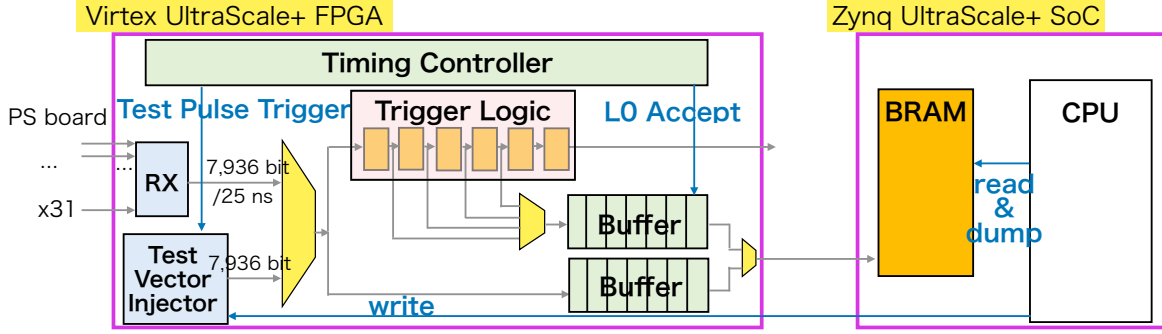


Figure 3. Block diagram of single-board test system.

This test system is designed to quickly process large datasets while also enabling detailed firmware debugging. The timing controller emulates the role of the Central Trigger Processor and Trigger Timing Controller systems [1], generating timing signals such as the test pulse trigger and L0A signals as described above. The L0A signals are produced after a set latency period following the test pulse trigger, reflecting the L0 latency. The depth of the L0 buffer is fixed and configured to correctly read out the appropriate bunch crossing data, taking into account the latency of the trigger logic and the interval between the test pulse trigger and the L0A signals. The test vector injector stores 7,936-bit test vectors in the BRAM and injects them simultaneously as a single bunch crossing data, synchronized with the test pulse trigger signal. The BRAM has a depth of 60, corresponding to 60 events, and can be repeatedly updated by the MPSoC CPU, enabling high-statistics testing. Trigger data readout allows for verifying both final and intermediate results, primarily for debugging purposes. The trigger readout selector can switch between outputs from various trigger modules. The L0 buffer depth is configured with specific values to read data at each stage of the trigger calculation, enabling confirmation of correct data retrieval for each L0A. This setup also ensures the trigger logic functions with the expected latency at every step. For inter-chip communication, two bi-directional serial links (16.08 Gbps) are established: one for the control and the other for the readout functionalities.

3 Trigger performance evaluation using single-board test system

We have successfully designed and implemented the single-board test system and put it into practical use. As an example of its application, the system has been utilized to evaluate the performance of the trigger logic, including the assessment of trigger efficiency, by running a chain of algorithms on Monte Carlo simulation data for realistic muon trajectories. The trigger efficiency derived from high-statistics Monte Carlo data has proven to be a reliable metric for assessing firmware quality, as well as for its validation and debugging. It takes approximately one minute to process 100,000 events, demonstrating the system's ability to efficiently analyze large datasets. Figure 4 (black points) shows the trigger efficiency as a function of the truth-level p_T of the muons in the pseudorapidity range of $2.0 < |\eta| < 2.35$, with a 5 GeV p_T threshold for 500,000 simulated muons. The plot indicates a high efficiency, as expected, with the efficiency about 94% at the plateau of the efficiency curve, demonstrating a good level of maturity in the trigger algorithm development.

Additionally, the figure shows performance improvements by comparing the online muon reconstruction efficiency between two different firmware versions used for refining the LUTs. Initially,

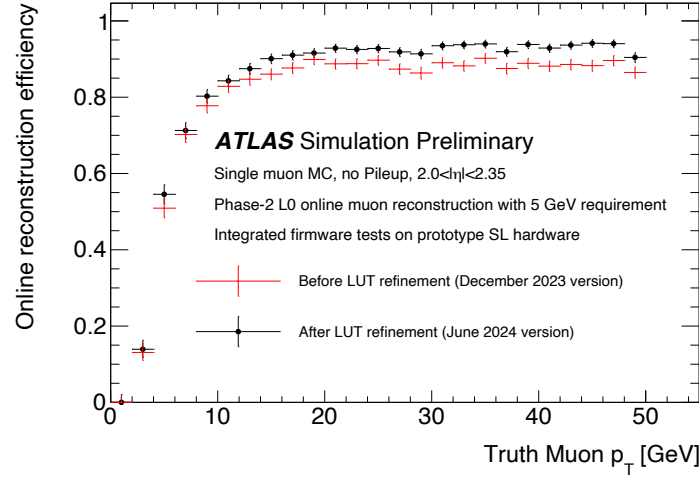


Figure 4. The trigger efficiency of the L0 endcap muon trigger [6]. This was measured using a single-board test system and a single-muon Monte Carlo data. Reproduced with permission from [6].

it was observed that the efficiency was lower than the expected value from the simulation, which was approximately 94%. A detailed investigation of the test vector and comparison between expected outputs and observed outputs allowed us to identify the issues in the logic and LUTs. As this example shows, this test system is useful not only for checking the performance but also for debugging.

4 Conclusion

To achieve the optimal TDAQ system, it is essential to establish a detailed and comprehensive validation system using actual hardware. One solution we have developed is the SoC-based single-board test system. This system allows us to process a sufficient amount and variety of datasets. By monitoring the trigger outputs or intermediate outputs and comparing them with input data or simulations, we can verify that the logic circuits are correctly implemented. We have completed the design and implementation of this test system for the Phase-II TGC Endcap SL and are now fully utilizing it in studies aimed at maximizing trigger performance. Moreover, the validation methods and implementation techniques used in this system are widely applicable to other electronic systems incorporating SoC devices.

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